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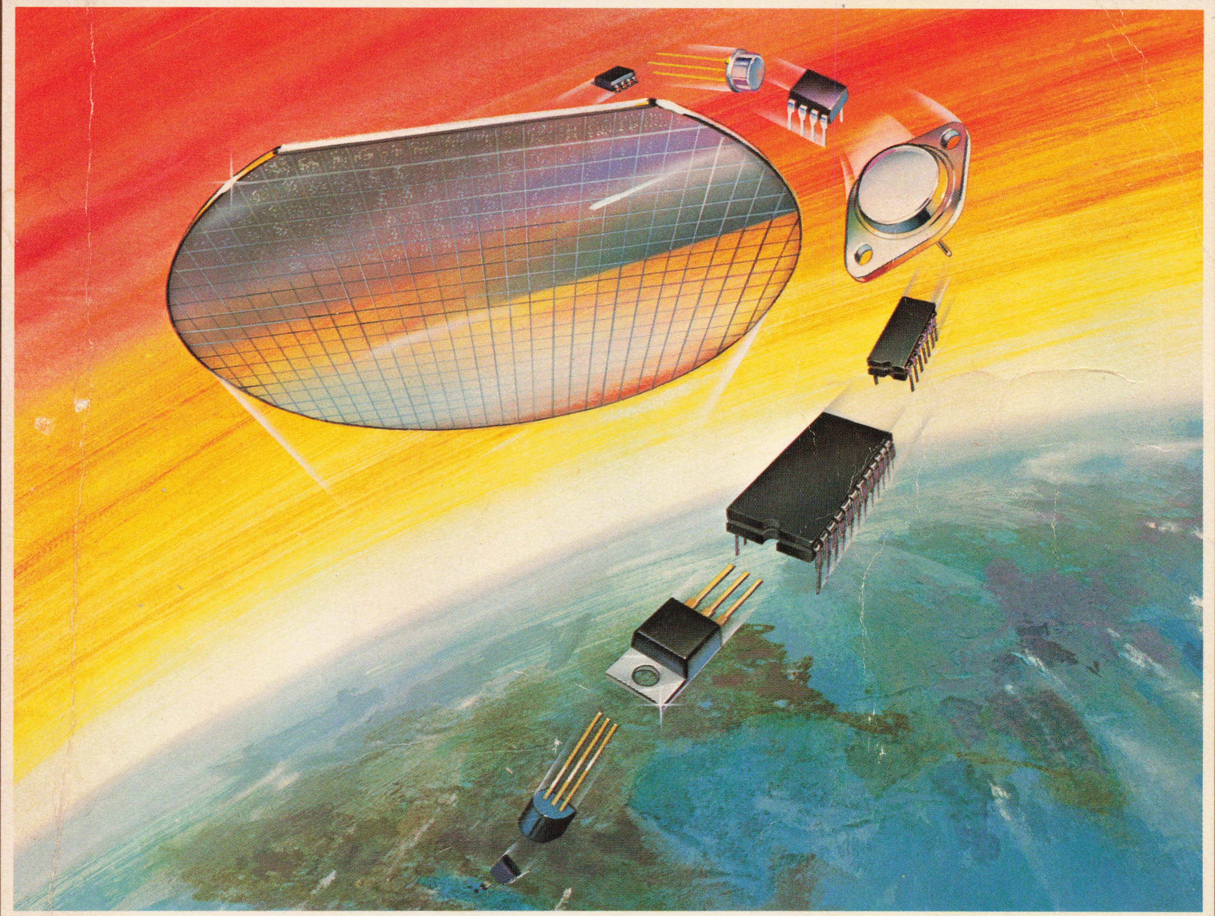
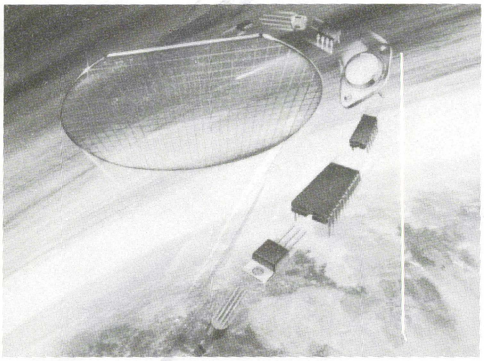


LINEAR AND INTERFACE INTEGRATED CIRCUITS



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MOTOROLA

LINEAR/INTERFACE INTEGRATED CIRCUITS

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of data sheets which are categorized by product type into nine chapters for easy reference. Selector guides by product family are provided in Chapter 2 to enable quick comparisons of performance characteristics. A cross-reference chapter lists Motorola direct replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate package outline and mounting hardware drawings, and includes information on the new Surface Mounted (SMD), Small Outline Integrated Circuit (SOIC) packages.

Additionally, chapters are provided with information on quality program concepts, high-reliability processing, and abstracts of available technical literature.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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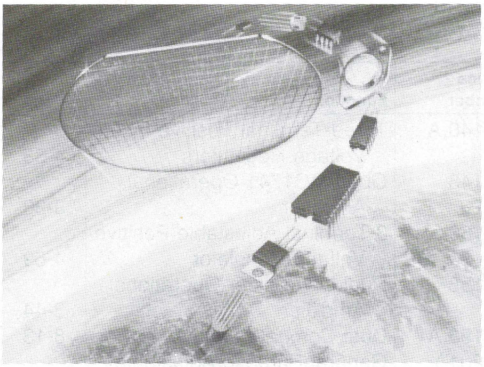

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Cross Reference

A complete interchangeability list linking over 3000 devices are offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Similar Replacement" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

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6605L		MC3443P
8216		MC8T26AL
8226		MC8T28L
9614DC		MC75S110L
9614DM		MC75S110L
9615DC		MC75108L
9615DM		MC55108L
9615FM		MC55108L
9616CDC		MC1488L
9616EDC		MC1488L
9616DM		MC1488L
9617DC		MC1489AL
9620DC		MC75S110L
9620DM		MC75S110L
9621DC		MC75108L
9621DM		MC55108L
9627CDC		MC1489AL
9627DM		MC1489AL
9636AT	MC3488AP	
9637T		MC3486P
9638T		MC3487P
9640D		MC3443P
9640DC	MC26S10L	
9640NC	MC3440AP	
9640PC	MC26S10P	
9641DC	MC26S11L	
9641PC	MC26S11P	
9665DC	MC1411L	
9665PC	MC1411P	
9666DC	MC1412L	
9666PC	MC1412P	
9667DC	MC1413L	
9667PC	MC1413P	
9668DC	MC1416L	
9668PC	MC1416P	
55107ADM	MC55107L	
55107BDM		MC55107L
55108ADM	MC55108L	
55108BDM		MC55108L
55110DM		MC75S110L
55207DM		MC55107L
55208DM		MC55108L
75107ADC	MC75107L	
75107APC	MC75107P	
75107BDC		MC75107L
75107BPC		MC75107P
75108ADC	MC75108L	
75108APC	MC75108P	
75108BDC		MC75108L
75108BPC		MC75108P
75110DC	MC75S110L	
75110PC	MC75S110P	
75207DC		MC75107L
75207PC		MC75107P
75208DC		MC75108L
75208PC		MC75108P
AD DAC-08AD	DAC-08AQ	
AD DAC-08CD	DAC-08CQ	
AD DAC-08D	DAC-08Q	
AD DAC-08ED	DAC-08EQ	
AD DAC-08HD	DAC-08HQ	
AD301AL		LM301AH
AD505J		MC1776CG
AD505K		MC1776CG
AD505S		MC1776G
AD509J		LM301AH
AD509K		LM301AH
AD509S		LM101AH
AD518J		LM301AH
AD518K		LM301AH
AD518S		LM101AH
AD530		MC1595L
AD531		MC1595L
AD532J		MC1595G
AD562AD	AD562AD	
AD562KD	AD562KD	
AD562SD	AD562SD	
AD563JD	AD563JD	
AD563KD	AD563KD	
AD563SD	AD563SD	
AD563TD	AD563TD	
AD565JD	MC3412L	
AD565KD		MC3412L
AD565SD	MC3512L	
AD565TD		MC3512L
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD589J		LM385Z-1.2
AD589K		LM385Z-1.2
AD589L		LM385Z-1.2
AD589M		LM385BZ-1.2
AD741CJ		MC1741CG
AD741J		MC1741G
AD741K		MC1741G
AD741L		MC1741G
AD741S		MC1741SG
AD1403AN		MC1403AU
AD1403N	MC1403U	
AD1408-7D	MC1408L7	
AD1408-8D	MC1408L8	
AD1508-8D	MC1508L8	
AD7520D		MC3410L
AD7520F		MC3410L
AD7520N		MC3410L
AM26LS31CJ	AM26LS31DC	
AM26LS31CN	AM26LS31PC	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
AM26LS31D	AM26LS31D	
AM26LS31P	AM26LS31P	
AM26LS32ACJ	AM26LS32ADC	
AM26LS32ACN	AM26LS32APC	
AM26LS32D	AM26LS32D	
AM26LS32P	AM26LS32P	
AM26S10DC	MC26S10L	
AM26S10PC	MC26S10P	
AM26S11DC	MC26S11L	
AM26S11PC	MC26S11P	
AM101	LM101AH	
AM101A	LM101AH	
AM101AD		LM101AH
AM101AF		LM101AH
AM101D		LM101AH
AM101F		LM101AH
AM107	LM107H	
AM107D		LM107H
AM107F		LM107H
AM111D	LM111J	
AM111H	LM111H	
AM201	LM201AH	
AM201A	LM201AH	
AM201AD		LM201AN
AM201AF		LM201AH
AM201D		LM201AN
AM201F		LM201AH
AM207	LM207H	
AM207D		LM207H
AM207F		LM207H
AM211D	LM211J	
AM211H	LM211H	
AM301	LM301AH	
AM301A	LM301AH	
AM301AD		LM301AJ
AM301D		LM301AJ
AM311D	LM311J-8	
AM311H	LM311H	
AM592DC	NE592F	
AM592DM	SE592F	
AM592HC	NE592K	
AM592HM	SE592K	
AM592PC	NE592N	
AM723DC	MC1723CL	
AM723DM	MC1723L	
AM723HC	MC1723CG	
AM723HM	MC1723G	
AM723PC	MC1723CP	
AM725HM	MC1556G	
AM733DC	MC1733CL	
AM733DM	MC1733L	
AM733HC	MC1733CG	
AM733HM	MC1733G	
AM741DC		MC1741CU
AM741DM		MC1741U
AM741HC	MC1741CG	
AM741HM	MC1741G	
AM747DC	MC1747CL	
AM747DM	MC1747L	
AM747HC	MC1747CG	
AM747HM	MC1747G	
AM748DC		MC1748CU
AM748DM		MC1748U
AM748HC	MC1748CG	
AM748HM	MC1748G	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
AN5150		MC13002P
AN5151		MC13001P
CA081AE		TL081ACP
CA081AS		TL081ACJG
CA081BE		TL081BCP
CA081CS		TL081CJG
CA081E		TL081CP
CA081S		TL081MJG
CA082AE		TL082ACP
CA082AS		TL082ACJG
CA082BE		TL082BCP
CA082CS		TL082CJG
CA082E		TL082CP
CA082S		TL082MJG
CA084AE		TL084ACN
CA084E		TL084CN
CA084S		TL082MJ
CA101AT	LM101AH	
CA101T	LM101AH	
CA107T	LM107H	
CA108AS	LM108AJ-8	
CA108AT	LM108AH	
CA108S	LM108J-8	
CA108T	LM108H	
CA139AG	LM139AJ	
CA139G	LM139J	
CA201AT	LM201AH	
CA201T		LM201AH
CA207T	LM207H	
CA208AT	LM208AH	
CA208S	LM208J-8	
CA208T	LM208H	
CA239AE	LM239AN	
CA239AG	LM239AJ	
CA239E	LM239N	
CA239G	LM239J	
CA301AT	LM301AH	
CA307T	LM307H	
CA308AS	LM308N	
CA308AT	LM308AH	
CA308S	LM308H	
CA339AE	LM339AN	
CA339AG	LM339AJ	
CA339E	LM339N	
CA339G	LM339J	
CA723CE	MC1723CP	
CA723CT	MC1723CG	
CA723E	MC1723L	
CA723T	MC1723G	
CA741CS	MC1741CP1	
CA741CT	MC1741CG	
CA741S	MC1741U	
CA741T	MC1741G	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747CT	MC1747CG	
CA747E	MC1747L	
CA747F	MC1747L	
CA747T	MC1747G	
CA748CS	MC1748CP1	
CA748CT	MC1748CG	
CA748S	MC1748U	
CA748T	MC1748G	
CA758E	μA758A	
CA1190		TDA1190Z

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
CA1310E	MC1310P	
CA1352E	MC1352P	
CA1391E	MC1391P	
CA1394E	MC1394P	
CA1458S	MC1458CP1	
CA1458T	MC1458G	
CA1558S		MC1558U
CA1558T	MC1558G	
CA2111AE	MC1357P	
CA3000		MC1550G
CA3001		MC1550G
CA3002		MC1550G
CA3004		MC1550G
CA3005		MC1550G
CA3006		MC1550G
CA3007		MC1550G
CA3008		MC1709U
CA3008A		MC1709U
CA3010		MC1709G
CA3010A		MC1709G
CA3011		MC1590G
CA3012		MC1590G
CA3013		MC1357P
CA3014		MC1357P
CA3015		MC1709G
CA3015A		MC1709G
CA3016		MC1709U
CA3016A		MC1709F
CA3020		MC1554G
CA3020A		MC1454G
CA3021		MC1590G
CA3022		MC1590G
CA3023		MC1590G
CA3026		CA3054
CA3028A		MC1550G
CA3028AF		MC1550G
CA3028AS		MC1550G
CA3028B		MC1550G
CA3028BF		MC1550G
CA3028BS		MC1550G
CA3029		MC1709P1
CA3029A		MC1709P1
CA3030		MC1709P1
CA3030A		MC1709P1
CA3031		MC1712G
CA3032		MC1712CG
CA3035		MC1352P
CA3035V1		MC1352P
CA3037		MC1709U
CA3037A		MC1709U
CA3038		MC1709U
CA3038A		MC1709U
CA3040		MC1510G
CA3041		MC1357P
CA3042		MC1357P
CA3043		MC1357P
CA3044		MC13010P
CA3044V1		MC13010P
CA3045		MC3346P
CA3045F		MC3346P
CA3046	MC3346P	
CA3048		MC3301P
CA3052		MC3301P
CA3053		MC1550G
CA3053F		MC1550G
CA3053S		MC1550G
CA3054	CA3054	
CA3056	MC1741CG	
CA3056A	MC1741G	
CA3058		CA3059
CA3059	CA3059	
CA3064		MC13010P
CA3065	MC1358P	
CA3067		MC1327P
CA3068		MC1352P
CA3072		MC1327P
CA3076		MC1590G
CA3078AS		MC1776G
CA3078AT		MC1776G
CA3078S		MC1776CG
CA3078T		MC1776CG
CA3079	CA3079	
CA3085		MC1723G
CA3085A		MC1723G
CA3085AF		MC1723L
CA3085AS		MC1723G
CA3085B		MC1723G
CA3085BF		MC1723L
CA3085BS		MC1723G
CA3085F		MC1723L
CA3085S		MC1723G
CA3086	MC3386P	
CA3086F		MC3346P
CA3090AQ		MC1310P
CA3091D		MC1594L
CA3121E		TDA3333
CA3125E		MC1327P
CA3134E		TDA1190Z
CA3134EM		TDA1190Z
CA3134QM		TDA1190Z
CA3136A		MC3346P
CA3137E		MC1327P
CA3139		MC13010P
CA3145E		TDA3333
CA3146		MC3346P
CA3151E		TDA3333
CA3201E		TDA3301
CA3210E		MC13001P
CA3217E		TDA3301
CA3221E		TDA3333
CA3223E		MC13002P
CA3302E	MC3302P	
CA3401E	MC3401P	
CA6078AS		MC1776G
CA6078AT		MC1776G
CA6741S		MC1776G
CA6741T		MC1776G
CA7607E		MC13010P
CA7611E		MC13010P
CMP-01CJ		MC1556G
CMP-01CP		MC1556P
CS3471	MC3471P	
D555CJ		MC1555G
D3242	MC3242AP	
D8216		MC8T26AL
D8226		MC8T28L
DAC-01		MC1506L
DAC-08AQ	DAC-08AQ	
DAC-08CN	DAC-08CP	
DAC-08CP	DAC-08CP	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
DAC-08CQ	DAC-08CQ	
DAC-08EN	DAC-08EP	
DAC-08EP	DAC-08EP	
DAC-08EQ	DAC-08EQ	
DAC-08HN	DAC-08HP	
DAC-08HP	DAC-08HP	
DAC-08HQ	DAC-08HQ	
DAC-08Q	DAC-08Q	
DAC-ICC10BC	MC3410L	
DAC0800LCJ	DAC-08EQ	
DAC0800LCN	DAC-08EP	
DAC0800LD	DAC-08Q	
DAC0801LCJ	DAC-08CQ	
DAC0801LCN	DAC-08CP	
DAC0802LCJ	DAC-08HQ	
DAC0802LCN	DAC-08HP	
DAC0802LD	DAC-08AQ	
DAC0806LCJ	MC1408L6	
DAC0806LCN	MC1408P6	
DAC0807LCJ	MC1408L7	
DAC0807LCN	MC1408P7	
DAC0808LCJ	MC1408L8	
DAC0808LCN	MC1408P8	
DAC0808LD	MC1508L8	
DM7822J		MC1489AL
DM7837J		MC3437L
DM7838J		MC3438L
DM7889J		MC3491L
DM7889N		MC3491L
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DM8838N	MC3438P	
DM8889J		MC3491P
DS26LS31J	AM26LS31D	
DS26LS31N	AM26LS31P	
DS26LS32J	AM26LS32D	
DS26LS32N	AM26LS32P	
DS26S10CJ	MC26S10L	
DS26S10CN	MC26S10P	
DS26S11CJ	MC26S11L	
DS26S11CN	MC26S11P	
DS1488J	MC1488L	
DS1488N	MC1488P	
DS1489AJ	MC1489AL	
DS1489AN	MC1489AP	
DS1489J	MC1489L	
DS1489N	MC1489P	
DS3486J	MC3486L	
DS3486N	MC3486P	
DS3487J	MC3487L	
DS3487N	MC3487P	
DS3612H		MC1472U
DS3612N		MC1472P
DS3632H		MC1472U
DS3632J		MC1472U
DS3632N		MC1472P1
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS7837J		MC3437L
DS7837W		MC3437L
DS7838J		MC3438L
DS7838W		MC3438L
DS7889J		MC3491L
DS8833J		MC8T28L
DS8833N		MC8T28P
DS8834J		MC8T26AL
DS8834N		MC8T26AP
DS8835J		MC8T26AL
DS8835N		MC8T26AP
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8838J	MC3438L	
DS8838N	MC3438P	
DS8839J		MC8T28L
DS8839N		MC8T28P
DS8889J		MC3491L
DS8889N		MC3491L
DS55107J	MC55107L	
DS55107W		MC75107L
DS55108J	MC55108L	
DS55108W		MC55108L
DS55110J		MC75S110L
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75110J	MC75S110L	
DS75110N	MC75S110P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC75108P
HC5501		MC3419CL
HC5502		MC3419L
HI-562-2		AD562SD
HI-562-5		AD562KD
ICB8000C		LM111J
ICB8001C		LM111J
ICB8741C		MC1741CG
ICH8500ATV		MC1776CG
ICH8500TV		MC1776CG
ICL101ALNDP		LM101AH
ICL101ALNFB		LM101AH
ICL101ALNTY		LM101AH
ICL301ALNPA		LM301AH
ICL301ALNTY		LM301AH
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL8001CTZ		LM111J
ICL8001MTZ		LM111J
ICL8007CTA		MC1709CG
ICL8007MTA		MC1709CG
ICL8008CPA		LM301AN
ICL8008CTY		LM301AN
ICL8013A		MC1594G
ICL8013B		MC1594G
ICL8013C		MC1594G
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8021C		MC1776G
ICL8021M		MC1776G
ICL8022C		MC1776G
ICL8022M		MC1776G

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ICL8043CDE		MC1776G
ICL8043CPE		MC1776G
ICL8043MDE		MC1776G
ICL8048CDE		MC1776G
ICL8048DPE		MC1776G
ICL8069CCZR		LM385BZ-1.2
ICL8069DCZR		LM385Z-1.2
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
ITT1330	MC1330P	
ITT1352	MC1352P	
ITT3064	MC13010P	
ITT3065	MC1358P	
ITT3701		TDA1190Z
ITT3710		MC1391P
ITT3714		MC1394P
L144AP		LM324N
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
L583		MC3484V2
LF347BN	LF347BN	
LF347N	LF347N	
LF351AH	MC34001AG	
LF351AN	MC34001AP	
LF351BH	MC34001BG	
LF351BN	MC34001BP	
LF351H	MC34001G	
LF351N	LF351N	
LF352D		LF355J
LF353AH	MC34002AG	
LF353AN	MC34002AP	
LF353BH	MC34002BG	
LF353BN	MC34002BP	
LF353H	MC34002G	
LF353N	LF353N	
LF355AH		
LF355AJG		
LF355AL		
LF355AP		
LF355BH	LF355BH	
LF355BJ	LF355BJ	
LF355BN	LF355BN	
LF355H	LF355H	
LF355JG	LF355J	
LF355L	LF355H	
LF355N	LF355N	
LF355P	LF355N	
LF356AH		
LF356AL		
LF356AJG		
LF356AP		
LF356BH	LF356BH	
LF356BJ	LF356BJ	
LF356BN	LF356BN	
LF356H	LF356H	
LF356JG	LF356J	
LF356L	LF356H	
LF356N	LF356N	
LF356P	LF356N	
LF357AH		
LF357BH	LF357BH	
LF357BJ	LF357BJ	
LF357BN	LF357BN	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LF357H	LF357H	
LF357JG	LF357J	
LF357L	LF357H	
LF357N	LF357N	
LF357P	LF357N	
LF411CH		MC34001AG
LF411CN		MC34001AP
LF412CH		MC34002AG
LF412CN		MC34002AP
LH0002CH		MC1538R
LH0002H		MC1538R
LH0004CH		MC1436G
LH0004H		MC1536G
LH0042CH		MC34001BG
LH740ACH		LF355H
LH2101AD		MC1537L
LH2101AF		MC1537L
LH2201AD		MC1537L
LH2201AF		MC1537L
LH2301AD		MC1437L
LH2301AF		MC1437L
LM11CH	LM11CH	
LM11CJ	LM11CJ	
LM11CJ-8	LM11CJ-8	
LM11CLH	LM11CLH	
LM11CLJ	LM11CLJ	
LM11CLJ-8	LM11CLJ-8	
LM11CLN	LM11CLN	
LM11CLN-14	LM11CLN-14	
LM11CN	LM11CN	
LM11CN-14	LM11CN-14	
LM11H	LM11H	
LM11J	LM11J	
LM11J-8	LM11J-8	
LM101AD		LM101AH
LM101AF		LM101AH
LM101AH	LM101AH	
LM101AJ		LM101AJ
LM101AJ-14		LM101AJ
LM101AJG	LM101AJ	
LM101AL	LM101AH	
LM101D		LM101AJ
LM101F		LM101AH
LM101H	LM101AH	
LM101J-14		LM101AJ
LM106H		MC1710G
LM107F		LM107H
LM107H	LM107H	
LM107L	LM107H	
LM108AD	LM108AJ	
LM108AF	LM108AF	
LM108AH	LM108AH	
LM108AJ	LM108J-8	
LM108D	LM108J	
LM108F	LM108F	
LM108H	LM108H	
LM109H	LM109H	
LM109K	LM109K	
LM109LA	LM109H	
LM111D		
LM111H		
LM111J	LM111J	
LM111JG	LM111J-8	
LM112D		MC1556L
LM112F		MC1556L

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM112H		MC1556G
LM117H	LM117H	
LM117K	LM117K	
LM117LA	LM117H	
LM118D		MC1741SU
LM118F		MC1741SU
LM118H		MC1741SG
LM120H-5.0		MC7905CK
LM120H-5.2		MC7905.2CK
LM120H-12		MC7912CK
LM120H-15		MC7915CK
LM120K-5.0		MC7905CK
LM120K-5.2		MC7905.2CK
LM120K-12		MC7912CK
LM120K-15		MC7915CK
LM122F		MC1555G
LM122H		MC1555G
LM123K	LM123K	
LM124AD		LM124J
LM124AF		LM124J
LM124AJ		LM124J
LM124D	LM124J	
LM124F		LM124J
LM124J	LM124J	
LM125H		MC1568G
LM126H		MC1568G
LM128H		MC1568G
LM137K	LM137K	
LM139AD	LM139AJ	
LM139AJ	LM139AJ	
LM139D	LM139J	
LM139J	LM139J	
LM140AK-5.0	LM140AK-5.0	
LM140AK-12	LM140AK-12	
LM140AK-15	LM140AK-15	
LM140K-5.0	LM140K-5.0	
LM140K-12	LM140K-12	
LM140K-15	LM140K-15	
LM140LAH-5.0		MC78L05ACG
LM140LAH-6.0		MC78L06ACG
LM140LAH-8.0		MC78L08ACG
LM140LAH-12		MC78L12ACG
LM140LAH-15		MC78L15ACG
LM140LAH-18		MC78L18ACG
LM140LAH-24		MC78L24ACG
LM143D		MC1536G
LM143F		MC1536G
LM143H		MC1536G
LM145K		MC7905CK
LM148D	LM148J	
LM148J	LM148J	
LM148F		MC4741L
LM149D		MC4741L
LM149F		MC4741L
LM150K	LM150K	
LM158AH		LM158H
LM158H	LM158H	
LM158JG	LM158J	
LM158L	LM158H	
LM171H		MC1590G
LM193AH	LM193AH	
LM193H	LM193H	
LM201AD		LM201AJ
LM201AF		LM201AH
LM201AH	LM201AH	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM201AJ		LM201AJ
LM201AJG	LM201AJ	
LM201AJ-14		LM201AJ
LM201AL	LM201AH	
LM201AN		LM201AN
LM201AP	LM201AN	
LM201D		LM201AJ
LM201F		LM201AH
LM201H	LM201AH	
LM201J	LM201AJ	
LM201J-14		LM201AJ
LM206H		MC1710CG
LM207F		LM207H
LM207H	LM207H	
LM208AD	LM208AJ	
LM208AF	LM208AF	
LM208AH	LM208AH	
LM208AJ	LM208AJ-8	
LM208D		LM208J-8
LM208F	LM208J-8	
LM208H	LM208H	
LM209H	LM209H	
LM209K	LM209K	
LM209LA	LM209H	
LM211D	LM211J	
LM211H	LM211H	
LM211JG	LM211J-8	
LM212D		MC1556L
LM212F		MC1556L
LM212H		MC1456G
LM217H	LM217H	
LM217K	LM217K	
LM217KC		LM217K
LM217KD		LM217H
LM217LA	LM217H	
LM218D		MC1741SU
LM218F		MC1741SU
LM218H		MC1741SG
LM220H-5.0		MC7905CK
LM220H-5.2		MC7905.2CK
LM220H-6.0		MC7906CK
LM220H-8.0		MC7908CK
LM220H-12		MC7912CK
LM220H-15		MC7915CK
LM220H-18		MC7918CK
LM220H-24		MC7924CK
LM220K-5.0		MC7905CK
LM220K-5.2		MC7905.2CK
LM220K-6.0		MC7906CK
LM220K-8.0		MC7908CK
LM220K-12		MC7912CK
LM220K-15		MC7915CK
LM220K-18		MC7918CK
LM220K-24		MC7924CK
LM222H		MC1555G
LM223K	LM223K	
LM224AD		LM224J
LM224AF		LM224J
LM224AJ		LM224J
LM224D	LM224J	
LM224F		LM224L
LM224J	LM224J	
LM225H		MC1568G
LM226H		MC1568G
LM228H		MC1568G

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM237K	LM237K	
LM239AD	LM239AJ	
LM239AJ	LM239AJ	
LM239D	LM239J	
LM239J	LM239J	
LM239N	LM239N	
LM240LAH-5.0		MC78L05ACG
LM240LAH-6.0		MC78L06CG
LM240LAH-8.0		MC78L08ACG
LM240LAH-12		MC78L12ACG
LM240LAH-15		MC78L15ACG
LM240LAH-18		MC78L18ACG
LM240LAH-24		MC78L24ACG
LM240LAZ-5.0		MC78L05ACP
LM240LAZ-6.0		MC78L06ACP
LM240LAZ-8.0		MC78L08ACP
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM243H		MC1536G
LM245K		MC7905CK
LM248D	LM248J	
LM248J	LM248J	
LM249D		MC4741L
LM249J		MC4741L
LM250K	LM250K	
LM258AH		LM258H
LM258H	LM258H	
LM271H		MC1590G
LM285Z-1.2	LM285Z-1.2	
LM285Z-2.5	LM285Z-2.5	
LM293AH	LM293AH	
LM293H	LM293H	
LM301AD		LM301AJ
LM301AF		LM301AH
LM301AH	LM301AH	
LM301AJ	LM301AJ	
LM301AJG	LM301AJ	
LM301AL	LM301AH	
LM301AN	LM301AN	
LM301AP	LM301AN	
LM306H		MC1710CG
LM307F		LM307H
LM307H	LM307H	
LM307L	LM307H	
LM307N	LM307N	
LM307P	LM307N	
LM308AD	LM308AJ	
LM308AF		LM308AJ
LM308AH	LM308AH	
LM308AH-1		LM308AH
LM308AH-2		LM308AH
LM308AJ	LM308AJ-8	
LM308D	LM308J	
LM308H	LM308H	
LM308N	LM308N	
LM309H	LM309H	
LM309K	LM309K	
LM309KC	LM309K	
LM309LA	LM309H	
LM311D	LM311J	
LM311H	LM311H	
LM311JG	LM311J-8	
LM311N	LM311N	
LM311N-14	LM311J	
LM311P	LM311N	
LM312D		MC1456L
LM312F		MC1456L
LM312H		MC1456G
LM317H	LM317H	
LM317K	LM317K	
LM317KC	LM317T	
LM317KD		LM317T
LM317LA	LM317H	
LM317MP	LM317MT	
LM317P	LM317T	
LM317T	LM317T	
LM318D		MC1741SCU
LM318F		MC1741SCU
LM318H		MC1741SCG
LM318N		MC1741SCP1
LM320H-5.0		MC7905CK
LM320H-12		MC7912CK
LM320H-15		MC7915CK
LM320K-5.0	MC7905CK	
LM320K-12	MC7912CK	
LM320K-15	MC7915CK	
LM320LZ-5.0	MC79L05ACP	
LM320LZ-12	MC79L12ACP	
LM320LZ-15	MC79L15ACP	
LM320MP-5.0		MC7905CT
LM320MP-5.2		MC7905.2CT
LM320MP-6.0		MC7906CT
LM320MP-8.0		MC7908CT
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320T-5.0	MC7905CT	
LM320T-12	MC7912CT	
LM320T-15	MC7915CT	
LM322H		MC1455G
LM322N		MC1455P1
LM323K	LM323K	
LM324AJ		LM324J
LM324AN		LM324N
LM324J	LM324J	
LM324N	LM324N	MC3403P
LM325AN		MC1468L
LM325AS		MC1468L
LM325G		MC1468L
LM325H		MC1468L
LM325N		MC1468L
LM326H		MC1468G
LM326N		MC1468L
LM326S		MC1468L
LM328AN		MC1468L
LM328H		MC1468G
LM328N		MC1468L
LM337K	LM337K	
LM337MP		LM337MT
LM337T	LM337T	
LM339AD	LM339AJ	
LM339AJ	LM339AJ	
LM339AN	LM339AN	
LM339J	LM339J	
LM339N	LM339N	
LM339P	LM339N	
LM340AK-5.0	LM340AK-5.0	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM340AK-12	LM340AK-12	
LM340AK-15	LM340AK-15	
LM340AT-5.0	LM340AT-5.0	
LM340AT-12	LM340AT-12	
LM340AT-15	LM340AT-15	
LM340K-5.0	LM340K-5.0	
LM340K-12	LM340K-12	
LM340K-15	LM340K-15	
LM340KC-5	LM340T-5.0	
LM340KC-6	LM340T-6.0	
LM340KC-8	LM340T-8.0	
LM340KC-12	LM340T-12	
LM340KC-15	LM340T-15	
LM340KC-18	LM340T-18	
LM340KC-24	LM340T-24	
LM340LAH-5.0		MC78L05ACG
LM340LAH-6.0		MC78L06ACG
LM340LAH-8.0		MC78L08ACG
LM340LAH-12		MC78L12ACG
LM340LAH-15		MC78L15ACG
LM340LAH-18		MC78L18ACG
LM340LAH-24		MC78L24ACG
LM340LAZ-5.0		MC78L05ACP
LM340LAZ-6.0		MC78L06ACP
LM340LAZ-8.0		MC78L08ACP
LM340LAZ-12		MC78L12ACP
LM340LAZ-15		MC78L15ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340T-5.0	LM340T-5.0	
LM340T-12	LM340T-12	
LM340T-15	LM340T-15	
LM341P-5.0	MC78M05CT	
LM341P-6.0	MC78M06CT	
LM341P-8.0	MC78M08CT	
LM341P-12	MC78M12CT	
LM341P-15	MC78M15CT	
LM341P-18	MC78M18CT	
LM341P-24	MC78M24CT	
LM342P-5.0	MC78M05CT	
LM342P-6.0	MC78M06CT	
LM342P-8.0	MC78M08CT	
LM342P-12	MC78M12CT	
LM342P-15	MC78M15CT	
LM342P-18	MC78M18CT	
LM342P-24	MC78M24CT	
LM343D		MC1436G
LM343H		MC1436G
LM345K		MC7905CK
LM348D	LM348J	
LM348J	LM348J	
LM348N	LM348N	
LM349D		MC4741CL
LM349J		MC4741CL
LM349N		MC4741CL
LM350K	LM350K	
LM358AH		LM358H
LM358AN		LM358N
LM358H	LM358H	
LM358JG	LM358J	
LM358L	LM358H	
LM358N	LM358N	
LM358P	LM358N	
LM371H		MC1590G
LM385BZ-1.2	LM385BZ-1.2	
LM385Z-1.2	LM385Z-1.2	
LM385BZ-2.5	LM385BZ-2.5	
LM385Z-2.5	LM385Z-2.5	
LM393AH	LM393AH	
LM393AN	LM393AN	
LM393H	LM393H	
LM393N	LM393N	
LM555CH	MC1455G	
LM555CN	MC1455P1	
LM555H	MC1555G	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556D	MC3556L	
LM556J	MC3556L	
LM565CH		NE565N
LM565CN	NE565N	
LM565H		NE565N
LM703LN		MC1350P
LM709AH	MC1709AG	
LM709CH	MC1709CG	
LM709CN-8	MC1709CP1	
LM709H	MC1709G	
LM710CH	MC1710CG	
LM710CN	MC1710CP	
LM710H	MC1710G	
LM711CH	MC1711CG	
LM711CN	MC1711CP	
LM711H	MC1711G	
LM723CD	LM723CJ	
LM723CH	MC1723CG	
LM723CJ	MC1723CL	
LM723CN	MC1723CP	
LM723D	LM723J	
LM723H	MC1723G	
LM723J	MC1723L	
LM733CD	MC1733CL	
LM733CH	MC1733CG	
LM733CJ	MC1733CL	
LM733CN	MC1733CP	
LM733D	MC1733L	
LM733H	MC1733G	
LM733J	MC1733L	
LM741AH		MC1741G
LM741CD	LM741CJ	
LM741CH	LM741CH	
LM741CJ-14	LM741CJ	
LM741CN	LM741CN	
LM741EH		MC1741CG
LM741EJ		MC1741CU
LM741EN		MC1741CP1
LM741H	LM741H	
LM747CD	LM747CJ	
LM747CH	LM747CH	
LM747CJ	LM747CJ	
LM747CN	LM747CN	
LM747D	LM747J	
LM747H	LM747H	
LM747J	LM747J	
LM748CH	MC1748CG	
LM748CJ	MC1748CU	
LM748CN	MC1748CP1	
LM748H	MC1748G	
LM748J	MC1748U	
LM1035		TCA5550

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM1310N	MC1310P	
LM1351N		MC1357P
LM1391N	MC1391P	
LM1394N	MC1394P	
LM1414J	MC1414L	
LM1414N	MC1414P	
LM1458H	MC1458G	
LM1458J	MC1458U	
LM1458N	MC1458P1	
LM1458N-14	MC1458P1	
LM1488J	MC1488L	
LM1488N	MC1488P	
LM1489AJ	MC1489AL	
LM1489AN	MC1489AP	
LM1489J	MC1489L	
LM1489N	MC1489P	
LM1496H	MC1496G	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM1514J	MC1514L	
LM1558H	MC1558G	
LM1558J	MC1558U	
LM1596H	MC1596G	
LM1596J	MC1596L	
LM1800AN		MC1310P
LM1800N		MC1310P
LM1808N		TDA1190Z
LM1822		MC13010P
LM1828N		MC1327P
LM1841N		MC1357P
LM1848N		MC1327P
LM1849A		MC3484V2
LM1889		MC1374P
LM1900D		MC3301L
LM1981		MC13020P
LM1989		MC1372P
LM2111N	MC1357P	
LM2113N		MC1357P
LM2808N		TDA1190Z
LM2900N	LM2900N	
LM2901N	LM2901N	
LM2902J	LM2902J	
LM2902N	LM2902N	
LM2903N	LM2903N	
LM2903P	LM2903N	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM3011H		MC1550G
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM3064N		MC13010P
LM3065N	MC1358P	
LM3067N		MC1327P
LM3086N	MC3386P	
LM3089		MC3356P
LM3146		MC3346P
LM3146A		MC3346P
LM3189		MC3356P
LM3301N	MC3301P	
LM3302	MC3302P	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM3401N	MC3401P	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM3900N	LM3900N	
LM3905N		MC1455P1
LM4250CH		MC1776CG
LM4250CN		MC1776CP1
LM4250H		MC1776G
LM4500A	TCA4500A	
LM7805CK	MC7805CK	
LM7805CT	MC7805CT	
LM7805KC	MC7805CK	
LM7806KC	MC7806CK	
LM7808KC	MC7808CK	
LM7812CK	MC7812CK	
LM7812CT	MC7812CT	
LM7812KC	MC7812CK	
LM7815CK	MC7815CK	
LM7815CT	MC7815CT	
LM7815KC	MC7815CK	
LM7818KC	MC7818CK	
LM7824KC	MC7824CK	
LM7905CK	MC7905CK	
LM7905CT	MC7905CT	
LM7912CK	MC7912CK	
LM7912CT	MC7912CT	
LM7915CK	MC7915CK	
LM7915CT	MC7915CT	
LM78L05ACH	MC78L05ACG	
LM78L05ACZ	MC78L05ACP	
LM78L05CH	MC78L05CG	
LM78L05CZ	MC78L05CP	
LM78L08ACH	MC78L08ACG	
LM78L08ACZ	MC78L08ACP	
LM78L08CH	MC78L08CG	
LM78L08CZ	MC78L08CP	
LM78L12ACH	MC78L12ACG	
LM78L12ACZ	MC78L12ACP	
LM78L12CH	MC78L12CG	
LM78L12CZ	MC78L12CP	
LM78L15ACH	MC78L15ACG	
LM78L15ACZ	MC78L15ACP	
LM78L15CH	MC78L15CG	
LM78L15CZ	MC78L15CP	
LM78L18ACH	MC78L18ACG	
LM78L18ACZ	MC78L18ACP	
LM78L18CH	MC78L18CG	
LM78L18CZ	MC78L18CP	
LM78L24ACH	MC78L24ACG	
LM78L24ACZ	MC78L24ACP	
LM78L24CH	MC78L24CG	
LM78L24CZ	MC78L24CP	
LM78M05CP		MC78M05CT
LM78M12CP		MC78M12CT
LM78M15CP		MC78M15CT
LM79L05ACZ	MC79L05ACP	
LM79L12ACZ	MC79L12ACP	
LM79L15ACZ	MC79L15ACP	
LM79M05CP		MC79M05CT
LM79M12CP		MC79M12CT
LM79M15CP		MC79M15CT
LM55107AJ	MC55107L	
LM55108AJ	MC55108L	
LM55109J		MC75S110L
LM55110J		MC75S110L
LM55107AJ	MC55107L	
LM75107AJ	MC75107L	
LM75107AN	MC75107P	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75S110L	
LM75110N	MC75S110P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
MB3759	TL494CN	
MB3760	TL495CN	
MC1310A	MC1310P	
MC1408B	MC1408P8	
MC1408FB	MC1408L8	
MC1458JG	MC1458U	
MC1458L	MC1458G	
MC1458P	MC1458P1	
MC1488J	MC1488L	
MC1488N	MC1488P	
MC1488N3	MC1488PDS	
MC1489AJ	MC1489AL	
MC1489AN	MC1489AP	
MC1489J	MC1489L	
MC1489N	MC1489P	
MC1489N3	MC1489PDS	
MC1545J	MC1545L	
MC1558JG	MC1558U	
MC1558L	MC1558G	
MC3446J		MC3446AP
MC3446N	MC3446AP	
MC3460P	DS3674N	
MC3470N	MC3470P	MC3470AP
MC3481J	MC3481L	
MC3481N	MC3481P	
MC3485J	MC3485L	
MC3485N	MC3485P	
MC3486J	MC3486L	
MC3486N	MC3486P	
MC3487J	MC3487L	
MC3487N	MC3487P	
MP562AD	AD562AD	
MP562KD	AD562KD	
MP562SD	AD562SD	
MP5531AJ	MC1500AG5	
MP5531BJ	MC1500G5	
MP5531CP	MC1404U5	
MP5531DP	MC1404U5	
MP5531EJ	MC1400AG5	
MP5531HJ	MC1400G5	
MP5532AJ	MC1500AG10	
MP5532BJ	MC1500G10	
MP5532CP	MC1404U10	
MP5532DP	MC1404U10	
MP5532EJ	MC1400AG10	
MP5532HJ	MC1400G10	
N8T13J	MC8T13L	
N8T13N	MC8T13P	
N8T14J	MC8T14L	
N8T14N	MC8T14P	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26AJ	MC8T26AL	
N8T26AN	MC8T26AP	
N8T26B	MC8T26AP	
N8T26J	MC8T26AL	
N8T26N	MC8T26AP	
N8T28B	MC8T28P	
N8T37A	MC3437P	
N8T38A	MC3438P	
N8T95B	MC8T95P	
N8T95F	MC8T95L	
N8T96B	MC8T96P	
N8T96F	MC8T96L	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
N5065A	MC1358P	
N5072A		MC1327P
N5556T	MC1456G	
N5556V	MC1456P1	
N5558F	MC1458L	
N5558T	MC1458G	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5596K	MC1496G	
N5709A	MC1709CP2	
N5709G	MC1709CF	
N5709T	MC1709CG	
N5709V	MC1709CP1	
N5710A	MC1710CP	
N5710T	MC1710CG	
N5711A	MC1711CP	
N5711K	MC1711CG	
N5723A		MC1723CP
N5723T	MC1723CG	
N5723K	MC1733CG	
N5741A	MC1741CP2	
N5741T	MC1741CG	
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N5748A		MC1747CG
N5748T	MC1748CG	
NE501A		MC1733CL
NE501K		MC1733CG
NE531G		MC1439G
NE531T		MC1439G
NE531V		MC1439P
NE533G		MC1776CG
NE533T		MC1776CG
NE533V		MC1776CG
NE537G		MC1456G
NE537T		MC1456G
NE540L		MC1554G
NE550A		MC1723CP
NE550L		MC1723CG
NE555JG	MC1455U	
NE555L	MC1455G	
NE555P	MC1455P1	
NE555T	MC1455G	
NE555V	MC1455P1	
NE556A	MC3456P	
NE556I	MC3456L	
NE565A	NE565N	
NE565K		NE565N

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
NE592A	NE592A	
NE592K	NE592K	
NE5118F		MC6890L
NE5118N		MC6890L
NE5410F	MC3410L	
NE5561FE		MC34060L
NE5561N		MC34060P
OP-01C		MC1536
OP-01G		MC1536
OP-01H		MC1536
OP-01J		MC1536G
OP-01L		MC1536G
OP-01P		MC1436P
OP-08		MC1776
OP-08A		MC1776
OP-08B		MC1776
OP-08C		MC1776
OP-08E		MC1776
OP-27AJ	OP-27AJ	
OP-27AZ	OP-27AZ	
OP-27BJ	OP-27BJ	
OP-27BZ	OP-27BZ	
OP-27CJ	OP-27CJ	
OP-27CZ	OP-27CZ	
OP-27EJ	OP-27EJ	
OP-27EP	OP-27EP	
OP-27EZ	OP-27EZ	
OP-27FJ	OP-27FJ	
OP-27FP	OP-27FP	
OP-27FZ	OP-27FZ	
OP-27GJ	OP-27GJ	
OP-27GP	OP-27GP	
OP-27GZ	OP-27GZ	
OP-37AJ	OP-37AJ	
OP-37AZ	OP-37AZ	
OP-37BJ	OP-37BJ	
OP-37BZ	OP-37BZ	
OP-37CJ	OP-37CJ	
OP-37CZ	OP-37CZ	
OP-37EJ	OP-37EJ	
OP-37EP	OP-37EP	
OP-37EZ	OP-37EZ	
OP-37FJ	OP-37FJ	
OP-37FP	OP-37FP	
OP-37FZ	OP-37FZ	
OP-37GJ	OP-37GJ	
OP-37GP	OP-37GP	
OP-37GZ	OP-37GZ	
PWM125AK	SG1525AJ	
PWM125BK	SG2525AJ	
PWM125CK	SG3525AJ	
RC702T	MC1712CG	
RC709DN	MC1709CP1	
RC709T	MC1709CG	
RC710DC	MC1710CL	
RC710DP	MC1710CP	
RC710T	MC1710CG	
RC711DC	MC1711CL	
RC711DP	MC1711CP	
RC711T	MC1711CG	
RC723D	MC1723CL	
RC723DB	MC1723CP	
RC723DC	MC1723CL	
RC723T	MC1723CG	
RC733D	MC1733CL	
RC733T	MC1733CG	
RC741DN	MC1741CP1	
RC741T	MC1741CG	
RC747D	MC1747CL	
RC747T	MC1747CG	
RC748T	MC1748CG	
RC1414DC	MC1414L	
RC1414DP	MC1414P	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC1437D	MC1437L	
RC1437DP	MC1437P	
RC1458DN	MC1458P1	
RC1458T	MC1458G	
RC1556T	MC1456CG	
RC1558T	MC1558G	
RC3302DB	MC3302P	
RC4131DP		MC1471SCP1
RC4131T		MC1741SG
RC4136D		MC3403L
RC4136DP		MC3403P
RC4136J		MC3403L
RC4136N		MC3403P
RC4194DC		MC1468L
RC4194TK		MC1468R
RC4195NB		MC1468L
RC4195T		MC1468G
RC4195TK		MC1468R
RC4444R	MC3416L	
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4558L	MC4558CG	
RC4558P	MC4558CP1	
RC4558T	MC4558CG	
RC75107AD	MC75107L	
RC75107ADP	MC75107P	
RC75108AD	MC75108L	
RC75108ADP	MC75108P	
RC75109D		MC75S110L
RC75109DP		MC75S110P
RC75110D	MC75S110L	
RC75110DP	MC75S110P	
REF-01AJ	MC1500AG10	
REF-01AZ		MC1500AG10
REF-01CJ		MC1404U10
REF-01CP	MC1404U10	
REF-01CZ	MC1404U10	
REF-01DJ		MC1404U10
REF-01DP	MC1404U10	
REF-01DZ	MC1404U10	
REF-01EJ	MC1400AG10	
REF-01EZ		MC1400AG10
REF-01HJ	MC1400G10	
REF-01HP		MC1400G10
REF-01HZ		MC1400G10
REF-01J	MC1500G10	
REF-01Z		MC1500G10
REF-02AJ	MC1500AG5	
REF-02AZ		MC1500AG5
REF-02CJ		MC1404U5
REF-02CP	MC1404U5	
REF-02CZ	MC1404U5	
REF-02DJ		MC1404U5
REF-02DP	MC1404U5	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
REF-02DZ	MC1404U5	
REF-02EJ	MC1400AG5	
REF-02EZ		MC1400AG5
REF-02HJ	MC1400G5	
REF-02HP		MC1400G5
REF-02HZ		MC1400G5
REF-02J	MC1500G5	
REF-02Z		MC1500G5
RM702T	MC1712G	
RM709T	MC1709G	
RM710D	MC1710L	
RM710T	MC1710G	
RM711DC	MC1711L	
RM711T	MC1711G	
RM723D	MC1723L	
RM723DC	MC1723L	
RM723T	MC1723G	
RM733D	MC1733L	
RM733T	MC1733G	
RM741DP	MC1741P	
RM741T	MC1741G	
RM747D	MC1747L	
RM747T	MC1747G	
RM748T	MC1748G	
RM1514DC	MC1514L	
RM1537D	MC1537L	
RM4136D		MC3503L
RM4136J		MC3503L
RM4194DC		MC1568L
RM4194TK		MC1568R
RM4195T		MC1568G
RM4195TK		MC1568R
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM4558L	MC4558G	
RM4558T	MC4558G	
RM55107AD	MC55107L	
RV3301DB	MC3301P	
S5556T	MC1556G	
S5558E	MC1558L	
S5558T	MC1558G	
S5596F	MC1596L	
S5596K	MC1596G	
S5709G	MC1709F	
S5709T	MC1709G	
S5710T	MC1710G	
S5711K	MC1711G	
S5723T	MC1723G	
S5733K	MC1733G	
S5741T	MC1741G	
SE501K		MC1733G
SE531G		MC1539G
SE531T		MC1539G
SE533G		MC1776G
SE533T		MC1776G
SE537G		MC1556G
SE537T		MC1556G
SE550L		MC1723G
SE555JG	MC1555U	
SE555L	MC1555G	
SE555T	MC1555G	
SE556A	MC3556L	
SE565A		MLM565CP
SE565K		MLM565CP
SE592A	SE592L	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SE592K	SE592G	
SE5118F	MC6890AL	MC6890AL
SE5410F	MC3510L	
SE5561FE		MC35060L
SG100T		MC1723G
SG101AD		LM101AH
SG101AT	LM101AH	
SG101J		LM101AH
SG101T	LM101AH	
SG104T	LM104H	
SG105N		LM105H
SG105T	LM105H	
SG107J		LM107H
SG107T	LM107H	
SG108AJ	LM108AJ	
SG108AT	LM108AH	
SG108J	LM108J	
SG108T	LM108H	
SG109K	LM109K	
SG109R		MC109K
SG109T	LM109H	
SG111D	LM111J	
SG111T	LM111H	
SG117K	LM117K	
SG117R		LM117K
SG117T	LM117H	
SG118T		MC1741SG
SG123K	LM123K	
SG124J	LM124J	
SG137K	LM137K	
SG137R		LM137K
SG137T	LM137H	
SG140K-05	LM140K-5.0	
SG140K-06	LM140K-6.0	
SG140K-08	LM140K-8.0	
SG140K-12	LM140K-12	
SG140K-15	LM140K-15	
SG140K-18	LM140K-18	
SG140K-24	LM140K-24	
SG150K	LM150K	
SG200T		MC1723G
SG201AD		LM201AH
SG201AM	LM201AN	
SG201AN		LM201AN
SG201AT	LM201AH	
SG201J		LM201AH
SG201M	LM201AN	
SG201N		LM201AN
SG201T	LM201AH	
SG207J		LM207H
SG207M		LM207H
SG207N		LM207H
SG207T	LM207H	
SG208AJ	LM208AJ	
SG208AM	LM208AJ-8	
SG208AT	LM208AH	
SG208J	LM208J	
SG208M	LM208J-8	
SG208T	LM208H	
SG209K	LM209K	
SG209R		MC209K
SG209T	LM209H	
SG211D	LM211J	
SG211M	LM211N	
SG211T	LM211H	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG217K	LM217K	
SG217R		LM217K
SG217T	LM217H	
SG218J		MC1741SL
SG218M		MC1741SL
SG218T		MC1741SG
SG223K	LM223K	
SG224J	LM224J	
SG224N	LM224N	
SG237K	LM237K	
SG237R		LM237K
SG237T	LM237H	
SG250K	LM250K	
SG300N		MC1723CP
SG300T		MC1723CG
SG301AD		LM301AH
SG301AM	LM301AN	
SG301AN		LM301AN
SG301AT	LM301AH	
SG307J		LM307N
SG307M	LM307N	
SG307N		LM307N
SG307T	LM307H	
SG308AJ	LM308AJ	
SG308AM	LM308AN	
SG308AT	LM308AH	
SG308J	LM308J	
SG308M	LM308N	
SG308T	LM308H	
SG309K	LM309K	
SG309P		LM309K
SG309R		MC309K
SG309T	LM309H	
SG311D	LM311J	
SG311M	LM311N	
SG311T	LM311H	
SG317K	LM317K	
SG317P	LM317T	
SG317R		LM317T
SG317T	LM317H	
SG318J		MC1741SCL
SG318M		MC1741CP1
SG318T		MC1741CG
SG324J	LM324J	
SG324N	LM324N	
SG337K	LM337K	
SG337P	LM337T	
SG337R		LM337T
SG337T	LM337H	
SG340K-05	LM340K-5.0	
SG340K-06	LM340K-6.0	
SG340K-08	LM340K-8.0	
SG340K-12	LM340K-12	
SG340K-15	LM340K-15	
SG340K-18	LM340K-18	
SG340K-24	LM340K-24	
SG350K	LM350K	
SG501AJ		MC1468G
SG555CM	MC1455P1	
SG555CT	MC1455G	
SG555T	MC1555G	
SG556CJ	MC3456L	
SG556CN	MC3456P	
SG556J	MC3556L	
SG556N	MC3556L	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG710CD	MC1710CL	
SG710CN	MC1710CP	
SG710CT	MC1710CG	
SG710D	MC1710L	
SG710N	MC1710CP	
SG710T	MC1710G	
SG711CD	MC1711CL	
SG711CN	MC1711CP	
SG711CT	MC1711CG	
SG711D	MC1711L	
SG711N	MC1711CP	
SG711T	MC1711G	
SG723CD	MC1723CL	
SG723CJ	MC1723CL	
SG723CN	MC1723CP	
SG723CT	MC1723CG	
SG723D	MC1723L	
SG723J	MC1723L	
SG723T	MC1723G	
SG733CD	MC1733CL	
SG733CN		MC1733CP
SG733CT	MC1733CG	
SG733D	MC1733L	
SG733N		MC1733L
SG733T	MC1733G	
SG741CM	MC1741CP1	
SG741CT	MC1741CG	
SG741SCM	MC1741SCP1	
SG741SCT	MC1741SCG	
SG741ST	MC1741SG	
SG741T	MC1741G	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747CT	MC1747CG	
SG747J	MC1747L	
SG747T	MC1747G	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG748CT	MC1748CG	
SG748D		MC1748G
SG748T	MC1748G	
SG777CJ		LM308AJ
SG777CM		LM308AN
SG777CN		LM308AN
SG777CT		LM308AH
SG777J		LM108AJ
SG777T		LM108AH
SG1118AJ		LM108AJ
SG1118AT		LM108AH
SG1118J		LM108J
SG1118T		LM108H
SG1217		MC1741G
SG1217T		MC1741SG
SG1250T		MC1776G
SG1402N		MC1594L
SG1402T		MC1594L
SG1436CT	MC1436CG	
SG1436M	MC1436U	
SG1436T	MC1436G	
SG1456CT	MC1456CG	
SG1456T	MC1456G	
SG1458M	MC1458P1	
SG1458T	MC1458G	
SG1468J	MC1468L	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG1468N		MC1468L
SG1468R	MC1468R	
SG1468T	MC1468G	
SG1495D	MC1495L	
SG1495N	MC1495L	
SG1496D	MC1496L	
SG1496N		MC1496L
SG1496T	MC1496G	
SG1501AD		MC1568L
SG1501AJ		MC1568L
SG1501AT		MC1568G
SG1501J	MC1568L	
SG1501T	MC1568G	
SG1502D		MC1568L
SG1502J		MC1568L
SG1502N		MC1568L
SG1503	MC1503U	
SG1503T		MC1503U
SG1503Y		MC1503U
SG1511J		MC1563G
SG1511T		MC1563G
SG1524J		TL494MJ
SG1525AJ	SG1525AJ	
SG1526J	SG1526J	
SG1527AJ	SG1527AJ	
SG1536T	MC1536G	
SG1542J		MC3524L
SG1543J		MC3524L
SG1544J		MC3424AL
SG1556T	MC1556G	
SG1558T	MC1558G	
SG1568J	MC1568L	
SG1568R	MC1568R	
SG1568T	MC1568G	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG1596T	MC1596G	
SG1660D		LM301AH
SG1660J		LM308J
SG1660M		LM308N
SG1660T		LM308H
SG1760D		LM307H
SG1760F		LM307H
SG1760J		LM308J
SG1760M		LM308N
SG1760T		LM308H
SG2118AJ		LM208AJ
SG2118AM		LM208AJ-8
SG2118AT		LM208AH
SG2118J		LM208J
SG2118M		LM208J-8
SG2118T		LM208H
SG2250T		MC1776G
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501AT		
SG2501D	MC1468L	
SG2501J	MC1468L	
SG2501N	MC1468L	
SG2501T	MC1468G	
SG2502J		MC1468L
SG2502N		MC1468L
SG2503	MC1403AU	
SG2503M		MC1403AU
SG2503T		MC1403AU
SG2503Y		MC1403AU
SG2524J		TL494IJ
SG2525AJ	SG2525AJ	
SG2526J	SG2526J	
SG2527AJ	SG2527AJ	
SG2542J		MC3324L
SG2542N		MC3324P
SG2543J		MC3324L
SG2544J		MC3324AL
SG3118AJ		LM308AJ
SG3118AM		LM308AN
SG3118AT		LM308AH
SG3118J		LM308J
SG3118M		LM308N
SG3118T		LM308H
SG3250T		MC1776G
SG3402N		MC1494L
SG3402T		MC1494L
SG3423M		MC3423P1
SG3423Y		MC3423U
SG3501AD	MC1468L	
SG3501AJ	MC1468L	
SG3501AN		MC1468L
SG3501AT	MC1468G	
SG3501J	MC1468L	
SG3501D	MC1468L	
SG3501N	MC1468L	
SG3501T	MC1468G	
SG3502D		MC1468L
SG3502G		MC1468G
SG3502J		MC1468L
SG3502N		MC1468L
SG3503	MC1403U	
SG3503M		MC1403U
SG3503T		MC1403U
SG3503Y	MC1403U	
SG3511J		MC1463G
SG3511N		MC1463G
SG3511T		MC1463G
SG3523Y		MC3523U
SG3524J		MC3420L
SG3525AJ	SG3525AJ	
SG3525AN	SG3525AN	
SG3526J	SG3526J	
SG3527AJ	SG3527AJ	
SG3527AN	SG3527AN	
SG3542J		MC3424L
SG3542N		MC3424P
SG3543J		MC3424L
SG3544J		MC3424AL
SG4194CJ		MC1468L
SG4194CR		MC1468R
SG4194J		MC1568L
SG4194R		MC1468R
SG4250CM		MC1776CP1
SG4250CT		MC1776CG
SG4250T		MC1776G
SG4501D	MC1468L	
SG4501J		MC1468L
SG4501N		MC1468L
SG4501T		MC1468G
SG7805ACK	MC7805ACK	
SG7805ACP	MC7805ACT	
SG7805ACR		MC7805ACT

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG7805ACT		MC7805ACT
SG7805AK	MC7805AK	
SG7805AR		MC7805AK
SG7805AT		MC7805AK
SG7805CK	MC7805CK	
SG7805CP	MC7805CT	
SG7805CR		MC7805CT
SG7805CT		MC78M05CG
SG7805K	MC7805K	
SG7805R		MC7805K
SG7805T		MC7805K
SG7806ACK	MC7806ACK	
SG7806ACP	MC7806ACT	
SG7806ACR		MC7806ACT
SG7806ACT		MC7806ACT
SG7806AK	MC7806AK	
SG7806AR		MC7806AK
SG7806AT		MC7806AK
SG7806CK	MC7806CK	
SG7806CP	MC7806CT	
SG7806CR		MC7806CT
SG7806CT		MC78M06CG
SG7806K	MC7806K	
SG7806R		MC7806K
SG7806T		MC7806K
SG7808ACK	MC7808ACK	
SG7808ACP	MC7808ACT	
SG7808ACR		MC78M08ACT
SG7808ACT		MC7808ACT
SG7808AK	MC7808AK	
SG7808AR		MC7808AK
SG7808AT		MC7808AK
SG7808CK	MC7808CK	
SG7808CP	MC7808CT	
SG7808CR		MC7808CT
SG7808CT		MC7808CG
SG7808K	MC7808K	
SG7808R		MC7808K
SG7808T		MC7808K
SG7812ACK	MC7812ACK	
SG7812ACP	MC7812ACT	
SG7812ACR		MC7812ACT
SG7812ACT		MC7812ACT
SG7812AK	MC7812AK	
SG7812AR		MC7812AK
SG7812AT		MC7812AK
SG7812CK	MC7812CK	
SG7812CP	MC7812CT	
SG7812CR		MC7812CT
SG7812CT		MC78M12CG
SG7812K	MC7812K	
SG7815ACK	MC7815ACK	
SG7815ACP	MC7815ACT	
SG7815ACR		MC7815ACT
SG7815ACT		MC7815ACT
SG7815AK	MC7815AK	
SG7815AR		MC7815AK
SG7815AT		MC7815AK
SG7815CK	MC7815CK	
SG7815CP	MC7815CT	
SG7815CR		MC7815CT
SG7815CT		MC78M15CG
SG7815K	MC7815K	
SG7815R		MC7815K
SG7815T		MC7815K

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SG7818ACK	MC7818ACK	
SG7818ACP	MC7818ACT	
SG7818ACR		MC7818ACT
SG7818ACT		MC7818ACT
SG7818AK	MC7818AK	
SG7818AR		MC7818AK
SG7818AT		MC7818AK
SG7818CK	MC7818CK	
SG7818CP	MC7818CT	
SG7818CR		MC7818CT
SG7818CT		MC7818CG
SG7818K	MC7818K	
SG7818R		MC7818K
SG7818T		MC7818K
SG7824ACK	MC7824ACK	
SG7824ACP	MC7824ACT	
SG7824ACR		MC7824ACT
SG7824ACT		MC7824ACT
SG7824AK	MC7824AK	
SG7824AR		MC7824AK
SG7824AT		MC7824AK
SG7824CK	MC7824CK	
SG7824CP	MC7824CT	
SG7824CR		MC7824CT
SG7824CT		MC78M24CG
SG7824K	MC7824K	
SG7824R		MC7824K
SG7824T		MC7824K
SG7905ACK	MC7905ACK	
SG7905ACP	MC7905ACT	
SG7905ACR		MC7905ACT
SG7905ACT		MC7905ACT
SG7905CK		MC7905CK
SG7905CP	MC7905CT	
SG7905CR		MC7905CT
SG7905CT		MC7905CT
SG7905.2CK	MC7905.2CK	
SG7905.2CP	MC7905.2CT	
SG7905.2CR		MC7905.2CT
SG7905.2CT		MC7905.2CT
SG7908CK	MC7908CK	
SG7908CP	MC7908CT	
SG7908CR		MC7908CT
SG7908CT		MC7908CT
SG7912ACK	MC7912ACK	
SG7912ACP	MC7912ACT	
SG7912ACR		MC7912ACT
SG7912ACT		MC7912ACT
SG7912CK	MC7912CK	
SG7912CP	MC7912CT	
SG7912CR		MC7912CT
SG7912CT		MC7912CT
SG7915ACK	MC7915ACK	
SG7915ACP	MC7915ACT	
SG7915ACR		MC7915ACT
SG7915ACT		MC7915ACT
SG7915CK	MC7915CK	
SG7915CP	MC7915CT	
SG7915CR		MC7915CT
SG7915CT		MC7915CT
SG7918CK	MC7918CK	
SG7918CP	MC7918CT	
SH323SKC	LM323K	
SH8090FM		MC1508L8
SN52101AL	LM101AH	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN52104L	LM101H	
SN52106J		MC1710L
SN52106L		MC1710G
SN52107L	LM107H	
SN52108AL	LM108AH	
SN52108L	LM108H	
SN52109L	LM109H	
SN52510J		MC1710L
SN52510L		MC1710G
SN52514J	MC1514L	
SN52555L	MC1555G	
SN52558L	MC1558G	
SN52702AJ		MC1712L
SN52702AL		MC1712G
SN52702FA		MC1712G
SN52702J	MC1712L	
SN52702L	MC1712G	
SN52709AL	MC1709AG	
SN52709L	MC1709G	
SN52710FA	MC1710F	
SN52710J	MC1710L	
SN52710L	MC1710G	
SN52711FA	MC1711F	
SN52711J	MC1711L	
SN52711L	MC1711G	
SN52723J	MC1723L	
SN52723L	MC1723G	
SN52733J	MC1733L	
SN52733L	MC1733G	
SN52741L	MC1741G	
SN52747J	MC1747L	
SN52747L	MC1747G	
SN52748L	MC1748G	
SN52770L		MC1556G
SN52771L		MC1556G
SN52810FA		MC1710F
SN52810J		MC1710L
SN52810L		MC1710G
SN52811FA		MC1711F
SN52811J		MC1711L
SN52811L		MC1711G
SN55107AJ	MC55107L	
SN55107BJ		MC55107L
SN55108AJ	MC55108L	
SN55108BJ		MC75108L
SN55109J		MC75S110L
SN55110J		MC75S110L
SN55244J	MC1544L	
SN72L022P		LM358N
SN72L044JA		LM324N
SN72L044N		LM324N
SN72301AL	LM301AH	
SN72301AP	LM301AN	
SN72306J		MC1710CL
SN72306L		MC1710CG
SN72306N		MC1710CP
SN72307L	LM307H	
SN72308AL	LM308AH	
SN72308L	LM308H	
SN72309L	LM309H	
SN72311L	LM311H	
SN72311P	LM311N	
SN72440J		MC3370P
SN72440N		MC3370P
SN72510J		MC1710CL
SN72510L		MC1710CG
SN72510N		MC1710CP
SN72514J		MC1414L
SN72514N		MC1414P
SN72555L	MC1455G	
SN72555P	MC1455P1	
SN72558L	MC1458G	
SN72558P	MC1458P1	
SN72702J	MC1712CL	
SN72702L	MC1712CG	
SN72709L	MC1709CG	
SN72709P	MC1709CP1	
SN72710J	MC1710CL	
SN72710L	MC1710CG	
SN72710N	MC1710CP	
SN72711J	MC1711CL	
SN72711L	MC1711CG	
SN72711N	MC1711CP	
SN72720J		MC1710CL
SN72720L		MC1710CG
SN72720N		MC1710CP
SN72723J	MC1723CL	
SN72723L	MC1723CG	
SN72733J	MC1733CL	
SN72733L	MC1733CG	
SN72741L	MC1741CG	
SN72741P	MC1741CP1	
SN72747J	MC1747CL	
SN72747L	MC1747CG	
SN72747N	MC1747CP2	
SN72748L	MC1748CG	
SN72748P	MC1748CP1	
SN72770L		MC1456G
SN72771L		MC1456G
SN72810J		MC1710CL
SN72810L		MC1710CG
SN72810N		MC1710CP
SN72811J		MC1711CL
SN72811L		MC1711CG
SN72811N		MC1711CP
SN72905	MC7905CT	
SN72906	MC7906CT	
SN72908	MC7908CT	
SN72912	MC7912CT	
SN72915	MC7915CT	
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75110AJ	MC75S110L	
SN75110AN	MC75S110P	
SN75121J		MC3481/5L
SN75121N		MC3481/5P
SN75122J		SN75125-9L
SN75122N		SN75125-9P
SN75125J	MC75125L	
SN75125N	MC75125P	
SN75126J		MC3481/5L
SN75126N		MC3481/5P
SN75127J	MC75127L	
SN75127N	MC75127P	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN75128J	MC75128L	
SN75128N	MC75128P	
SN75129J	MC75129L	
SN75129N	MC75129P	
SN75138N		MC3443P
SN75138J		MC3443P
SN75150J		MC1488L
SN75150N		MC1488P
SN75154J		MC1489L
SN75154N		MC1489P
SN75160J		MC3447L
SN75160N		MC3447P/P3
SN75172J	SN75172J	
SN75172NG	SN75172NG	
SN75173J	SN75173J	
SN75173N	SN75173N	
SN75174J	SN75174J	
SN75174NG	SN75174NG	
SN75175J	SN75175J	
SN75175N	SN75175N	
SN75176JG	SN75176JG*	
SN75176P	SN75176P*	
SN75177JG	SN75177JG*	
SN75177P	SN75177P*	
SN75178JG	SN75178JG*	
SN75178P	SN75178P*	
SN75188J	MC1488L	
SN75188N	MC1488P	
SN75188N3	MC1488PDS	
SN75189AJ	MC1489AL	
SN75189AJ4	MC1489ALDS	
SN75189AN	MC1489AP	
SN75189J	MC1489L	
SN75189J4	MC1489LDS	
SN75189N	MC1489P	
SN75189N3	MC1489PDS	
SN75207J		MC75107L
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75251N		MC3471P
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475JG	MC1472U	
SN75475P	MC1472P1	
SN75491AN	MC75491P	
SN75491N	MC75491P	
SN75492AN	MC75492P	
SN75492N	MC75492P	
SN76104N		MC1310P
SN76105N		MC1310P
SN76111N		MC1310P
SN76113N		MC1310P
SN76115N	MC1310P	
SN76116N		MC1310P
SN76117N		MC1310P
SN76246N		MC1327P
SN76298N	MC1398P	
SN76514L		MC1496G
SN76514N	MC1496P	
SN76564N		MC13010P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SN76565N		MC13010P
SN76591P	MC1391P	
SN76594P	MC1394P	
SN76600P	MC1350P	
SN76642N	MC1357P	
SN76644N		MC1352P
SN76650N	MC1352P	
SN76651N		MC1357P
SN76653N		MC1352P
SN76660N		MC1357P
SN76665N		MC13010P
SN76666N	MC1358P	
SN76669N		MC1357P
SN76678P		MC1355P
SSS101AL		LM101AH
SSS101AJ	LM101AH	
SSS107J	LM107H	
SSS107P		LM107H
SSS201AJ	LM201AH	
SSS201AL		LM201AH
SSS201AP		LM201AN
SSS207J	LM207H	
SSS207P		LM207H
SSS301AJ	LM301AH	
SSS301AL		LM301AH
SSS301AP	LM301AN	
SSS741BJ		MC1741G
SSS741CJ		MC1741CG
SSS741GJ	MC1741SG	
SSS741GP		MC1741SG
SSS741J		MC1741G
SSS747BP		MC1747L
SSS747CK		MC1747CG
SSS747CM		MC1747CF
SSS747CP		MC1747CL
SSS747GK		MC1747G
SSS747GP		MC1747L
SSS747P		MC1747L
SSS1408A-6Z	MC1408L6	
SSS1408A-7Z	MC1408L7	
SSS1408A-8Z	MC1408L8	
SSS1458J	MC1458G	
SSS1508A-8Z	MC1508L8	
SSS1558J	MC1558G	
TAA630		MC1327P
TBA120		TBA120C
TBA440		MC13010P
TBA520		MC1327P
TBA920		MC1391P
TBA920S		MC1391P
TBA990		MC1327P
TBA1440		MC13010P
TCA4500A	TCA4500A	
TDA1085	TDA1085	
TDA1190Z	TDA1190Z	
TDA1524		TCA5550
TDA2540		MC13010P
TDA2544		MC13010P
TDA3780		MC1376P
TDA4420		MC13010P
TDA4600	TDA4600	
TDA5600		MC13010P
TDC1027J7		MC10315L
TL022CJG		LM358J
TL022CL		LM358H

*To be introduced.

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
TL022CP		LM358N
TL022MJG		LM158J
TL022ML		LM158H
TL044CJ		LM324J
TL044CN		LM324N
TL044MJ		LM124J
TL071ACJG	TL071ACJG	
TL071ACP	TL071ACP	
TL071BCJG	TL071BCJG	
TL071BCP	TL071BCP	
TL071CJG	TL071CJG	
TL071CP	TL071CP	
TL072ACJG	TL072ACJG	
TL072ACP	TL072ACP	
TL072BCJG	TL072BCJG	
TL072BCP	TL072BCP	
TL072CJG	TL072CJG	
TL072CP	TL072CP	
TL074ACJ	TL074ACJ	
TL074ACN	TL074ACN	
TL074BCJ	TL074BCJ	
TL074BCN	TL074BCN	
TL074CJ	TL074CJ	
TL074CN	TL074CN	
TL081ACJG	TL081ACJG	
TL081ACP	TL081ACP	
TL081BCJG	TL081BCJG	
TL081BCP	TL081BCP	
TL081CJG	TL081CJG	
TL081CP	TL081CP	
TL082ACJG	TL082ACJG	
TL082ACP	TL082ACP	
TL082BCJG	TL082BCJG	
TL082BCP	TL082BCP	
TL082CJG	TL082CJG	
TL082CP	TL082CP	
TL084ACJ	TL084ACJ	
TL084ACN	TL084ACN	
TL084BCJ	TL084BCJ	
TL084BCN	TL084BCN	
TL084CJ	TL084CJ	
TL084CN	TL084CN	
TL431CJG	TL431CJG	
TL431CLP	TL431CLP	
TL431CP	TL431CP	
TL431IJG	TL431IJG	
TL431IP	TL431IP	
TL431ILP	TL431ILP	
TL431MJG	TL431MJG	
TL494CJ	TL494CJ	
TL494CN	TL494CN	
TL494IJ	TL494IJ	
TL494IN	TL494IN	
TL494MJ	TL494MJ	
TL495CJ	TL495CJ	
TL495CN	TL495CN	
TL495IJ	TL495IJ	
TL495IN	TL495IN	
TL497CJ		MC34063U
TL497CN		MC34063P1
TL497MJ		MC35063U
TL514MJ	MC1514L	
TL710CP	MC1710CP	
TL710MJ	MC1710L	
TL780-05CKC	TL780-05CKC	
TL780-12CKC	TL780-12CKC	
TL780-15CKC	TL780-15CKC	
TL7805ACKC	MC7805ACT	
UC117K	LM117K	
UC137K	LM137K	
UC150K	LM150K	
UC217K	LM217K	
UC237K	LM237K	
UC250K	LM250K	
UC317K	LM317K	
UC317T	LM317T	
UC337K	LM337K	
UC337T	LM337T	
UC350K	LM350K	
UC1525AJ	SG1525AJ	
UC1526J	SG1526J	
UC1527AJ	SG1527AJ	
UC2525AJ	SG2525AJ	
UC2526J	SG2526J	
UC2526N	SG2526N	
UC2527AJ	SG2527AJ	
UC3525AJ	SG3525AJ	
UC3525AN	SG3525AN	
UC3526J	SG3526J	
UC3526N	SG3526N	
UC3527AJ	SG3527AJ	
UC3527AN	SG3527AN	
UDN5711M	MC1471P1	
UDN5712M	MC1472P1	
UDN5713M	MC1473P1	
UDN5714M	MC1474P1	
UDN7183A		MC3491L
UDN7184A		MC3491L
ULN2001A	ULN2001A	
ULN2001AN	MC1411P	
ULN2002A	ULN2002A	
ULN2002AJ	MC1412L	
ULN2002AN	MC1412P	
ULN2003A	ULN2003A	
ULN2003AJ	MC1413L	
ULN2003AJ4	MC1413LDS	
ULN2003AN	MC1413P	
ULN2003AN3	MC1413PDS	
ULN2004A	ULN2004A	
ULN2004AJ	MC1416L	
ULN2004AJ4	MC1416LDS	
ULN2004AN	MC1416P	
ULN2004AN3	MC1416PDS	
ULN2064NE	ULN2064B	
ULN2065NE	ULN2065B	
ULN2066NE	ULN2065B	
ULN2067NE	ULN2066B	
ULN2068B	ULN2068B	
ULN2068NE	ULN2068B	
ULN2069NE	ULN2069B	
ULN2074B	ULN2074B	
ULN2074NE	ULN2074B	
ULN2111A	MC1357P	
ULN2113A		MC1357P
ULN2113N		MC1357P
ULN2114A		MC1327P
ULN2114K		MC1327P
ULN2114N		MC1327P
ULN2120A		MC1310P
ULN2121A		MC1310P

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
ULN2122A		MC1310P
ULN2128A		MC1310P
ULN2136A		MC1357P
ULN2139D		MC1439G
ULN2139G		MC1439G
ULN2139H		MC1439P2
ULN2139M		MC1439P1
ULN2151D		MC1741CG
ULN2151G		MC1741CF
ULN2151H		MC1741CP1
ULN2151M		MC1741CP1
ULN2156D		MC1456G
ULN2156G		MC1456G
ULN2156H		MC1456G
ULN2156M		MC1456G
ULN2157A		MC1458P2
ULN2157H		MC1458P2
ULN2157K		MC1458G
ULN2165A	MC1358P	
ULN2209A		MC1357P
ULN2210A	MC1310P	
ULN2224A		MC1327P
ULN2228A		MC1327P
ULN2244A		MC1310P
ULN2264A		MC13010P
ULN2267A		MC1327P
ULN2741D		MC1741CG
ULN2747A		MC1747CL
ULN2801A	ULN2801A	
ULN2802A	ULN2802A	
ULN2803A	ULN2803A	
ULN2804A	ULN2804A	
ULN8126A	SG3526N	
ULN8126R	SG3526J	
ULQ8126A	SG2526N	
ULQ8126R	SG2526J	
ULS2139D		MC1539G
ULS2139G		MC1539G
ULS2139H		MC1539L
ULS2139M		MC1439P1
ULS2151D		MC1741G
ULS2151M		MC1741CP1
ULS2156D		MC1556G
ULS2156G		MC1556G
ULS2156H		MC1556G
ULS2156M		MC1556G
ULS2157A		MC1558L
ULS2157H		MC1558L
ULS2157K		MC1558G
ULS8126R	SG1526J	
ULX8161M		MC34060P
XR082CN	TL082CJG	
XR082CP	TL082CP	
XR082M	TL082MJG	
XR084CN	TL084CJ	
XR084CP	TL084CN	
XR084M	TL084MJ	
XR3470A	MC3470AP	
µA0802DC-1	MC1408L8	
µA0802DC-2	MC1408L7	
µA0802DC-3	MC1408L6	
µA0802DM-1	MC1508L8	
µA0802PC-1	MC1408P8	
µA0802PC-2	MC1408P7	
µA0802PC-3	MC1408P6	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
µA78GHM		LM117K
µA78GKC		LM117K
µA78GKM		LM117K
µA78GUC		LM317T
µA78GU1C		LM317T
µA78H05KC		MC7805CK
µA78L02ACJG		MC78L02ACG
µA78L05ACJG		MC78L05ACG
µA78L05ACLP	MC78L05ACP	
µA78L05AHC	MC78L05ACG	
µA78L05AWC	MC78L05ACP	
µA78L05CJG		MC78L05CG
µA78L05CLP	MC78L05CP	
µA78L05HC	MC78L05CG	
µA78L05WC	MC78L05CP	
µA78L06ACJG		MC78L06ACG
µA78L06ACLP	MC78L06ACP	
µA78L06CJG		MC78L06CG
µA78L06CLP	MC78L06CP	
µA78L08ACJG		MC78L08ACG
µA78L08ACLP		MC78L08ACP
µA78L08AWC	MC78L08ACP	
µA78L08CJG		MC78L08CG
µA78L08CLP	MC78L08CP	
µA78L12ACJG		MC78L12ACG
µA78L12ACLP	MC78L12ACP	
µA78L12AHC	MC78L12ACG	
µA78L12AWC	MC78L12ACP	
µA78L12CJG		MC78L12CG
µA78L12CLP	MC78L12CP	
µA78L12HC	MC78L12CG	
µA78L12WC	MC78L12CP	
µA78L15ACJG		MC78L15ACG
µA78L15ACLP	MC78L15ACP	
µA78L15AHC	MC78L15ACG	
µA78L15AWC	MC78L15ACP	
µA78L15CJG		MC78L15CG
µA78L15CLP	MC78L15CP	
µA78L15HC	MC78L15CG	
µA78L15WC	MC78L15CP	
µA78L18AHC	MC78L18ACG	
µA78L18AWC	MC78L18ACP	
µA78L24AHC	MC78L24ACG	
µA78L24AWC	MC78L24ACP	
µA78L26AWC	MC7802ACP	
µA78MGHC		LM317MR
µA78MGHM		LM117MR
µA78MGT2C		LM317T
µA78MGU1C		LM317T
µA78MGUC		LM317MT
µA78M05CKC	MC78M05CT	
µA78M05CKD		MC78M05CT
µA78M05CLA	MC78M05CG	
µA78M05HC	MC78M05CG	
µA78M05HM		MC78M05CG
µA78M05UC	MC78M05CT	
µA78M06CKC	MC78M06CT	
µA78M06CKD		MC78M06CT
µA78M06CLA	MC78M06CG	
µA78M06HC	MC78M06CG	
µA78M06HM		MC78M06CG
µA78M06UC	MC78M06CT	
µA78M08CKC	MC78M08CT	
µA78M08CKD		MC78M08CT
µA78M08CLA	MC78M08CG	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA78M08HC	MC78M08CG	
μA78M08HM		MC78M08CG
μA78M08UC	MC78M08CT	
μA78M12CKC	MC78M12CT	
μA78M12CKD		MC78M12CT
μA78M12CLA	MC78M12CG	
μA78M12HC	MC78M12CG	
μA78M12HM		MC78M12CG
μA78M12UC	MC78M12CT	
μA78M15CKC	MC78M15CT	
μA78M15CKD		MC78M15CT
μA78M15CLA	MC78M15CG	
μA78M15HC		MC78M15CG
μA78M15HM		MC78M15CG
μA78M15UC	MC78M15CT	
μA78M18HC	MC78M18CG	
μA78M18HM		MC78M18CG
μA78M18UG	MC78M18CT	
μA78M20CKC	MC78M20CT	
μA78M20CKD		MC78M20CT
μA78M20CLA	MC78M20CG	
μA78M20HC	MC78M20CG	
μA78M20HM		MC78M20CG
μA78M20UG	MC78M20CT	
μA78M24CKC	MC78M24CT	
μA78M24CKD		MC78M24CT
μA78M24CLA	MC78M24CG	
μA78M24HC	MC78M24CG	
μA78M24HM		MC78M24CG
μA78M24UC	MC78M24CT	
μA78S40DC	μA78S40DC	
μA78S40DM	μA78S40DM	
μA78S40PC	μA78S40PC	
μA79L05AHC	MC79L05ACG	
μA79L05AWC	MC79L05ACP	
μA79L05HC	MC79L05CG	
μA79L05WC	MC79L05CP	
μA79L12AHC	MC79L12ACG	
μA79L12AWC	MC79L12ACP	
μA79L12HC	MC79L12CG	
μA79L12WC	MC79L12CP	
μA79L15AHC	MC79L15ACG	
μA79L15AWC	MC79L15ACP	
μA79L15HC	MC79L15CG	
μA79L15WC	MC79L15CP	
μA79M05AUC	MC79M05CT	
μA79M05CKC	MC79M05CT	
μA79M06AHM		MC7906CK
μA79M06AUC		MC7906CT
μA79M06CKC		MC7806CT
μA79M06HM		MC7906CK
μA79M06UC		MC7906CT
μA79M08AHM		MC7908CK
μA79M08AUC		MC7908CT
μA79M08CKC		MC7908CT
μA79M08HM		MC7908CK
μA79M08UC		MC7908CT
μA79M12AUC	MC79M12CT	
μA79M12CKC	MC79M12CT	
μA79M15AUC	MC79M15CT	
μA79M15CKC	MC79M15CT	
μA79M18AHM		MC7918CK
μA79M18AUC		MC7918CT
μA79M18HM		MC7918CK
μA79M18UC		MC7918CT

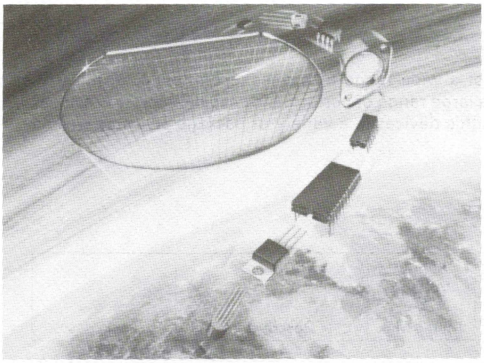
PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA79M24AHM		MC7924CK
μA79M24AUC		MC7924CT
μA79M24CKC		MC7924CT
μA79M24HM		MC7924CK
μA79M24UC		MC7924CT
μA101AD		LM101AJ
μA101AF		LM101AJ
μA101AH	LM101AH	
μA101D		LM101AJ
μA101F		LM101AJ
μA101H	LM101AH	
μA107H	LM107H	
μA108AD	LM108AJ	
μA108AF		LM108AH
μA108AH	LM108AH	
μA108D	LM108J	
μA108F	LM108F	
μA108H	LM108H	
μA109KM	LM109K	
μA117KM	LM117K	
μA201AD		LM201AJ
μA201AF		LM201AJ
μA201AH	LM201AH	
μA201D		LM201AJ
μA201F		LM201AJ
μA201H	LM201AH	
μA207H	LM207H	
μA208AD	LM208AJ	
μA208AF		LM208AH
μA208AH	LM208AH	
μA208D	LM208J	
μA208F	LM208F	
μA208H	LM208H	
μA209KM	LM209K	
μA217UV		LM217K
μA301AD		LM301AJ
μA301AH	LM301AH	
μA301AT	LM301AN	
μA307H	LM307H	
μA307T	LM307N	
μA308AD	LM308AJ	
μA308AH	LM308AH	
μA308D	LM308J	
μA308H	LM308H	
μA309KC	LM309K	
μA311T	LM311N	
μA317KC	LM317K	
μA317UC	LM317T	
μA431AWC	TL431CP	
μA494DC	TL494CJ	
μA494DM	TL494MJ	
μA494PC	TL494CN	
μA555HC	MC1455G	
μA555HM	MC1555G	
μA555TC	MC1455P1	
μA556DC	MC3456L	
μA556DM	MC3556L	
μA556PC	MC3456P	
μA565JJC	MC3412L	
μA565KJC		MC3412L
μA565SJM	MC3512L	
μA565TJM		MC3512L
μA702DC	MC1712CL	
μA702DM	MC1712L	
μA702FM		MC1712L

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
µA702HC	MC1712CG	
µA702HM	MC1712G	
µA702MJ	MC1712L	
µA702ML	MC1712G	
µA709AHM	MC1709AG	
µA709AMJG	MC1709AU	
µA709AML	MC1709AG	
µA709CJG	MC1709CU	
µA709CL	MC1709CG	
µA709CP	MC1709CP1	
µA709HC	MC1709CG	
µA709HM	MC1709G	
µA709MJG	MC1709U	
µA709ML	MC1709G	
µA709TC	MC1709CP1	
µA710CJ	MC1710CL	
µA710CP	MC1710CP	
µA710DC	MC1710CL	
µA710DM	MC1710L	
µA710HC	MC1710CG	
µA710HM	MC1710G	
µA710MJ	MC1710L	
µA710PC	MC1710CP	
µA711CJ	MC1711CL	
µA711CN	MC1711CP	
µA711DC	MC1711CL	
µA711DM	MC1711L	
µA711HC	MC1711CG	
µA711HM	MC1711G	
µA711MJ	MC1711L	
µA711PC	MC1711CP	
µA715DC		MC1741SCU
µA715DM		MC1741SU
µA715HC		MC1741SCG
µA715HM		MC1741SG
µA723CF	MC1723CL	
µA723CJ	MC1723CL	
µA723CL	MC1723CG	
µA723CN	MC1723CP	
µA723DC	MC1723CL	
µA723DM	MC1723L	
µA723F	MC1723L	
µA723HC	MC1723CG	
µA723HM	MC1723G	
µA723MJ	MC1723L	
µA723ML	MC1723G	
µA723PC	MC1723CP	
µA725AHM		LM108AH
µA725EHC		LM308AH
µA725HC		LM308AH
µA725HM		LM108AH
µA732DC		MC1310P
µA732PC		MC1310P
µA733CJ	MC1733CL	
µA733CL	MC1733CG	
µA733CN	MC1733CP	
µA733DC	MC1733CL	
µA733DM	MC1733L	
µA733FM	MC1733F	
µA733HC	MC1733CG	
µA733HM	MC1733G	
µA733MJ	MC1733L	
µA733ML	MC1733G	
µA734DC		LM311J
µA734DM		LM311J
µA734HC		LM311H
µA734HM		LM311H
µA740HC		LF355H
µA740HM		LF155H
µA741ADM		MC1741L
µA741AFM		MC1741F
µA741AHM		MC1741G
µA741CJG	MC1741CU	
µA741CL	MC1741CG	
µA741CP	MC1741CP1	
µA741DC	µA741DC	
µA741EHC		MC1741G
µA741HC	µA741HC	
µA741HM	MC1741G	
µA741MJG	MC1741U	
µA741ML	MC1741G	
µA741RC	MC1741CU	
µA741RM	MC1741U	
µA741TC	µA741TC	
µA742DC		CA3059
µA746DC		MC1327P
µA746HC		MC1327P
µA747ADM		MC1747L
µA747AHM		MC1747G
µA747CL	MC1747CG	
µA747CN	MC1747CP2	
µA747DC	MC1747CL	
µA747DM	MC1747L	
µA747EDC	MC1747CL	
µA747EHC	MC1747CG	
µA747HC	MC1747CG	
µA747HM	MC1747G	
µA747MJ	MC1747L	
µA747ML	MC1747G	
µA747PC	MC1747CP2	
µA748AHM		MC1748G
µA748CJG	MC1748CU	
µA748CL	MC1748CG	
µA748CP	MC1748CP1	
µA748HC	MC1748CG	
µA748HM	MC1748G	
µA748MJG	MC1748U	
µA748ML	MC1748G	
µA748TC	MC1748CP1	
µA753TC		MC1357P
µA754HC		MC1355P
µA754TC		MC1355P
µA757DC		MC1350P
µA757DM		MC1350P
µA758	µA758A	
µA767DC		MC1310P
µA767PC		MC1310P
µA772		MC1741S
µA775DC	LM339J	
µA775DM	LM339J	
µA775PC	LM339N	
µA776DC		MC1776CG
µA776DM		MC1776G
µA776HC	MC1776CG	
µA776HM	MC1776G	
µA776TC	MC1776CP1	
µA777CJ		LM308AJ-8
µA777CJG		LM308AJ-8
µA777CL		LM308AH
µA777CN		LM308AN

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA777CP		LM308AN
μA777DC		LM308AJ-8
μA777HC		LM308AH
μA777MJ		LM108AJ-8
μA777MJG		LM108AJ-8
μA777ML		LM108AH
μA777TC		LM308AN
μA786DC		MC1327P
μA791KC		MC1438R
μA791KM		MC1538R
μA791P5		MC1438R
μA796DC	MC1496L	
μA796DM	MC1596L	
μA796HC	MC1496G	
μA796HM	MC1596G	
μA798HC	MC3458G	
μA798HM	MC3558G	
μA798RC	MC3458U	
μA798RM	MC3558U	
μA798TC	MC3458P1	
μA799HC		MC1741G
μA799HM		MC1741G
μA1310	MC1310P	
μA1391PC	MC1391P	
μA1394PC	MC1394P	
μA1458CHC	MC1458CG	
μA1458CP	MC1458CP1	
μA1458CRC	MC1458CU	
μA1458CTC	MC1458CP1	
μA1458E	MC1458G	
μA1458HC	MC1558G	
μA1458P	MC1458P1	
μA1458RC	MC1458U	
μA1458TC	MC1458P1	
μA1558E	MC1558G	
μA1558HM	MC1558G	
μA2136PC		MC1357P
μA2240DC		MC1455U
μA2240DM		MC1555G
μA2240PC		MC1455P1
μA3026HM		CA3054
μA3045		MC3346P
μA3046DC	MC3346P	
μA3054DC	CA3054P	
μA3064PC		MC13010P
μA3065PC	MC1358P	
μA3086DM	MC3386P	
μA3301P	MC3301P	
μA3302P	MC3302P	
μA3303P	MC3303P	
μA3401P	MC3401P	
μA3403D	MC3403L	
μA3403P	MC3403P	
μA4136DC		MC4741CL
μA4136DM		MC4741L
μA4136PC		MC4741CP
μA4558HC	MC4558CG	
μA4558HM	MC4558G	
μA4558TC	MC4558CP1	
μA7805CKC	MC7805CT	
μA7805KC	MC7805CK	
μA7805KM	MC7805K	
μA7805UC	MC7805CT	
μA7805UV	MC7805BT	
μA7806CKC	MC7806CT	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
μA7806KC	MC7806CK	
μA7806KM	MC7806K	
μA7806UC	MC7806CT	
μA7806UV	MC7806BT	
μA7808CKC	MC7808CT	
μA7808KC	MC7808K	
μA7808KM	MC7808K	
μA7808UC	MC7808CT	
μA7808UV	MC7808BT	
μA7812CKC	MC7812CT	
μA7812KC	MC7812CK	
μA7812KM	MC7812K	
μA7812UC	MC7812CT	
μA7812UV	MC7812BT	
μA7815CKC	MC7815CT	
μA7815KC	MC7815CK	
μA7815KM	MC7815K	
μA7815UC	MC7815CT	
μA7815UV	MC7815BT	
μA7818CKC	MC7818CT	
μA7818KC	MC7818CK	
μA7818KM	MC7818K	
μA7818UC	MC7818CT	
μA7818UV	MC7818BT	
μA7824CKC	MC7824CT	
μA7824KC	MC7824CK	
μA7824KM	MC7824K	
μA7824UC	MC7824CT	
μA7824UV	MC7824BT	
μA7902KC	MC7902K	
μA7902KM	MC7902K	
μA7902UC	MC7902CT	
μA7905CKC	MC7905CT	
μA7905KC	MC7905CK	
μA7905KM		MC7905CK
μA7905UC	MC7905CT	
μA7905.2CKC	MC7905.2CT	
μA7906CKC	MC7906CT	
μA7906KC	MC7906CK	
μA7906KM		MC7906CK
μA7906UC	MC7906CT	
μA7908CKC	MC7908CT	
μA7908KC	MC7908CT	
μA7908KM		MC7908CK
μA7908UC		MC7908CT
μA7912CKC	MC7912CT	
μA7912KC	MC7912CK	
μA7912KM		MC7912CK
μA7912UC	MC7912CT	
μA7915CKC	MC7915CT	
μA7915KC	MC7915CK	
μA7915KM		MC7915CK
μA7915UC	MC7915CT	
μA7918CKC	MC7918CT	
μA7918KC	MC7918CK	
μA7918KM		MC7918CK
μA7918UC	MC7918CT	
μA7924CKC	MC7924CT	
μA7924KC	MC7924CK	
μA7924KM		MC7924CK
μA7924UC	MC7924CT	
μA9636ACJG	*	
μA9636ACP	*	
μPC1373		MC3373P

*To be introduced.



Selector Guides

Operational Amplifiers

Motorola offers a broad line of operational amplifiers to meet a wide range of usages. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of package styles as well as standard chips.

Single Operational Amplifiers

Noncompensated

Device	I_{IB} µA Max	V_{IO} mV Max	TC_{VIO} µV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V = 1$) MHz Typ	SR ($A_V = 1$) V/µs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Packages
Military Temperature Range (−55°C to +125°C)											
LM101A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	601,693
LM108	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	601,693
LM108A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	601,693
MC1539	0.5	3.0	15	60	50	2.0	4.2	±4.0	±18	High Slew Rate	601
MC1709	0.5	5.0	15	200	25	1.0	0.3	±3.0	±18	General Purpose	601,693
MC1709A	0.6	3.0	5.0	100	25	1.0	0.5	±3.0	±18	High Performance MC1709	601
MC1748	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	601,693
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	601,626,693,751
LM308	7.0	7.5	15	1.0	25	1.0	0.3	±3.0	±18	Precision	601,626,693
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	601,626,693
MC1439	1.0	7.5	15	100	15	2.0	4.2	±6.0	±18	High Slew Rate	601,626
MC1709C	1.5	7.5	15	500	15	1.0	0.3	±3.0	±18	General Purpose	601,626,693
MC1748C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	601,626,693
Industrial Temperature Range (−25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	601,626,693
LM208	0.002	2.0	3.0	0.2	50	1.0	0.3	±3.0	±20	Precision	601,632,693
LM208A	0.002	0.5	1.0	0.2	80	1.0	0.3	±3.0	±20	Precision	601,632,693

Internally Compensated

Device	I_{IB} µA Max	V_{IO} mV Max	TC_{VIO} µV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V = 1$) MHz Typ	SR ($A_V = 1$) V/µs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Packages
Military Temperature Range (−55°C to +125°C)											
LM11	50 pA	0.3	1.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	601,632,693
MC1536	0.02	5.0	10	3.0	100	1.0	2.0	±15	±40	High Voltage	693,601
MC1556	0.015	4.0	10	2.0	100	1.0	2.5	±3.0	±22	High Performance	601,693
MC1733	0.20	—	—	3.0 µA	90	90	—	±4.0	±8.0	Differential Wideband Video Amp	603,632
MC1741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	601,693
MC1741N	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	Low Noise	601,693
MC1741S	0.5	5.0	15	200	50	1.0	10	±3.0	±22	High Slew Rate	601,693
MC1776	0.0075	5.0	15	3.0	200	1.0	0.2	±1.5	±18	µPower, Programmable	601,632
MC35001	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	601,693
MC35001A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	601,693
MC35001B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	601,693
OP-27A	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	601,693
OP-27B	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	601,693
OP-27C	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	601,693
OP-37A	0.040	0.025	0.2	35	1000	40	17	±4.0	±22	Low Noise, Precision,	601,693
OP-37B	0.055	0.060	0.3	50	1000	40	17	±4.0	±22	Decompensated for	601,693
OP-37C	0.080	0.100	0.4	75	700	40	17	±4.0	±22	$A_V \geqslant 5$	601,693
TL071M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	693
TL081M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	693

Single Operational Amplifiers (continued)

Internally Compensated

Device	I_{IB} µA Max	V_{IO} mV Max	TC_{VIO} µV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V = 1$) MHz Typ	SR ($A_V = 1$) V/µs Typ	Supply Voltage V Min	Supply Voltage V Max	Description	Packages
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	626
LF355	200 pA	10	5.0	50 pA	50	1.0	5.0	±5.0	±18	JFET Input	601,626,693
LF355B	100 pA	5.0	5.0	20 pA	50	2.5	5.0	±5.0	±22	JFET Input	601,626,693
LF356	200 pA	10	5.0	50 pA	50	2.0	15	±5.0	±18	JFET Input	601,626,693
LF356B	100 pA	5.0	5.0	20 pA	50	5.0	12	±5.0	±22	JFET Input	601,626,693
LF357	200 pA	10	5.0	50 pA	50	3.0	75	±5.0	±18	Wideband FET Input	601,626,693
LF357B	100 pA	5.0	5.0	20 pA	50	20	50	±5.0	±22	JFET Input	601,626,693
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	626,632,646,601
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	693
LM307	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	626
MC1436	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	626,601,693
MC1456	0.03	10	12	10	70	1.0	2.5	±3.0	±18	High Performance	601,626,693
MC1733C	30	—	—	5.0 µA	80	90	—	±4.0	±8.0	Differential Wideband Video Amp	601,632,646
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	601,626,693,751
MC1741NC	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Low Noise	601,626,693
MC1741SC	0.5	6.0	15	200	20	1.0	10	±3.0	±18	High Slew Rate	601,626,693
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.5	±18	µPower, Programmable	693,626,601,751
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost µPower, Programmable	601,626,693
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	601,626,693,751
MC34001A	100 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	601,626,693,751
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	601,626,693,751
OP-27EP	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	626
OP-27FP	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	626
OP-27GP	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low Noise, Precision	626
OP-37EP	0.040	0.025	0.2	35	1000	40	17	±4.0	±22	Low Noise, Precision	626
OP-27FP	0.055	0.060	0.3	50	1000	40	17	±4.0	±22	Decompensated for	626
OP-27GP	0.080	0.100	0.4	75	700	40	17	±4.0	±22	$A_V \geqslant 5$	626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL071BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	626,693
TL081BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	626,693
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	626,693
Industrial Temperature Range (−25°C to +85°C)											
OP-27E	0.040	0.025	0.2	35	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	601,693
OP-27F	0.055	0.060	0.3	50	1000	8.0	2.8	±4.0	±22	Low Noise, Precision	601,693
OP-27G	0.080	0.100	0.4	75	700	8.0	2.8	±4.0	±22	Low, Noise, Precision	601,693
OP-37E	0.040	0.025	0.2	35	1000	40	17	±4.0	±22	Low Noise, Precision,	601,693
OP-37F	0.055	0.060	0.3	50	1000	40	17	±4.0	±22	Decompensated for	601,693
OP-37G	0.080	0.100	0.4	75	700	40	17	±4.0	±22	$A_V \geqslant 5$	601,693

Dual Operational Amplifiers

Internally Compensated

Military Temperature Range (−55°C to +125°C)

LM158	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Power Consumption)	601,632,693
MC1558	0.5	5.0	10	200	50	1.1	0.8	±3.0	±22	Dual MC1741	601,693
MC1558N	0.5	5.0	10	200	50	1.1	0.8	±3.0	±22	Low Noise	601,693
MC1558S	0.5	5.0	10	200	50	1.0	10	±3.0	±22	High Slew Rate	601,693
MC1747	0.5	5.0	10	200	50	1.0	0.5	±3.0	±22	Dual MC1741	601,632
MC3558	0.5	5.0	10	50	50	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	601,693
MC4558	0.5	5.0	10	200	50	4.0	1.5	±3.0	±22	High Frequency	601,693
MC35002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	601,693
MC35002A	75 pA	2.0	10	25 pA	50	4.0	13	±5.0	±22	JFET Input	601,693
MC35002B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	601,693
TL072M	200 pA	6.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	693
TL082M	200 pA	6.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	693

Dual Operational Amplifiers (continued)

Internally Compensated

Device	I_{IB} μA Max	V_{IO} mV Max	TC_{VIO} μV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V = 1$) MHz Typ	SR ($A_V = 1$) V/μs Typ	Supply Voltage V Min	Max	Description	Packages

Commercial Temperature Range (0°C to +70°C)

LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply (Low Power Consumption)	601,626,693,751
MC1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	601,626,693,751
MC1458C	0.70	10	10	300	20	1.1	0.8	±3.0	±18	Dual General Purpose	601,626,751
MC1458N	0.5	6.0	10	200	20	1.1	0.8	±3.0	+18	Low Noise	601,626,693
MC1458S	0.5	6.0	10	200	20	1.0	10	±3.0	±18	High Slew Rate	601,626,693
MC1747C	0.5	6.0	10	200	25	1.0	0.5	±3.0	±18	Dual MC1741	603,632,646
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply (Low Crossover Distortion)	601,626,693
MC4558C	0.5	6.0	10	200	20	3.0	1.5	±3.0	+18	High Frequency	601,626,693,751
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	601,626,693,751
MC34002A	75 pA	2.0	10	50 pA	50	4.0	13	±5.0	±18	JFET Input	601,626,693,751
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	601,626,693,751
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL072BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	626,693
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	626,693
TL082BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	626,693
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	626,693

Automotive Temperature Range (−40°C to +85°C)

MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	626
LM2904	0.25	7.0	7.0	50	100 typ	1.0	0.6	±1.5 ±3.0	±13 ±26	Split or Single Supply OP Amp	626,751

Industrial Temperature Range (−25°C to +85°C)

LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 ±3.0	±18 ±36	Split or Single Supply OP Amp	601,626,693

Noncompensated

Military Temperature Range (−55°C to +125°C)

MC1537	0.5	5.0	10	200	25	1.0	0.25	±3.0	±18	Dual MC1709	632

Commercial Temperature Range (0°C to +70°C)

MC1437	1.5	7.5	10	500	15	1.0	0.25	±3.0	±18	Dual MC1709	632,646

Quad Operational Amplifiers

Internally Compensated

Military Temperature Range (−55°C to +125°C)

LM124	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	632,646
LM148	0.10	5.0	—	25	50	1.0	0.5	±3.0	±18	Quad MC1741	632
MC3503	0.5	5.0	7.0	50	50	1.0	0.6	±1.5 +3.0	±18 +36	General Purpose Low Power	632,646
MC4741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	Quad MC1741	632,646
MC35004	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	632
MC35004B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	632
MC35074	0.50	4.5	10	75	25	4.5	10	+3.0	+44	High Performance,	632
MC35074A	0.50	2.0	10	50	50	4.5	10	+3.0	+44	Single Supply	632
MC35084	200 pA	10	10	50 pA	25	10	40	±5.0	±18	Hi-Speed, JFET Input	632
MC35084A	200 pA	5.0	10	50 pA	50	10	40	±5.0	±18	Hi-Speed, JFET Input	632
MC35085	200 pA	10	10	50 pA	25	20	80	±5.0	±18	Decompensated	632
MC35085A	200 pA	5.0	10	50 pA	50	20	80	±5.0	±18	MC35084 for $A_V \geq 2$	632
TL074M	200 pA	9.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise, JFET Input	632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	632

Quad Operational Amplifiers (continued)

Internally Compensated

Device	I_{IB} µA Max	V_{IO} mV Max	TC_{VIO} µV/°C Typ	I_{IO} nA Max	A_{vol} V/mV Min	BW ($A_V = 1$) MHz Typ	SR ($A_V = 1$) V/µs Typ	Supply Voltage V Min	Max	Description	Packages
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	646
LM324	0.25	6.0	7.0	50	25	1.0	0.6	±1.5	±16	Low Power	632,646,751A
								+3.0	+32	Consumption	
LM348	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	632,646,751A
MC3401	0.3	—	—	—	1.0	5.0	0.6	±1.5	±18	Norton Input	632,646
LM3900								+3.0	+36		
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5	±18	No Crossover	632,646,751A
								+3.0	+36	Distortion	
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	632,646
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	632,646
MC3400B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	632,646
MC34074	0.50	4.5	10	75	25	4.5	10	+3.0	+44	High Performance,	632,646
MC34074A	0.50	2.0	10	50	50	4.5	10	+3.0	+44	Single Supply	632,646
MC34084	200 pA	10	10	50 pA	25	10	40	±5.0	±18	Hi-Speed, JFET Input	632,646
MC34084A	200 pA	5.0	10	50 pA	50	10	40	±5.0	±18	Hi-Speed, JFET Input	632,646
MC34085	200 pA	10	10	50 pA	25	20	80	±5.0	±18	Decompensated	632,646
MC34085A	200 pA	5.0	10	50 pA	50	20	80	±5.0	±18	MC34084 for $A_V \geqslant 2$	632,646
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	632,646
TL074BC	200 pA	3.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	632,646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	632,646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	632,646
TL084BC	200 pA	3.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	632,646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	632,646
Automotive Temperature Range (−40°C to +85°C)											
LM2902	0.5	10	—	50	—	1.0	0.6	±1.5	±13	Differential	646,751A
								+3.0	+26	Low Power	
MC3301	0.3	—	—	—	1.0	4.0	0.6	±2.0	±15	Norton Input	646
LM2900								+4.0	+28		
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5	±18	Differential	646
								+3.0	+36	General Purpose	
MC33074	0.50	4.5	10	75	25	4.5	10	+3.0	+44	High Performance,	632,646
MC33074A	0.50	2.0	10	50	50	4.5	10	+3.0	+44	Single Supply	632,646
MC33084	200 pA	10	10	50 pA	25	10	40	±5.0	±18	Hi-Speed, JFET Input	632,646
MC33084A	200 pA	5.0	10	50 pA	50	10	40	±5.0	±18	Hi-Speed, JFET Input	632,646
MC33085	200 pA	10	10	50 pA	25	20	80	±5.0	±18	Decompensated	632,646
MC33085A	200 pA	5.0	10	50 pA	50	20	80	±5.0	±18	MC33084 for $A_V \geqslant 2$	632,646
Industrial Temperature Range (−25°C to +85°C)											
LM224	0.15	5.0	7.0	30	50	1.0	0.6	±1.5	±16	Split or Single	632,646
								±3.0	±32	Supply OP Amp	
LM248	0.20	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	632,646

Electrical Specifications

AGC Amplifiers

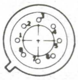
Operating Temperature Range					
−55 to +125°C	0 to +75°C	A_V dB	Band-width MHz	V_{CC}/V_{EE} Vdc	Case
MC1590	—	44 Typ @	10	+12/−	601
		4 Typ @	100		
MC1545	MC1445	19 Typ @	75	+5/−5	603,632

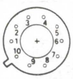
Non AGC Amplifiers

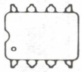
MC1733	MC1733C	52	@	40	+6/−6	603,632, 646
		40		90		
		20		120		
SE592	NE592	55	@	40	+6/−6	603,632 646
		45	@	90		

Single Operational Amplifiers (continued)

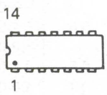
Package Styles

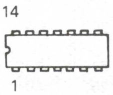


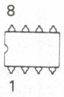


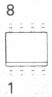


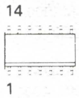
CASE	601	603	626
MATERIAL	Metal	Metal	Plastic
SUFFIX after type number	G, H	G, H	P, P1, N











CASE	632	646	693	751	751A
MATERIAL	Ceramic	Plastic	Ceramic	Plastic	Plastic
SUFFIX after type number	J, L	P, P2	J-8, J, U	D	D

High Frequency Amplifiers

A variety of high-frequency circuits with features ranging from low-cost simplicity to multi-function versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see "Circuits for Consumer Applications".

Non-AGC Amplifiers

SE/NE592 — Differential Two Stage Video Amplifier

A monolithic, two state differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C — Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 v/v. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

AGC Amplifiers

MC1545/MC1445 — Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 75 MHz bandwidth makes it suitable for high-frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

MC1590 — Wide-Band General Purpose

Has differential inputs and outputs with unneutralized power gain as high as 35 dB typical at 100 MHz in tuned amplifier service. Effective AGC voltage range from 5 to 7 volts for a 30 dB gain reduction.

Voltage Regulators

Fixed Output Voltage Regulators

- Low-cost monolithic circuits for positive and/or negative regulation at currents from 100 mA to 3.0 A
- Ideal for on-card regulation of subsystems
- Internal current limiting thermal shutdown and safe-area compensation

Fixed/Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
2	±0.1	1500	—	MC7902C	5.5/35	40	120	1.0	1, 221A
3	±0.15	100	—	MC79L03AC	4.7/30	60	72	—	29, 79
	±0.3			MC79L03C		80			
5	±0.5	100	MC78L05C	MC79L05C	6.7/30	200	60	—	29, 79
	±0.25		MC78L05AC	MC79L05AC		150			
		500	MC78M05C	MC79M05C	7/35	100	100	1.0	79, 221A
	±0.4	1500	LM109	—				1.1	1, 79
			LM209	—					
	±0.25		LM309	—		50		1.0	
	±0.35		MC7805*	—	8.0/35			0.6	1
	±0.25		MC7805B#	—	8/35	100		1.0	1, 221A
			MC7805C	MC7905C	7/35				
	±0.2		MC7805A*	—	7.5/35	10	50	0.6	1
			MC7805AC	MC7905AC			100		1, 221A
	±0.25		LM140-5*	—	7.0/35	50	50		1
	±0.2		LM140A-5*	—		10	25		
	±0.25		LM340-5	—		50	50		1, 221A
	±0.2		LM340A-5	—		10	25		
	±0.1		TL780-05C	—	7.0/35	5.0	25	0.06	221A
	±0.25	3000	MC78T05*	—	7.3/35	25	30	0.1	1
			MC78T05C	—					
	±0.2								1, 221A
			MC78T05A*	—		10	25		1
			MC78T05AC	—					1, 221A
	±0.4		LM123*	—	7.5/20	25	100		1
			LM223	—					
	±0.25		LM323	—					221A
	±0.2		LM123A	—					1
			LM223A	—		15	50		
			LM323A	—					221A
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	1, 221A
6	±0.3	500	MC78M06C		8/35	100	120	1.0	79, 221A
	±0.35	1500	MC7806*	—	9/35	60	100	0.7	1
	±0.3		MC7806B#	—	9/35	120	120		1, 221A
			MC7806C	MC7906C	8/35				
	±0.24		MC7806A*	—	8.6/35	11	50		1
			MC7806AC	—			100		1, 221A
	±0.3		LM140-6*	—	8/35	60	60		1
			LM340-6	—					1, 221A
		3000	MC78T06*	—	8.3/35	30	30	0.12	1
			MC78T06C	—					1, 221A

#T_J = −40 to +125°C
*T_J = −55 to +150°C

†Output Voltage Tolerance for Worst Case

(continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
8	±0.8	100	MC78L08C	—	9.7/30	200	80	—	29, 79
			MC78L08AC	—		175			
	±0.4	500	MC78M08C	—	10/35	100	160	1.0	79, 221A
		1500	MC7808*	—	11.5/35	80	100		1
			MC7808B#	—	11.5/35	160	160		1, 221A
			MC7808C	MC7908C	10.5/35				
	±0.3		MC7808A*	—	10.6/35	13	50		1
			MC7808AC	—			100		1, 221A
	±0.4		LM140-8*	—	10.5/35	80	80		1
			LM340-8	—					1, 221A
		3000	MC78T08*	—	10.4/35	35	30	0.16	1
			MC78T08C	—					1, 221A
12	±1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	—	29, 79
	±0.6		MC78L12AC	MC79L12AC					
		500	MC78M12C	MC79M12C	14/35	100	240	1.0	79, 221A
		1500	MC7812*	—	15.5/35	120	120	1.5	1
			MC7812B#	—		240	240		1, 221A
			MC7812C	MC7912C	14.5/35				
	±0.5		MC7812A*	—	14.8/35	18	50		1
			MC7812AC	—			100		1, 221A
	±0.6		LM140-12*	—	14.5/35	120	120	1.5	1
	±0.5		LM140A-12*	—		18	32		
	±0.6		LM340-12	—		120	120		1, 221A
	±0.5		LM340A-12	—		18	32		
	±0.24		TL780-12C	—		5.0		0.15	221A
	±0.6	3000	MC78T12*	—	14.5/35	45	30	0.24	1
			MC78T12C	—					1, 221A
	±0.5		MC78T12A*	—		18	25		1
			MC78T12AC	—					1, 221A
15	±1.5	100	MC78L15C	MC78L15C	16.7/35	300	150	—	29, 79
	±0.75		MC78L15AC	MC78L15A					
		500	MC78M15C	MC79M15C	17/35	100	300	1.0	79, 221A
		1500	MC7815*	—	18.5/35	150	150	1.8	1
			MC7815B#	—		300	300		1, 221A
			MC7815C	MC7915C	17.5/35				
	±0.6		MC7815A*	—	17.9/35	22	50		1
			MC7815AC	—			100		1, 221A
	±0.75		LM140-15*	—	17.5/35	150	150		1
	±0.6		LM140A-15*	—		22	35		
	±0.75		LM340-15	—		150	150		1, 221A
	±0.6		LM340A-15			22	35		
	±0.3		TL780-15C	—		15	60	0.18	221A
	±0.75	3000	MC78T15*	—	17.5/40	55	30	0.3	1
			MC78T15C	—					1, 221A
	±0.6		MC78T15A*	—		22	25		1
			MC78T15AC	—					1, 221A

#T_J = −40 to +125°C
*T_J = −55 to +150°C
†Output Voltage Tolerance for Worst Case

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	—	29, 79
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	—	20/35	100	360	1.0	79, 221A
		1500	MC7818*	—	22/35	180	180	2.3	1
			MC7818B#	—		360	360		1, 221A
	±0.7		MC7818C	MC7918C	21/35				
			MC7818A*	—		31	50		1
			MC7818AC	—			100		1, 221A
	±0.9		LM140-18*	—		180	180		1
			LM340-18	—					1, 221A
		3000	MC78T18*	—	20.6/40	80	30	0.36	1
			MC78T18C	—					1, 221A
20	±1.0	500	MC78M20C	—	22/40	10	400	1.1	79, 221A
24	±2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	29, 79
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C		26/40	100	480	1.2	79, 221A
		1500	MC7824*	—	28/40	240	240	3.0	1
			MC7824B#	—		480	480		1, 221A
			MC7824C	MC7924C	27/40				
	±1.0		MC7824A*	—	27.3/40	36	50		1
			MC7824AC	—			100		1, 221A
	±1.2		LM140-24*	—		240	240		1
			LM340-24	—					1, 221A
		3000	MC78T24*		26.7/40	90	30	0.48	1
			MC78T24C						1, 221A

Adjustable Output Voltage Regulators

Positive Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts		V_{in} Volts		$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max		Regulation % V_{out} @ T_A = 25°C Max		TC V_{out} Typ %/°C	T_J = °C Max	Case
			Min	Max	Min	Max		T_A = 25°C	T_C = 25°C	Line	Load			
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29, 79
	LM217L#									0.02	0.3	0.004	150	
	LM117L*											0.003		
150	MC1723	CP	2.0	37	9.5	40	3.0	1.25	—	0.1	0.3	0.003	150	646
		CG						1.0	2.1			0.003		603C
		G										0.002		
		CL						1.5	—			0.003	175	632
		L							—			0.002		
		CD						1.25	—			0.003	150	751A
250	MC1469	G	2.5	32	9.0	35	3.0	0.68	1.8	0.03	0.13	0.002	150	603
	MC1569			37	8.5	40	2.7			0.015				

#T_J = −40 to +125°C
*T_J = −55 to +150°C
†Output Voltage Tolerance for Worst Case

(continued)

Adjustable Output Voltage Regulators (continued)

Positive Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	V_{in} — V_{out} Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.0056	125	221A
	LM317M	R												80
	LM217M#									0.02	0.3	0.004	150	
	LM117M*											0.0036		
600	MC1469	R	2.5	32	9.0	35	3.0	3.0	14.0	0.03	0.05	0.002	150	614
	MC1569			37	8.5	40	2.7			0.015				
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	221A
	LM317	H, K												79, 1
	LM217#											0.004		
	LM117*									0.02	0.3	0.003	150	
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.03	0.5	0.008	125	221A
	LM350	K												1
	LM250#									0.01	0.3	0.0057	150	
	LM150*											0.0051		

#T_J = −25 to +150°C
*T_J = −55 to +150°C

Negative Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	V_{in} — V_{out} Differential Volts Min	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Max Line	Regulation % V_{out} @ T_A = 25°C Max Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
250	MC1463	G	−3.8	−32	9.0	35	3.0	0.68	1.8	0.03	0.05	0.002	150	603
	MC1563		−3.6	−33	8.5	40	2.7			0.015	0.13			
500	LM337M	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
	LM337M	R												80
	LM237M#									0.02	0.5	0.0034	150	
	LM137M*											0.0031		
600	MC1463	R	−3.8	−34	9.0	35	3.0	2.4	9.0	0.03	0.05	0.002	175	614
	MC1563		−3.6	−37	8.5	40	2.7			0.015				
1500	LM337	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
	LM337	H, K												79, 1
	LM237#									0.02	0.5	0.0034	150	
	LM137*											0.0031		

#T_J = −25 to +150°C
*T_J = −55 to +150°C

Switching Regulators

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O mA Max	V_{CC} Volts		f_o kHz		Device	Suffix	T_A °C	Case
	Min	Max	Min	Max				
40	1	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	−55 to +125	620
250*	7.0	40	1.0	300	MC34060	P	0 to +70	646
						L		632
					MC35060	L	−55 to +125	632
250	7.0	40	1.0	300	TL494	CN	0 to +70	648
						CJ		620
						IN	−25 to +.85	648
						IJ		620
						MJ	−55 to +125	620
250		>40	1.0	300	TL495**	CN	0 to +70	707
						CJ		726
						IN	−25 to +85	707
						IJ	−25 to +85	726
±400	8	40	0.1	400	SG3525A	N	0° to +70	648
					SG3525A	J	0 to +70	620
					SG2525A	N	−40 to +85	648
					SG2525A	J		620
					SG1525A	J	−55 to +125	620
±400	8	40	0.1	400	SG3527A	N	0 to +70	648
					SG3527A	J		620
					SG2527A	N	−40 to +85	648
					SG2527A	J		620
					SG1527A	J	−55 to +125	620
±200	8	40	0.001	400	SG3526	N	0 to +70	707
					SG3526	J		726
					SG2526	N	−40 to +85	707
					SG2526	J		726
					SG1526	J	−55 to +125	726
1500*	2.5	40	0.1	100	μA78S40	PC	0 to +70	648
					μA78S40	DC		620
					μA78S40	DM	−55 to +125	
1500*	2.5	40	0.1	100	MC34063	PI	0 to +70	626
					MC34063	U		693
					MC33063	PI	−40 to +85	626
					MC33063	U		693
					MC35063	U	−55 to +125	693

*Single output device
**Internal 39 V zener for <40 volt operation

Special Regulators

Floating Voltage and Current Regulators

Designed for laboratory type power supplies. Voltage is limited only by the break down voltage of associated, external, series-pass transistors.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	Device	Suffix	V_{aux} Volts Min	V_{aux} Volts Max	P_D Watts Max	$\Delta V_{ref}/V_{ref}$ % Line	$\Delta V_{ref}/V_{ref}$ % Load	$\Delta I_L/L_L$ % Max	TC V_{out} %/°C Typ	Case
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.001	632
			MC1566	L	20	35		0.004	0.004	0.1	0.006	

*Dependent on characteristics of external series-pass elements.

Dual ±15 V Tracking Regulators

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	V_{in} Volts Min	V_{in} Volts Max	Device	Suffix	P_D Watts Max	Reg_{line} mV	Reg_{load} mV	TC %/°C (T_{low} to T_{high}) Typ	T_A °C	Case
14.8	15.2	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
						R	2.4					614
					MC1568	G	0.8				−55 to +125	603C
						L	1.0					632
						R	2.4					614

Low Temperature Drift, Voltage References

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
1.235 ± 12 mV	20	20 Typ	LM385BZ-1.2	(Note 1)	1.0 (Note 2)	0 to +70	29
			LM285Z-1.2			−40 to +85	
1.235 ± 25 mV			LM385Z-1.2			0 to +70	
2.5 ± 38 mV			LM385BZ-2.5		2.0 (Note 3)		
			LM285Z-2.5			−40 to +85	
2.5 ± 75 mV			LM385Z-2.5			0 to +70	
2.5 ± 5.0 mV	±10	25	MC1400G2	3.0 (Note 4)	10 (Note 7)	0 to +70	601
		10	MC1400AG2				
		40	MC1500G2			−55 to +125	
		10	MC1500AG2				
2.5 ± 25 mV	10	40	MC1403	3.0/4.5 (Note 5)	10 (Note 8)	0 to +70	693, 79, 751
		25	MC1403A				693, 79
		55	MC1503			−55 to +125	
		25	MC1503A				

Notes:

1. Micro-Power Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 μA
2. 10 μA ≤ I_R ≤ 1.0 mA
3. 20 μA ≤ I_R ≤ 1.0 mA
4. (V_{out} ± IV) ≤ V_{in} ≤ 40 V
5. 4.5 V ≤ V_{in} ≤ 15 V
   15 V ≤ V_{in} ≤ 40 V
6. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V
7. −10 mA ≤ I_L ≤ + 10 mA
8. 0 mA ≤ I_L ≤ 10 mA

(continued)

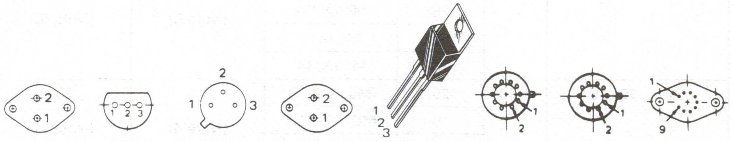
Special Regulators (continued)

Low Temperature Drift, Voltage References

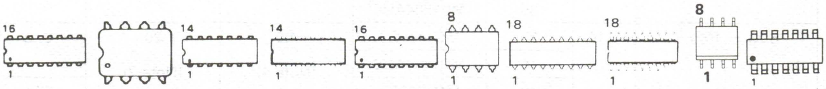
V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
5.0 ± 10 mV	±10	25	MC1400G5	4.0	20	0 to +70	693
		10	MC1400AG5	(Note 4)	(Note 7)		
		40	MC1500G5			−55 to +125	
		10	MC1500AG5				
5.0 ± 50 mV	10	40	MC1404U5	6.0	10	0 to +70	
		25	MC1404AU5	(Note 6)	(Note 8)		
		55	MC1504U5			−55 to +125	
		25	MC1504AU5				
6.25 ± 10 mV	±10	25	MC1400G6	4.0	20	0 to +70	601
		10	MC1400AG6	(Note 4)	(Note 7)		
		40	MC1500G6			−55 to +125	
		10	MC1500AG6				
6.25 ± 60 mV	10	40	MC1404U6	6.0	10	0 to +70	693
		25	MC1404AU6	(Note 6)	(Note 8)		
		55	MC1504U6			−55 to +125	
		25	MC1504AU6				
10 ± 20 mV	±10	25	MC1400G10	4.0	20	0 to +70	601
		10	MC1400AG10	(Note 4)	(Note 7)		
		40	MC1500G10			−55 to +125	
		10	MC1500AG10				
10 ± 100 mV	10	40	MC1404U10	6.0	10	0 to +70	693
		25	MC1404AU10	(Note 6)	(Note 8)		
		55	MC1504U10			−55 to +125	
		25	MC1504AU10				
2.5 to 37	100	50 Typ	TL431C	Shunt Reference Dynamic Impedance z ≤ 0.5 Ω		0 to +70	29, 626
			TL431I			−40 to +85	693
			TL431M			−55 to +125	693

Notes:
1. Micro-Power Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at $I_R = 100\ \mu A$
2. $10\ \mu A \le I_R \le 1.0$ mA
3. $20\ \mu A \le I_R \le 1.0$ mA
4. $(V_{out} + 1.0\ V) \le V_{in} \le 40\ V$
5. $4.5\ V \le V_{in} \le 15\ V/15\ V \le V_{in} \le 40\ V$
6. $(V_{out} + 2.5\ V) \le V_{in} \le 40\ V$
7. $-10\ mA \le I_L \le +10\ mA$
8. $0\ mA \le I_L \le 10\ mA$

Package Styles



CASE	1 (TO-3)	29 (TO-92)	79 (TO-39)	80 (TO-66)	221A (TO-220)	603 (TO-5 Type)	603C	614
MATERIAL	Metal	Plastic	Metal	Metal	Plastic	Metal	Metal	Metal
SUFFIX	SK, K, KC	P, Z	G, H	R	T	G, H	G	R



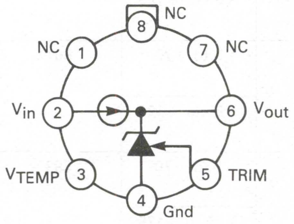
CASE	620	626	632 (TO-116)	646	648	693	707	726	751	751A
MATERIAL	Ceramic	Plastic	Ceramic	Plastic	Plastic	Ceramic	Plastic	Ceramic	Plastic	Plastic
SUFFIX	J, L	P or P1	L	P or P2	N, P	U	N	J	D	D

Voltage References

Precision Low-Voltage References

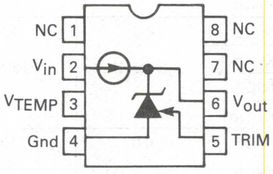
A family of precision low-voltage bandgap voltage reference, these devices are designed for applications requiring low temperature drift.

MC1400/MC1500



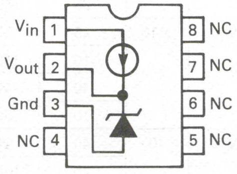
G SUFFIX — CASE 601

MC1404/MC1504



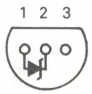
U SUFFIX — CASE 693

MC1403/MC1503



U SUFFIX — CASE 693
D SUFFIX — CASE 751

LM285/LM385



Z SUFFIX

CASE 29
(TO-92)

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
1.235 ± 12 mV	20	20 Typ	LM385BZ-1.2	(Note 1)	1.0 (Note 2)	0 to +70	29
			LM285Z-1.2			−40 to +85	
1.235 ± 25 mV			LM385Z-1.2			0 to +70	
2.5 ± 38 mV			LM385BZ-2.5		2.0 (Note 3)		
			LM285Z-2.5			−40 to +85	
2.5 ± 75 mV			LM385Z-2.5			0 to +70	
2.5 ± 5.0 mV	±10	25	MC1400G2	3.0 (Note 4)	10 (Note 7)	0 to +70	601
		10	MC1400AG2				
		40	MC1500G2			−55 to +125	
		10	MC1500AG2				
2.5 ± 25 mV	10	40	MC1403	3.0/4.5 (Note 5)	10 (Note 8)	0 to +70	693,79,751
		25	MC1403A				693, 79
		55	MC1503			−55 to +125	
		25	MC1503A				
5.0 ± 10 mV	±10	25	MC1400G5	4.0 (Note 4)	20 (Note 7)	0 to +70	693
		10	MC1400AG5				
		40	MC1500G5			−55 to +125	
		10	MC1500AG5				
5.0 ± 50 mV	10	40	MC1404U5	6.0 (Note 6)	10 (Note 8)	0 to +70	
		25	MC1404AU5				
		55	MC1504U5			−55 to +125	
		25	MC1504AU5				
6.25 ± 10 mV	±10	25	MC1400G6	4.0 (Note 4)	20 (Note 7)	0 to +70	601
		10	MC1400AG6				
		40	MC1500G6			−55 to +125	
		10	MC1500AG6				

(continued)

Precision Low-Voltage References (Continued)

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
6.25 ± 60 mV	10	40	MC1404U6	6.0 (Note 6)	10 (Note 8)	0 to +70	693
		25	MC1404AU6				
		55	MC1504U6			−55 to +125	
		25	MC1504AU6				
10 ± 20 mV	±10	25	MC1400G10	4.0 (Note 4)	20 (Note 7)	0 to +70	601
		10	MC1400AG10				
		40	MC1500G10			−55 to +125	
		10	MC1500AG10				
10 ± 100 mV	10	40	MC1404U10	6.0 (Note 6)	10 (Note 8)	0 to +70	693
		25	MC1404AU10				
		55	MC1504U10			−55 to +125	
		25	MC1504AU10				
2.5 to 37	100	50 Typ	TL431C	Shunt Reference Dynamic Impedance (z) ≤ 0.5 Ω		0 to +70	29,626,693
			TL431I			−40 to +85	
			TL431M			−55 to +125	693

Notes:
1. Micro-Power Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 µA
2. 10 µA ≤ I_R ≤ 1.0 mA
3. 20 µA ≤ I_R ≤ 1.0 mA
4. (V_{out} +1.0 V) ≤ V_{in} ≤ 40 V
5. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40 V
6. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V
7. −10 mA ≤ I_L ≤ + 10 mA
8. 0 mA ≤ I_L ≤ 10 mA

Data Conversion

The Line of data conversion products which Motorola offers, span a wide spectrum of speed and resolution/accuracy. Features including bus compatibility minimize external parts count and provide easy interface to microprocessor systems. Various technologies such as ion implantation, thin-film, laser trimming and CMOS are utilized to achieve functional capability, accuracy and production repeatability.

A-D Converters

Resolution (Bits)	Device	Accuracy (Max)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range †			Package	Technology	Comments
						M	I	C			
7	MC10315L	±½ LSB	66 ns	1 to 2 V_{p-p}	+5.0, −5.2			●	24-Pin DIP	Bipolar	Video Speed Flash, ECL Logic Levels
7	MC10317L	±½ LSB	66 ns	1 to 2 V_{p-p}	+5.0, ±5.2			●	24-Pin DIP	Bipolar	Video Speed Flash, Expandable to 8-Bits, ECL Logic Levels
8	*AM6108A	±½ LSB	2.0 μs**	±5.0 V 0 to 5.0 V 0 to 10 V	+5.0, −5.2			●	28-Pin DIP	Bipolar	μP Compatible, Three-State Outputs, includes Reference
8	MC145040	±½ LSB	50 μs**	0 to V_{DD}	+5.0, ±10%		▲		20-Pin DIP	CMOS	Requires External Clock
8	MC145041	±½ LSB	50 μs**	0 to V_{DD}	+5.0, ±10%		▲		20-Pin DIP	CMOS	Includes Internal Clock
8	MC14442	±½ LSB	32 μs	0 to V_{DD}	+5.0, ±10%		■		28-Pin DIP	CMOS	M68 μP Compatible 12-channel MUX S.A.R.
8	MC14444	±½ LSB	32 μs	0 to V_{DD}	+5.0, ±10%		■		40-Pin DIP	CMOS	M68 μP Compatible 16-channel MUX S.A.R.
8–10	MC14443/47	±0.3%	300 μs	Variable w/Supply	+5.0 to +18		■		16-Pin DIP	CMOS	μP Compatible, Single Slope, 6-channel MUX
3½ Digit	MC14433	±0.05%	40 ms	±2.0 V ±200 mV	+5.0, +8.0		■		24-Pin DIP	CMOS	Dual Slope

▱ Devices in shaded area — Refer to MOS Special Function Data Book, DL130, for further information.
* To Be Introduced.
** Includes Data Transfer Time.
† Temperature Ranges:
M ● — Military (−55°C to +125°C)
I ● — Industrial (−25°C to +85°C)
I ■ — Automotive (−40°C to +85°C)
I ▲ — Automotive (−40°C to +125°C)
C ● — Commercial (0°C to +70°C)

D-A Converters

Resolution (Bits)	Part Number	Accuracy @ 25°C (Max)	Settling Time (± ½ LSB)	Internal Reference	Supplies (V)	Temperature Range† M	I	C	Package	Technology	Comments
6	MC1406	± ½ LSB	300 ns	—	+ 5.0, − 15			●	14-Pin DIP	Bipolar	Multiplying
6	MC144110	± 2.0%	—	—	+ 5.0 to + 15			●	20-Pin DIP	CMOS	Serial input, HEX DAC, 6 outputs
6	MC144111	± 2.0%	—	—	+ 5.0 to + 15			●	14-Pin DIP	CMOS	Serial input, Quad DAC, 4 outputs
8	DAC-08	± ½ LSB	150 ns	—	± 5.0 to ± 15	●			16-Pin DIP	Bipolar	High-speed multiplying
8	DAC-08A	± ¼ LSB	135 ns	—	± 5.0 to ± 15	●			16-Pin DIP	Bipolar	High-speed multiplying
8	DAC-08C	± 1 LSB	150 ns	—	± 5.0 to ± 15			●	16-Pin DIP	Bipolar	High-speed multiplying
8	DAC-08E	± ½ LSB	150 ns	—	± 5.0 to ± 15			●	16-Pin DIP	Bipolar	High-speed multiplying
8	DAC-08H	± ¼ LSB	135 ns	—	± 5.0 to ± 15			●	16-Pin DIP	Bipolar	High-speed multiplying
8	MC1408L6	± 2 LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1408L7	± 1 LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1408L8	± ½ LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1408P6	± 2 LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1408P7	± 1 LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1408P8	± ½ LSB	300 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
8	MC1508L8	± ½ LSB	300 ns Typ	—	+ 5.0, − 15	●			16-Pin DIP	Bipolar	Multiplying
8	MC6890	± ½ LSB	300 ns	2.5 V	± 5.0 to ± 15			●	20-Pin DIP	Bipolar Thin-Film	μP Compatible Double Buffered
8	MC6890A	± ½ LSB	300 ns	2.5 V	± 5.0 to ± 15	●			20-Pin DIP	Bipolar Thin-Film	Includes Application Resistors

▱ Devices in shaded area — Refer to MOS Special Function Data Book, DL130, for further information.

(continued)

† Temperature Ranges:
M ● — Military (− 55°C to + 125°C)
I ● — Industrial (− 25°C to + 85°C)
I ■ — Automotive (− 40°C to + 85°C)
I ▲ — Automotive (− 40°C to + 125°C)
C ● — Commercial (0°C to + 70°C)

D-A Converters (continued)

Resolution (Bits)	Part Number	Accuracy @ 25°C (Max)	Settling Time (± ½ LSB)	Internal Reference	Supplies (V)	Temperature Range †			Package	Technology	Comments
						M	I	C			
8	MC10318CL6	± 2 LSB	10 ns Typ	—	− 5.2			●	16-Pin DIP	Bipolar ECL	ECL input Logic Levels
8	MC10318CL7	± 1 LSB	10 ns Typ	—	− 5.2			●	16-Pin DIP	Bipolar ECL	ECL input Logic Levels
8	MC10318L	± ½ LSB	10 ns Typ	—	− 5.2			●	16-Pin DIP	Bipolar ECL	ECL input Logic Levels
8	MC10318L9	± ¼ LSB	10 ns Typ	—	− 5.2			●	16-Pin DIP	Bipolar ECL	ECL input Logic Levels
10	MC3410	± ½ LSB	250 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
10	MC3410C	± 1 LSB	250 ns Typ	—	+ 5.0, − 15			●	16-Pin DIP	Bipolar	Multiplying
10	MC3510	± ½ LSB	250 ns Typ	—	+ 5.0, − 15	●			16-Pin DIP	Bipolar	Multiplying
12	AD562A	± ½ LSB	1.0 µs	—	+ 15, − 15		●		24-Pin DIP	Bipolar Thin-Film	Multiplying, includes Applications Resistors
12	AD562K	± ½ LSB	1.0 µs	—	+ 15, − 15			●	24-Pin DIP	Bipolar Thin-Film	Multiplying, includes Applications Resistors
12	AD562S	± ¼ LSB	1.0 µs	—	+ 15, − 15	●			24-Pin DIP	Bipolar Thin-Film	Multiplying, includes Applications Resistors
12	AD563J	± ½ LSB	1.2 µs	2.5 V	+ 5.0, − 15			●	24-Pin DIP	Bipolar Thin-Film	Includes Applications Resistors
12	AD563K	± ¼ LSB	1.2 µs	2.5 V	+ 5.0, − 15			●	24-Pin DIP	Bipolar Thin-Film	Includes Applications Resistors
12	AD563S	± ¼ LSB	1.2 µs	2.5 V	+ 5.0, − 15	●			24-Pin DIP	Bipolar Thin-Film	Includes Applications Resistors
12	AD563T	± ¼ LSB	1.2 µs	2.5 V	+ 5.0, − 15	●			24-Pin DIP	Bipolar Thin-Film	Includes Applications Resistors
12	MC3412	± ½ LSB	400 ns	10 V	+ 15, − 15			●	24-Pin DIP	Bipolar Thin-Film	High-speed, includes Applications Resistors
12	MC3512	± ½ LSB	400 ns	10 V	+ 15, − 15	●			24-Pin DIP	Bipolar Thin-Film	High-speed, includes Applications Resistors

† Temperature Ranges:
M ● — Military (− 55°C to + 125°C)
I ● — Industrial (− 25°C to + 85°C)
I ■ — Automotive (− 40°C to + 85°C)
I ▲ — Automotive (− 40°C to + 125°C)
C ● — Commercial (0°C to + 70°C)

Bus Interface

Microprocessor Bus

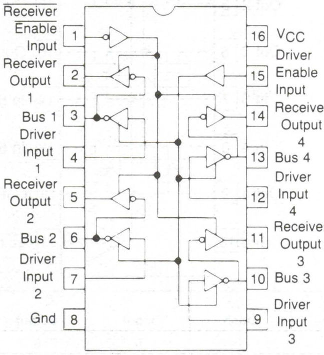
This family of devices is designed to extend the limited drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

General features include:
- Single +5.0 V Power Supply Requirement
- Three-State Logic Output
- Low Input Loading — 200 µA Max.

DATA BUS EXTENDERS

Quad, Bidirectional, with 3-State Outputs

MC8T26A/MC6880A# — Inverting



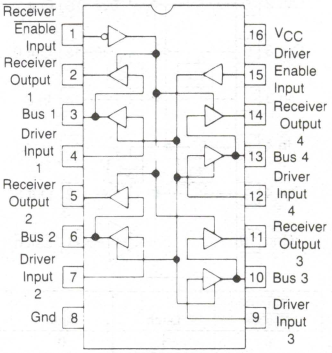
Receiver Enable Input 1
Receiver Output 1 2
Bus 1 3
Driver Input 1 4
Receiver Output 2 5
Bus 2 6
Driver Input 2 7
Gnd 8
16 VCC
15 Driver Enable Input
14 Receiver Output 4
13 Bus 4
12 Driver Input 4
11 Receiver Output 3
10 Bus 3
9 Driver Input 3

#These devices may be ordered by either of the paired numbers.

Both types:
$T_A = 0$ to $+75°C$

Packages:
L Suffix — Case 620
P Suffix — Case 648

MC8T28/MC6889# — Noninverting

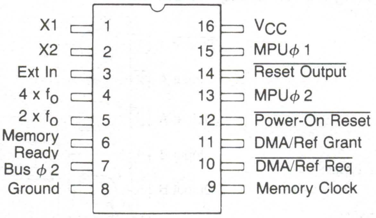


Receiver Enable Input 1
Receiver Output 1 2
Bus 1 3
Driver Input 1 4
Receiver Output 2 5
Bus 2 6
Driver Input 2 7
Gnd 8
16 VCC
15 Driver Enable Input
14 Receiver Output 4
13 Bus 4
12 Driver Input 4
11 Receiver Output 3
10 Bus 3
9 Driver Input 3

Device Number	Input Current I_{IH} µA Max	Input Current I_{IL} µA Max	I_{OHL} Output Disabled Leakage Current — High Logic State µA Max	t_{PLH}, t_{PHL} Propagation Delay Time — High to Low or Low to High ns Max
MC8T26A/MC6880A	25	−200	100	14
MC8T28/MC6889	25	−200	100	17

M6800 CLOCK GENERATOR

MC6875/MC6875A — Provides the non-overlapping two-phase clock signals for M6800 MPU systems.



X1 1
X2 2
Ext In 3
4 x fo 4
2 x fo 5
Memory Ready 6
Bus ϕ 2 7
Ground 8
16 VCC
15 MPUϕ 1
14 Reset Output
13 MPUϕ 2
12 Power-On Reset
11 DMA/Ref Grant
10 DMA/Ref Req
9 Memory Clock

MC6875L — $T_A = 0$ to $+70°C$
MC6875AL — $T_A = -55$ to $+125°C$

Package:
L Suffix — Case 620

A-D/D-A CONVERTERS

(See Precision Circuits — Data Conversion)

MPU Bus Compatible
MC6890/MC6890A — Split Supply

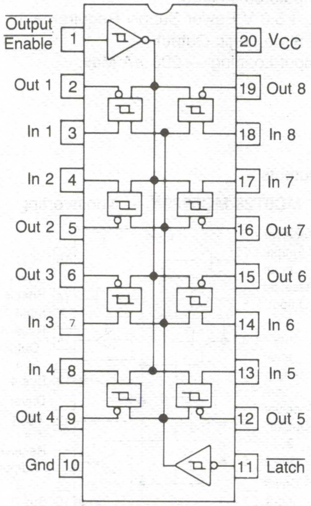
ADDRESS AND CONTROL BUS EXTENDERS

Octal, Buffer/Latch Unidirectional with 3-State Outputs

MC3482A/MC6882A# — Inverting

#These devices may be ordered by either of the paired numbers.

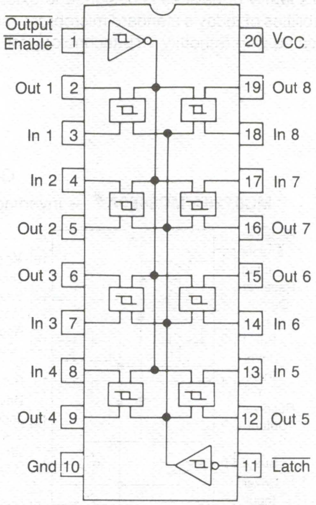
MC3482B/MC6882B# — Noninverting



$\overline{\text{Output Enable}}$ 1
Out 1 2
In 1 3
In 2 4
Out 2 5
Out 3 6
In 3 7
In 4 8
Out 4 9
Gnd 10
20 V_{CC}
19 Out 8
18 In 8
17 In 7
16 Out 7
15 Out 6
14 In 6
13 In 5
12 Out 5
11 $\overline{\text{Latch}}$

All types:
T_A = 0 to +75°C

Packages:
L Suffix — Case 732



$\overline{\text{Output Enable}}$ 1
Out 1 2
In 1 3
In 2 4
Out 2 5
Out 3 6
In 3 7
In 4 8
Out 4 9
Gnd 10
20 V_{CC}
19 Out 8
18 In 8
17 In 7
16 Out 7
15 Out 6
14 In 6
13 In 5
12 Out 5
11 $\overline{\text{Latch}}$

$\overline{\text{Output Enable}}$	Latch	Input	Output
0	1	0	1
0	1	1	0
0	0	X	Q_0
1	X	X	Z

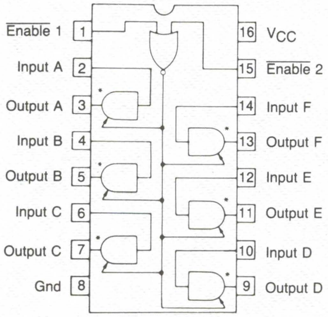
$\overline{\text{Output Enable}}$	Latch	Input	Output
0	1	0	0
0	1	1	1
0	0	X	Q_0
1	X	X	Z

Device Number	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = −20 mA Volts Min	I_{OS} mA Typ	t_{PHL} ns Typ
MC3482A/MC6882A	0.5	2.4	−80	8.0
MC3482B/MC6882B	0.5	2.4	−80	8.0

Hex, Unidirectional, with 3-State Outputs

MC8T95/MC6885# — Noninverting
MC8T96/MC6886# — Inverting
Two-input Enable controls all six buffers.

MC8T97/MC6887# — Noninverting
MC8T98/MC6888# — Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.

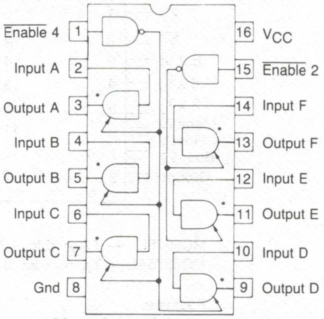


$\overline{\text{Enable}}$ 1 1
Input A 2
Output A 3
Input B 4
Output B 5
Input C 6
Output C 7
Gnd 8
16 V_{CC}
15 $\overline{\text{Enable}}$ 2
14 Input F
13 Output F
12 Input E
11 Output E
10 Input D
9 Output D

*Add inverter for MC6886/MC8T96.

All four types:
T_A = 0 to +75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648



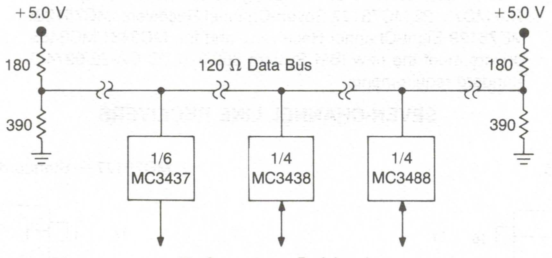
$\overline{\text{Enable}}$ 4 1
Input A 2
Output A 3
Input B 4
Output B 5
Input C 6
Output C 7
Gnd 8
16 V_{CC}
15 $\overline{\text{Enable}}$ 2
14 Input F
13 Output F
12 Input E
11 Output E
10 Input D
9 Output D

*Add inverter for MC6888/MC8T98.

V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = −5.2 mA Volts Min	I_{OS} mA Typ	t_{PLH} ns Typ	$t_{PZH/L(E)}$ ns Typ
0.5	2.4	−80	6.0	11/15

Minicomputer Bus

Transceivers and receivers for bus organized minicomputers employing 120-ohm terminated lines.


+5.0 V
+5.0 V
180
180
120 Ω Data Bus
390
390
1/6 MC3437
1/4 MC3438
1/4 MC3488
To Computer or Peripherals

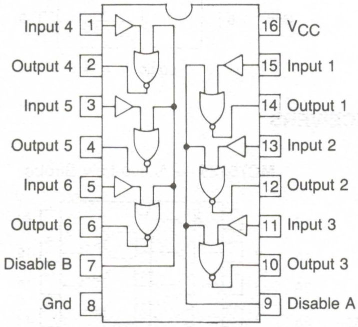
All three devices:
T_A = 0 to +70°C

Packages:

MC3437
MC3438 MC3488
L Suffix — Case 620 — J Suffix
P Suffix — Case 648 — N Suffix

HEX RECEIVERS

MC3437 — Hysteresis-equipped for improved noise immunity. DS8837 equivalent.

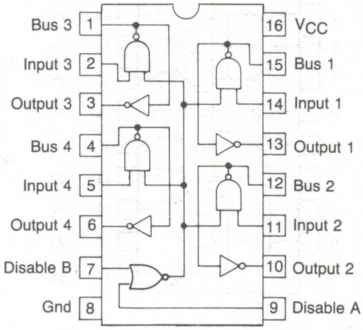

Input 4 1
Output 4 2
Input 5 3
Output 5 4
Input 6 5
Output 6 6
Disable B 7
Gnd 8
16 VCC
15 Input 1
14 Output 1
13 Input 2
12 Output 2
11 Input 3
10 Output 3
9 Disable A

$I_{I(R)}$ @ $V_{I(R)}$ = 4.0 V μA Max	Hysteresis Volts Min	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
50	0.5	30

QUAD TRANSCEIVERS

MC3438

Open-collector driver outputs allow wire-OR connection. MC3438 has hysteresis-equipped receiver for improved noise immunity. MC3438 is equivalent to the DS8838.


Bus 3 1
Input 3 2
Output 3 3
Bus 4 4
Input 4 5
Output 4 6
Disable B 7
Gnd 8
16 VCC
15 Bus 1
14 Input 1
13 Output 1
12 Bus 2
11 Input 2
10 Output 2
9 Disable A

Receiver Hysteresis Volts Min	$V_{L(BUS)}$ @ I_{BUS} = 50 mA Volts Max	I_{BUS} @ $V_{IH(BUS)}$ = 4.0 V μA Max	$t_{PLH(D)}$ @ C_L = 15 pF ns Max	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
0.25	0.7	100	25	30

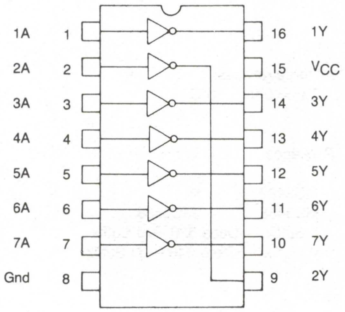
Computer Bus

NEW IBM 360/370 I/O INTERFACE

Line Receivers and Drivers designed to operate compatibly. The MC75125/MC75127 Seven-Channel Receivers, MC75128/MC75129 Eight-Channel Receivers, and the MC3481/MC3485 Drivers meet the new IBM System 360/370 I/O GA-22-6974-3 standard requirements.

SEVEN-CHANNEL LINE RECEIVERS

MC75125

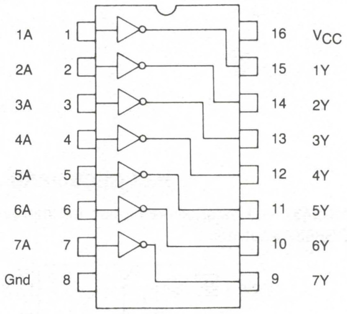

1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 1Y
15 V_{CC}
14 3Y
13 4Y
12 5Y
11 6Y
10 7Y
9 2Y

Logic: Y = $\overline{A}$

All types:
T_A = 0 to +70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648

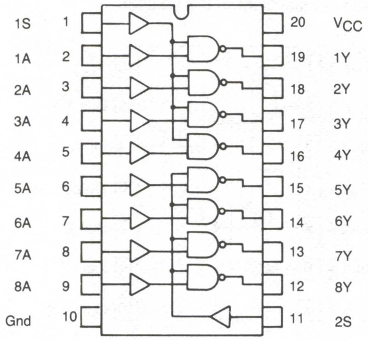
MC75127 — Standard V_{CC} and Ground Pinouts.


1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 V_{CC}
15 1Y
14 2Y
13 3Y
12 4Y
11 5Y
10 6Y
9 7Y

Logic: Y = $\overline{A}$

EIGHT-CHANNEL LINE RECEIVERS

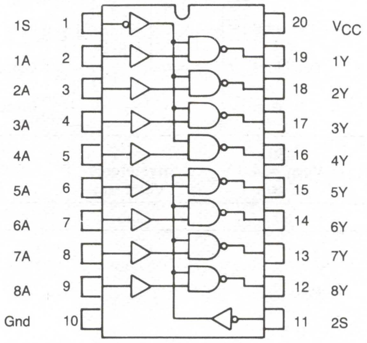
MC75128 — Active-High Strobe


1S 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
Gnd 10
20 V_{CC}
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

Packages:
L Suffix — Case 732
P Suffix — Case 738

positive logic: Y = AS

MC75129 — Active-Low Strobe


1S 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
Gnd 10
20 V_{CC}
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

Device Number	Input Resistance kΩ Min/Max	$I_{IH(R)}$ @ V_{IH} = 3.11 V mA Max	t_{PLH} @ C_L = 50 pF ns Max
MC75125/75127	7.0/20	0.42	25
MC75128/75129	7.0/20	0.42	25

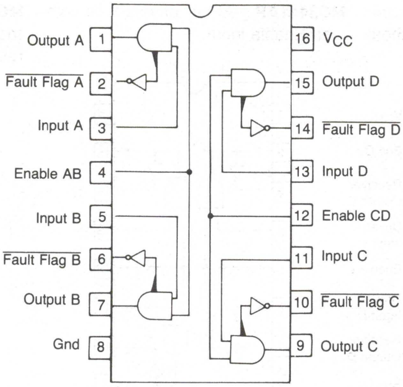
BUS INTERFACE (continued)

New IBM 360/370 I/O Interface (continued)

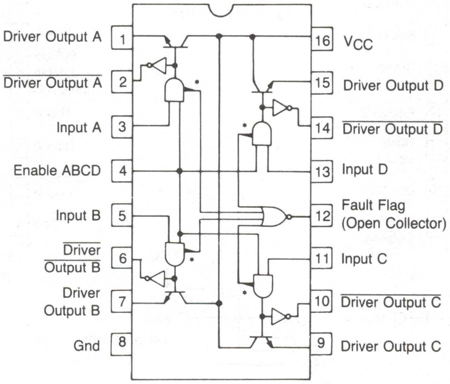
QUAD LINE DRIVERS

MC3481 — Open emitter driver with individual fault flags.

Both types:
$T_A = 0$ to $+70°C$


Output A 1
$\overline{\text{Fault Flag A}}$ 2
Input A 3
Enable AB 4
Input B 5
$\overline{\text{Fault Flag B}}$ 6
Output B 7
Gnd 8
16 V_{CC}
15 Output D
14 $\overline{\text{Fault Flag D}}$
13 Input D
12 Enable CD
11 Input C
10 $\overline{\text{Fault Flag C}}$
9 Output C

MC3485 — Open emitter driver with combined open collector fault flag and inverted outputs.


Driver Output A 1
$\overline{\text{Driver Output A}}$ 2
Input A 3
Enable ABCD 4
Input B 5
$\overline{\text{Driver Output B}}$ 6
Driver Output B 7
Gnd 8
16 V_{CC}
15 Driver Output D
14 $\overline{\text{Driver Output D}}$
13 Input D
12 Fault Flag (Open Collector)
11 Input C
10 $\overline{\text{Driver Output C}}$
9 Driver Output C

Packages:
L Suffix — Case 620
P Suffix — Case 648

Meets GA-22-6974-3

Device Number	V_{OH} @ $I_{OH} = -59.3$ mA Volts Min	I_{OS}* @ $V_O = 0$ mA Max	t_{PLH} @ $C_L = 100$ pF ns Typ
MC3481/3485	3.11	−5.0	20

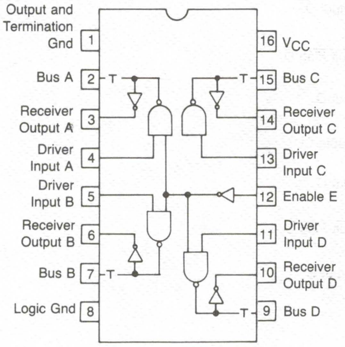
*Fault Protection

Instrumentation Bus

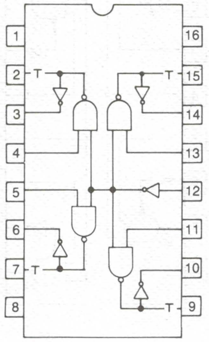
QUAD INTERFACE TRANSCEIVERS

These devices are designed to meet the GPIB bus specification of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

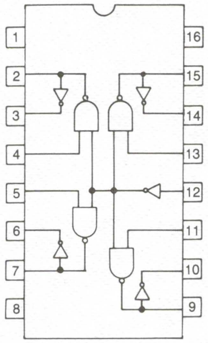
MC3440AP — Three drivers with common Enable input; one driver without Enable.


Output and Termination Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
16 V_{CC}
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D
T

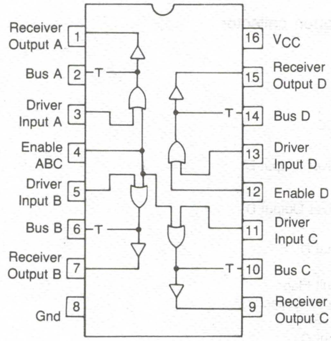
MC3441AP — Four drivers with common Enable input.


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
T

MC3443AP — Four drivers with common Enable input; no termination resistors.

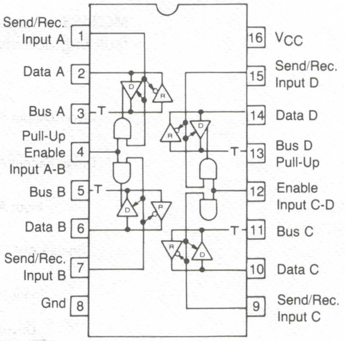

1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

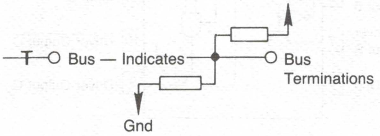
MC3446AP — For low-power instruments, including MOS.


Receiver Output A 1
Bus A 2
Driver Input A 3
Enable ABC 4
Driver Input B 5
Bus B 6
Receiver Output B 7
Gnd 8
16 V_{CC}
15 Receiver Output D
14 Bus D
13 Driver Input D
12 Enable D
11 Driver Input C
10 Bus C
9 Receiver Output C
T

All types:
T_A = 0 to +70°C

MC3448A — For common Send-Receive bus; bidirectional.


Send/Rec. Input A 1
Data A 2
Bus A 3
Pull-Up Enable Input A-B 4
Bus B 5
Data B 6
Send/Rec. Input B 7
Gnd 8
16 V_{CC}
15 Send/Rec. Input D
14 Data D
13 Bus D Pull-Up
12 Enable Input C-D
11 Bus C
10 Data C
9 Send/Rec. Input C
T
D
R


V_{CC}
T
Bus — Indicates
Bus Terminations
Gnd

Packages:
L Suffix — Case 620
P Suffix — Case 648

Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3440AP	400	0.5	30
MC3441AP	400	0.5	30
MC3443AP	400	0.5	25 (D) 22 (R)
MC3446AP	400	0.5	50 (D) 40 (R)
MC3448A	400	0.5	17 (D) 23 (R)

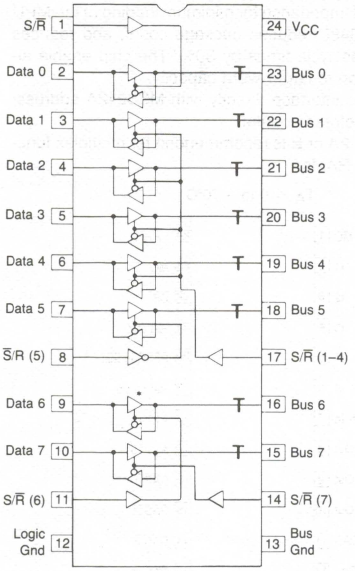
BUS INTERFACE (continued)

Instrumentation Bus (continued)

OCTAL LOW-POWER INTERFACE TRANSCEIVER

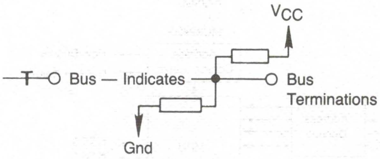
These devices are designed to meet the GPIB bus specifications of IEEE Standard 488-1978, for the interconnection of Measurement Apparatus.

MC3447 — Open collector, 3-State outputs with terminations.


S/R̄ 1
Data 0 2
Data 1 3
Data 2 4
Data 3 5
Data 4 6
Data 5 7
S̄/R (5) 8
Data 6 9
Data 7 10
S/R̄ (6) 11
Logic Gnd 12
24 VCC
23 Bus 0
22 Bus 1
21 Bus 2
20 Bus 3
19 Bus 4
18 Bus 5
17 S/R̄ (1–4)
16 Bus 6
15 Bus 7
14 S/R̄ (7)
13 Bus Gnd
*

All types:
$T_A = 0$ to $+70°C$

Packages:
L Suffix — Case 623
P3 Suffix — Case 724
(Narrow)


Bus — Indicates
VCC
Bus Terminations
Gnd

Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	t_{PHL} (Driver or Receiver) ns Max
MC3447	400	0.5	30 (D) 22 (R)*

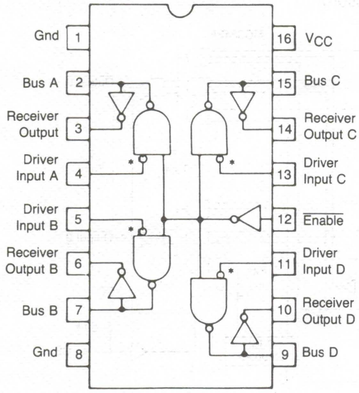
*Fast Channel.

HIGH-CURRENT PARTY-LINE BUS TRANSCEIVERS

Devices for industrial control and data communication.

MC26S10 — Inverting
MC26S11 — Noninverting

Quad transceivers with open-collector drivers and PNP-buffered inputs for MOS compatibility.


Gnd 1
Bus A 2
Receiver Output 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable
11 Driver Input D
10 Receiver Output D
9 Bus D
*
*
*
*

Packages:
L Suffix — Case 620
P Suffix — Case 648

Test	Condition	Limits
V_{OL} (D)	I_{OL} = 100 mA	0.8 Volts Max
I_O (D)	V_{OH} = 4.5 V	100 µA Max
I_{O1} (D)	V_{CC} = 0 V, V_{OH} = 4.5 V	100 µA Max
I_{IH} (D)	V_{IH} = 2.7 V	30 µA Max
I_{IL} (D)	V_{IL} = 0.4 V	−0.54 mA Max
t_P (D)	MC26S10	15 ns Max
	MC26S11	19 ns Max
t_P (R)	Both Types	15 ns Max

*Inverter on MC26S11 only.

NMOS Memories to TTL Systems

MULTIPLEXED 16-PIN RAM CONTROL
(For 4K, 16K, and 64K Dynamic Memories)

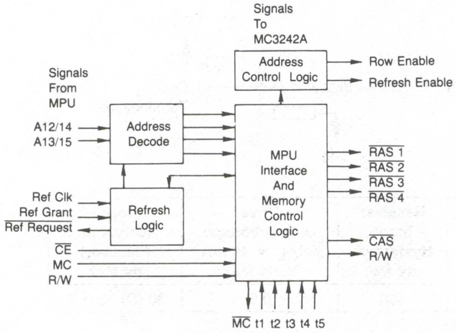
MC3480 — Memory Controller. Used with all three levels of RAM.

The memory controller chip is designed to greatly simplify the interface logic required to control popular 16-pin 4K, 16K, or 64K dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper RAS and timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

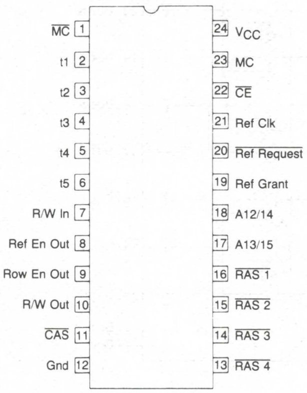
With Schottky TTL technology for high performance, and high input impedance for minimum loading of the MPU bus, the MC3480 reduces package count, and reduces system access/cycle times by 30%. The chip enable allows expansion to larger-word capacity.

Designed to interface directly with MC3242A address/multiplexers/refresh counter.

The MC3482A or B is recommended for multiplex function with 64K RAMs.


Signals To MC3242A
Address Control Logic
Row Enable
Refresh Enable
Signals From MPU
A12/14
A13/15
Address Decode
MPU Interface And Memory Control Logic
RAS 1
RAS 2
RAS 3
RAS 4
Ref Clk
Ref Grant
Ref Request
Refresh Logic
CE
MC
R/W
CAS
R/W
MC t1 t2 t3 t4 t5

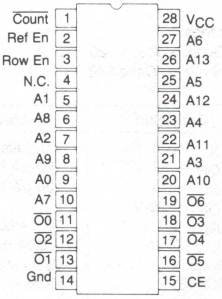
T_A = 0 to +70°C


MC 1
t1 2
t2 3
t3 4
t4 5
t5 6
R/W In 7
Ref En Out 8
Row En Out 9
R/W Out 10
CAS 11
Gnd 12
24 VCC
23 MC
22 CE
21 Ref Clk
20 Ref Request
19 Ref Grant
18 A12/14
17 A13/15
16 RAS 1
15 RAS 2
14 RAS 3
13 RAS 4

Packages:
L Suffix — Case 623
P Suffix — Case 649

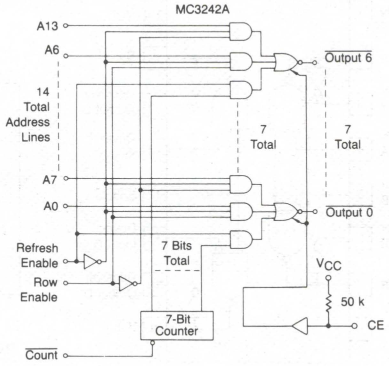
MC3242A — Designed for multiplexing 14 address lines into 7 for the 16-pin multiplexed 16K RAMs, while also containing a 7-bit refresh counter.

T_A = 0 to +75°C


Count 1
Ref En 2
Row En 3
N.C. 4
A1 5
A8 6
A2 7
A9 8
A0 9
A7 10
O0 11
O2 12
O1 13
Gnd 14
28 VCC
27 A6
26 A13
25 A5
24 A12
23 A4
22 A11
21 A3
20 A10
19 O6
18 O3
17 O4
16 O5
15 CE

Packages:
L Suffix — Case 733
P Suffix — Case 710

MC3242A — 7-Bit (16K RAM) Address Multiplexer/Refresh Counter
MC3482A/B — 8-Bit Address Multiplexer (See Microprocessor Bus Section)


MC3242A
A13
A6
14 Total Address Lines
A7
A0
Output 6
7 Total
7 Total
Output 0
Refresh Enable
Row Enable
7 Bits Total
7-Bit Counter
Count
VCC
50 k
CE

MEMORY INTERFACE and CONTROL (continued)

BUS EXTENSION
(See Microprocessor Bus)

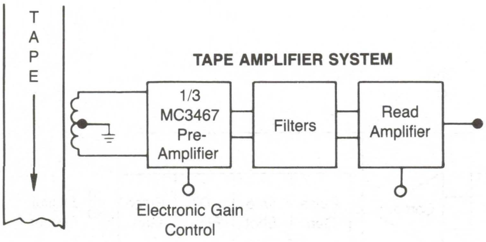
Data Bus (Bidirectional) Extenders
- MC8T26A/MC6880A — Inverting
- MC8T28A/MC6889 — Noninverting

Address Bus (Unidirectional) Extenders
- MC8T95/MC6885 — Hex Noninverting
- MC8T96/MC6886 — Hex Inverting
- MC8T97/MC6887 — Hex Noninverting
- MC8T98/MC6888 — Hex Inverting
- MC3482A/MC6882A — Octal Inverting
- MC3482B/MC6882B — Octal Noninverting

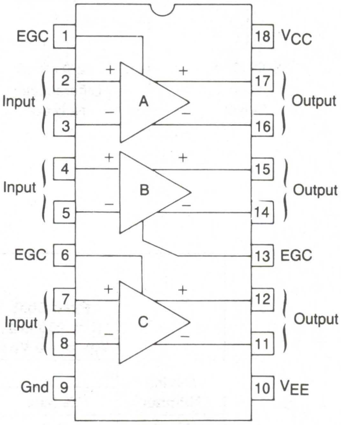
Magnetic Memories to TTL Systems

SENSE AMPLIFIERS

. . . for Magnetic Tape Memories


TAPE AMPLIFIER SYSTEM
T
A
P
E
1/3
MC3467
Pre-
Amplifier
Filters
Read
Amplifier
Electronic Gain
Control

MC3467 — Triple Preamplifier


EGC 1
Input 2
3
Input 4
5
EGC 6
Input 7
8
Gnd 9
18 VCC
17 Output
16
15 Output
14
13 EGC
12 Output
11
10 VEE
A
B
C
+
−

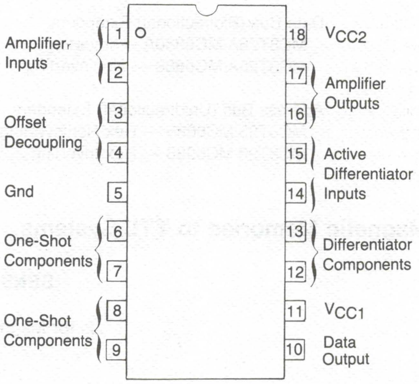
T_A = 0 to +70°C

Packages:
- L Suffix — Case 726
- P Suffix — Case 707

Magnetic Memories to TTL Systems (continued)

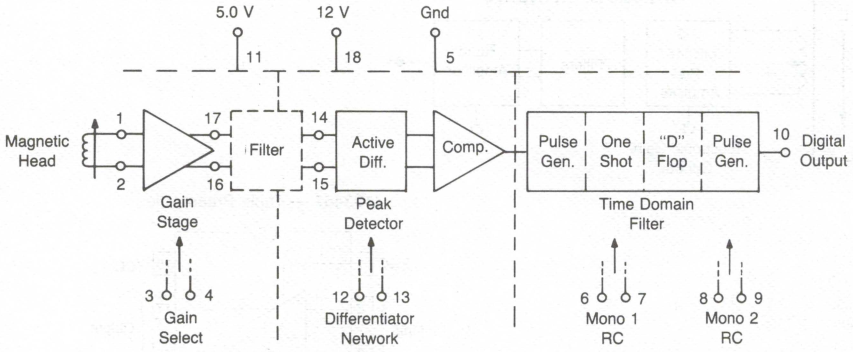
FLOPPY DISK READ AMPLIFIER SYSTEM

MC3470/MC3470A — Designed as monolithic READ Amplifier Systems for obtaining digital information from floppy disk storage. They are designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. They combine all the active circuitry to perform the floppy disk READ amplifier function in one circuit, and are guaranteed to have a maximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.


Amplifier Inputs
1
2
Offset Decoupling
3
4
Gnd
5
One-Shot Components
6
7
One-Shot Components
8
9
18
V_{CC2}
17
16
Amplifier Outputs
15
14
Active Differentiator Inputs
13
12
Differentiator Components
11
V_{CC1}
10
Data Output

T_A = 0 to +70°C

Package:
P Suffix — Case 707


5.0 V
12 V
Gnd
11
18
5
Magnetic Head
1
2
17
16
Filter
14
15
Active Diff.
Comp.
Pulse Gen.
One Shot
"D" Flop
Pulse Gen.
10
Digital Output
Gain Stage
Peak Detector
Time Domain Filter
3
4
Gain Select
12
13
Differentiator Network
6
7
Mono 1 RC
8
9
Mono 2 RC

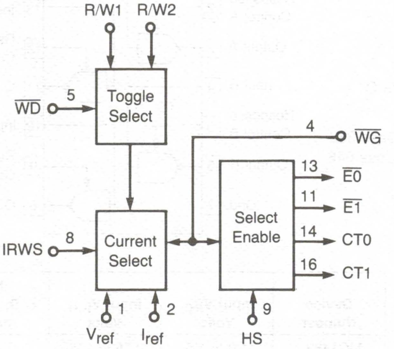
Device Number	Peak Shift (f = 250 kHz, V_{ID} = 1.0 V_{PP})	Differential Input Voltage Gain (f = 200 kHz, V_{ID} = 5.0 mV [RMS])		Input Common Mode Range (5% Max THD)	
		V/V		V	
	% Max	Min	Max	Min	Max
MC3470 MC3470A	5.0 2.0	80 100	130 130	−0.1	1.5

Magnetic Memories to TTL Systems (continued)

FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER SYSTEMS

MC3469P (Straddle Erase) — is designed to provide the entire interface between floppy disk heads and the head control and write data signals for stradle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

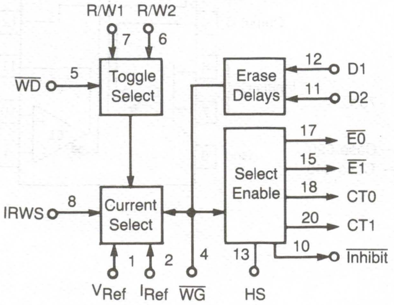

R/W1
R/W2
5
WD
Toggle Select
4
WG
13
E0
11
E1
14
CT0
16
CT1
Select Enable
8
IRWS
Current Select
1
2
9
Vref
Iref
HS

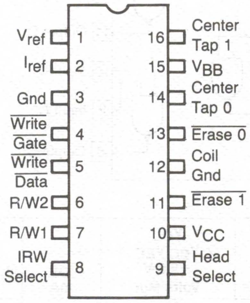
MC3471P (Tunnel Erase) — is designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additonally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

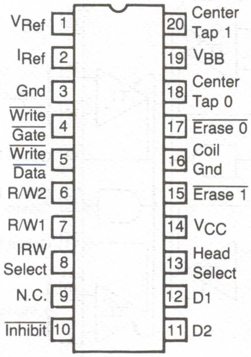
In addition, a Inhibit output is provided which indicates that the heads are active during write, degauss, or erase.


R/W1
R/W2
7
6
5
WD
Toggle Select
Erase Delays
12
D1
11
D2
17
E0
15
E1
Select Enable
18
CT0
20
CT1
8
IRWS
Current Select
10
Inhibit
1
2
4
13
VRef
IRef
WG
HS


Vref 1
Iref 2
Gnd 3
Write Gate 4
Write Data 5
R/W2 6
R/W1 7
IRW Select 8
16 Center Tap 1
15 VBB
14 Center Tap 0
13 Erase 0
12 Coil Gnd
11 Erase 1
10 VCC
9 Head Select

T_A = 0 to +70°C

Packages:
MC3469P — Case 648
MC3471P — Case 738


VRef 1
IRef 2
Gnd 3
Write Gate 4
Write Data 5
R/W2 6
R/W1 7
IRW Select 8
N.C. 9
Inhibit 10
20 Center Tap 1
19 VBB
18 Center Tap 0
17 Erase 0
16 Coil Gnd
15 Erase 1
14 VCC
13 Head Select
12 D1
11 D2

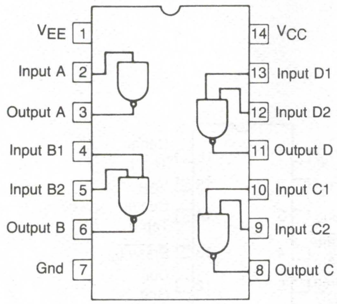
Line Drivers and Receivers for Computer/Terminal Applications

Voltage Mode

RS-232C SPECIFICATION

DRIVER

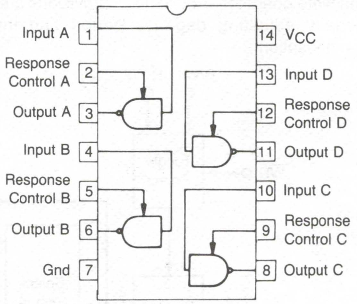
MC1488 — Quad; output current limiting.



V_{EE} 1
Input A 2
Output A 3
Input B1 4
Input B2 5
Output B 6
Gnd 7
14 V_{CC}
13 Input D1
12 Input D2
11 Output D
10 Input C1
9 Input C2
8 Output C

RECEIVERS

MC1489 — Quad; 0.25 V input hysteresis.
MC1489A — Quad; 1.1 V input hysteresis.



Input A 1
Response Control A 2
Output A 3
Input B 4
Response Control B 5
Output B 6
Gnd 7
14 V_{CC}
13 Input D
12 Response Control D
11 Output D
10 Input C
9 Response Control C
8 Output C

Both devices:
T_A = 0 to +75°C
Package:
L Suffix — Case 632
P Suffix — Case 646

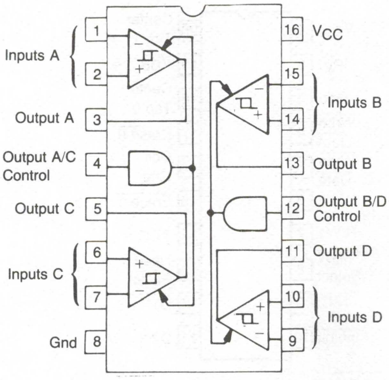
V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	−6.0	±6.0 to 12	175

Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

RS-422/423 SPECIFICATION

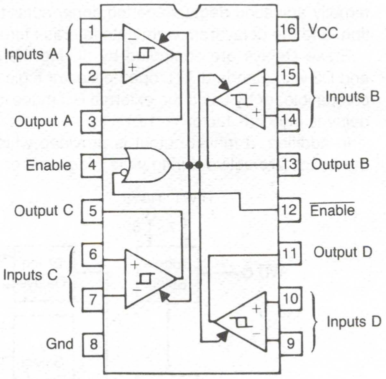
RECEIVERS

MC3486 — Quad; three-state outputs and input hysteresis, RS-422/423



Inputs A 1 2
Output A 3
Output A/C Control 4
Output C 5
Inputs C 6 7
Gnd 8
16 V_{CC}
Inputs B 15 14
13 Output B
12 Output B/D Control
11 Output D
Inputs D 10 9

AM26LS32 — Quad; three-state outputs and input hysteresis



Inputs A 1 2
Output A 3
Enable 4
Output C 5
Inputs C 6 7
Gnd 8
16 V_{CC}
Inputs B 15 14
13 Output B
12 $\overline{\text{Enable}}$
11 Output D
Inputs D 10 9

Both devices:
T_A = 0 to +70°C
Packages:
L Suffix — Case 620
P Suffix — Case 648

$V_{TH(D)}$ @ V_{ICM} = ±7.0 V Volts Max	I_{IB} @ $V_{I(D)}$ = ±10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
±0.2	±3.25	20/25	25

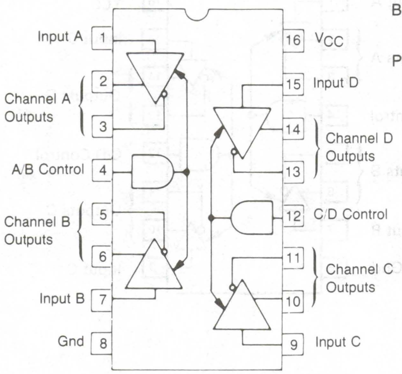
LINE DRIVERS AND RECEIVERS FOR COMPUTER/TERMINAL APPLICATIONS (continued)

RS-422/423 Specification (continued)

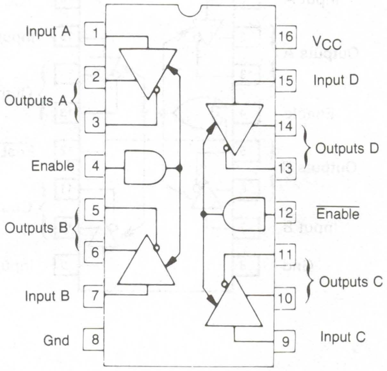
DRIVERS

MC3487 — Quad; three-state outputs, RS-422

AM26LS31 — Quad; three-state outputs, RS-422


Input A
1
Channel A Outputs
2
3
A/B Control
4
Channel B Outputs
5
6
Input B
7
Gnd
8
16
V_{CC}
15
Input D
14
Channel D Outputs
13
12
C/D Control
11
Channel C Outputs
10
9
Input C

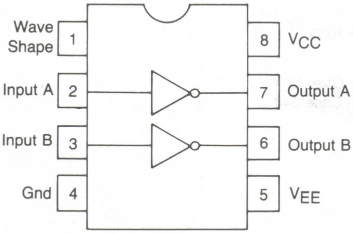
Both devices:
T_A = 0 to +70°C
Packages:
L Suffix — Case 620
P Suffix — Case 648


Input A
1
Outputs A
2
3
Enable
4
Outputs B
5
6
Input B
7
Gnd
8
16
V_{CC}
15
Input D
14
Outputs D
13
12
$\overline{\text{Enable}}$
11
Outputs C
10
9
Input C

Device Number	V_{OH} @ I_{OH} = −20 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OD} (Differential) @ R_L = 100 Ω Volts Min	t_{PLH} & t_{PHL} ns Max
MC3487	2.5	0.5	2.0	20
AM26LS31	2.5	0.5	*	20

*Not guaranteed.

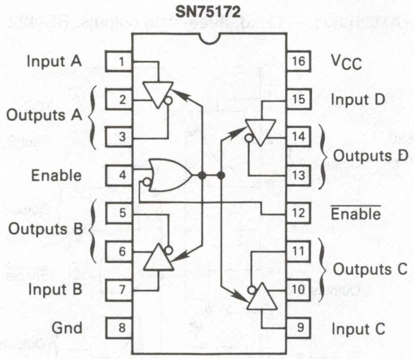
MC3488A (μA9636A) — Dual; RS-423/232C with adjustable slew rate.

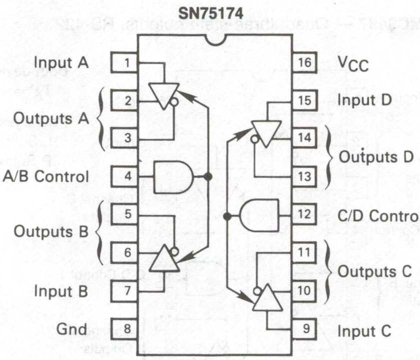

Wave Shape
1
Input A
2
Input B
3
Gnd
4
8
V_{CC}
7
Output A
6
Output B
5
V_{EE}

T_A = 0 to +70°C
Packages: P1 Suffix — Case 626
U Suffix — Case 693

RS-449/485 SPECIFICATION (PARTY LINE)

The **SN75172/SN75174** are monolithic quad differential line drivers with three-state outputs.


SN75172
Input A
Outputs A
Enable
Outputs B
Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Input D
Outputs D
$\overline{\text{Enable}}$
Outputs C
Input C


SN75174
Input A
Outputs A
A/B Control
Outputs B
Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Input D
Outputs D
C/D Control
Outputs C
Input C

TRUTH TABLE

Input	Control Inputs ($E/\overline{E}$)	Noninverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

TRUTH TABLE

Input	Control Input	Noninverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

$T_A = 0$ to $+70°C$

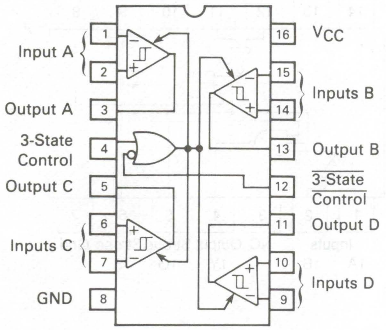
Packages:
L Suffix — Case 620
P Suffix — Case 648

RS-449/485 SPECIFICATION (PARTY LINE) (continued)

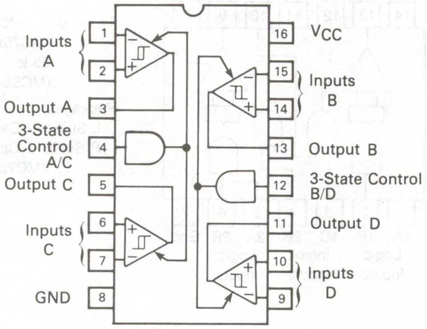
RECEIVERS

The **SN75173/SN75175** are monolithic quad differential line receivers with three-state outputs.

SN75173


Input A
1
2
Output A
3
3-State Control
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
14
Inputs B
13
Output B
12
$\overline{\text{3-State Control}}$
11
Output D
10
9
Inputs D

SN75175


Inputs A
1
2
Output A
3
3-State Control A/C
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
14
Inputs B
13
Output B
12
3-State Control B/D
11
Output D
10
9
Inputs D

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs	Enables		Output
A–B	G	$\overline{G}$	Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2 \text{ V} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs A–B	Enable	Output Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2 \text{ V} < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

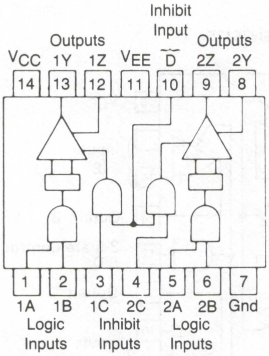
H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

LINE DRIVERS AND RECEIVERS FOR COMPUTER/TERMINAL APPLICATIONS (continued)

Differential Current Mode

DRIVERS

MC75S110 — Dual; industry standard.

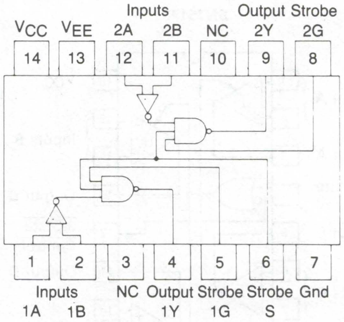

Inhibit Input
Outputs
Outputs
V_{CC}
1Y
1Z
V_{EE}
$\overline{D}$
2Z
2Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1C
2C
2A
2B
Gnd
Logic Inputs
Inhibit Inputs
Logic Inputs

T_A = 0 to +70°C
(MC75xxx)
−55 to +125°C
(MC55xxx)

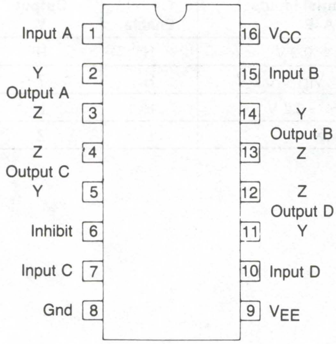
Packages:
L Suffix — Case 632
P Suffix — Case 646
(MC75xxx only)

RECEIVERS

MC75107/MC55107 — Dual; active pullup output.
MC75108/MC55108 — Dual; open-collector output.


Inputs
Output Strobe
V_{CC}
V_{EE}
2A
2B
NC
2Y
2G
14
13
12
11
10
9
8
1
2
3
4
5
6
7
Inputs
1A
1B
NC
Output
1Y
Strobe
1G
Strobe
S
Gnd

MC3453 — Quad: common inhibit input; current sink approximately 12 mA.

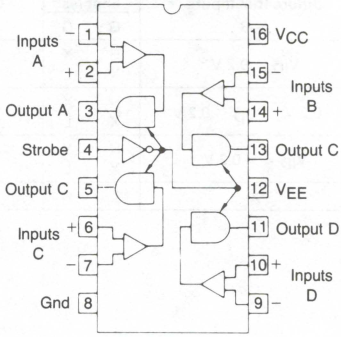

Input A
1
Y
Output A
2
Z
3
Z
Output C
4
Y
5
Inhibit
6
Input C
7
Gnd
8
16
V_{CC}
15
Input B
14
Y
Output B
13
Z
12
Z
Output D
11
Y
10
Input D
9
V_{EE}

All three devices:
T_A = 0 to +70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648

MC3450 — Quad; active pullup outputs; common three-state enable.

MC3452 — Quad; open-collector outputs.


Inputs A
−
1
+
2
Output A
3
Strobe
4
Output C
5
Inputs C
+
6
−
7
Gnd
8
16
V_{CC}
15
−
Inputs B
14
+
13
Output C
12
V_{EE}
11
Output D
10
+
Inputs D
9
−

BOTH DRIVERS

I_O (on) mA Min	I_O (off) µA Max	t_{PHL} ns Max
6.5	100	15

ALL RECEIVERS

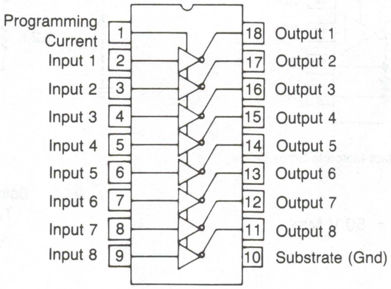
Input V_{ID} mV Max	I_{IH} @ V_{ID} = 2.0 V µA Max	I_{IL} @ V_{ID} = −2.0 V µA Max	t_{PLH} ns Max
±25	75	−10	25

Numeric Display Interface

. . . for mating multiplexed LED or gas discharge numeric displays to MOS or TTL logic systems.

Gas Discharge Drivers

MC3491 — Eight segment cathode drivers with programmable current.


Programming Current 1
Input 1 2
Input 2 3
Input 3 4
Input 4 5
Input 5 6
Input 6 7
Input 7 8
Input 8 9
18 Output 1
17 Output 2
16 Output 3
15 Output 4
14 Output 5
13 Output 6
12 Output 7
11 Output 8
10 Substrate (Gnd)

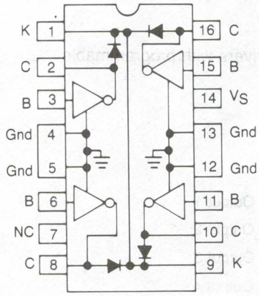
Package: L Suffix — Case 726

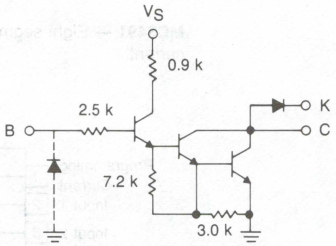
All Devices:
T_A = 0 to +70°C

Device Number	Output ON Current mA Max	Breakdown Voltage Volts Min	Current Deviation (All 8 Outputs) % Max	Output Voltage Compliance Range Volts
MC3491	1.85	80	10	5.0 to 50

Driver Arrays

ULN2068* — Quad 1.5 A, V_{CE} = 50 V Max


K 1
C 2
B 3
Gnd 4
Gnd 5
B 6
NC 7
C 8
16 C
15 B
14 VS
13 Gnd
12 Gnd
11 B
10 C
9 K

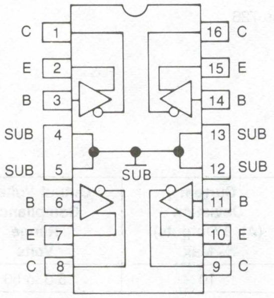

VS
0.9 k
2.5 k
B
7.2 k
3.0 k
K
C

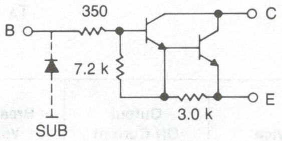
*Other members of series available. Contact Motorola Sales Office.

ULN2074* — Quad 1.5 A, V_{CE} = 50 V Max

Both devices:
T_A = 0 to +70°C

Package:
B Suffix — Case 648C


C 1
E 2
B 3
SUB 4
SUB 5
B 6
E 7
C 8
16 C
15 E
14 B
13 SUB
12 SUB
11 B
10 E
9 C
SUB

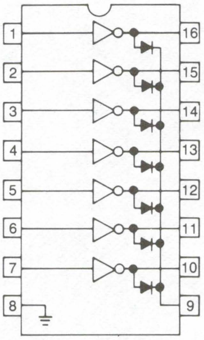

350
B
7.2 k
3.0 k
C
E
SUB

MC1411 Series/ULN2001 Series
. . . Seven Darlington transistors with output clamp diodes.

Device Number	Application	Input Element
MC1411/ULN2001	General Purpose	Basic
MC1412/ULN2002	14–25 V PMOS	Zener and Series 10.5 kΩ resistor
MC1413/ULN2003	5.0 V CMOS or TTL	Series 2.7 kΩ resistor
MC1416/ULN2004	8–18 V MOS	Series 10.5 kΩ resistor

All Types:
V_{Max} = 50 V
I_{Max} = 500 mA
T_A = 0 to +85°C

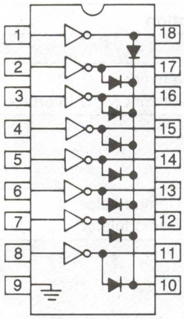
Packages:
L Suffix — Case 620
P Suffix — Case 648

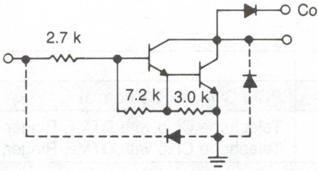

1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

PERIPHERAL INTERFACE (continued)

Driver Arrays (continued)

ULN2801,2,3,4
ULN2803 — Octal Darlington Arrays


1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10


2.7 k
7.2 k
3.0 k
Com

I_C = 500 mA
V_{CE} = 50 V Max
T_A = 0 to +70°C

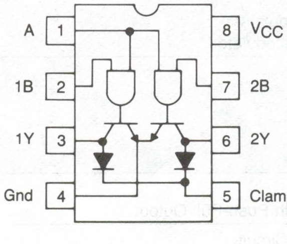
Package:
A Suffix — Case 726

Characteristics			
Device	Input Compatibility	V_{CE}(Max)/ I_C(Max)	T_A
ULN2801A	General Purpose CMOS, PMOS	50 V/500 mA	0 to +70°C
ULN2802A	14–25 Volt PMOS	50 V/500 mA	0 to +70°C
ULN2803A	TTL, 5.0 V CMOS	50 V/500 mA	0 to +70°C
ULN2804A	6–15 V CMOS, PMOS	50 V/500 mA	0 to +70°C

Dual Driver

. . . for relays, lamps, and other peripherals requiring more power than generally available from logic gates.

MC1472


A
1B
1Y
Gnd
1
2
3
4
8
7
6
5
VCC
2B
2Y
Clamp

T_A = 0 to +70°C

Packages:
P1 Suffix — Case 626
U Suffix — Case 693

$V_{(BR)CER}$ = 70 V

Telecommunications

Motorola offers the broadest product line with the widest selection of telecommunications integrated circuits in the industry, including products for station set, switching and transmission systems. The range of processes encompasses high density digital CMOS, high and low voltage linear bipolar, and laser trim. A wide variety of package options are available.

Function	Device	Description
CODEC	MC14407	PCM CODEC, D3 Format
Complete Telephone Circuit	MC34011	Telephone Chip with DTMF, Ringer, Speech Network
	MC34010	Telephone Chip with DTMF, Ringer, Speech Network MPU Interface Logic
Crosspoint Switches	MC142100	4 x 4 x 1 Analog Switch
	MC145100	4 x 4 x 1 Analog Switch
	MC3416	4 x 4 x 2 Analog Switch
CVSD	MC3417	Continuously Variable Slope Delta Modulator/Demodulator
	MC3418	Continuously Variable Slope Delta Modulator/Demodulator
Dialers	MC14408	Binary-to-Pulse Converter Subsystem
	MC14409	Binary-to-Pulse Converter Subsystem
	MC14410	2-of-8 Tone Encoder
	MC14419	2-of-8 Keypad-to-Binary Encoder
	*MC34015	2-of-8 DTMF Encoder
	MC34013	DTMF Encoder with Speech Network
Filters	MC14413	PCM Filter with Transmit Bandpass and RCV Lowpass
	MC14414	PCM Filter with Transmit and RCV Lowpass
	MC145414	Dual Tuneable Lowpass Filter
	MC145415	Dual Lowpass Filter-Linear Phase
	MC145431	Tuneable Lowpass/Bandpass Filter
	MC145433	Tuneable Notch/Bandpass Filter
	MC145440	300 Baud Modem Filter-Bell 103
	MC145441	300 Baud Modem Filter-CCITT V.21
	MC145432	Tuneable Notch/Bandpass Filter
Modems	MC14411	Bit Rate Generator
	MC14412	Universal Low-Speech (0-600BPS)
	MC145440	300 Baud Modem Filter-Bell 103
	MC145441	300 Baud Modem Filter-CCITT V.21
	MC145445	300 Baud Digital Modem
	MC145450	1200 Baud Digital Videotext Modem
	MC6860	0-600 BPS Digital Modem
	MC6172	1200/2400 BPS Digital Modulator
	MC6173	1200/2400 BPS Digital Demodulator
Monocircuit	MC14400	PCM CODEC/Filter
	MC14401	PCM CODEC/Filter
	MC14402	PCM CODEC/Filter
	MC14403	PCM CODEC/Filter
	MC14405	PCM CODEC/Filter
Ringers	MC34012	Telephone Tone Ringer
	MC34017	Telephone Tone Ringer with Push-Pull Output
SLIC	MC3419	Subscriber Loop Interface Circuit
	MC3419-1L	Subscriber Loop Interface Circuit
TSAC	MC14416	Serial Input Time Slot Assigner Circuit
	MC14417	Parallel Input Time Slot Assigner Circuit
	MC14418	Bus-Addressable Time Slot Assigner Circuit
Voice/Data	*MC145420	Four-Wire Universal Digital Loop Transceiver
	*MC145422	Two-Wire Master Universal Digital Loop Transceiver
	*MC145423	Two-Wire Master Universal Digital Loop Transceiver
	*MC145428	Data Set Interface
	*MC145429	Audio Processor

*To Be Introduced.

▱ Devices in shaded area — refer to Motorola High-Speed CMOS Logic Data.

Circuits for Consumer and Automotive Applications

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for Television, Audio, Radio, TV Games, Cordless Telephone, Automotive and Organ Applications.

Consumer Circuits

Television Subsystems

Function	Features	Case	Device
MONOMAX — 1-Chip TV	Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems	710	MC13001
	Same as Above Except For 625 Line Systems	710	MC13002
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	648C	TDA3190P
	Same as TDA1190Z Except for 750 mW Output	648C	TDA1190P

Video

Function	Features	Case	Device
1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz = 60 dB typ, AGC Range = 70 dB min	626	MC1349
	IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min	626	MC1350
1st and 2nd Video IF, AGC Keyer and Amplifier	IF Gain @ 45 MHz = 53 dB typ, AGC Range = 75 dB min, "Forward AGC" Provided for Tuner	646	MC1352
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low-Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V	626	MC1330A1
	Same as MC1330A1 Except Zero Signal dc Output Voltage of 7.8 to 9.0 V	626	MC1330A2
SAW Preamp, IF Amplifier, Detector, AGC, AFC	Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector	707	MC13010

Chroma

Function	Features	Case	Device
Chroma Demodulator	Dual Doubly Balanced Demodulator with RGB Matrix and PAL Switch	646	MC1327
Color Processor	PAL/NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays	711	TDA3301 TDA3303
Color Processor	PAL/NTSC Input, RGB Outputs, on-Chip Hue Control	724	TDA3330
Color Processor	PAL/NTSC Input, Color Difference Outputs on-Chip Hue Control	707	TDA3333

Deflection

Function	Features	Case	Device
Horizontal Processor	Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle	626	MC1391
	Same as MC1391 except designed to accept negative Flyback Input Pulse	626	MC1394

Sound

Function	Features	Case	Device
Sound IF Detector	Interchangeable with ULN2111A	646	MC1357
Sound IF Detector, dc Volume Control, Preamplifier	Excellent AMR, Interchangeable with CA3065	646	MC1358
	30 μV, 3.0 dB Limiting, Excellent AMR	646	TBA120C
Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier	Complete TV Sound System; 100 μV, 3 dB Limiting Sensitivity; 4 Watts Output; V_{CC} = 24 V; R_L = 16 Ω	648C	TDA3190P
	750 mW Output	648C	TDA1190P
Stereo Sound Control System	Stereo Balance, Volume, Bass, Treble Control	707	TCA5550

Modulators

Function	Features	Case	Device
Color TV Video Modulator	Chroma Oscillator and Clock Driver, Lead and Lag Network, Chroma Modulator, RF Oscillator, and Modulator	646	MC1372
	RF Oscillator and Modulator	626	MC1373
TV Modulator (Hi Quality)	RF Oscillator/Modulator, and FM Sound Oscillator/Modulator	646	MC1374
FM Modulator	FM Oscillator and Modulator 1.4 MHz to 14 MHz Applications	626	MC1376
RGB to PAL/NTSC Encoder	RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable	738	MC1377

Tuning System Circuits

Function	Features	Case	Device
Tuner Control	Interface Between Synthesizer and Tuner	707	MC2801
Two Modulus Prescaler	Divide-by-15 and 16. Toggle Frequency = 140 MHz	626	MC3393
Divide-by-20 Prescaler	200 MHz Toggle Frequency	626	MC3396
Remote Control Amplifier	Infrared Diode Signal Amplifier Shaper	626	MC3373

IF Amplifiers — Radio

Function	Recommended Frequency IF/RF* MHz	3 dB Limiting @ 10.7 MHz μV (RMS) Typ	AMR dB Typ	Recovered Audio Output Δf = ±75 kHz Δf = ±3 kHz* mV (RMS)	Power Supply Volts Max	Case	Device
AGC IF Amplifier	0.5–50	—	—	—	18	626	MC1350
Limiting FM-IF Amplifier	10.7	600	45	480	18	646	MC1355
Limiting IF Amplifier/Quad Detector	1–70	400	45	480	16	646	MC1357
Wideband FSK Receiver Oscillator/Mixer, FM, IF Detector, Meter Drive, Data Shaper	10.7/200*	30	50	500	15	738	MC3356
Low-Power FM-IF for Dual Conversion Scanning Receivers	0.5/10.7*	5.0	40	350*	8.0	648	MC3357
Narrow Band FM, Oscillator Mixer IF, AFT, Squelch	0.5/10.7*	2.0	40	700*	12	707	MC3359
Low Voltage Version of MC3357	0.5/10.7*	2.0	40	150*	8	648	MC3361

FM Stereo Decoders

Function	Channel Separation dB Typ	THD % Typ	Stereo/Indicator Lamp Driver mA Max	Features	Case	Device
FM Multiplex Stereo Decoder Coiless Operation	41	0.1	50	Low V_{CC} Automotive	646	MC1309
PLL Designs	41	0.1	75	High Input Signal Handling	646	MC1310
	62	0.1	100	Low Signal Blend for Noise Reduction	648	TCA4500A
	45	0.2	150	Power Supply Ripple Resection	648	μA758A

AM Stereo Decoder

Features	Function	Case	Device
CQUAM® AM Stereo Decoder	Monaural/Stereo AM Detector, Indicator	738	MC13020

Attenuators

Function	V_{CC} Range Vdc	THD % Typ	V dB Typ	Attenuation Range dB Typ	Case	Device
Electronic Attenuator	9.0–18	0.6	13	90	626	MC3340
Stereo, Volume, Bass, Treble, Balance	8.5–18	0.1	10	80	707	TCA5550

Audio

Features	(System) P_O Watts	V_{CC} Vdc Max	V_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Case	Type
Class B Audio Driver	10.0	35	89	10	165	626	MC3320
	10.0	20	32	7.0	65	626	MC3321

Transistor Arrays

Function	$I_{C(max)}$ mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Case	Device
One Differentially Connected Pair and Three Isolated Transistors	50	15	20	5.0	646	MC3346 MC3386
Dual Independent Differential Amplifiers with Associated Constant Current Transistors	50	15	20	5.0	646	CA3054
Three Differentially Connected Pairs	50	35	40	5.0	648	MC3350

Automotive Circuits

Voltage Regulator

Function	Features	Case	Device
Automotive Voltage Regulator	Designed for use with NPN Darlington, Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field Alternator Charging System	646	MC3325

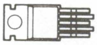
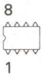
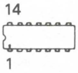
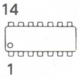
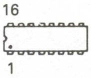
Electronic Ignition

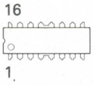
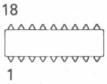
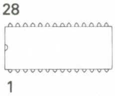
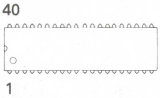
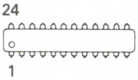
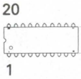
Electronic Ignition Circuit	Designed for Use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable	626	MC3334
Flip-Chip Electronic Ignition Circuit	Same as MC3334	—	MCCF3334

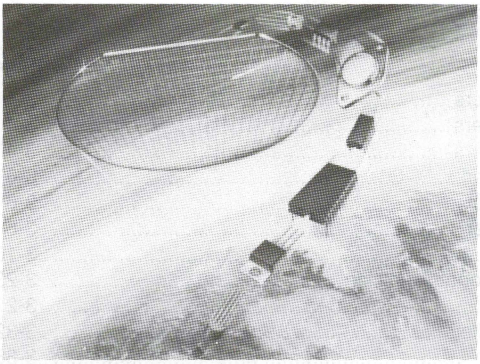
Special Function — Automotive

Programmable Frequency Switch (Engine RPM Switch)	Wide Input Frequency Range (10 Hz to 100 kHz) Adjustable Hysteresis Wide Supply Operating Range (7 to 24 V)	646, 632	MC3344
Injector Driver	Power Driver for Automotive Fuel Injection Systems, Reduced Hold Current	314B	MC3484

Package Styles

Lead Configuration					
Case	314B	626	632	646	648
Material	Plastic	Plastic	Ceramic	Plastic	Plastic
Suffix after Type Number	V	P or PL	L	P	P

Lead Configuration						
Case	648C	707	710	711	724	738
Material	Plastic	Plastic	Plastic	Plastic	Plastic	Plastic
Suffix after Type Number	P	P	P	P	P	(20 pin)



Amplifiers

AMPLIFIERS

Device	Function	Page
LF347	Family of BIFET Operational Amplifiers	3-4
LF351	Family of BIFET Operational Amplifiers	3-4
LF353	Family of BIFET Operational Amplifiers	3-4
LF355	Monolithic JFET Operational Amplifier	3-6
LF356	Monolithic JFET Operational Amplifier	3-6
LF357	Monolithic JFET Operational Amplifier	3-6
LM11,C,CL	Precision Operational Amplifiers	3-16
LM101A	General Purpose Adjustable Operational Amplifier	3-23
LM108,A	Precision Operational Amplifiers	3-27
LM124	Quad Low-Power Operational Amplifier	3-32
LM148	Quad MC1741 Operational Amplifier	3-38
LM158	Dual Low-Power Operational Amplifier	3-44
LM201A	General Purpose Adjustable Operational Amplifier	3-23
LM208,A	Precision Operational Amplifiers	3-27
LM224	Quad Low-Power Operational Amplifiers	3-32
LM248	Quad MC1741 Operational Amplifier	3-38
LM258	Dual Low-Power Operational Amplifier	3-44
LM301A	General Purpose Adjustable Operational Amplifier	3-23
LM307	Internally Compensated Monolithic Operational Amplifier	3-50
LM308,A	Precision Operational Amplifiers	3-27
LM324	Quad Low-Power Operational Amplifier	3-32
LM348	Quad MC1741 Operational Amplifier	3-38
LM358	Dual Low-Power Operational Amplifier	3-44
LM2900	Quad Single-Supply Operational Amplifier	3-152
LM2902	Quad Low-Power Operational Amplifier	3-32
LM2904	Dual Low-Power Operational Amplifier	3-44
LM3900	Quad Single-Supply Operational Amplifier	3-152
MC1436,C	High-Voltage Operational Amplifier	3-54
MC1437	Dual Operational Amplifier	3-58
MC1438R	Power Booster	3-62
MC1439	High-Slew-Rate Operational Amplifier	3-68
MC1445	Wideband Amplifier	3-76
MC1454G	1-Watt Power Amplifier	3-82
MC1456,C	High-Performance Operational Amplifier	3-86
MC1458,C,N	Dual Operational Amplifiers	3-92
MC1458S	High-Slew-Rate Dual Operational Amplifier	3-97
MC1536	High-Voltage Operational Amplifiers	3-54
MC1537	Dual Operational Amplifier	3-58
MC1538R	Power Booster	3-62
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LF347
LF351
LF353

MOTOROLA

FAMILY OF BIFET OPERATIONAL AMPLIFIERS

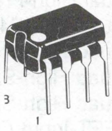
SILICON MONOLITHIC INTEGRATED CIRCUITS

JFET INPUT OPERATIONAL AMPLIFIERS

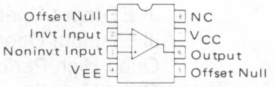
These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

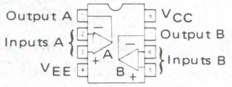
- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current – 50 pA
- Low Input Noise Voltage – 16 nV/$\sqrt{\text{Hz}}$
- Wide Gain Bandwidth – 4.0 MHz
- High Slew Rate – 13 V/μs
- Low Supply Current – 1.8 mA per Amplifier
- High Input Impedance – 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios – 100 dB



N SUFFIX
PLASTIC PACKAGE
CASE 626-04
(LF351, LF353 only)

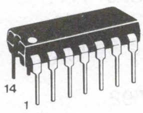


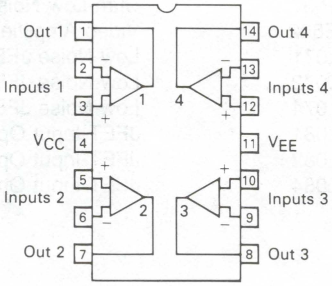
LF351
(Top View)



LF353
(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 646-05
(LF347 only)





(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_S	Continuous	
Power Dissipation at T_A = +25°C	P_D	900	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:

1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.

2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature ratings may be exceeded.

ORDERING INFORMATION

Op Amp Function	Device	Package
Single	LF351N	Plastic DIP
Dual	LF353N	Plastic DIP
Quad	LF347BN LF347N	Plastic DIP Plastic DIP

NOTES: (continued)

3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k, V_{CM} = 0)	V_{IO}							mV
T_A = +25°C		—	1.0	5.0	—	5.0	10	
0°C ≤ T_A ≤ +70°C		—	—	8.0	—	—	13	
Average Temperature Coefficient of Input Offset Voltage R_S ≤ 10 k, 0°C ≤ T_A ≤ +70°C	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0, Note 3)	I_{IO}							
T_A = +25°C		—	25	100	—	25	100	pA
0°C ≤ T_A ≤ +70°C		—	—	4.0	—	—	4.0	nA
Input Bias Current (V_{CM} = 0, Note 3)	I_{IB}							
T_A = +25°C		—	50	200	—	50	200	pA
0°C ≤ T_A ≤ +70°C		—	—	8.0	—	—	8.0	nA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large-Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
T_A = +25°C		50	100	—	25	100	—	
0°C ≤ T_A ≤ +70°C		25	—	—	15	—	—	
Output Voltage Swing (R_L = 10 k)	V_O	±12	±14	—	±12	±14	—	V
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	80	100	—	70	100	—	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	80	100	—	70	100	—	dB
Supply Current	I_D							mA
LF347		—	7.2	11	—	7.2	11	
LF351		—	—	—	—	1.8	3.4	
LF353		—	—	—	—	3.6	6.5	
Slew Rate (A_V = +1)	SR	—	13	—	—	13	—	V/μs
Gain-Bandwidth Product	BW_p	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	16	—	—	16	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	—	—	−120	—	—	−120	—	dB

For Typical Characteristic Performance Curves, refer to MC34001/34002/34004 data sheet.

LF355, LF356, LF357* LF355B, LF356B, LF357B*

MOTOROLA

Specifications and Applications Information

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 μV/°C
- Low Input Noise Current – 0.01 pA/$\sqrt{\text{Hz}}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

SERIES FEATURES

- LF355/355B — Low Power Supply Current
- LF356/356B — Wide Bandwidth
- LF357/357B — **Wider** Bandwidth Decompensated ($A_{V\min}$ = 5)

	LF355/355B	LF356/356B	LF357/357B
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 V/μs	12 V/μs	50 V/μs
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 nV/$\sqrt{\text{Hz}}$	12 nV/$\sqrt{\text{Hz}}$	12 nV/$\sqrt{\text{Hz}}$

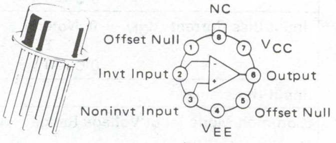
ORDERING INFORMATION

Device	Temperature Range	Package
LF355BH, H LF355BJ, J LF355BN, N	0 to +70°C 0 to +70°C 0 to +70°C	Metal Can Ceramic DIP Plastic DIP
LF356BH, H LF356BJ, J LF356BN, N	0 to +70°C 0 to +70°C 0 to +70°C	Metal Can Ceramic DIP Plastic DIP
LF357BH, H LF357BJ, J LF357BN, N	0 to +70°C 0 to +70°C 0 to +70°C	Metal Can Ceramic DIP Plastic DIP

MONOLITHIC JFET OPERATIONAL AMPLIFIERS

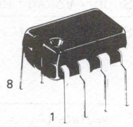
SILICON MONOLITHIC INTEGRATED CIRCUITS

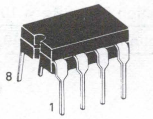
H SUFFIX
METAL PACKAGE
CASE 601-04



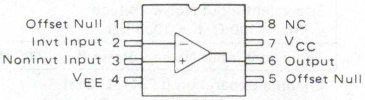
(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 626-04





J SUFFIX
CERAMIC PACKAGE
CASE 693-02



(Top View)

APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High-Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

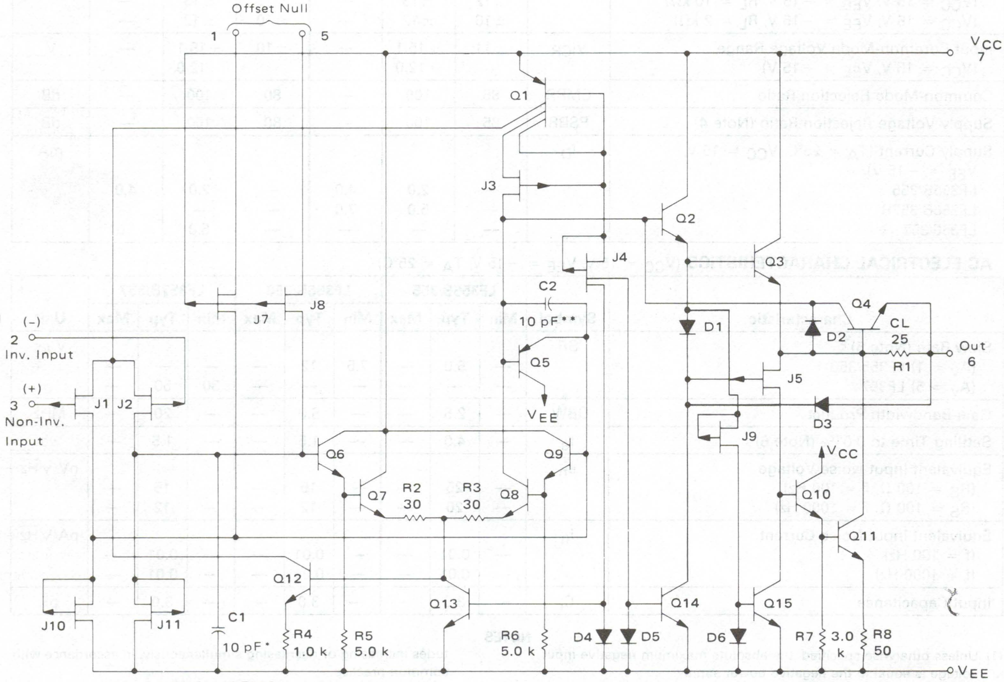
***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated ($A_{V\min}$ = 5).

MAXIMUM RATINGS

Rating	Symbol	LF355B/356B/357B	LF355/356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	T_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70		°C
Operating Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 115 100		°C
Storage Temperature Range Metal and Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125		°C

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

CIRCUIT SCHEMATIC


Offset Null
1
5
V_{CC}
7
Q1
J3
Q2
J4
Q3
C2
10 pF**
J8
J7
Q4
CL
25
R1
Out
6
D1
D2
Q5
V_{EE}
J5
D3
J9
V_{CC}
(−)
2
Inv. Input
(+)
3
Non-Inv.
Input
J1
J2
Q6
Q9
Q7
R2
30
R3
30
Q8
Q10
Q11
Q12
Q13
Q14
Q15
J10
J11
C1
10 pF*
R4
1.0 k
R5
5.0 k
R6
5.0 k
D4
D5
D6
R7
3.0
k
R8
50
V_{EE}

*C1 = 5.0 pF on LF357.
**C2 = 2.0 pF on LF357.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = −15 to −20 V for LF355B/356B/357B; V_{CC} = 15 V, V_{EE} = −15 V for LF355/356/357; T_A = 0°C to +70°C unless otherwise noted)

		LF355B/6B/7B			LF355/6/7			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0)	V_{IO}							mV
(T_A = 25°C)		—	3.0	5.0	—	3.0	10	
(Over Temperature)		—	—	6.5	—	—	13	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	μV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	μV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}							
(T_J = 25°C)		—	3.0	20	—	3.0	50	pA
(T_J ≤ 70°C)		—	—	1.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}							
(T_J = 25°C)		—	30	100	—	30	200	pA
(T_J ≤ 70°C)		—	—	5.0	—	—	8.0	nA
Input Resistance (T_J = 25°C)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V)	A_{VOL}							V/mV
(T_A = 25°C)		50	200	—	25	200	—	
(0°C ≤ T_A ≤ +70°C)		25	—	—	15	—	—	
Output Voltage Swing	V_O							V
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ)		±12	±13	—	±12	±13	—	
(V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)		±10	±12	—	±10	±12	—	
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±11	+15.1 −12.0	—	±10	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	85	100	—	80	100	—	dB
Supply Voltage Rejection Ratio (Note 4)	PSRR	85	100	—	80	100	—	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V)	I_D							mA
LF355B/355		—	2.0	4.0	—	2.0	4.0	
LF356B/357B		—	5.0	7.0	—	—	—	
LF356/357		—	—	—	—	5.0	10	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

		LF355B/355			LF356B/356			LF357B/357			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Slew Rate (Note 5)	SR										V/μs
(A_V = 1) LF355/356		—	5.0	—	7.5	12	—	—	—	—	
(A_V = 5) LF357		—	—	—	—	—	—	30	50	—	
Gain-Bandwidth Product	GBW	—	2.5	—	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	4.0	—	—	1.5	—	—	1.5	—	μs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω, f = 100 Hz)		—	25	—	—	15	—	—	15	—	
(R_S = 100 Ω, f = 1000 Hz)		—	20	—	—	12	—	—	12	—	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
(f = 1000 Hz)		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_i	—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(5) The Min. slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.

(6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF355, LF356, and LF357 series unless otherwise specified)

INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 — (LF355 SERIES)

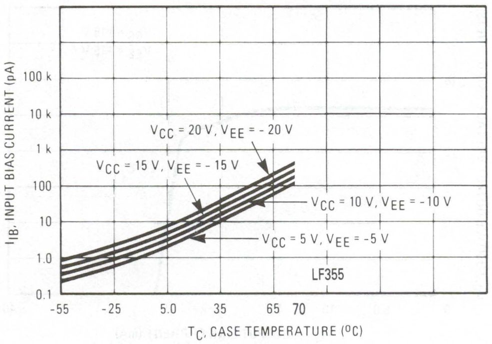


FIGURE 2 — (LF356 AND LF357 SERIES)

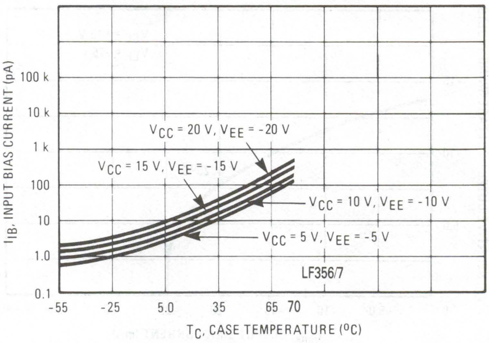


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

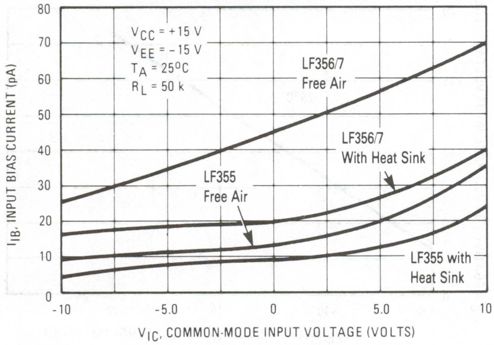
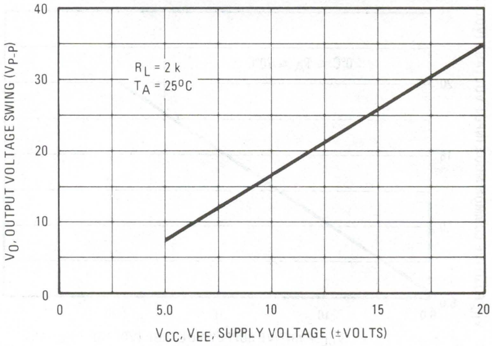


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE (LF355B/356B/357B)



SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 — (LF355 SERIES)

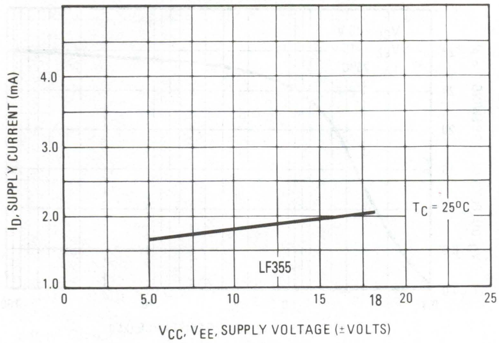
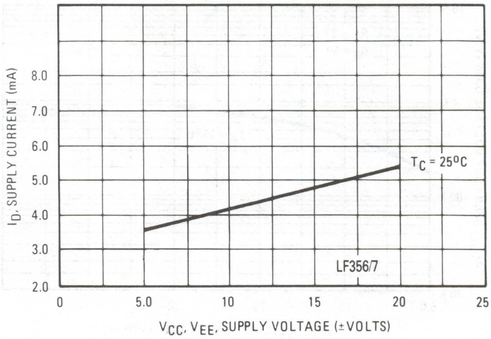


FIGURE 6 — (LF356 AND LF357 SERIES)



TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 7 — NEGATIVE CURRENT LIMIT

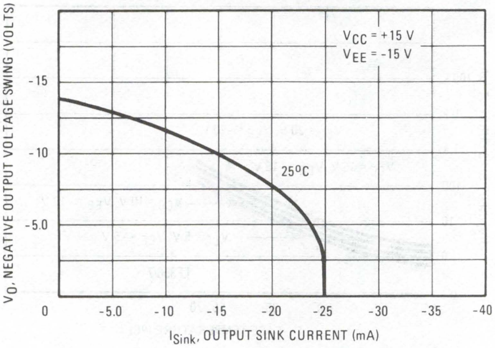


FIGURE 8 — POSITIVE CURRENT LIMIT

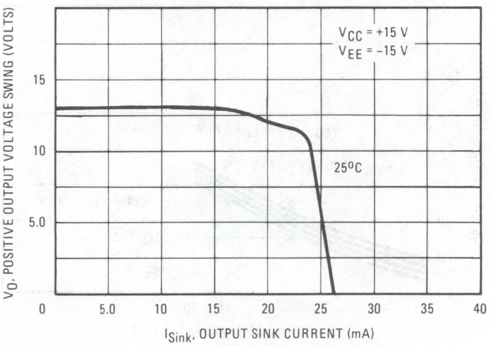


FIGURE 9 — POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

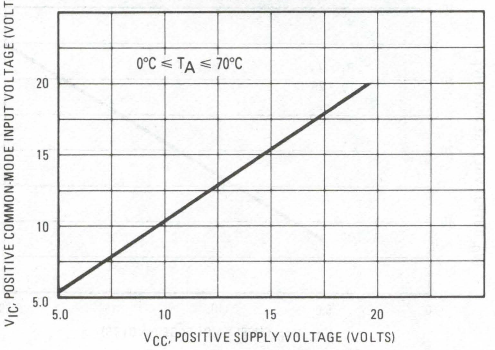


FIGURE 10 — NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

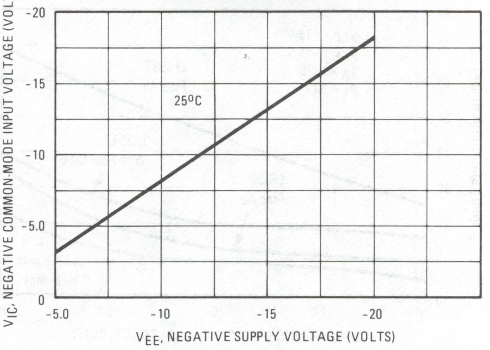


FIGURE 11 — OPEN LOOP VOLTAGE GAIN

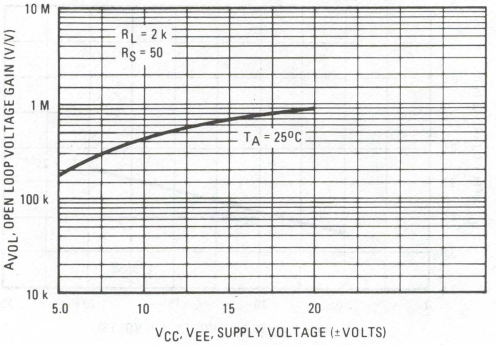
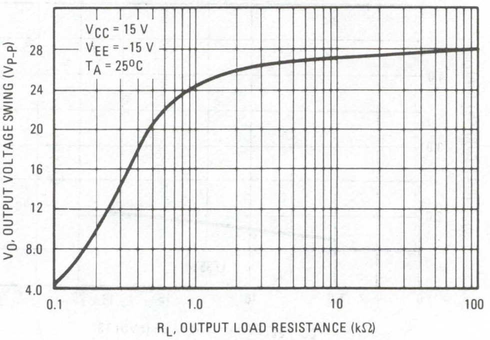


FIGURE 12 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL AC PERFORMANCE CHARACTERISTICS

GAIN BANDWIDTH PRODUCT

FIGURE 13 — (LF355 SERIES)

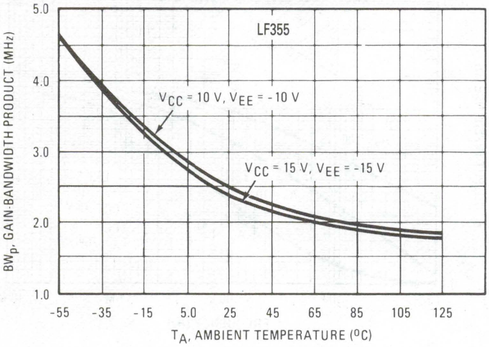
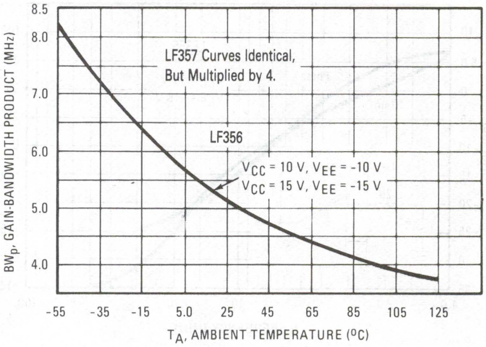


FIGURE 14 — (LF356/357 SERIES)



INVERTER SETTLING TIME

FIGURE 15 — (LF355 SERIES)

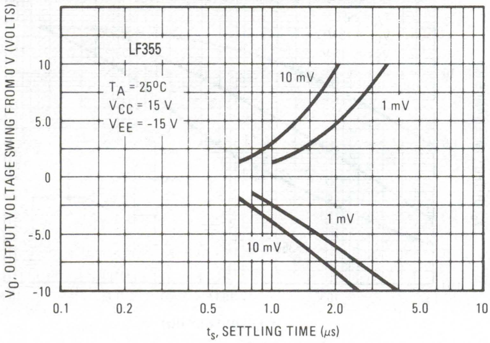


FIGURE 16 — (LF356 AND LF357 SERIES)

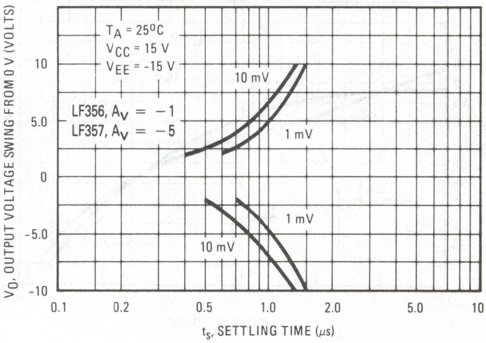


FIGURE 17 — NORMALIZED SLEW RATE

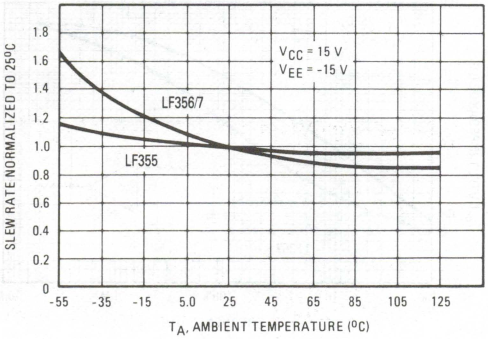
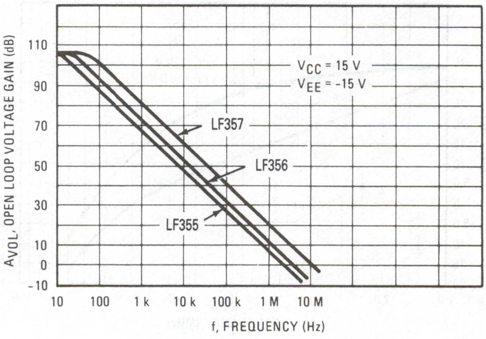


FIGURE 18 — OPEN LOOP FREQUENCY RESPONSE



TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

BODE PLOT

FIGURE 19 — (LF355 SERIES)

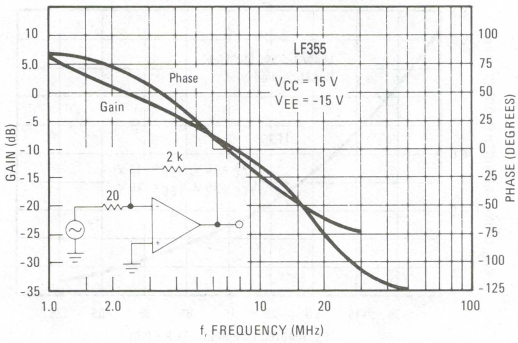


FIGURE 20 — (LF356 SERIES)

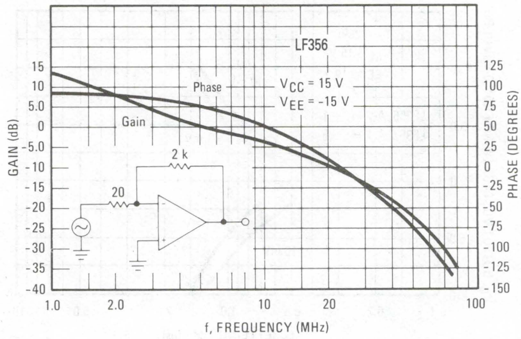
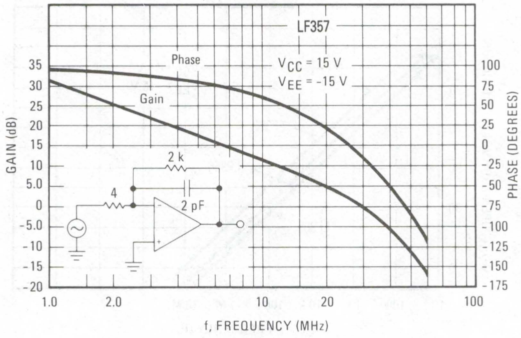


FIGURE 21 — (LF357 SERIES)



OUTPUT IMPEDANCE

FIGURE 22 — (LF355 SERIES)

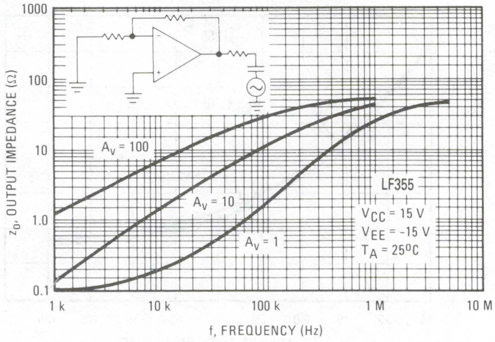


FIGURE 23 — (LF356 SERIES)

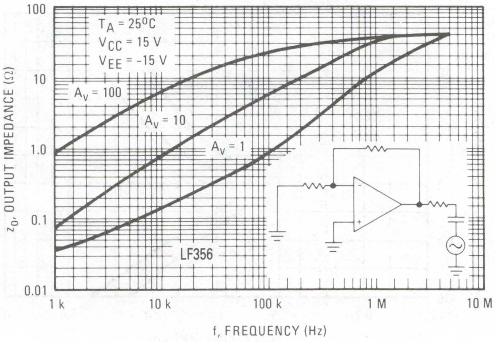
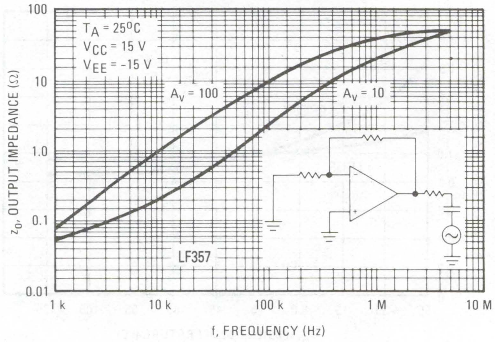


FIGURE 24 — (LF357 SERIES)



TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 25 — COMMON-MODE REJECTION RATIO

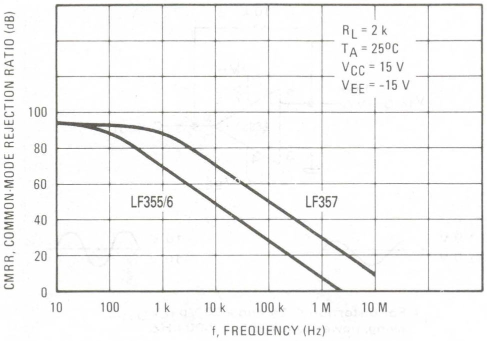
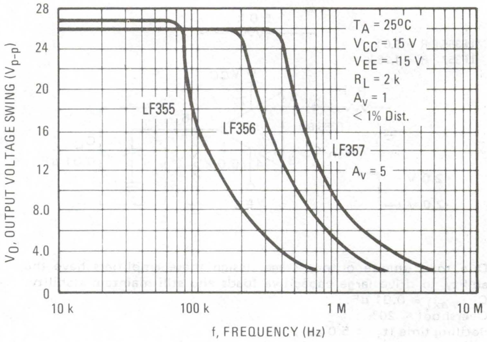


FIGURE 26 — UNDISTORTED OUTPUT VOLTAGE SWING



POWER SUPPLY VOLTAGE REJECTION RATIO

FIGURE 27 — (LF355 SERIES)

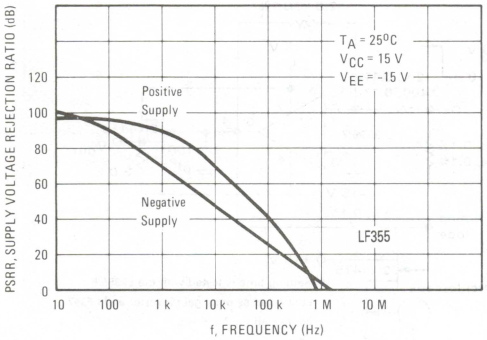
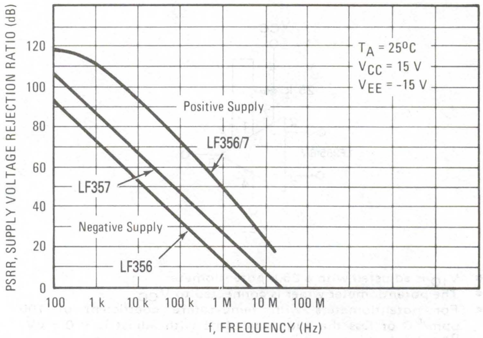


FIGURE 28 — (LF356 AND LF357 SERIES)



EQUIVALENT NOISE VOLTAGE

FIGURE 29 — (LF355/356/357 SERIES)

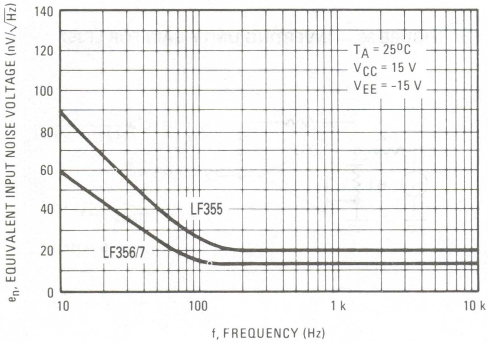
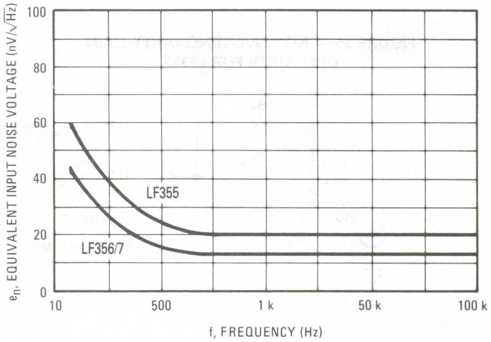
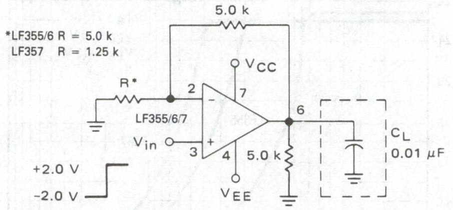


FIGURE 30 (EXPANDED SCALE)



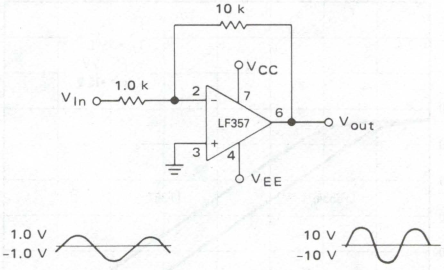
TYPICAL CIRCUIT CONNECTIONS

FIGURE 31 — DRIVING CAPACITIVE LOADS


*LF355/6 R = 5.0 k
LF357 R = 1.25 k
5.0 k
VCC
R*
2
7
6
LF355/6/7
Vin
3
4
5.0 k
CL
0.01 µF
+2.0 V
−2.0 V
VEE

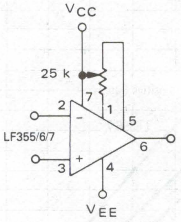
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot $\leqslant$ 20%
Settling time (t_s) $\cong$ 5.0 µs

FIGURE 32 — LARGE POWER BANDWIDTH AMPLIFIER


10 k
VCC
1.0 k
Vin
2
7
6
LF357
Vout
3
4
VEE
1.0 V
−1.0 V
10 V
−10 V

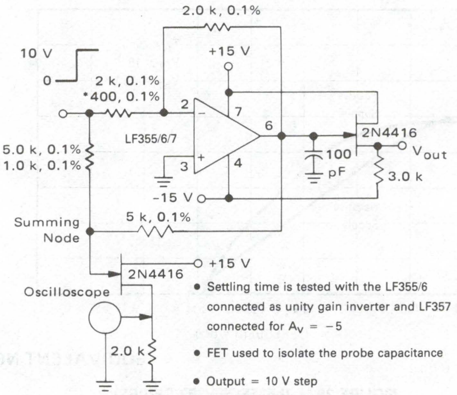
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

FIGURE 33 — INPUT OFFSET VOLTAGE ADJUSTMENT


VCC
25 k
7
1
5
2
LF355/6/7
6
3
4
VEE

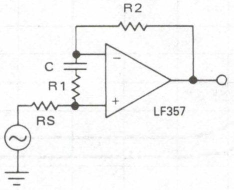
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment.
- Typical overall drift: 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

FIGURE 34 — SETTLING TIME TEST CIRCUIT


2.0 k, 0.1%
10 V
0
+15 V
2 k, 0.1%
*400, 0.1%
2
7
6
LF355/6/7
2N4416
5.0 k, 0.1%
*1.0 k, 0.1%
3
4
100 pF
Vout
3.0 k
−15 V
Summing Node
5 k, 0.1%
+15 V
2N4416
Oscilloscope
2.0 k

- Settling time is tested with the LF355/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step
- *$A_V = -5$ for LF357

FIGURE 35 — NONINVERTING UNITY GAIN OPERATION FOR LF357


R2
C
R1
RS
LF357

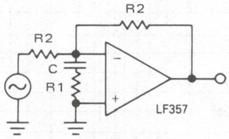
$R1C \geqslant \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\ MHz$

FIGURE 36 — INVERTING UNITY GAIN FOR LF357


R2
R2
C
R1
LF357

$R1C \geqslant \frac{1}{(2\pi)(5\ MHz)}$

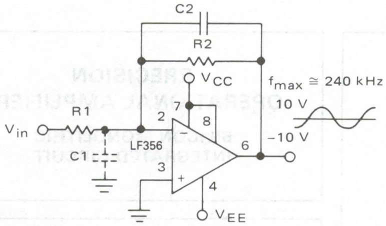
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\ MHz$

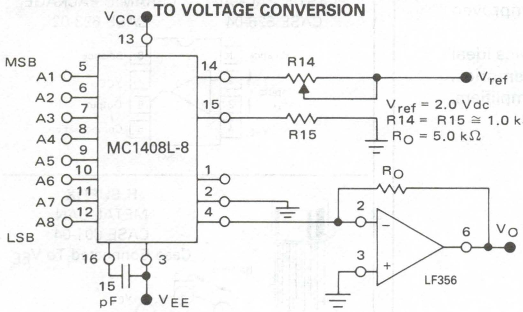
TYPICAL APPLICATIONS

FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER


C2
R2
VCC
fmax ≅ 240 kHz
10 V
−10 V
R1
Vin
2
7
8
LF356
6
C1
3
4
VEE

- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance (C1 ≅ 3 pF for LF355, LF356, and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION


VCC
13
MSB
A1
A2
A3
A4
A5
A6
A7
A8
LSB
5
6
7
8
9
10
11
12
MC1408L-8
14
15
R14
Vref
R15
Vref = 2.0 Vdc
R14 = R15 ≅ 1.0 kΩ
RO = 5.0 kΩ
1
2
4
RO
2
3
6
VO
LF356
16
3
15 pF
VEE

Theoretical V_O

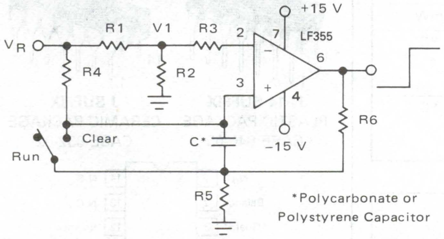
$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

FIGURE 41 — LONG INTERVAL RC TIMER


+15 V
VR
R1
V1
R3
2
7
LF355
6
R4
R2
3
4
Clear
C*
−15 V
R6
Run
R5

*Polycarbonate or Polystyrene Capacitor

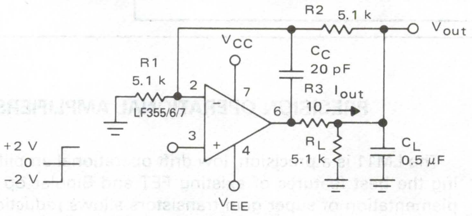
Time (t) = $R4C\ell n(V_R/V_R - V_I)$, $R_3 = R_4$, $R_5 = 0.1\ R6$

If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 V	C = 1 μF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2 k	R1 = R2 = 1 k

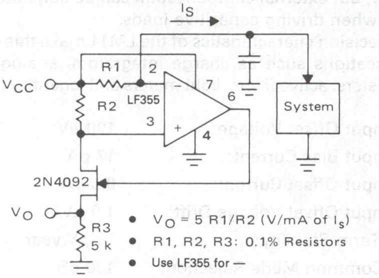
FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS


R2
5.1 k
Vout
VCC
CC
20 pF
R1
5.1 k
2
7
R3
10
Iout
LF355/6/7
6
3
4
RL
5.1 k
CL
0.5 μF
+2 V
0
−2 V
VEE

- Overshoot 6%
- t_s = 10 μs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

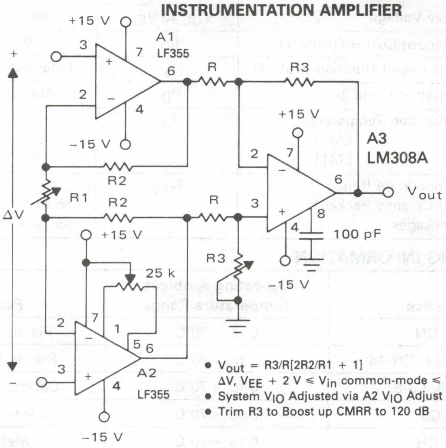
$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 40 — PRECISION CURRENT MONITOR


IS
R1
2
VCC
7
R2
LF355
6
System
3
4
2N4092
VO
R3
5 k

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% Resistors
- Use LF355 for
  - Common-Mode Range to Supply Range
  - Low I_{IB}
  - Low V_{IO}
  - Low Supply Current

FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER


+15 V
+
A1
3
7
LF355
6
R
R3
2
4
−15 V
+15 V
A3
LM308A
ΔV
R2
R1
R2
2
7
6
Vout
R
3
8
4
100 pF
+15 V
R3
−15 V
25 k
2
7
1
5
6
A2
3
4
LF355
−15 V
−

- V_{out} = R3/R[2R2/R1 + 1]
- ΔV, V_{EE} + 2 V ≤ V_{in} common-mode ≤ V_{CC}
- System V_{IO} Adjusted via A2 V_{IO} Adjust
- Trim R3 to Boost up CMRR to 120 dB

LM11
LM11C
LM11CL

MOTOROLA

PRECISION OPERATIONAL AMPLIFIERS

The LM11 is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM108A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm-up stabilization time in critical applications.

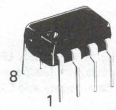
Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

The precision characteristics of the LM11 make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

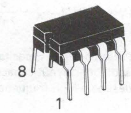
● Low Input Offset Voltage:	100 μV
● Low Input Bias Current:	17 pA
● Low Input Offset Current:	0.5 pA
● Low Input Offset Voltage Drift:	1.0 μV/°C
● Long-Term Stability:	10 μV/year
● High Common Mode Rejection:	130 dB

PRECISION OPERATIONAL AMPLIFIERS

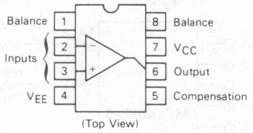
SILICON MONOLITHIC INTEGRATED CIRCUIT



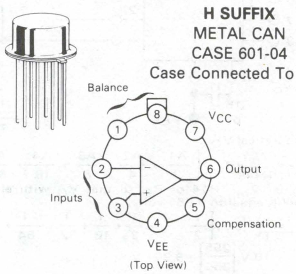
N SUFFIX
PLASTIC PACKAGE
CASE 626-04

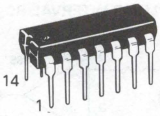


J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02

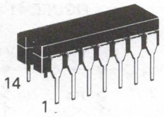


H SUFFIX
METAL CAN
CASE 601-04
Case Connected To V_{EE}

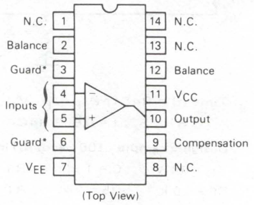




N-14 SUFFIX
PLASTIC PACKAGE
CASE 646-05



J SUFFIX
CERAMIC PACKAGE
CASE 632-02



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short-Circuit Duration (Note 2)	t_s	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature LM11 LM11C/CL	T_J	 150 85	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 −55 to +125	°C

ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
LM11CLN, CN	0 to +70°C	Plastic 8-Pin DIP
LM11CLN-14, CN-14	0 to +70°C	Plastic 14-Pin DIP
LM11CLJ-8, CJ-8	0 to +70°C	Ceramic 8-Pin DIP
LM11CLJ, CJ	0 to +70°C	Ceramic 14-Pin DIP
LM11CLH, CH	0 to +70°C	Metal Can
LM11J-8	−55 to +125°C	Ceramic 8-Pin DIP
LM11J	−55 to +125°C	Ceramic 14-Pin DIP
LM11H	−55 to +125°C	Metal Can

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted [Note 4])

		LM11			LM11C			LM11CL			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{IO}	—	0.1	0.3	—	0.2	0.6	—	0.5	5.0	mV
T_{low} to T_{high}		—	—	0.6	—	—	0.8	—	—	6.0	
Input Offset Current	I_{IO}	—	0.5	10	—	1.0	10	—	4.0	25	pA
T_{low} to T_{high}		—	—	30	—	—	20	—	—	50	
Input Bias Current	I_{IB}	—	17	50	—	17	100	—	17	200	pA
T_{low} to T_{high}		—	—	150	—	—	150	—	—	300	
Input Resistance	r_i	—	10^{11}	—	—	10^{11}	—	—	10^{11}	—	Ω
Input Offset Voltage Drift T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	1.0	3.0	—	2.0	5.0	—	3.0	—	µV/°C
Input Offset Current Drift T_{low} to T_{high}	$\Delta I_{IO}/\Delta T$	—	20	—	—	10	—	—	50	—	fA/°C
Input Bias Current Drift T_{low} to T_{high}	$\Delta I_{IB}/\Delta T$	—	0.5	1.5	—	0.8	3.0	—	1.4	—	pA/°C
Large Signal Voltage Gain	A_{VOL}										V/mV
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±2.0 mA		100	300	—	100	300	—	25	300	—	
T_{low} to T_{high} (Note 5)		50	—	—	50	—	—	15	—	—	
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±0.5 mA		250	1200	—	250	1200	—	50	800	—	
T_{low} to T_{high}		100	—	—	100	—	—	30	—	m	
Common Mode Rejection Ratio	CMRR										dB
V_S = ±15 V, $-13\ V \leq V_{CM} \leq 14\ V$		110	130	—	110	130	—	96	110	—	
V_S = ±15 V, $-12.5\ V \leq V_{CM} \leq 14\ V$, T_{low} to T_{high}		100	—	—	100	—	—	90	—	—	
Power Supply Rejection Ratio	PSRR										dB
$\pm 2.5\ V \leq V_S \leq \pm 20\ V$		100	118	—	100	118	—	84	100	—	
T_{low} to t_{high}		96	—	—	96	—	—	80	—	—	
Power Supply Current	I_D	—	0.3	0.6	—	0.3	0.8	—	0.3	0.8	mA
T_{low} to T_{high}		—	—	0.8	—	—	1.0	—	—	1.0	
Output Short-Circuit Current T_J = 150°C, Output Shorted to Ground	I_{os}	—	±10	—	—	±10	—	—	±10	—	mA

Notes:

1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2 kΩ resistance in each input is suggested to prevent possible latch-up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heat sinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for $V_{EE} + 2.0\ V \leq V_{CM} \leq V_{CC} - 1.0\ V$ ($V_{EE} + 2.5\ V \leq V_{CM} \leq V_{CC} - 1.0\ V$ for T_{low} to T_{high}) and $\pm 2.5\ V \leq V_S \leq \pm 20\ V$
   T_{low} to T_{high}: $-55°C \leq T_J \leq +125°C$ for LM11
   $0°C \leq T_J \leq +70°C$ for LM11C and LM11CL
5. V_{out} = ±11.5 V, all other conditions unchanged.

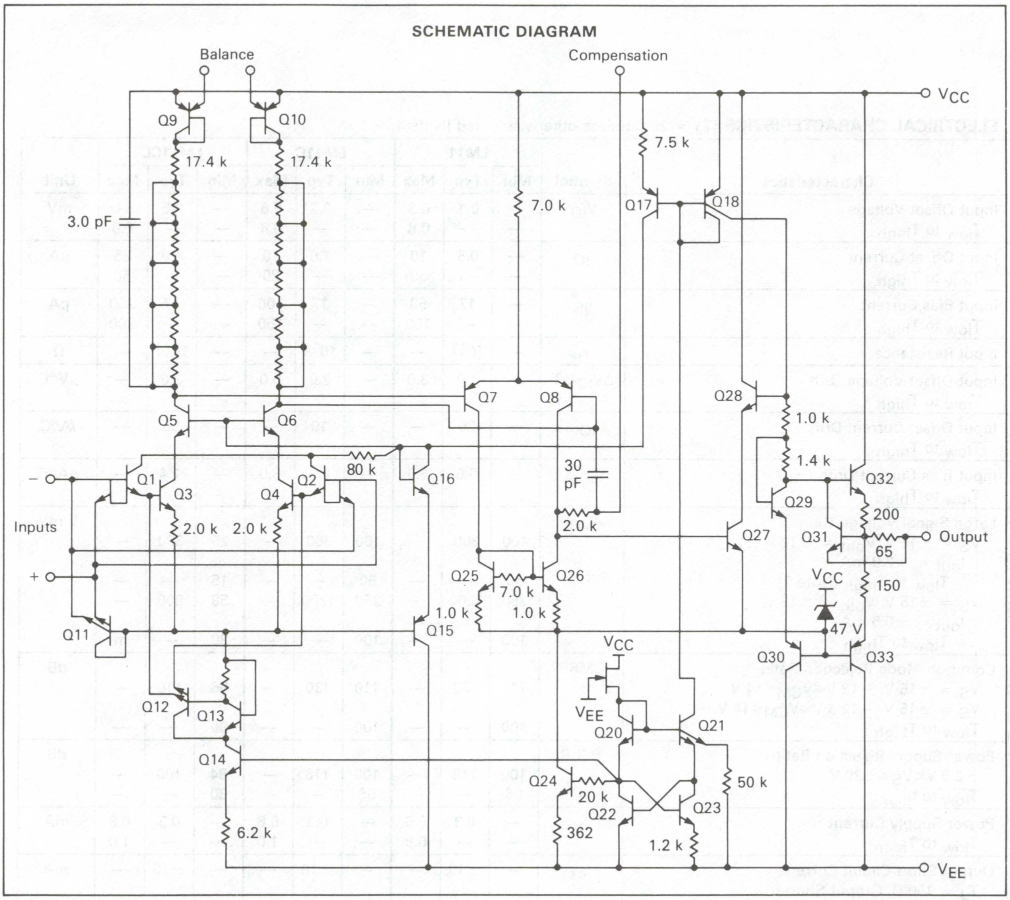

SCHEMATIC DIAGRAM
Balance
Compensation
VCC
Q9
Q10
17.4 k
17.4 k
3.0 pF
7.5 k
7.0 k
Q17
Q18
Q7
Q8
Q28
Q5
Q6
1.0 k
1.4 k
80 k
30 pF
−
Q1
Q2
Q16
Q3
Q4
Q32
Q29
Inputs
2.0 k
2.0 k
2.0 k
200
Q27
Q31
Output
65
+
Q25
Q26
VCC
150
7.0 k
1.0 k
1.0 k
Q11
Q15
47 V
VCC
Q30
Q33
Q12
Q13
VEE
Q20
Q21
Q14
Q24
50 k
20 k
Q22
Q23
362
6.2 k
1.2 k
VEE

FIGURE 1 — INPUT BIAS CURRENT versus CASE TEMPERATURE

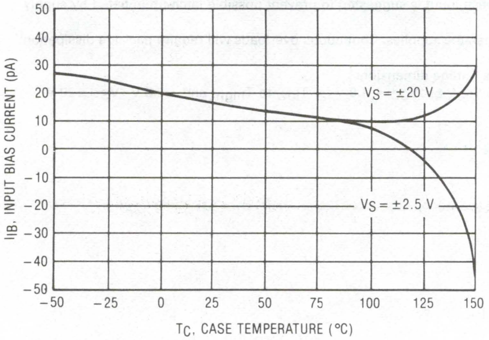


FIGURE 2 — INPUT OFFSET CURRENT versus CASE TEMPERATURE

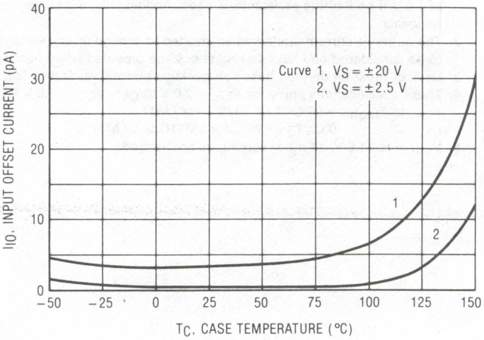


FIGURE 3 — TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE versus INPUT OFFSET VOLTAGE

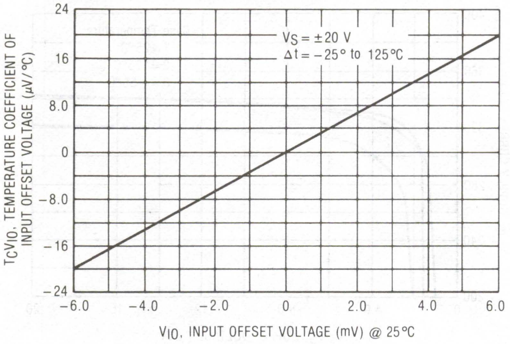


FIGURE 4 — SPECTRAL NOISE DENSITY

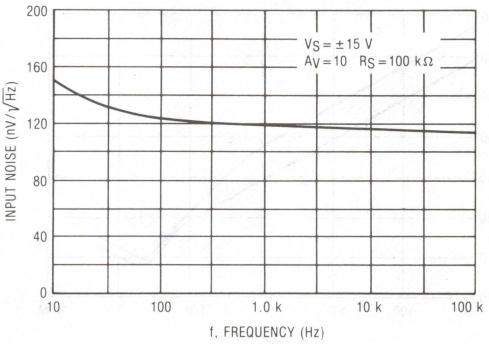


FIGURE 5 — COMMON-MODE LIMITS versus TEMPERATURE

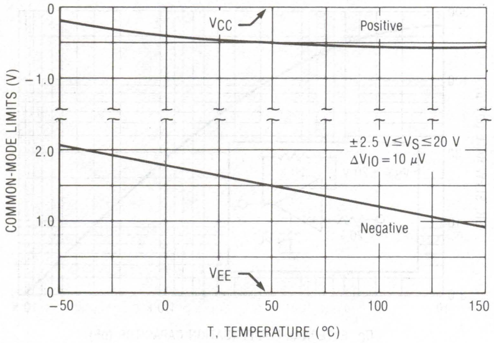


FIGURE 6 — COMMON-MODE REJECTION AND SLEW LIMIT versus FREQUENCY

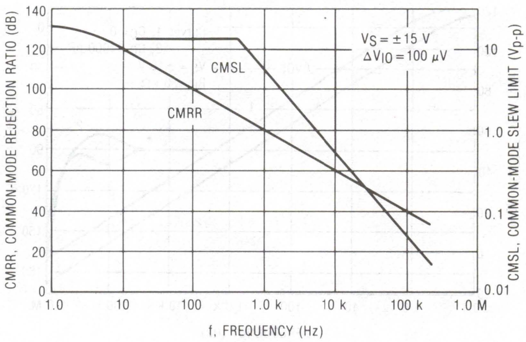


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

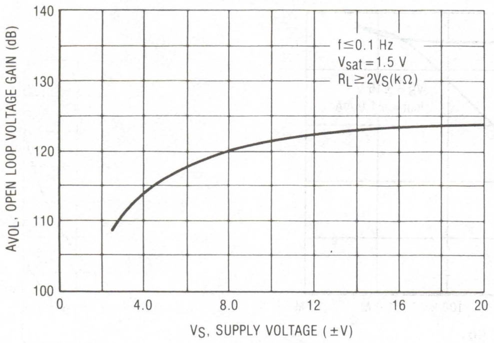


FIGURE 8 — OUTPUT SATURATION versus LOAD CURRENT

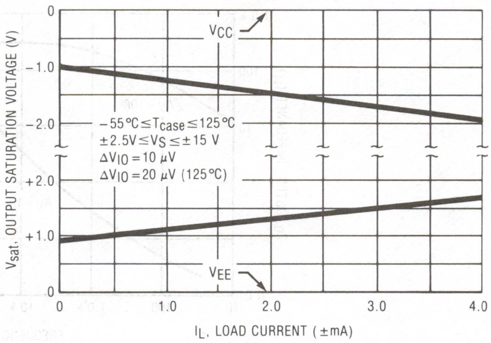


FIGURE 9 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

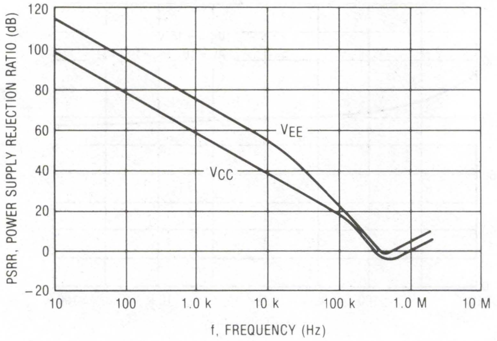


FIGURE 10 — SUPPLY CURRENT versus SUPPLY VOLTAGE

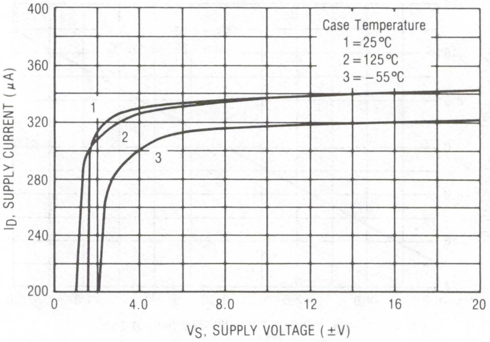


FIGURE 11 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

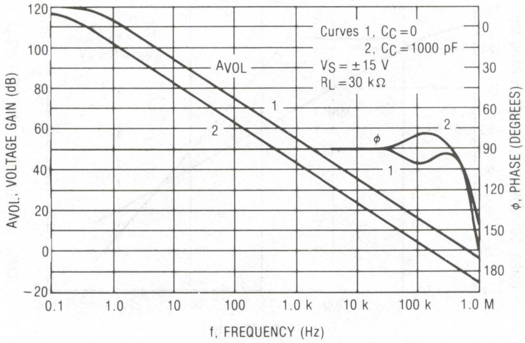


FIGURE 12 — SLEW RATE versus EXTERNAL COMPENSATION CAPACITOR

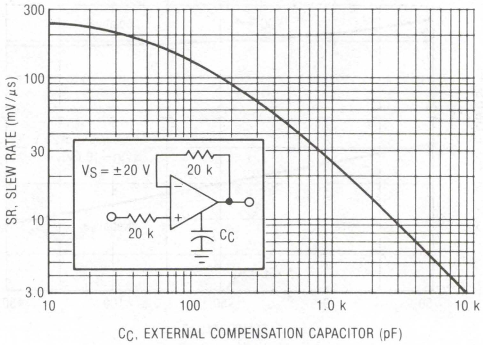
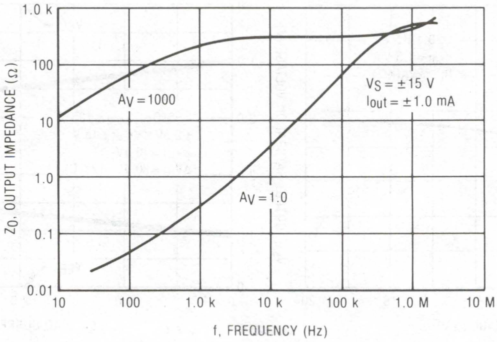


FIGURE 13 — CLOSED LOOP OUTPUT IMPEDANCE versus FREQUENCY



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3 volts are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 µF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited to only the LM11.

The LM11 is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of p.c. board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

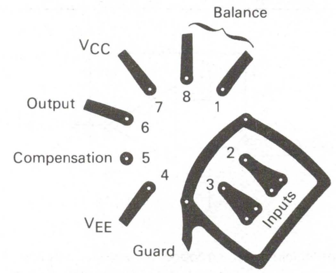
The suggested printed circuit board layout for input guarding is shown in Figure 14. Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 15. For critical applications, a 14-pin dual in-line package is available with guard pins (internally unconnected) adjacent to the inputs for minimal package leakage effects.

Electrostatic shielding is suggested in high-impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11 is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

FIGURE 14 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT FOR INPUT GUARDING USING METAL PACKAGED DEVICE



(Bottom View)

The above guard ring, required on both sides of the board, is connected to a low impedance point of the same potential as the sensitive inputs to reduce surface leakage paths. Bulk leakage is reduced less, and depends more on guard ring width.

FIGURE 15 — GUARD RING ELECTRICAL CONNECTIONS FOR COMMON AMPLIFIER CONFIGURATIONS

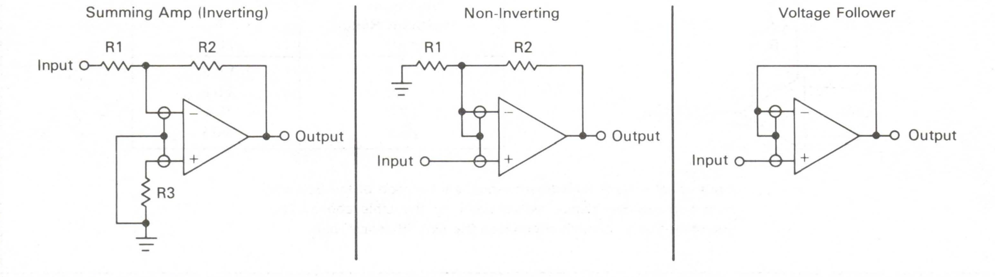
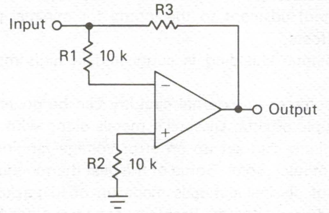
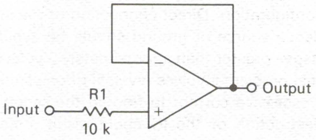


FIGURE 16 — INPUT PROTECTION FOR SUMMING (INVERTING) AMPLIFIER



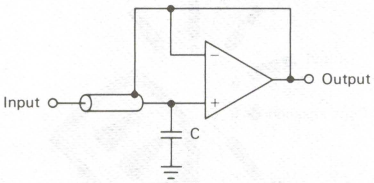
Current is limited by R1 in the event the input is connected to a low impedance source outside the common-mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

FIGURE 17 — INPUT PROTECTION FOR A VOLTAGE FOLLOWER

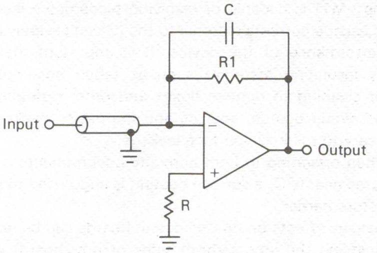


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

FIGURE 18 — CABLE BOOT STRAPPING AND INPUT SHIELDS

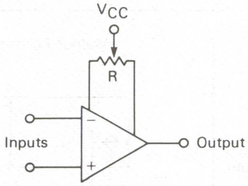


An input shield boot strapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

FIGURE 19 — ADJUSTING INPUT OFFSET VOLTAGE WITH BALANCE POTENTIOMETER



Minimum Adjustment Range (mV)	R Ω
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.

MOTOROLA

LM101A
LM201A
LM301A

OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

- Low Input Offset Current — 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – STANDARD COMPENSATION AND OFFSET BALANCING CIRCUIT

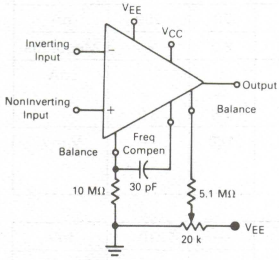
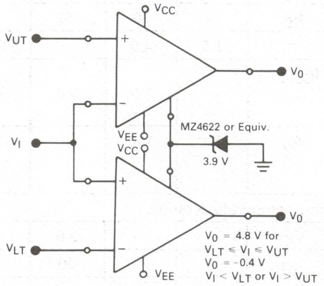
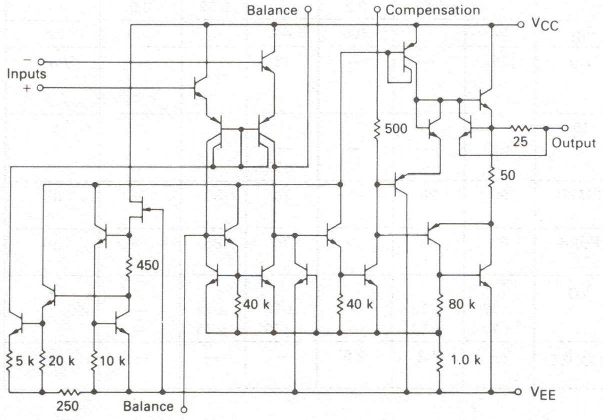

VEE
VCC
Inverting Input
Noninverting Input
Output
Balance
Freq Compen
Balance
10 MΩ
30 pF
5.1 MΩ
20 k
VEE

FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR


VCC
VUT
VO
VI
VEE
VCC
MZ4622 or Equiv.
3.9 V
VO
VLT
VEE
VO = 4.8 V for
VLT ≤ VI ≤ VUT
VO = −0.4 V
VI < VLT or VI > VUT

Pins Not Shown Are Not Connected

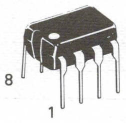
FIGURE 3 – REPRESENTATIVE CIRCUIT SCHEMATIC

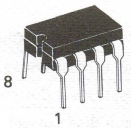

Balance
Compensation
VCC
Inputs
−
+
500
25
Output
50
450
40 k
40 k
80 k
5 k
20 k
10 k
1.0 k
250
Balance
VEE

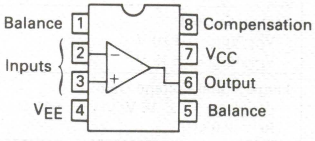
N SUFFIX
PLASTIC PACKAGE
CASE 626-04

J SUFFIX
CERAMIC PACKAGE
CASE 693-02

(LM201A and LM301A)

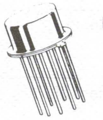


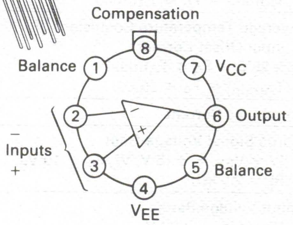



Balance 1
Inputs 2
3
VEE 4
8 Compensation
7 VCC
6 Output
5 Balance
−
+

(Top View)

H SUFFIX
METAL PACKAGE
CASE 601-04




Compensation
8
Balance 1
7 VCC
2
6 Output
Inputs
−
+
3
5 Balance
4
VEE

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM101AH	−55°C to +125°C	Metal Can
LM101AJ	−55°C to +125°C	Ceramic DIP
LM201AH	−25°C to +85°C	Metal Can
LM201AN	−25°C to +85°C	Plastic DIP
LM201AJ	−25°C to +85°C	Ceramic DIP
LM301AH	0°C to +70°C	Metal Can
LM301AN	0°C to +70°C	Plastic DIP
LM301AJ	0°C to +70°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	VALUE LM101A	LM201A	LM301A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	← ±30 →			Volts
Input Common-Mode Range (Note 1)	V_{ICR}	← ±15 →			Volts
Output Short-Circuit Duration	t_S	← Continuous →			
Power Dissipation (Package Limitation)	P_D				
Metal Can		← 500 →			mW
Derate above T_A = +75°C		← 6.8 →			mW/°C
Plastic Dual In-Line Package (LM201A/301A)		—	625	625	mW
Derate above T_A = + 25°C		—	5.0	5.0	mW/°C
Ceramic Package		← 750 →			mW
Derate above 25°C		← 6.6 →			mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	← −65 to +150 →			°C

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM101A and LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristics	Symbol	LM101A LM201A Min	Typ	Max	LM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 50$ kΩ)	V_{IO}	—	0.7	2.0	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	1.5	10	—	3.0	50	nA
Input Bias Current	I_{IB}	—	30	75	—	70	250	nA
Input Resistance	r_i	1.5	4.0	—	0.5	2.0	—	Megohms
Supply Current	I_{CC}, I_{EE}							mA
V_{CC}/V_{EE} = ±20 V		—	1.8	3.0	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	—	1.8	3.0	
Large Signal Voltage Gain (V_{CC}/V_{EE} = ± 15 V, V_O = ±10 V, $R_L > 2.0$ kΩ)	A_V	50	160	—	25	160	—	V/mV

The following specifications apply over the operating temperature range.

Characteristics	Symbol	LM101A LM201A Min	Typ	Max	LM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 50$ kΩ)	V_{IO}	—	—	3.0	—	—	10	mV
Input Offset Current	I_{IO}	—	—	20	—	—	70	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$	$\Delta V_{IO}/\Delta T$	—	3.0	15	—	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
+25°C ≤ T_A ≤ T_A(max)		—	0.01	0.1	—	0.01	0.3	
$T_{A(min)}$ ≤ T_A ≤ 25°C		—	0.02	0.2	—	0.02	0.6	
Input Bias Current	I_{IB}	—	—	100	—	—	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ± 10 V, $R_L > 2.0$ kΩ)	A_V	25	—	—	15	—	—	V/mV
Input Voltage Range	V_I							V
V_{CC}/V_{EE} = ±20 V		±15	—	—	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	±12	—	—	
Common-Mode Rejection Ratio $R_S \leq 50$ kΩ	CMRR	80	96	—	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \leq 50$ kΩ	PSRR	80	96	—	70	96	—	dB
Output Voltage Swing	V_O							V
V_{CC}/V_{EE} = ±15 V, R_L = 10 kΩ,		±12	±14	—	±12	±14	—	
R_L = 2.0 kΩ		±10	±13	—	±10	±13	—	
Supply Currents (T_A = T_A(max), V_{CC}/V_{EE} = ±20 V)	I_{CC}, I_{EE}	—	1.2	2.5	—	—	—	mA

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = + 25°C unless otherwise noted.)

FIGURE 4 — MINIMUM INPUT VOLTAGE RANGE

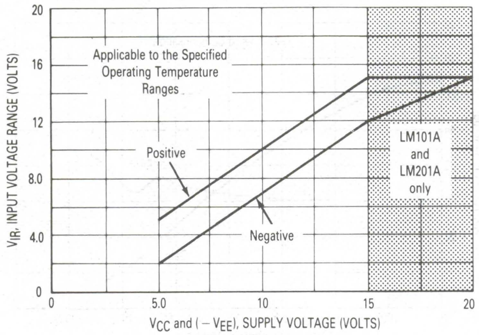


FIGURE 5 — MINIMUM OUTPUT VOLTAGE SWING

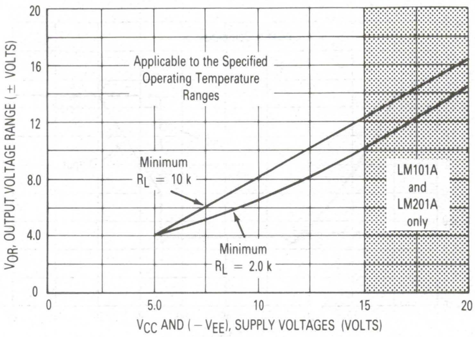


FIGURE 6 — MINIMUM VOLTAGE GAIN

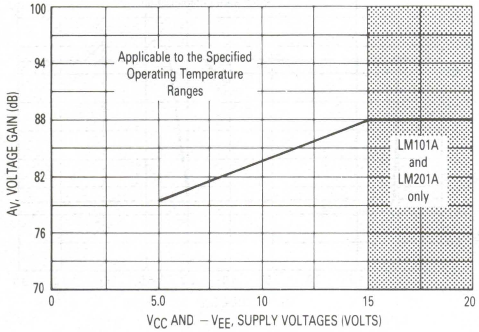


FIGURE 7 — TYPICAL SUPPLY CURRENTS

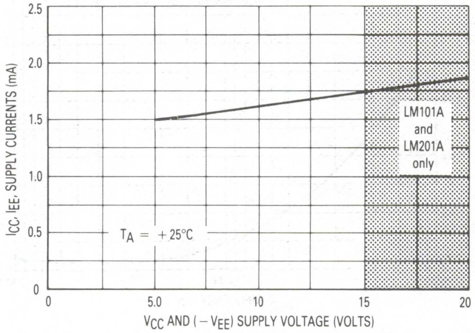


FIGURE 8 — OPEN-LOOP FREQUENCY RESPONSE

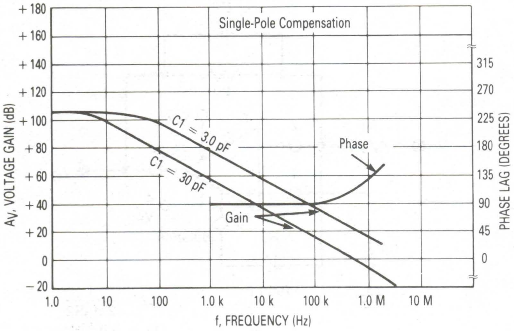
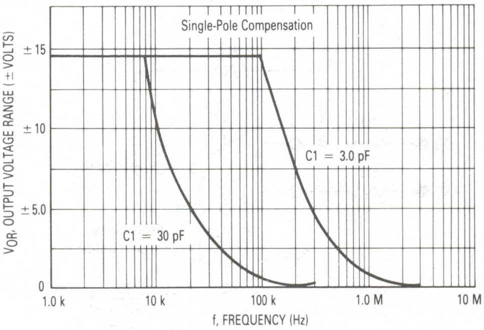


FIGURE 9 — LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 — VOLTAGE FOLLOWER PULSE RESPONSE

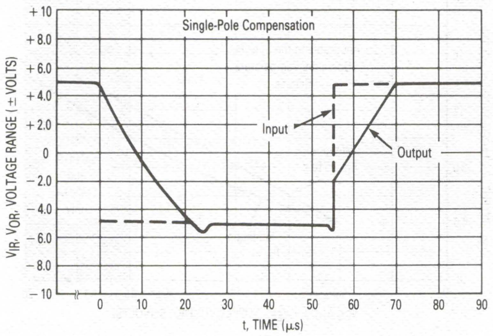


FIGURE 11 — OPEN-LOOP FREQUENCY RESPONSE

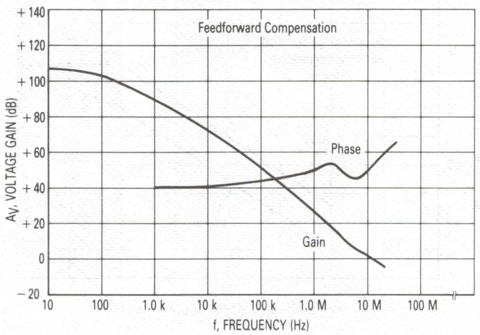


FIGURE 12 — LARGE-SIGNAL FREQUENCY RESPONSE

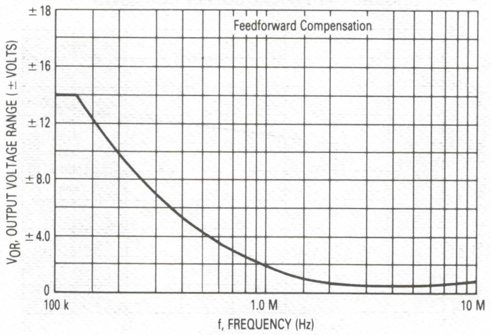
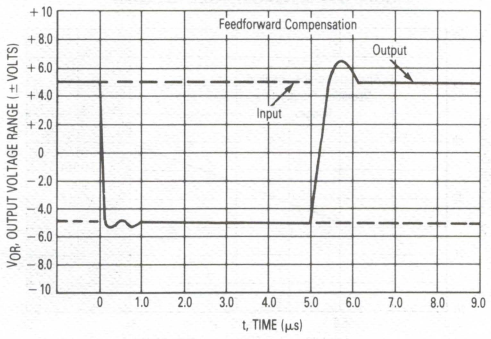


FIGURE 13 — INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

FIGURE 14 — SINGLE-POLE COMPENSATON

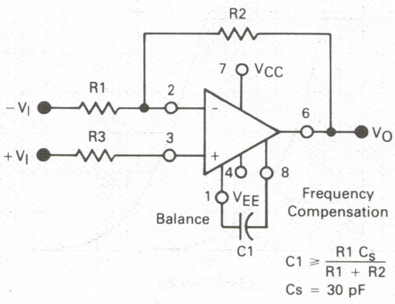
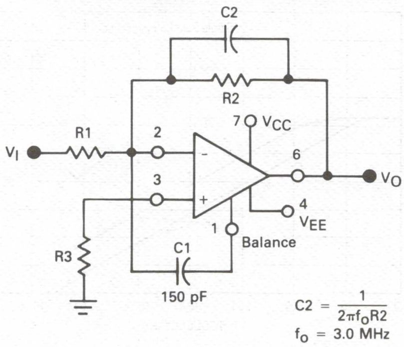

R2
7
VCC
R1
2
−VI
R3
3
+VI
6
VO
4
8
1
VEE
Balance
Frequency Compensation
C1
C1 ≥ R1 Cs / (R1 + R2)
Cs = 30 pF

FIGURE 15 — FEEDFORWARD COMPENSATION


C2
R2
7
VCC
R1
2
VI
3
6
VO
4
VEE
1
Balance
R3
C1
150 pF
C2 = 1 / (2πfoR2)
fo = 3.0 MHz

MOTOROLA

LM108, LM108A
LM208, LM208A
LM308, LM308A

SUPER GAIN OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

PRECISION OPERATIONAL AMPLIFIERS

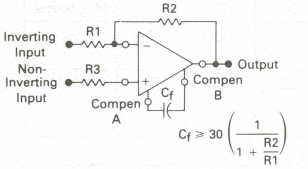
The LM108/LM208/LM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM108A/LM208A/LM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

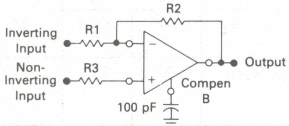
- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

FREQUENCY COMPENSATION

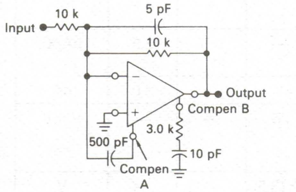
Standard Compensation


R2
R1
Inverting Input
Non-Inverting Input
R3
Output
Compen B
C_f
Compen A
$C_f \geq 30 \left(\frac{1}{1 + \frac{R2}{R1}}\right)$

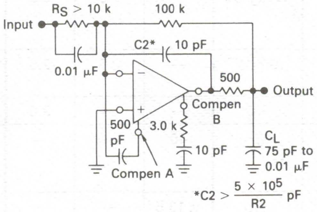
Modified Compensation


R2
Inverting Input
R1
Non-Inverting Input
R3
Output
Compen B
100 pF

Standard Feedforward Compensation


10 k
5 pF
Input
10 k
Output
Compen B
3.0 k
500 pF
10 pF
Compen A

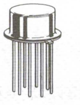
Feedforward Compensations for Decoupling Load Capacitance

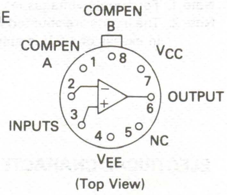

$R_S > 10$ k
100 k
Input
C2*
10 pF
0.01 μF
500
Output
Compen B
500 pF
3.0 k
10 pF
C_L 75 pF to 0.01 μF
Compen A
$^*C2 > \frac{5 \times 10^5}{R2}$ pF

DEVICE SELECTION TABLE

	OPERATING TEMPERATURE RANGE		
	−55 to +125°C	−25 to +85°C	0 to +70°C
STANDARD OFFSET VOLTAGE SPECIFICATION	LM108 Pkg. Suffix	LM208 Pkg. Suffix	LM308 Pkg. Suffix
TIGHTENED OFFSET VOLTAGE SPECIFICATION	LM108A Pkg. Suffix	LM208A Pkg. Suffix	LM308A Pkg. Suffix

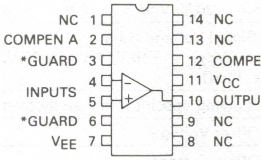
H SUFFIX
METAL PACKAGE
CASE 601-04




COMPEN B
COMPEN A
VCC
OUTPUT
INPUTS
NC
VEE
1
2
3
4
5
6
7
8

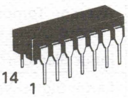
(Top View)

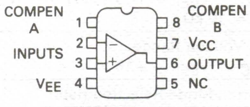
J SUFFIX
CERAMIC PACKAGE
CASE 632-02


NC 1
COMPEN A 2
*GUARD 3
INPUTS 4
5
*GUARD 6
VEE 7
14 NC
13 NC
12 COMPEN B
11 VCC
10 OUTPUT
9 NC
8 NC

(Top View)

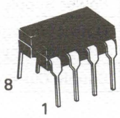
N SUFFIX
PLASTIC PACKAGE
CASE 626-04
(LM308 and LM308A Only)




COMPEN A 1
INPUTS 2
3
VEE 4
COMPEN B 8
7 VCC
6 OUTPUT
5 NC

(Top View)

J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
		LM108, LM108A	LM208, LM208A	LM308, LM308A	
Power Supply Voltage	V_{CC}, V_{EE}	±20	±20	±18	Vdc
Input Voltage (See Note 1)	V_I	±15			Volts
Input Differential Current (See Note 2)	I_{ID}	±10			mA
Output Short-Circuit Duration	t_S	Indefinite			
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150			°C
Junction Temperature	T_J				°C
Metal, Ceramic Package		+175			
Plastic Package		+150			

Note 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of $+5.0\ V \leq V_{CC} \leq +20\ V$ and $-5.0\ V \geq V_{EE} \geq -20\ V$, $T_A = +25°C$.)

Characteristic	Symbol	LM108A LM208A			LM108 LM208			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{IO}	—	0.05	0.2	—	0.005	0.2	nA
Input Bias Current	I_{IB}	—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	r_i	30	70	—	30	70	—	Megohms
Power Supply Currents $V_{CC} = +20\ V$, $V_{EE} = -20\ V$	I_{CC}, I_{EE}	—	±0.3	±0.6	—	±0.3	±0.6	mA
Large Signal Voltage Gain $V_{CC} = \lvert V_{EE} \rvert = +15\ V$, $V_O = \pm 10\ V$, $R_L \geq 10\ k\Omega$	A_{VOL}	80	300	—	50	300	—	V/mV

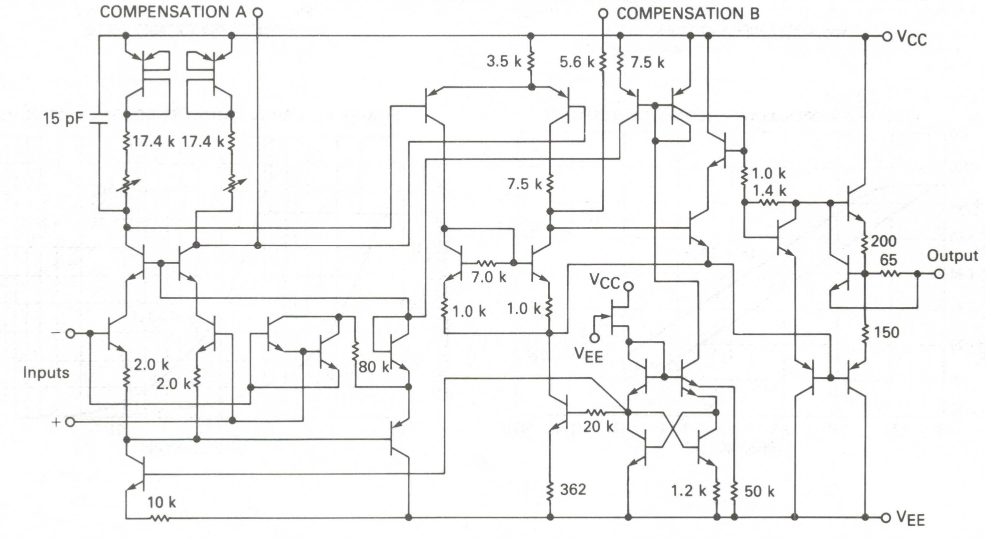
The following specifications apply over the operating temperature range.

Input Offset Voltage	V_{IO}	—	—	1.0	—	—	3.0	mV
Input Offset Current	I_{IO}	—	—	0.4	—	—	0.4	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	3.0	15	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	0.5	2.5	—	0.5	2.5	pA/°C
Input Bias Current	I_{IB}	—	—	3.0	—	—	3.0	nA
Large Signal Voltage Gain $V_{CC} = \lvert V_{EE} \rvert = +15\ V$, $V_O = \pm 10\ V$, $R_L = 10\ k\Omega$	A_{VOL}	40	—	—	25	—	—	V/mV
Input Voltage Range $V_{CC} = \lvert V_{EE} \rvert = +15\ V$	V_{IR}	±13.5	—	—	±13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	96	110	—	85	100	—	dB
Power Supply Voltage Rejection Ratio	PSRR	96	100	—	80	96	—	dB
Output Voltage Range $V_{CC} = \lvert V_{EE} \rvert = +15\ V$, $R_L = 10\ k\Omega$	V_{OR}	±13	±14	—	±13	±14	—	V
Supply Current ($T_A = T_A[max]$)	I_{CC}, I_{EE}	—	±0.15	±0.4	—	±0.15	±0.4	mA

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +15 V and −5.0V ≥ V_{EE} ≥ −15 V, T_A = +25°C.)

Characteristic	Symbol	LM308A			LM308			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_{IB}	—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	r_i	10	40	—	10	40	—	Megohms
Power Supply Currents V_{CC} = +15 V, V_{EE} = −15 V	I_{CC}, I_{EE}	—	±0.3	±0.8	—	±0.3	±0.8	mA
Large Signal Voltage Gain V_{CC} = +15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	80	300	—	25	300	—	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	—	—	0.73	—	—	10	mV
Input Offset Current	I_{IO}	—	—	1.5	—	—	1.5	nA
Average Temperature Coefficient of Input Offset Voltage $T_A(min)$ ≤ T_A ≤ $T_A(max)$	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	—	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	2.0	10	—	2.0	10	pA/°C
Input Bias Current	I_{IB}	—	—	10	—	—	10	nA
Large Signal Voltage Gain V_{CC}+15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	60	—	—	15	—	—	V/mV
Input Voltage Range V_{CC} = +15 V, V_{EE} = −15V	V_{IR}	±13.5	—	—	±13.5	—	—	V
Common-Mode Rejection Ratio R_S ≤ 50 kΩ	CMRR	96	110	—	80	100	—	dB
Supply Voltage Rejection Ratio R_S ≤ 50 kΩ	PSRR	96	110	—	80	96	—	dB
Output Voltage Range V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ	V_{OR}	±13	±14	—	±13	±14	—	V

REPRESENTATIVE CIRCUIT SCHEMATIC


COMPENSATION A
COMPENSATION B
VCC
15 pF
17.4 k
17.4 k
3.5 k
5.6 k
7.5 k
7.5 k
1.0 k
1.4 k
7.0 k
1.0 k
1.0 k
200
65
Output
VCC
VEE
150
−
Inputs
+
2.0 k
2.0 k
80 k
20 k
362
1.2 k
50 k
10 k
VEE

TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT BIAS AND INPUT OFFSET CURRENTS

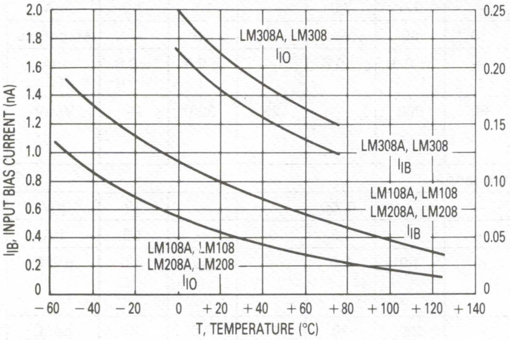


FIGURE 2 – MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

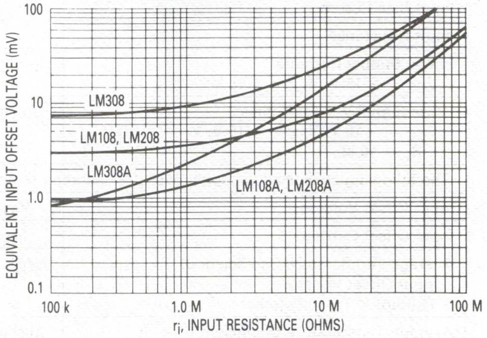


FIGURE 3 – VOLTAGE GAIN versus SUPPLY VOLTAGES

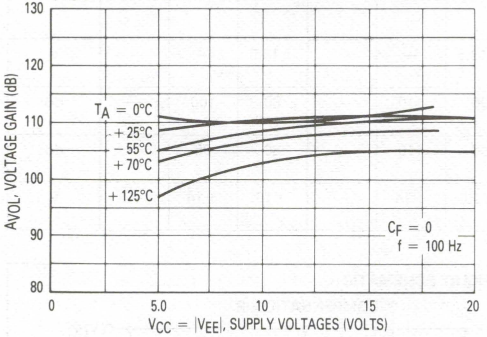


FIGURE 4 – POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

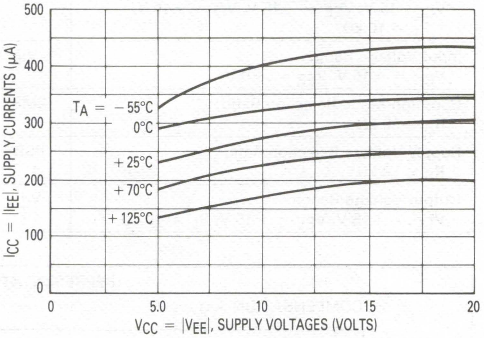


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

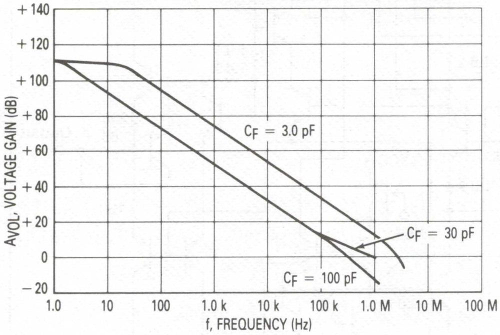
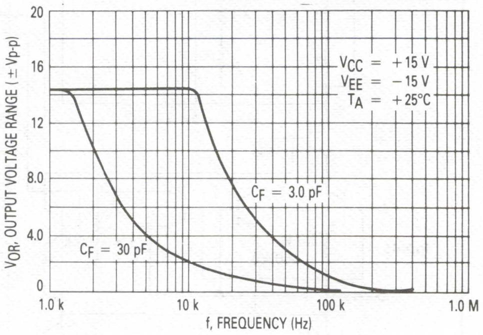
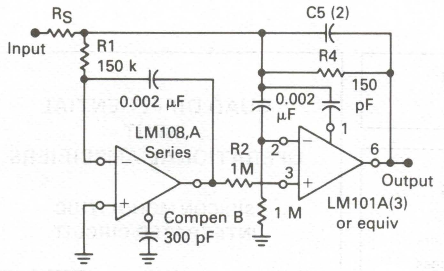


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



SUGGESTED DESIGN APPLICATIONS

FIGURE 7 — FAST (1) SUMMING AMPLIFIER WITH LOW INPUT CURRENT

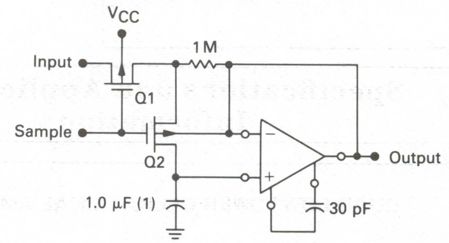

RS
Input
R1
150 k
0.002 µF
LM108,A
Series
Compen B
300 pF
C5 (2)
R4
150
pF
0.002
µF
R2
1M
2
3
1 M
1
6
Output
LM101A(3)
or equiv

(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

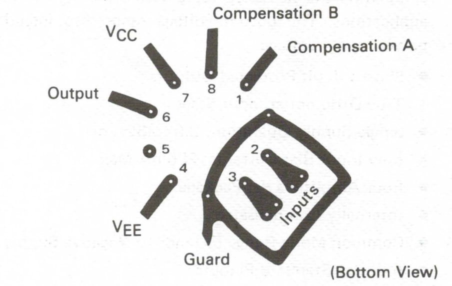
(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

FIGURE 8 — SAMPLE AND HOLD


VCC
Input
1 M
Q1
Sample
Q2
Output
1.0 µF (1)
30 pF

(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

FIGURE 9 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE


Compensation B
VCC
Compensation A
Output
7
8
1
6
5
2
4
3
Inputs
VEE
Guard
(Bottom View)

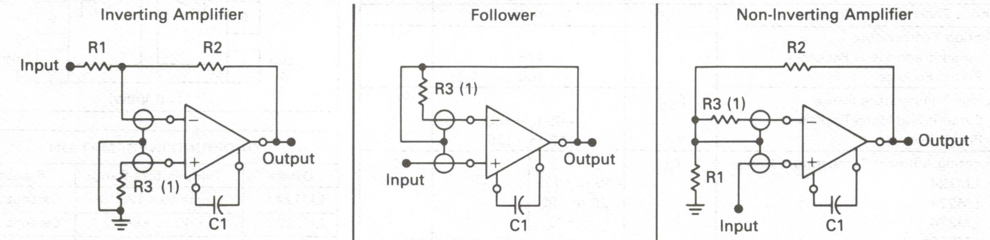
INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM108,A amplifier series. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and LM101A pin configuration).

FIGURE 10 — CONNECTION OF INPUT GUARDS


Inverting Amplifier
Input
R1
R2
Output
R3 (1)
C1
Follower
R3 (1)
Input
Output
C1
Non-Inverting Amplifier
R2
R3 (1)
Output
R1
Input
C1

(1) Used to compensate for large source resistances.

Note: $\frac{R1\ R2}{R1 + R2}$ must be an impedance.

LM124, LM224, LM324, LM2902

MOTOROLA

Specifications and Applications Information

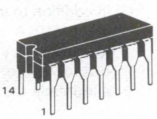
QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

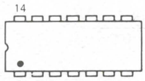
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The LM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

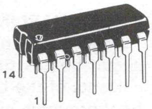
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents: 250 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts



J SUFFIX
CERAMIC PACKAGE
CASE 632-02

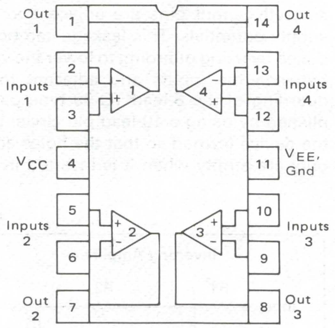


(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646-05
(LM224, LM324, LM2902 only)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM124 LM224 LM324	LM2902	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	±16	±13	
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) ($V_I < -0.3$ V)	I_{IF}	50	—	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			°C
Ceramic and Metal Packages		175		
Plastic Package		150		
Storage Temperature Range	T_{stg}			°C
Ceramic and Metal Packages		-65 to +150		
Plastic Package		-55 to +125		
Operating Ambient Temperature Range	T_A			°C
LM124		-55 to +125	—	
LM224		-25 to +85	—	
LM324		0 to +70	—	
LM2902		—	-40 to +85	

(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V for the **LM124/224/324** and 26 V for the **LM2902**, the absolute maximum input voltage is equal to the supply voltage.
(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than −0.3 V.

ORDERING INFORMATION

Device	Temperature Range	Package
LM124J	-55 to +125°C	Ceramic DIP
LM2902J	-40 to +85°C	Ceramic DIP
LM2902N	-40 to +85°C	Plastic DIP
LM224J	-25 to +85°C	Ceramic DIP
LM224N	-25 to +85°C	Plastic DIP
LM324J	0 to +70°C	Ceramic DIP
LM324N	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

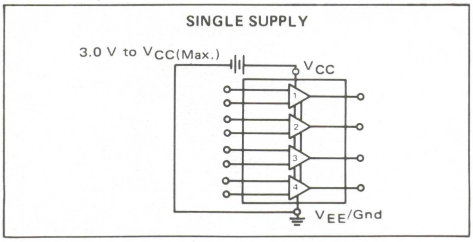
Characteristic	Symbol	LM124/LM224			LM324			LM2902			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902), V_{IC} = 0 V to V_{CC} – 1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω	V_{IO}										mV
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high} to T_{low} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	–	-45	-250	nA
T_A = T_{high} to T_{low} (Note 1)		–	-50	-300	–	-50	-500	–	-50	-500	
Input Common-Mode Voltage Range (Note 2)	V_{ICR}										V
V_{CC} = 30 V (26 V for LM2902)		0	–	28.3	0	–	28.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2902), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	–	25	100	–	–	100	–	
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	–	–	–	
Channel Separation 1.0 kHz ⩽ f ⩽ 20 kHz, Input Referenced	–	–	-120	–	–	-120	–	–	-120	–	dB
Common-Mode Rejection Ratio R_S ⩽ 10 kΩ	CMRR	70	85	–	65	70	–	50	70	–	dB
Power Supply Rejection Ratio	PSRR	65	100	–	65	100	–	50	100	–	dB
Output Voltage Range R_L = 2 kΩ (R_L ⩾ 10 kΩ for LM2902),	V_{OR}	0	–	3.3	0	–	3.3	0	–	3.3	V
Output Voltage—High Limit (T_A = T_{high} to T_{low})(Note 1)	V_{OH}										V
V_{CC} = 30 V (26 V for LM2902), R_L = 2 kΩ		26	–	–	26	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2902), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	
Output Voltage—Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V)	I_{O+}										mA
T_A = 25°C		20	40	–	20	40	–	20	40	–	
T_A = T_{high} to T_{low} (Note 1)		10	20	–	10	20	–	10	20	–	
Output Sink Current V_{ID} = –1.0 V, V_{CC} = 15 V	I_{O-}										mA
T_A = 25°C		10	20	–	10	20	–	10	20	–	
T_A = T_{high} to T_{low} (Note 1)		5	8	–	5	8	–	5	8	–	
V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C		12	50	–	12	50	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{os}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(Note 1)	I_{CC}										mA
V_{CC} = 30 V (26 V for LM2902), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

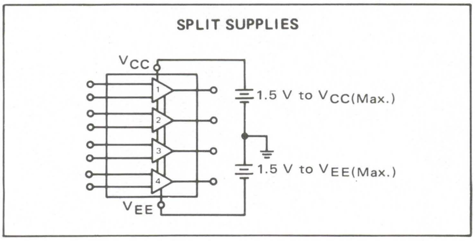
NOTES:

(1) T_{low} = –55°C for LM124; = –40°C for LM2902; = –25°C for LM224; = 0°C for LM324
T_{high} = +125°C for LM124; = +85°C for LM2902 and LM224; = +70°C for LM324

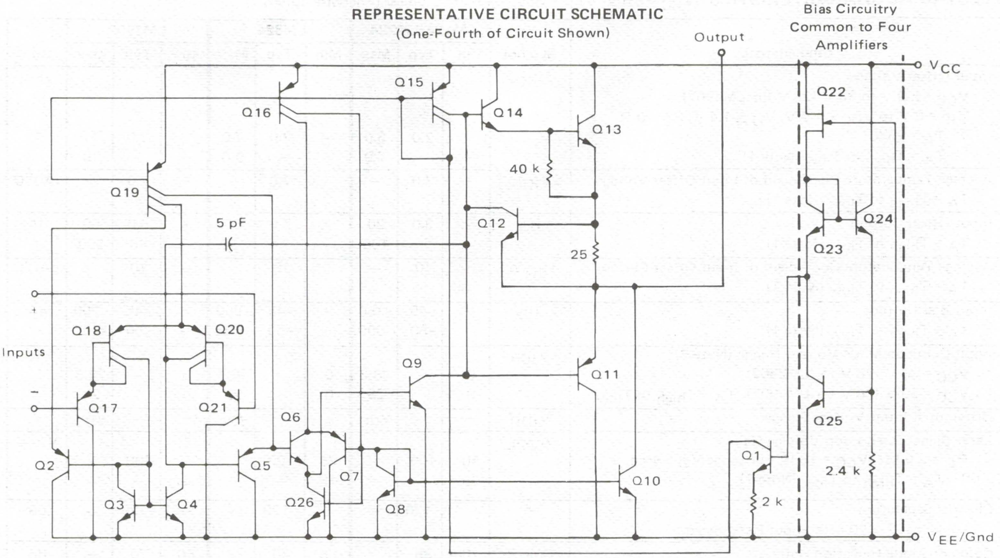
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} – 1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2902).

(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

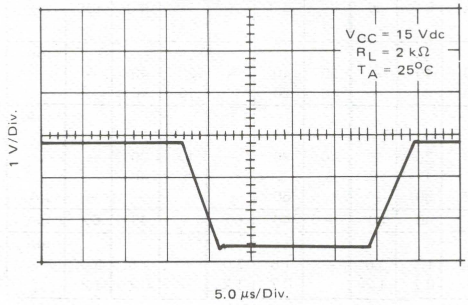

SINGLE SUPPLY


SPLIT SUPPLIES

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Fourth of Circuit Shown)


Output
Bias Circuitry
Common to Four
Amplifiers
VCC
Q15
Q16
Q14
Q13
Q22
40 k
Q19
5 pF
Q12
25
Q24
Q23
+
Q18
Q20
Inputs
−
Q9
Q11
Q17
Q21
Q6
Q25
Q2
Q5
Q7
Q1
Q10
2.4 k
Q3
Q4
Q26
Q8
2 k
VEE/Gnd

LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE



CIRCUIT DESCRIPTION

The LM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

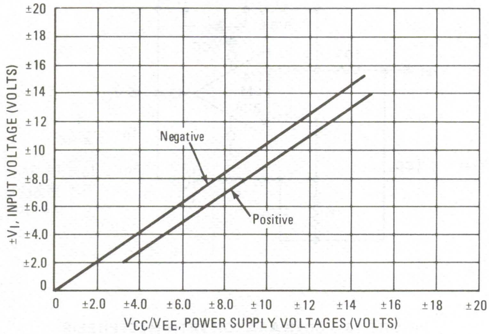


FIGURE 2 – OPEN LOOP FREQUENCY

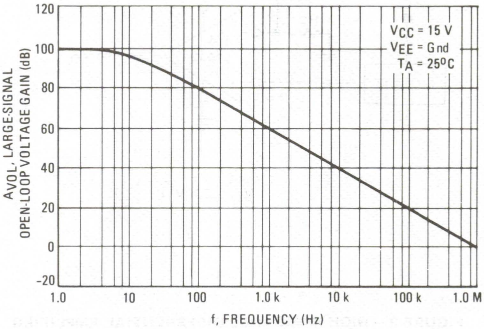


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

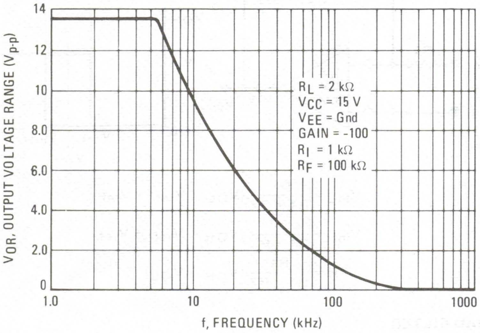


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

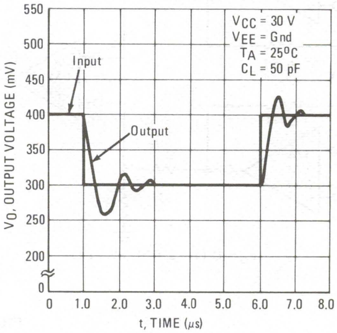


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

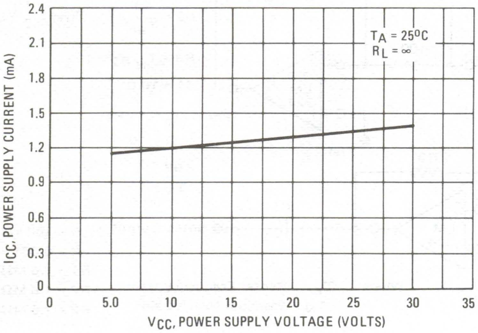
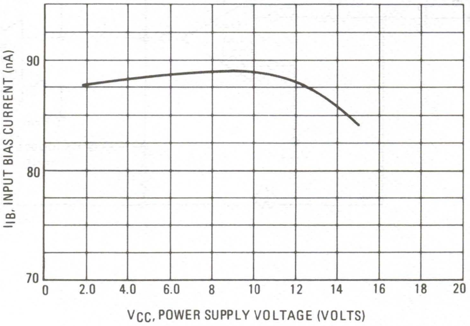


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

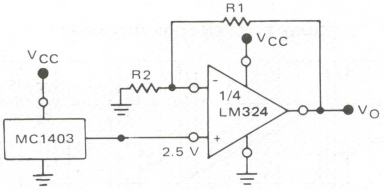

R1
VCC
VCC
R2
1/4
LM324
VO
MC1403
2.5 V

FIGURE 7 – VOLTAGE REFERENCE

$V_O = 2.5\ V(1 + \frac{R1}{R2})$

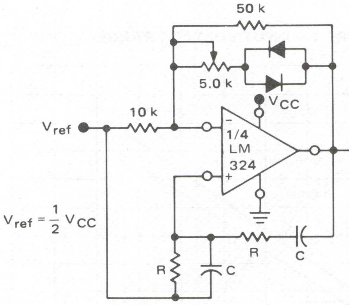

50 k
5.0 k
VCC
10 k
Vref
1/4
LM
324
VO
Vref = 1/2 VCC
R
C
R
C

FIGURE 8 – WIEN BRIDGE OSCILLATOR

$f_o = \frac{1}{2\pi RC}$

For $f_o = 1$ kHz
R = 16 kΩ
C = 0.01 µF

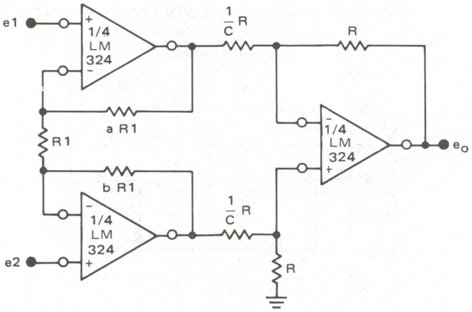

e1
1/4
LM
324
1/C R
R
a R1
R1
b R1
1/4
LM
324
eo
1/4
LM
324
1/C R
e2
R

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

$e_o = C\ (1 + a + b)\ (e2 - e1)$

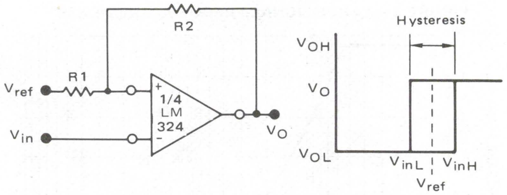

R2
Vref
R1
1/4
LM
324
Vin
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

FIGURE 10 – COMPARATOR WITH HYSTERESIS

$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

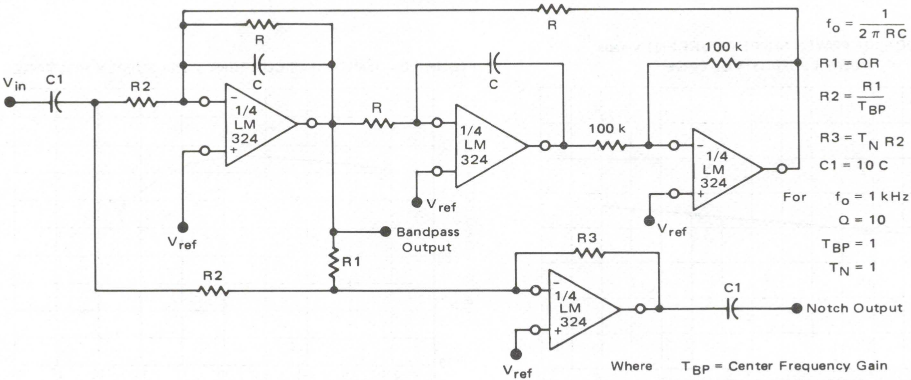

R
R
C
Vin
C1
R2
1/4
LM
324
Vref
R
C
1/4
LM
324
Vref
100 k
100 k
1/4
LM
324
Vref
Bandpass
Output
R1
R2
R3
1/4
LM
324
Vref
C1
Notch Output

FIGURE 11 – BI-QUAD FILTER

$f_o = \frac{1}{2\pi RC}$

R1 = QR

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

C1 = 10 C

$V_{ref} = \frac{1}{2} V_{CC}$

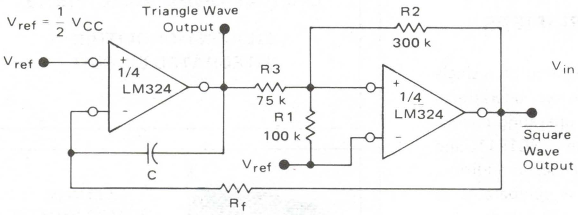
For $f_o = 1$ kHz
Q = 10
$T_{BP} = 1$
$T_N = 1$

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

APPLICATIONS INFORMATION (continued)

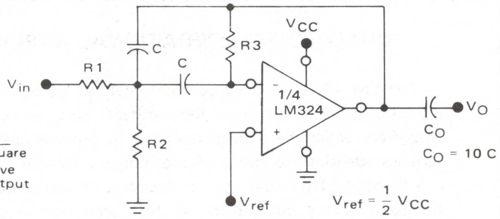
FIGURE 12 – FUNCTION GENERATOR



$V_{ref} = \frac{1}{2} V_{CC}$
Triangle Wave Output
R2
300 k
V_{ref}
+
1/4 LM324
–
R3
75 k
R1
100 k
+
1/4 LM324
–
Square Wave Output
V_{ref}
C
R_f

$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



C
R3
V_{CC}
R1
C
V_{in}
–
1/4 LM324
+
R2
V_O
C_O
C_O = 10 C
V_{ref}
$V_{ref} = \frac{1}{2} V_{CC}$

Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \qquad \text{Where } f_o \text{ and BW are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

LM148
LM248
LM348

MOTOROLA

Specifications and Applications Information

QUAD MC1741 DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

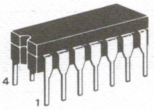
SILICON MONOLITHIC INTEGRATED CIRCUIT

QUAD MC1741 OPERATIONAL AMPLIFIERS

The LM148 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

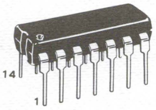
The LM148 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3503 and LM124
- True Differential Inputs
- Internally Frequency Compensated
- Short Circut Protection
- Low Power Supply Current (0.6 mA/Amplifier)

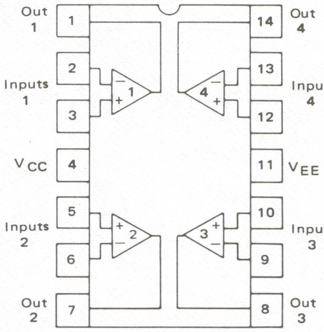


J SUFFIX
CERAMIC PACKAGE
CASE 632-02

N SUFFIX
PLASTIC PACKAGE
CASE 646-05
(LM248 and
LM348 only)

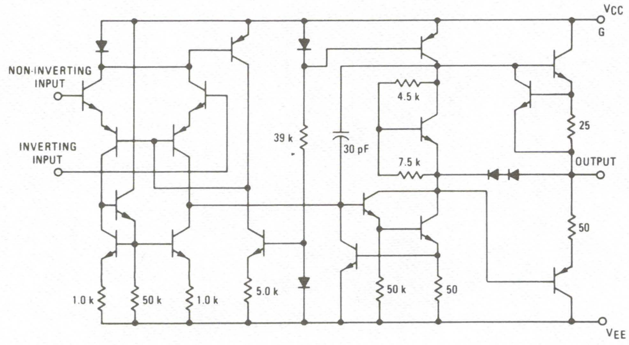


PIN CONNECTIONS


Out 1
1
Inputs 1
2
3
VCC
4
Inputs 2
5
6
Out 2
7
14
Out 4
13
Inputs 4
12
11
VEE
10
Inputs 3
9
8
Out 3
1
2
3
4
+
−

(Top View)

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)


VCC
G
NON-INVERTING INPUT
INVERTING INPUT
4.5 k
39 k
30 pF
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE

ORDERING INFORMATION		
Device	Temperature Range	Package
LM148J	−55 to +125°C	Ceramic DIP
LM248J	−25 to +85°C	Ceramic DIP
LM248N	−25 to +85°C	Plastic DIP
LM348J	0 to +70°C	Ceramic DIP
LM348N	0 to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM148	LM248/LM348		Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18		Vdc Vdc
Input Differential Voltage	V_{ID}	±44	±36		Volts
Input Common Mode Voltage	V_{ICM}	±22	±18		Volts
Output Short Circuit Duration	t_S	Continuous			
Operating Ambient Temperature Range	T_A	−55 to +125	−25 to +85	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125			°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

		LM148			LM248/348			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ k)	V_{IO}	–	1.0	5.0	–	1.0	6.0	mV
Input Offset Current	I_{IO}	–	4.0	25	–	4.0	50	nA
Input Bias Current	I_{IB}	–	30	100	–	30	200	nA
Input Resistance	r_i	0.8	2.5	–	0.8	2.5	–	MΩ
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	±12	–	–	V
Large Signal Voltage Gain ($R_L \geqslant 2.0$ k, $V_O = \pm 10$ V)	A_v	50	160	–	25	160	–	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	–	–	-120	–	–	-120	–	dB
Common Mode Rejection Ratio ($R_S \leqslant 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k)	PSRR	77	96	–	77	96	–	dB
Output Voltage Swing	V_O							V
($R_L \geqslant 10$ k)		±12	±13	–	±12	±13	–	
($R_L \geqslant 2$ k)		±10	±12	–	±10	±12	–	
Output Short-Circuit Current	I_{os}	–	25	–	–	25	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	3.6	–	2.4	4.5	mA
Small Signal Bandwidth (A_v = 1)	BW	–	1.0	–	–	1.0	–	MHz
Phase Margin (A_v = 1)	ϕm	–	60	–	–	60	–	degrees
Slew Rate (A_v = 1)	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted)

Input Offset Voltage ($R_S \leqslant 10$ kΩ)	V_{IO}	–	–	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
LM148		–	–	75	–	–	–	
LM248		–	–	–	–	–	125	
LM348		–	–	–	–	–	100	
Input Bias Current	I_{IB}							nA
LM148		–	–	325	–	–	–	
LM248		–	–	–	–	–	500	
LM348		–	–	–	–	–	400	
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	±12	–	–	V
Large Signal Voltage Gain ($R_L \geqslant 2$ k, $V_O = \pm 10$ V)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio ($R_S \leqslant 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k)	PSRR	77	96	–	77	96	–	dB
Output Voltage Swing	V_O							V
($R_L \geqslant 10$ k)		±12	±13	–	±12	±13	–	
($R_L \geqslant 2$ k)		±10	±12	–	±10	±12	–	

*T_{high} = 125°C for LM148, 85°C for LM248, and 70°C for LM348. T_{low} = −55°C for LM148, −25°C for LM248, and 0°C for LM348.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

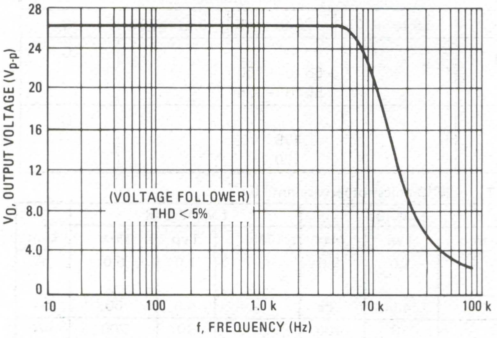


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

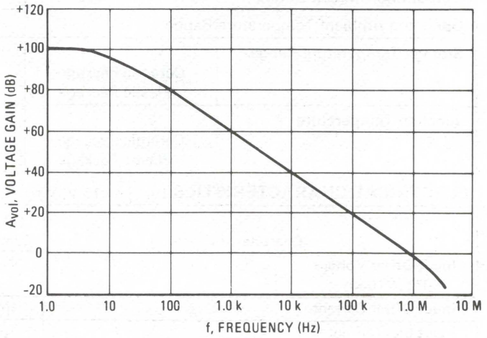


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

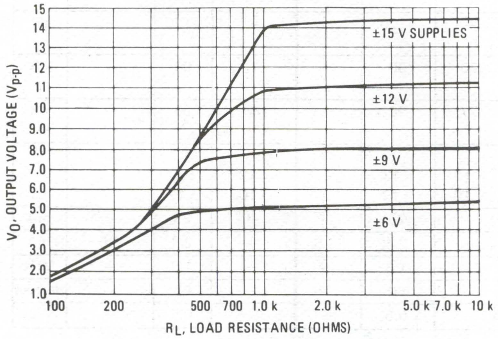


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

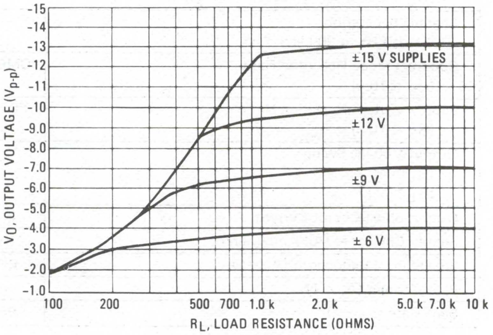


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

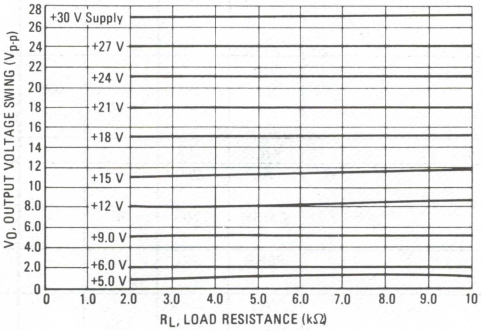


FIGURE 6 — NONINVERTING PULSE RESPONSE

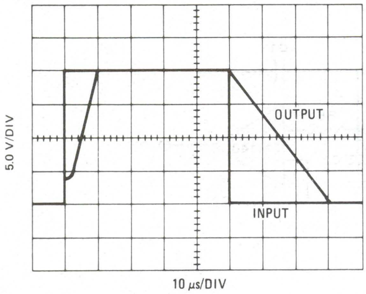
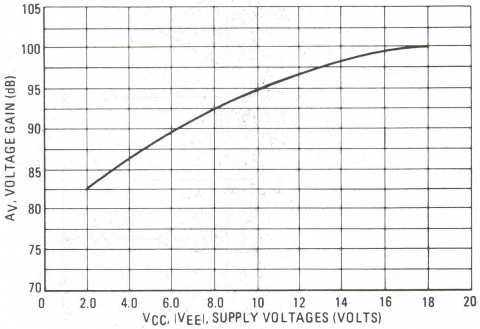
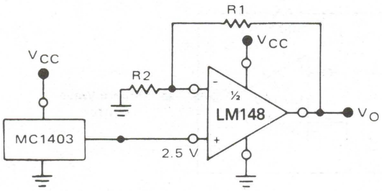


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



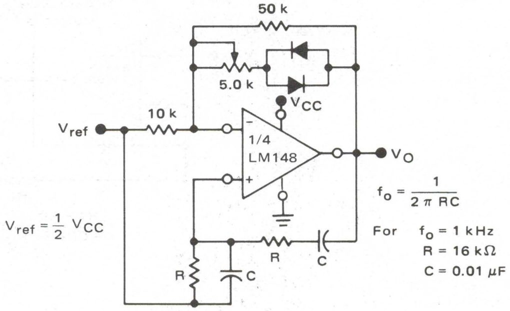
APPLICATIONS INFORMATION

FIGURE 8 — VOLTAGE REFERENCE


R1
VCC
VCC
R2
½
LM148
VO
MC1403
2.5 V

$V_O = 2.5\ V(1 + \frac{R1}{R2})$

FIGURE 9 — WIEN BRIDGE OSCILLATOR


50 k
5.0 k
VCC
10 k
Vref
1/4
LM148
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

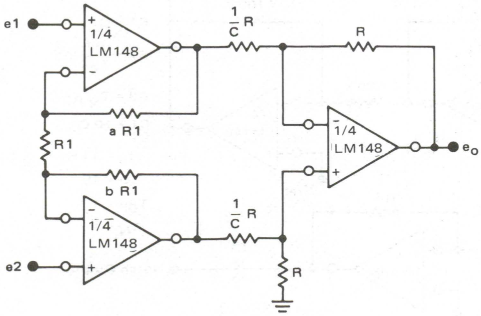
$f_o = \frac{1}{2 \pi RC}$

For $f_o = 1$ kHz

$R = 16\ k\Omega$

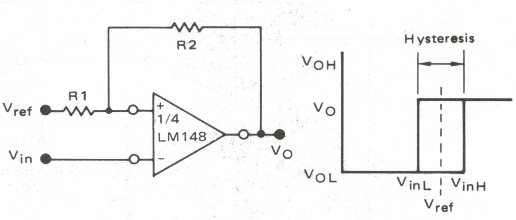
$C = 0.01\ \mu F$

FIGURE 10 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4
LM148
1/C R
R
a R1
R1
1/4
LM148
eo
b R1
1/4
LM148
e2
1/C R
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 11 — COMPARATOR WITH HYSTERESIS


R2
R1
Vref
1/4
LM148
Vin
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$

FIGURE 12 – HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER

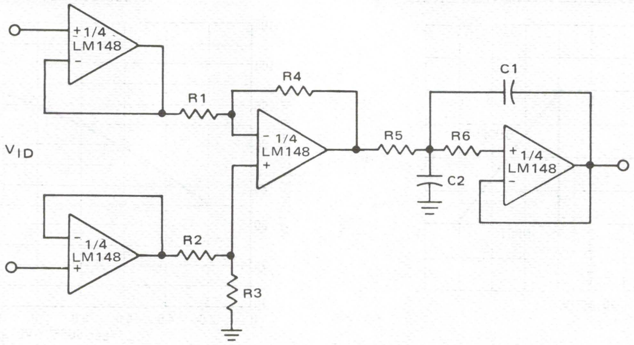

+ 1/4 LM148 –
R1
R4
– 1/4 LM148 +
R5
R6
C1
C2
+ 1/4 LM148 –
V_ID
– 1/4 LM148 +
R2
R3

FIGURE 13 – FUNCTION GENERATOR

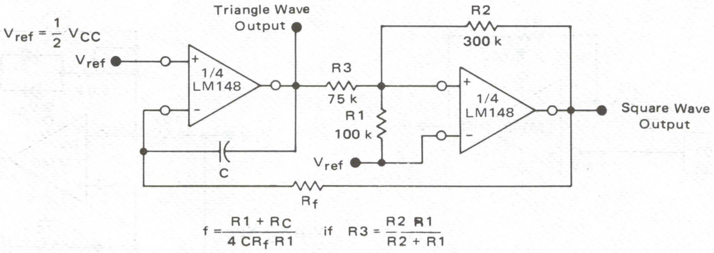

$V_{ref} = \frac{1}{2} V_{CC}$
Triangle Wave Output
R2
300 k
V_{ref}
+ 1/4 LM148 –
R3
75 k
R1
100 k
+ 1/4 LM148 –
Square Wave Output
C
V_{ref}
R_f
$f = \frac{R1 + R_C}{4 CR_f R1}$ if $R3 = \frac{R2\ R1}{R2 + R1}$

FIGURE 14 – BI-QUAD FILTER

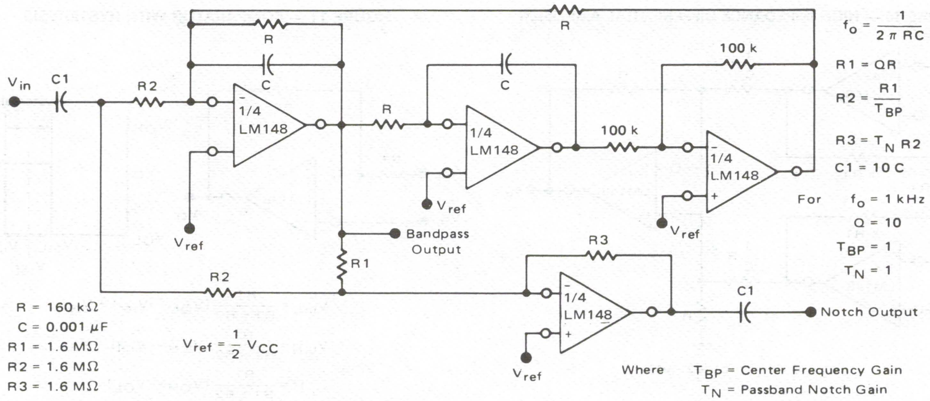
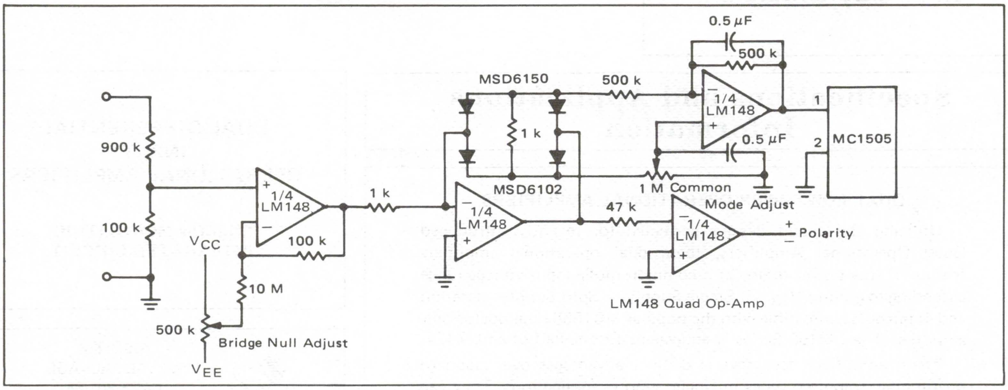

V_{in}
C1
R2
R
C
– 1/4 LM148 +
V_{ref}
R
C
R
1/4 LM148
V_{ref}
100 k
100 k
– 1/4 LM148 +
V_{ref}
Bandpass Output
R1
R2
R3
– 1/4 LM148 +
V_{ref}
C1
Notch Output
$f_o = \frac{1}{2 \pi RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N\ R2$
C1 = 10 C
For f_o = 1 kHz
Q = 10
$T_{BP} = 1$
$T_N = 1$
R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
$V_{ref} = \frac{1}{2} V_{CC}$
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 15 — ABSOLUTE VALUE DVM FRONT END


900 k
100 k
1/4 LM148
100 k
VCC
10 M
500 k
Bridge Null Adjust
VEE
1 k
MSD6150
1 k
MSD6102
1/4 LM148
500 k
0.5 μF
500 k
1/4 LM148
0.5 μF
1 M Common Mode Adjust
47 k
1/4 LM148
Polarity
1
2
MC1505
LM148 Quad Op-Amp

LM158, LM258, LM358, LM2904

MOTOROLA

Specifications and Applications Information

DUAL LOW POWER OPERATIONAL AMPLIFIERS

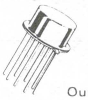
Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

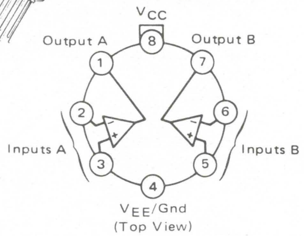
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

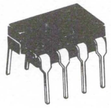
SILICON MONOLITHIC INTEGRATED CIRCUIT

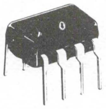


H SUFFIX
METAL PACKAGE
CASE 601-04

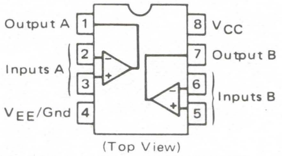


J SUFFIX
CERAMIC PACKAGE
CASE 693-02





N SUFFIX
PLASTIC PACKAGE
CASE 626-04
(LM258, LM358, LM2904 only)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	LM158 LM258 LM358	LM2904	Unit
Power Supply Voltages				Vdc
Single Supply	V_{CC}	32	26	
Split Supplies	V_{CC}, V_{EE}	±16	±13	
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	-0.3 to 26	Vdc
Input Forward Current (3) ($V_I < -0.3$ V)	I_{IF}	50	–	mA
Output Short Circuit Duration	t_S	Continuous		
Junction Temperature	T_J			°C
Ceramic and Metal Packages		175		
Plastic Package		150		
Storage Temperature Range	T_{stg}			°C
Ceramic and Metal Packages		-65 to +150		
Plastic Package		-55 to +125		
Operating Ambient Temperature Range	T_A			°C
LM158		-55 to +125	–	
LM258		-25 to +85	–	
LM358		0 to +70	–	
LM2904		–	-40 to +85	

(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.
(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than -0.3 V.

ORDERING INFORMATION

Device	Temperature Range	Package
LM158H	-55 to +125°C	Metal Can
LM158J	-55 to +125°C	Ceramic DIP
LM2904H	-40 to +85°C	Metal Can
LM2904J	-40 to +85°C	Ceramic DIP
LM2904N	-40 to +85°C	Plastic DIP
LM258H	-25 to +85°C	Metal Can
LM258J	-25 to +85°C	Ceramic DIP
LM258N	-25 to +85°C	Plastic DIP
LM358H	0 to +70°C	Metal Can
LM358J	0 to +70°C	Ceramic DIP
LM358N	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

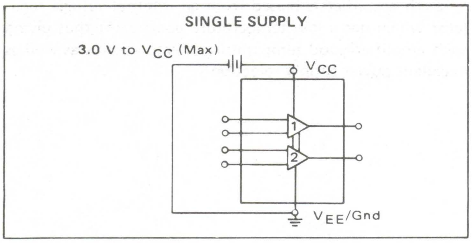
Characteristic	Symbol	LM158/LM258			LM358			LM2904			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}										mV
V_{CC} = 5.0 V to 30 V (26 V for LM2904),											
V_{IC} = 0 V to V_{CC} − 1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω											
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	
T_A = T_{high} to T_{low} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	μV/°C
T_A = T_{high} to T_{low} (Note 1)											
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
T_A = T_{high} to T_{low} (Note 1)											
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	–	-45	-250	nA
T_A = T_{high} to T_{low} (Note 1)		–	-50	-300	–	-50	-500	–	-50	-500	
Input Common-Mode Voltage Range (Note 2)	V_{ICR}										V
V_{CC} = 30 V (26 V for LM2904)		0	–	28.3	0	–	28.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2904), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	–	25	100	–	–	100	–	
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	–	–	–	
Channel Separation	–	–	-120	–	–	-120	–	–	-120	–	dB
1.0 kHz ⩽ f ⩽ 20 kHz, Input Referenced											
Common-Mode Rejection Ratio	CMRR	70	85	–	65	70	–	50	70	–	dB
R_S ⩽ 10 kΩ											
Power Supply Rejection Ratio	PSRR	65	100	–	65	100	–	50	100	–	dB
Output Voltage Range	V_{OR}	0	–	3.3	0	–	3.3	0	–	3.3	V
R_L = 2 kΩ (R_L ⩾ 10 kΩ for LM2904)											
Output Voltage—High Limit (T_A = T_{high} to T_{low})(Note 1)	V_{OH}										V
V_{CC} = 30 V (26 V for LM2904), R_L = 2 kΩ		26	–	–	26	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	
Output Voltage—Low Limit	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	mV
V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)											
Output Source Current	I_{O+}	20	40	–	20	40	–	20	40	–	mA
V_{ID} = +1.0 V, V_{CC} = 15 V											
Output Sink Current	I_{O-}										
V_{ID} = −1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	mA
V_{ID} = −1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	μA
Output Short Circuit to Ground (Note 3)	I_{os}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(Note 1)	I_{CC}										mA
V_{CC} = 30 V (26 V for LM2904), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

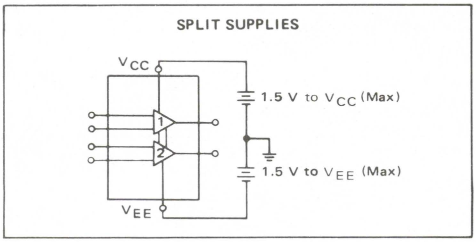
NOTES:

(1) T_{low} = −55°C for LM158 T_{high} = +125°C for LM158
= −40°C for LM2904 = +85°C for LM2904
= −25°C for LM258 and LM258
= 0°C for LM358 = +70°C for LM358

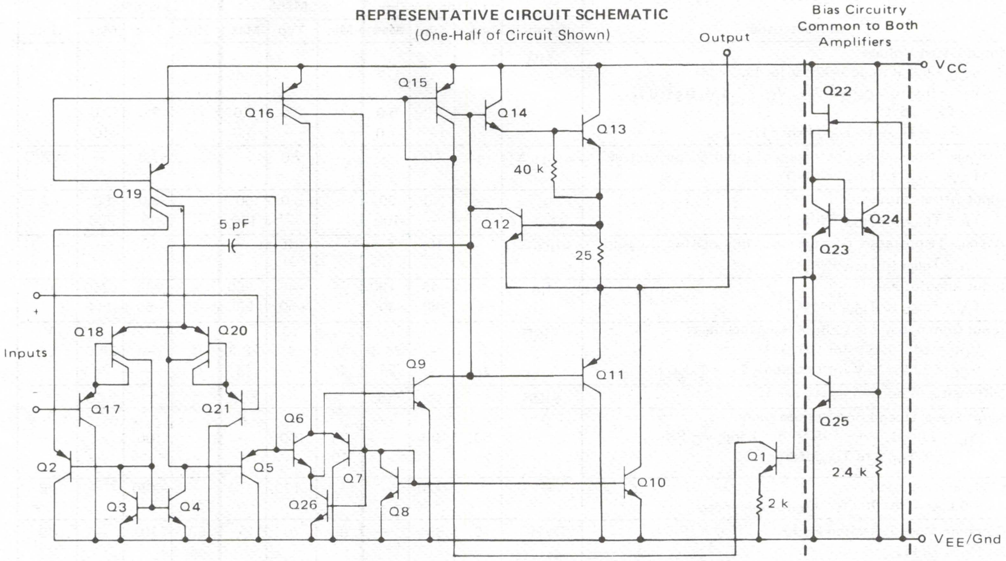
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} −1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2904).

(3) Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

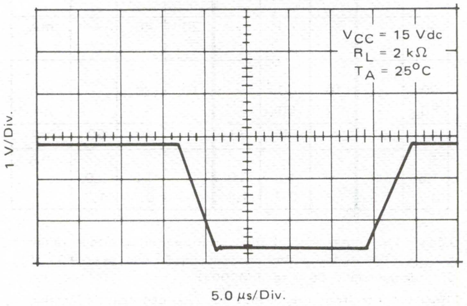

SINGLE SUPPLY


SPLIT SUPPLIES

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Half of Circuit Shown)


Output
Bias Circuitry
Common to Both
Amplifiers
VCC
Q15
Q16
Q14
Q13
Q22
40 k
Q19
5 pF
Q12
25
Q24
Q23
+
Inputs
−
Q18
Q20
Q17
Q21
Q9
Q11
Q25
Q6
Q2
Q5
Q7
Q1
Q10
2.4 k
Q3
Q4
Q26
Q8
2 k
VEE/Gnd

LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE



CIRCUIT DESCRIPTION

The LM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

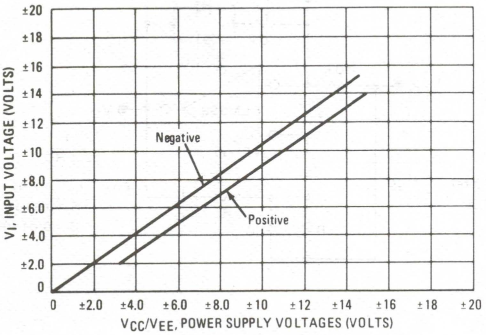


FIGURE 2 – OPEN LOOP FREQUENCY

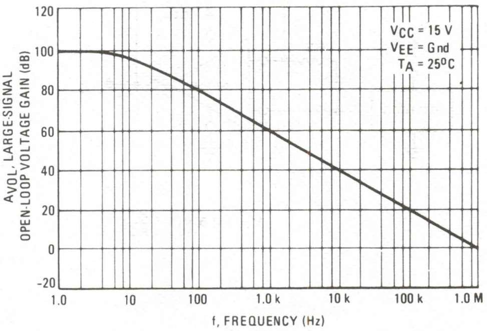


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

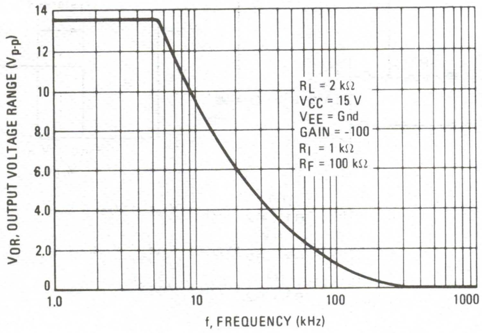


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

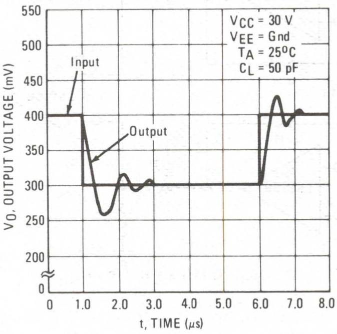


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

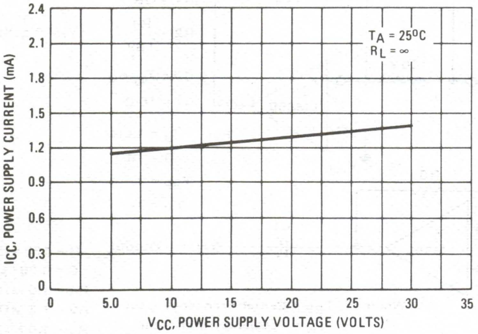
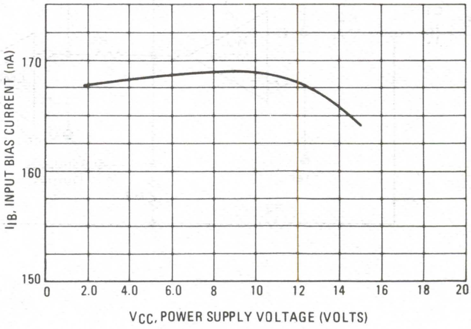
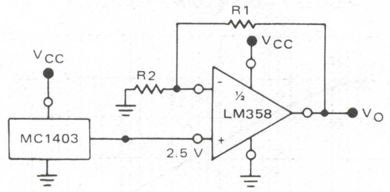


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



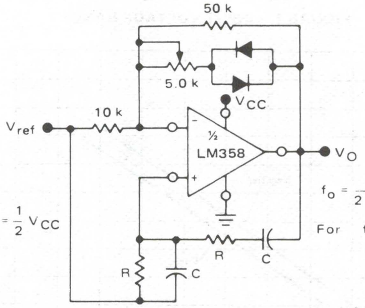
APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE


R1
V_CC
V_CC
R2
½
LM358
V_O
MC1403
2.5 V

$$V_O = 2.5\ V(1 + \frac{R1}{R2})$$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

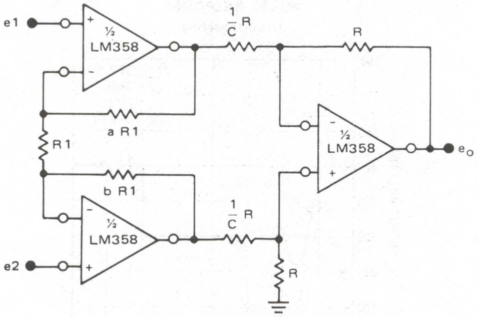

50 k
5.0 k
V_CC
10 k
V_ref
½
LM358
V_O
R
C
R
C

$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

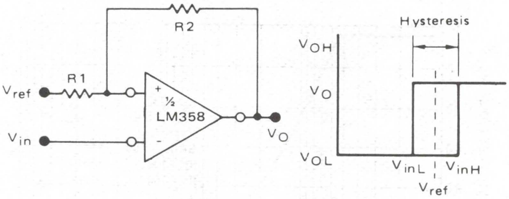
For $f_o = 1$ kHz
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
½
LM358
1/C R
R
a R1
R1
b R1
½
LM358
e_o
½
LM358
1/C R
e2
R

$$e_O = C\ (1 + a + b)\ (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

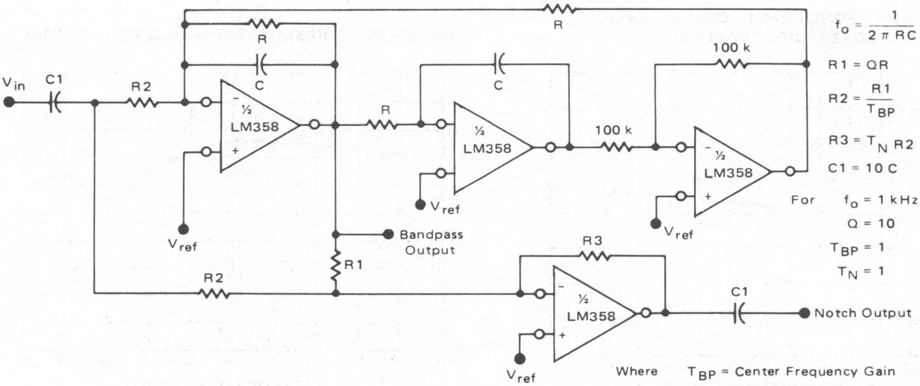

R2
V_ref
R1
½
LM358
V_in
V_O
Hysteresis
V_OH
V_O
V_OL
V_inL
V_inH
V_ref

$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER


R
R
C
C
100 k
V_in
C1
R2
½
LM358
R
½
LM358
100 k
½
LM358
V_ref
V_ref
V_ref
Bandpass Output
R3
R1
R2
½
LM358
C1
Notch Output
V_ref

$$f_o = \frac{1}{2 \pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\ R2$
$C1 = 10\ C$

$$V_{ref} = \frac{1}{2} V_{CC}$$

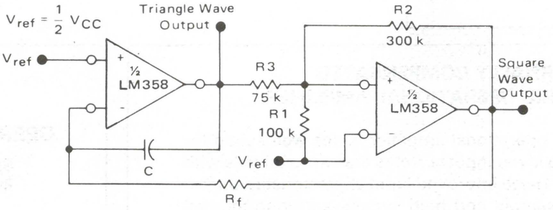
For $f_o = 1$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

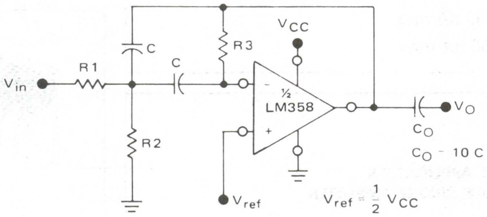
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR


$V_{ref} = \frac{1}{2} V_{CC}$
Triangle Wave Output
R2
300 k
V_{ref}
+
½ LM358
-
R3
75 k
R1
100 k
+
½ LM358
-
Square Wave Output
C
V_{ref}
R_f

$$f = \frac{R1 + R_C}{4\ C R_f\ R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


V_{CC}
C
R3
R1
C
V_{in}
-
½ LM358
+
R2
V_O
C_O
C_O – 10 C
V_{ref}
$V_{ref} = \frac{1}{2} V_{CC}$

Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi\ f_o\ C}$$

$$R1 = \frac{R3}{2\ A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o\ f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

LM307

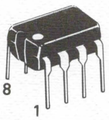
INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

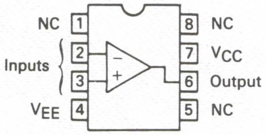
- Internally Compensated
- Low Offset Voltage: 7.5 mV max
- Low Input Offset Current: 50 nA max
- Low Input Bias Current: 250 nA max

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

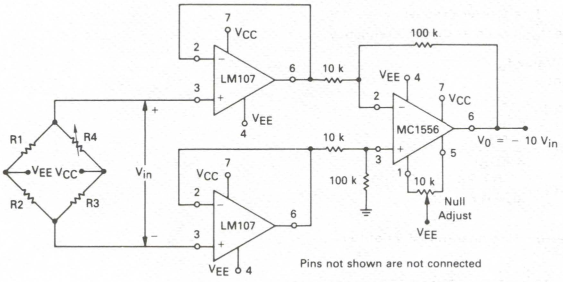


N SUFFIX
PLASTIC PACKAGE
CASE 626-04


NC 1
Inputs
2
3
VEE 4
8 NC
7 VCC
6 Output
5 NC
−
+

(Top View)

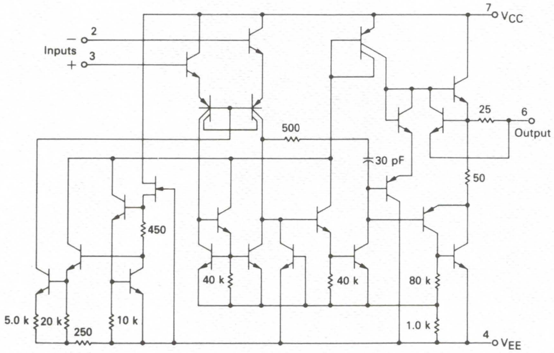
TYPICAL APPLICATION HIGH IMPEDANCE BRIDGE AMPLIFIER


7
VCC
2
3
−
+
LM107
6
VEE
4
10 k
100 k
VEE 4
7
VCC
2
3
MC1556
6
5
1
10 k
Null Adjust
VEE
100 k
VO = − 10 Vin
R1
R4
R2
R3
VEE VCC
Vin
+
−
Pins not shown are not connected

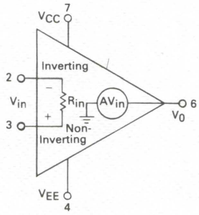
ORDERING INFORMATION

Device	Temperature Range	Package
LM307N	0°C to +70°C	Plastic DIP

CIRCUIT SCHEMATIC


7 VCC
Inputs
− 2
+ 3
500
25
6
Output
30 pF
50
450
40 k
40 k
80 k
5.0 k
20 k
250
10 k
1.0 k
4 VEE

EQUIVALENT CIRCUIT


VCC 7
2
Inverting
Vin
Rin
AVin
3
Non-Inverting
6
VO
VEE 4

Pins 1, 5, and 8 no connection.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	LM307	Unit
Power Supply Voltages	V_{CC} V_{EE}	+18 −18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	±15	Volts
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation (Package Limitation) (Note 2)	P_D	500	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 3.)

Characteristics	Symbol	LM307			Unit
		Min	Typ	Max	
Input Offset Voltage $R_S \leq 50$ kΩ, T_A = + 25°C $R_S \leq 50$ kΩ, T_A = T_{low} to T_{high}	V_{IO}	 — —	 2.0 —	 7.5 10	mV
Input Offset Current T_A = +25°C T_A = T_{low} to T_{high}	I_{IO}	 — —	 3.0 —	 50 70	nA
Input Bias Current T_A = +25°C T_A = T_{low} to T_{high}	I_{IB}	 — —	 70 —	 250 300	nA
Input Resistance	r_i	0.5	2.0	—	MΩ
Supply Current V_S = ±15 V, T_A = +25°C	I_D	—	1.8	3.0	mA
Large-Signal Voltage Gain V_S = ±15 V, V_O = ±10 V, $R_L > 2.0$ kΩ, T_A = +25°C V_S = ±15 V, V_O = ±10 V, $R_L \geq 2.0$ kΩ, T_A = T_{low}	A_v	 25 15	 160 —	 — —	V/mV
Average Temperature Coefficient of Input Offset Voltage $T_{low} \leq T_A \leq T_{high}$	TCV_{IO}	—	6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current +25°C ≤ $T_A \leq T_{high}$ $T_{low} \leq T_A \leq$ +25°C	TCI_{IO}	 — —	 0.01 0.02	 0.3 0.6	nA/°C
Output Voltage Swing (T_A = T_{low} to T_{high}) V_S = ±15 V, R_L = 10 kΩ R_L = 2.0 kΩ	V_O	 ±12 ±10	 +14 ±13	 — —	V
Input Voltage Range (T_A = T_{low} to T_{high}) V_S = ±15 V	V_{ICR}	±12	—	—	V
Common-Mode Rejection Ratio (T_A = T_{low} to T_{high}) $R_S \leq 50$ kΩ	CMRR	70	90	—	dB
Supply-Voltage Rejection Ratio (T_A = T_{low} to T_{high}) $R_S \leq 50$ kΩ	PSRR	70	96	—	dB

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of 100°C for the LM307. The H package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for: ±5.0 V ≤ V_{CC}/V_{EE} ≤ ±15 V, T_{low} = 0°C, T_{high} = +70°C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 — MINIMUM INPUT VOLTAGE RANGE

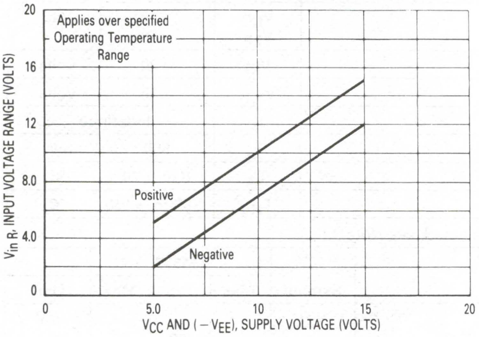


FIGURE 2 — MINIMUM OUTPUT VOLTAGE SWING

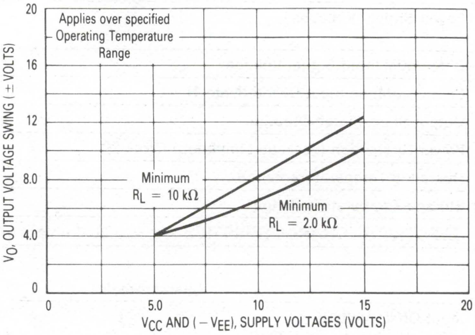


FIGURE 3 — MINIMUM VOLTAGE GAIN

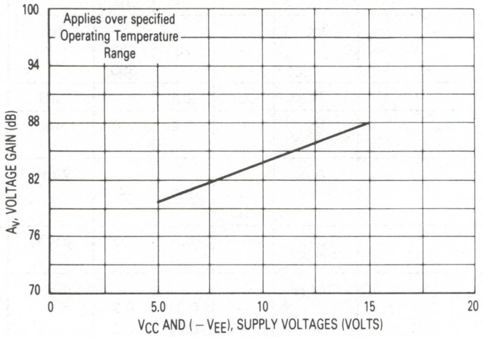


FIGURE 4 — TYPICAL SUPPLY CURRENTS

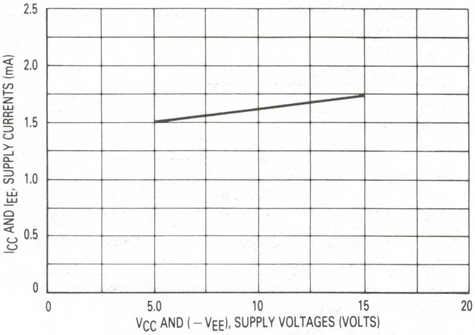


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

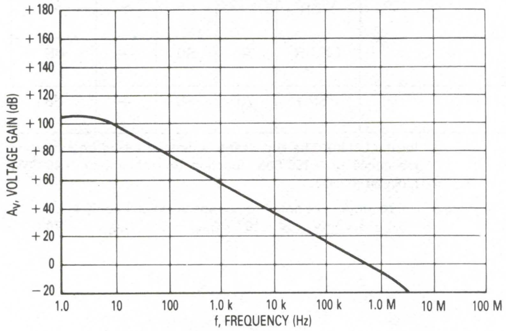
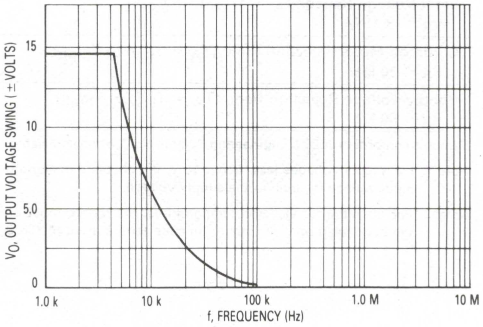
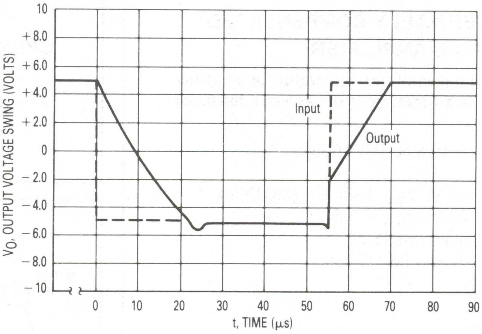


FIGURE 6 — LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — VOLTAGE FOLLOWER PULSE RESPONSE



MC1436
MC1436C
MC1536

ORDERING INFORMATION

Device	Temperature Range	Package
MC1436P1	0°C to +70°C	Plastic DIP
MC136CP1	0°C to +70°C	Plastic DIP
MC1436G	0°C to +70°C	Metal Can
MC1436U	0°C to +70°C	Ceramic DIP
MC1436CG	0°C to +70°C	Metal Can
MC1436CU	0°C to +70°C	Ceramic DIP
MC1536G	−55°C to +125°C	Metal Can
MC1536U	−55°C to +125°C	Ceramic DIP

HIGH VOLTAGE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ±40 Vdc (MC1536)
- Output Voltage Swing –
  $\pm 30\ V_{pk(min)}$ (V_{CC} = +36 V, V_{EE} = −36 V) (MC1536)
  $\pm 22\ V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = −28 V)
- Input Bias Current – 20 nA max (MC1536)
- Input Offset Current – 3.0 nA max (MC1536)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601-04

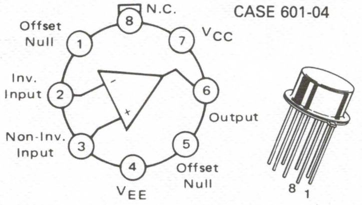
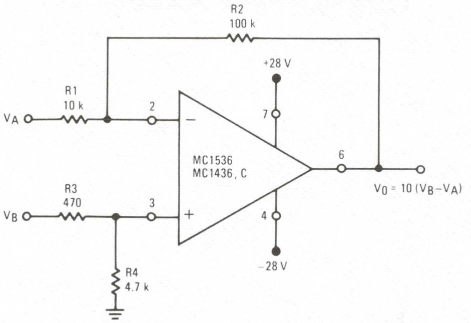
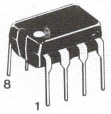
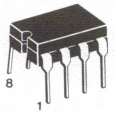

N.C.
8
Offset Null
1
7
V_{CC}
Inv. Input
2
6
Output
Non-Inv. Input
3
5
Offset Null
4
V_{EE}
8
1

FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ± 20 V COMMON-MODE INPUT VOLTAGE RANGE


R2
100 k
+28 V
R1
10 k
V_A
2
7
MC1536
MC1436, C
6
$V_O = 10 (V_B - V_A)$
R3
470
V_B
3
4
−28 V
R4
4.7 k





P SUFFIX
PLASTIC PACKAGE
CASE 626-04

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

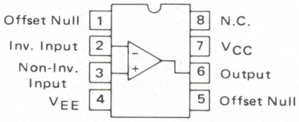

Offset Null 1
Inv. Input 2
Non-Inv. Input 3
V_{EE} 4
8 N.C.
7 V_{CC}
6 Output
5 Offset Null

FIGURE 2 — TYPICAL NONINVERTING X10 VOLTAGE AMPLIFIER

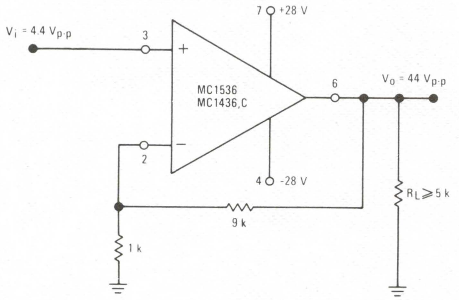
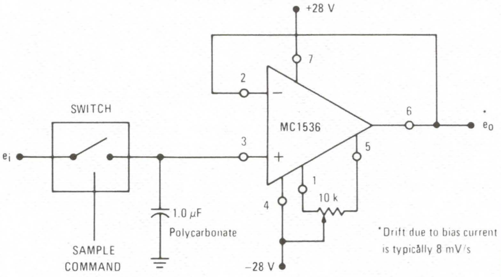

V_i = 4.4 $V_{p\text{-}p}$
3
7 +28 V
MC1536
MC1436,C
6
V_O = 44 $V_{p\text{-}p}$
2
4 −28 V
$R_L \geq 5$ k
9 k
1 k

FIGURE 3 — LOW-DRIFT SAMPLE AND HOLD


+28 V
7
2
SWITCH
MC1536
6
e_o
e_i
3
5
1
10 k
4
1.0 μF
Polycarbonate
SAMPLE COMMAND
−28 V

*Drift due to bias current is typically 8 mV/s

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 -40	+34 -34	+30 -30	Vdc
Input Differential Voltage Range	V_{IDR}	$\pm(V_{CC} + V_{EE} - 3)$			Volts
Input Common-Mode Voltage Range	V_{ICR}	$+V_{CC}, -(V_{EE} - 3)$			Volts
Output Short Circuit Duration ($V_{CC} = V_{EE}$ = 28 Vdc, V_o = 0)	t_S	5.0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 Vdc, V_{EE} = -28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536			MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}										nAdc
T_A = +25°C		–	8.0	20	–	15	40	–	25	90	
$T_A = T_{low}$ to T_{high} (See Note 1)		–	–	35	–	–	55	–	–	–	
Input Offset Current	I_{IO}										nAdc
T_A = +25°C		–	1.0	3.0	–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	4.5	–	–	14	–	–	–	
$T_A = T_{low}$ to +25°C		–	–	7.0	–	–	14	–	–	–	
Input Offset Voltage	V_{IO}										mVdc
T_A = +25°C		–	2.0	5.0	–	5.0	10	–	5.0	12	
$T_A = T_{low}$ to T_{high}		–	–	7.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)											
Parallel Input Resistance	r_P	–	10	–	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_P	–	2.0	–	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	–	250	–	–	250		–	250	–	Meg ohms
Input Common-Mode Voltage Range	V_{ICR}	±24	±25	–	±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	50	–	–	50	–	–	50	–	nV/(Hz)½
Common-Mode Rejection Ratio (dc)	CMRR	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}										V/V
(V_o = ± 10 V, R_L = 100 k ohms) T_A = +25°C		100,000	500,000	–	70,000	500,000	–	50,000	500,000	–	
(V_o = ± 10 V, R_L = 100 k ohms) $T_A = T_{low}$ to T_{high}		50,000	–	–	50,000	–	–	–	–	–	
(V_o = ±10 V, R_L = 10 k ohms, T_A = +25°C)		–	200,000	–		200,000		–	200,000	–	
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_o = 40 Vp-p)	BW_P	–	23	–	–	23	–	–	23	–	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕm	–	50	–	–	50	–	–	50	–	degrees
Gain Margin	A_M	–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	SR	–	2.0	–	–	2.0	–	–	2.0	–	V/µs
Output Impedance (f ≤ 5.0 Hz)	z_o	–	1.0	–	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{OS}	–	±17	–	–	±17			±19	–	mAdc
Output Voltage Range (R_L = 5.0 k ohms)	V_{OR}										V_{pk}
V_{CC} = +28 Vdc, V_{EE} = -28 Vdc		±22	±23	–	±20	±22	–	±20	±22	–	
V_{CC} = +36 Vdc, V_{EE} = -36 Vdc		±30	±32	–	–	–	–	–	–	–	
Power Supply Sensitivity (dc)											µV/V
V_{EE} = constant, R_s ≤ 10 k ohms	PSS+	–	15	100	–	35	200	–	50	–	
V_{CC} = constant, R_s ≤ 10 k ohms	PSS-	–	15	100	–	35	200	–	50	–	
Power Supply Current (See Note 2)	I_{CC}	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	mAdc
	I_{EE}	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	
DC Quiescent Power Consumption (V_o = 0)	P_C	–	124	224	–	146	280	–	146	280	mW

Note 1: T_{low}: 0°C for MC1436,C
-55°C for MC1536
T_{high}: +70°C for MC1436,C
+125°C for MC1536

Note 2: $V_{CC} = V_{EE}$ = 5.0 Vdc to 36 Vdc for MC1536
$V_{CC} = V_{EE}$ = 5.0 Vdc to 30 Vdc for MC1436
$V_{CC} = V_{EE}$ = 5.0 Vdc to 28 Vdc for MC1436C

FIGURE 4 – POWER BANDWIDTH

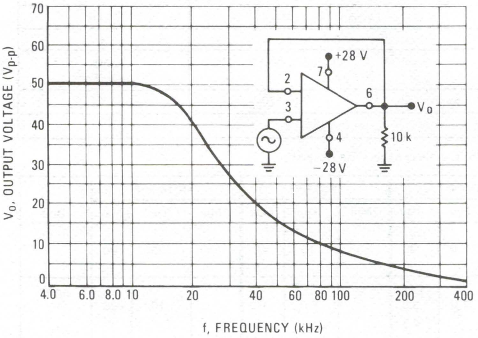


FIGURE 5 – PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

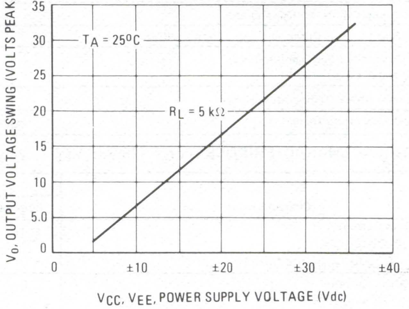


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

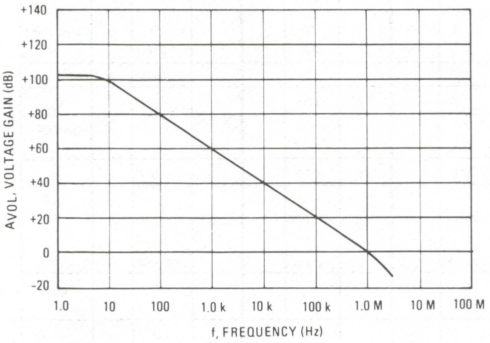


FIGURE 7 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

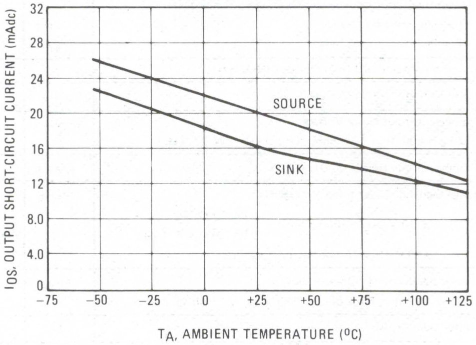


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

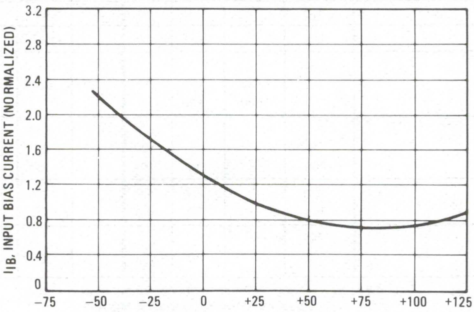
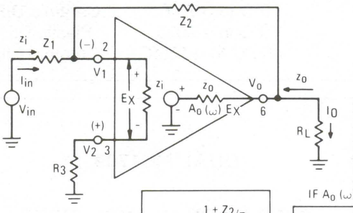


FIGURE 9 – INVERTING FEEDBACK MODEL



Z2
zi
Z1
(-) 2
Iin
V1
Vin
+
EX
-
zi
zo
Vo
Ao (ω) EX
6
zo
Io
RL
(+)
V2 3
R3

$$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$$

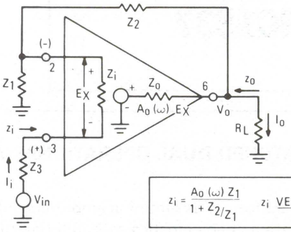
IF $A_o(\omega) \to \infty$

$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

IF $R_3 << Z_1$

$$z_i \approx Z_1$$

FIGURE 10 – NON-INVERTING FEEDBACK MODEL



Z2
(-)
2
Z1
EX
Zi
Zo
Ao (ω) EX
6
Vo
zo
RL
Io
zi
(+) 3
Z3
Ii
Vin

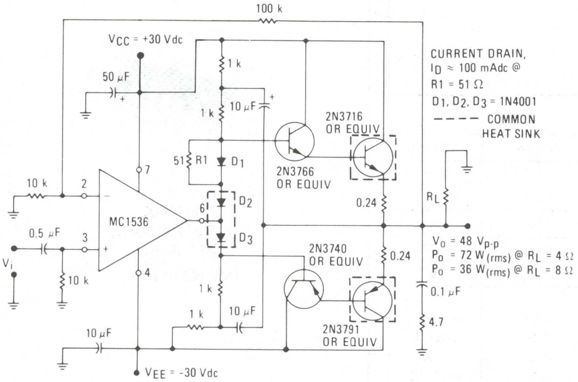
$$z_i = \frac{A_o(\omega)\, Z_1}{1 + Z_2/Z_1} \quad z_i\ \underline{\text{VERY}}\ \underline{\text{HIGH}}$$

$$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$$

$z_o \to 0$
$A_o(\omega) \to \infty$

$$\frac{V_o}{V_i} = 1 + Z_2/Z_1 \quad \text{When } A_o(\omega) \to \infty$$

FIGURE 11 – AUDIO AMPLIFIER

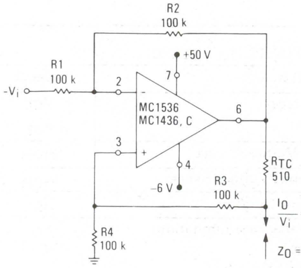


100 k
VCC = +30 Vdc
50 µF
1 k
10 µF
1 k
2N3716 OR EQUIV
51 R1
D1
2N3766 OR EQUIV
7
10 k
2
MC1536
6
D2
D3
0.24
RL
0.5 µF
3
Vi
10 k
4
2N3740 OR EQUIV
0.24
1 k
10 µF
1 k
2N3791 OR EQUIV
0.1 µF
4.7
10 µF
VEE = -30 Vdc

CURRENT DRAIN,
$I_D \approx 100$ mAdc @
$R1 = 51\ \Omega$
D_1, D_2, D_3 = 1N4001
– – – – COMMON HEAT SINK

V_o = 48 $V_{p\text{-}p}$
P_o = 72 $W_{(rms)}$ @ $R_L = 4\ \Omega$
P_o = 36 $W_{(rms)}$ @ $R_L = 8\ \Omega$

FIGURE 12 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

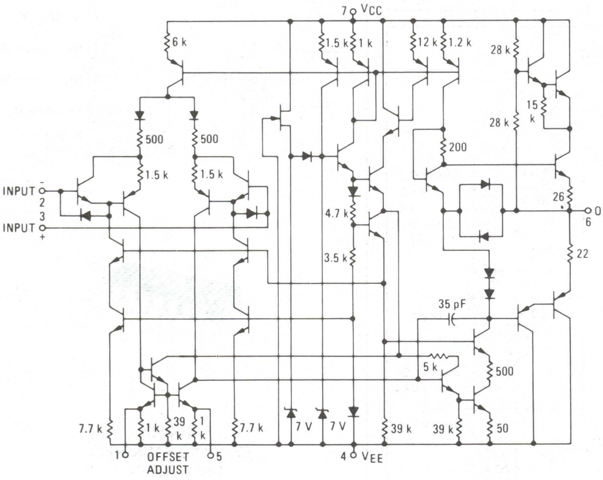


R2
100 k
+50 V
R1
100 k
-Vi
2
7
MC1536
MC1436, C
6
3
4
-6 V
RTC
510
R3
100 k
R4
100 k

$$\frac{I_O}{V_i} = \frac{I}{R_{TC}} = 2\ \text{mA/V}$$

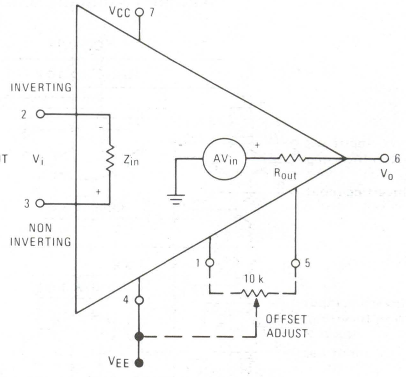
$$Z_O = \frac{R1\, R_{TC}\,(R3 + R4)}{R1(R_{TC} + R3) - R2\, R4}$$

FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC



7 VCC
6 k
1.5 k
1 k
12 k
1.2 k
28 k
15 k
28 k
500
500
200
1.5 k
1.5 k
INPUT -
2
3
INPUT +
4.7 k
26
OUTPUT
6
3.5 k
22
35 pF
5 k
500
7.7 k
1 k
39 k
1 k
7.7 k
7 V
7 V
39 k
39 k
50
1
OFFSET ADJUST
5
4 VEE

FIGURE 14 – EQUIVALENT CIRCUIT



VCC 7
INVERTING
2
Vi
Zin
AVin
Rout
6
Vo
3
NON INVERTING
1
5
10 k
4
OFFSET ADJUST
VEE

MC1437
MC1537

ORDERING INFORMATION

Device	Temperature Range	Package
MC1437L	0°C to +70°C	Ceramic DIP
MC1437P	0°C to +70°C	Plastic DIP
MC1537L	−55°C to +125°C	Ceramic DIP

MATCHED DUAL OPERATIONAL AMPLIFIERS

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

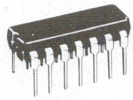
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – A_{VOL} = 45,000 typical
- Low Temperature Drift – ± 3 μV/°C
- Large Output Voltage Swing – ± 14 V typical @ ± 15 V Supply

DUAL MC1709

OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

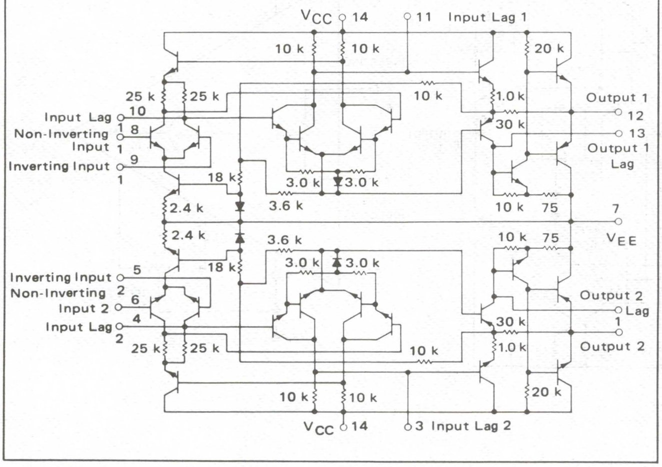


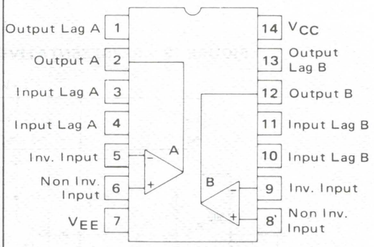
P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC1437P only)

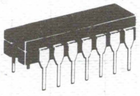
MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	Vdc Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	$\pm V_{CC}$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		750	mW
Derate above T_A = +25°C		6.0	mW/°C
Plastic Package MC1437P		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC1537		-55 to +125	
MC1437		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC


V_{CC} 14
11 Input Lag 1
10 k
10 k
20 k
25 k
25 k
10 k
Input Lag 10
1.0 k
Output 1
12
Non-Inverting 8
30 k
13
Input 1
Output 1
Lag
Inverting Input 9
1
18 k
3.0 k
3.0 k
2.4 k
3.6 k
10 k
75
7
2.4 k
3.6 k
10 k
75
V_{EE}
3.0 k
3.0 k
18 k
Inverting Input 5
Non-Inverting 2
6
Output 2
Lag
Input 2
4
30 k
1
Input Lag 2
25 k
25 k
10 k
1.0 k
Output 2
10 k
10 k
20 k
V_{CC} 14
3 Input Lag 2


Output Lag A 1
Output A 2
Input Lag A 3
Input Lag A 4
Inv. Input 5
Non Inv. Input 6
V_{EE} 7
14 V_{CC}
13 Output Lag B
12 Output B
11 Input Lag B
10 Input Lag B
9 Inv. Input
8 Non Inv. Input
A
B



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

ELECTRICAL CHARACTERISTICS – Each Amplifier (V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = +25°C unless otherwise noted.)

		MC1537			MC1437			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_O = ±10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	z_i	150	400	–	50	150	–	kΩ
Output Voltage Range	V_{OR}							V_{peak}
(R_L = 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L = 2.0 kΩ)		±10	±13	–	–	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	70	100	–	65	100	–	dB
Input Bias Current	I_{IB}							μA
$\left(I_{IB} = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C)		–	0.2	0.5	–	0.4	1.5	
(T_A = T_{low} ①)		–	0.5	1.5	–	–	2.0	
Input Offset Current	I_{IO}							μA
(I_{IO} = $I_1 - I_2$)		–	0.05	0.2	–	0.05	0.5	
(I_{IO} = $I_1 - I_2$, T_A = T_{low} ①)		–	–	0.5	–	–	0.75	
(I_{IO} = $I_1 - I_2$, T_A = T_{high} ②)		–	–	0.2	–	–	0.75	
Input Offset Voltage	V_{IO}							mV
(T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	10	
Step Response								
(Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF)	t_{TLH}	–	0.8	–	–	0.8	–	μs
	t_{PLH}-t_{PHL}	–	0.38	–	–	0.38	–	μs
	SR	–	12	–	–	12	–	V/μs
(Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF)	t_{TLH}	–	0.6	–	–	0.6	–	μs
	t_{PLH}-t_{PHL}	–	0.34	–	–	0.34	–	μs
	SR	–	1.7	–	–	1.7	–	V/μs
(Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF)	t_{TLH}	–	2.2	–	–	2.2	–	μs
	t_{PLH}-t_{PHL}	–	1.3	–	–	1.3	–	μs
	SR	–	0.25	–	–	0.25	–	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
(R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)		–	1.5	–	–	1.5	–	
($R_S \leqq$ 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
Average Temperature Coefficient of Input Offset Voltage	$\Delta I_{IO}/\Delta T$							nA/°C
(T_A = T_{low} ① to +25°C)		–	0.7	–	–	0.7	–	
(T_A = +25°C to T_{high} ②)		–	0.7	–	–	0.7	–	
DC Power Consumption (Total) (Power Supply = ±15 V, V_O = 0)	P_C	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V_{EE} constant)	PSS+	–	10	150	–	10	200	μV/V
Negative Supply Sensitivity (V_{CC} constant)	PSS–	–	10	150	–	10	200	μV/V

① T_{low} = 0°C for MC1437
= -55°C for MC1537

② T_{high} = +70°C for MC1437
= +125°C for MC1537

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{IB1}-I_{IB2}	–	±0.15	–	–	±0.15	–	μA
Input Offset Current	I_{IO1}-I_{IO2}	–	±0.02	–	–	±0.02	–	μA
Average Temperature Coefficient	$\left\lvert\frac{\Delta I_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta I_{IO2}}{\Delta T}\right\rvert$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	V_{IO1}-V_{IO2}	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta V_{IO2}}{\Delta T}\right\rvert$	–	±0.5	–	–	±0.5	–	μV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	90	–	–	90	–	dB

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT

$V_{CC} = +15$ Vdc, $V_{EE} = 15$ Vdc, $T_A = 25^{\circ}C$

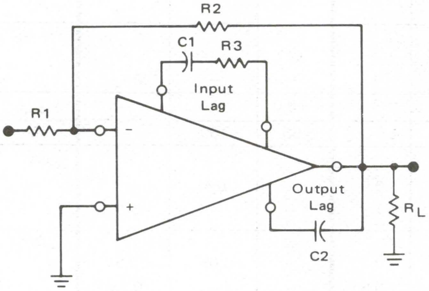


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS					OUTPUT NOISE (mV[rms])
			R_1(Ω)	R_2(Ω)	R_3(Ω)	C_1(pF)	C_2(pF)	
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

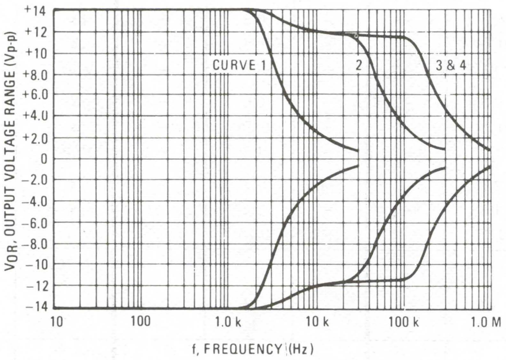


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

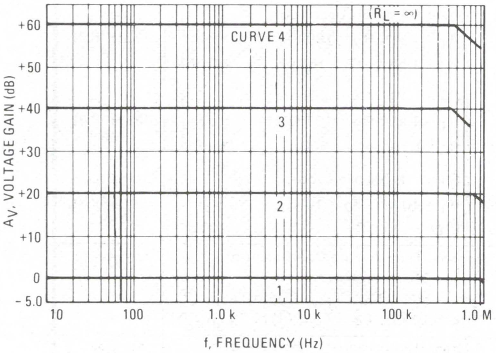


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

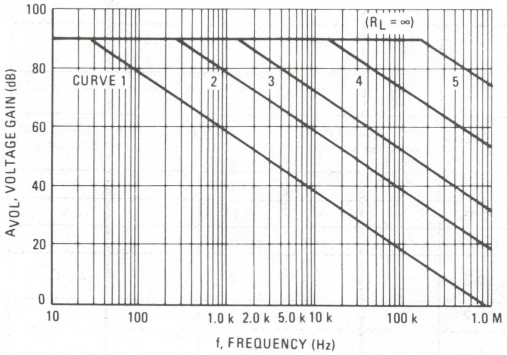
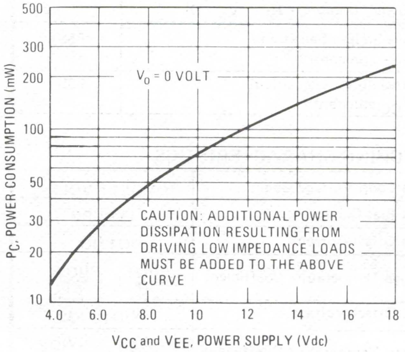


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

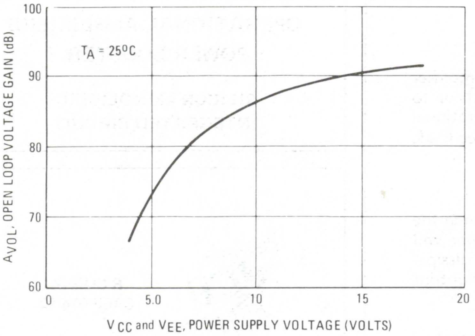


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

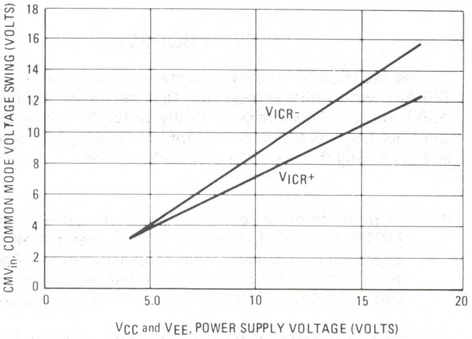


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

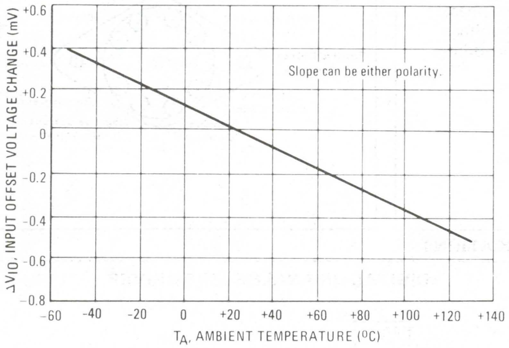


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

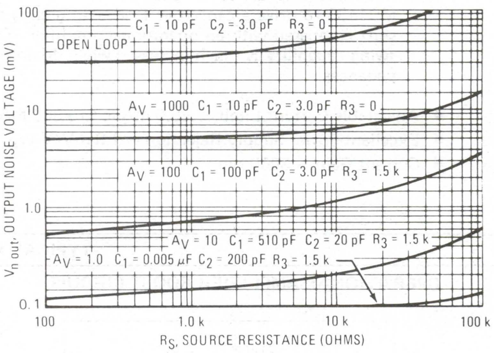
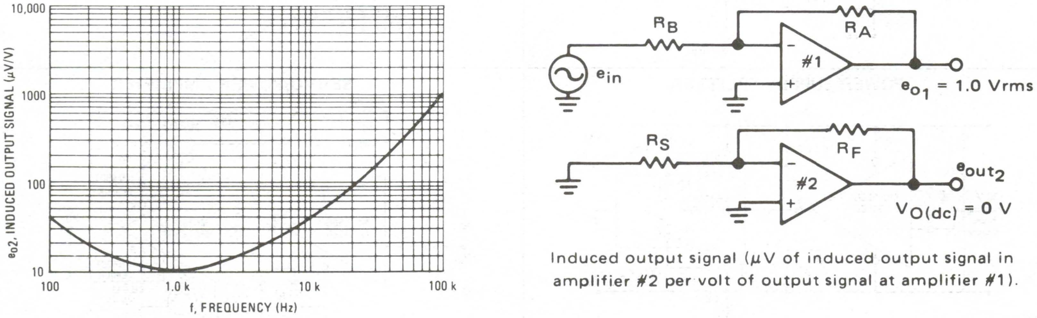


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY



Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

MC1438R
MC1538R

ORDERING INFORMATION

Device	Temperature Range	Package
MC1438R	0°C to +70°C	Metal Power
MC1538R	−55°C to +125°C	Metal Power

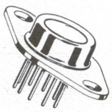
POWER BOOSTER

The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ±300 mAdc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

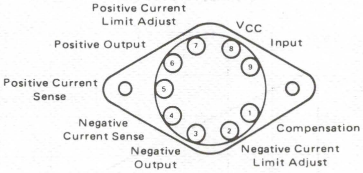
- High Input Impedance – 0.4 Meg-Ohm typ – when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth – 1.5 MHz typ – considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance – 10 Ohms typ – allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit – ±5.0 mAdc to ±300 mAdc
- Excellent Power-Supply Rejection – 1.0 mV/V typ
- Current Gain – 3000 typ

OPERATIONAL AMPLIFIERS
POWER BOOSTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

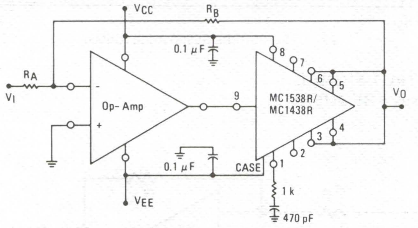


R SUFFIX
CASE 614-02

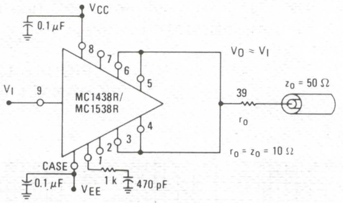

Positive Current Limit Adjust
VCC
Input
Positive Output
Positive Current Sense
Negative Current Sense
Negative Output
Compensation
Negative Current Limit Adjust
7
8
9
6
5
4
3
2
1

TYPICAL APPLICATIONS

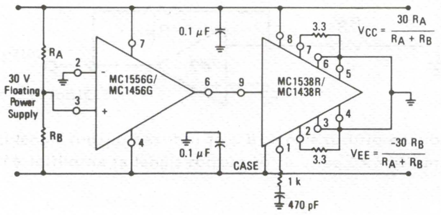
OPERATIONAL AMPLIFIER BOOST CIRCUIT


VCC
RB
RA
VI
0.1 μF
Op-Amp
9
MC1538R/ MC1438R
VO
8
7
6
5
4
3
2
1
0.1 μF
CASE
1 k
470 pF
VEE

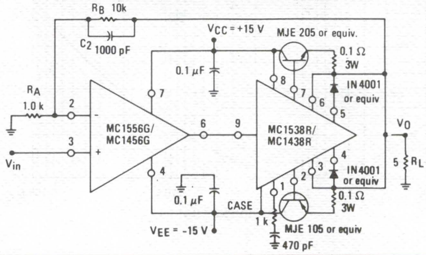
DIGITAL OR ANALOG LINE DRIVER


VCC
0.1 μF
VO ≈ VI
VI
9
MC1438R/ MC1538R
39
zo = 50 Ω
ro
ro = zo = 10 Ω
CASE
0.1 μF
VEE
1 k
470 pF

POWER SUPPLY SPLITTER


RA
2
30 V Floating Power Supply
3
RB
MC1556G/ MC1456G
7
4
0.1 μF
6
9
MC1538R/ MC1438R
3.3
VCC = 30 RA / (RA + RB)
0.1 μF
CASE
3.3
VEE = −30 RB / (RA + RB)
1 k
470 pF

SERVO/POWER AMPLIFIER


RB 10k
C2 1000 pF
VCC = +15 V
MJE 205 or equiv.
0.1 Ω 3W
IN4001 or equiv
RA 1.0 k
0.1 μF
MC1556G/ MC1456G
6
9
MC1538R/ MC1438R
VO
5
RL
Vin
IN4001 or equiv
0.1 Ω 3W
0.1 μF
CASE
VEE = −15 V
1 k
MJE 105 or equiv
470 pF

Under some conditions of circuit layout and loading, the MC1538R/MC1438R will oscillate when driven into current limiting. Oscillation during positive current limiting can usually be suppressed by placing a 0.02 μF capacitor between Pins 7 and 5. Oscillations during negative current limit can usually be suppressed by placing a 0.02 μF capacitor between Pins 1 and 2. 100 Ohms in series with this capacitor will reduce any cross-over distortion occurring when driving extremely low impedance loads.

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	MC1538R	MC1438R	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Voltage Swing	$\|V_{in}\|$	V_{CC} or V_{EE}		Vdc
Load Current	I_L	350		mAdc
Power Dissipation @ T_A = +25°C Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	3.0 24		Watts mW/°C
Power Dissipation @ T_C = +25°C Derate above T_C = +25°C	P_D $1/R_{\theta JC}$	17.5 140		Watts mW/°C
Operating Ambient Temperature Range MC1438R MC1538R	T_A	0 to + 70 -55 to +125		°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	41.6	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.15	°C/W

ELECTRICAL CHARACTERISTICS

(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

				MC1538R			MC1438R			
				5.0 V $\leqslant V_{CC} = \|V_{EE}\| \leqslant$ 20 V			V_{CC} = +15 V, V_{EE} = -15 V			
Characteristic (Linear Operation)	**Fig**	**Note**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Voltage Gain (f = 1.0 kHz)	1	–	A_V	0.9	0.95	1.0	0.85	0.95	1.0	V/V
Current Gain ($A_I = \Delta I_O/\Delta I_I$)	1	–	A_I	–	3000	–	–	3000	–	A/A
Output Impedance (f = 1.0 kHz)	1	–	z_o	–	10	–	–	10	–	Ohms
Input Impedance (f = 1.0 kHz)	1	–	z_i	–	400	–	–	400	–	k ohms
Output Voltage Swing (See Note 3)	1	3	V_O	±12	±13	–	±11	±12	–	Vdc
Input Bias Current	2	–	I_{IB}	–	60	200	–	60	300	µAdc
Output Offset Voltage	2	1	V_{OO}	–	25	150	–	25	200	mVdc
Small Signal Bandwidth (R_L = 300 ohms) (V_I = 0 Vdc, V_I = 100 mV [rms])	1	–	BW	–	8.0	–	–	8.0	–	MHz
Power Bandwidth (See Note 3) (V_O = 20 V_{p-p}, THD = 5%)	1	–	BW_P	–	1.5	–	–	1.5	–	MHz
Total Harmonic Distortion (Note 3) (f = 1.0 kHz, V_O = 20 V_{p-p})	1	–	THD	–	0.5	–	–	0.5	–	%
Output Short-Circuit Current			I_{OS}							mAdc
(R1 = R2 = ∞)	3	2		75	95	125	65	95	140	
(R1 = R2 = 3.3. ohms)	3			–	300	–	–	300	–	
Adjustable Range	4,5			–	5.0 to 300	–	–	5.0 to 300	–	
Power Supply Sensitivity	2	–	PSRR							mV/V
(V_{EE} constant)				–	1.0	–	–	1.0	–	
(V_{CC} constant)				–	1.0	–	–	1.0	–	
Power Supply Current (R_L ∞, V_I = 0)	2	3	I_{CC} I_{EE}	4.5	6.0	10	2.5	6.0	15	mAdc
Power Dissipation (See Note 3) (R_L ∞, V_I = 0)	2	3	P_C	150	180	300	75	180	450	mW

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.

Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R1, R2, R3 and R4. The positive current limit is set by R1 or R3, and the negative current limit is set by R2 or R4. See Figures 4 and 5 for curves of short-circuit current versus R1, R2, R3 and R4.

Note 3. V_{CC} = +15 V, V_{EE} = -15 V.

TEST CIRCUITS

FIGURE 1

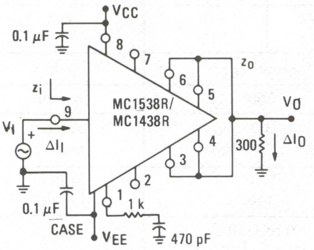

VCC
0.1 µF
8
7
6
5
4
3
2
1
zo
zi
MC1538R/
MC1438R
9
VI
+
ΔII
VO
300
ΔIO
0.1 µF
CASE
VEE
1 k
470 pF

FIGURE 2

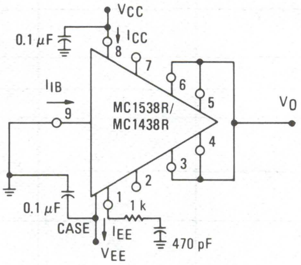
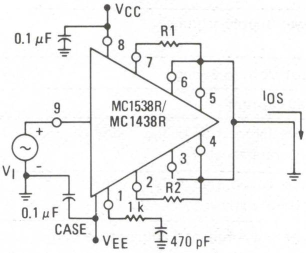
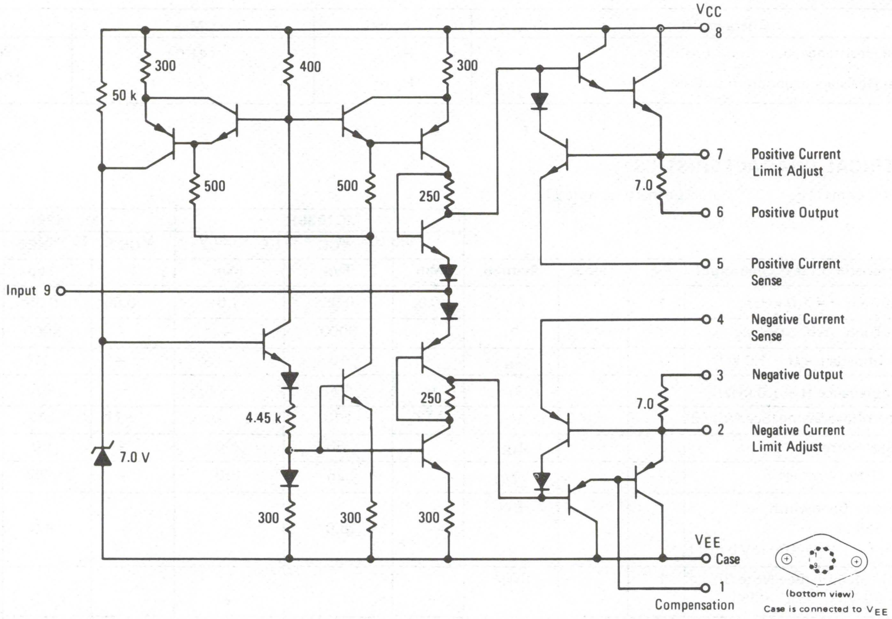

VCC
0.1 µF
ICC
8
7
6
5
4
3
2
1
IIB
9
MC1538R/
MC1438R
VO
0.1 µF
CASE
IEE
VEE
1 k
470 pF

FIGURE 3


VCC
0.1 µF
8
R1
7
6
5
9
+
MC1538R/
MC1438R
IOS
4
3
2
R2
VI
-
0.1 µF
CASE
1
1 k
VEE
470 pF

CIRCUIT SCHEMATIC


VCC
8
300
400
300
50 k
500
500
250
7.0
7
Positive Current Limit Adjust
6
Positive Output
5
Positive Current Sense
Input 9
4
Negative Current Sense
3
Negative Output
250
4.45 k
7.0
2
Negative Current Limit Adjust
7.0 V
300
300
300
VEE
Case
1
Compensation
(bottom view)
Case is connected to VEE

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – SHORT-CIRCUIT CURRENT versus R1 OR R2
(100 mA to 300 mA)

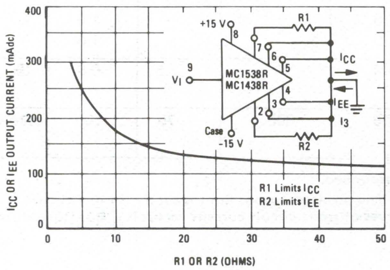
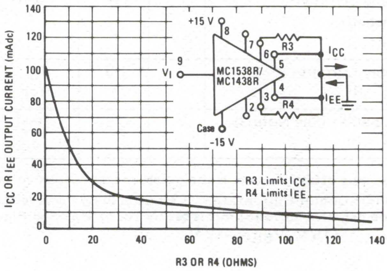


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R3 OR R4
(5.0 mA to 100 mA)



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – POWER SUPPLY CURRENT versus SHUNT RESISTANCE

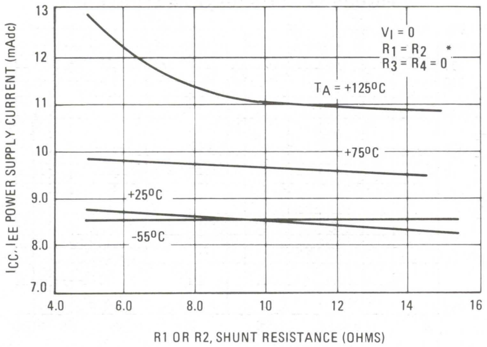


FIGURE 7 – SMALL SIGNAL GAIN AND PHASE RESPONSE

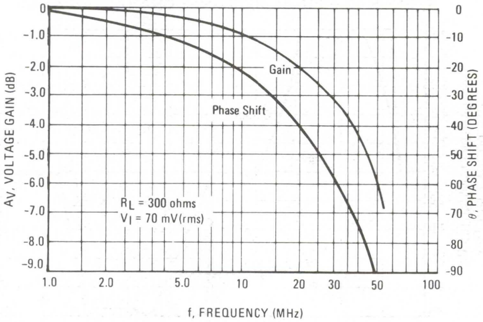


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

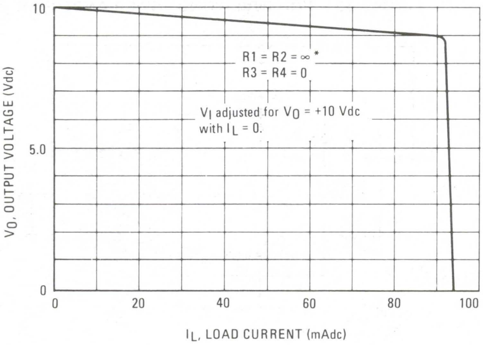


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

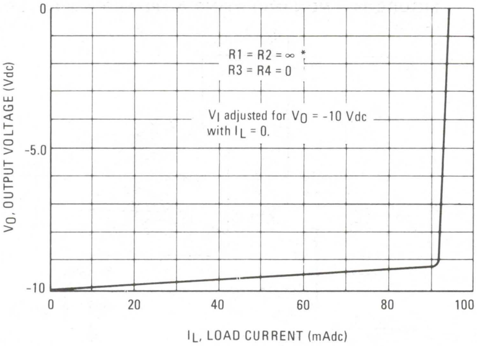


FIGURE 10 – OUTPUT OFFSET VOLTAGE versus TEMPERATURE

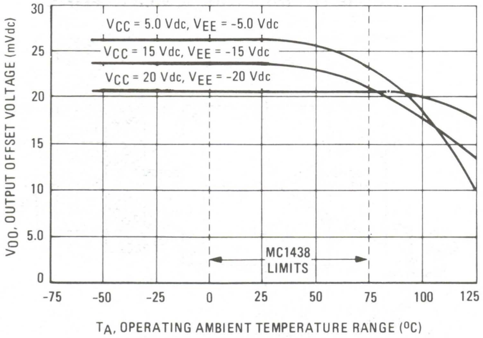
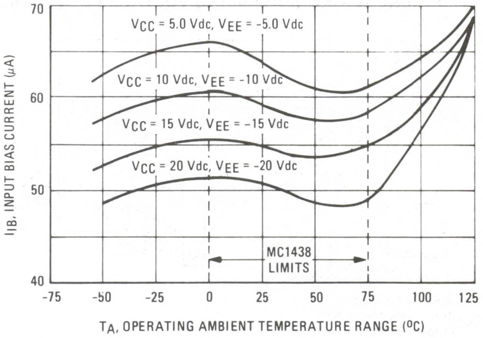


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



*See Figures 4 and 5 for definition of R1, R2, R3, and R4.

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 12 – PULSE RESPONSE CHARACTERISTICS

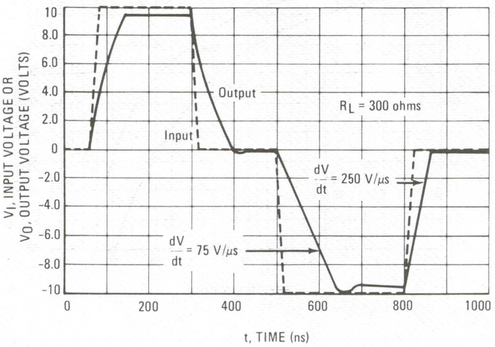
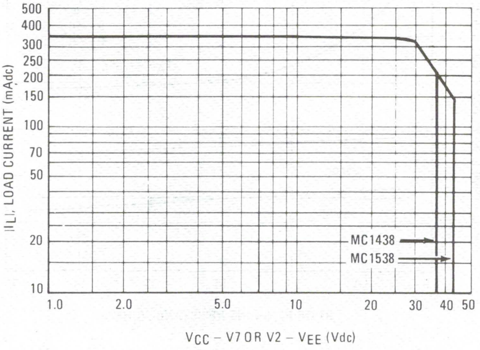
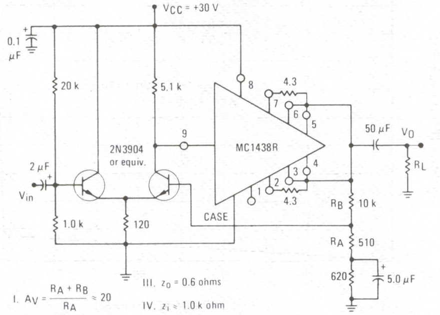


FIGURE 13 – DC SAFE OPERATING AREA



TYPICAL APPLICATIONS

FIGURE 14 – NON-INVERTING AC POWER AMPLIFIER



V_{CC} = +30 V
0.1 μF
20 k
5.1 k
8
4.3
7
6
5
9
MC1438R
2N3904 or equiv.
2 μF
V_{in}
50 μF
V_O
R_L
3
4
2
1
4.3
CASE
R_B
10 k
1.0 k
120
R_A
510
620
5.0 μF

I. $A_V = \frac{R_A + R_B}{R_A} \approx 20$

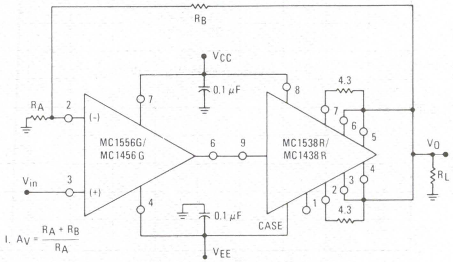
II. I_{OS} = 200 mA

III. z_0 = 0.6 ohms

IV. $z_i \approx$ 1.0 k ohm

V. BW_p = 1.0 MHz

FIGURE 15 – NON-INVERTING POWER AMPLIFIER



R_B
V_{CC}
0.1 μF
R_A
2
(-)
7
8
4.3
MC1556G/ MC1456G
6
9
MC1538R/ MC1438R
7
6
5
4
3
2
1
4.3
V_O
R_L
V_{in}
3
(+)
4
0.1 μF
CASE
V_{EE}

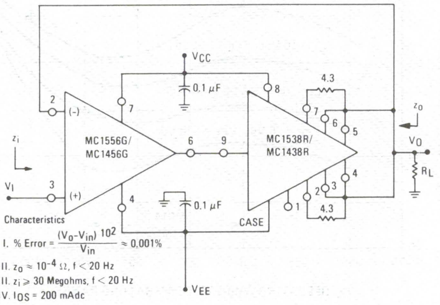
I. $A_V = \frac{R_A + R_B}{R_A}$

II. $z_0 \approx \frac{R_A + R_B}{R_A} 10^{-4} \Omega$

III. $z_i \geqslant$ 30 megohm for f < 20 Hz

IV. I_{OS} = 200 mA

FIGURE 16 – NON-INVERTING VOLTAGE FOLLOWER



V_{CC}
0.1 μF
2
(-)
7
8
4.3
7
6
5
z_0
z_i
MC1556G/ MC1456G
6
9
MC1538R/ MC1438R
V_O
R_L
V_I
3
(+)
4
0.1 μF
2
3
4
1
4.3
CASE
V_{EE}

Characteristics

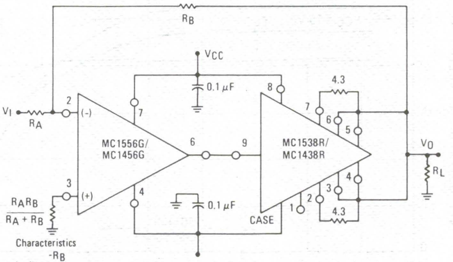
I. % Error = $\frac{(V_o - V_{in})\ 10^2}{V_{in}} \approx$ 0.001%

II. $z_0 \approx 10^{-4}$ Ω, f < 20 Hz

III. $z_i \geqslant$ 30 Megohms, f < 20 Hz

IV. I_{OS} = 200 mAdc

FIGURE 17 – INVERTING POWER AMPLIFIER



R_B
V_{CC}
0.1 μF
8
4.3
V_I
R_A
2
(-)
7
7
6
5
MC1556G/ MC1456G
6
9
MC1538R/ MC1438R
V_O
R_L
3
(+)
$\frac{R_A R_B}{R_A + R_B}$
4
0.1 μF
1
2
3
4
4.3
CASE

Characteristics

I. $A_V = \frac{-R_B}{R_A}$

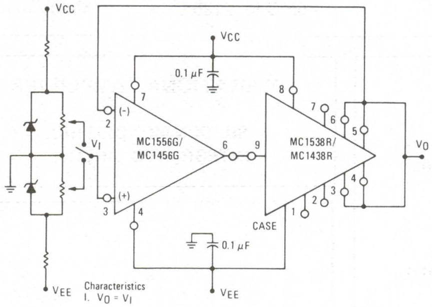
II. $z_0 \approx \frac{R_A + R_B}{R_A} 10^{-4} \Omega$

III. $z_i \approx R_A$

IV. $I_{OS} \approx$ 200 mA

TYPICAL APPLICATIONS (continued)

FIGURE 18 – PROGRAMMABLE VOLTAGE SOURCE

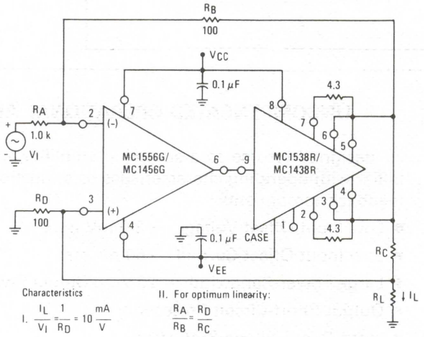

VCC
VCC
0.1 µF
(-)
2
7
8
7
6
5
VI
MC1556G/
MC1456G
6
9
MC1538R/
MC1438R
VO
(+)
3
4
4
3
2
1
CASE
0.1 µF
VEE
VEE

Characteristics

I. $V_O = V_I$

II. $z_O << 1.0$ milli-ohm, f = 20 Hz

FIGURE 19 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER


RB
100
VCC
0.1 µF
4.3
RA
1.0 k
2
(-)
7
8
7
6
5
VI
MC1556G/
MC1456G
6
9
MC1538R/
MC1438R
RD
100
3
(+)
4
4
3
2
1
4.3
0.1 µF
CASE
VEE
RC
RL
IL

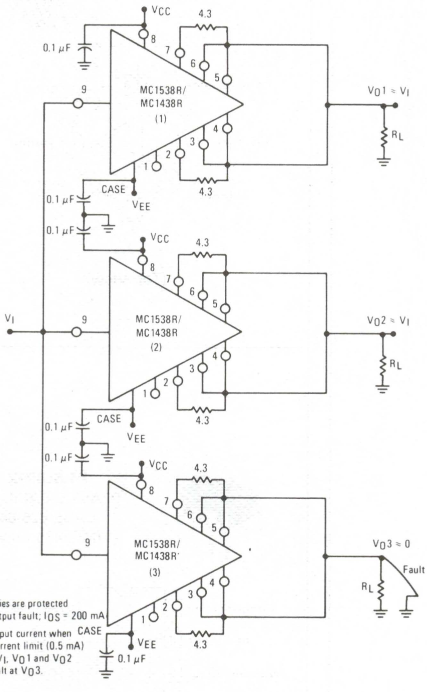
Characteristics

I. $\frac{I_L}{V_I} = \frac{1}{R_D} = 10 \frac{mA}{V}$

II. For optimum linearity:

$\frac{R_A}{R_B} = \frac{R_D}{R_C}$

FIGURE 20 – SIGNAL DISTRIBUTION

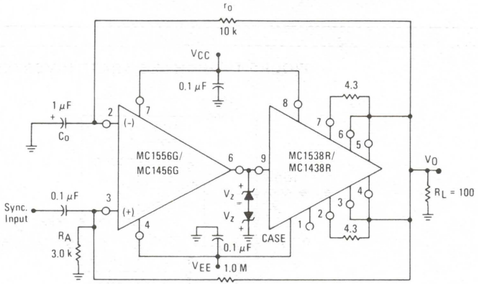

VCC
4.3
0.1 µF
8
7
6
5
9
MC1538R/
MC1438R
(1)
VO1 ≈ VI
RL
4
3
2
1
4.3
CASE
VEE
0.1 µF
0.1 µF
VCC
4.3
VI
9
MC1538R/
MC1438R
(2)
VO2 ≈ VI
RL
4.3
CASE
VEE
0.1 µF
0.1 µF
VCC
4.3
9
MC1538R/
MC1438R
(3)
VO3 ≈ 0
Fault
RL
CASE
VEE
0.1 µF
4.3

Characteristics

I. Power supplies are protected from the output fault; I_{OS} = 200 mA

II. The small input current when in output current limit (0.5 mA) will isolate V_I, V_O1 and V_O2 from the fault at V_O3.

FIGURE 21 – ASTABLE MULTIVIBRATOR


ro
10 k
VCC
0.1 µF
4.3
1 µF
Co
2
(-)
7
8
MC1556G/
MC1456G
6
9
MC1538R/
MC1438R
VO
RL = 100
Sync. Input
0.1 µF
3
(+)
Vz
Vz
RA
3.0 k
4
0.1 µF
CASE
4.3
VEE
1.0 M
RB

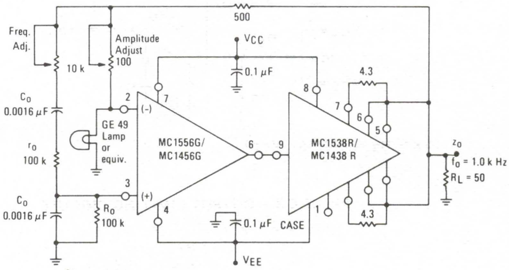
Characteristics

I. $f_O = \frac{1}{2\ r_O C_O\ \ln(1 + \frac{2R_A}{R_B})}$

II. I_{OS} = 200 mA

III. $V_{O(pk)}$ = ± $(V_z + 0.7)$ Volts

FIGURE 22 – WIEN BRIDGE OSCILLATOR


500
Freq. Adj.
Amplitude Adjust
100
10 k
VCC
0.1 µF
4.3
Co
0.0016 µF
2
(-)
GE 49 Lamp or equiv.
ro
100 k
MC1556G/
MC1456G
6
9
MC1538R/
MC1438 R
zo
fo = 1.0 k Hz
RL = 50
Co
0.0016 µF
3
(+)
Ro
100 k
4
0.1 µF
CASE
4.3
VEE

Characteristics

I. $f_O = \frac{1}{2\pi r_O C_O}$ from 0.01 Hz to 10 kHz

II. I_{OS} = 200 mA

MC1439
MC1539

ORDERING INFORMATION

Device	Temperature Range	Package
MC1439G	0°C to +70°C	Metal Can
MC1439P1	0°C to +70°C	Plastic DIP
MC1539G	−55°C to +125°C	Metal Can

UNCOMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Offset Voltage — 3.0 mV max
- Low Input Offset Current — 60 nA max
- Large Power-Bandwidth — 20 Vp-p Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate — 34 V/μs typ

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – HIGH SLEW-RATE INVERTER

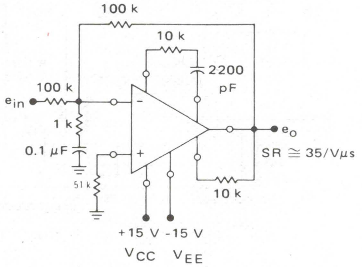
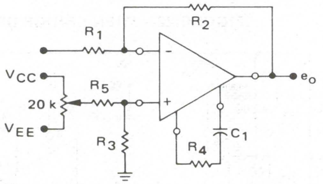
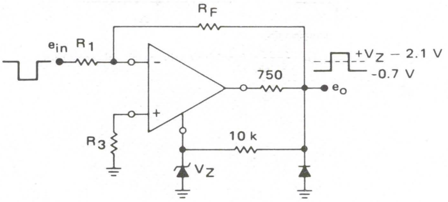

100 k
10 k
2200 pF
100 k
e_in
1 k
0.1 μF
51 k
e_O
SR ≅ 35/V μs
10 k
+15 V -15 V
VCC VEE

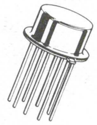
FIGURE 2 – OUTPUT NULLING CIRCUIT


R1
R2
VCC
R5
20 k
VEE
R3
R4
C1
e_O

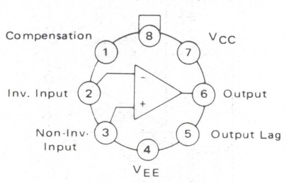
$10\text{ k} \leqslant R_S \leqslant 100(R_3)\,(V_{CC})$

FIGURE 3 – OUTPUT LIMITING CIRCUIT

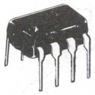

RF
e_in R1
750
+VZ − 2.1 V
-0.7 V
e_O
R3
10 k
VZ



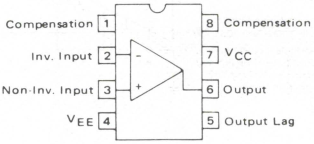
G SUFFIX
METAL PACKAGE
CASE 601-04


Compensation
Compensation
VCC
Inv. Input
Output
Non-Inv. Input
Output Lag
VEE
1
2
3
4
5
6
7
8

(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1439 only)


Compensation 1
Inv. Input 2
Non-Inv. Input 3
VEE 4
8 Compensation
7 VCC
6 Output
5 Output Lag

(Top View)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

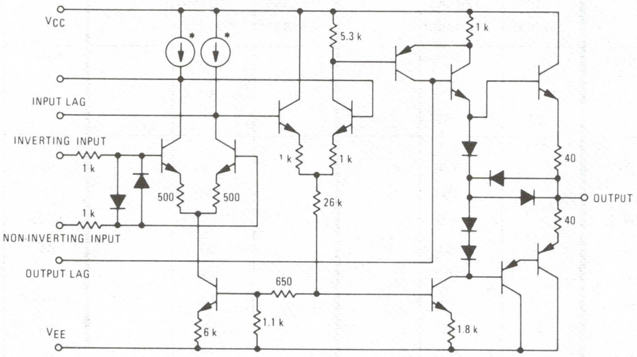
Characteristic	Symbol	MC1539			MC1439			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\|I_{IO}\|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\|V_{IO}\|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TCV_{IO}\|$							μV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
(R_S ≤ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Range	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{VOL}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_V = 1, THD ≤ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ, R_5 = 10 k)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot,	t_{THL}	–	130	–	–	130	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	190	–	–	190	–	ns
R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	SR	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot,	t_{THL}	–	80	–	–	80	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 0, R5 = 10 kΩ, C1 = 10 pF	SR	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot,	t_{THL}	–	60	–	–	60	–	ns
R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	SR	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot,	t_{THL}	–	120	–	–	120	–	ns
R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	SR	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot,	t_{THL}	–	160	–	–	160	–	ns
R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	SR	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_O							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Rejection Ratio (V_{EE} constant, R_5 = ∞)	PSRR+	–	50	150	–	50	200	μV/V
Negative Supply Rejection Ratio (V_{CC} constant, R_5 = ∞)	PSRR−	–	50	150	–	50	200	μV/V
Power Supply Current (V_O = 0)	I_{CC}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{EE}	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439 / −55°C for MC1539; T_{high} = +70°C for MC1439 / +125°C for MC1539

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

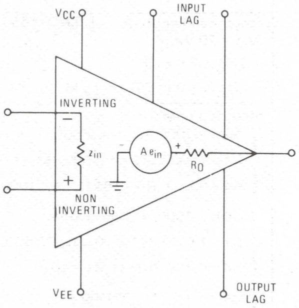
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm(V_{CC} + \lvert V_{EE}\rvert)$	Vdc
Common-Mode Input Voltage Range	V_{ICR}	$+V_{CC}, -\lvert V_{EE}\rvert$	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Packages MC1439		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}		°C
Metal Packages		-65 to +150	
Plastic Packages		-55 to +125	

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC



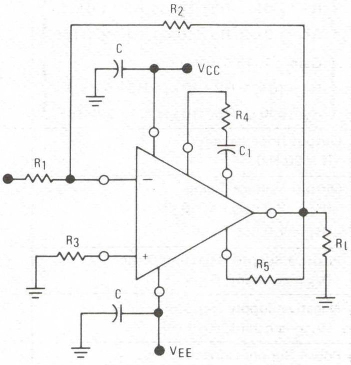
VCC
*
*
5.3 k
1 k
INPUT LAG
INVERTING INPUT
1 k
1 k
1 k
1 k
500
500
26 k
40
OUTPUT
40
NON-INVERTING INPUT
OUTPUT LAG
650
1.1 k
6 k
1.8 k
VEE

FIGURE 5 – EQUIVALENT CIRCUIT



VCC
INPUT LAG
INVERTING
−
zin
Aein
+
RO
+
NON INVERTING
VEE
OUTPUT LAG

FIGURE 6 – TEST CIRCUIT



R2
C
VCC
R4
C1
R1
−
R3
+
RL
R5
C
VEE

TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6) R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	C1 (pF)
7,10,12	1	A_{vol}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	5.0 k	390	10 k	2200
	3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
	4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
	5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
	6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10
8	1	A_{vol}	0	∞	0	∞	∞	0
	2	↓	↓	↓	↓	390	↓	2200
	3	↓	↓	↓	↓	1.0 k	↓	2200
	4	↓	↓	↓	↓	10 k	↓	2200
	5	↓	↓	↓	↓	30 k	↓	1000
	6	↓	↓	↓	↓	0	↓	10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 7 – LARGE-SIGNAL SWING versus FREQUENCY

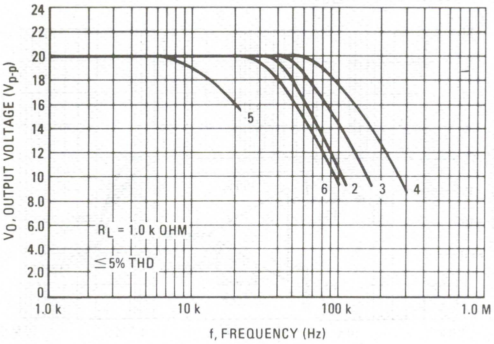


FIGURE 8 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

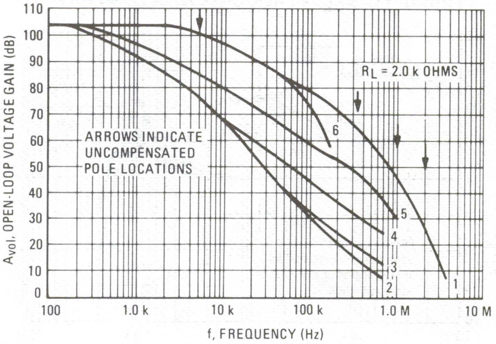


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

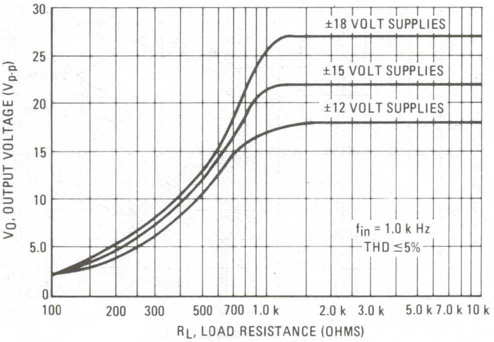


FIGURE 10 – OPEN-LOOP PHASE-SHIFT versus FREQUENCY

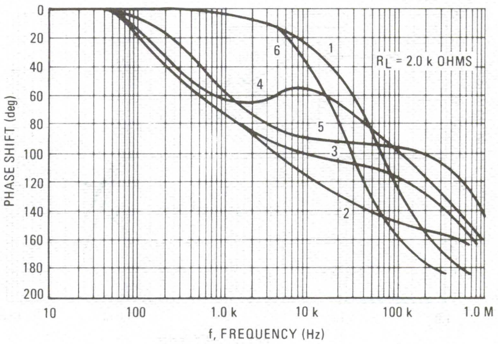


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

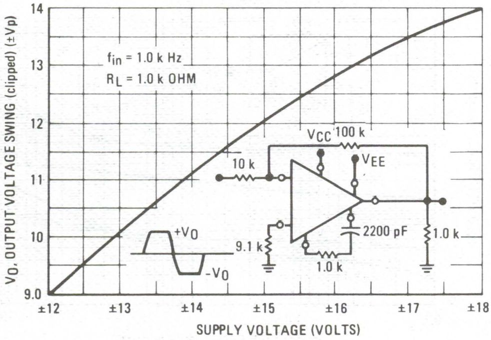
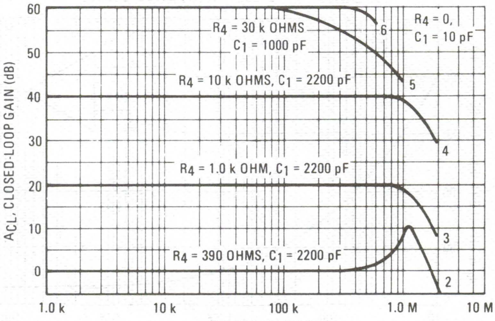


FIGURE 12 – CLOSED-LOOP GAIN versus FREQUENCY



* A_{CL} = Closed-Loop Gain

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

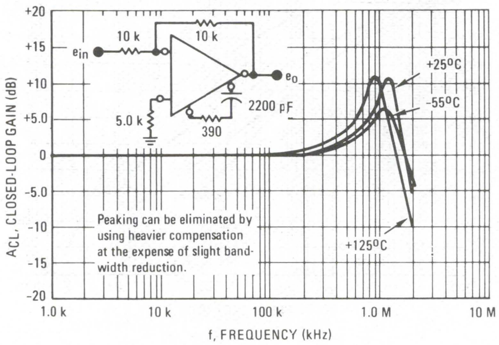


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

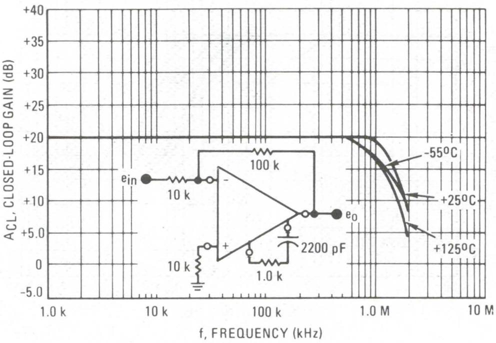


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

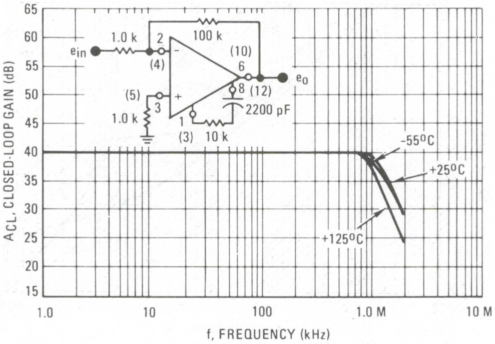


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

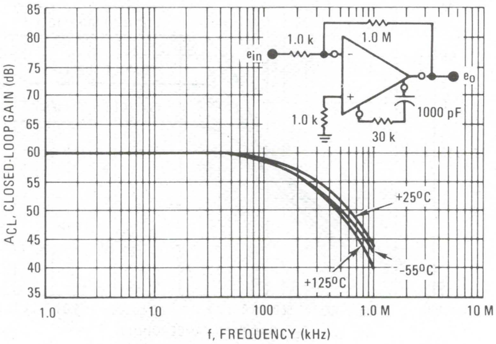


FIGURE 17 – SPECTRAL NOISE DENSITY

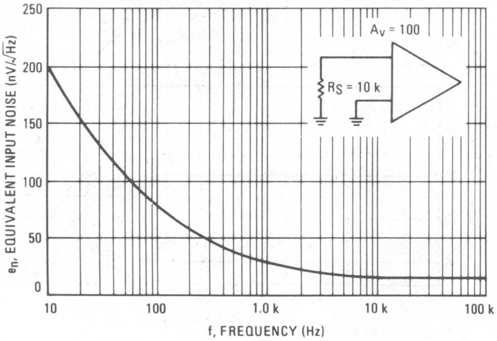
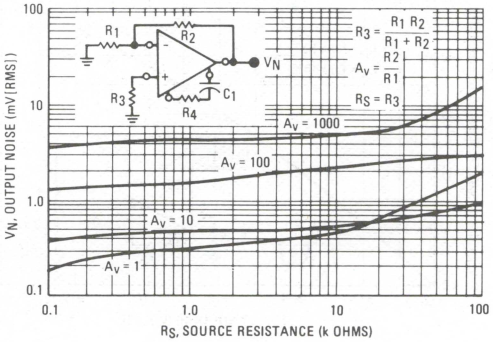


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*A_{CL} = Closed-Loop Gain

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

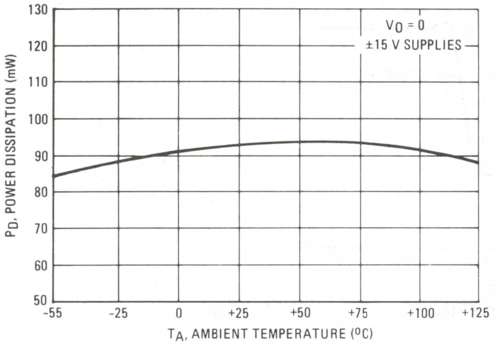


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

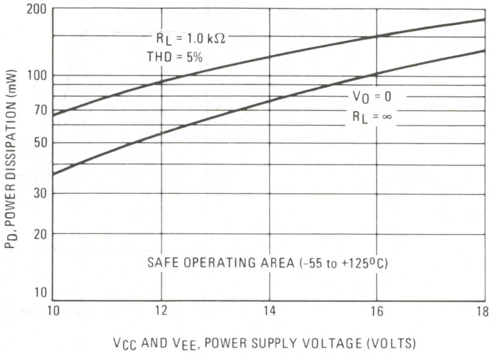


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

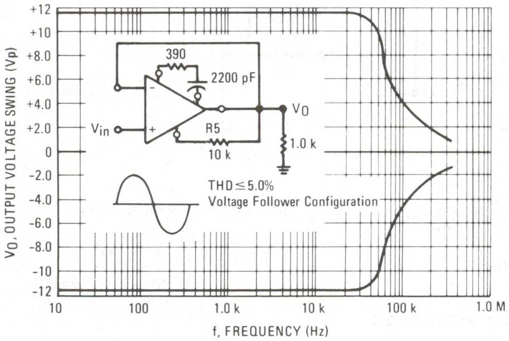


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

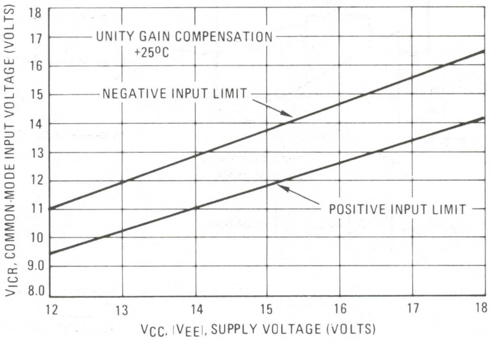


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

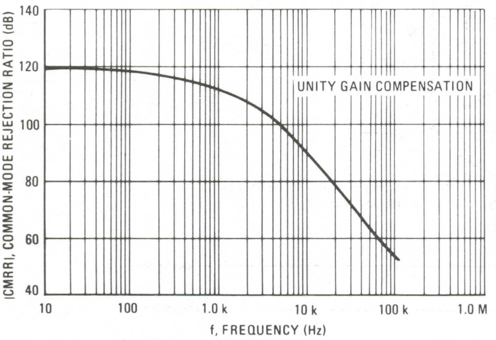


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE

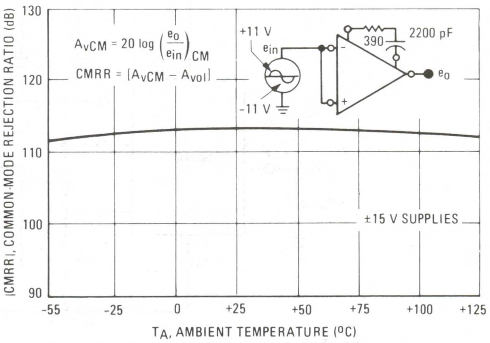
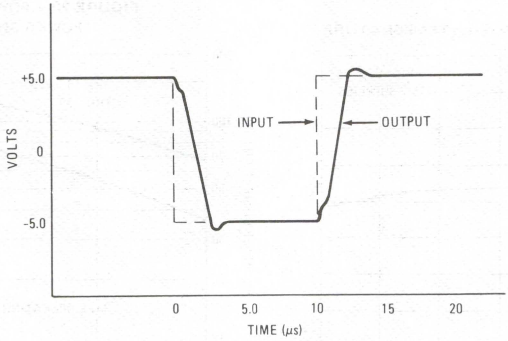
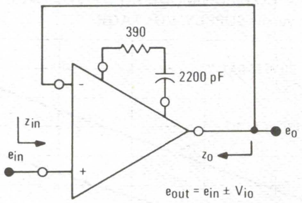


FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 26 – VOLTAGE FOLLOWER

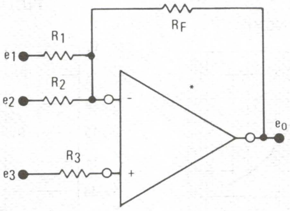

390
2200 pF
-
+
zin
ein
zo
eo

$e_{out} = e_{in} \pm V_{io}$

$z_{in} > 40$ M OHMS

$$z_{oCL} = z_{oOL}\left[\frac{1+\frac{R_F}{R_i}}{A_{ol}}\right] = 4\text{ k}\left[\frac{1+0}{10^5}\right] \approx 0.04 \text{ OHM}$$

FIGURE 27 – DIFFERENTIAL AMPLIFIER

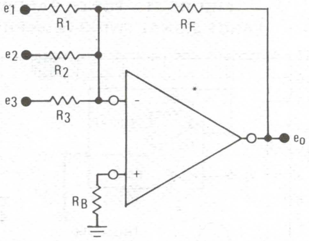

RF
R1
e1
R2
e2
R3
e3
-
+
*
eo

$$e_o = -\left|\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2\right| + \left|1+\frac{R_F}{R_3}\right| e3$$

For $R_3 = \frac{R_1, R_2}{R_1 + R_2}$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

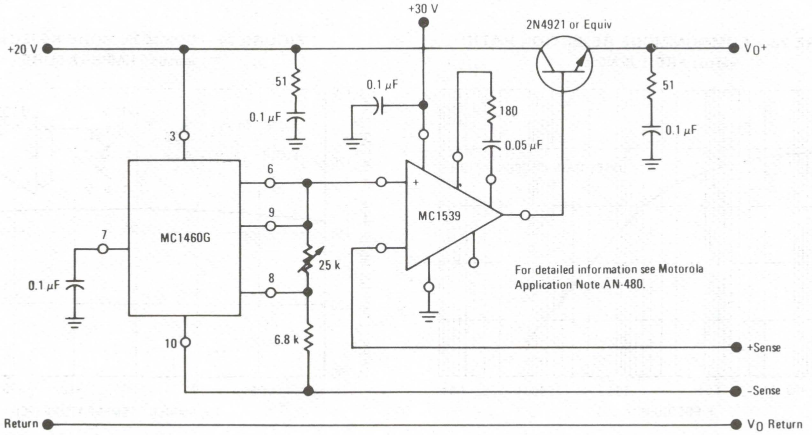

e1
R1
RF
e2
R2
e3
R3
-
+
*
RB
eo

R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$$e_o = -\left|\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2 + \frac{R_F}{R_3}e3\right|$$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR


+30 V
2N4921 or Equiv
+20 V
Vo+
51
0.1 µF
0.1 µF
180
0.05 µF
51
0.1 µF
3
6
9
8
7
10
0.1 µF
MC1460G
MC1539
+
25 k
6.8 k
+Sense
-Sense
Return
Vo Return

For detailed information see Motorola Application Note AN-480.

TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

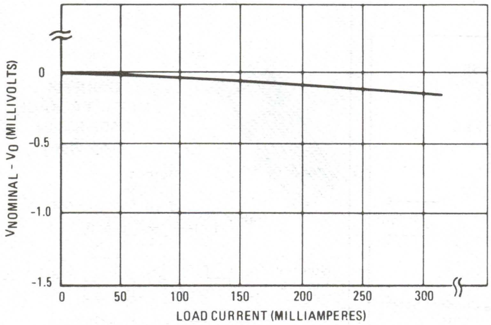
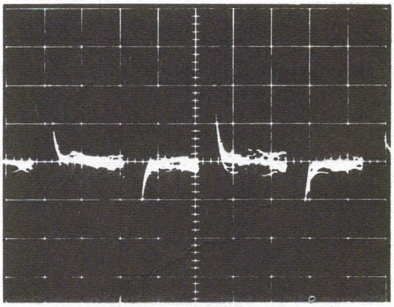


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



Horizontal Scale: 200 µs/Div
Vertical Scale: 1 mV/Div

MC1445
MC1545

ORDERING INFORMATION

Device	Temperature Range	Package
MC1445G	0°C to +75°C	Metal Can
MC1445L	0°C to +75°C	Ceramic DIP
MC1545G	−55°C to +125°C	Metal Can
MC1545L	−55°C to +125°C	Ceramic DIP

3

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN491 for design details.

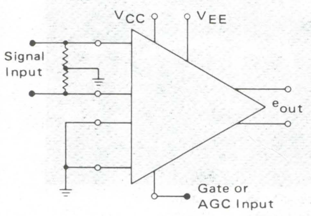
- Large Bandwidth; 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

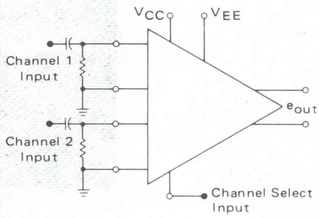
SILICON MONOLITHIC INTEGRATED CIRCUIT

TYPICAL APPLICATIONS

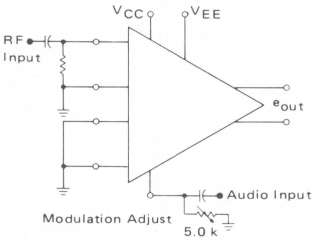
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC


VCC
VEE
Signal Input
eout
Gate or AGC Input

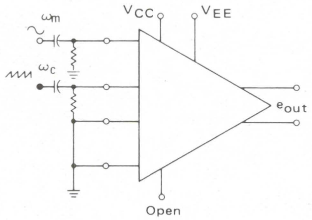
MULTIPLEX OR FSK


VCC
VEE
Channel 1 Input
Channel 2 Input
eout
Channel Select Input

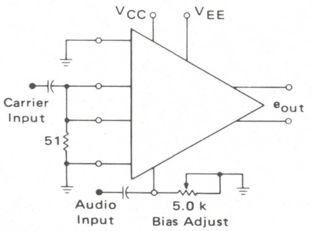
AMPLITUDE MODULATOR


VCC
VEE
RF Input
eout
Audio Input
Modulation Adjust
5.0 k

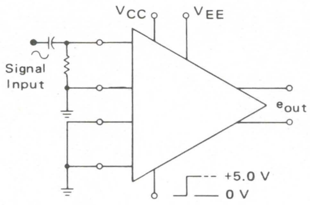
PULSE-WIDTH MODULATOR

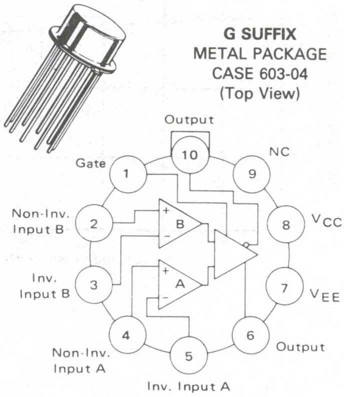

ωm
VCC
VEE
ωc
eout
Open

BALANCED MODULATOR

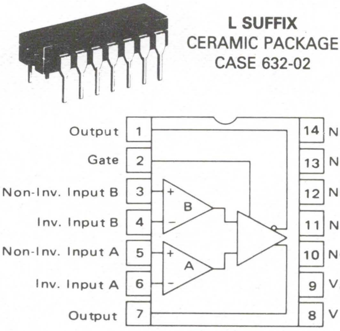

VCC
VEE
Carrier Input
51
eout
Audio Input
5.0 k
Bias Adjust

ANALOG SWITCH


VCC
VEE
Signal Input
eout
+5.0 V
0 V


Output
10
NC
9
Gate
1
Non-Inv. Input B
2
B
8
VCC
Inv. Input B
3
A
7
VEE
4
5
6
Output
Non-Inv. Input A
Inv. Input A

G SUFFIX
METAL PACKAGE
CASE 603-04
(Top View)


Output 1
Gate 2
Non-Inv. Input B 3
Inv. Input B 4
Non-Inv. Input A 5
Inv. Input A 6
Output 7
B
A
14 NC
13 NC
12 NC
11 NC
10 NC
9 VCC
8 VEE

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Ceramic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Ambient Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = 5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted.)

Characteristic	Fig. No.	Symbol	MC1545			MC1445			Unit
			Min	Typ	Max	Min	Typ	Max	
Single-Ended Voltage Gain	1,12	A_{vs}	16	19	21	16	19.5	23	dB
Bandwidth	1,12	BW	40	50	–	–	50	–	MHz
Input Impedance (f = 50 kHz)	5,14	z_i	4.0	10	–	3.0	10	–	k ohms
Output Impedance (f = 50 kHz)	6,15	z_o	–	25	–	–	25	–	Ohms
Output Differential Voltage Range (R_L = 1.0 k ohm, f = 50 kHz)	4,13	V_{ODR}	1.5	2.5	–	1.5	2.5	–	Vp-p
Input Bias Current	16	I_{IB}	–	15	25	–	15	30	μAdc
Input Offset Current	16	I_{IO}	–	2.0	–	–	2.0	–	μAdc
Input Offset Voltage	17	V_{IO}	–	1.0	5.0	–	–	7.5	mVdc
Quiescent Output dc Level	17	V_O	–	0.1	–	–	0.1	–	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV_O	–	±15	–	–	±15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9,18	CMRR	–	85	–	–	85	–	dB
Input Common-Mode Voltage Range	18	V_{ICR}	–	±2.5	–	–	±2.5	–	Vp
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1)	8	$V_{IL(G)}$	0.40	0.70	–	0.2	0.4	–	Vdc
Gate Input Voltage – High Logic State (Note 2)		$V_{IH(G)}$	–	1.5	2.2	–	1.3	3.0	
Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V)	18	$I_{IL(G)}$	–	–	2.5	–	–	4.0	mA
Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V)	18	$I_{IH(G)}$	–	–	2.0	–	–	4.0	μA
Step Response (e_{in} = 20 mV)	19	t_{PLH}	–	6.5	10	–	6.5	–	ns
		t_{PHL}	–	6.3	10	–	6.3	–	
		t_{TLH}	–	6.5	15	–	6.5	–	
		t_{THL}	–	7.0	15	–	7.0	–	
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)	10,20	e_n	–	25	–	–	25	–	μV(rms)
DC Power Consumption	11,20	P_C	–	70	110	–	70	150	mW

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.

Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

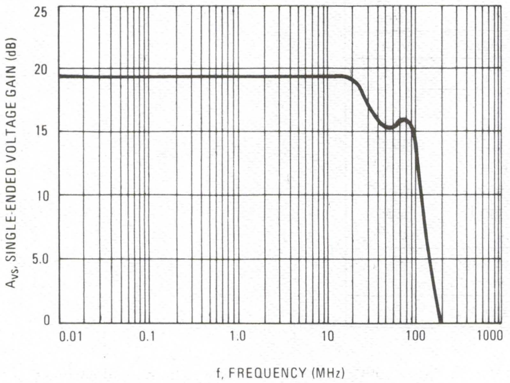


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

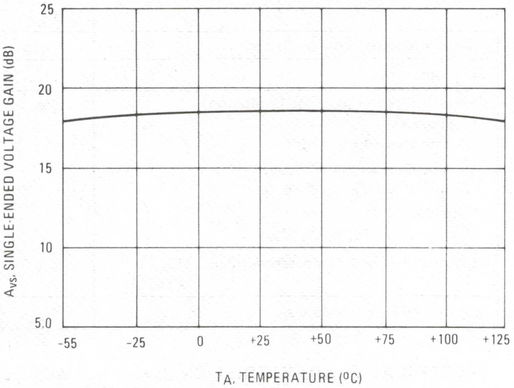


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

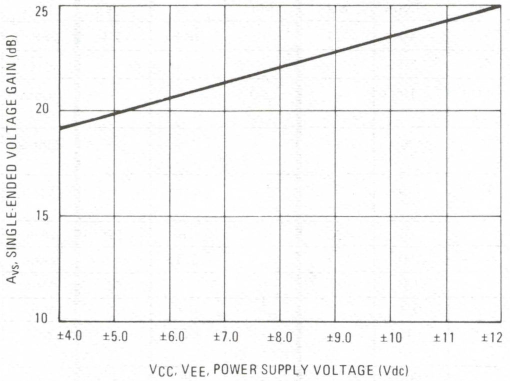


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

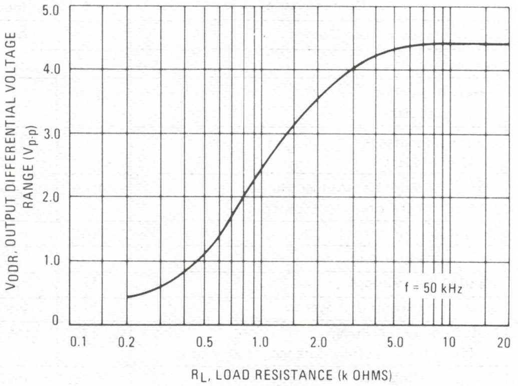


FIGURE 5 – INPUT Cp AND Rp versus FREQUENCY (BOTH CHANNELS)

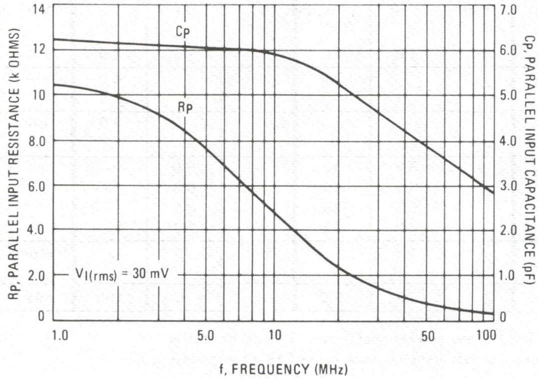


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

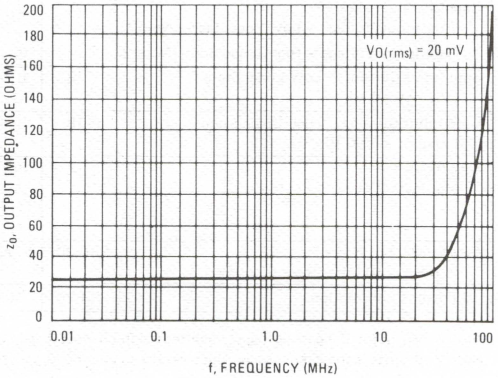


FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

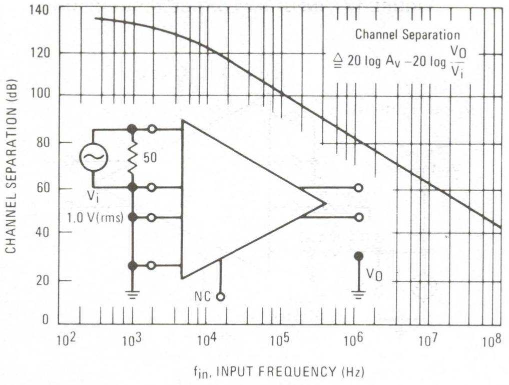


FIGURE 8 – GATE CHARACTERISTICS

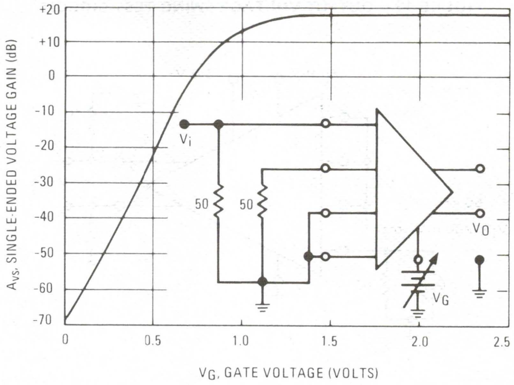


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

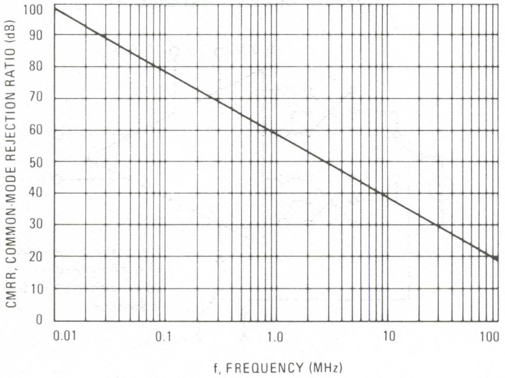


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

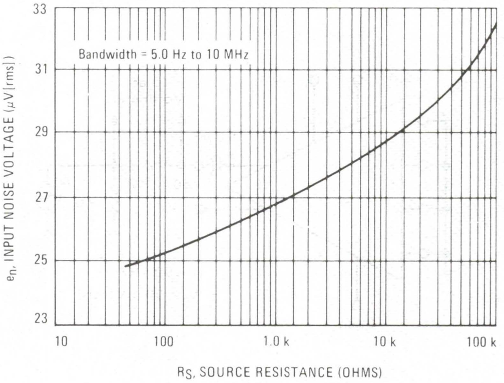


FIGURE 11 – CIRCUIT SCHEMATIC

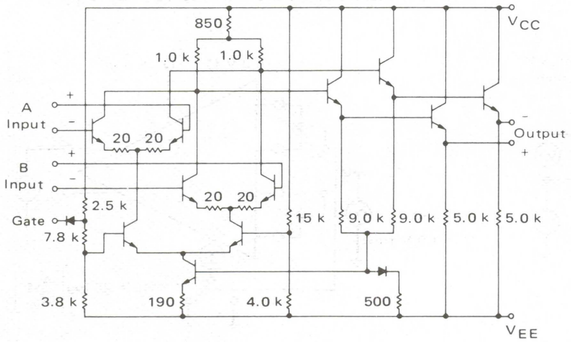
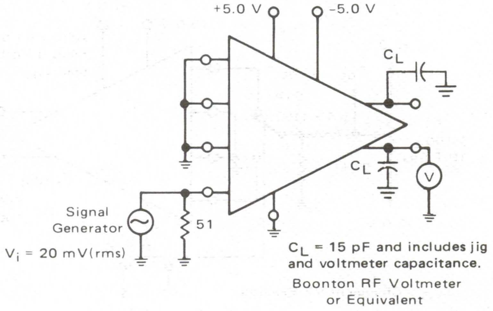

V_{CC}
850
1.0 k
1.0 k
A Input
+
–
20
20
B Input
+
–
20
20
2.5 k
Gate
7.8 k
15 k
9.0 k
9.0 k
5.0 k
5.0 k
Output
–
+
3.8 k
190
4.0 k
500
V_{EE}

FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT


+5.0 V
-5.0 V
C_L
C_L
V
Signal Generator
51
V_i = 20 mV(rms)

C_L = 15 pF and includes jig and voltmeter capacitance.

Boonton RF Voltmeter or Equivalent

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

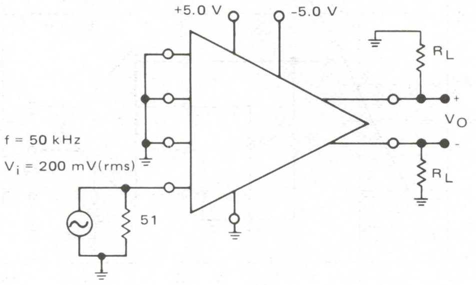

+5.0 V
-5.0 V
R_L
+
V_O
-
R_L
f = 50 kHz
V_i = 200 mV(rms)
51

FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

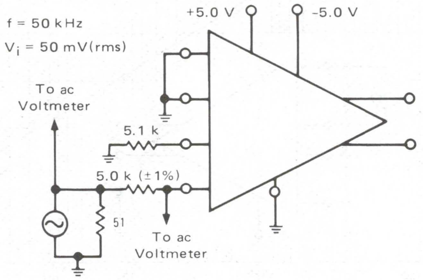

f = 50 kHz
V_i = 50 mV(rms)
+5.0 V
-5.0 V
To ac Voltmeter
5.1 k
5.0 k (±1%)
51
To ac Voltmeter

FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

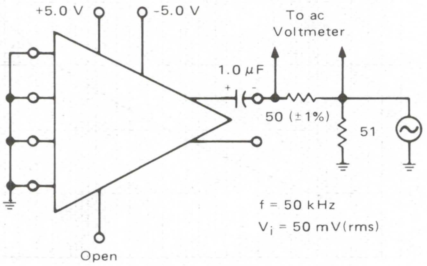
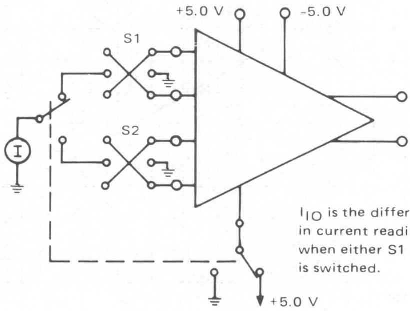
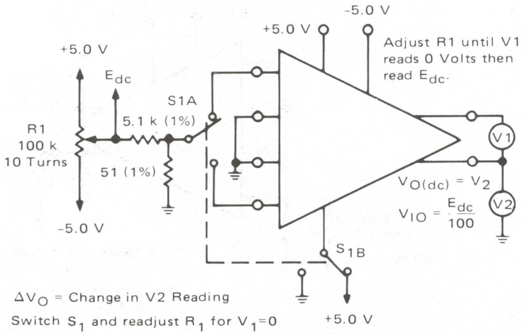

+5.0 V
-5.0 V
To ac Voltmeter
1.0 μF
+
-
50 (±1%)
51
f = 50 kHz
V_i = 50 mV(rms)
Open

FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT


+5.0 V
-5.0 V
S1
S2
I
+5.0 V

I_{IO} is the difference in current reading when either S1 or S2 is switched.

FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT


-5.0 V
+5.0 V
+5.0 V
E_dc
S1A
R1
100 k
10 Turns
5.1 k (1%)
51 (1%)
-5.0 V
V1
V2
S_1B
+5.0 V

Adjust R1 until V1 reads 0 Volts then read E_{dc}.

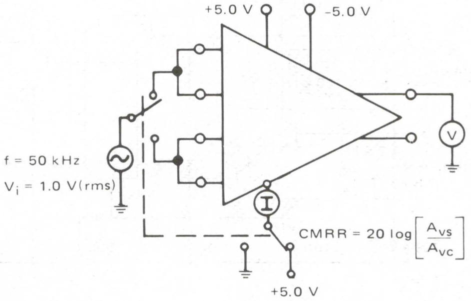
$V_{O(dc)} = V_2$

$V_{IO} = \frac{E_{dc}}{100}$

ΔV_O = Change in V2 Reading

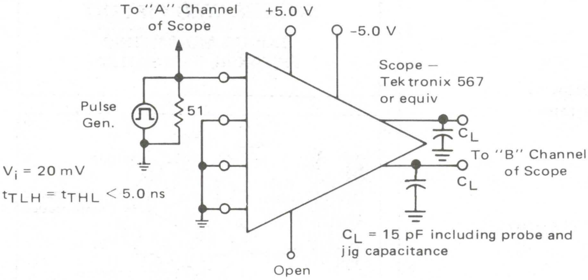
Switch S_1 and readjust R_1 for $V_1 = 0$

FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT


+5.0 V
-5.0 V
V
I
f = 50 kHz
V_i = 1.0 V(rms)
+5.0 V

$$\text{CMRR} = 20 \log \left[\frac{A_{vs}}{A_{vc}}\right]$$

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT


To "A" Channel of Scope
+5.0 V
-5.0 V
Scope – Tektronix 567 or equiv
Pulse Gen.
51
C_L
To "B" Channel of Scope
C_L
V_i = 20 mV
$t_{TLH} = t_{THL} < 5.0$ ns
C_L = 15 pF including probe and jig capacitance
Open

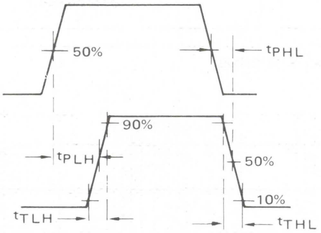

50%
t_{PHL}
90%
t_{PLH}
50%
10%
t_{TLH}
t_{THL}

FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

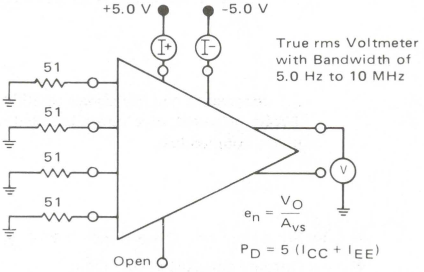
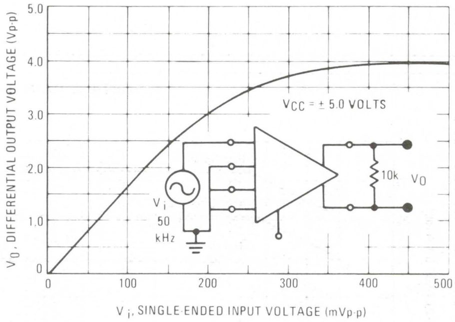

+5.0 V
-5.0 V
I+
I−
True rms Voltmeter with Bandwidth of 5.0 Hz to 10 MHz
51
51
51
51
V
$e_n = \frac{V_O}{A_{vs}}$
$P_D = 5 (I_{CC} + I_{EE})$
Open

FIGURE 21 – LIMITING CHARACTERISTIC



MC1454G
MC1554G

ORDERING INFORMATION

Device	Temperature Range	Package
MC1454G	0°C to +70°C	Metal Can
MC1554G	−55°C to +125°C	Metal Can

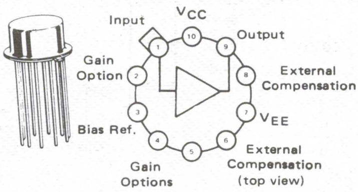
1-WATT POWER AMPLIFIERS

. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion — 0.4% (Typ) @ 1 Watt
- Low Output Impedance — 0.2 Ohm
- Excellent Gain — Temperature Stability

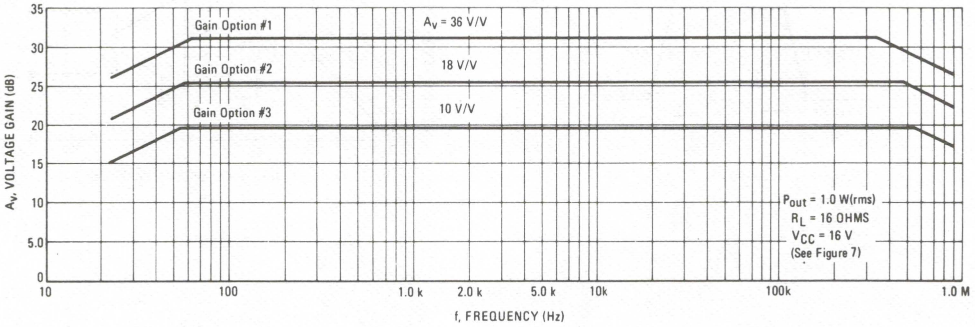
1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED

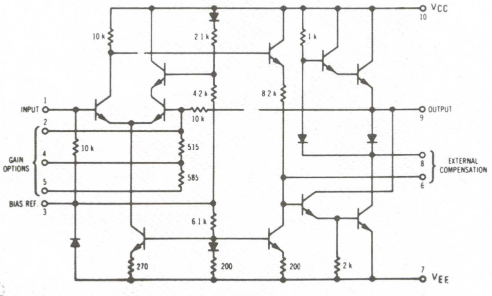

Input
V_{CC}
10
Output
9
1
Gain Option
2
8
External Compensation
3
7
V_{EE}
Bias Ref.
4
5
6
External Compensation
Gain Options
(top view)

G SUFFIX
CASE 603B-01

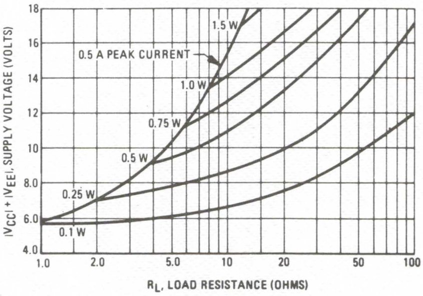
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC


V_{CC}
10
10 k
2 1 k
1 k
4 2 k
8 2 k
INPUT
1
10 k
OUTPUT
9
2
GAIN OPTIONS
4
5
10 k
515
585
EXTERNAL COMPENSATION
8
6
BIAS REF.
3
6 1 k
270
200
200
2 k
7
V_{EE}

MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C)			MC1454 (0 to +70°C)			Unit
					Min	Typ	Max	Min	Typ	Max	
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16 16 16	10 18 36	A_v	8.0 – –	10 18 36	12 – –	– – –	10 18 36	– – –	V/V
Input Impedance	1	–	10	z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	z_o	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16 16 16	10 18 36	BW	– – –	270 250 210	– – –	– – –	270 250 210	– – –	kHz
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	V_o (dc)	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V_{EE} constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V_{CC} constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions
(Linear Operation)

FIGURE 1

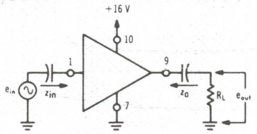

+16 V
10
1
9
e_{in}
z_{in}
7
z_o
R_L
e_{out}

FIGURE 3

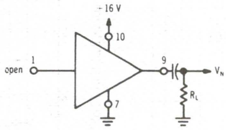

+16 V
10
open
1
9
V_n
7
R_L

FIGURE 4

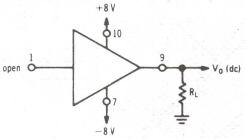
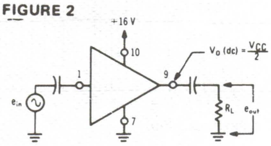

+8 V
10
open
1
9
V_o (dc)
R_L
7
−8 V

FIGURE 2


+16 V
10
V_o (dc) = $\frac{V_{CC}}{2}$
1
9
e_{in}
7
R_L
e_{out}

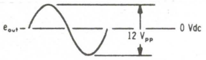
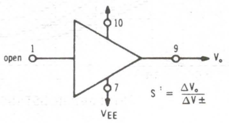

e_{out}
0 Vdc
12 V_{pp}

FIGURE 5


V_{CC}
10
open
1
9
V_o
7
V_{EE}
$S^{\pm} = \frac{\Delta V_o}{\Delta V\pm}$

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Total Power Supply Voltage		$\lvert V_{CC} \rvert + \lvert V_{EE} \rvert$	18	Vdc
Peak Load Current		I_{out}	0.5	Ampere
Audio Output Power		P_{out}	1.8	Watts
Power Dissipation (package limitation)				
T_A = +25°C		P_D	600	mW
Derate above 25°C		$1/\theta_{JA}$	4.8	mW/°C
T_C = +25°C		P_D	1.8	Watts
Derate above 25°C		$1/\theta_{JC}$	14.4	mW/°C
Operating Temperature Range	MC1454	T_A	0 to +70	°C
	MC1554		-55 to +125	
Storage Temperature Range		T_{stg}	-55 to +150	°C

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

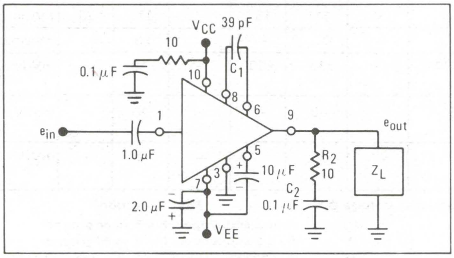
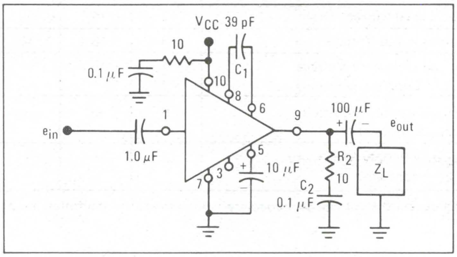


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 µF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V_{CC} supply to pin 10 can cause high frequency instability. To prevent this, the V_{CC} by-pass capacitor should be connected with short leads from the V_{CC} pin to ground. If this capacitor is remotely located a series R-C network (0.1 µF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

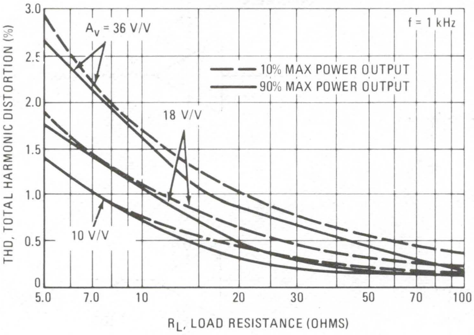
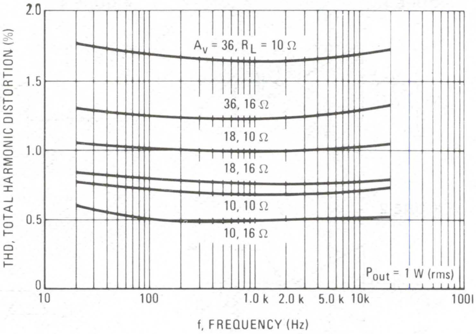


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

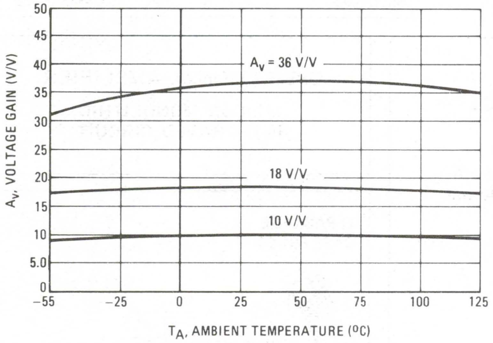


FIGURE 11 – OUTPUT VOLTAGE CHANGE

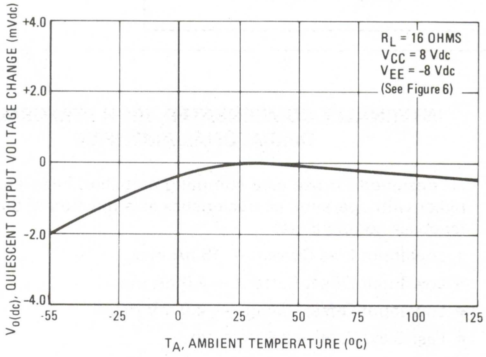


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

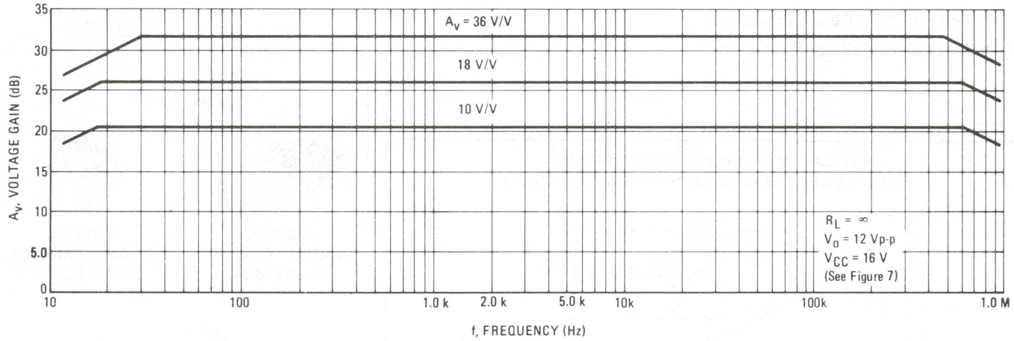
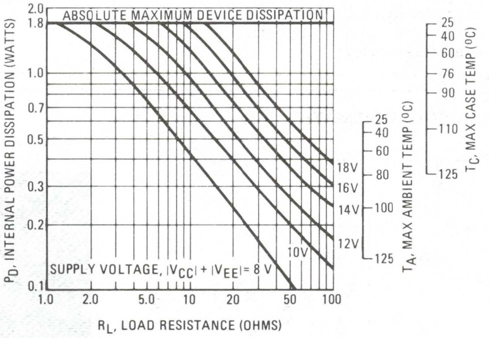


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)



MC1456
MC1456C
MC1556

ORDERING INFORMATION

Device	Temperature Range	Package
MC1456G,CG	0°C to +70°C	Metal Can
MC1456CP1,P1	0°C to +70°C	Plastic DIP
MC1556G	−55°C to +125°C	Metal Can
MC1556U	−55°C to +125°C	Ceramic DIP

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATONAL AMPLIFIER

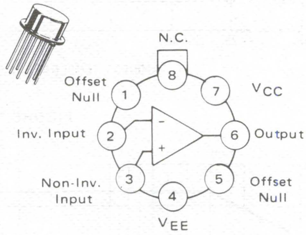
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Bias Current — 15 nA max
- Low Input Offset Current — 2.0 nA max
- Low Input Offset Voltage — 4.0 mV max
- Fast Slew Rate — 2.5 V/µs typ
- Large Power Bandwidth — 40 kHz typ
- Low Power Consumption — 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

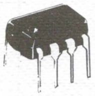
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

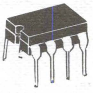
G PACKAGE
CASE 601-04


N.C.
8
Offset Null
1
7
VCC
Inv. Input
2
−
+
6
Output
Non-Inv. Input
3
4
5
Offset Null
VEE

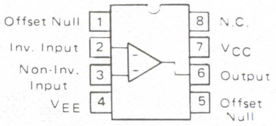
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

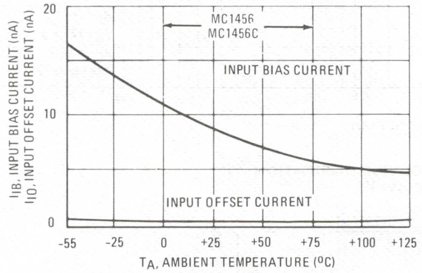


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

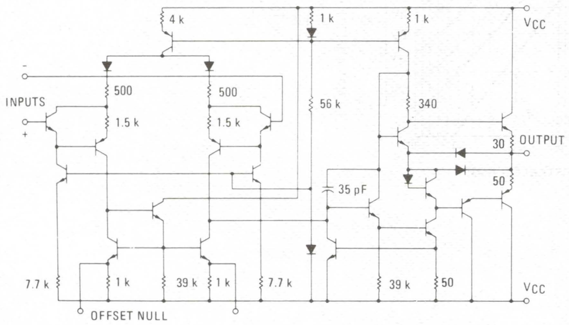

Offset Null
1
Inv. Input
2
Non-Inv. Input
3
VEE
4
8
N.C.
7
VCC
6
Output
5
Offset Null

(Top View)

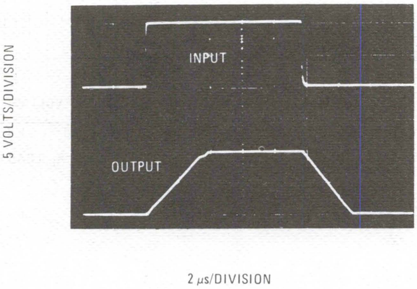
TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556



REPRESENTATIVE CIRCUIT SCHEMATIC


4 k
1 k
1 k
VCC
−
INPUTS
+
500
500
1.5 k
1.5 k
56 k
340
30
OUTPUT
50
35 pF
7.7 k
1 k
39 k
1 k
7.7 k
39 k
50
VCC
OFFSET NULL

VOLTAGE-FOLLOWER PULSE RESPONSE



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556	MC1456 MC1456C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Voltage Range	V_{IDR}	$\pm V_{CC}$		Volts
Common-Mode Voltage Range	V_{ICR}	$\pm V_{CC}$		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation)	P_D	680		mW
Derate above T_A = +25°C		4.6		mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = - 15 Vdc, T_A = +25°C unless otherwise noted).

			MC1556			MC1456			MC1456C			
Characteristic	Fig.	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Input Bias Current		I_{IB}										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
T_A = T_{low} to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		I_{IO}										nAdc
T_A = +25°C			–	1.0	2.0	–	5.0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
T_A = T_{low} to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		V_{IO}										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		r_p	–	5.0	–	–	3.0	–	–	3.0	–	Megohms
Parallel Input Capacitance		c_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		z_i	–	250	–	–	250		–	250	–	Megohms
Common-Mode Input Voltage Range	1	V_{ICR}	±12	±13	–	+11	±12	–	±10.5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	2	e_n	–	45			45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CMRR	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_O = ± 10 V, R_L = 2.0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
T_A = T_{low} to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_O = 20 Vp-p)	9	BW_p	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		SR	–	2.5	–	–	2.5	–	–	2.5	–	V/µs
Output Impedance (f = 20 Hz)		z_o	–	1.0	2.0	–	1.0	2.5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{OS}	–	-17, +9.0	–	–	-17, +9.0	–	–	-17, +9.0	–	mAdc
Output Voltage Swing (R_L = 2.0 k ohms)	10	V_{OR}	±12	±13	–	+11	±12	–	±10	±12	–	V_{pk}
Power Supply Rejection Ratio												µV/V
V_{CC} = constant, $R_S \leqslant$ 10 k ohms		PSRR+		50	100	–	75	200	–	75	–	
V_{EE} = constant, $R_S \leqslant$ 10 k ohms		PSRR-		50	100	–	75	200	–	75	–	
Power Supply Current		I_{CC}	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	mAdc
		I_{EE}	–	1.0	1.5	–	1.3	3.0	–	1.3	4.0	
DC Quiescent Power Dissipation (V_O = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1: T_{low}: 0° for MC1456 and MC1456C
-55°C for MC1556
T_{high}: +70°C for MC1456 and MC1456C
+125°C for MC1556

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 — INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

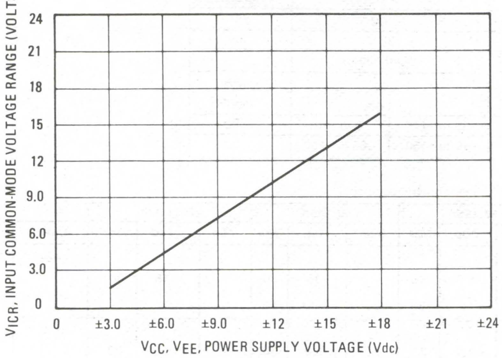


FIGURE 2 — SPECTRAL NOISE DENSITY

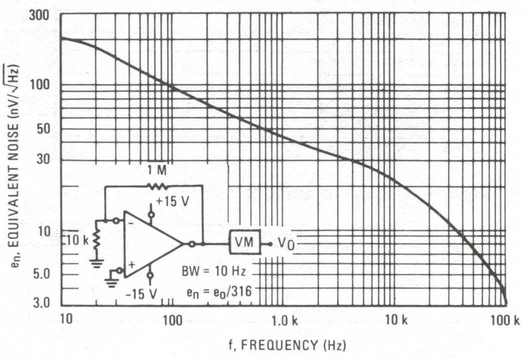


FIGURE 3 — COMMON-MODE REJECTION RATIO versus FREQUENCY

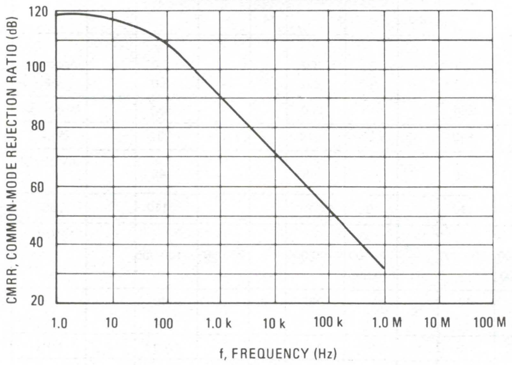


FIGURE 4 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

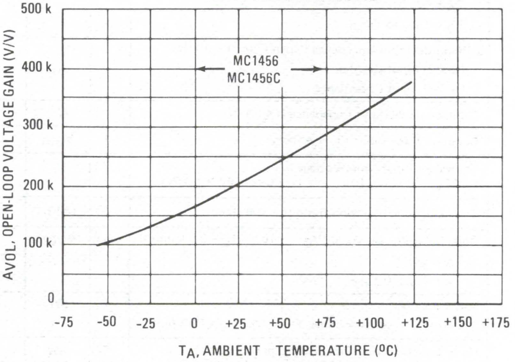


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

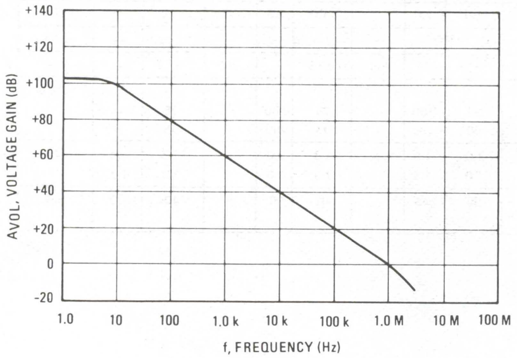
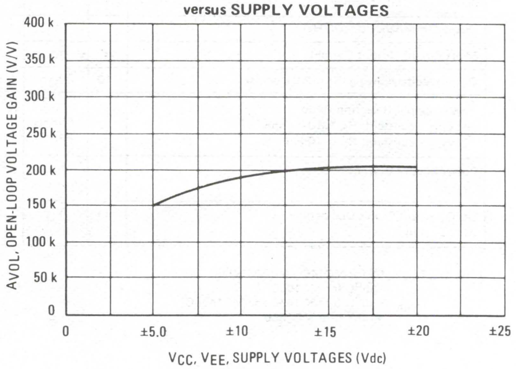


FIGURE 6 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

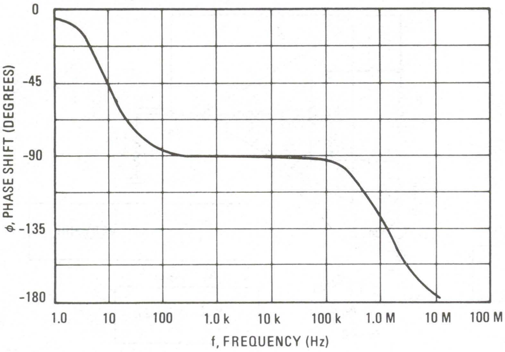


FIGURE 7 – OPEN-LOOP PHASE SHIFT

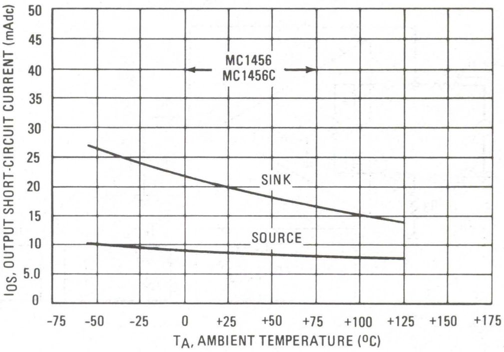


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

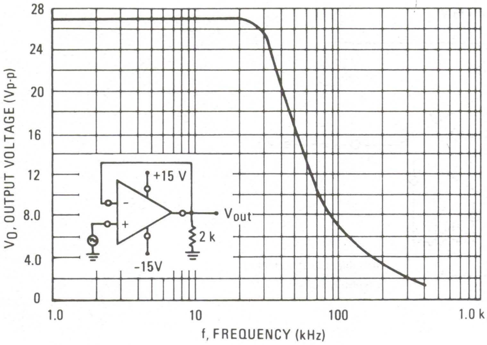


FIGURE 9 – POWER BANDWIDTH

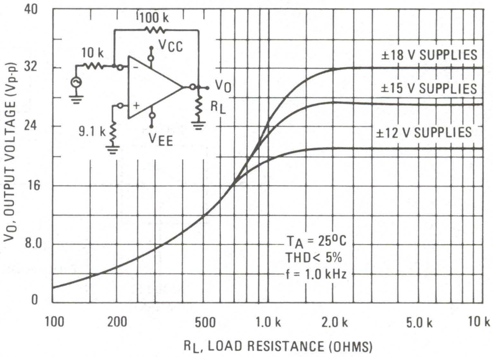


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

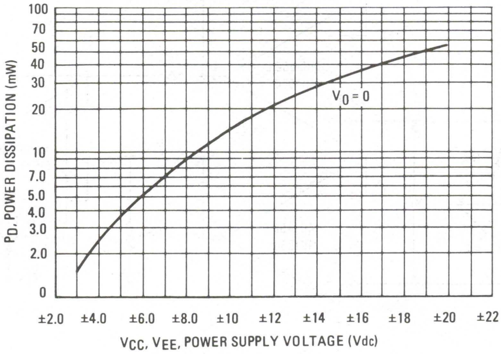
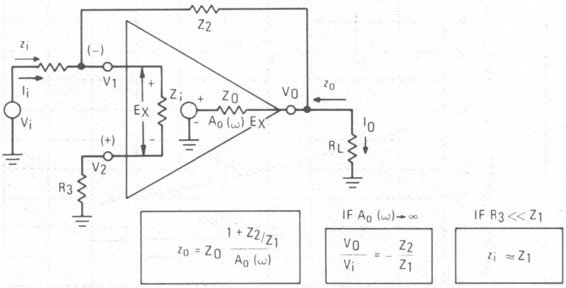


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 — INVERTING FEEDBACK MODEL


Z2
zi
Ii
Vi
(−)
V1
+
EX
−
Zi
+
ZO
−
AO (ω) EX
VO
zo
IO
RL
(+)
V2
R3

$z_o = Z_O \frac{1 + Z_2/Z_1}{A_O(\omega)}$

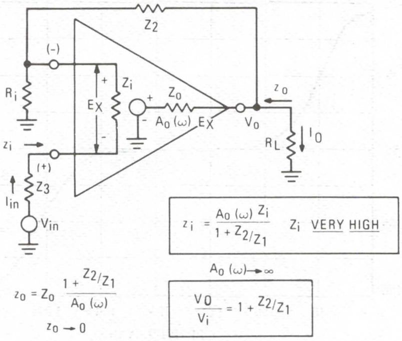
IF $A_O(\omega) \to \infty$

$\frac{V_O}{V_i} = -\frac{Z_2}{Z_1}$

IF $R_3 << Z_1$

$z_i \approx Z_1$

FIGURE 13 — NONINVERTING FEEDBACK MODEL


Z2
(−)
Ri
+
EX
−
Zi
+
ZO
−
AO (ω) EX
zo
VO
RL
IO
zi
(+)
Z3
Iin
Vin

$z_i = \frac{A_O(\omega)\, Z_i}{1 + Z_2/Z_1}$ Z_i VERY HIGH

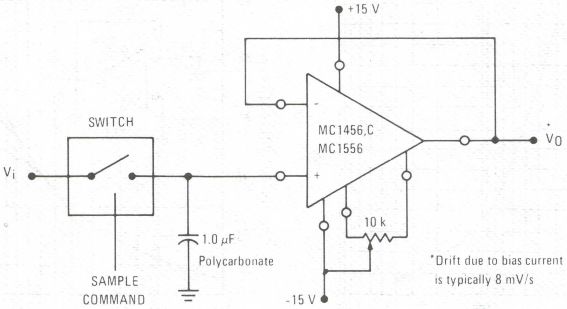
$A_O(\omega) \to \infty$

$\frac{V_O}{V_i} = 1 + Z_2/Z_1$

$z_o = Z_O \frac{1 + Z_2/Z_1}{A_O(\omega)}$

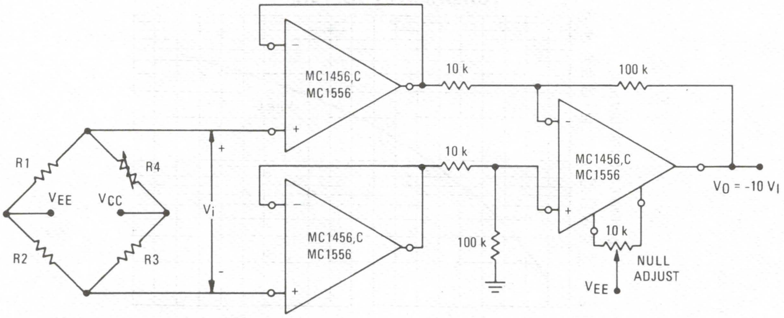
$z_O \to 0$

FIGURE 14 — LOW-DRIFT SAMPLE AND HOLD


+15 V
SWITCH
Vi
SAMPLE COMMAND
1.0 µF Polycarbonate
−
+
MC1456,C
MC1556
10 k
−15 V
VO

*Drift due to bias current is typically 8 mV/s

FIGURE 15 — HIGH IMPEDANCE BRIDGE AMPLIFIER


MC1456,C
MC1556
10 k
100 k
R1
R4
VEE
VCC
R2
R3
+
Vi
−
MC1456,C
MC1556
10 k
100 k
MC1456,C
MC1556
10 k
NULL ADJUST
VEE
VO = −10 VI

TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER

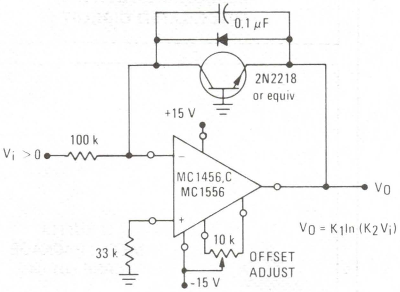

0.1 μF
2N2218
or equiv
+15 V
100 k
Vi > 0
MC1456,C
MC1556
VO
VO = K1ln (K2Vi)
33 k
10 k
OFFSET
ADJUST
-15 V

FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT

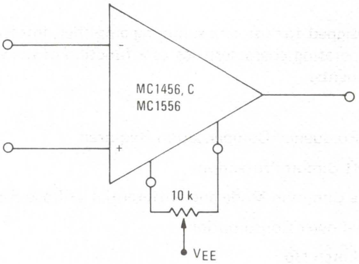
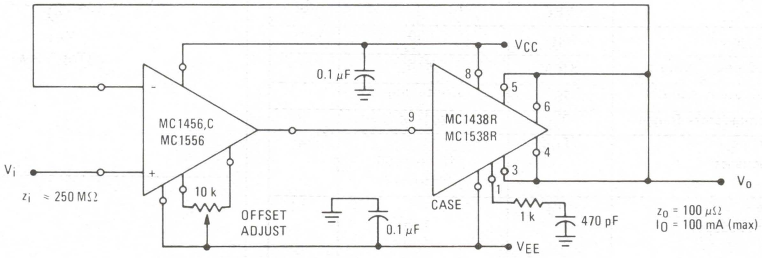

MC1456, C
MC1556
10 k
VEE

FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER


VCC
0.1 μF
8
5
6
9
MC1456,C
MC1556
MC1438R
MC1538R
4
3
Vi
zi ≈ 250 MΩ
10 k
OFFSET
ADJUST
CASE
1
1 k
470 pF
0.1 μF
VEE
Vo
zO = 100 μΩ
IO = 100 mA (max)

MC1458, MC1458N, MC1458C MC1558, MC1558N

ORDERING INFORMATION

Device	Temperature Range	Package
MC1458G,CG,NG	0°C to + 70°C	Metal Can
MC1558G,NG	−55°C to +125°C	Metal Can
MC1458CU,NU,U	0°C to +70°C	Ceramic DIP
MC1558NU,U	−55°C to +125°C	Ceramic DIP
MC1458CP1,NP1,P1	0°C to +70°C	Plastic DIP

DUAL MC1741 INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

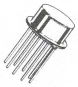
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered — N Suffix

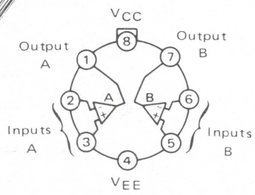
(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04


VCC
Output A
Output B
Inputs A
Inputs B
VEE
1
2
3
4
5
6
7
8
A
B

(Top View)

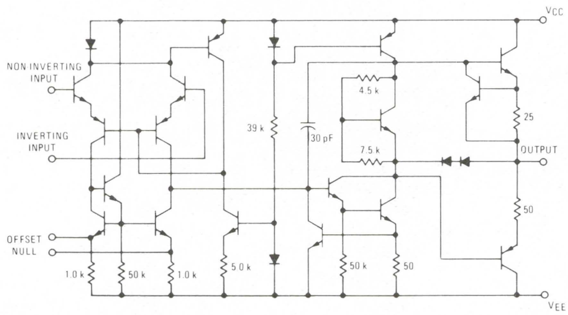
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

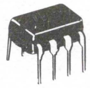
Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

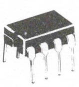
EQUIVALENT CIRCUIT SCHEMATIC

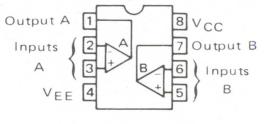

VCC
NON INVERTING INPUT
INVERTING INPUT
OFFSET NULL
4.5 k
39 k
30 pF
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1458, MC1458C, MC1458N)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02




Output A
Inputs A
VEE
VCC
Output B
Inputs B
1
2
3
4
5
6
7
8
A
B

(Top View)

ELECTRICAL CHARACTERISTICS – Note 1. (V_{CC} = 15 V, V_{EE} = 15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2.0 k)		50	200	–	20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	60	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	–	30	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	±11	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	150	–	70	170	–	70	240	mW
Transient Response (Unity Gain)											
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS Note 1 (V_{CC} = 15 V, V_{EE} = 15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	–	–	12	mV
Input Offset Current	I_{IO}										nA
(T_A = 125°C)		–	7.0	200	–	–	–	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	–	–	400	
Input Bias Current	I_{IB}										nA
(T_A = 125°C)		–	30	500	–	–	–	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	–	–	1000	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	–	–	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2 k)		25	–	–	15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	15	–	–	
Supply Currents (Both Amplifiers)	I_D										mA
(T_A = 125°C)		–	–	4.5	–	–	–	–	–	–	
(T_A = -55°C)		–	–	6.0	–	–	–	–	–	–	
Power Consumption (T_A = 125°C)	P_C	–	–	135	–	–	–	–	–	–	mW
(T_A = -55°C)		–	–	180	–	–	–	–	–	–	

*T_{high} = 125°C for MC1558 and 70°C for MC1458, MC1458C
T_{low} = –55°C for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

NOISE CHARACTERISTICS (Applies for MC1558N and MC1458N only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC1558N			MC1458N			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 kΩ) (Input Referenced)	E_n	–	–	20	–	–	20	μVpeak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

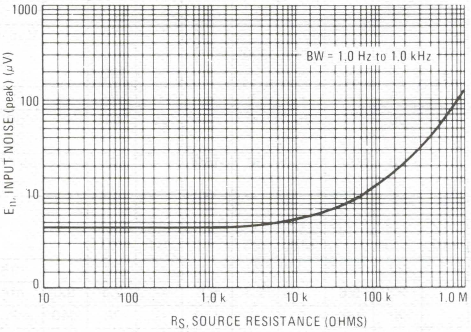


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

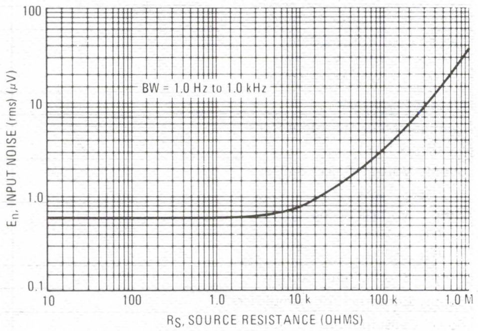


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

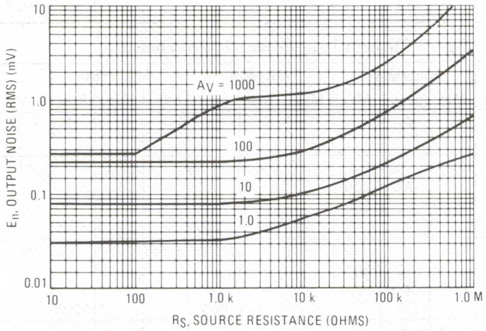


FIGURE 4 – SPECTRAL NOISE DENSITY

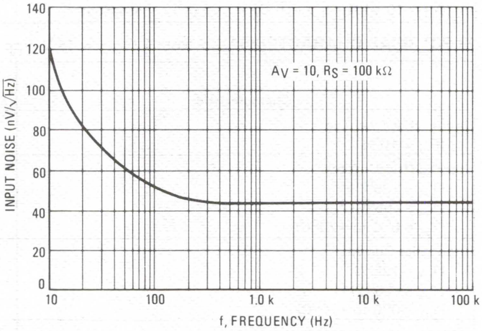
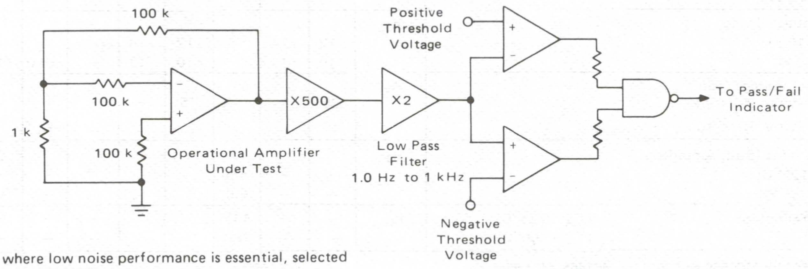


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)


100 k
100 k
1 k
100 k
Operational Amplifier
Under Test
X500
X2
Low Pass
Filter
1.0 Hz to 1 kHz
Positive
Threshold
Voltage
Negative
Threshold
Voltage
To Pass/Fail
Indicator

For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

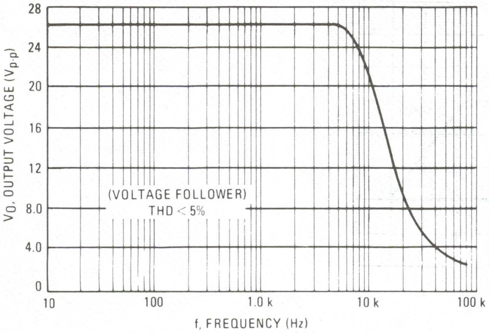


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

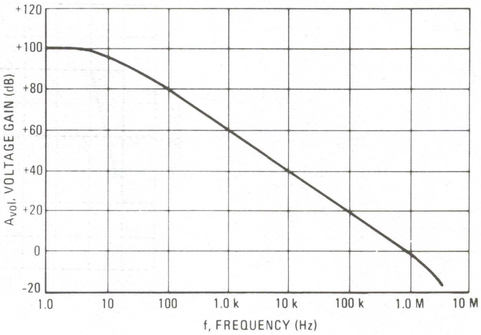


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

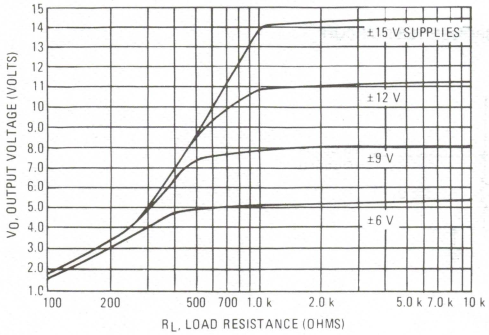


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

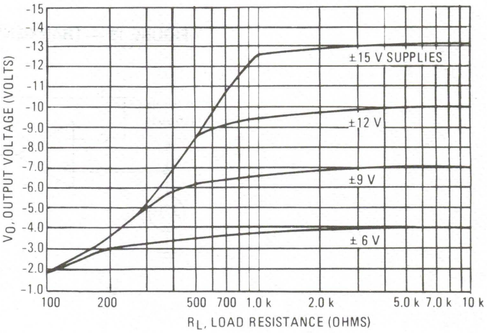


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

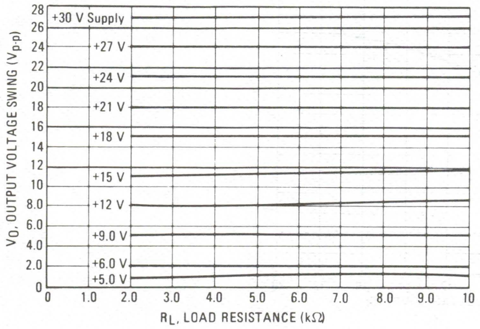


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

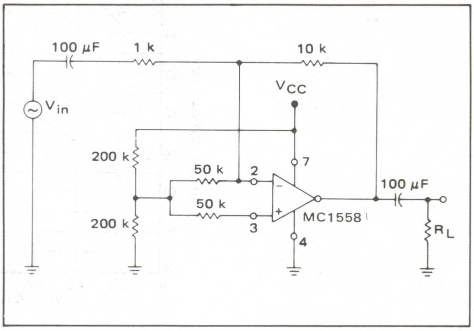


FIGURE 12 — NONINVERTING PULSE RESPONSE

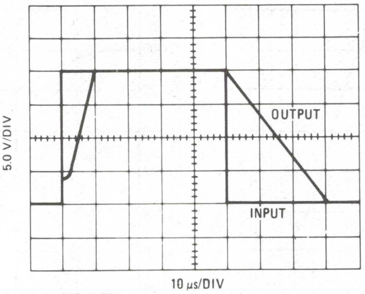


FIGURE 13 — TRANSIENT RESPONSE TEST CIRCUIT

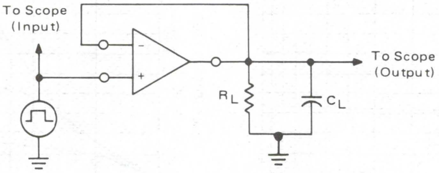
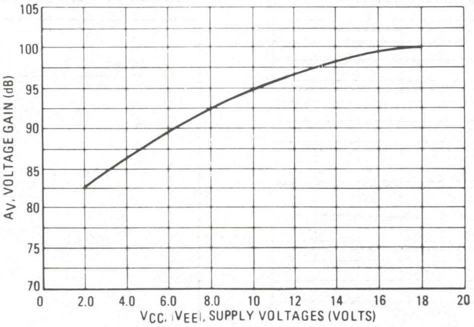

To Scope
(Input)
-
+
To Scope
(Output)
RL
CL

FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



MC1458S
MC1558S

DUAL OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

ORDERING INFORMATION

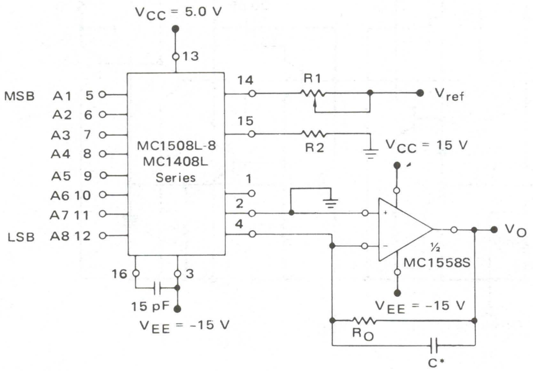
Device	Temperature Range	Package
MC1458SG	0°C to +70°C	Metal Can
MC1458SP1	0°C to +70°C	Plastic DIP
MC1458SU	0°C to +70°C	Ceramic DIP
MC1558SG	−55°C to +125°C	Metal Can
MC1558SU	−55°C to +125°C	Ceramic DIP

DUAL HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/µs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


VCC = 5.0 V
13
MSB
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB
A8 12
MC1508L-8
MC1408L
Series
14
R1
Vref
15
R2
VCC = 15 V
1
2
4
½
MC1558S
VO
16
3
15 pF
VEE = −15 V
VEE = −15 V
RO
C*

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 µs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

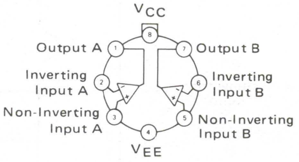
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

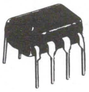
$$V_{ref} = 2.0\ \text{Vdc}$$
$$R1 = R2 \cong 1.0\ \text{k}\Omega$$
$$R_O = 5.0\ \text{k}\Omega$$

$$V_O = \frac{2\ \text{V}}{1\ \text{k}}(5\ \text{k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ \text{V}\left[\frac{255}{256}\right] = 9.961\ \text{V}$$

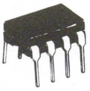
G SUFFIX
METAL PACKAGE
CASE 601-04


VCC
8
Output A
1
Output B
7
Inverting
Input A
2
Inverting
Input B
6
Non-Inverting
Input A
3
Non-Inverting
Input B
5
4
VEE

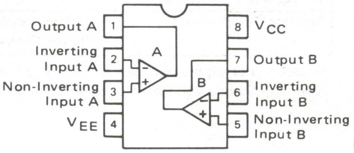
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1458S Only)

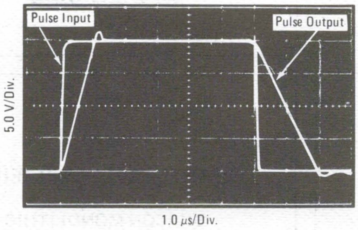


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

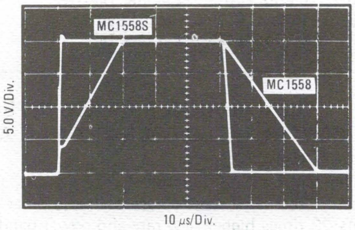

Output A
1
Inverting
Input A
2
Non-Inverting
Input A
3
VEE
4
A
B
8
VCC
7
Output B
6
Inverting
Input B
5
Non-Inverting
Input B

(Top View)

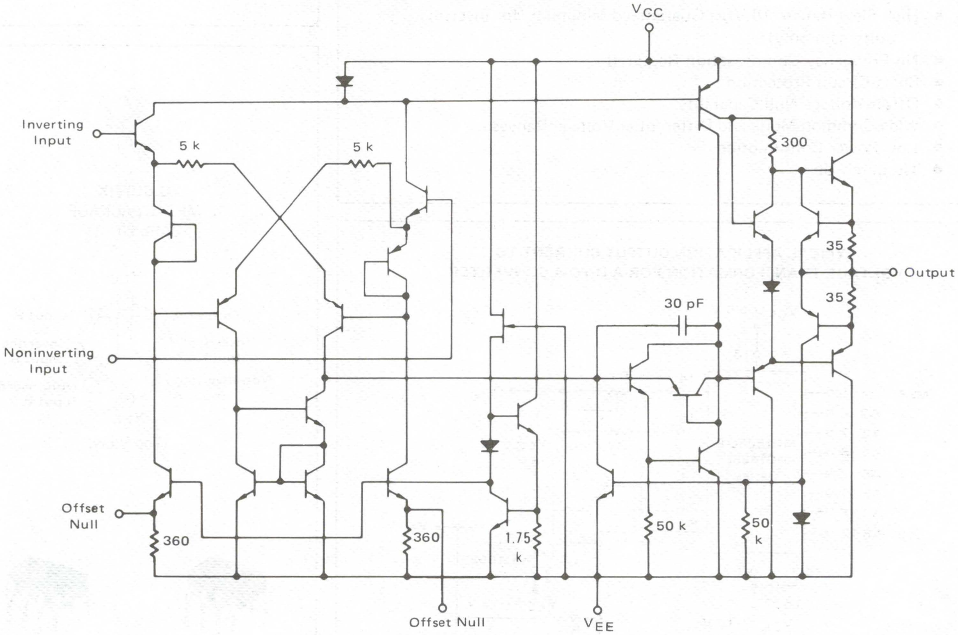
MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)



STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)



½ REPRESENTATIVE CIRCUIT SCHEMATIC


VCC
Inverting Input
5 k
5 k
300
35
Output
35
30 pF
Noninverting Input
Offset Null
360
360
1.75 k
50 k
50 k
Offset Null
VEE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage		V_{CC} V_{EE}	+22 −22	+18 −18	Vdc
Input Differential Voltage Range ①		V_{IDR}	±30		Volts
Input Common-Mode Voltage Range ②		V_{ICR}	±15		Volts
Output Short Circuit Duration		t_S	Continuous		
Operating Ambient Temperature Range		T_A	−55 to +125	0 to +70	°C
Storage Temperature Range		T_{stg}	−65 to +150	−65 to +150	°C
Junction Temperature	Ceramic and Metal Package	T_J	175	175	°C
	Plastic Package		150	150	°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3)	BW_p							kHz
A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)		150	200	–	150	200	–	
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(−) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(−)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±45	±10	–	±45	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4)	A_{VOL}							–
V_O = ±10 V		50,000	200,000	–	20,000	100,000	–	
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}	–	200	500	–	200	500	nA
Input Offset Current	$\|I_{IO}\|$	–	30	200	–	30	200	nA
Input Offset Voltage (R_S = ≤10 kΩ)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_C	–	70	150	–	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	–	2.0	150	–	2.0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS−	–	10	150	–	10	150	µV/V

**Plastic package offered in limited temperature range device only.

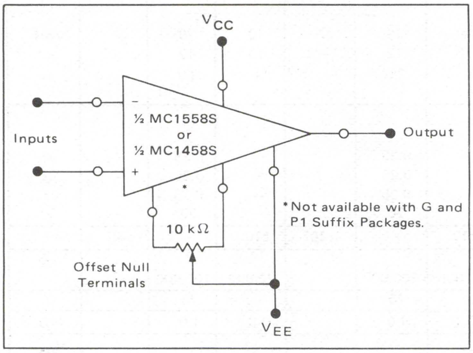
ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, V_{EE} = −15 Vdc, T_A = −55 to +125°C for MC1558S and T_A = 0 to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain V_O = ±10 V	A_{VOL}	25,000	–	–	15,000	–	–	V/V
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	–	–	±12	–	–	
R_L = 2 kΩ		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±12	–	–	–	–	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	–	–	–	–	–	dB
Input Bias Current	I_{IB}							nA
T_A = 125°C		–	200	500	–	–	–	
T_A = −55°C		–	500	1500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	800	
Input Offset Current	I_{IO}							nA
T_A = 125°C		–	30	200	–	–	–	
T_A = −55°C		–	–	500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	300	
Input Offset Voltage R_S ≤ 10 kΩ	V_{IO}	–	–	6.0	–	–	7.5	mV
DC Power Consumption V_O = 0 V	P_C	–	–	200	–	–	–	mW
Positive Power Supply Sensitivity V_{EE} = −15 V	P_{SS+}	–	–	150	–	–	–	µV/V
Negative Power Supply Sensitivity V_{CC} = 15 V	P_{SS-}	–	–	150	–	–	–	µV/V

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT


VCC
Inputs
−
+
½ MC1558S
or
½ MC1458S
Output
*
10 kΩ
Offset Null
Terminals
VEE

*Not available with G and P1 Suffix Packages.

FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

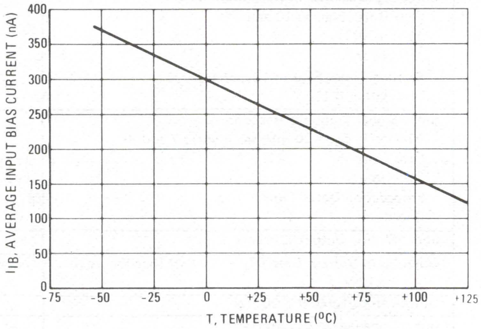


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

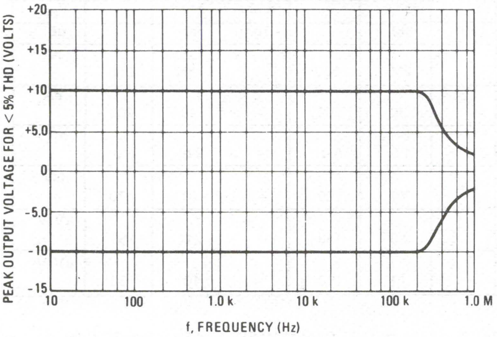


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

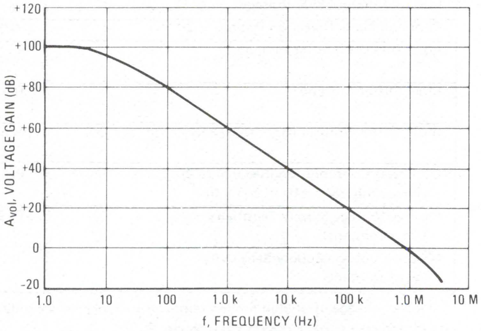
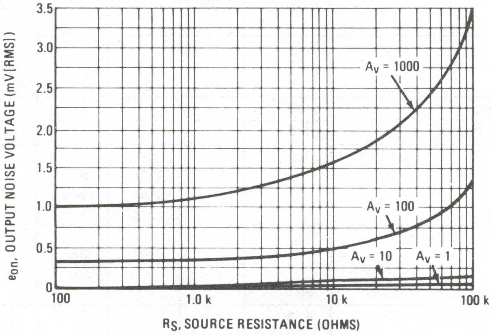


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 — SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

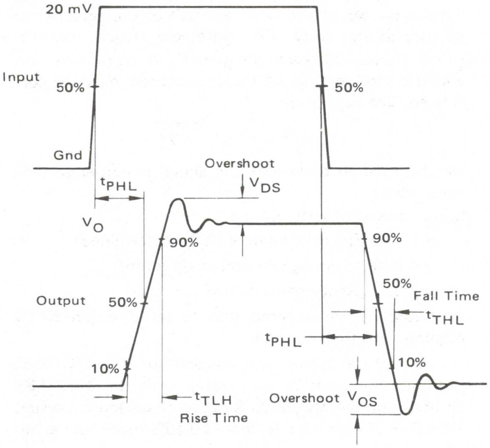

20 mV
Input
50%
50%
Gnd
Overshoot
V_{DS}
t_{PHL}
V_O
90%
90%
Output
50%
50%
Fall Time
t_{THL}
t_{PHL}
10%
10%
t_{TLH}
Rise Time
Overshoot V_{OS}

FIGURE 7 — SMALL-SIGNAL TRANSIENT RESPONSE

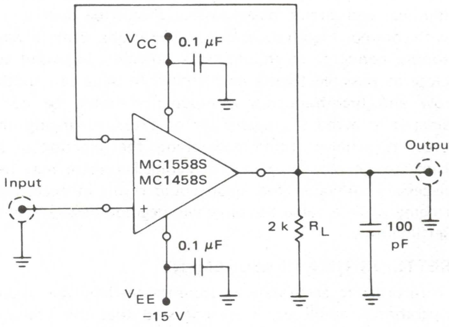

V_{CC}
0.1 μF
MC1558S
MC1458S
Input
Output
2 k
R_L
100 pF
0.1 μF
V_{EE}
−15 V

FIGURE 8 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

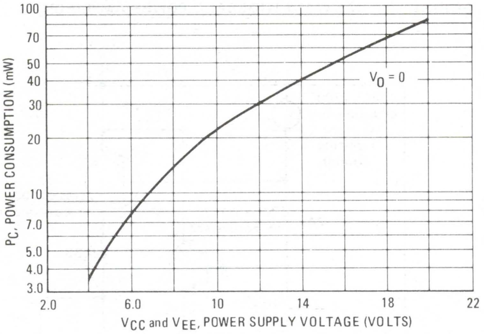


FIGURE 9 — LARGE-SIGNAL TRANSIENT WAVEFORMS

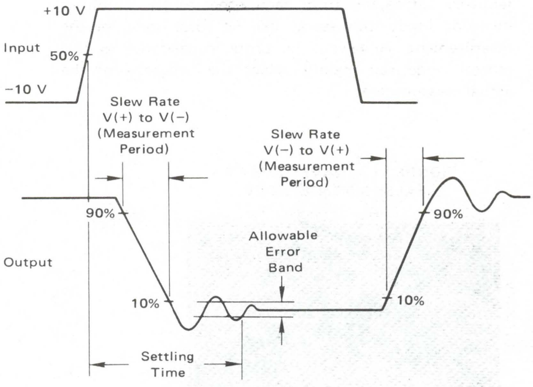
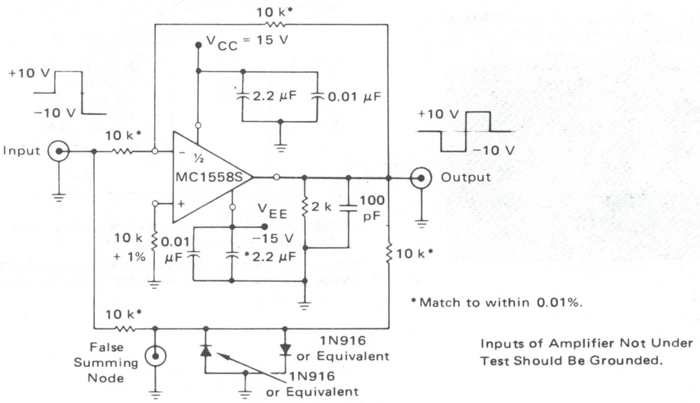

+10 V
Input
50%
−10 V
Slew Rate V(+) to V(−) (Measurement Period)
Slew Rate V(−) to V(+) (Measurement Period)
90%
90%
Output
Allowable Error Band
10%
10%
Settling Time

FIGURE 10 — SLEW RATE AND SETTLING TIME TEST CIRCUIT*


10 k*
V_{CC} = 15 V
2.2 μF
0.01 μF
+10 V
−10 V
10 k*
Input
½
MC1558S
+10 V
−10 V
Output
V_{EE}
2 k
100 pF
10 k + 1%
0.01 μF
−15 V
*2.2 μF
10 k*
10 k*
False Summing Node
1N916 or Equivalent
1N916 or Equivalent

*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

FIGURE 11 — WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)

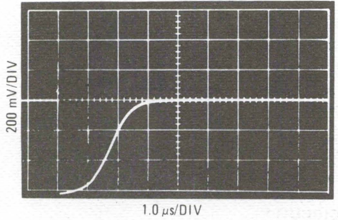
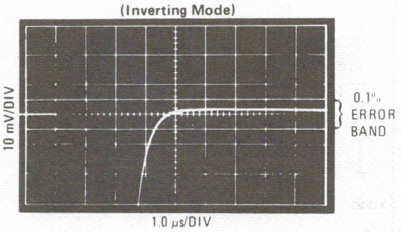


FIGURE 12 — EXPANDED WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)



The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

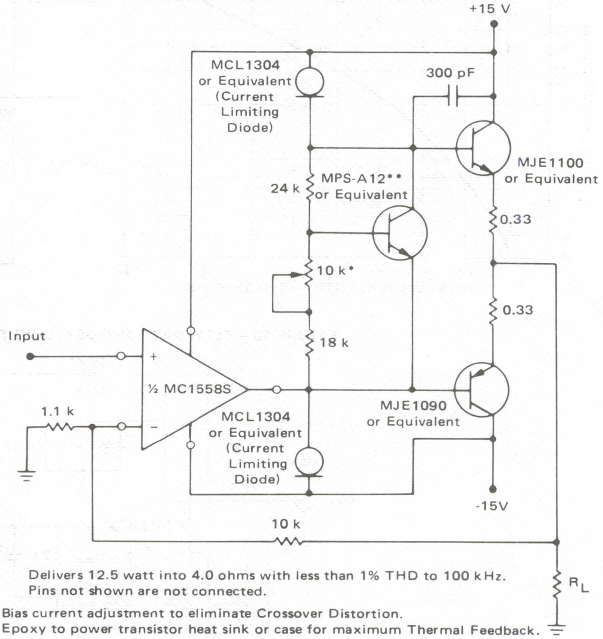
t_{setlg} = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

TYPICAL APPLICATION

FIGURE 13 — 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

MOTOROLA

MC1590

WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

RF/IF/AUDIO AMPLIFIER

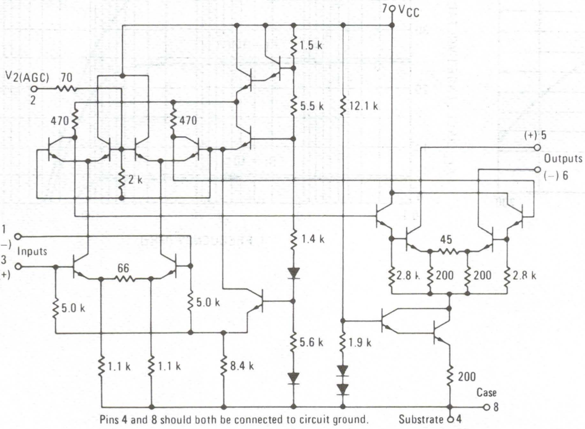
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, −55 to +125°C. See Motorola Application Note AN-513 for design details.

- High Power Gain – 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

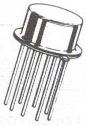
Rating	Symbol*	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	$V_{2(AGC)}$	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

REPRESENTATIVE CIRCUIT SCHEMATIC

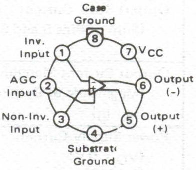


Pins 4 and 8 should both be connected to circuit ground.

PIN CONNECTIONS



G SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)

ADMITTANCE PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C)

Parameter	Symbol	f = MHz Typ		Unit
		30	60	
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.6 −3.0	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	$\|Y_{21}\|$ θ_{21} (Polar)	175 −30	150 −105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	−0 −5.0	−0 −10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ		Unit
		30	60	
Input Reflection Coefficient	$\|S_{11}\|$ θ_{11}	0.95 −7.3	0.93 −16	– degrees
Output Reflection Coefficient	$\|S_{22}\|$ θ_{22}	0.99 −3.0	0.98 −5.5	– degrees
Forward Transmission Coefficient	$\|S_{21}\|$ θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = –55°C to 125°C unless otherwise noted)

Characteristic	Fig.	Symbol	MC1590 Min	MC1590 Typ	MC1590 Max	Unit
AGC Range						
($V_{2(AGC)}$ = 5.0 V to 7.0 V)		M_{AGC}	58	–	–	dB
($V_{2(AGC)}$ = 5.0 V to 7.0 V, T_A = 25°C)	24		60	68	–	
Single-Ended Power Gain		G_p	37	–	–	dB
(T_A = 25°C)	24		40	45		
Noise Figure (R_s optimized for best NF) (T_A = 25°C)	24	NF	–	6.0	7.0	dB
Output Voltage Swing Differential Output	25	V_{ODR}				Vpp
(0 dB AGC)			10	–	–	
(0 dB AGC, T_A = 25°C)			13	14	–	
(-30 dB AGC)			4.0	–	–	
(-30 dB AGC, T_A = 25°C)			5.0	6.0	–	
Single-Ended Output (Pin 5, 6)	25	V_{OCR}				Vpp
(0 dB AGC)			5.0	–	–	
(0 dB AGC, T_A = 25°C)			6.5	7.0	–	
(-30 dB AGC)			2.0	–	–	
(-30 dB AGC, T_A = 25°C)			2.5	3.0	–	
Output Stage Current	32	I_O				
(Sum of Pins 5 and 6)			3.5	–	8.0	mA
(T_A = 25°C)			4.0	5.6	7.5	
Output Current Matching (Magnitude of Difference of Output Currents) (I_5 - I_6) (T_A = 25°C)	32	ΔI_O	–	0.7	–	mA
Power Supply Current	32					
(V_O = 0 V)		I_{CC}	–	–	20	mA
(V_O = 0 V, T_A = 25°C)			–	14	17	
Power Consumption (12 x I_{CC})	–					
(V_I = 0 V)		P_C	–	–	240	mW
(V_I = 0 V, T_A = 25°C)			–	168	204	

FIGURE 1 — UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, See Figure 24)

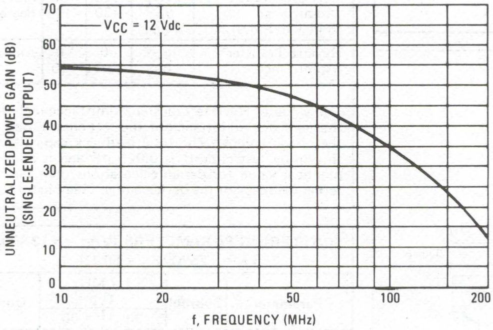
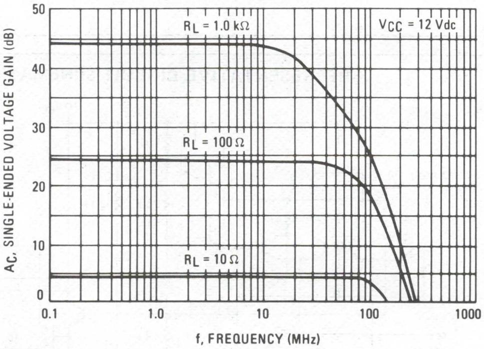


FIGURE 2 — VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, See Figure 26)



TYPICAL CHARACTERISTICS

($V_{2\,(AGC)} = 0$, $V_{CC} = 12$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted)

FIGURE 3 – DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)

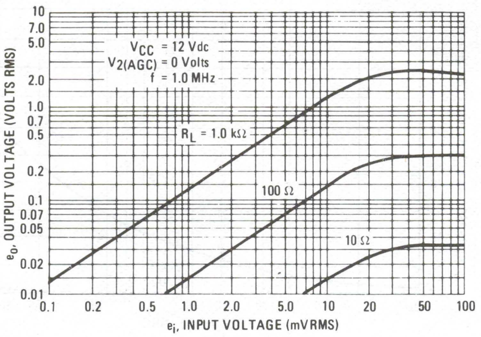


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)

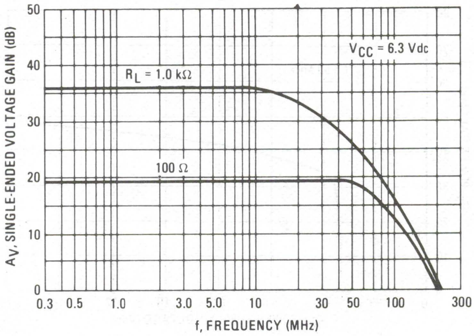


FIGURE 5 – VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)

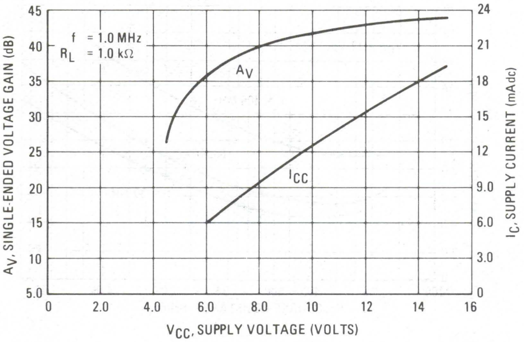


FIGURE 6 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE

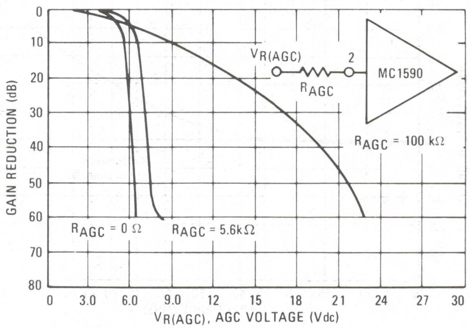


FIGURE 7 – TYPICAL GAIN REDUCTION versus AGC CURRENT

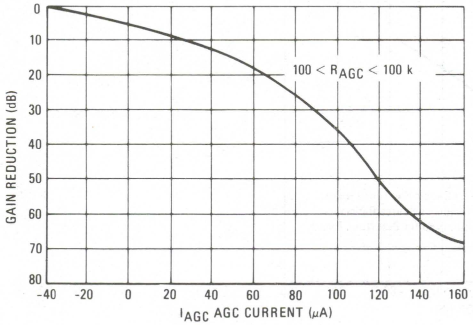
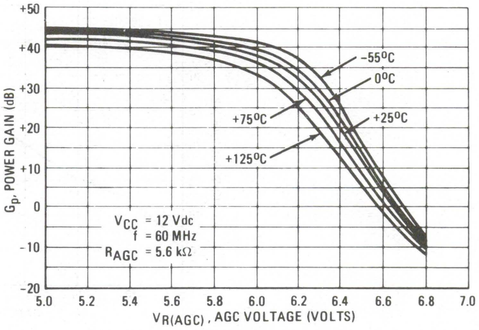


FIGURE 8 – FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 24)

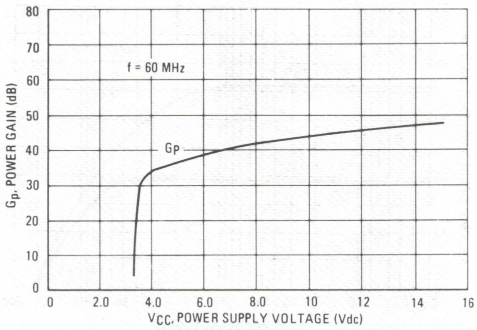


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, Page 1)

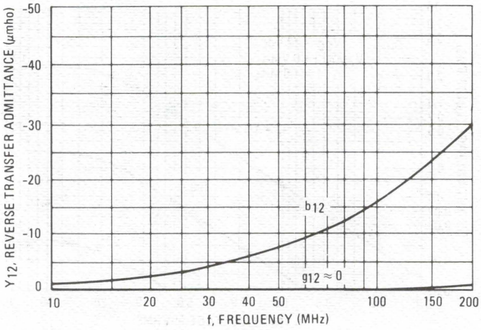


FIGURE 11 – NOISE FIGURE versus FREQUENCY

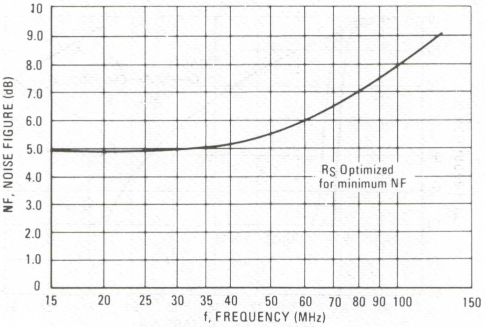


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

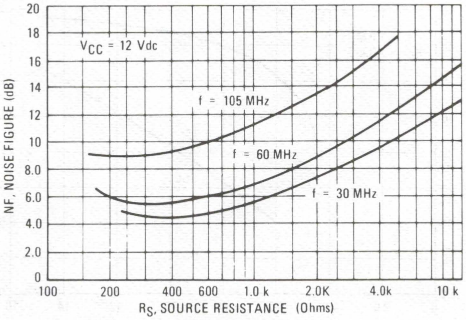
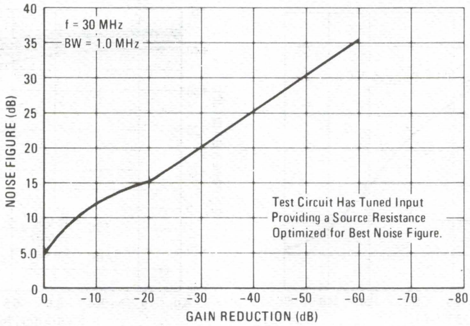


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – SINGLE-ENDED OUTPUT ADMITTANCE

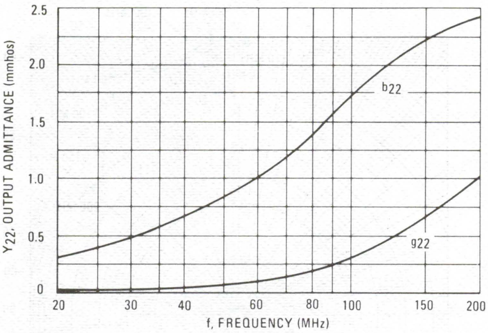


FIGURE 15 – SINGLE-ENDED INPUT ADMITTANCE

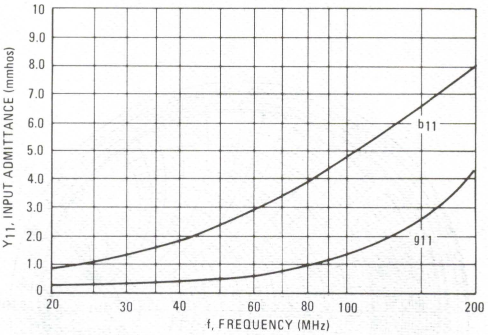


FIGURE 16 – HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

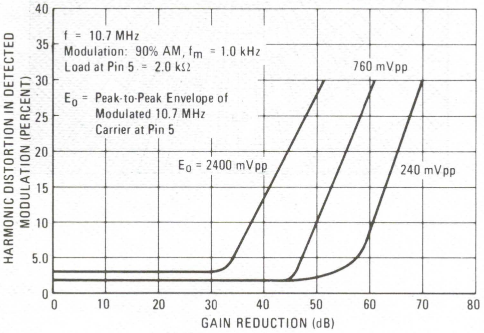
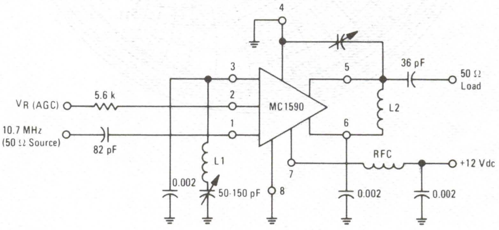


FIGURE 17 – 10.7-MHz AMPLIFIER
Gain ≃ 55 dB, BW ≃ 100 kHz



4
3
5
36 pF
50 Ω Load
VR (AGC)
5.6 k
2
MC1590
L2
10.7 MHz (50 Ω Source)
82 pF
1
6
RFC
+12 Vdc
L1
7
0.002
50-150 pF
8
0.002
0.002

L1 = 24 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (~124 pF)
L2 = 20 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (~100 pF)

FIGURE 18 – Y_{21}, FORWARD TRANSFER ADMITTANCE RECTANGULAR FORM

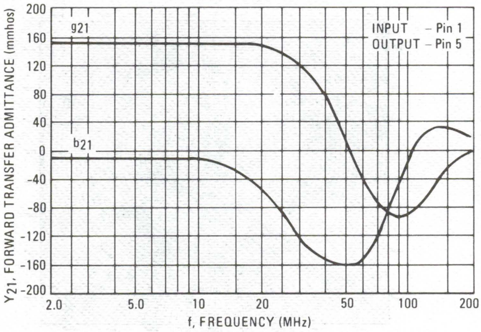
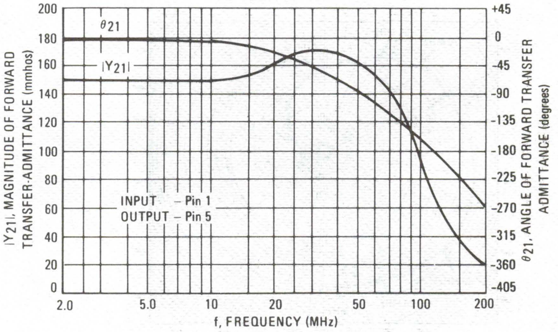


FIGURE 19 – Y_{21}, FORWARD TRANSFER ADMITTANCE POLAR FORM



TYPICAL CHARACTERISTICS (continued)

FIGURE 20 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

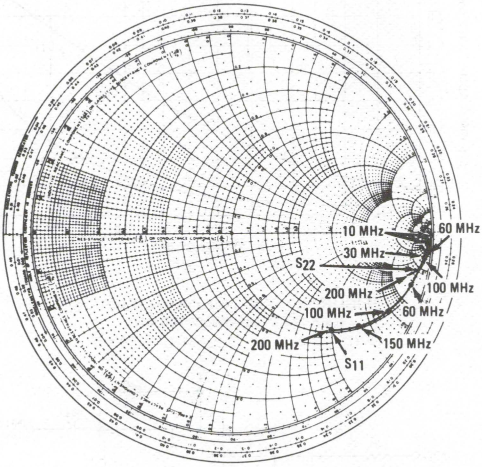


FIGURE 21 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

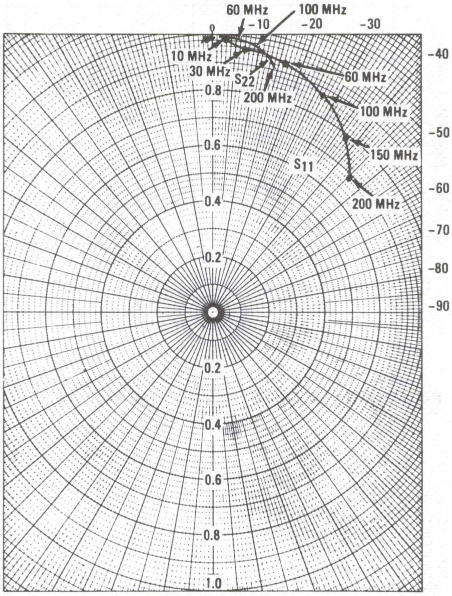


FIGURE 22 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

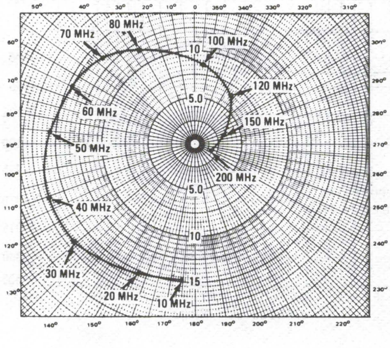
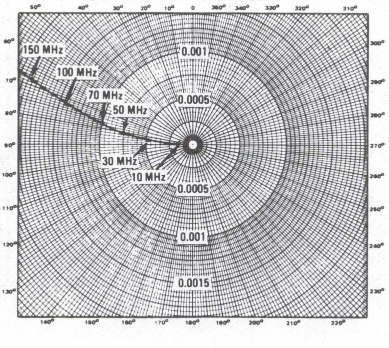
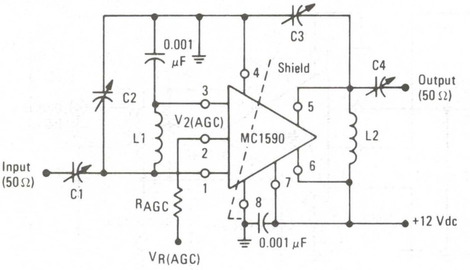


FIGURE 23 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



TYPICAL APPLICATIONS

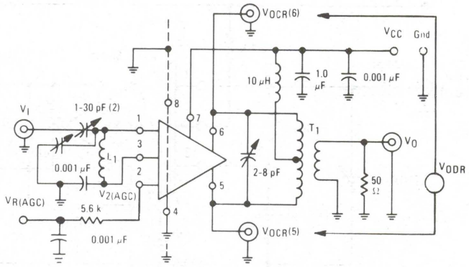
FIGURE 24 – 60-MHz POWER GAIN TEST CIRCUIT


0.001
μF
C3
C2
3
4
Shield
C4
Output
(50 Ω)
5
V2(AGC)
L1
MC1590
L2
2
Input
(50Ω)
C1
1
6
7
RAGC
8
L
0.001 μF
+12 Vdc
VR(AGC)

L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long

C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 25 – DIFFERENTIAL OUTPUT VOLTAGE SWING, (V5, V6) (60 MHz)


VOCR(6)
VCC
Gnd
10 μH
1.0 μF
0.001 μF
VI
1-30 pF (2)
8
7
1
3
L1
6
T1
VO
0.001 μF
2
2-8 pF
5
50 Ω
VODR
VR(AGC)
V2(AGC)
5.6 k
4
0.001 μF
VOCR(5)

L1: 7 Turns, # 22 AWG Wire on 5/16" Dia. Form, 5/8" Long
T1: Close Wound Over 1/4" Form
Primary Winding - 16 Turns # 26 AWG, Center Tapped
Secondary Winding = 2 Turns # 26 AWG.

FIGURE 25a – PROCEDURE FOR SET–UP USING FIGURES 24 OR 25

Test	e_{in}	$V_{2(AGC)}$	R_{AGC}(kΩ)
M_{AGC}	2.23 mV (–40dBm)	5-7 V	0
Gp	1.0 mV (–47dBm)	≤5.0 V	5.6
NF	1.0 mV (–47dBm)	≤5.0 V	5.6
$V_{OCR(5)}$ $V_{OCR(6)}$ V_{ODR}			5.6
(0dB)	Adjust e_{in} for Square Wave Output $V_{2(AGC)} = V_{R(AGC)} = 0$ V	>0 dB Limit	
(–30 dB)	Adjust e_{in} to 1.0 mV Adjust $V_{R(AGC)}$ so that output is –30 dB then reset e_{in} to Square Wave Output	>–30 dB Limit	

FIGURE 26 – VIDEO AMPLIFIER

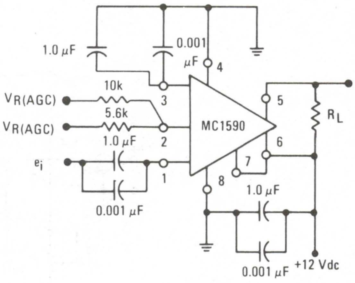
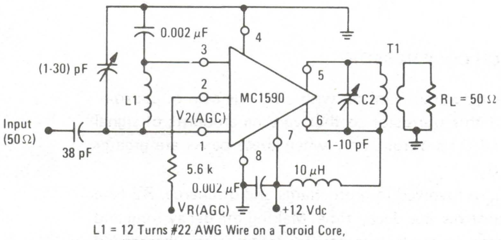
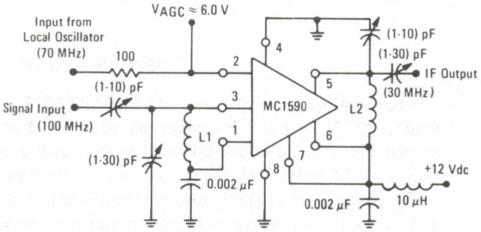

1.0 μF
0.001 μF
4
10k
eo
VR(AGC)
3
5
5.6k
RL
VR(AGC)
MC1590
1.0 μF
2
6
ei
7
1
8
0.001 μF
1.0 μF
0.001 μF
+12 Vdc

FIGURE 27 – 30-MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)


0.002 μF
4
3
T1
(1-30) pF
5
2
L1
MC1590
C2
RL = 50 Ω
V2(AGC)
6
Input
(50Ω)
7
1-10 pF
1
38 pF
8
5.6 k
10 μH
0.002 μF
VR(AGC)
+12 Vdc

L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

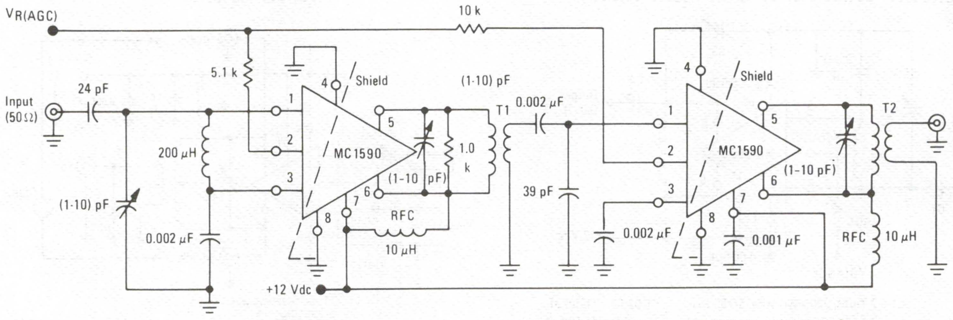
FIGURE 28 – 100 MHz MIXER


VAGC ≈ 6.0 V
Input from
Local Oscillator
(70 MHz)
(1-10) pF
(1-30) pF
4
100
2
IF Output
(30 MHz)
(1-10) pF
5
3
Signal Input
(100 MHz)
MC1590
L2
L1
1
6
7
(1-30) pF
8
+12 Vdc
0.002 μF
0.002 μF
10 μH

L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

TYPICAL APPLICATIONS (continued)

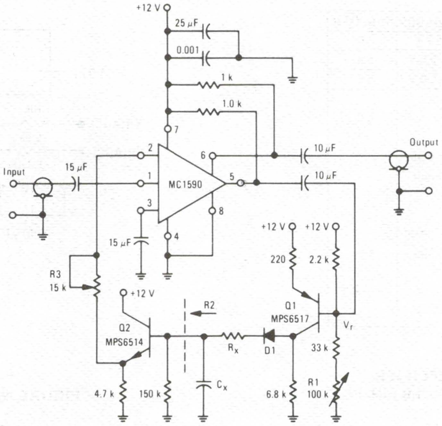
FIGURE 29 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)


VR(AGC)
10 k
5.1 k
Input
(50 Ω)
24 pF
200 μH
(1-10) pF
0.002 μF
4
Shield
1
2
3
MC1590
5
6
7
8
(1-10) pF
1.0 k
(1-10 pF)
RFC
10 μH
T1
0.002 μF
39 pF
+12 Vdc
4
Shield
1
2
3
MC1590
5
6
7
8
0.002 μF
0.001 μF
(1-10 pF)
T2
Output
(50 Ω)
RFC
10 μH

T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4″ ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4″ ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

FIGURE 30 – SPEECH COMPRESSOR


+12 V
25 μF
0.001
1 k
1.0 k
7
2
6
1
5
3
8
4
MC1590
Input
15 μF
10 μF
10 μF
Output
15 μF
R3
15 k
+12 V
+12 V
220
2.2 k
+12 V
R2
Q1
MPS6517
Q2
MPS6514
Rx
D1
Vr
33 k
Cx
4.7 k
150 k
6.8 k
R1
100 k

DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ Volts. The resulting output is filtered by C_x, R_x.

R_x controls the charging time constant or attack time. C_x is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_x small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590 and reduces the gain. R3 controls the slope of signal compression. The following graph (Figure 31) details performance with R3 set to 15 kΩ.

FIGURE 31 – OUTPUT VOLTAGE versus INPUT VOLTAGE

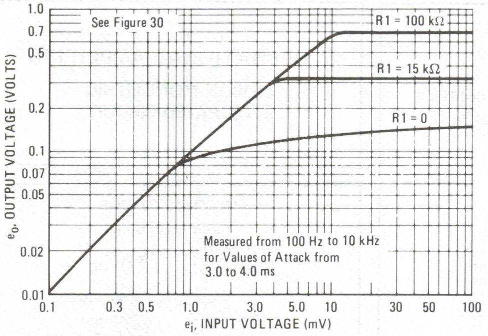


FIGURE 32 – OUTPUT CURRENT, CURRENT MATCH AND I_{CC} FIXTURE

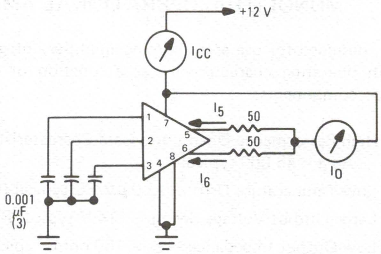


TABLE I – DISTORTION versus FREQUENCY

FREQUENCY	DISTORTION		DISTORTION	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Note: (1) Decay = 300 ms
Attack = 20 ms
(2) C_X = 7.5 µF
R_X = 0 (Short)
(3) Decay = 20 ms
Attack = 3 ms
(4) C_X = 0.68 µF
R_X = 1.5 kΩ

MC1709
MC1709A
MC1709C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1709CG	0°C to +70°C	Metal Can
MC1709CU	0°C to +70°C	Ceramic DIP
MC1709CP1	0°C to +70°C	Plastic DIP
MC1709G,AG	−55°C to +125°C	Metal Can
MC1709AU	−55°C to +125°C	Ceramic DIP

MONOLITHIC OPERATIONAL AMPLIFIER

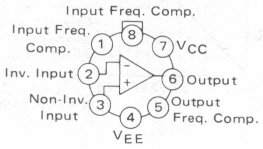
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{vol} = 45,000 typical
- Low Temperature Drift – ±3.0 $\mu V/^{o}C$ typical (MC1709)
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – z_o = 150 ohms typical

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

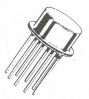
PIN CONNECTIONS



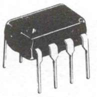
Input Freq. Comp.
Input Freq. Comp.
1
8
7
V_CC
Inv. Input
2
6
Output
Non-Inv. Input
3
4
5
Output Freq. Comp.
V_EE
−
+

(Top View)

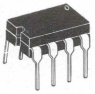
G SUFFIX
METAL PACKAGE
CASE 601-04



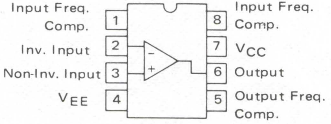
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1709C only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



(Top View)

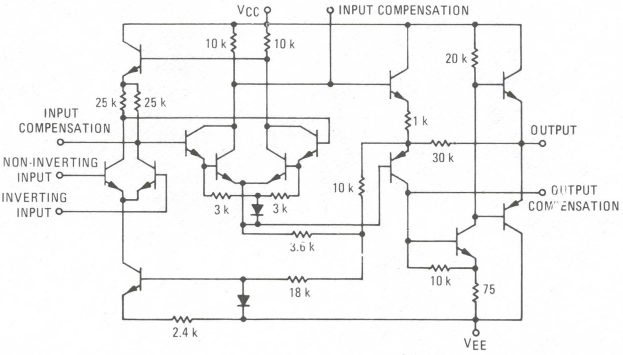


Input Freq. Comp.
1
Inv. Input
2
Non-Inv. Input
3
V_EE
4
8
Input Freq. Comp.
7
V_CC
6
Output
5
Output Freq. Comp.
−
+

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Input Common-Mode Range	V_{ICR}	±10	Volts
Output Load Current	I_L	10	mA
Output Short-Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Packages (MC1709C only)		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Ceramic Dual In-Line Package		750	mW/°C
Derate above T_A = +25°C		6.0	mW/°C
Operating Ambient Temperature Range MC1709A, MC1709 MC1709C	T_A	−55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}		°C
Metal and Ceramic Packages		−65 to +150	
Plastic Packages		−55 to +125	

FIGURE 1 – EQUIVALENT CIRCUIT SCHEMATIC



V_CC
INPUT COMPENSATION
10 k
10 k
20 k
25 k
25 k
INPUT COMPENSATION
NON-INVERTING INPUT
INVERTING INPUT
1 k
OUTPUT
30 k
10 k
3 k
3 k
OUTPUT COMPENSATION
3.6 k
10 k
75
18 k
2.4 k
V_EE

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $9.0\ V \leqslant V_{CC} \leqslant 15\ V$, $-9.0\ V \geqslant V_{EE} \geqslant -15\ V$, $T_A = 25^{o}C$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant 10\ k\Omega$)	V_{IO}	–	0.6	2.0	–	1.0	5.0	mV
Input Offset Current	I_{IO}	–	10	50	–	50	200	nA
Input Bias Current	I_{IB}	–	100	200	–	200	500	nA
Input Resistance	r_i	350	700	–	150	400	–	kΩ
Output Resistance	r_o	–	150	–	–	150	–	Ω
Power Supply Currents ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	I_{CC}, I_{EE}	–	2.5	3.6	–	–	–	mA
Power Consumption ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	P_C	–	75	108	–	80	165	mW
Transient Response ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$) See Figure 8								
Risetime	t_{TLH}	–	–	1.5	–	0.3	1.0	µs
Overshoot	OS	–	–	30	–	10	30	%

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $9.0\ V \leqslant V_{CC} \leqslant 15\ V$, $-9.0\ V \geqslant V_{EE} \geqslant -15\ V$, $T_A = -55^{o}C$ to $+125^{o}C$)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant 10\ k\Omega$)	V_{IO}	–	–	3.0	–	–	6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
($R_S = 50\ \Omega$, $T_A = 25^{o}C$ to $125^{o}C$)		–	1.8	10	–	–	–	
($R_S = 50\ \Omega$, $T_A = -55^{o}C$ to $25^{o}C$)		–	1.8	10	–	–	–	
($R_S = 50\ \Omega$, $T_A = -55^{o}C$ to $125^{o}C$)		–	–	–	–	3.0	–	
($R_S = 10\ k\Omega$, $T_A = 25^{o}C$ to $125^{o}C$)		–	2.0	15	–	–	–	
($R_S = 10\ k\Omega$, $T_A = -55^{o}C$ to $25^{o}C$)		–	4.8	25	–	–	–	
($R_S = 10\ k\Omega$, $T_A = -55^{o}C$ to $125^{o}C$)		–	–	–	–	6.0	–	
Input Offset Current	I_{IO}							nA
($T_A = -55^{o}C$)		–	40	250	–	100	500	
($T_A = 125^{o}C$)		–	3.5	50	–	20	200	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
($T_A = -55^{o}C$ to $25^{o}C$)		–	0.45	2.8	–	–	–	
($T_A = 25^{o}C$ to $125^{o}C$)		–	0.08	0.5	–	–	–	
Input Bias Current ($T_A = -55^{o}C$)	I_{IB}	–	300	600	–	500	1500	nA
Input Resistance ($T_A = -55^{o}C$)	r_i	85	170	–	40	100	–	kΩ
Input Common-Mode Voltage Range ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leqslant 10\ k\Omega$)	CMRR	80	110	–	70	90	–	dB
Supply Voltage Rejection Ratio ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$, $R_S \leqslant 10\ k\Omega$)	PSRR	–	40	100	–	25	150	µV/V
Large Signal Voltage Gain ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$, $R_L \geqslant 2.0\ k\Omega$, $V_O = \pm 15\ V$)	A_V	25	45	70	25	45	70	V/mV
Output Voltage Range ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	V_{OR}							V
($R_L \geqslant 10\ k\Omega$)		±12	±14	–	±12	±14	–	
($R_L \geqslant 2.0\ k\Omega$)		±10	±13	–	±10	±13	–	
Power Supply Currents ($V_{CC} = 15\ V$, $V_{EE} = -15\ V$)	I_{CC}/I_{EE}							mA
($T_A = -55^{o}C$)		–	2.7	4.5	–	–	–	
($T_A = 125^{o}C$)		–	2.1	3.0	–	–	–	
Power Consumption ($V_{CC} = 15$, $V_{EE} = -15\ V$)	P_C							mW
($T_A = -55^{o}C$)		–	81	135	–	–	–	
($T_A = 125^{o}C$)		–	63	90	–	–	–	

ELECTRICAL CHARACTERISTICS (unless otherwise ntoed, V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ, 9.0 V ⩽ 15 V, −9.0 V ⩾ V_{EE} ⩾ −15 V)	V_{IO}	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	100	500	nA
Input Bias Current	I_{IB}	–	300	1500	nA
Input Resistance	r_i	50	250	–	kΩ
Output Resistance	r_o	–	150	–	Ω
Power Consumption	P_C	–	80	200	mW
Large Signal Voltage Gain ($R_L \geqslant 2.0$ kΩ, V_O = ±10 V)	A_V	15	45	–	V/mV
Output Voltage Range	V_{OR}				V
($R_L \geqslant 10$ kΩ)		±12	±14	–	
($R_L \geqslant 2.0$ kΩ)		±10	±13	–	
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leqslant 10$ kΩ)	CMRR	65	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ kΩ)	PSRR	–	25	200	µV/V
Transient Response See Figure 8					
Rise Time	t_{TLH}	–	0.3	–	µs
Overshoot	OS	–	10	–	%

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 15 V, V_{EE} = −15 V, T_A = 0°C to 70°C)

Parameter	Symbol	MC1709C Min	MC1709C Typ	MC1709C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ, 9.0 V ⩽ V_{CC} ⩽ 15 V, −9.0 V ⩾ V_{EE} ⩾ 15 V)	V_{IO}	–	–	10	mV
Input Offset Current	I_{IO}	–	–	750	nA
Input Bias Current	I_{IB}	–	–	2.0	µA
Large Signal Voltage Gain ($R_L \geqslant 2.0$ kΩ, V_O = ±10 V)	A_V	12	–	–	V/mV
Input Resistance	ri	35	–	–	kΩ

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C)

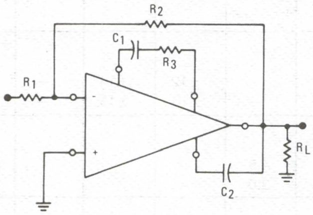


Fig. No.	Curve No.	Test Conditions R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

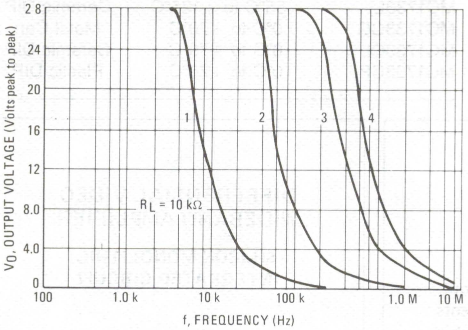


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

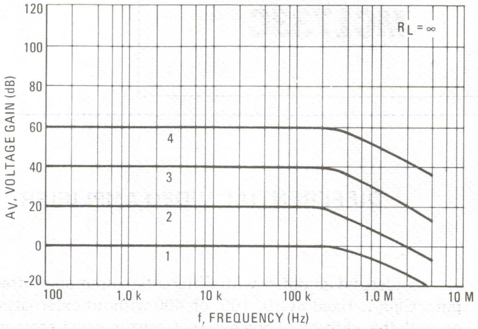


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

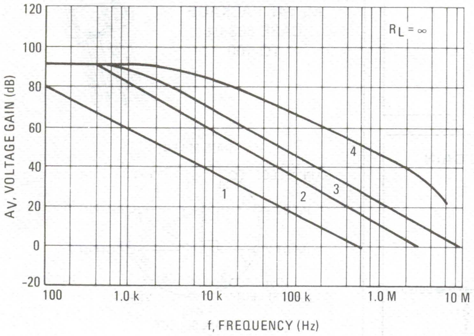


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

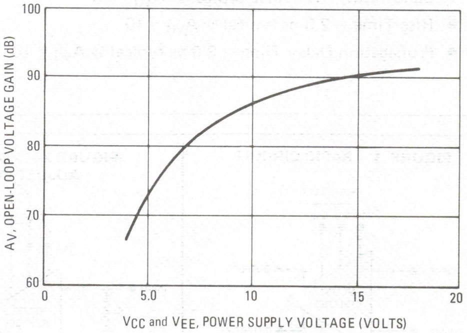


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

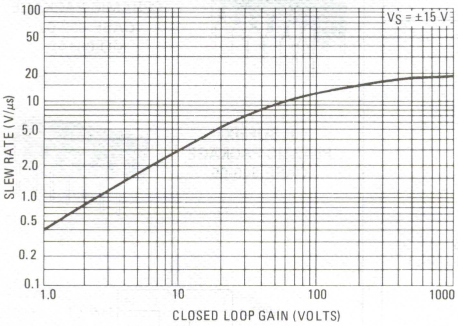
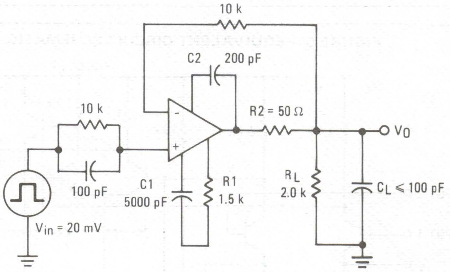


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT


10 k
C2
200 pF
10 k
R2 = 50 Ω
VO
100 pF
C1
5000 pF
R1
1.5 k
RL
2.0 k
CL ≤ 100 pF
Vin = 20 mV

MC1733
MC1733C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1733G	−55°C to +125°C	Metal Can
MC1733L	−55°C to +125°C	Ceramic DIP
MC1733CG	0°C to +70°C	Metal Can
MC1733CL	0°C to +70°C	Ceramic DIP
MC1733CP	0°C to +70°C	Plastic DIP

DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @ A_{vd} = 10
- Rise Time – 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time – 3.6 ns typical @ A_{vd} = 10

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – BASIC CIRCUIT

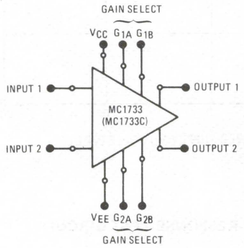

GAIN SELECT
VCC G1A G1B
INPUT 1
INPUT 2
MC1733 (MC1733C)
OUTPUT 1
OUTPUT 2
VEE G2A G2B
GAIN SELECT

FIGURE 2 – VOLTAGE GAIN ADJUST CIRCUIT

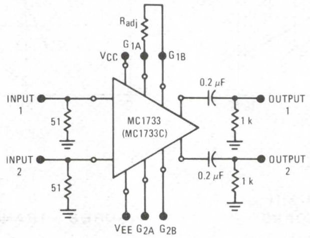
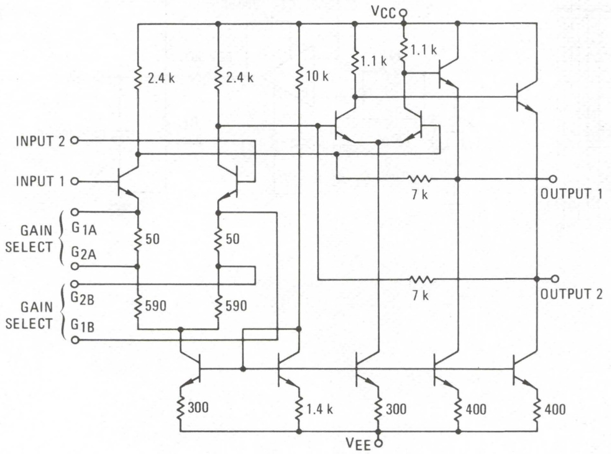
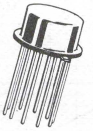
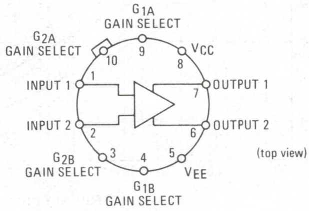

Radj
G1A
VCC
G1B
INPUT 1
51
INPUT 2
51
MC1733 (MC1733C)
0.2 μF
OUTPUT 1
1 k
0.2 μF
OUTPUT 2
1 k
VEE G2A G2B

FIGURE 3 – EQUIVALENT CIRCUIT SCHEMATIC

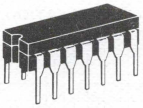

VCC
2.4 k
2.4 k
10 k
1.1 k
1.1 k
INPUT 2
INPUT 1
7 k
OUTPUT 1
GAIN SELECT
G1A
G2A
50
50
7 k
OUTPUT 2
GAIN SELECT
G2B
G1B
590
590
300
1.4 k
300
400
400
VEE

G SUFFIX
METAL PACKAGE
CASE 603-04
TO-100



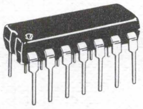

G1A GAIN SELECT
G2A GAIN SELECT
VCC
INPUT 1
OUTPUT 1
INPUT 2
OUTPUT 2
G2B GAIN SELECT
VEE
G1B GAIN SELECT
1
2
3
4
5
6
7
8
9
10
(top view)

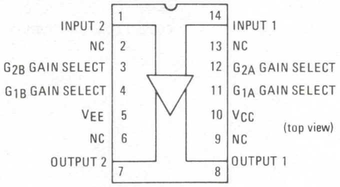
(Top View)



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

P SUFFIX
PLASTIC PACKAGE
CASE 646-05




INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
VEE 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 VCC
9 NC
8 OUTPUT 1
(top view)

(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 −8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	V_{ICM}	±6.0	Volts
Output Current	I_O	10	mA
Internal Power Dissipation (Note 1)	P_D		
Metal Can Package		500	mW
Ceramic Dual In-Line Package		500	
Operating Temperature Range MC1733C MC1733	T_A	0 to +70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, at T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1733			MC1733C			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		300	400	500	250	400	600	
Gain 2 (Note 3)		90	100	110	80	100	120	
Gain 3 (Note 4)		9.0	10	11	8.0	10	12	
Bandwidth (R_s = 50 Ω)	BW							MHz
Gain 1		–	40	–	–	40	–	
Gain 2		–	90	–	–	90	–	
Gain 3		–	120	–	–	120	–	
Rise Time (R_s = 50 Ω, V_O = 1 Vp-p)	t_{TLH} t_{THL}							ns
Gain 1		–	10.5	–	–	10.5	–	
Gain 2		–	4.5	10	–	4.5	12	
Gain 3		–	2.5	–	–	2.5	–	
Propagation Delay (R_s = 50 Ω, V_O = 1 Vp-p)	t_{PLH} t_{PHL}							ns
Gain 1		–	7.5	–	–	7.5	–	
Gain 2		–	6.0	10	–	6.0	10	
Gain 3		–	3.6	–	–	3.6	–	
Input Resistance	R_{in}							kΩ
Gain 1		–	4.0	–	–	4.0	–	
Gain 2		20	30	–	10	30	–	
Gain 3		–	250	–	–	250	–	
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	0.4	3.0	–	0.4	5.0	µA
Input Bias Current (Gain 3)	I_{IB}	–	9.0	20	–	9.0	30	µA
Input Noise Voltage (R_s = 50 Ω, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	µV(rms)
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio	CMRR							dB
Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)		60	86	–	60	86	–	
Gain 2 (V_{CM} = ±1 V, f = 5 MHz)		–	60	–	–	60	–	
Supply Voltage Rejection Ratio	PSRR							dB
Gain 2 (ΔV_s = ±0.5 V)		50	70	–	50	70	–	
Output Offset Voltage	V_{OO}							V
Gain 1		–	0.6	1.5	–	0.6	1.5	
Gain 2 and Gain 3		–	0.35	1.0	–	0.35	1.5	
Output Common-Mode Voltage (Gain 3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing (Gain 2)	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current (Gain 2)	I_D	–	18	24	–	18	24	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, at T_A = T_{high} to T_{low} unless otherwise noted.)*

		MC1733			MC1733C			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		200	–	600	250	–	600	
Gain 2 (Note 3)		80	–	120	80	–	120	
Gain 3 (Note 4)		8.0	–	12	8.0	–	12	
Input Resistance Gain 2	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3)	$\lvert I_{IO} \rvert$	–	–	5.0	–	–	6.0	µA
Input Bias Current (Gain 3)	I_{IB}	–	–	40	–	–	40	µA
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ⩽ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage	V_{OO}							V
Gain 1		–	–	1.5	–	–	1.5	
Gain 2 and Gain 3		–	–	1.2	–	–	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	–	–	2.5	–	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.2	–	–	2.5	–	–	mA
Power Supply Current (Gain 2)	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for MC1733C, −55°C for MC1733
T_{high} = +70°C for MC1733C, +125°C for MC1733.

NOTES

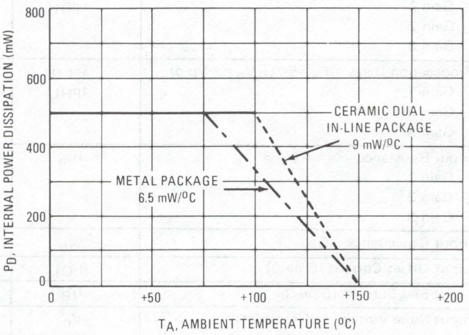
Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.

Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

Note 4: All Gain Select pins open.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

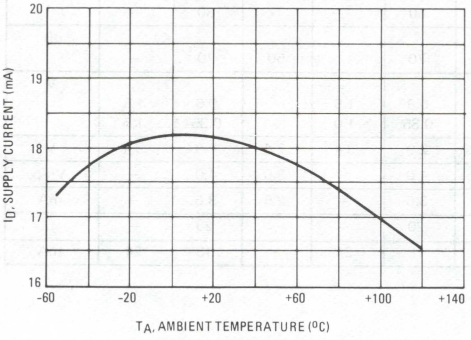
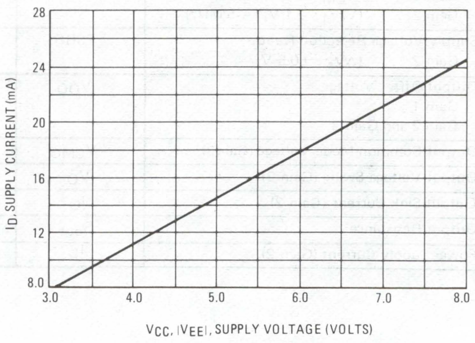


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = –6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 7 – GAIN versus TEMPERATURE

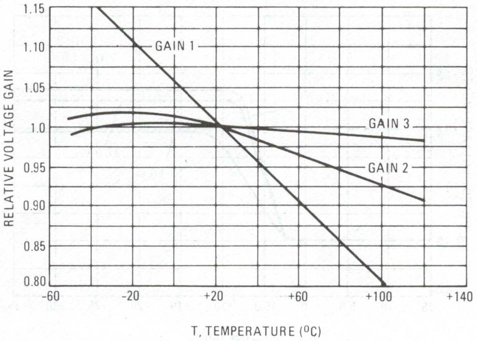


FIGURE 8 – GAIN versus FREQUENCY

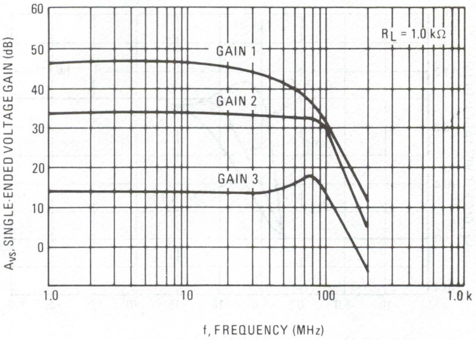


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

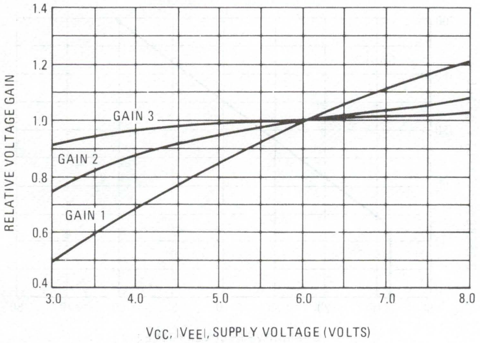


FIGURE 10 – GAIN versus R_{ADJUST}

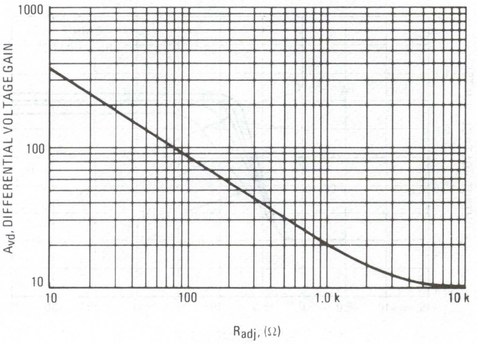


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

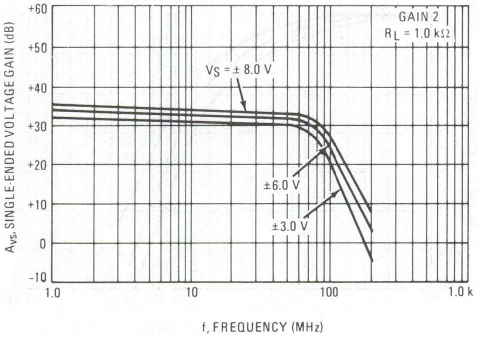
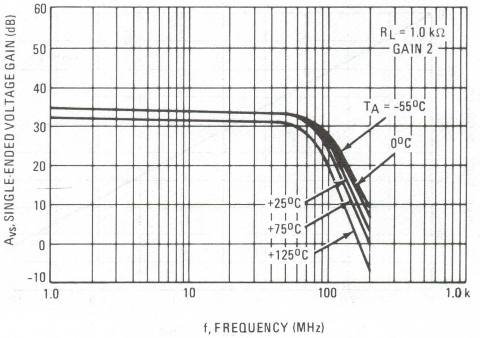


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 — PULSE RESPONSE versus GAIN

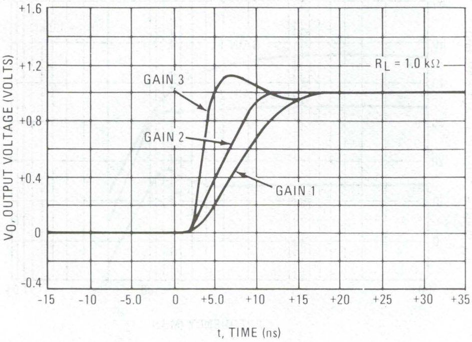


FIGURE 14 — PULSE RESPONSE versus SUPPLY VOLTAGE

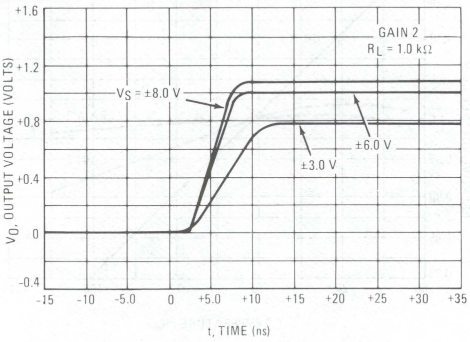


FIGURE 15 — PULSE RESPONSE versus TEMPERATURE

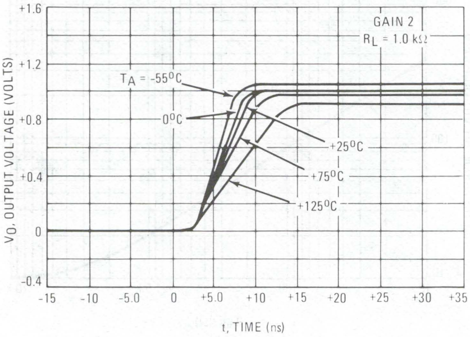


FIGURE 16 — DIFFERENTIAL OVERDRIVE RECOVERY TIME

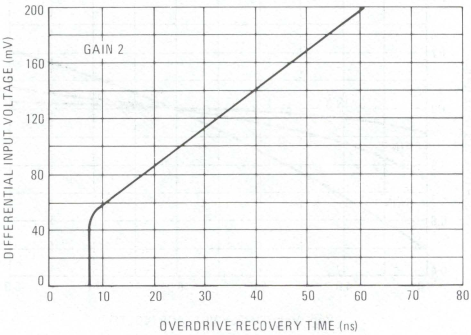


FIGURE 17 — PHASE SHIFT versus FREQUENCY

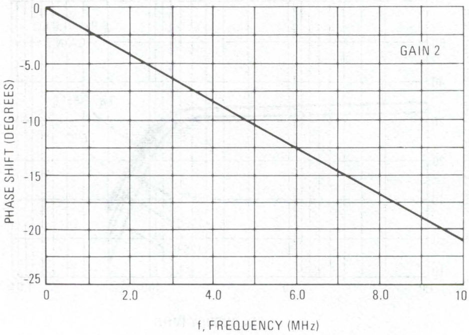
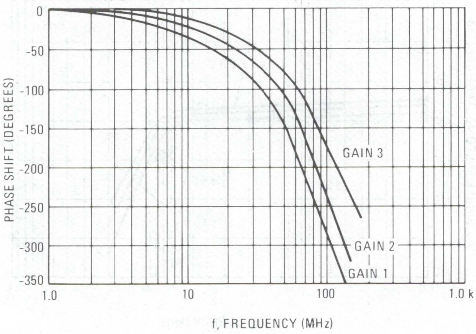


FIGURE 18 — PHASE SHIFT versus FREQUENCY



TYPICAL CHARACTERISTICS (Continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

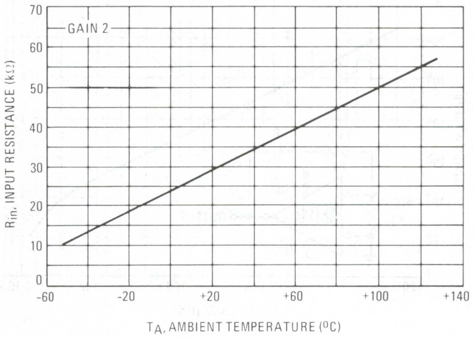


FIGURE 20 – INPUT NOISE VOLTAGE

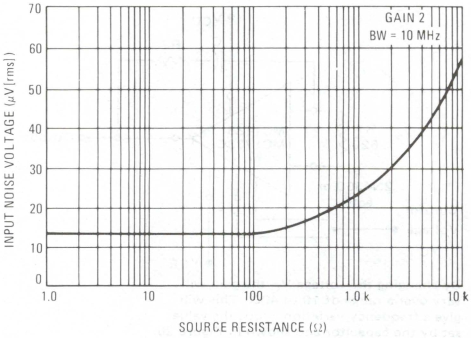


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

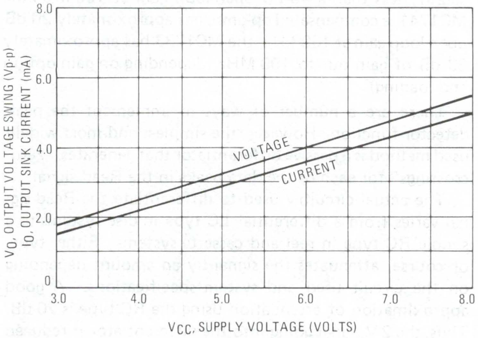


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

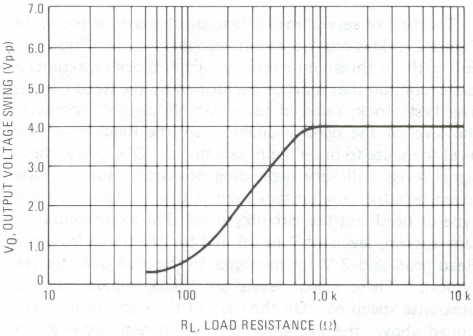


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

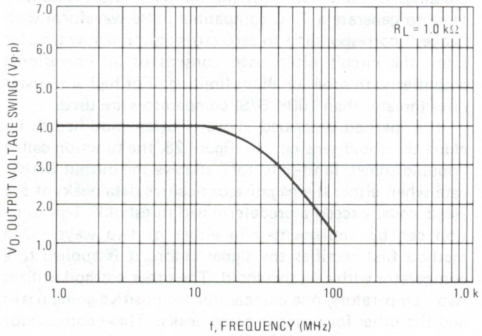
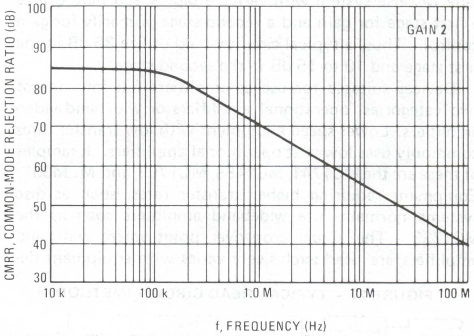
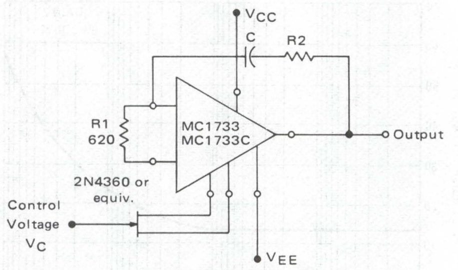


FIGURE 24 – COMMON-MODE REJECTION RATIO



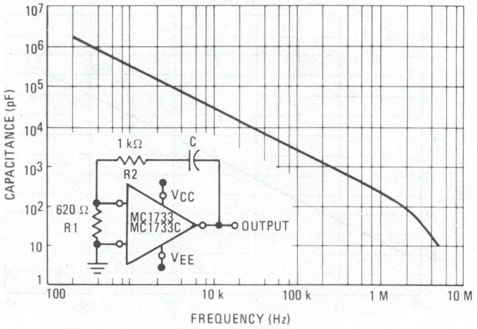
APPLICATIONS INFORMATION

FIGURE 25 – VOLTAGE CONTROLLED OSCILLATOR



By changing the voltage V_C the gain will vary over a range of 10 to 400. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

FIGURE 26 – OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



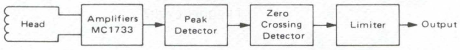
TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplfiication", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

FIGURE 27 – TYPICAL READ CIRCUIT (METHOD 1)



There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

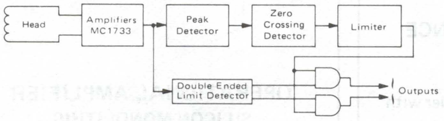
The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

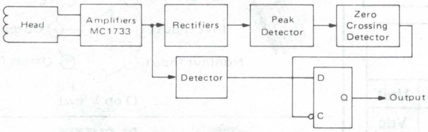
APPLICATIONS INFORMATION (continued)

FIGURE 28 – READ CIRCUIT (METHOD 2)


Head
Amplifiers MC1733
Peak Detector
Zero Crossing Detector
Limiter
Double Ended Limit Detector
Outputs

Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 – READ CIRCUIT (METHOD 3)

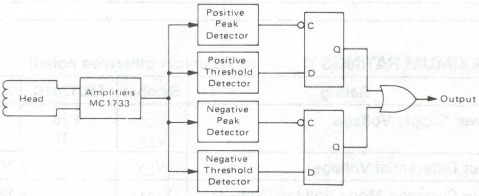

Head
Amplifiers MC1733
Rectifiers
Peak Detector
Zero Crossing Detector
Detector
D
Q
C
Output

The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 – READ CIRCUIT (Method 4)


Positive Peak Detector
Positive Threshold Detector
Negative Peak Detector
Negative Threshold Detector
Head
Amplifiers MC1733
C
Q
D
C
Q
D
Output

MC1741, MC1741C
MC1741N, MC1741NC

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CG	LM741CD, μA741HC	0°C to +70°C	Metal Can
MC1741CP1	LM741CN, μA741TC	0°C to +70°C	Plastic DIP
MC1741NCP1	—	0°C to +70°C	Plastic DIP
MC1741CU,NCU	—	0°C to +70°C	Ceramic DIP
MC1741G,NG	—	−55°C to +125°C	Metal Can
MC1741U,NU	—	−55°C to +125°C	Ceramic DIP
MC1741NCG	—	0°C to +70°C	Metal Can

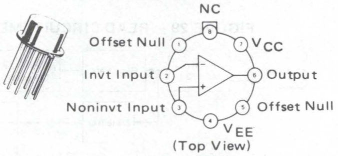
INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

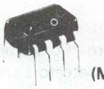
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered — N Suffix

OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

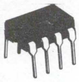
G SUFFIX
METAL PACKAGE
CASE 601-04

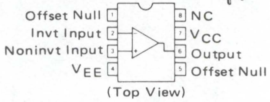

NC
Offset Null 1
8
7 VCC
Invt Input 2
6 Output
Noninvt Input 3
5 Offset Null
4
VEE
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1741C, MC1741NC)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



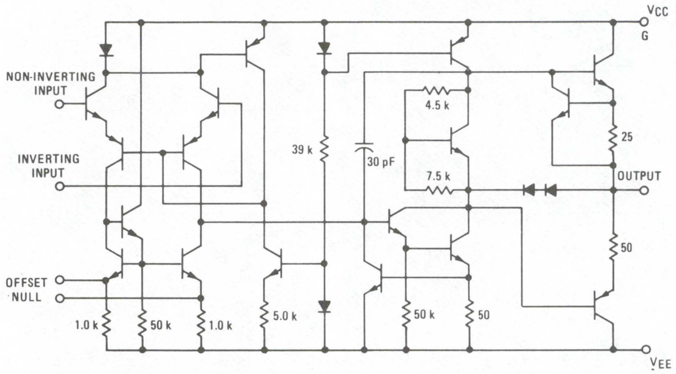

Offset Null 1
Invt Input 2
Noninvt Input 3
VEE 4
8 NC
7 VCC
6 Output
5 Offset Null
(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	+22 −22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	−55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 −55 to +125		°C

Note 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC


VCC
G
NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
1.0 k
50 k
1.0 k
5.0 k
39 k
30 pF
4.5 k
7.5 k
50 k
50
25
OUTPUT
50
VEE

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geqslant 2.0$ k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leqslant 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k)	PSRR	–	30	150	–	30	150	µV/V
Output Voltage Swing	V_O							V
($R_L \geqslant 10$ k)		±12	±14	–	±12	±14	–	
($R_L \geqslant 2$ k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	–	50	85	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	µs
(V_I = 20 mV, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high} unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leqslant 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k)	PSRR	–	30	150	–	–	–	µV/V
Output Voltage Swing	V_O							V
($R_L \geqslant 10$ k)		±12	±14	–	–	–	–	
($R_L \geqslant 2$ k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain ($R_L \geqslant 2$ k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Supply Currents	I_D							mA
(T_A = 125°C)		–	1.5	2.5	–	–	–	
(T_A = -55°C)		–	2.0	3.3	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	45	75	–	–	–	mW
(T_A = -55°C)		–	60	100	–	–	–	

*T_{high} = 125°C for MC1741 and 70°C for MC1741C
T_{low} = -55°C for MC1741 and 0°C for MC1741C

NOISE CHARACTERISTICS (Applies for MC1741N and MC1741NC only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = +25°C)

Characteristic	Symbol	MC1741N			MC1741NC			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 k) (Input Referenced)	E_n	–	–	20	–	–	20	µV/peak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

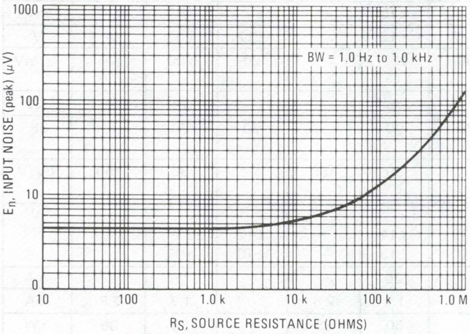


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

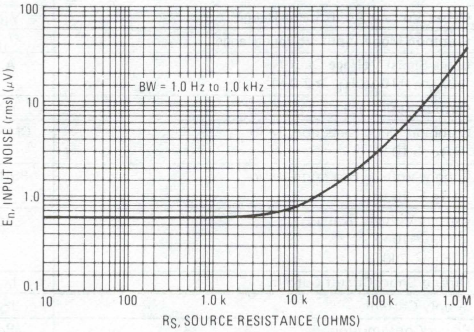


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

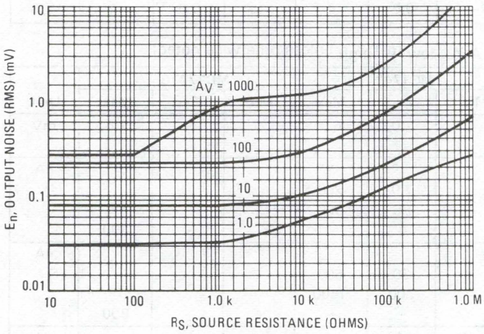


FIGURE 4 – SPECTRAL NOISE DENSITY

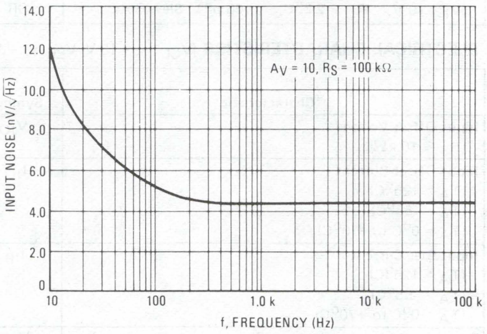
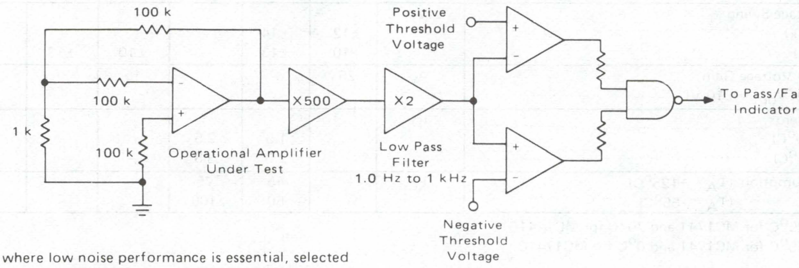


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



100 k
100 k
1 k
100 k
-
+
Operational Amplifier Under Test
X500
X2
Low Pass Filter 1.0 Hz to 1 kHz
Positive Threshold Voltage
+
-
+
-
To Pass/Fail Indicator
Negative Threshold Voltage

For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 µV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

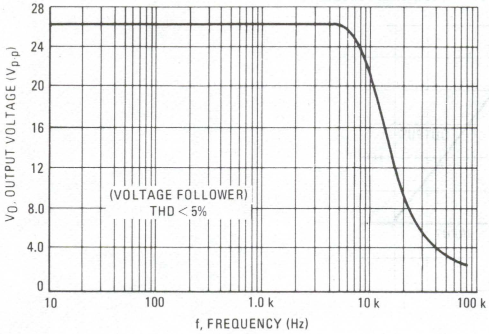


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

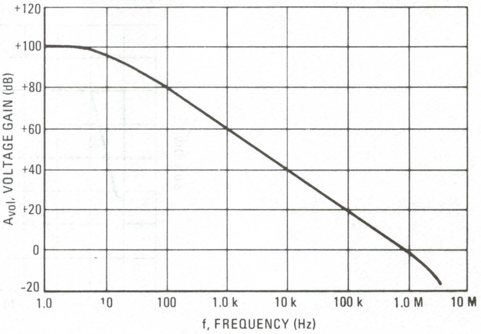


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

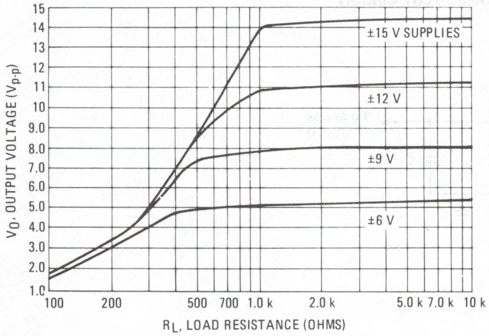


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

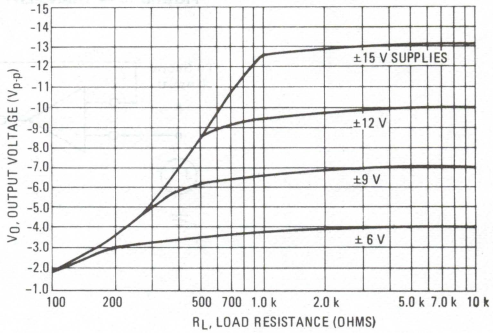


FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)

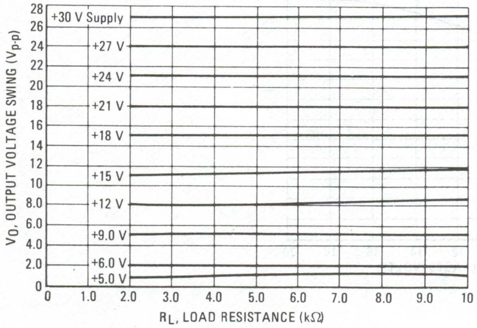


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

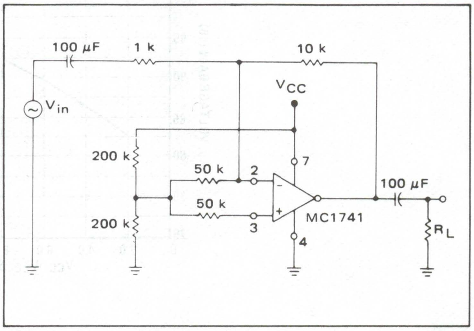

100 μF
1 k
10 k
V_{in}
V_{CC}
200 k
50 k
2
7
50 k
3
200 k
−
+
MC1741
4
100 μF
R_L

FIGURE 12 — NONINVERTING PULSE RESPONSE

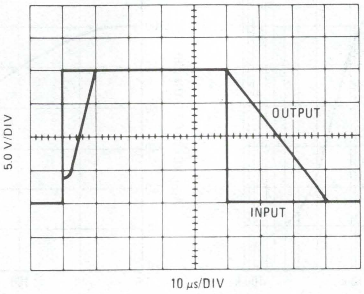


FIGURE 13 — TRANSIENT REPONSE TEST CIRCUIT

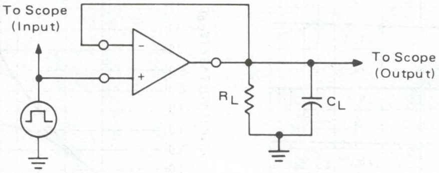
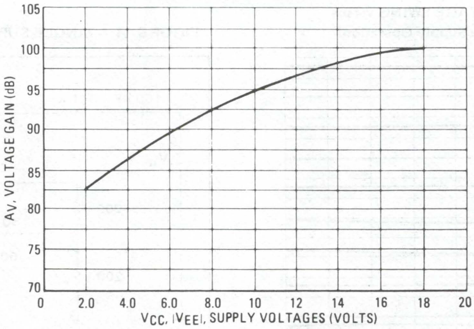

To Scope
(Input)
−
+
To Scope
(Output)
R_L
C_L

FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



MC1741S
MC1741SC

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	−55°C to +125°C	Metal Can
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1	0°C to +70°C	Plastic DIP

HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

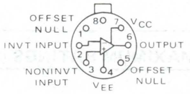
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

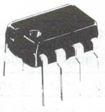
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

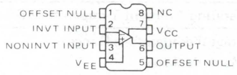
G SUFFIX
METAL PACKAGE
CASE 601-04


OFFSET NULL
INVT INPUT
NONINVT INPUT
VEE
OFFSET NULL
OUTPUT
VCC
1
2
3
4
5
6
7
8

(Top View)

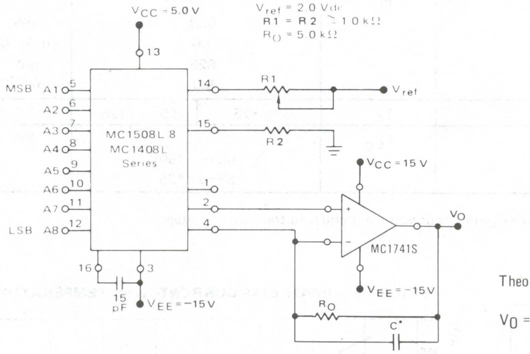


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04


OFFSET NULL
INVT INPUT
NONINVT INPUT
VEE
NC
VCC
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

(Top View)

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


VCC = 5.0 V
Vref = 2.0 Vdc
R1 = R2 ≅ 1.0 kΩ
RO = 5.0 kΩ
13
MSB
A1
A2
A3
A4
A5
A6
A7
LSB
A8
5
6
7
8
9
10
11
12
MC1508L 8
MC1408L
Series
14
R1
Vref
15
R2
1
2
4
VCC = 15 V
VO
MC1741S
VEE = −15 V
16
3
15 pF
VEE = −15 V
RO
C*

Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

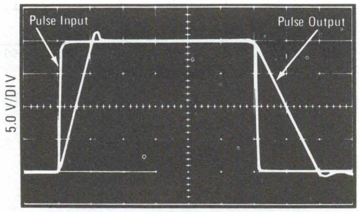
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

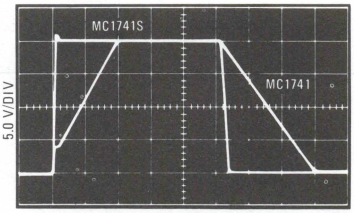
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

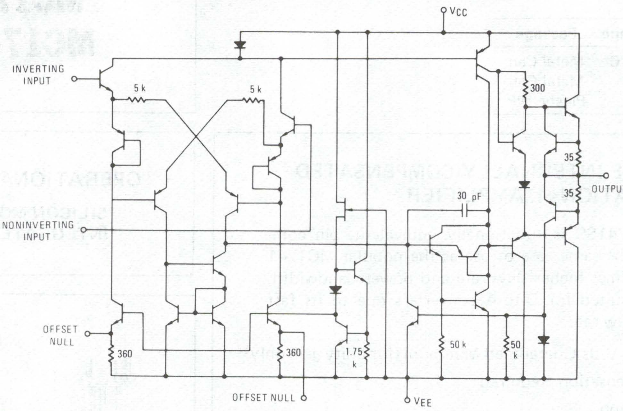
MC1741S LARGE-SIGNAL TRANSIENT RESPONSE



STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



CIRCUIT SCHEMATIC


VCC
INVERTING INPUT
5 k
5 k
300
35
OUTPUT
30 pF
35
NONINVERTING INPUT
OFFSET NULL
360
360
1.75 k
50 k
50 k
OFFSET NULL
VEE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MC1741SC	Value MC1741S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0		 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

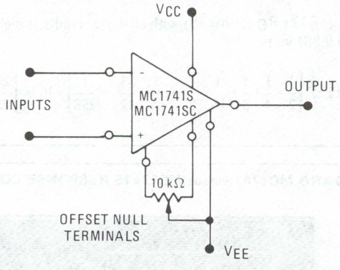
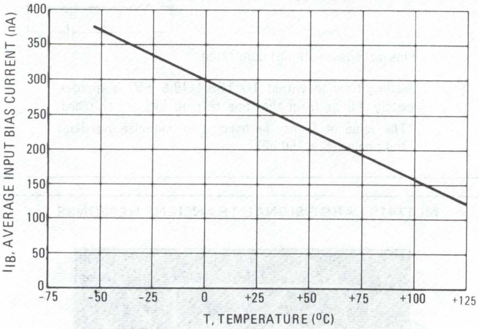

VCC
INPUTS
-
+
MC1741S
MC1741SC
OUTPUT
10 kΩ
OFFSET NULL TERMINALS
VEE

FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S			MC1741SC			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3)	BW_P							kHz
$A_v = 1$, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)		150	200	–	150	200	–	
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(-) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(–)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4)	A_{vol}							–
V_O = ±10 V, T_A = +25°C		50,000	200,000	–	20,000	100,000	–	
V_O = ±10 V, T_A = T_{low}* to T_{high}*		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only)		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}							nA
T_A = +25°C and T_{high}		–	200	500	–	200	500	
T_A = T_{low}		–	500	1500	–	–	800	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C and T_{high}		–	30	200	–	30	200	
T_A = T_{low}		–	–	500	–	–	300	
Input Offset Voltage (R_S = ≤10 kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	1.0	5.0	–	2.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2.0	100	–	2.0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS−	–	10	150	–	10	150	µV/V

*T_{low} = 0 for MC1741SC
= −55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

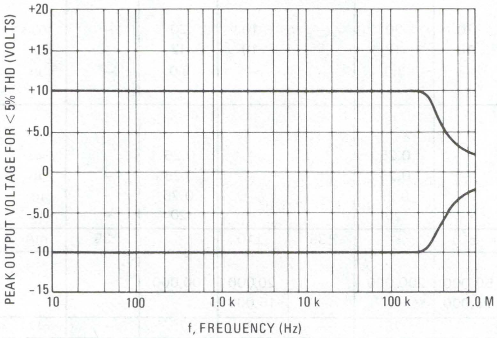


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

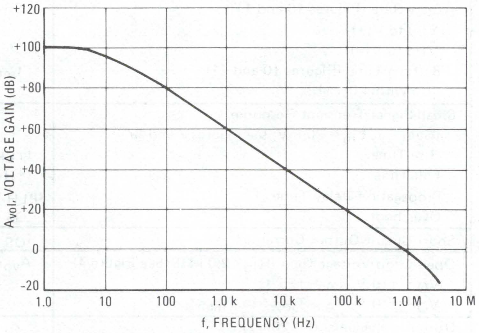


FIGURE 5 – NOISE versus FREQUENCY

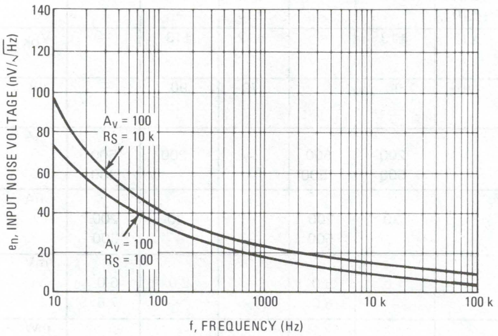


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

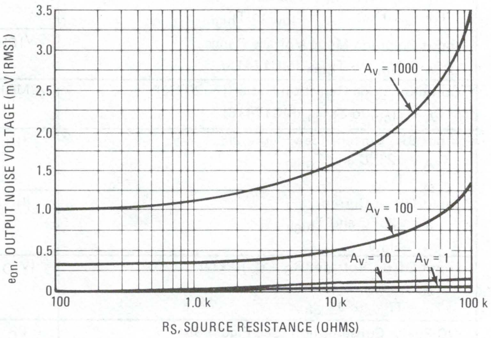


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

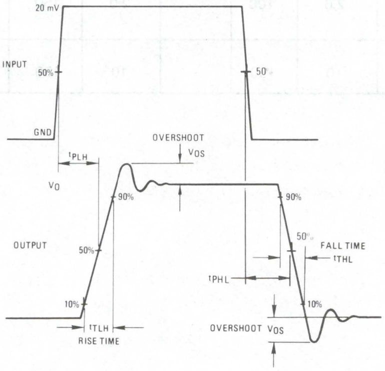
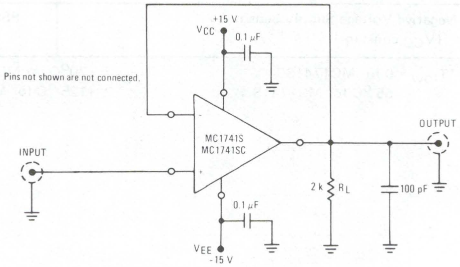

20 mV
INPUT
50%
50%
GND
OVERSHOOT
VOS
tPLH
VO
90%
90%
OUTPUT
50%
50%
FALL TIME
tTHL
tPHL
10%
10%
tTLH
RISE TIME
OVERSHOOT
VOS

FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


+15 V
VCC
0.1 µF
Pins not shown are not connected.
-
+
MC1741S
MC1741SC
OUTPUT
INPUT
2 k
RL
100 pF
0.1 µF
VEE
-15 V

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

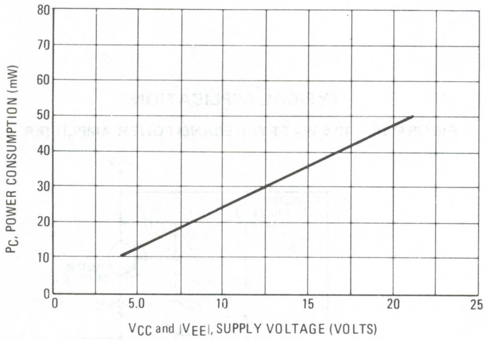
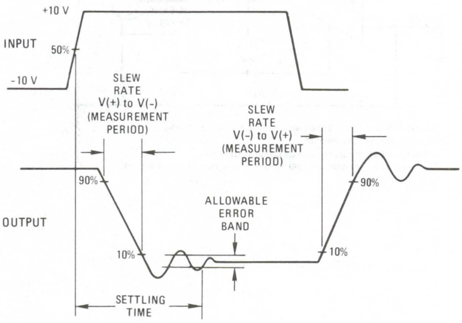
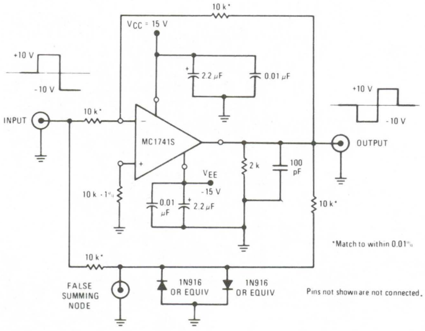


FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS



+10 V
INPUT
50%
-10 V
SLEW RATE V(+) to V(-) (MEASUREMENT PERIOD)
SLEW RATE V(-) to V(+) (MEASUREMENT PERIOD)
90%
90%
ALLOWABLE ERROR BAND
OUTPUT
10%
10%
SETTLING TIME

FIGURE 11 – SETTLING TIME AND SLEW RATE TEST CIRCUIT



*Match to within 0.01%

Pins not shown are not connected.

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

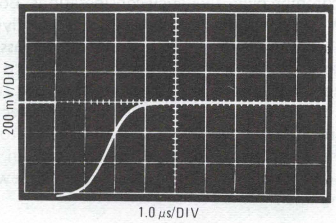
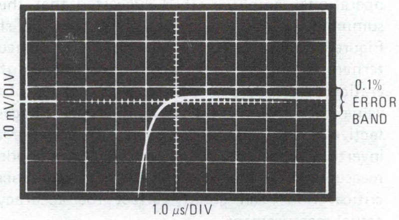
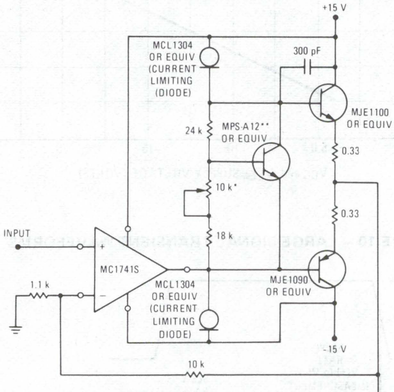


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER


+15 V
MCL1304 OR EQUIV (CURRENT LIMITING (DIODE)
300 pF
MJE1100 OR EQUIV
24 k
MPS-A12** OR EQUIV
0.33
10 k*
0.33
18 k
INPUT
+
MC1741S
−
1.1 k
MCL1304 OR EQUIV (CURRENT LIMITING DIODE)
MJE1090 OR EQUIV
-15 V
10 k
RL

Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

ORDERING INFORMATION

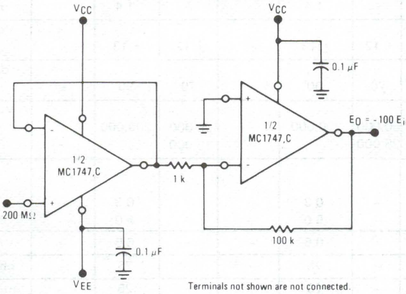
Device	Temperature Range	Package
MC1747G	−55°C to +125°C	Metal Can
MC1747L	−55°C to +125°C	Ceramic DIP
MC1747CG	0°C to +75°C	Metal Can
MC1747CL	0°C to +75°C	Ceramic DIP
MC1747CP2	0°C to +75°C	Plastic DIP

DUAL MC1741 INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the µA747 and µA747C respectively.

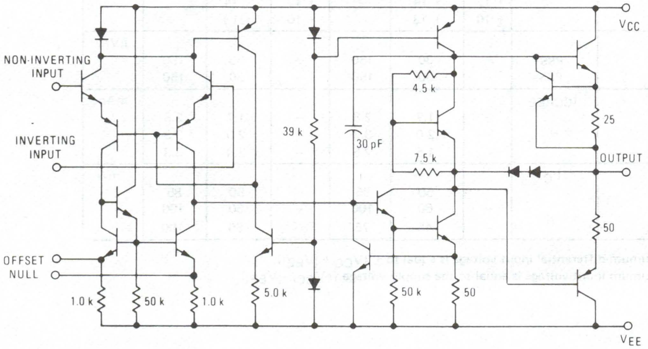
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

FIGURE 1 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER


V_{CC}
V_{CC}
0.1 µF
1/2 MC1747,C
1/2 MC1747,C
$E_O = -100\ E_{in}$
1 k
100 k
E_{in}
$z_i \approx 200\ M\Omega$
0.1 µF
V_{EE}

Terminals not shown are not connected.

FIGURE 2 – CIRCUIT SCHEMATIC


NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
1.0 k
50 k
1.0 k
5.0 k
39 k
30 pF
4.5 k
7.5 k
50 k
50
25
50
V_{CC}
OUTPUT
V_{EE}

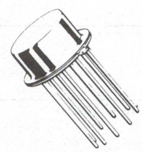
Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent right of Motorola Inc. or others.

MC1747
MC1747C

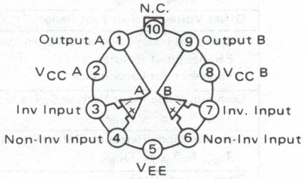
(DUAL MC1741)

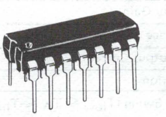
DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

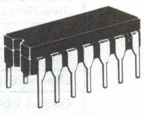


G SUFFIX
METAL PACKAGE
CASE 603-04
TO-100

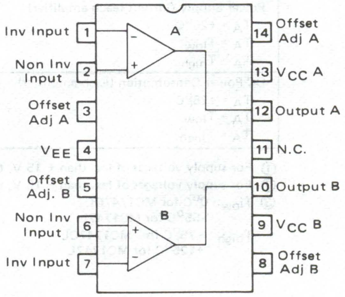

N.C.
10
Output A 1
9 Output B
V_{CC} A 2
8 V_{CC} B
A
B
Inv Input 3
7 Inv. Input
Non-Inv Input 4
6 Non-Inv Input
5
V_{EE}



P2 SUFFIX
PLASTIC PACKAGE
CASE 646-05



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA


Inv Input 1
Non Inv Input 2
Offset Adj A 3
V_{EE} 4
Offset Adj. B 5
Non Inv Input 6
Inv Input 7
14 Offset Adj A
13 V_{CC} A
12 Output A
11 N.C.
10 Output B
9 V_{CC} B
8 Offset Adj B
A
B

V_{CC}A and V_{CC}B are not connected internally.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC}	+22	+18	Vdc
	V_{EE}	−22	−18	
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C
Junction Temperature	T_J			°C
Ceramic and Metal Package		175		
Plastic Package		150		

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

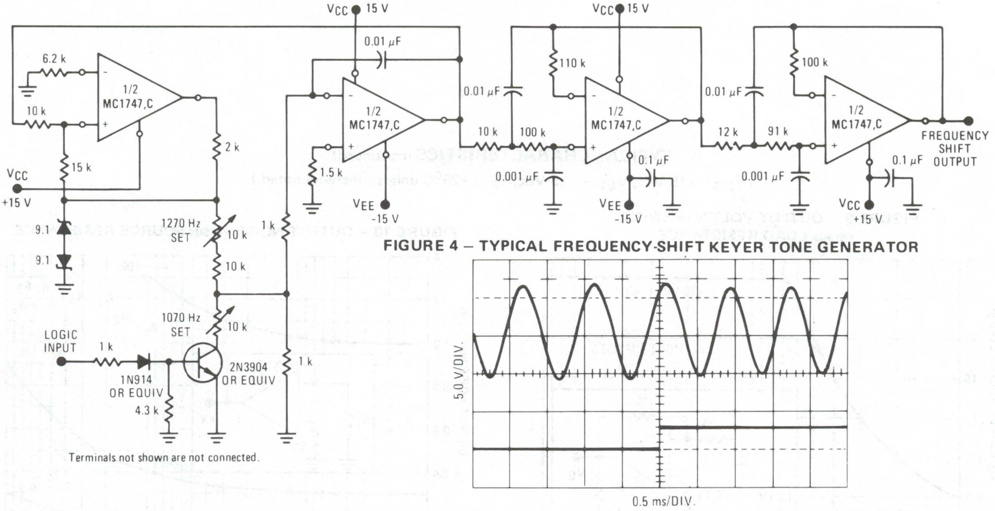
Characteristics	Symbol	MC1747 Min	MC1747 Typ	MC1747 Max	MC1747C Min	MC1747C Typ	MC1747C Max	Unit
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	80	500	–	80	500	
$T_A = T_{high}$ ③		–	30	500	–	30	800	
$T_A = T_{low}$ ③		–	300	1500	–	30	800	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	20	200	–	20	200	
$T_A = T_{high}$		–	7.0	200	–	7.0	300	
$T_A = T_{low}$		–	85	500	–	7.0	300	
Input Offset Voltage ($R_S \leqslant$ 10 kΩ)	V_{IO}							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
$T_A = T_{low}$ to T_{high}		–	1.0	6.0	–	1.0	7.5	
Offset Voltage Adjustment Range		–	± 15	–	–	± 15	–	mV
Differential Input Impedance (Open-loop, f = 20 Hz)								
Parallel Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Parallel Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common-Mode Input Voltage Swing	V_{ICR}							Volts
$T_{low} \leqslant T_A \leqslant T_{high}$		± 12	± 13	–	± 12	± 13	–	
Common-Mode Rejection Ratio (R_S = 10 kΩ)	CMRR							dB
$T_{low} \leqslant T_A \leqslant T_{high}$		70	90	–	70	90	–	
Open-Loop Voltage Gain	A_{vol}							Volts
T_A = +25°C (V_O = ±10 V, R_L = 2.0 kΩ)		50,000	200,000	–	25,000	200,000	–	
$T_A = T_{low}$ to T_{high} (V_O = ±10 V, R_L = 2.0 kΩ)		25,000	–	–	15,000	–	–	
Transient Response (Unity Gain) (V_{in} = 20 mV, R_L = 2.0 kΩ, $C_L \leqslant$ 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate (Unity Gain)	SR	–	0.5	–	–	0.5	–	V/µs
Output Impedance	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{OS}	–	25	–	–	25	–	mAdc
Channel Separation		–	120	–	–	120	–	dB
Output Voltage Swing ($T_{low} \leqslant T_A \leqslant T_{high}$)	V_{OR}							V_{pk}
R_L = 10 kΩ		± 12	± 14	–	± 12	± 14	–	
R_L = 2.0 kΩ		± 10	± 13	–	± 10	± 13	–	
Power Supply Sensitivity (T_{low} to T_{high})								µV/V
V_{EE} = Constant, $R_S \leqslant$ 10 kΩ	PSS+	–	30	150	–	30	150	
V_{CC} = Constant, $R_S \leqslant$ 10 kΩ	PSS-	–	30	150	–	30	150	
Power Supply Current (each amplifier)	I_{CC}, I_{EE}							mAdc
T_A = +25°C		–	1.7	2.8	–	1.7	2.8	
$T_A = T_{low}$		–	2.0	3.3	–	2.0	3.3	
$T_A = T_{high}$		–	1.5	2.5	–	2.0	3.3	
DC Power Consumption (each amplifier)	P_C							mW
T_A = +25°C		–	50	85	–	50	85	
$T_A = T_{low}$		–	60	100	–	60	100	
$T_A = T_{high}$		–	45	75	–	60	100	

① For supply voltages of less than ± 15 V, the maximum differential input voltage is equal to ± (V_{CC} + $|V_{EE}|$).

② For supply voltages of less than ± 15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, −$|V_{EE}|$).

③ T_{low}: 0°C for MC1747CL
−55°C for MC1747L
T_{high}: +75°C for MC1747CL
+125°C for MC1747L

FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT


VCC 15 V
VCC 15 V
0.01 µF
6.2 k
1/2 MC1747,C
10 k
2 k
VCC +15 V
15 k
9.1
9.1
1270 Hz SET
10 k
10 k
1070 Hz SET
10 k
LOGIC INPUT
1 k
1N914 OR EQUIV
4.3 k
2N3904 OR EQUIV
1 k
1 k
1/2 MC1747,C
1.5 k
VEE -15 V
0.01 µF
110 k
10 k
100 k
1/2 MC1747,C
0.001 µF
0.1 µF
VEE -15 V
0.01 µF
100 k
12 k
91 k
1/2 MC1747,C
0.001 µF
0.1 µF
VCC +15 V
FREQUENCY SHIFT OUTPUT

Terminals not shown are not connected.

FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR

5.0 V/DIV.
0.5 ms/DIV.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

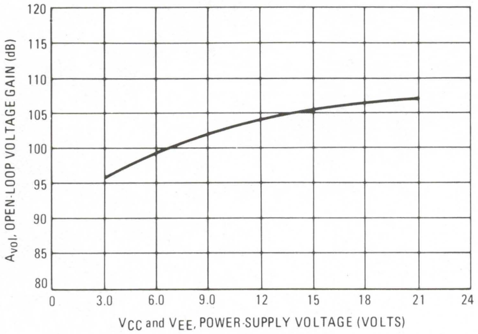


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

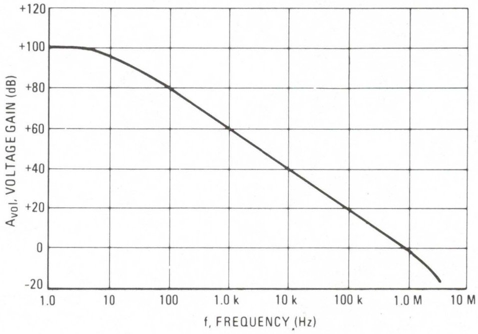


FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

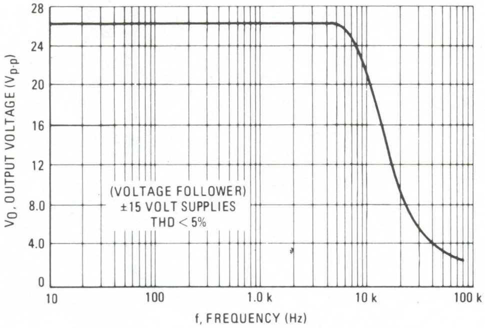
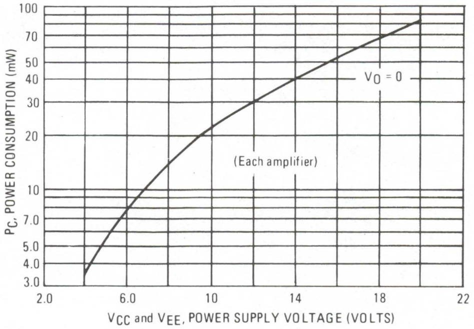


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

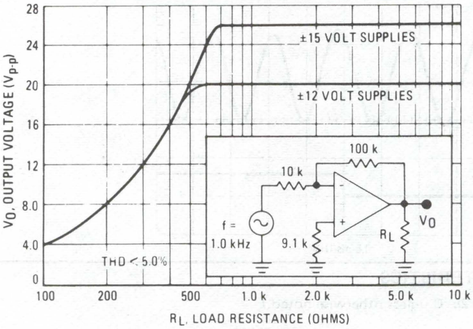
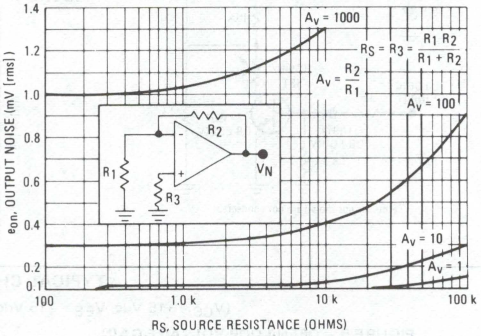


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE



MC1748
MC1748C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1748G	−55°C to +125°C	Metal Can
MC1748U	−55°C to +125°C	Ceramic DIP
MC1748CG	0°C to +70°C	Metal Can
MC1748CP1	0°C to +70°C	Plastic DIP
MC1748CU	0°C to +70°C	Ceramic DIP

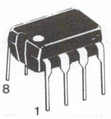
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

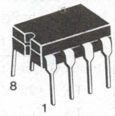
- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

OPERATIONAL AMPLIFIER

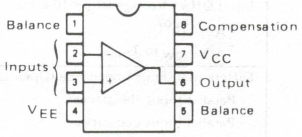
SILICON MONOLITHIC INTEGRATED CIRCUIT



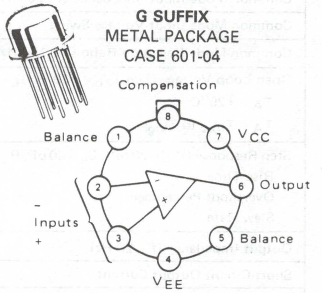
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1748C only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



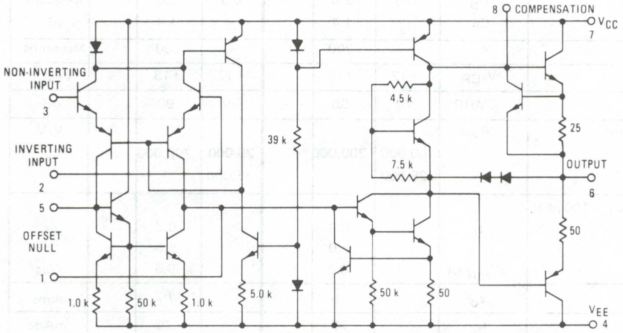
Balance 1
Inputs 2 3
VEE 4
8 Compensation
7 VCC
6 Output
5 Balance



G SUFFIX
METAL PACKAGE
CASE 601-04

Compensation
8
Balance 1
7 VCC
2
6 Output
Inputs
3
5 Balance
4
VEE

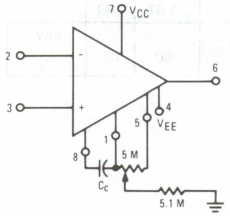
FIGURE 1 – CIRCUIT SCHEMATIC



8 COMPENSATION
VCC 7
NON-INVERTING INPUT 3
INVERTING INPUT 2
5
OFFSET NULL
1
1.0 k
50 k
1.0 k
5.0 k
39 k
4.5 k
7.5 k
50 k
50
25
OUTPUT 6
50
VEE 4

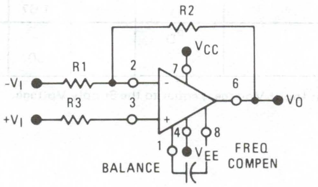
TYPICAL COMPENSATION CIRCUITS

FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION



7 VCC
2
3
6
4
5 VEE
1
8
5 M
Cc
5.1 M

FIGURE 3 – SINGLE-POLE COMPENSATION

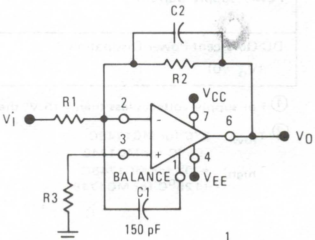


R2
VCC
R1
2
7
−VI
6
R3
3
VO
+VI
4
8
1
VEE
BALANCE
FREQ COMPEN
C1

$$C1 \geq \frac{R1\,C_s}{R1 + R2}$$

$C_s = 30\ pF$

FIGURE 4 – FEEDFORWARD COMPENSATION



C2
R2
R1
VCC
2
7
VI
6
3
VO
1
4
BALANCE
VEE
C1
R3
150 pF

$$C2 = \frac{1}{2\pi f_0 R2}$$

$f_0 = 3.0\ MHz$

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748	MC1748C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_s	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

		MC1748			MC1748C			
Characteristics	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Bias Current	I_{IB}							µAdc
T_A = +25°C		–	0.08	0.5	–	0.08	0.5	
T_A = T_{low} to T_{high} ②		–	0.3	1.5	–	–	0.8	
Input Offset Current	$\|I_{IO}\|$							µAdc
T_A = +25°C		–	0.02	0.2	–	0.02	0.2	
T_A = T_{low} to T_{high}		–	0.08	0.5	–	–	0.3	
Input Offset Voltage ($R_S \le 10$ kΩ)	$\|V_{IO}\|$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f 20 Hz)	z_{in}	–	200	–	–	200	–	Megohms
Common-Mode Input Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_O = ±10 V, R_L = 2.0 k ohms)	A_{vol}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
T_A = T_{low} to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	µs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/µs
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{sc}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms (T_A = T_{low} to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								µV/V
V_{EE} = constant, $R_s \leqslant 10$ k ohms	S+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leqslant 10$ k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation	P_D							mW
(V_o = 0)		–	50	85	–	50	85	

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748C
-55°C for MC1748
T_{high}: +70° for MC1748C
+125°C for MC1748

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – MINIMUM INPUT VOLTAGE RANGE

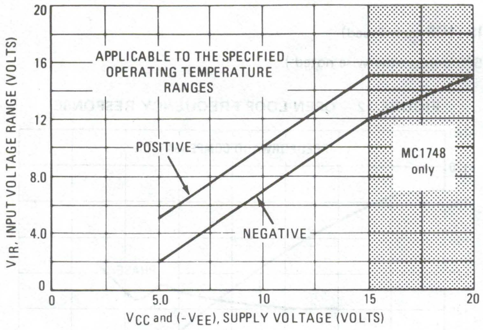


FIGURE 6 – MINIMUM OUTPUT VOLTAGE SWING

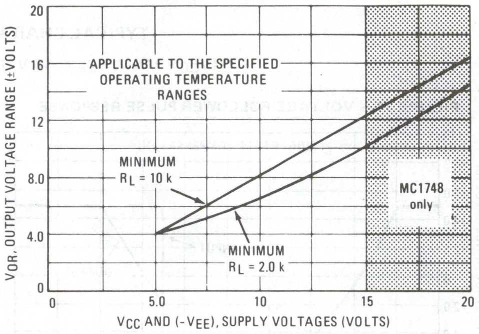


FIGURE 7 – MINIMUM VOLTAGE GAIN

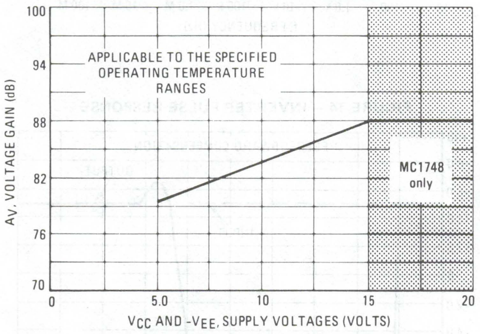


FIGURE 8 – TYPICAL SUPPLY CURRENTS

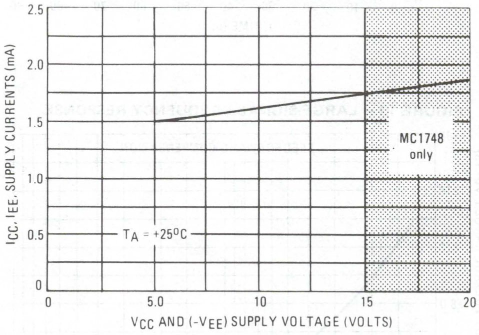


FIGURE 9 – OPEN-LOOP FREQUENCY RESPONSE

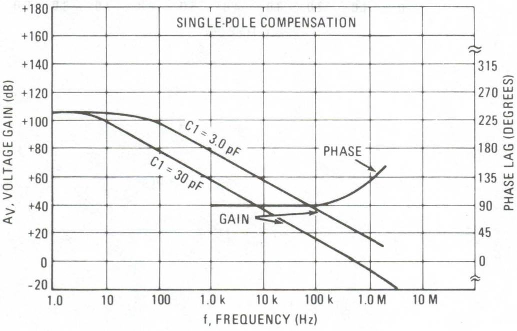
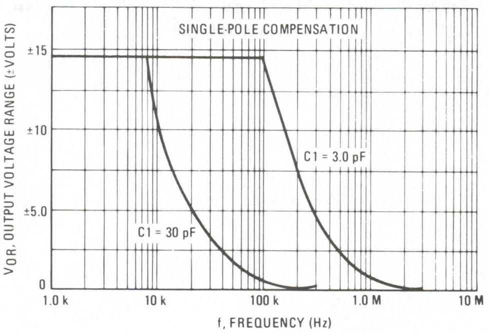


FIGURE 10 – LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

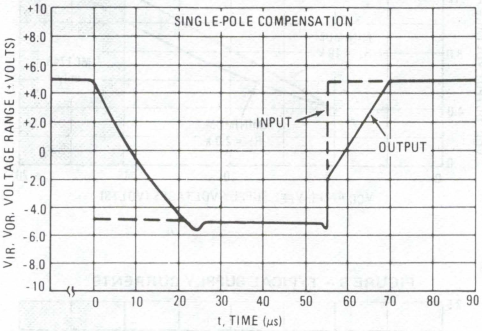


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

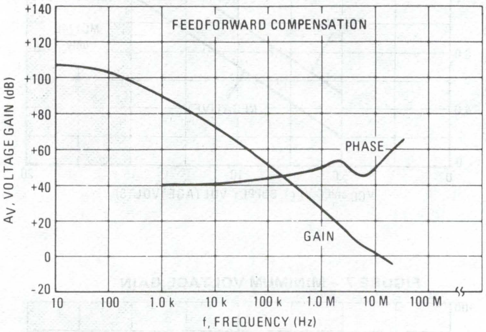


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

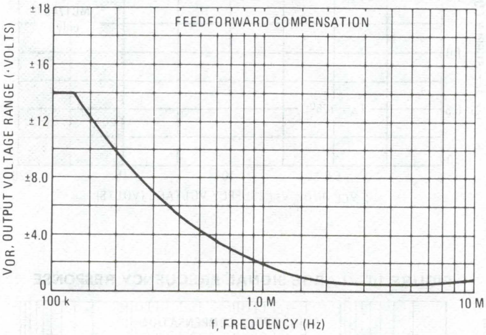
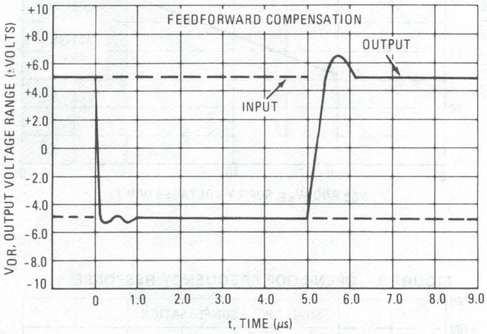


FIGURE 14 – INVERTER PULSE RESPONSE



MOTOROLA

MC1776
MC1776C

Specifications and Applications Information

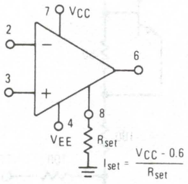
MONOLITHIC MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



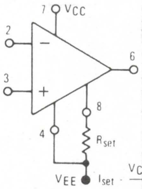
7
VCC
2
3
6
4
8
VEE
Rset

$I_{set} = \frac{V_{CC} - 0.6}{R_{set}}$

Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0V	3.6 MΩ	360 kΩ
±10V	6.2 MΩ	620 kΩ
±12V	7.5 MΩ	750 kΩ
±15V	10 MΩ	1.0 MΩ

R_{set} to NEGATIVE SUPPLY

(Recommended for supply voltage less than ±6.0 V)



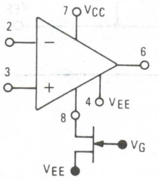
7
VCC
2
3
6
8
4
Rset
VEE

$I_{set} = \frac{V_{CC} - 0.6 - V_{EE}}{R_{set}}$

Typical R_{set} Values		
V_{CC}, V_{EE}	Iset = 1.5 µA	I_{set} = 15 µA
±1.5V	1.6 MΩ	160 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

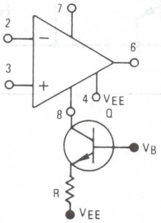
ACTIVE PROGRAMMING

FET CURRENT SOURCE



7
VCC
2
3
6
4
VEE
8
VG
VEE

BIPOLAR CURRENT SOURCE

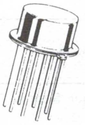


7
2
3
6
4
VEE
8
Q
VB
R
VEE

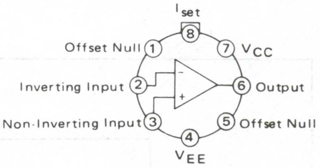
Pins not shown are not connected.

PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

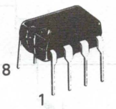


G SUFFIX
METAL PACKAGE
CASE 601-04



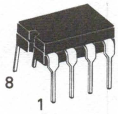
Iset
8
Offset Null
1
7
VCC
Inverting Input
2
6
Output
Non-Inverting Input
3
5
Offset Null
4
VEE

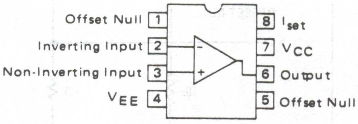
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC1776C only)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02





Offset Null
1
Inverting Input
2
Non-Inverting Input
3
VEE
4
8
Iset
7
VCC
6
Output
5
Offset Null

(Top View)

ORDERING INFORMATION

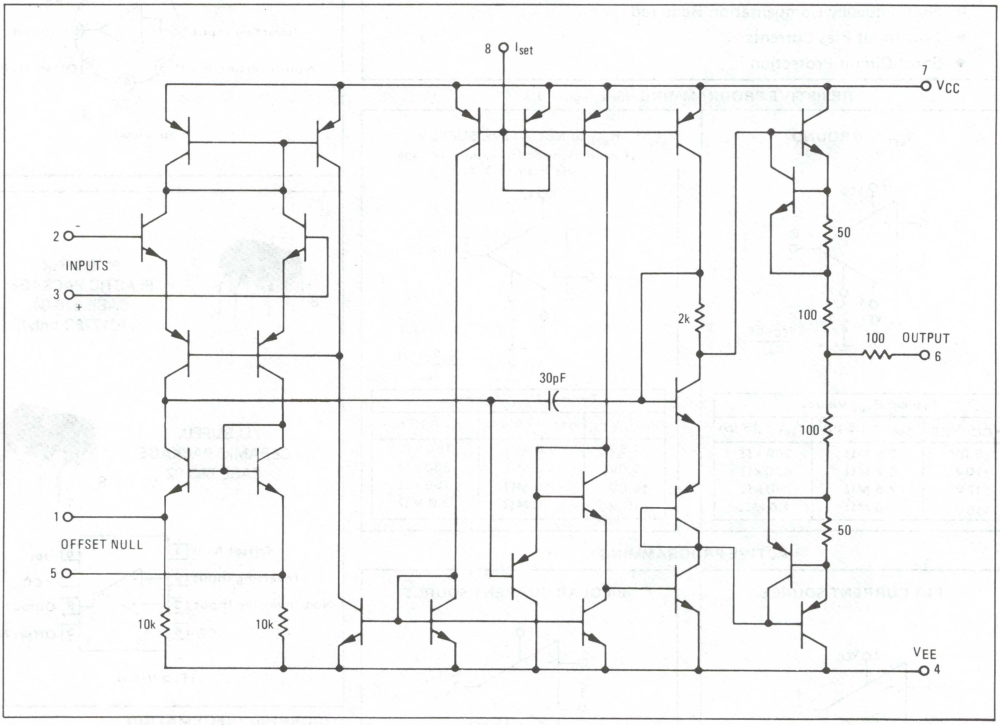
Device	Temperature Range	Package
MC1776G	−55 to +125°C	Metal Can
MC1776U	−55 to +125°C	Ceramic DIP
MC1776CG	0 to +70°C	Metal Can
MC1776CP1	0 to +70°C	Plastic DIP
MC1776CU	0 to +70°C	Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common-Mode Input Voltage	V_{ICM}		Vdc
V_{CC} and $\lvert V_{EE}\rvert < 15$ V		V_{CC}, V_{EE}	
V_{CC} and $\lvert V_{EE}\rvert \geq 15$ V		±15	
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	500	µA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}-2.0 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range	T_A		°C
MC1776		-55 to +125	
MC1776C		0 to +70	
Storage Temperature Range	T_{stg}		°C
Metal and Ceramic Packages		-65 to +150	
Plastic Package		-55 to +125	
Junction Temperature	T_J		°C
Metal and Ceramic Packages		175	
Plastic Package		150	

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ µA.

SCHEMATIC DIAGRAM

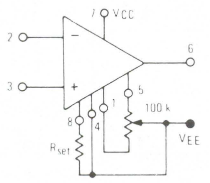


ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

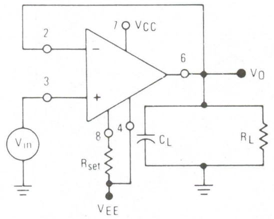
Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leqslant$ 10 kΩ)	V_{IO}							mV
T_A = +25°C		—	2.0	5.0	—	2.0	6.0	
T_{low}* $\leqslant T_A \leqslant T_{high}$*		—	—	6.0	—	—	7.5	
Offset Voltage Adjustment Range	V_{IOR}	—	9.0	—	—	9.0	—	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		—	0.7	3.0	—	0.7	6.0	
$T_A = T_{high}$		—	—	5.0	—	—	6.0	
$T_A = T_{low}$		—	—	10	—	—	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		—	2.0	7.5	—	2.0	10	
$T_A = T_{high}$		—	—	7.5	—	—	10	
$T_A = T_{low}$		—	—	20	—	—	20	
Input Resistance	r_i	—	50	—	—	50	—	MΩ
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range	V_{ID}							V
$T_{low} \leqslant T_A \leqslant T_{high}$		±1.0	—	—	±1.0	—	—	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geqslant$ 75 kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	—	25 k	200 k	—	
$R_L \geqslant$ 75 kΩ, V_O = ±1.0 V, $T_{low} \leqslant T_A \leqslant T_{high}$		25 k	—	—	25 k	—	—	
Output Voltage Swing	V_O							V
$R_L \geqslant$ 75 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		±2.0	±2.4	—	±2.0	±2.4	—	
Output Resistance	r_o	—	5.0	—	—	5.0	—	kΩ
Output Short-Circuit Current	I_{os}	—	3.0	—	—	3.0	—	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		70	86	—	70	86	—	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$		—	25	150	—	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		—	13	20	—	13	20	
$T_{low} \leqslant T_A \leqslant T_{high}$		—	—	25	—	—	25	
Power Dissipation	P_D							μW
T_A = +25°C		—	78	120	—	78	120	
$T_{low} \leqslant T_A \leqslant T_{high}$		—	—	150	—	—	150	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geqslant$ 5.0 kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	—	3.0	—	—	3.0	—	μs
Overshoot	OS	—	0	—	—	0	—	%
Slew Rate ($R_L \geqslant$ 5.0 kΩ)	S_R	—	0.03	—	—	0.03	—	V/μs

*T_{low} = −55°C for MC1776 T_{high} = +125°C for MC1776
0°C for MC1776C +70°C for MC1776C

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
$T_A = +25^\circ C$		–	2.0	5.0	–	2.0	6.0	
$T_{low}{}^* \leq T_A \leq T_{high}{}^*$		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
$T_A = +25^\circ C$		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
$T_A = +25^\circ C$		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±1.0	–	–	±1.0	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 5.0$ kΩ, $V_O = \pm 1.0$ V, $T_A = +25^\circ C$		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 5.0$ kΩ, $V_O = \pm 1.0$ V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±1.9	±2.1	–	±2.0	±2.1	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	5.0	–	–	5.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
$T_A = +25^\circ C$		–	130	160	–	130	170	
$T_{low} \leq T_A \leq T_{high}$		–	–	180	–	–	180	
Power Dissipation	P_D							μW
$T_A = +25^\circ C$		–	780	960	–	780	1020	
$T_{low} \leq T_A \leq T_{high}$		–	–	1080	–	–	1080	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.6	–	–	0.6	–	μs
Overshoot	OS	–	5.0	–	–	5.0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.35	–	–	0.35	–	V/μs

*T_{low} = −55°C for MC1776 T_{high} = +125°C for MC1776
0°C for MC1776C +70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
T_A = T_{high}		–	–	5.0	–	–	6.0	
T_A = T_{low}		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
T_A = T_{high}		–	–	7.5	–	–	10	
T_A = T_{low}		–	–	20	–	–	20	
Input Resistance	r_i	–	50	–	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \geq 75$ kΩ, V_O = ±10 V, T_A = +25°C		200 k	400 k	–	50 k	400 k	–	
$R_L \geq 75$ kΩ, V_O = ±10 V, T_{low} ≤ T_A ≤ T_{high}		100 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
$R_L \geq 75$ kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
$R_L \geq 75$ kΩ, T_{low} ≤ T_A ≤ T_{high}		±10	–	–	±10	–	–	
Output Resistance	r_o	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	3.0	–	–	3.0	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, T_{low} ≤ T_A ≤ T_{high}		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, T_{low} ≤ T_A ≤ T_{high}		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	20	25	–	20	30	
T_{low} ≤ T_A ≤ T_{high}		–	–	30	–	–	35	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	0.75	–	–	0.9	
T_{low} ≤ T_A ≤ T_{high}		–	–	0.9	–	–	1.05	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	1.6	–	–	1.6	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.1	–	–	0.1	–	V/μs

*T_{low} = −55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}							mV
$T_A = +25°C$		–	2.0	5.0	–	2.0	6.0	
$T_{low}^* \le T_A \le T_{high}^*$		–	–	6.0	–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Input Offset Current	I_{IO}							nA
$T_A = +25°C$		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
$T_A = +25°C$		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	r_i	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	–	2.0	–	pF
Input Voltage Range	V_{ID}							V
$T_{low} \le T_A \le T_{high}$		±10	–	–	±10	–	–	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \ge 5.0$ kΩ, $V_O = \pm 10$ V, $T_A = +25°C$		100 k	400 k	–	50 k	400 k	–	
$R_L \ge 75$ kΩ, $V_O = \pm 10$ V, $T_{low} \le T_A \le T_{high}$		75 k	–	–	50 k	–	–	
Output Voltage Swing	V_O							V
$R_L \ge 5.0$ kΩ, $T_A = +25°C$		±10	±13	–	±10	±13	–	
$R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$		±10	–	–	±10	–	–	
Output Resistance	r_o	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	–	12	–	mA
Common-Mode Rejection Ratio	CMRR							dB
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		–	25	150	–	25	200	
Supply Current	I_{CC}, I_{EE}							μA
$T_A = +25°C$		–	160	180	–	160	190	
$T_{low} \le T_A \le T_{high}$		–	–	200	–	–	200	
Power Dissipation	P_D							mW
$T_A = +25°C$		–	–	5.4	–	–	5.7	
$T_{low} \le T_A \le T_{high}$		–	–	6.0	–	–	6.0	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot	OS	–	10	–	–	10	–	%
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	–	0.8	–	–	0.8	–	V/μs

*T_{low} = −55°C for MC1776 T_{high} = +125°C for MC1776
0°C for MC1776C +70°C for MC1776C

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

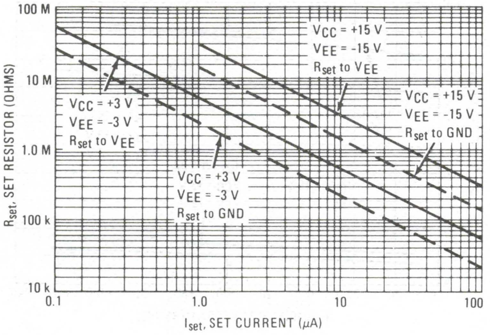


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

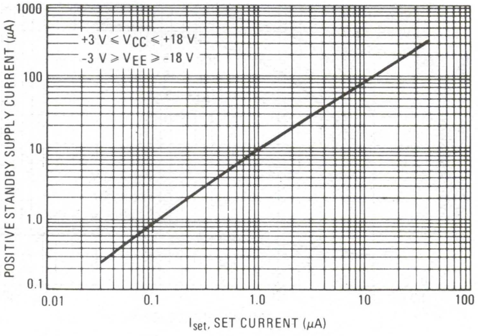


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

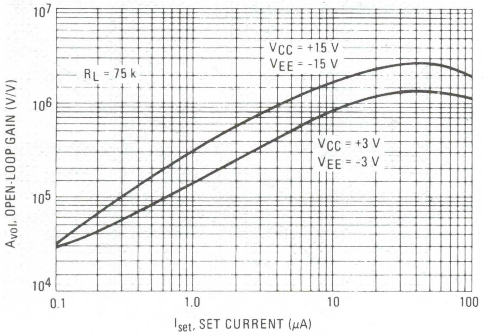


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

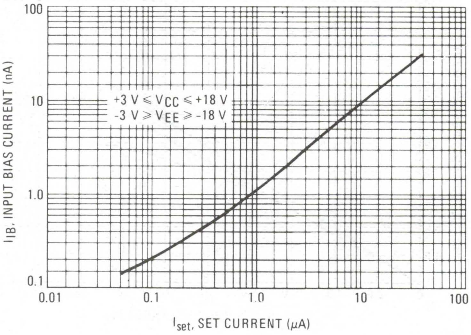


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

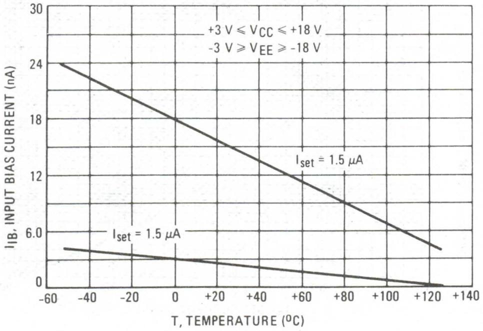
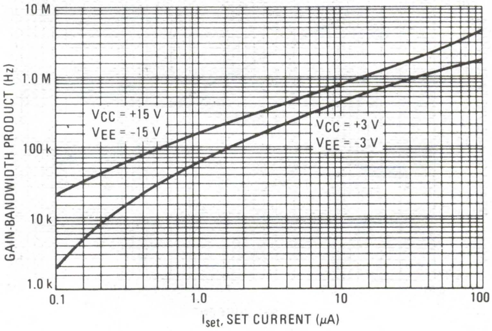


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

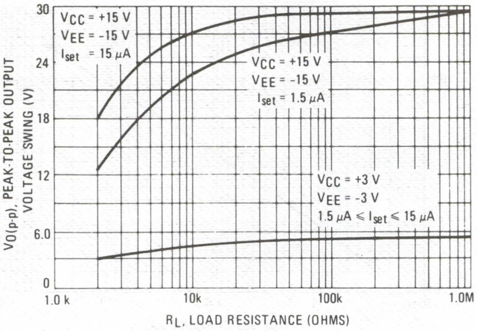


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

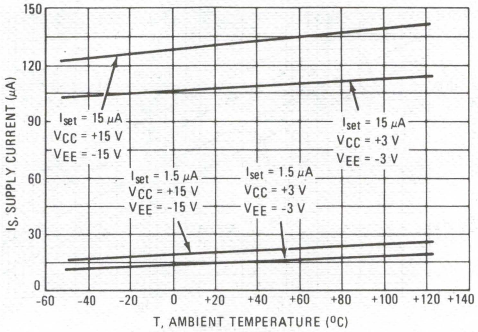


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

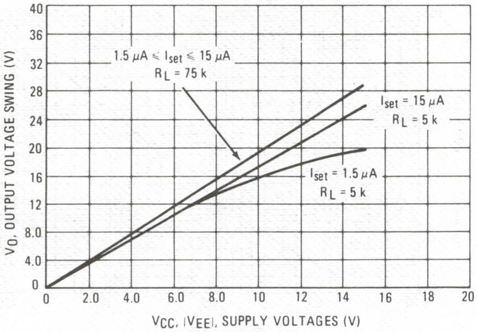


FIGURE 10 – SLEW RATE versus SET CURRENT

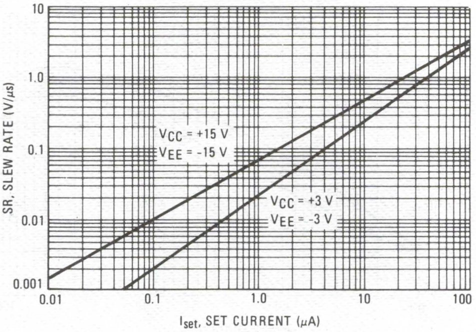


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

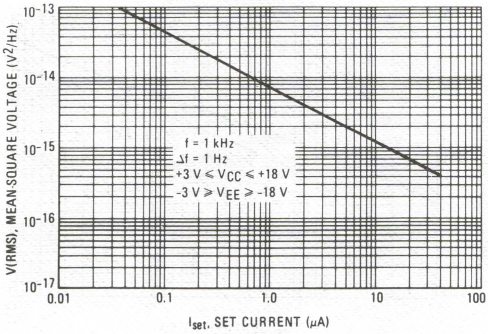
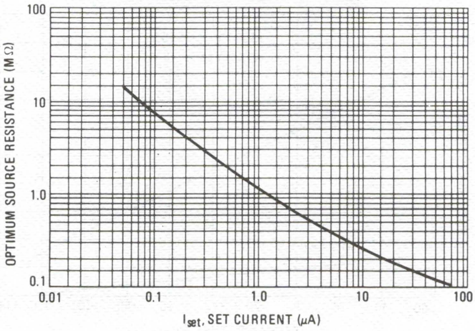
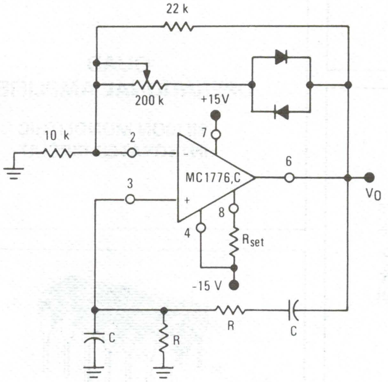


FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



APPLICATIONS INFORMATION

FIGURE 13 – WIEN BRIDGE OSCILLATOR

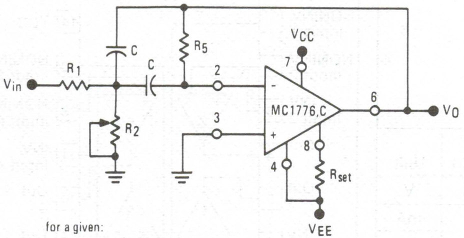

22 k
200 k
+15V
10 k
2
7
3
6
MC1776,C
Vo
8
4
Rset
-15 V
R
C
C
R

$f_0 = \frac{1}{2\pi RC}$

(for f_0 = 1.0 kHz)

R = 16 kΩ
C = 0.01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER


C
R5
VCC
R1
C
2
7
Vin
6
Vo
MC1776,C
R2
3
8
4
Rset
VEE

for a given:
f_0 = center frequency
A (f_0) = Gain at center frequency
Q = quality factor
Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_0 C}$$

$$R1 = \frac{R5}{2A(f_0)}$$

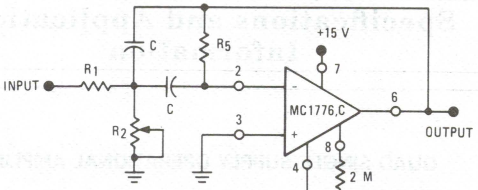
$$R2 = \frac{R1\,R5}{4Q^2\,R1\text{-}R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_0\,f_0}{GBW} \leqslant 0.1$$

where f_0 and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)


C
R5
+15 V
R1
2
7
INPUT
C
MC1776,C
6
OUTPUT
R2
3
8
4
2 M
-15V

for a 1.0 kHz filter
with Q = 10
and A (f_0) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

FIGURE 16 – GATED AMPLIFIER

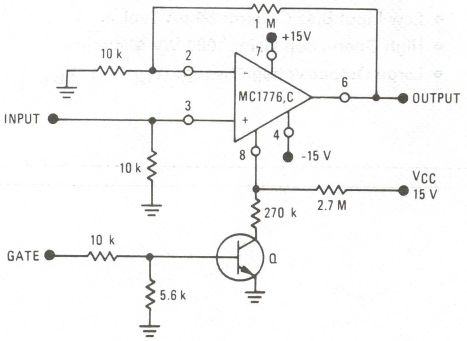
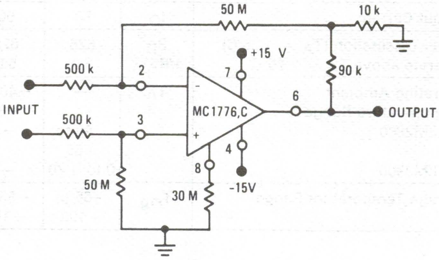

1 M
+15V
10 k
2
7
6
MC1776,C
OUTPUT
INPUT
3
4
8
-15 V
10 k
VCC
15 V
2.7 M
270 k
10 k
GATE
Q
5.6 k

FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER


50 M
10 k
+15 V
500 k
2
7
90 k
6
MC1776,C
OUTPUT
INPUT
500 k
3
8
4
50 M
30 M
-15V

MC3301 LM2900
MC3401 LM3900

MOTOROLA

Specifications and Applications Information

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usages.

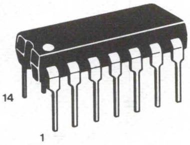
- Single-Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} − 1) V_{p-p}

MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	MC3401	Unit
Supply Voltage	V_{CC}	+32	+28	+18	V
Input Currents (I_{in}^+ or I_{in}^-)	I_{in}	5.0	5.0	5.0	mA
Output Current	I_O	50	50	50	mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0	625 5.0	625 5.0	mW mW/°C
Operating Ambient Temperature Range	T_A	—	−40 to +85	0 to +70	°C
LM2900		−40 to +85	—	—	
LM3900		0 to +70	—	—	
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	−65 to +150	°C

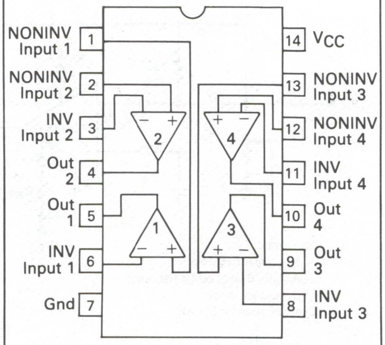
QUAD OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS


NONINV Input 1
1
NONINV Input 2
2
INV Input 2
3
Out 2
4
Out 1
5
INV Input 1
6
Gnd
7
14
V_{CC}
13
NONINV Input 3
12
NONINV Input 4
11
INV Input 4
10
Out 4
9
Out 3
8
INV Input 3
1
2
3
4

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM3900N MC3401P	0°C to +70°C	Plastic DIP
LM2900N MC3301P	−40°C to +85°C	

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	LM2900			LM3900			MC3301			MC3401			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open-Loop Voltage Gain	A_{VOL}													V/mV
f = 100 Hz, R_L = 5.0 k		1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	1.2	2.0	—	
T_A = T_{low} to T_{high} (Notes 1, 2)		—	—	—	—	—	—	—	—	—	0.8	—	—	
Input Resistance (Inverting Input)	r_i	—	1.0	—	—	1.0	—	—	1.0	—	0.1	1.0	—	MΩ
Output Resistance	r_O	—	8.0	—	—	8.0	—	—	8.0	—	—	8.0	—	kΩ
Input Bias Current (Inverting Input)	I_{IB}	—	50	200	—	50	200	—	50	300	—	50	300	nA
T_A = T_{low} to T_{high} (Note 1)		—	—	—	—	—	—	—	—	—	—	—	500	
Slew Rate (C_L = 100 pF, R_L = 2.0 k)	SR													V/µs
Positive Output Swing		—	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	
Negative Output Swing		—	20	—	—	20	—	—	20	—	—	20	—	
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	—	4.0	—	—	4.0	—	MHz
Output Voltage Swing (Note 7)														V
V_{CC} = +15 V, R_L = 2.0 k														
V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	V_{OH}	13.5	14.2	—	13.5	14.2	—	13.5	14.2	—	13.5	14.2	—	
V_{out} Low (I_{in}^- = 10 µA, I_{in}^+ = 0)	V_{OL}	—	0.03	0.2	—	0.03	0.2	—	0.03	0.2	—	0.03	0.2	
V_{CC} = Maximum Rating, R_L = ∞														
V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	V_{OH}	—	29.5	—	—	29.5	—	—	25.5	—	—	15.5	—	
Output Current														mA
Source	I_{source}	6.0	10	—	6.0	10	—	5.0	10	—	5.0	10	—	
Sink (Note 3)	I_{sink}	0.5	0.87	—	0.5	0.87	—	0.5	0.87	—	0.5	0.87	—	
Low Level Output Current I_{in}^- = 5.0 µA, V_{OL} = 1.0 V	I_{OL}	—	5.0	—	—	5.0	—	—	5.0	—	—	5.0	—	
Supply Current (All Four Amplifiers)														mA
Noninverting Inputs Open	I_{DO}	—	6.9	10	—	6.9	10	—	6.9	10	—	6.9	10	
Noninverting Inputs Grounded	I_{DG}	—	7.8	14	—	7.8	14	—	7.8	14	—	7.8	14	
Power Supply Rejection (f = 100 Hz)	PSRR	—	55	—	—	55	—	—	55	—	—	55	—	dB
Mirror Gain (T_A = T_{low} to T_{high}; Notes 1, 4)	A_i													µA
I_{in}^+ = 20 µA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
I_{in}^+ = 200 µA		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.0	
Δ Mirror Gain (T_A = T_{low} to T_{high}; Notes 1, 4) 20 µA ≤ I_{in}^+ ≤ 200 µA	ΔA_i	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	%
Mirror Current (T_A = T_{low} to T_{high}; Note 1)		—	10	500	—	10	500	—	10	500	—	10	500	µA
Negative Input Current (Note 6)		—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	mA

NOTES:

1. T_{low} = −40°C for LM2900, MC3301 T_{high} = +85°C for LM2900, MC3301
   = 0°C for LM3900, MC3401 = +70°C ffor LM3900, MC3401
2. Open-loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 µA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately −0.3 volts. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. Negative input currents in excess of 4.0 mA will cause the output to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 1 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

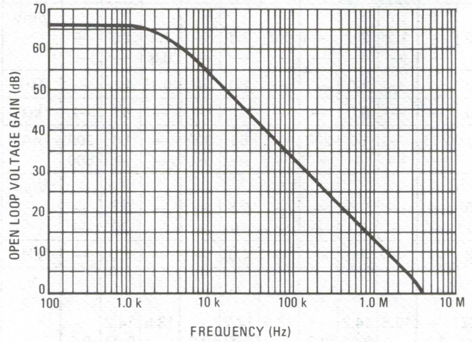


FIGURE 2 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

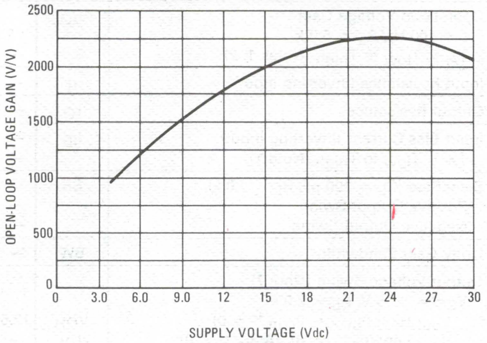


FIGURE 3 — OUTPUT RESISTANCE versus FREQUENCY

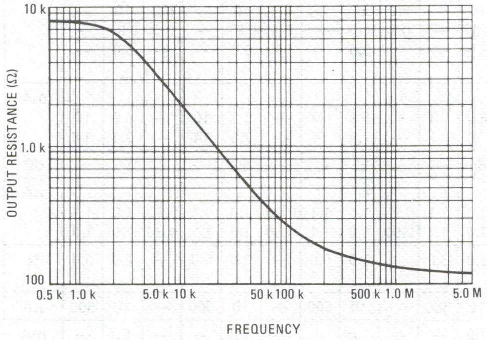


FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE

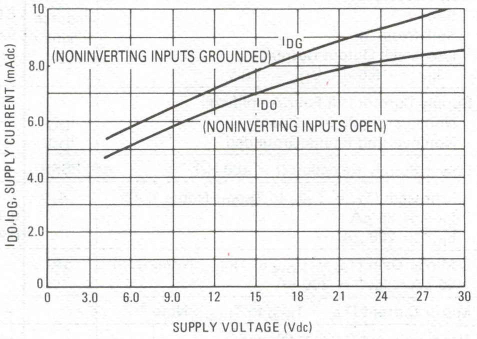


FIGURE 5 — LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

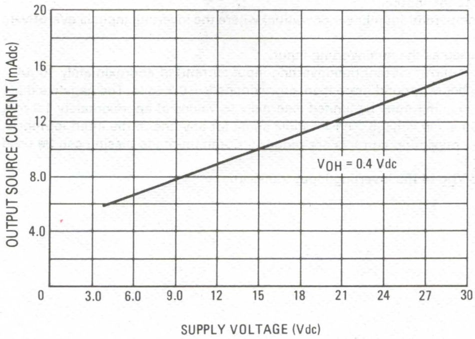
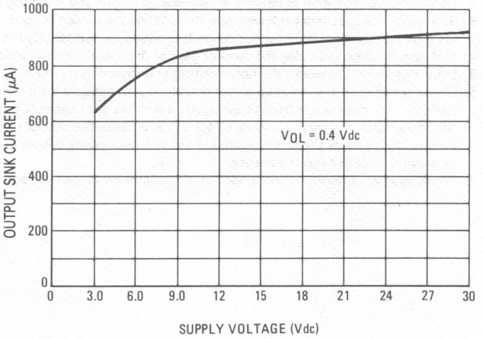


FIGURE 6 — LINEAR SINK CURRENT versus SUPPLY VOLTAGE

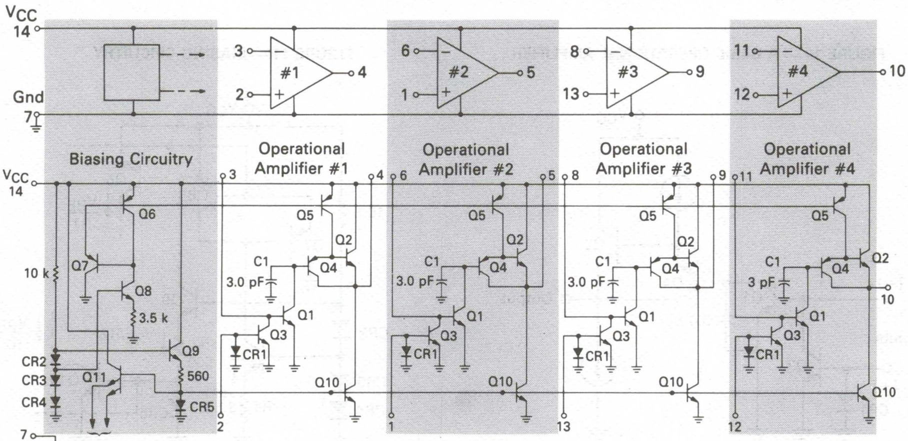


OPERATION AND APPLICATIONS

BASIC AMPLIFIER

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

FIGURE 7 — BLOCK DIAGRAM


VCC
14
Gnd
7
3
2
#1
4
6
1
#2
5
8
13
#3
9
11
12
#4
10
Biasing Circuitry
Operational Amplifier #1
Operational Amplifier #2
Operational Amplifier #3
Operational Amplifier #4
Q6
Q7
Q8
10 k
3.5 k
Q9
560
CR2
CR3
CR4
CR5
Q11
Q5
Q2
C1
3.0 pF
3 pF
Q4
Q1
Q3
CR1
Q10
Gnd

Multiple emitter (8) transistor — one emitter connected to each input.

A noninverting input is obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, $I_{in}+$, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to $I_{in}+$. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to $I_{in}+$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 8 — A BASIC GAIN STAGE

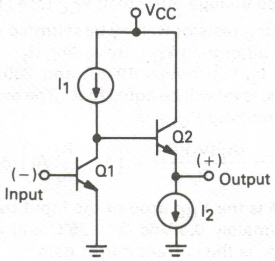
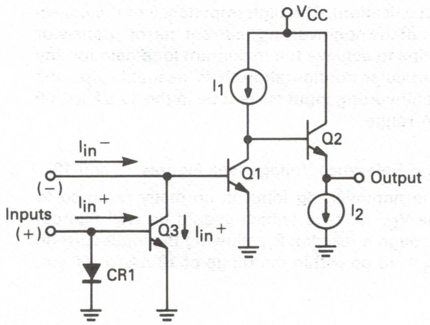

VCC
I1
Q2
Q1
(−)
Input
(+)
Output
I2

FIGURE 9 — OBTAINING A NONINVERTING INPUT


VCC
I1
Q2
Iin −
Q1
(−)
Output
Iin +
Inputs
(+)
Q3
Iin +
I2
CR1

OPERATION AND APPLICATIONS (continued)

BIASING CIRCUITRY

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

FIGURE 10 — A BASIC OPERATIONAL AMPLIFIER

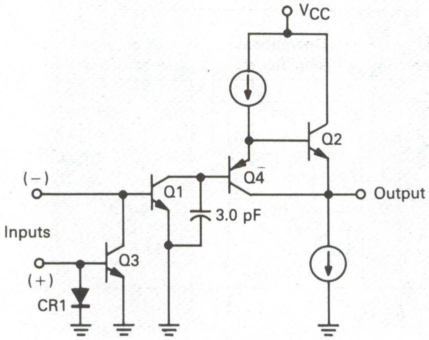
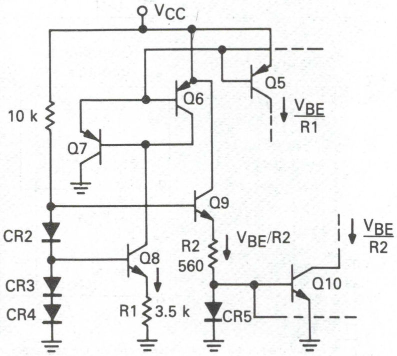


FIGURE 11 — BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing; as shown in Figures 12 and 13 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13)

   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, $I_{in}+$, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14)

   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping $I_{in}+$ between 10 μA and 200 μA) the output dc level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

FIGURE 12 — INVERTING AMPLIFIER

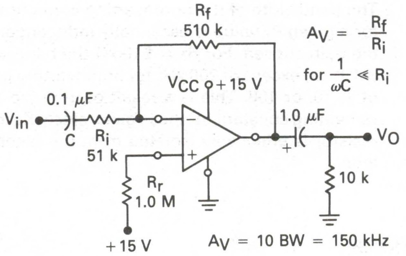
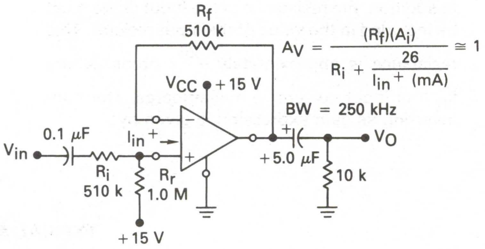

Rf
510 k
AV = −Rf/Ri
for 1/ωC ≪ Ri
VCC +15 V
0.1 µF
Vin
C
Ri
51 k
1.0 µF
VO
Rr
1.0 M
10 k
+15 V
AV = 10 BW = 150 kHz

FIGURE 13 — NONINVERTING AMPLIFIER


Rf
510 k
AV = (Rf)(Ai) / (Ri + 26/Iin+ (mA)) ≅ 1
VCC +15 V
BW = 250 kHz
0.1 µF
Iin+
Vin
Ri
510 k
Rr
1.0 M
+5.0 µF
VO
10 k
+15 V

2. Gain Determination

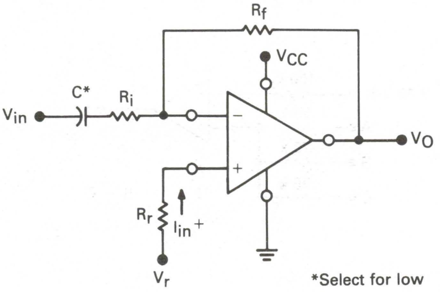
A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

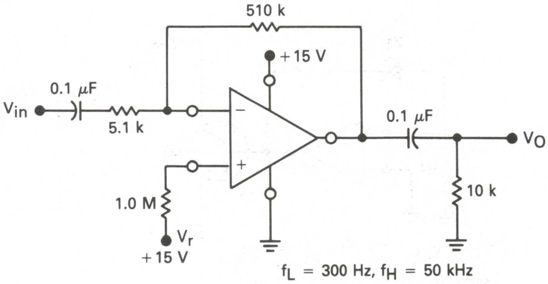
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

FIGURE 14 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE


Rf
VCC
C*
Ri
Vin
VO
Rr
Iin+
Vr

*Select for low frequency response.

FIGURE 15 — INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$


510 k
+15 V
0.1 µF
Vin
5.1 k
0.1 µF
VO
10 k
1.0 M
Vr
+15 V

$f_L = 300$ Hz, $f_H = 50$ kHz
$A_V = 100$

B. Noninverting Amplifier

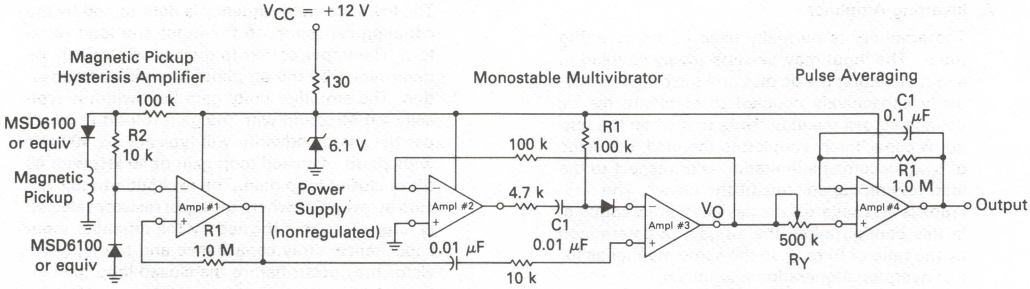
These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in}^{+}}$ ohms, where I_{in}^{+} is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in}^{+}\ (mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 16 — TACHOMETER CIRCUIT


VCC = +12 V
Magnetic Pickup
Hysterisis Amplifier
100 k
MSD6100
or equiv
R2
10 k
Magnetic
Pickup
Ampl #1
R1
1.0 M
MSD6100
or equiv
130
6.1 V
Power
Supply
(nonregulated)
Monostable Multivibrator
100 k
R1
100 k
Ampl #2
4.7 k
C1
0.01 µF
0.01 µF
10 k
Ampl #3
VO
Pulse Averaging
C1
0.1 µF
R1
1.0 M
Ampl #4
500 k
RY
Output

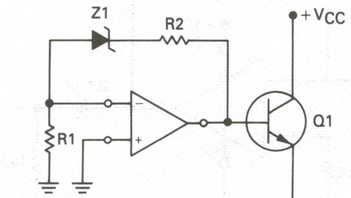
Hysteresis Voltage for Switching

$$V_H = \frac{A_iR2}{R1}(V_{CC} - 1.6)$$

Timing Interval: t ≈ 0.7 R1 C1

$$V_{p\text{-}p} \cong \frac{(V_O - 0.6) \cdot A_i \cdot t}{R_Y C1}$$

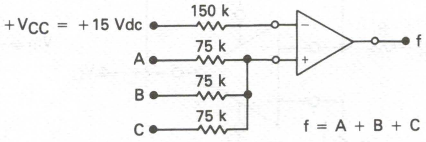
FIGURE 17 — VOLTAGE REGULATOR


Z1
R2
+VCC
R1
Q1
VO

$$V_O = V_{Z1} + 0.6\left(1 + \frac{R2}{R1}\right) - V_{BE_{Q1}}$$

NOTE:
For positive T_C zeners R2 and R1 can be selected to give T_C output.

FIGURE 18 — LOGIC "OR" GATE


+VCC = +15 Vdc
150 k
A
75 k
B
75 k
C
75 k
f

f = A + B + C

TYPICAL APPLICATIONS (continued)

FIGURE 19 — LOGIC "NAND" GATE (Large Fan-In)

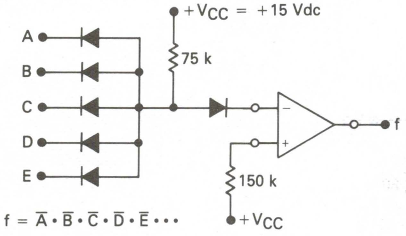

+VCC = +15 Vdc
A
B
C
D
E
75 k
150 k
+VCC
f
f = $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}\cdot\overline{E}\cdots$

FIGURE 20 — LOGIC "NOR" GATE

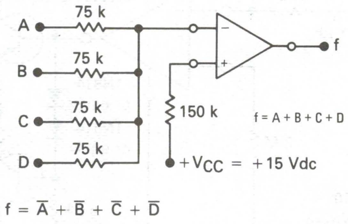

A
B
C
D
75 k
75 k
75 k
75 k
150 k
f
f = A + B + C + D
+VCC = +15 Vdc
f = $\overline{A}+\overline{B}+\overline{C}+\overline{D}$

FIGURE 21 — R-S FLIP-FLOP

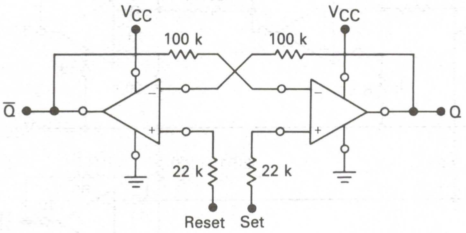

VCC
VCC
100 k
100 k
$\overline{Q}$
Q
22 k
22 k
Reset
Set

FIGURE 22 — ASTABLE MULTIVIBRATOR

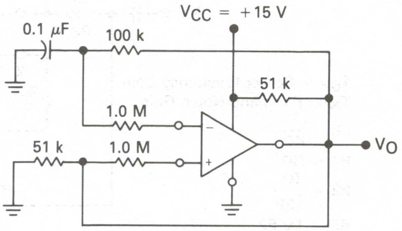

VCC = +15 V
0.1 μF
100 k
51 k
1.0 M
51 k
1.0 M
VO

FIGURE 23 — POSITIVE-EDGE DIFFERENTIATOR

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

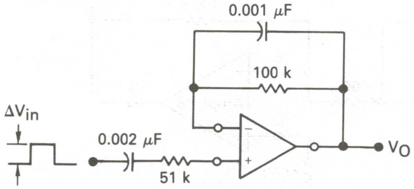
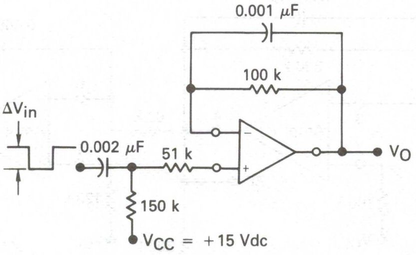
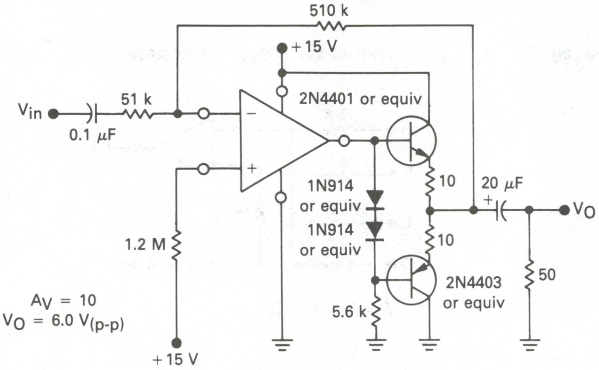

0.001 μF
100 k
ΔVin
0.002 μF
51 k
VO

FIGURE 24 — NEGATIVE-EDGE DIFFERENTIATOR


0.001 μF
100 k
ΔVin
0.002 μF
51 k
150 k
VO
VCC = +15 Vdc

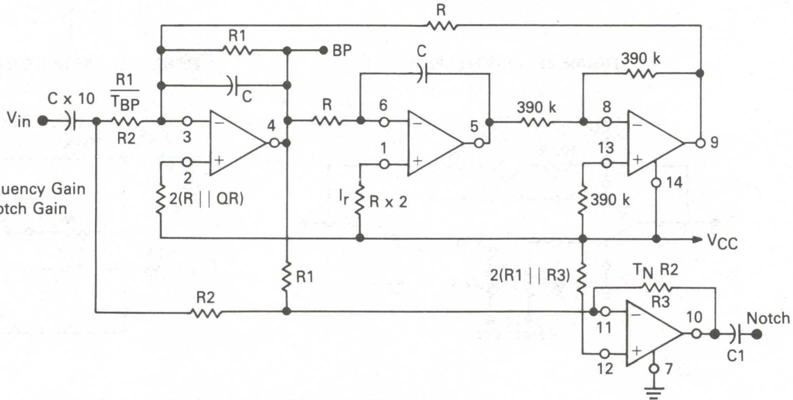
$V_{O(dc)}$ ≈ 7.0 Vdc
Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

FIGURE 25 — AMPLIFIER AND DRIVER FOR A 50-OHM LINE


510 k
+15 V
Vin
51 k
0.1 μF
2N4401 or equiv
1N914
or equiv
1N914
or equiv
10
20 μF
+
Vo
10
1.2 M
2N4403
or equiv
50
5.6 k
+15 V

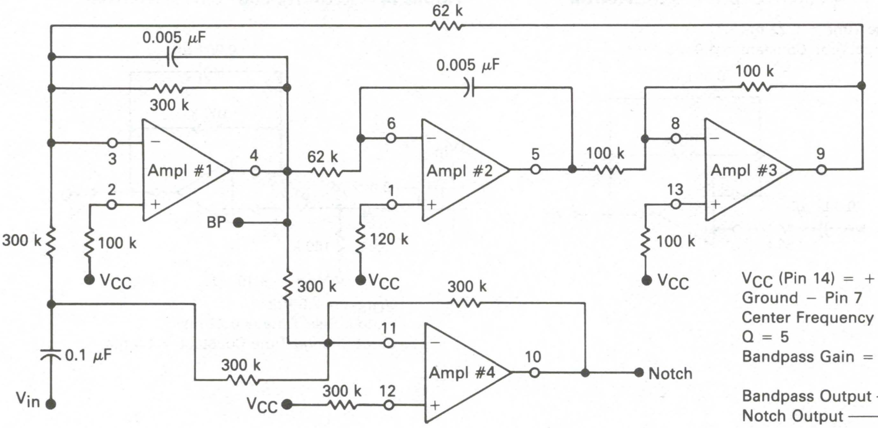
$A_V = 10$
$V_O = 6.0\ V_{(p\text{-}p)}$

FIGURE 26 — BASIC BANDPASS AND NOTCH FILTER


R
R1
BP
C
390 k
R1
TBP
C x 10
Vin
R2
C
3
4
R
6
5
390 k
8
9
2
1
13
14
2(R || QR)
Ir
R x 2
390 k
VCC
R1
2(R1 || R3)
TN R2
R3
R2
11
10
Notch
12
7
C1

T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain
$\omega 0 = \frac{1}{RC}$
$R1 = QR$
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N\ R2$

FIGURE 27 — BANDPASS AND NOTCH FILTER

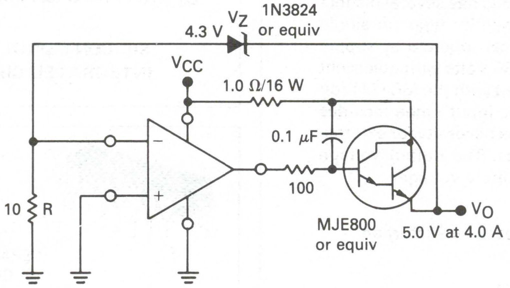

62 k
0.005 μF
300 k
0.005 μF
100 k
3
Ampl #1
4
62 k
6
Ampl #2
5
100 k
8
Ampl #3
9
2
1
13
BP
300 k
100 k
VCC
120 k
VCC
100 k
VCC
300 k
300 k
11
0.1 μF
300 k
Ampl #4
10
Notch
Vin
VCC
300 k
12

V_{CC} (Pin 14) = +12 Volts
Ground – Pin 7
Center Frequency 500 Hz
Q = 5
Bandpass Gain = 1

Bandpass Output →Pin 4
Notch Output ——→ Pin 10

TYPICAL APPLICATIONS (continued)

FIGURE 28 — VOLTAGE REGULATOR

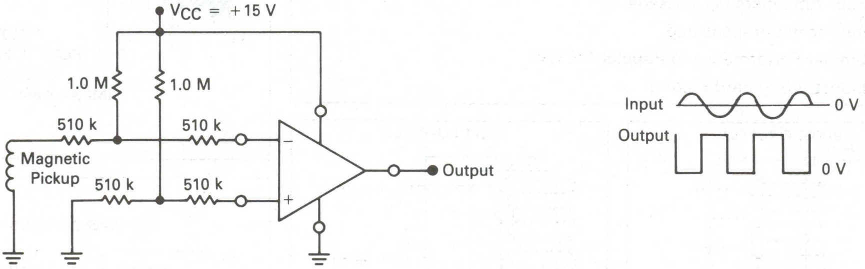

1N3824
or equiv
V_Z
4.3 V
V_{CC}
1.0 Ω/16 W
0.1 μF
100
10
R
MJE800
or equiv
V_O
5.0 V at 4.0 A

$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero-TC. A 7.0 Volt Zener will give approximately zero-TC.

FIGURE 29 — ZERO CROSSING DETECTOR


$V_{CC} = +15$ V
1.0 M
1.0 M
510 k
510 k
510 k
510 k
Magnetic
Pickup
Output
Input
0 V
Output
0 V

MC3403
MC3503
MC3303

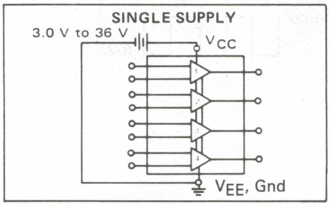
MOTOROLA

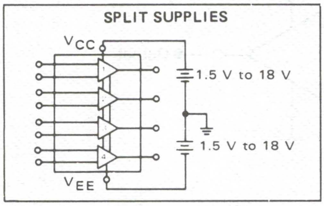
Specifications and Applications Information

QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- SImilar Performance to Popular MC1741
- Industry Standard Pinouts





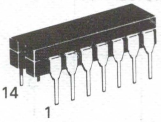
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	-18	
Input Differential Voltage Range (1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}		°C
Ceramic Package		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3503		-55 to +125	
MC3403		0 to +70	
MC3303		-40 to +85	
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

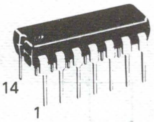
(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

QUAD DIFFERENTIAL
INPUT
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

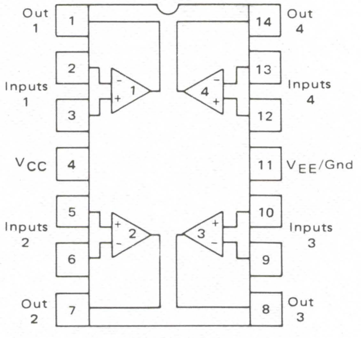


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC3403 and MC3303 only)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Type	Temperature Range	Package
MC3303L	-40°C to +85°C	Ceramic DIP
MC3303P	-40°C to +85°C	Plastic DIP
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	-55°C to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V for MC3503, MC3403; V_{CC} = +14 V, V_{EE} = Gnd for MCC3303. T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	8.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	6.0	–	–	12	–	–	10	
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	30	75	nA
$T_A = T_{high}$ to T_{low}		–	–	200	–	–	200	–	–	250	
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
$V_O = \pm 10$ V, $R_L = 2.0$ kΩ,		50	200	–	20	200	–	20	200	–	
$T_A = T_{high}$ to T_{low}		25	–	–	15	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	-200	-500	nA
$T_A = T_{high}$ to T_{low}		–	-300	-1500	–	–	-800	–	–	-1000	
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range	V_{OR}										V
$R_L = 10$ kΩ		±12	±13.5	–	±12	±13.5	–	+12	+12.5	–	
$R_L = 2.0$ kΩ		±10	±13	–	±10	±13	–	+10	+12	–	
$R_L = 2.0$ kΩ, $T_A = T_{high}$ to T_{low}		±10	–	–	±10	–	–	+10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+13 V −V_{EE}	+13.5 V −V_{EE}	–	+13 V −V_{EE}	+13.5 V −V_{EE}	–	+12 V −V_{EE}	+12.5 V −V_{EE}	–	V
Common-Mode Rejection Ratio $R_S \leqslant 10$ kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_o = 0) $R_L = \infty$	I_{CC}, I_{EE}	–	2.8	4.0	–	2.8	7.0	–	2.8	7.0	mA
Individual Output Short-Circuit Current (2)	$I_{OS\pm}$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR−	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
Power Bandwidth $A_V = 1$, $R_L = 2.0$ kΩ, V_o = 20 V(p-p), THD = 5%	BWp	–	9.0	–	–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth $A_V = 1$, $R_L = 10$ kΩ, V_o = 50 mV	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Slew Rate $A_V = 1$, V_i = −10 V to +10 V	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
Rise Time $A_V = 1$, $R_L = 10$ kΩ, V_o = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Fall Time $A_V = 1$, $R_L = 10$ kΩ, V_o = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Overshoot $A_V = 1$, $R_L = 10$ kΩ, V_o = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin $A_V = 1$, $R_L = 2.0$ kΩ, C_L = 200 pF	ϕm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	–	–	1.0	–	–	1.0	–	–	1.0	–	%

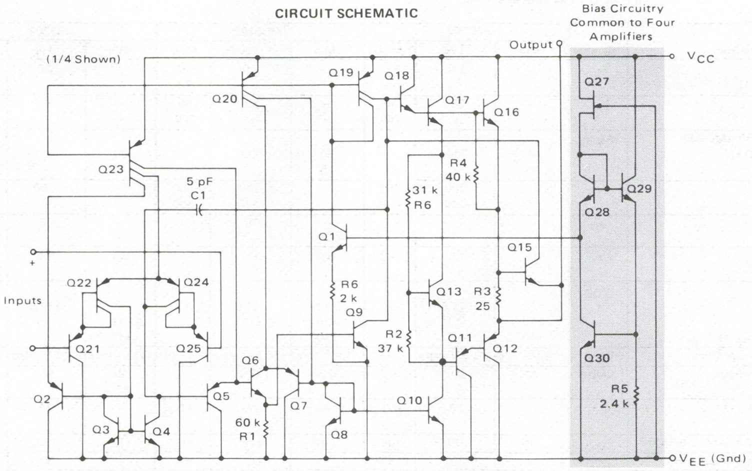
(1) T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = −55°C for MC3503, 0°C for MC3403, −40°C for MC3303

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

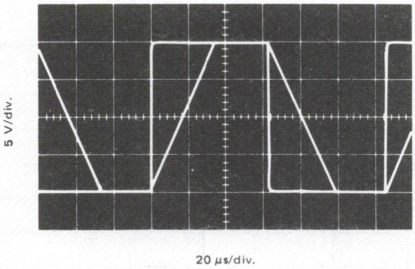
Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain $R_L = 2.0$ kΩ	A_{VOL}	10	200	–	10	200	–	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3)	V_{OR}										Vp-p
$R_L = 10$ kΩ, $V_{CC} = 5.0$ V		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
$R_L = 10$ kΩ, $5.0\text{ V} \leqslant V_{CC} \leqslant 30$ V		$V_{CC} - 2.0$	$V_{CC} - 1.7$	–	$V_{CC} - 2.0$	$V_{CC} - 1.7$	–	$V_{CC} - 2.0$	$V_{CC} - 1.7$	–	
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

CIRCUIT SCHEMATIC


(1/4 Shown)
Bias Circuitry
Common to Four
Amplifiers
Output
VCC
Q19
Q18
Q17
Q16
Q20
Q27
Q23
5 pF
C1
R4
40 k
31 k
R6
Q29
Q28
Q1
Q15
+
Q22
Q24
Inputs
R6
2 k
Q9
Q13
R3
25
R2
37 k
Q11
Q12
Q21
Q25
Q30
Q6
R5
2.4 k
Q2
Q5
Q7
Q10
Q3
Q4
60 k
R1
Q8
VEE (Gnd)

INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

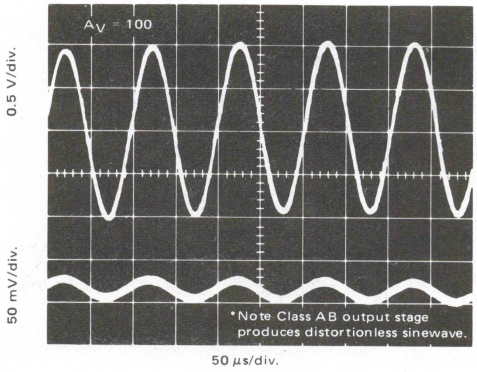


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

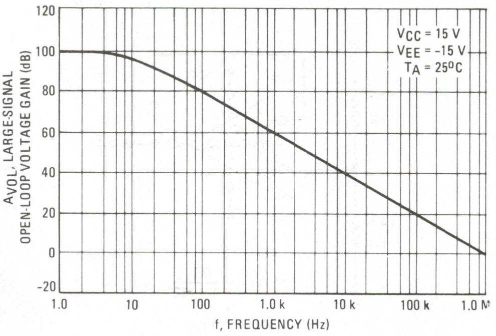


FIGURE 3 – POWER BANDWIDTH

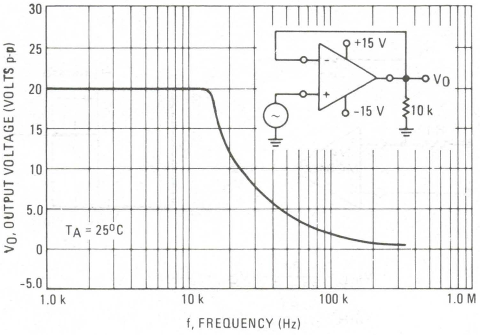


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

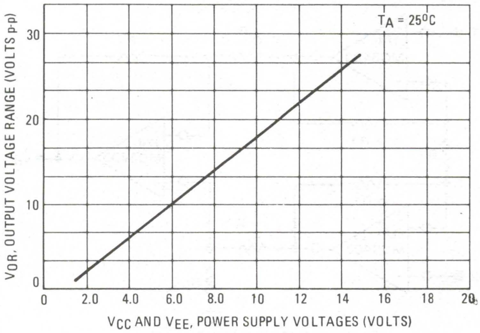


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

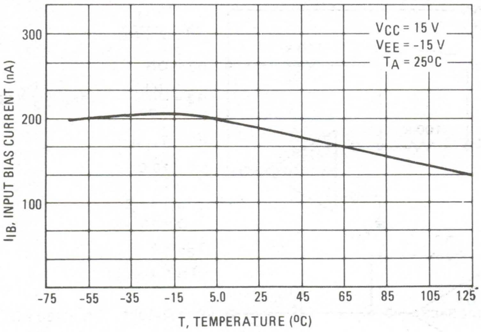
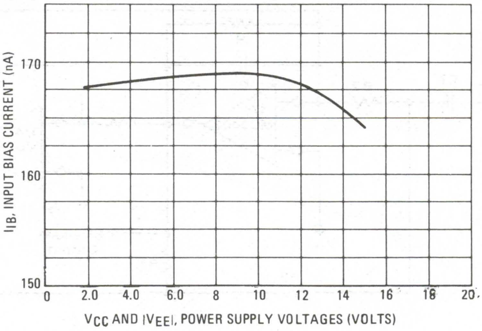
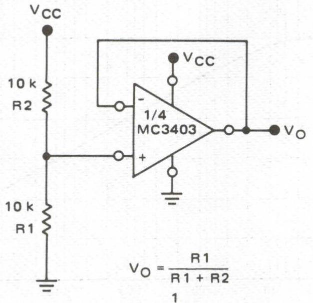


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

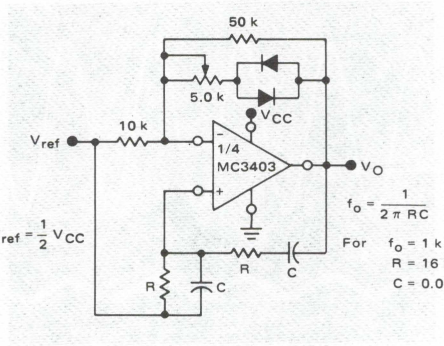
FIGURE 7 – VOLTAGE REFERENCE


VCC
10 k
R2
10 k
R1
VCC
1/4
MC3403
-
+
VO

$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 — WIEN BRIDGE OSCILLATOR

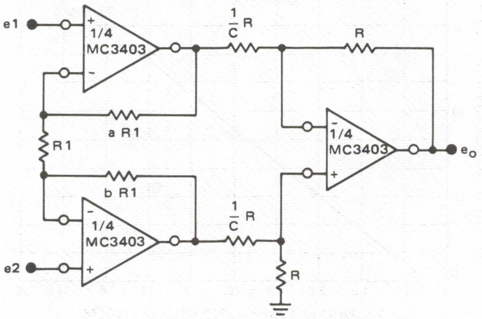

50 k
5.0 k
VCC
10 k
Vref
1/4
MC3403
-
+
VO
R
C
R
C

$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

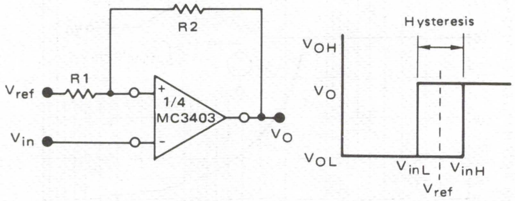
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 µF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4
MC3403
+
-
1/C R
R
a R1
R1
b R1
1/4
MC3403
-
+
eo
1/4
MC3403
-
+
e2
1/C R
R

$$e_o = C (1 + a + b) (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

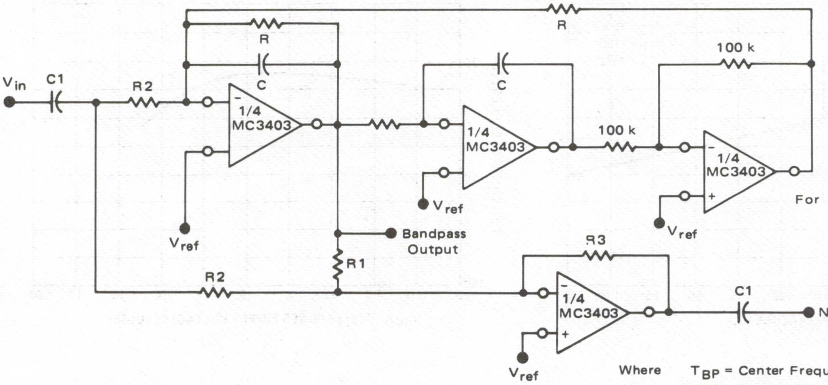

R2
R1
Vref
Vin
1/4
MC3403
+
-
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER


Vin
C1
R2
R
C
R
1/4
MC3403
-
+
Vref
C
1/4
MC3403
Vref
100 k
100 k
1/4
MC3403
-
+
Vref
Bandpass Output
R1
R2
R3
1/4
MC3403
-
+
Vref
C1
Notch Output

$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\ R2$

C1 = 10 C

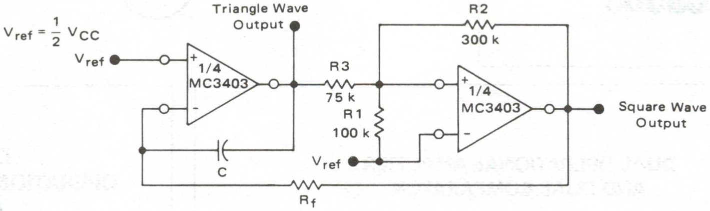
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

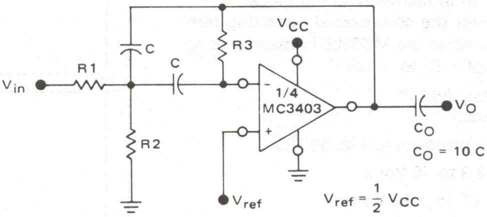
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR


$V_{ref} = \frac{1}{2} V_{CC}$
V_{ref}
Triangle Wave Output
1/4 MC3403
R3
75 k
R1
100 k
R2
300 k
1/4 MC3403
Square Wave Output
C
V_{ref}
R_f

$$f = \frac{R1 + R_C}{4\ CR_f\ R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


V_{CC}
C
R3
C
R1
V_{in}
1/4 MC3403
V_O
C_O
$C_O = 10\ C$
R2
V_{ref}
$V_{ref} = \frac{1}{2} V_{CC}$

Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi\ f_o\ C}$$

$$R1 = \frac{R3}{2\ A(f_o)}$$

$$R2 = \frac{R1\ R5}{4Q^2\ R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o\ f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3405
MC3505

MOTOROLA

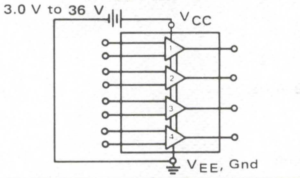
DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

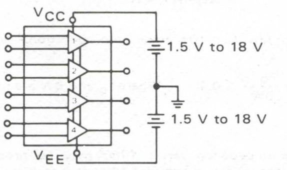
The MC3405 is specified over the commercial operating temperature range of 0 to +70°C, while the MC3505 is specified over the military operating range of −55 to +125°C.

- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Supply Current Drain
- Operational Amplifiers Are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible

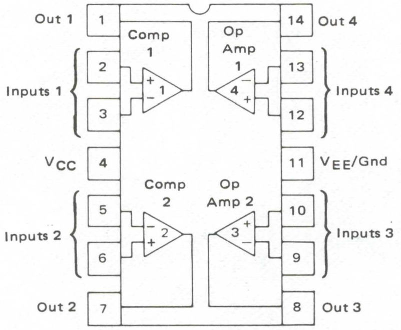
SINGLE SUPPLY


3.0 V to 36 V
VCC
1
2
3
4
VEE, Gnd

SPLIT SUPPLIES


VCC
1
2
3
4
1.5 V to 18 V
1.5 V to 18 V
VEE

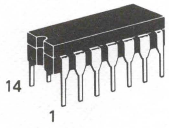
PIN CONNECTIONS


Out 1
1
Inputs 1
2
3
VCC
4
Inputs 2
5
6
Out 2
7
Comp 1
+
−
1
Comp 2
−
+
2
Op Amp 1
4
−
+
Op Amp 2
3
+
−
14
Out 4
13
Inputs 4
12
11
VEE/Gnd
10
Inputs 3
9
8
Out 3

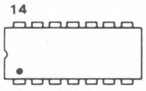
(Top View)

DUAL OPERATIONAL AMPLIFIER AND DUAL VOLTAGE COMPARATOR

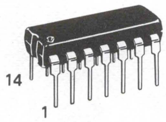
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



(Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

(MC3405 only)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0 to +70°C	Ceramic DIP
MC3405P	0 to +70°C	Plastic DIP
MC3505L	-55 to +125°C	Ceramic DIP

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply	V_{CC}	36	Vdc
Split Supplies	V_{CC}, V_{EE}	±18	
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range—MC3505	T_A	−55 to +125	°C
MC3405		0 to +70	
Storage Temperature Range—Ceramic Package	T_{stg}	−65 to +150	°C
Plastic Package		−55 to +125	
Operating Junction Temperature Range—Ceramic Package	T_J	175	°C
Plastic Package		150	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	nA
Input Bias Current	I_{IB}	—	−200	−500	—	−200	−500	nA
Large-Signal Open-Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	—	20	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	μV/V
Output Voltage Range (Note 1)	V_{OR}							Vp-p
(R_L = 10 kΩ, V_{CC} = 5.0 V)		3.3	3.5	—	3.3	3.5	—	
(R_L = 10 kΩ, 5.0 V ⩽ V_{CC} ⩽ 30 V)		$V_{CC}-2.0$	$V_{CC}-1.7$	—	$V_{CC}-2.0$	$V_{CC}-1.7$	—	
Power Supply Current (Notes 2 and 3)	I_{CC}	—	2.5	4.0	—	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	—	—	−120	—	—	−120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	mV
(T_A = T_{low} to T_{high}) (Note 4)		—	—	6.0	—	—	12	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	μV/°C
Input Offset Current	I_{IO}	—	—	50	—	—	50	nA
(T_A = T_{low} to T_{high}) (Note 4)		—	—	200	—	—	200	
Input Bias Current	I_{IB}	—	−200	−500	—	−200	−500	nA
(T_A = T_{low} to T_{high} (Note 4)		—	−300	−1500	—	—	−800	
Input Common Mode Voltage Range	V_{ICR}	$+13-V_{EE}$	—	—	$+13-V_{EE}$	—	—	Vdc
Large Signal Open Loop Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2.0 kΩ)		50	200	—	20	200	—	
(T_A = T_{low} to T_{high}) (Note 4)		25	100	—	15	100	—	
Common Mode Rejection Ratio	CMRR	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	—	30	150	—	30	150	μV/V
Output Voltage	V_O							Vdc
(R_L = 10 kΩ)		±12	±13.5	—	±12	±13.5	—	
(R_L = 2.0 kΩ)		±10	±13	—	±10	±13	—	
(R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)		±10	—	—	±10	—	—	
Output Short-Circuit Current	I_{OS}	±10	±30	±45	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	—	2.8	4.0	—	2.8	7.0	mA
Phase Margin	ϕm	—	60	—	—	60	—	Degrees
Small-Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	—	1.0	—	—	1.0	—	MHz
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V (p-p), THD = 5%)	BW_p	—	9.0	—	—	9.0	—	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	—	0.35	—	—	0.35	—	μs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	OS	—	20	—	—	20	—	%
Slew Rate	SR	—	0.6	—	—	0.6	—	V/μs

NOTES:
1. Output will swing to ground
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.
4. T_{low} = −55°C for MC3505 T_{high} = +125°C for MC3505
   = 0°C for MC3405 = +70°C for MC3405

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Single Supply	V_{CC}	36	Vdc
Split Supplies	V_{CC}, V_{EE}	±18	
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Sink Current	I_{sink}	20	mA
Operating Ambient Temperature Range—MC3505	T_A	-55 to +125	°C
MC3405		0 to +70	
Storage Temperature Range—Ceramic Package	T_{stg}	-65 to +150	°C
Plastic Package		-55 to +125	
Operating Junction Temperature Range—Ceramic Package	T_J	175	°C
Plastic Package		150	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted)

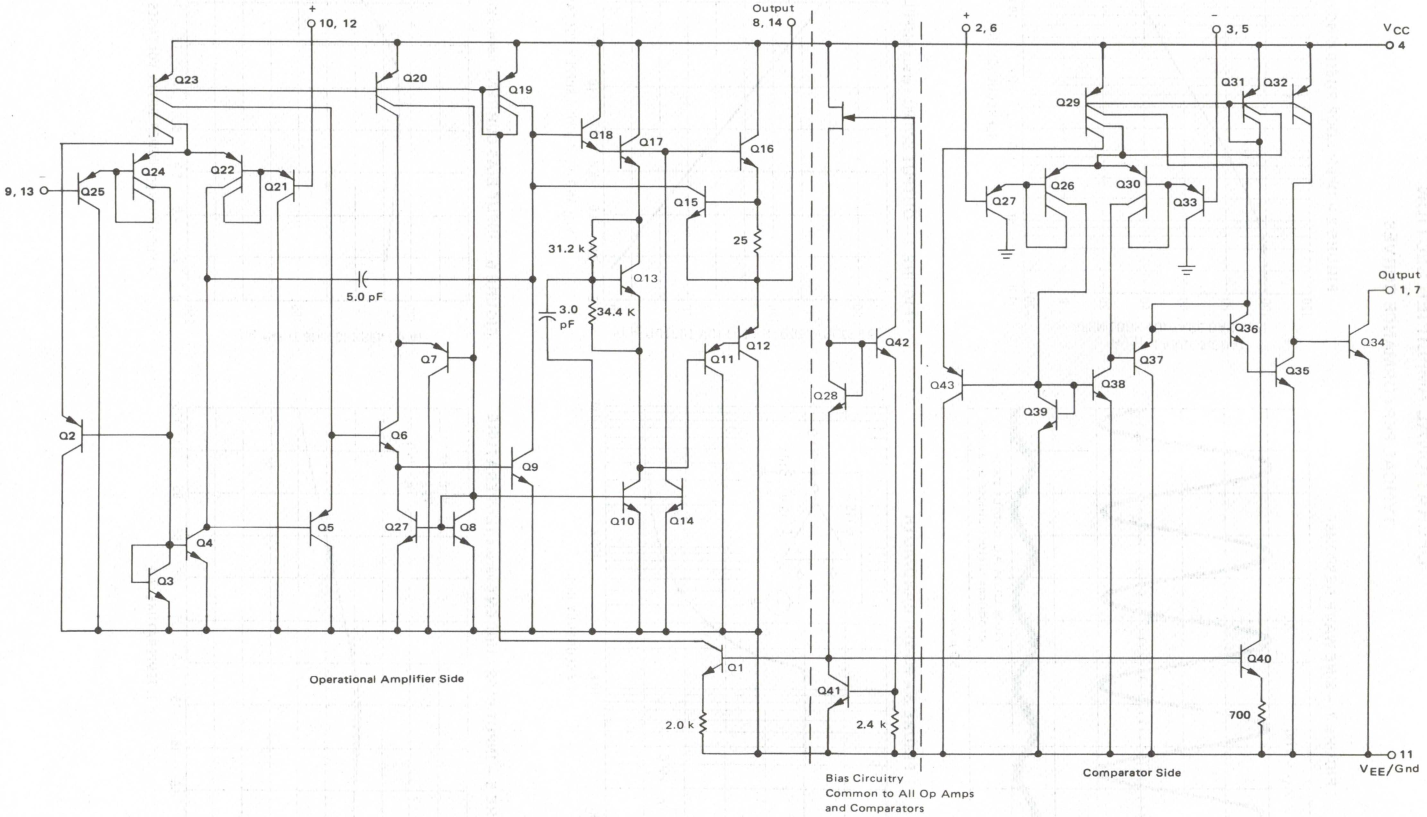
Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
($T_A = T_{low}$ to T_{high}) (Notes 1 and 2)		–	–	9.0	–	–	12	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	μV/°C
Input Offset Current	I_{IO}	–	50	75	–	50	100	nA
($T_A = T_{low}$ to T_{high}) (Note 1)		–	–	150	–	–	200	
Input Bias Current	I_{IB}	–	-125	-500	–	-125	-500	nA
($T_A = T_{low}$ to T_{high}) (Note 1)		–	–	-1500	–	–	-800	
Input Common Mode Voltage Range	V_{ICR}	0	V_{CC} -1.5	V_{CC} -1.7	0	V_{CC} -1.5	V_{CC} -1.7	Vp-p
($T_A = T_{low}$ to T_{high}) (Note 1)		0	V_{CC} -1.7	V_{CC} -2.0	0	V_{CC} -1.7	V_{CC} -2.0	
Input Differential Voltage (All $V_{in} \geq 0$ Vdc)	V_{ID}	–	–	36	–	–	36	V
Large-Signal Open-Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	–	200	–	–	200	–	V/mV
Output Sink Current ($V_{in}(-) \geq 1.0$ Vdc, $V_{in}(+) = 0$, $V_O \leq 1.5$ V)	I_{sink}	6.0	16	–	6.0	16	–	mA
Low Level Output Voltage ($V_{in}(+) = 0$ V, $V_{in}(-) = 1.0$ V, I_{sink} = 4.0 mA)	V_{OL}	–	350	500	–	350	500	mV
($T_A = T_{low}$ to T_{high}) (Note 1)		–	–	700	–	–	700	
Output Leakage Current ($V_{in}(+) \geq 1.0$ Vdc, $V_{in}(-) = 0$, V_O = 5.0 Vdc)	I_{OL}	–	0.1	1.0	–	0.1	1.0	μA
($T_A = T_{low}$ to T_{high}) (Note 1)		–	0.1	1.0	–	0.1	1.0	
Large-Signal Response	–	–	300	–	–	300	–	ns
Response Time (Note 3) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	–	1.3	–	μs

NOTES: 1. T_{low} = -55°C for MC3505 T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

2. $V_O \cong 1.4$ V, $R_S = 0$ Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} – 1.7 V.

3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)


+
10, 12
Output
8, 14
+
2, 6
−
3, 5
VCC
4
Q23
Q20
Q19
Q18
Q17
Q16
Q24
Q22
Q21
Q25
9, 13
−
Q15
25
31.2 k
Q13
5.0 pF
3.0 pF
34.4 K
Q12
Q11
Q7
Q6
Q2
Q9
Q10
Q14
Q5
Q27
Q8
Q4
Q3
Q1
2.0 k
Operational Amplifier Side
Q42
Q28
Q41
2.4 k
Bias Circuitry Common to All Op Amps and Comparators
Q29
Q31
Q32
Q26
Q30
Q27
Q33
Output
1, 7
Q36
Q34
Q37
Q43
Q38
Q39
Q35
Q40
700
11
VEE/Gnd
Comparator Side

OPERATIONAL AMPLIFIER SECTION

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

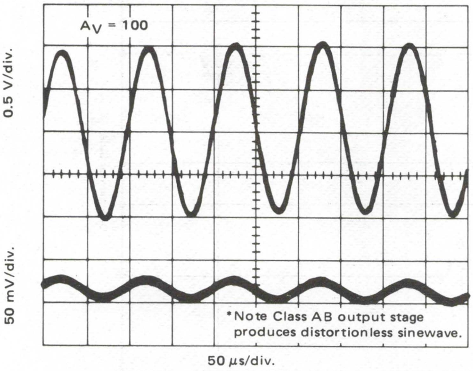


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

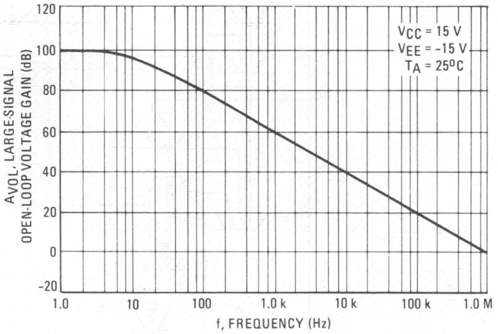


FIGURE 3 – POWER BANDWIDTH

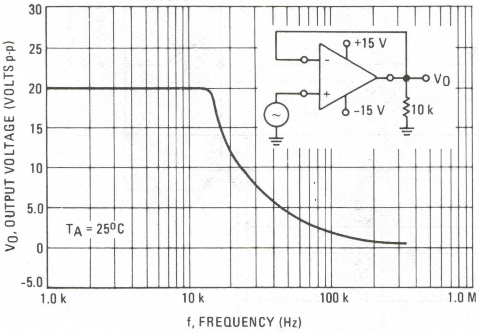


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

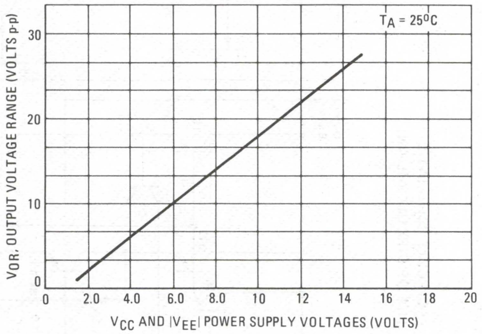


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

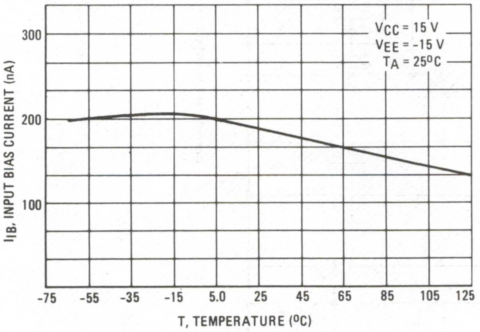
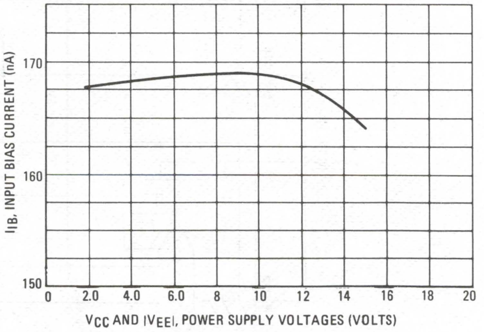


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



COMPARATOR SECTION

TYPICAL PERFORMANCE CURVES

FIGURE 7 — NORMALIZED INPUT OFFSET VOLTAGE

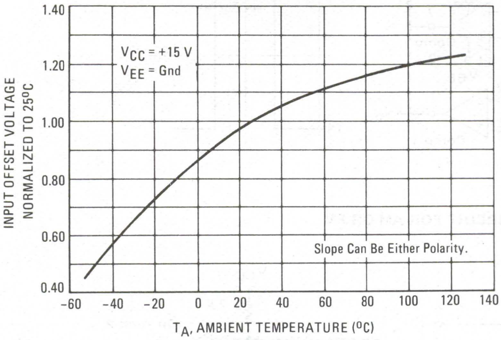


FIGURE 8 — INPUT BIAS CURRENT

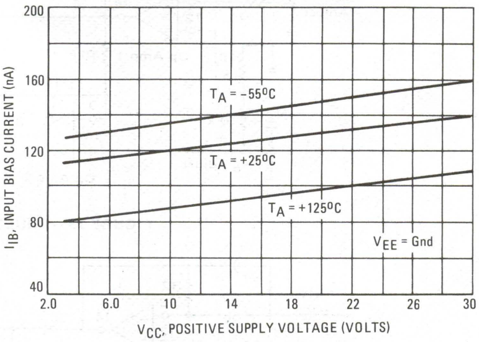


FIGURE 9 — NORMALIZED INPUT OFFSET CURRENT

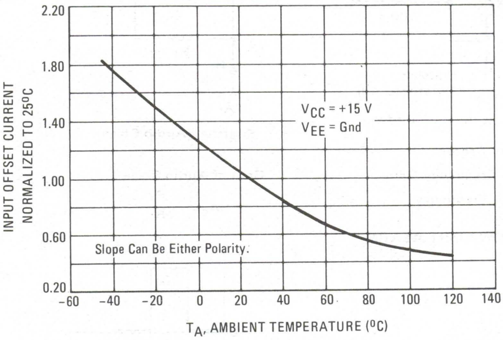
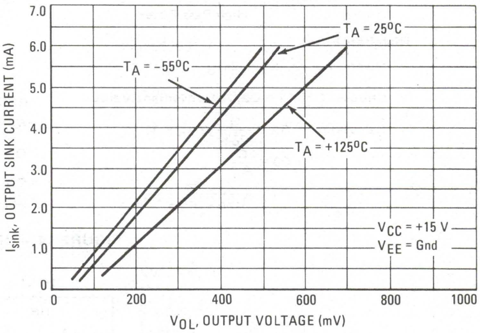
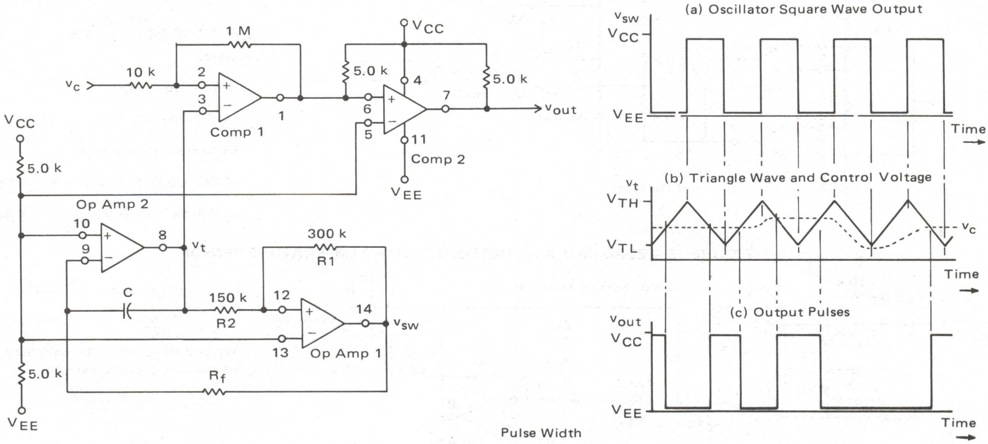


FIGURE 10 — OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



APPLICATIONS INFORMATION

FIGURE 11 — PULSE WIDTH MODULATOR SCHEMATIC AND WAVEFORMS


VCC
1 M
10 k
vc
2
3
Comp 1
1
5.0 k
4
6
5
7
11
Comp 2
5.0 k
vout
VEE
VCC
5.0 k
Op Amp 2
10
9
8
vt
300 k
R1
C
150 k
R2
12
13
14
vsw
Op Amp 1
5.0 k
Rf
VEE
(a) Oscillator Square Wave Output
vsw
VCC
VEE
Time
(b) Triangle Wave and Control Voltage
vt
VTH
VTL
vc
Time
(c) Output Pulses
vout
VCC
VEE
Time

$V_{TH} = \frac{1}{2}V_S(1 + R2/R1) + V_{EE}$ $\quad V_S = V_{CC} - V_{EE}$

$V_{TL} = \frac{1}{2}V_S(1 - R2/R1) + V_{EE}$

Oscillator Frequency

$f = \frac{R1}{4R_fCR2}$

Pulse Width

$P.W. = \left(\frac{1}{f}\right)\left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right)$ When: $V_{TL} < V_c < V_{TH}$

Duty Cycle in %

$D.C. = \left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$

FIGURE 12 – WINDOW COMPARATOR

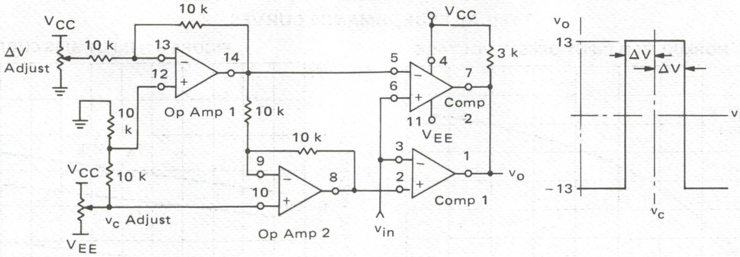
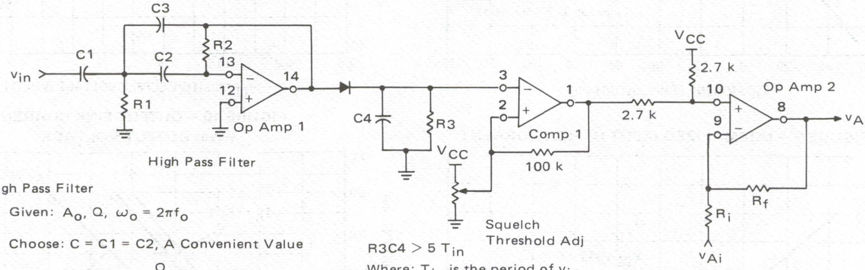

10 k
VCC
ΔV Adjust
10 k
13
12
14
Op Amp 1
10 k
10 k
VCC
10 k
vc Adjust
VEE
10 k
9
10
8
Op Amp 2
5
6
4
7
3 k
Comp 2
11
VEE
3
2
1
Comp 1
vo
vin
vo
13
ΔV
ΔV
vin
–13
vc

FIGURE 13 – SQUELCH CIRCUIT FOR AM OR FM


C3
C1
C2
R2
vin
13
12
14
R1
Op Amp 1
High Pass Filter
C4
R3
3
2
1
Comp 1
VCC
100 k
Squelch Threshold Adj
VCC
2.7 k
2.7 k
10
9
Op Amp 2
8
vAo
Rf
Ri
vAi

Switched Audio Stage

High Pass Filter

Given: A_o, Q, $\omega_o = 2\pi f_o$

Choose: C = C1 = C2, A Convenient Value

Calculate: $R2 = \frac{Q}{\omega_o C}(2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\,T_{in}$

Where: T_{in} is the period of v_{in}

Q = Quality Factor

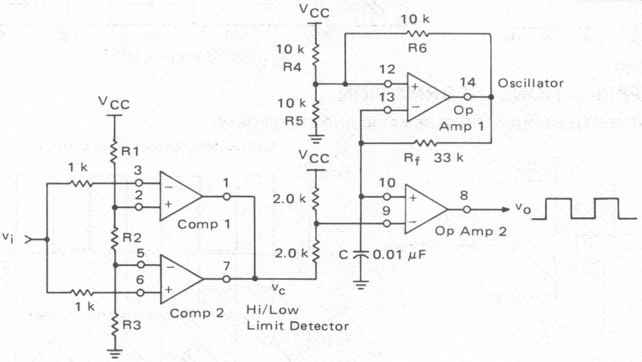
A_o = High Frequency Gain

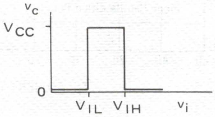
ω_o = Break Frequency

Gain of Audio Stage

$A_{cl} = -\frac{R_f}{R_i}$

FIGURE 14 – HIGH/LOW LIMIT ALARM


VCC
10 k
R4
10 k
R5
10 k
R6
12
13
14
Oscillator
Op Amp 1
Rf 33 k
VCC
R1
1 k
3
2
1
Comp 1
vi
R2
5
6
7
Comp 2
1 k
R3
VCC
2.0 k
2.0 k
C 0.01 µF
10
9
8
Op Amp 2
vo
vc
Hi/Low Limit Detector



$V_{IL} = V_{CC}\frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

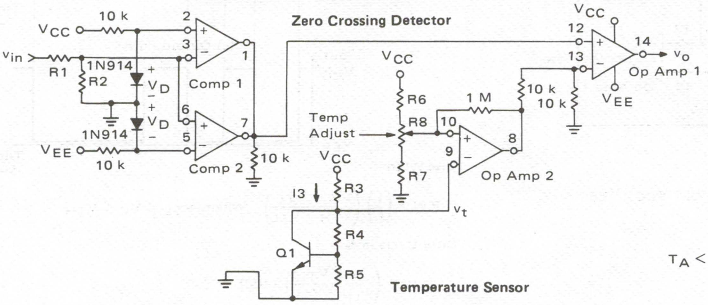
$f = 0.72/R_fC$

As Shown, f = 2.2 kHz

v_o Will Oscillate If $V_{IH} < v_i$, or $V_{IL} > v_i$

v_o Will Be Low If $V_{IL} < v_i < V_{IH}$

FIGURE 15 – ZERO CROSSING DETECTOR WITH TEMPERATURE SENSOR


10 k
VCC
vin
R1
1N914
R2
VD
VD
1N914
VEE
10 k
2
3
1
Comp 1
6
5
7
Comp 2
10 k
Zero Crossing Detector
VCC
R6
R8
Temp Adjust
R7
1 M
10
9
8
Op Amp 2
10 k
10 k
VCC
12
13
14
vo
Op Amp 1
VEE
VCC
I3
R3
vt
R4
Q1
R5
Temperature Sensor

$v_t = (V_{BE} \text{ of Q1})\left(\frac{R4 + R5}{R5}\right)$

$I3 > \frac{2V_{BE}}{R5}$

R1 and R2 control the switching voltage of the zero crossing detector

$\pm V_s = \pm V_D\,\frac{R1 + R2}{R2}$

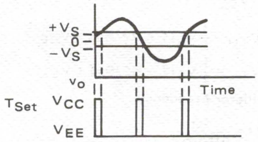
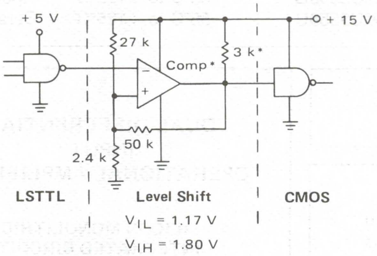
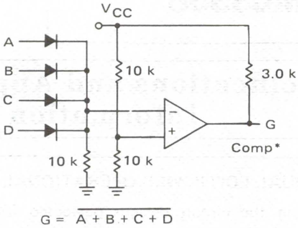


FIGURE 16 – LSTTL to CMOS INTERFACE WITH HYSTERESIS


+ 5 V
+ 15 V
27 k
3 k*
Comp*
50 k
2.4 k
LSTTL
Level Shift
CMOS
V_{IL} = 1.17 V
V_{IH} = 1.80 V

*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

FIGURE 17 – "NOR" GATE


V_{CC}
A
B
C
D
10 k
3.0 k*
G
Comp*
10 k
10 k
G = $\overline{A + B + C + D}$

*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

MC3458
MC3558
MC3358

ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	−40°C to +85°C	Plastic DIP
MC3458G	0°C to +70°C	Metal Can
MC3458P1	0°C to +70°C	Plastic DIP
MC3458U	0°C to +70°C	Ceramic DIP
MC3558G	−55°C to +125°C	Metal Can
MC3558U	−55°C to +125°C	Ceramic DIP

Specifications and Applications Information

DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC} V_{EE}	+18 −18	
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Input Forward Current ($V_I < -0.3$ V)	I_{IF}	50	mA
Junction Temperature	T_J		°C
Ceramic and Metal Packages		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}		°C
Ceramic and Metal Packages		−65 to +150	
Plastic Package		−55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3558		−55 to +125	
MC3458		0 to +70	
MC3358		−40 to +85	

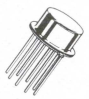
(1) Split Power Supplies.

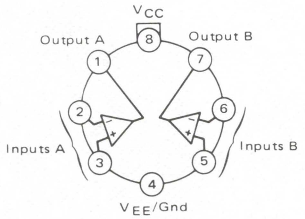
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

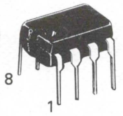
G SUFFIX
METAL PACKAGE
CASE 601-04



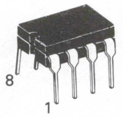


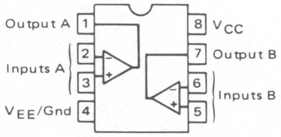
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC3458, MC3358 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693





(Top View)

ELECTRICAL CHARACTERISTICS (For MC3558, MC3458, V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted.) (For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage T_A = T_{high} to T_{low} (1)	V_{IO}	– –	2.0 –	5.0 6.0	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current T_A = T_{high} to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	A_{VOL}	 50 25	 200 300	 – –	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current T_A = T_{high} to T_{low}	I_{IB}	– –	-200 -300	-500 -1500	– –	-200 –	-500 -800	– –	-200 –	-500 -1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	V_{OR}	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+12 V -V_{EE}	+12.5 V -V_{EE}	–	V
Common-Mode Rejection Ratio $R_S \leqslant$ 10 kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_o = 0) R_L = ∞	I_{CC}, I_{EE}	–	1.6	2.2	–	1.6	3.7	–	1.6	3.7	mA
Individual Output Short-Circuit Current (2)	$I_{OS}\pm$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_o = 20 V(p-p), THD = 5%	BW_P	–	9.0	–	–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_o = 50 mV	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_o = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	φm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	–	–	1.0	–	–	1.0	–	–	1.0	–	%

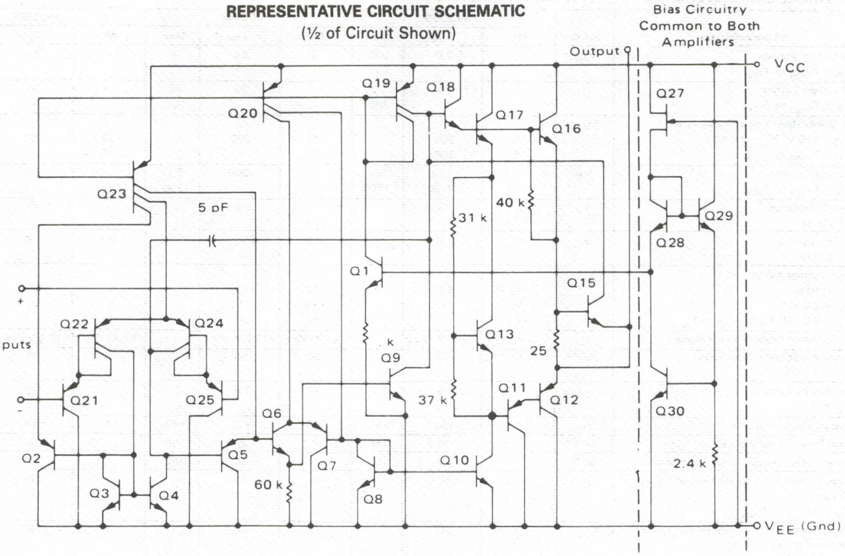
(1) T_{high} = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358.
T_{low} = -55°C for MC3558, 0°C for MC3458, -40°C for MC3358.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

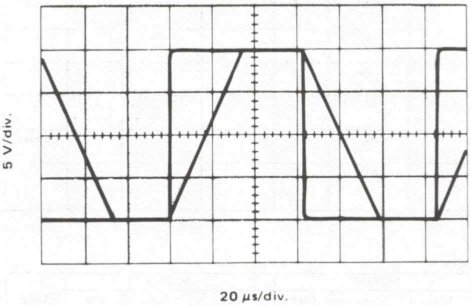
Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 V $\leqslant V_{CC} \leqslant$ 30 V	V_{OR}	 3.3 –	 3.5 V_{CC}-1.7 V	 – –	 3.3 –	 3.5 V_{CC} -1.7 V	 – –	 3.3 –	 3.5 V_{CC} -1.7 V	 – –	Vp-p
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

REPRESENTATIVE CIRCUIT SCHEMATIC
(½ of Circuit Shown)


Bias Circuitry
Common to Both
Amplifiers
Output
VCC
VEE (Gnd)
Inputs
+
-
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q27
Q28
Q29
Q30
5 pF
31 k
40 k
k
37 k
25
60 k
2.4 k

INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

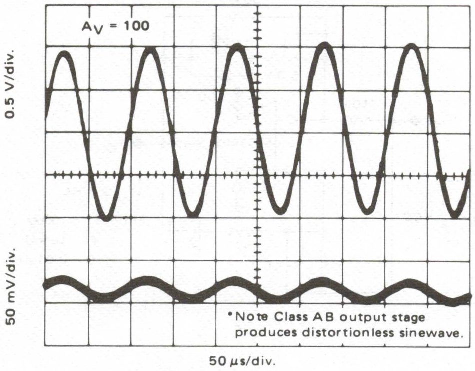
The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE



*Note Class AB output stage produces distortionless sinewave.

FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

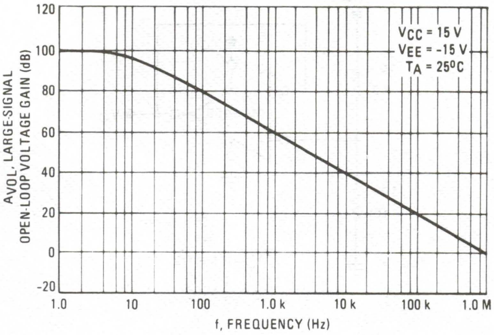


FIGURE 3 – POWER BANDWIDTH

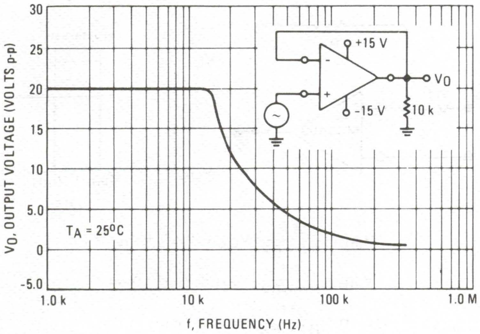


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

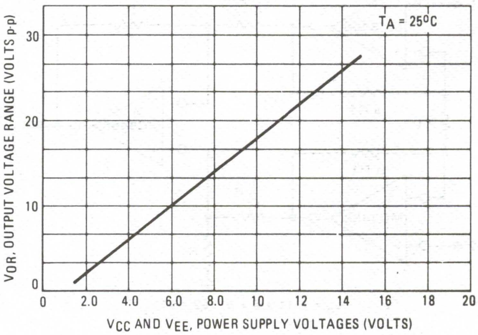


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

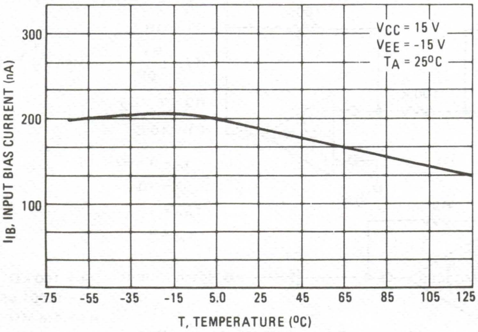
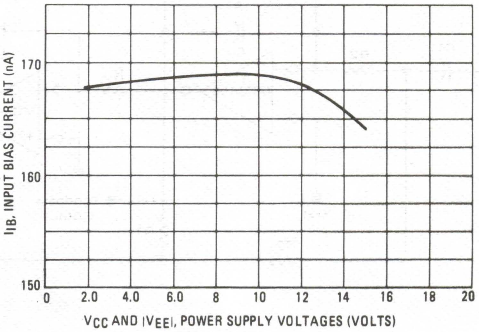
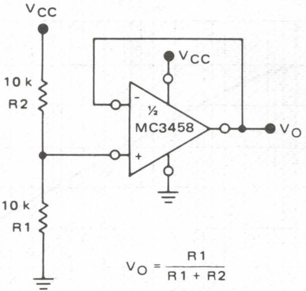


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

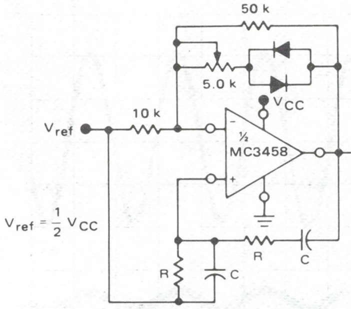
FIGURE 7 – VOLTAGE REFERENCE


V_CC
10 k
R2
V_CC
½
MC3458
V_O
10 k
R1

$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

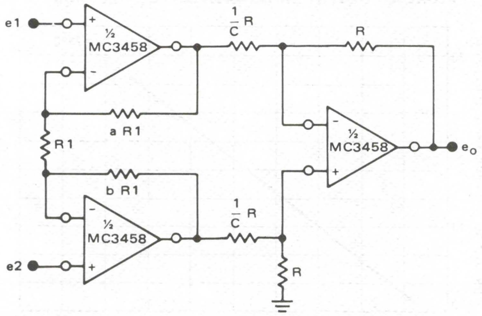

50 k
5.0 k
V_CC
10 k
V_ref
½
MC3458
V_O
R
C
R
C

$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

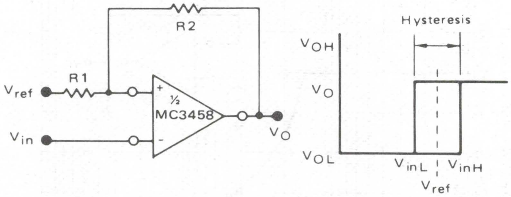
For $f_o = 1$ kHz
$R = 16$ kΩ
$C = 0.01$ µF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
½
MC3458
1/C R
R
a R1
R1
½
MC3458
e_o
b R1
½
MC3458
1/C R
e2
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

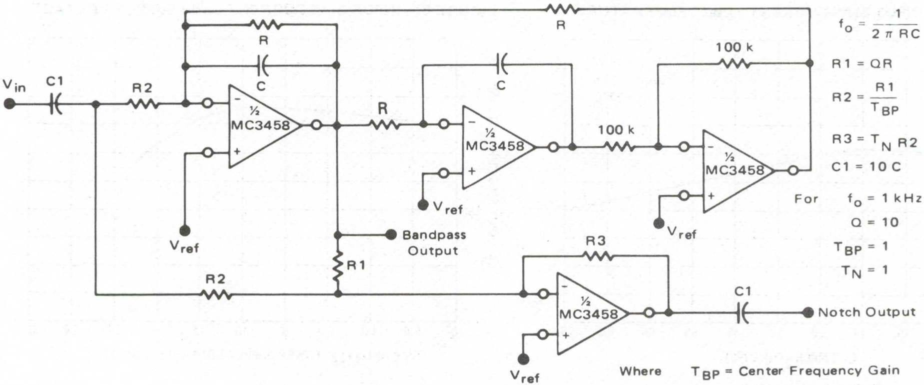

R2
R1
V_ref
½
MC3458
V_in
V_O
Hysteresis
V_OH
V_O
V_OL
V_inL
V_inH
V_ref

$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER


R
R
C
V_in
C1
R2
½
MC3458
V_ref
R
C
½
MC3458
V_ref
100 k
100 k
½
MC3458
V_ref
Bandpass Output
R1
R2
R3
½
MC3458
V_ref
C1
Notch Output

$$f_o = \frac{1}{2 \pi RC}$$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

$$V_{ref} = \frac{1}{2} V_{CC}$$

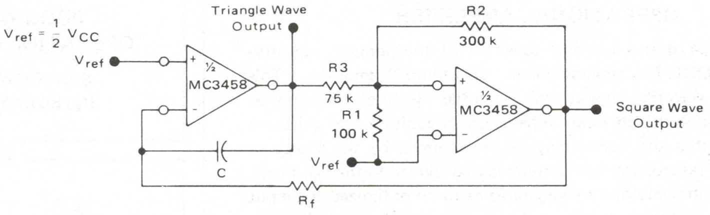
For $f_o = 1$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160$ kΩ
$C = 0.001$ µF
$R1 = 1.6$ MΩ
$R2 = 1.6$ MΩ
$R3 = 1.6$ MΩ

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

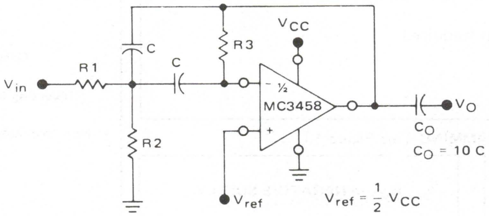
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR


$V_{ref} = \frac{1}{2} V_{CC}$
V_{ref}
Triangle Wave Output
+
½
MC3458
–
C
R3
75 k
R1
100 k
V_{ref}
R2
300 k
+
½
MC3458
–
Square Wave Output
R_f

$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\;R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


V_{in}
R1
C
C
R2
R3
V_{CC}
–
½
MC3458
+
V_O
C_O
$C_O = 10\ C$
V_{ref}
$V_{ref} = \frac{1}{2} V_{CC}$

Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\;R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3476

MOTOROLA

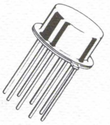
LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

The MC3476 is a low-cost selection of the popular, industry-standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

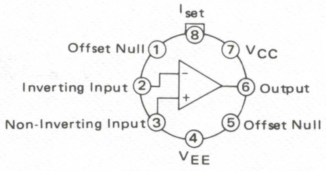
- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

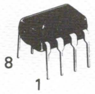
SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-04

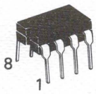

Iset
8
Offset Null 1
7 VCC
Inverting Input 2
6 Output
Non-Inverting Input 3
5 Offset Null
4
VEE

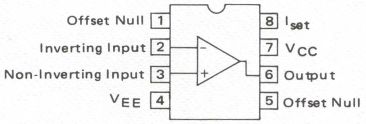
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

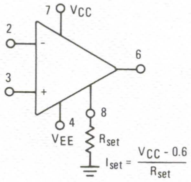



Offset Null 1
Inverting Input 2
Non-Inverting Input 3
VEE 4
8 Iset
7 VCC
6 Output
5 Offset Null

(Top View)

RESISTIVE PROGRAMMING (See Figure 1.)

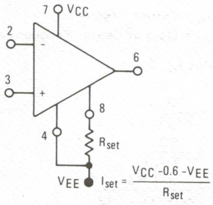
R_{set} to GROUND


7 VCC
2
3
6
8
4
VEE
Rset

$$I_{set} = \frac{V_{CC} - 0.6}{R_{set}}$$

Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	560 kΩ	360 kΩ
±9.0 V	820 kΩ	560 kΩ
±12 V	1.0 MΩ	750 kΩ
±15 V	1.5 MΩ	1.0 MΩ

R_{set} to NEGATIVE SUPPLY

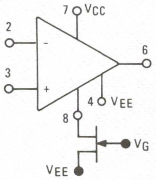

7 VCC
2
3
6
8
4
Rset
VEE

$$I_{set} = \frac{V_{CC} - 0.6 - V_{EE}}{R_{set}}$$

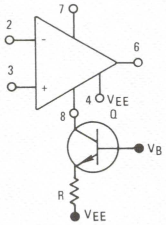
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	1.0 MΩ	820 kΩ
±9.0 V	1.8 MΩ	1.2 MΩ
±12 V	2.2 MΩ	1.5 MΩ
±15 V	2.7 MΩ	2.0 MΩ

ACTIVE PROGRAMMING

FET CURRENT SOURCE


7 VCC
2
3
6
4 VEE
8
VG
VEE

BIPOLAR CURRENT SOURCE


7
2
3
6
4 VEE
8
Q
VB
R
VEE

Pins not shown are not connected.

ORDERING INFORMATION

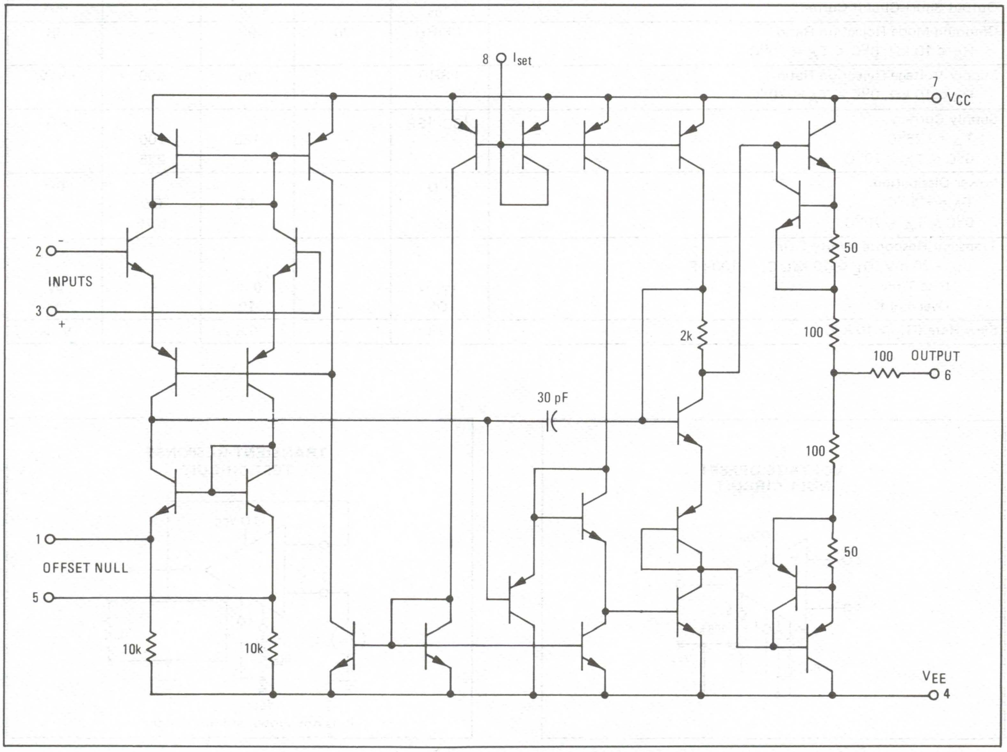
Device	Temperature Range	Package
MC3476G	0 to +70°C	Metal Can
MC3476P1	0 to +70°C	Plastic DIP
MC3476U	0 to +70°C	Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common-Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}−0.6 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_S	Indefinite	s
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C

*Short-Circuit to ground with $I_{set} \leqslant 15\ \mu A$. Rating applies up to ambient temperature of +70°C.

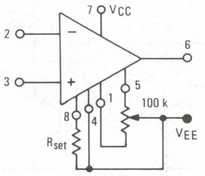
EQUIVALENT SCHEMATIC DIAGRAM



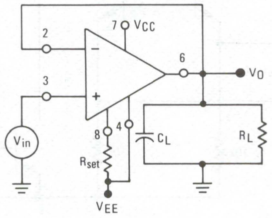
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 15 µA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ 70°C		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
T_A = 70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = 70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Input Common-Mode Voltage Range 0°C ≤ T_A ≤ 70°C	V_{ICR}	±10	–	–	V
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 10$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \geq 10$ kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ 70°C		25 k	–	–	
Output Voltage Range	V_{OR}				V
$R_L \geq 10$ kΩ, T_A = +25°C		±12	±13	–	
$R_L \geq 10$ kΩ, 0°C ≤ T_A ≤ 70°C		±12	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short-Circuit Current	I_{os}	–	12	–	mA
Common-Mode Rejection Ratio $R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C	CMRR	70	90	–	dB
Supply Voltage Rejection Ratio $R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C	PSRR	–	25	200	µV/V
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ 70°C		–	–	225	
Power Dissipation	P_D				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ 70°C		–	–	6.75	
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geq 10$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	µs
Overshoot	OS	–	10	–	%
Slew Rate ($R_L \geq 10$ kΩ)	SR	–	0.8	–	V/µs

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected.

TYPICAL CHARACTERISTICS

(T$_A$ = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

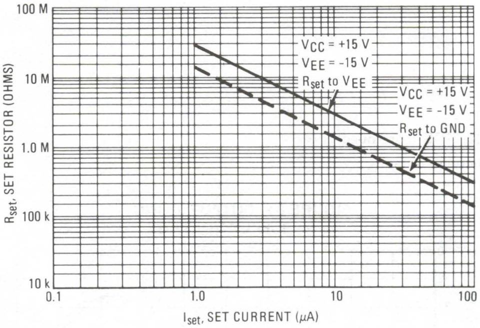


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

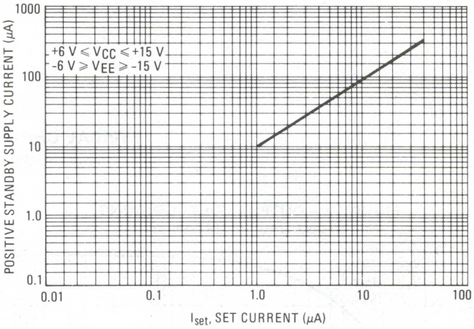


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

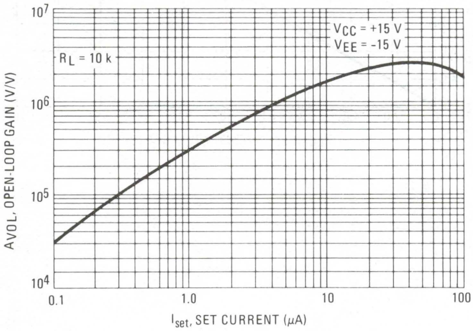


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

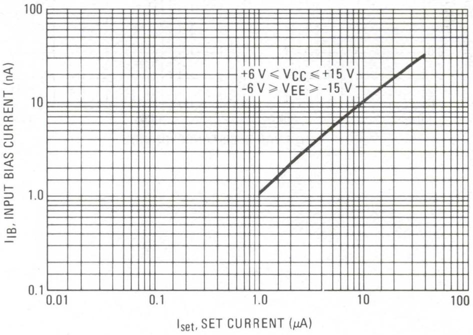


FIGURE 5 – SLEW RATE versus SET CURRENT

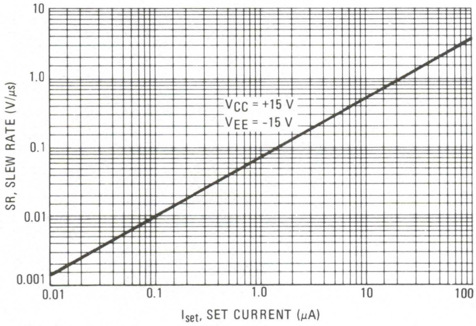
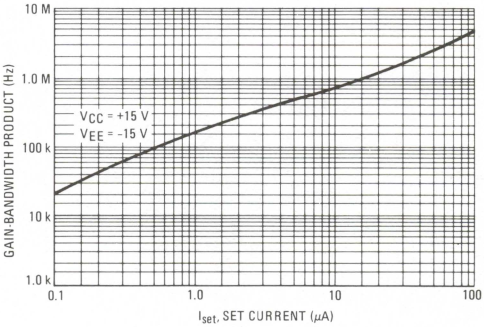


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

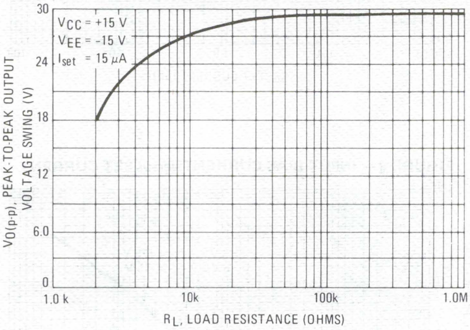
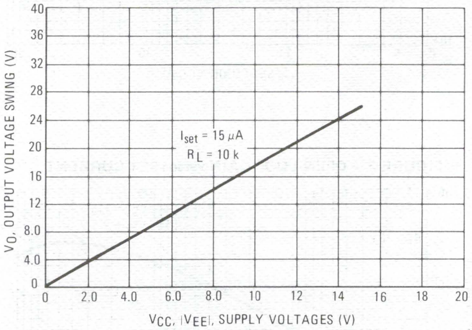


FIGURE 8 – OUTPUT SWING versus SUPPLY VOLTAGE



MOTOROLA

MC4558, MC4558AC, MC4558C, MC4558N, MC4558NC

DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558, MC4558AC, and MC4558C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

- **2.5 MHz Unity Gain Bandwidth Guaranteed on MC4558 and MC4558AC**
- **2 MHz Unity Gain Bandwidth Guaranteed on MC4558C**
- Internally Compensated
- Short-Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption
- Low Noise Selections Offered — N Suffix

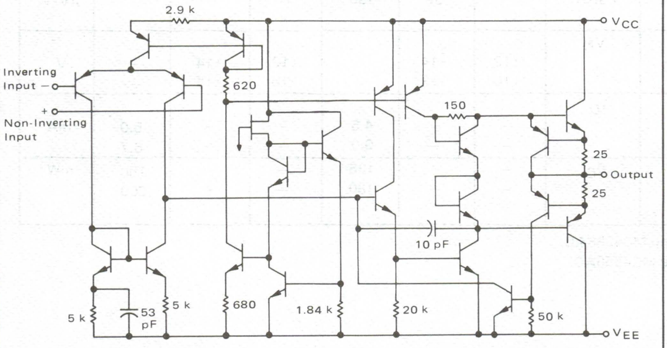
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC4558 MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	See Ordering Information Below		
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 −65 to +150 −55 to +125		°C
Junction Temperature Metal and Ceramic Packages Plastic Package	T_J	 175 150		°C

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Short circuit may be to ground or either supply.

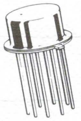
EQUIVALENT CIRCUIT SCHEMATIC
(1/2 of Circuit Shown)



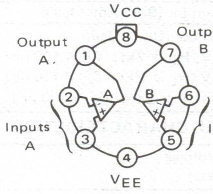
2.9 k
V_{CC}
Inverting Input
+
Non-Inverting Input
620
150
25
Output
25
10 pF
5 k
53 pF
5 k
680
1.84 k
20 k
50 k
V_{EE}

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

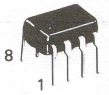


G SUFFIX
METAL PACKAGE
CASE 601-04



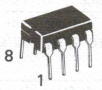
V_{CC}
Output A
Output B
8
1
7
2
6
A
B
Inputs A
Inputs B
3
5
4
V_{EE}

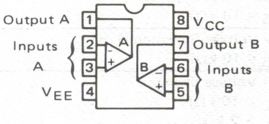
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

U SUFFIX
CERAMIC PACKAGE
CASE 693-02





Output A
Inputs A
V_{EE}
1
2
3
4
A
B
8
7
6
5
V_{CC}
Output B
Inputs B

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC4558G,NG	−55 to +125°C	Metal Can
MC4558NU,U	−55 to +125°C	Ceramic DIP
MC4558CG,NCG	0 to +70°C	Metal Can
MC4558ACP1, CP1,NCP1	0 to +70°C	Plastic DIP
MC4558CU,NCU	0 to +70°C	Ceramic DIP

FREQUENCY CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC4558, MC4558AC Min	MC4558, MC4558AC Typ	MC4558, MC4558AC Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Unity Gain Bandwidth	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC4558, MC4558AC Min	MC4558, MC4558AC Typ	MC4558, MC4558AC Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current†	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leqslant 10$ kΩ)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ kΩ)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing ($R_L \geqslant 10$ kΩ) ($R_L \geqslant 2$ kΩ)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V
Output Short-Circuit Current	I_{os}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain) (V_I = 20 mV, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Rise Time (V_I = 20 mV, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Overshoot (V_I = 10 V, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Slew Rate	t_{TLH} os SR	– – 1.5	0.3 15 1.6	– – –	– – 1.0	0.3 15 1.6	– – –	μs % V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC4558, MC4558AC Min	MC4558, MC4558AC Typ	MC4558, MC4558AC Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Input Offset Voltage ($R_S \leqslant 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current ($T_A = T_{high}$) ($T_A = T_{low}$) (T_A = 0°C to +70°C)	I_{IO}	– – –	7.0 85 –	200 500 –	– – –	– – –	– – 300	nA
Input Bias Current ($T_A = T_{high}$) ($T_A = T_{low}$) (T_A = 0°C to +70°C)	I_{IB}	– – –	30 300 –	500 1500 –	– – –	– – –	– – 800	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 kΩ)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio ($R_S \leqslant 10$ kΩ)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leqslant 10$ kΩ)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing ($R_L \geqslant 10$ kΩ) ($R_L \geqslant 2$ kΩ)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V
Supply Currents (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	I_D	– –	– –	4.5 6.0	– –	– –	5.0 6.7	mA
Power Consumption (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	P_C	– –	– –	135 180	– –	– –	150 200	mW

*T_{high} = 125°C for MC4558 and 70°C for MC4558C and MC4558AC.
T_{low} = −55°C for MC4558 and 0°C for MC4558C and MC4558AC.

†I_{IB} is out of the amplifier due to PNP input transistors.

NOISE CHARACTERISTICS (Applies for MC4558N and MC4558NC only, V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristic	Symbol	MC4558N			MC4558NC			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 kΩ) (Input Referenced)	E_n	–	–	20	–	–	20	μVpeak

FIGURE 1 — BURST NOISE versus SOURCE RESISTANCE

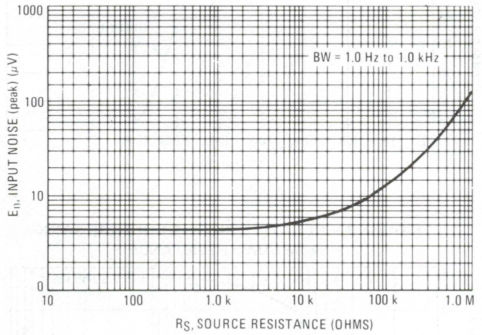


FIGURE 2 — RMS NOISE versus SOURCE RESISTANCE

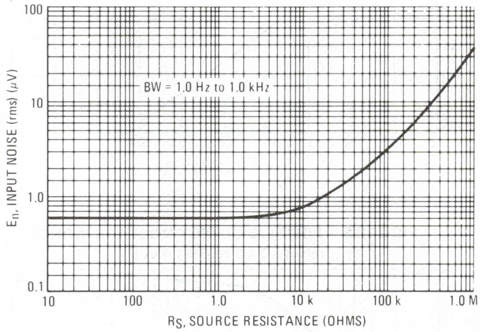


FIGURE 3 — OUTPUT NOISE versus SOURCE RESISTANCE

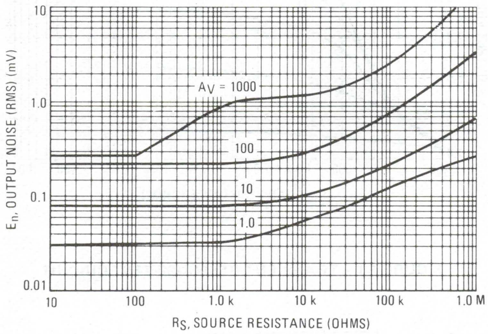


FIGURE 4 — SPECTRAL NOISE DENSITY

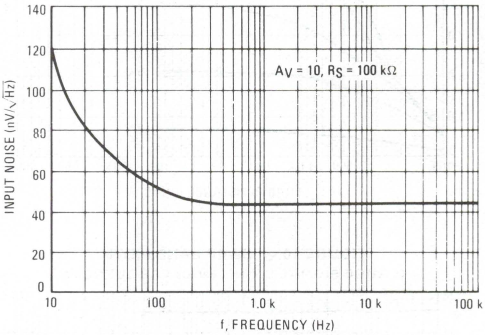
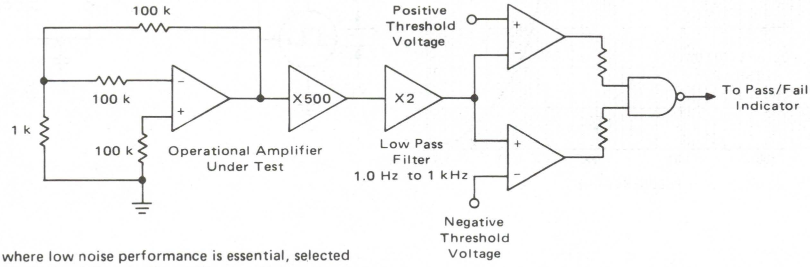


FIGURE 5 — BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)


100 k
100 k
1 k
100 k
Operational Amplifier Under Test
X500
X2
Low Pass Filter 1.0 Hz to 1 kHz
Positive Threshold Voltage
Negative Threshold Voltage
To Pass/Fail Indicator

For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

FIGURE 6 – OPEN LOOP FREQUENCY RESPONSE

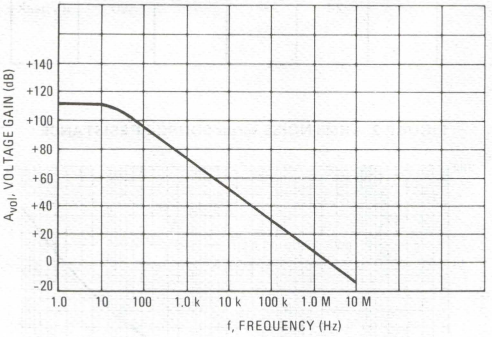


FIGURE 7 – PHASE MARGIN versus FREQUENCY

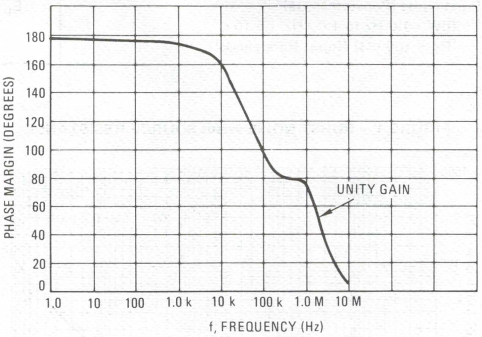


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

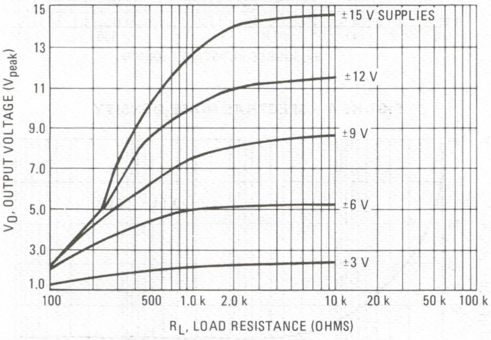


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

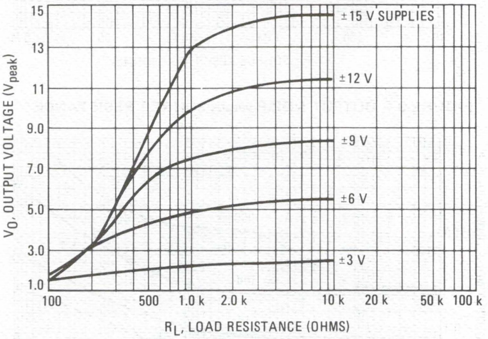


FIGURE 10 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

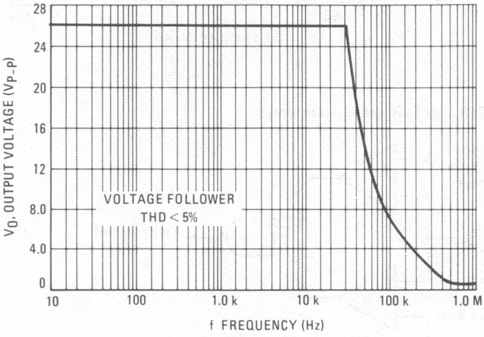
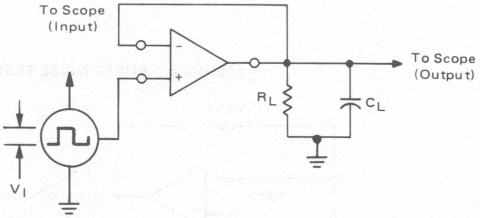


FIGURE 11 – TRANSIENT RESPONSE TEST CIRCUIT



ORDERING INFORMATION

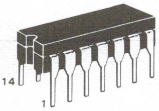
Device	Temperature Range	Package
MC4741L	−55°C to +125°C	Ceramic DIP
MC4741CL	0°C to +70°C	Ceramic DIP
MC4741CP	0°C to +70°C	Plastic DIP

MC4741
MC4741C

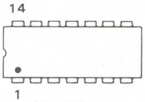
Specifications and Applications Information

QUAD MC1741
DIFFERENTIAL INPUT
OPERATIONAL AMPLIFIERS

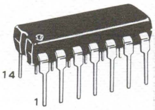
SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



(Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

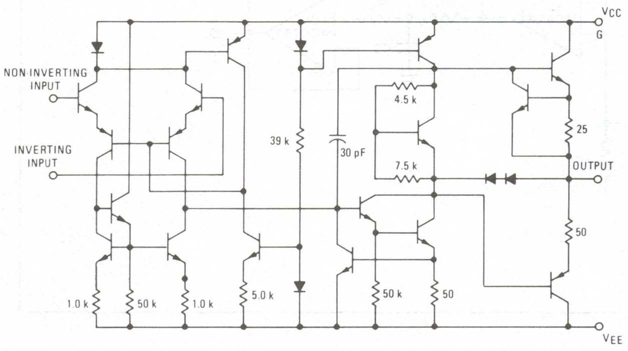
QUAD MC1741 OPERATIONAL AMPLIFIERS

The MC4741 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

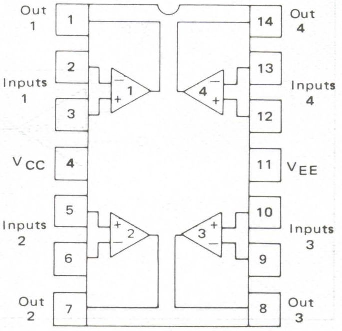
The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)


VCC
G
NON-INVERTING INPUT
INVERTING INPUT
4.5 k
39 k
30 pF
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE

PIN CONNECTIONS


Out 1
1
2
Inputs 1
3
VCC
4
5
Inputs 2
6
Out 2
7
14
Out 4
13
Inputs 4
12
11
VEE
10
Inputs 3
9
8
Out 3
1
2
3
4

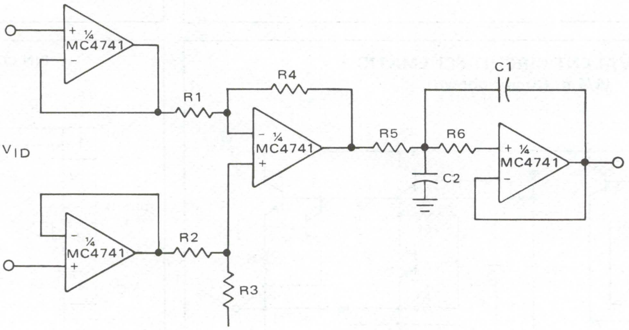
(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc Vdc
Input Differential Voltage	V_{ID}	±44	±36	Volts
Input Common Mode Voltage	V_{ICM}	±22	±18	Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

TYPICAL APPLICATION

HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

		MC4741			MC4741C			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	30	150	µV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	±12	±14	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	4.0	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	72	120	–	105	210	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	µs
(V_I = 20 mV, R_L ≥ 2 k, C_L ≤ 100 pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, R_L ≥ 2 k, C_L ≤ 100 pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low} unless otherwise noted.)

		MC4741			MC4741C			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = −55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = −55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain (R_L ≥ 2 k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	–	–	–	µV/V
Output Voltage Swing	V_O							V
(R_L ≥ 10 k)		±12	±14	–	–	–	–	
(R_L ≥ 2 k)		±10	±13	–	±10	±13	–	
Supply Currents – (All Amplifiers)	I_D							mA
(T_A = 125°C)		–	2.4	3.4	–	–	–	
(T_A = −55°C)		–	3.6	5.0	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	72	102	–	–	–	mW
(All Amplifiers) (T_A = −55°C)		–	108	150	–	–	–	

*T_{high} = 125°C for MC4741 and 70°C for MC4741C
T_{low} = −55°C for MC4741 and 0°C for MC4741C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

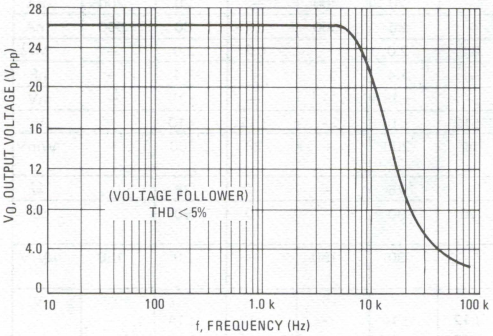


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

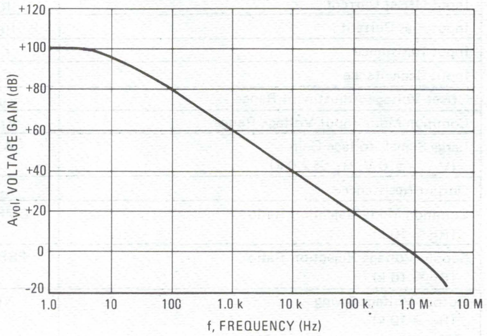


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

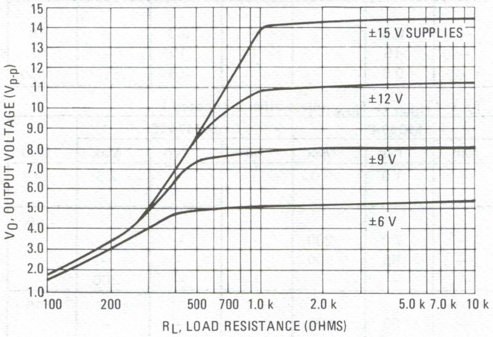


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

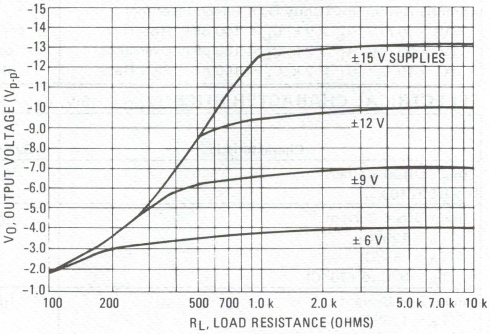


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

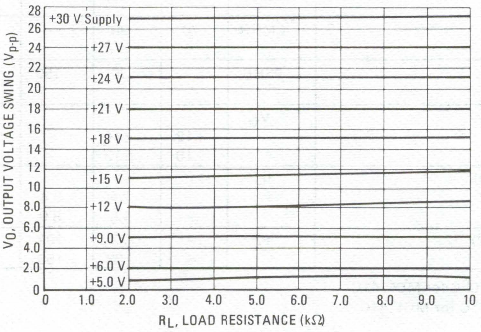


FIGURE 6 — BI-QUAD FILTER

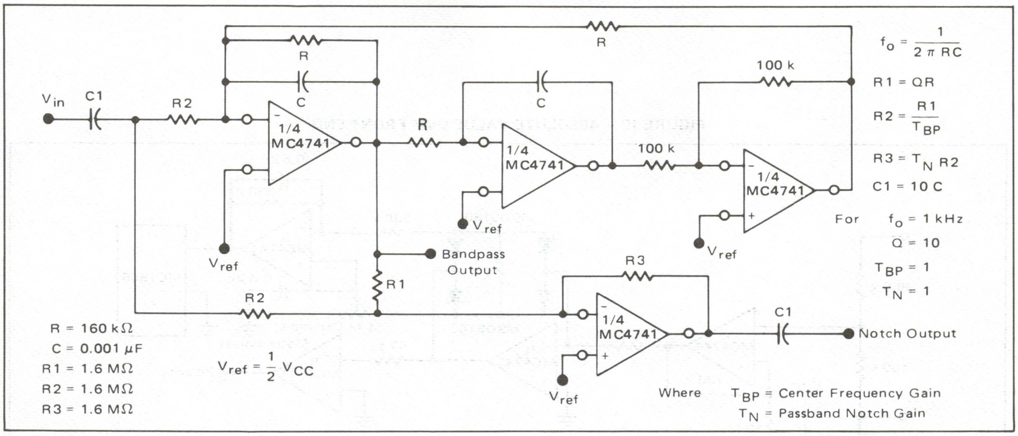

V_in
C1
R2
R
C
1/4 MC4741
V_ref
Bandpass Output
R1
R2
R
C
1/4 MC4741
V_ref
R
100 k
100 k
1/4 MC4741
V_ref
R3
1/4 MC4741
V_ref
C1
Notch Output
R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
V_ref = 1/2 V_CC
f_o = 1/(2 π RC)
R1 = QR
R2 = R1/T_BP
R3 = T_N R2
C1 = 10 C
For f_o = 1 kHz
Q = 10
T_BP = 1
T_N = 1
Where T_BP = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 7 — NONINVERTING PULSE RESPONSE

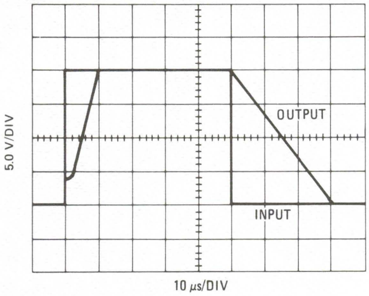


FIGURE 8 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

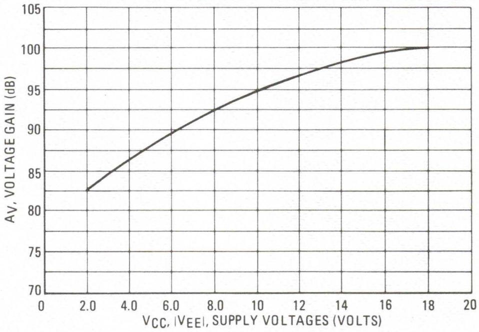


FIGURE 9 — TRANSIENT RESPONSE TEST CIRCUIT

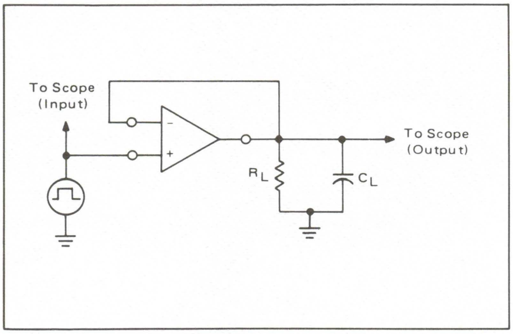
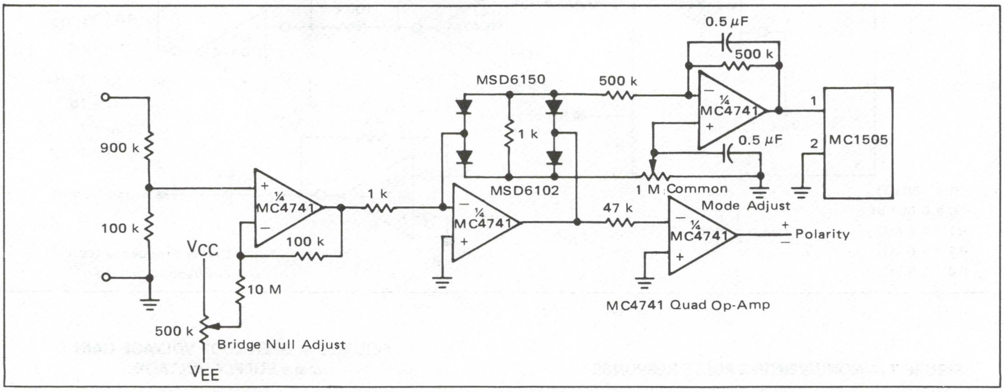

To Scope (Input)
To Scope (Output)
R_L
C_L

FIGURE 10 – ABSOLUTE VALUE DVM FRONT END


0.5 μF
500 k
MSD6150
500 k
¼ MC4741
1
MC1505
2
0.5 μF
900 k
1 k
¼ MC4741
1 k
MSD6102
1 M Common Mode Adjust
¼ MC4741
47 k
¼ MC4741
Polarity
100 k
VCC
100 k
10 M
500 k
Bridge Null Adjust
VEE
MC4741 Quad Op-Amp

MOTOROLA

MC34001, MC35001
MC34002, MC35002
MC34004, MC35004

JFET-INPUT OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC INTEGRATED CIRCUITS

JFET-INPUT OPERATIONAL AMPLIFIERS

These low cost JFET-Input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

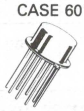
The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of −55°C to +125°C and the MC34001/34002/34004 series are specified from 0°C to +70°C.

- Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.8 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

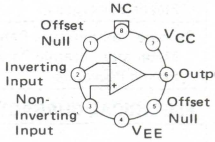
ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34001AG,BG,G	0 to +70°C	Metal Can
	MC34001AP,BP,P	0 to +70°C	Plastic DIP
	MC34001AU,BU,U	0 to +70°C	Ceramic DIP
	MC35001AG,BG,G	−55 to +125°C	Metal Can
	MC35001AU,BU,U	−55 to +125°C	Ceramic DIP
Dual	MC34002AG,BG,G	0 to +70°C	Metal Can
	MC34002AP,BP,P	0 to +70°C	Plastic DIP
	MC34002AU,BU,U	0 to +70°C	Ceramic DIP
	MC35002,AG,BG,G	−55 to +125°C	Metal Can
	MC35002,AU,BU,U	−55 to +125°C	Ceramic DIP
Quad	MC34004BL,L	0 to +70°C	Ceramic DIP
	MC34004BP,P	0 to +70°C	Plastic DIP
	MC35004BL,L	−55 to +125°C	Ceramic DIP

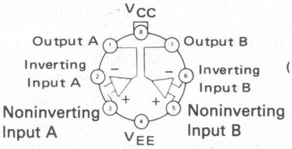
G SUFFIX
METAL PACKAGE
CASE 601-04

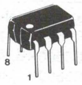


MC34001, MC35001
(Top View)

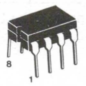

NC
Offset Null
VCC
Inverting Input
Output
Non-Inverting Input
Offset Null
VEE
1
2
3
4
5
6
7
8

MC34002, MC35002
(Top View)


VCC
Output A
Output B
Inverting Input A
Inverting Input B
Noninverting Input A
Noninverting Input B
VEE
1
2
3
4
5
6
7
8

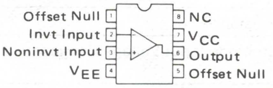


P SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC34001, MC34002 only)

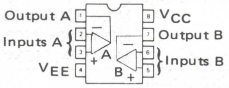


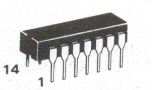
U SUFFIX
CERAMIC PACKAGE
CASE 693-02

MC34001, MC35001
(Top View)

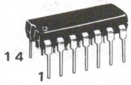

Offset Null
Invt Input
Noninvt Input
VEE
NC
VCC
Output
Offset Null
1
2
3
4
5
6
7
8

MC34002, MC35002
(Top View)

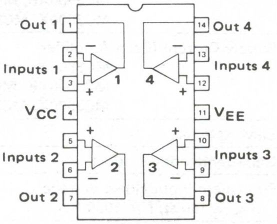

Output A
Inputs A
VEE
VCC
Output B
Inputs B
A
B
1
2
3
4
5
6
7
8



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CAE 646-05
(MC34004 only)


Out 1
Inputs 1
VCC
Inputs 2
Out 2
Out 4
Inputs 4
VEE
Inputs 3
Out 3
1
2
3
4
1
2
3
4
5
6
7
8
9
10
11
12
13
14

MC34004, MC35004 (Top View)

MAXIMUM RATINGS

Rating	Symbol	MC35001 MC35002 MC35004	MC34001 MC34002 MC34004	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range	V_{IDR}	±20	±16	V
Output Short-Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Operating Junction Temperature	T_J			°C
Metal and Ceramic Packages		150	115	
Plastic Packages		—	115	
Storage Temperature Range	T_{stg}			°C
Metal and Ceramic Packages		−65 to +150	−65 to +150	
Plastic Packages		—	−55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25° unless otherwise noted).

Characteristic	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}							mV
MC3500XA, MC3400XA		—	1.0	2.0	—	1.0	2.0	
MC3500XB, MC3400XB		—	3.0	5.0	—	3.0	5.0	
MC3500X, MC3400X		—	5.0	10	—	5.0	10	
Average Temperature Coefficient of Input Offset Voltage R_S ≤ 10 k, T_A = T_{low} to T_{high} (Note 1)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							pA
MC3500XA, MC3400XA		—	10	25	—	25	50	
MC3500XB, MC3400XB		—	10	50	—	25	100	
MC3500X, MC3400X		—	25	100	—	25	100	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							pA
MC3500XA, MC3400XA		—	40	75	—	50	100	
MC3500XB, MC3400XB		—	40	100	—	50	200	
MC3500X, MC3400X		—	50	200	—	50	200	
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 −12	—	±11	+15 −12	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
MC3500XA, MC3400XA		50	150	—	50	150	—	
MC3500XB, MC3400XB		50	150	—	50	150	—	
MC3500X, MC3400X		25	100	—	25	100	—	
Output Voltage Swing	V_O				±12	±14	—	V
(R_L ≥ 10 k)		±12	±14	—	±10	±13	—	
(R_L ≥ 2.0 k)		±10	±13	—				
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR							dB
MC3500XA, MC3400XA		80	100	—	80	100	—	
MC3500XB, MC3400XB		80	100	—	80	100	—	
MC3500X, MC3400X		—	—	—	70	100	—	
Supply Voltage Rejection Ratio (R_S ≤ 10 k) (Note 3)	PSRR							dB
MC3500XA, MC3400XA		80	100	—	80	100	—	
MC3500XB, MC3400XB		80	100	—	80	100	—	
MC3500X, MC3400X		70	100	—	70	100	—	
Supply Current (Each Amplifier)	I_D							mA
MC3500XA, MC3400XA		—	1.4	2.5	—	1.4	2.5	
MC3500XB, MC3400XB		—	1.4	2.5	—	1.4	2.5	
MC3500X, MC3400X		—	1.4	2.7	—	1.4	2.7	
Slew Rate (A_V = 1)	SR	—	13	—	—	13	—	V/µs
Gain-Bandwidth Product	GBW	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	—	25	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 1]).

Characteristic	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}							mV
MC3500XA, MC3400XA		—	—	4.0	—	—	4.0	
MC3500XB, MC3400XB		—	—	7.0	—	—	7.0	
MC3500X, MC3400X		—	—	14	—	—	13	
Input Offset Current (V_{CM} = 0) (Note 2)	I_{IO}							nA
MC3500XA, MC3400XA		—	—	20	—	—	2.0	
MC3500XB, MC3400XB		—	—	40	—	—	4.0	
MC3500X, MC3400X		—	—	40	—	—	4.0	
Input Bias Current (V_{CM} = 0) (Note 2)	I_{IB}							nA
MC3500XA, MC3400XA		—	—	50	—	—	4.0	
MC3500XB, MC3400XB		—	—	50	—	—	8.0	
MC3500X, MC3400X		—	—	50	—	—	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
MC3500XA, MC3400XA		25	—	—	25	—	—	
MC3500XB, MC3400XB		25	—	—	25	—	—	
MC3500X, MC3400X		15	—	—	15	—	—	
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	—	—	±12	—	—	
($R_L \geq 2.0$ k)		±10	—	—	±10	—	—	
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR							dB
MC3500XA, MC3400XA		80	—	—	80	—	—	
MC3500XB, MC3400XB		80	—	—	80	—	—	
MC3500X, MC3400X		70	—	—	70	—	—	
Supply Voltage Rejection Ratio ($R_S \leq 10$ k) (Note 3)	PSRR							dB
MC3500XA, MC3400XA		80	—	—	80	—	—	
MC3500XB, MC3400XB		80	—	—	80	—	—	
MC3500X, MC3400X		70	—	—	70	—	—	
Supply Current (Each Amplifier)	I_D							mA
MC3500XA, MC3400XA		—	—	2.8	—	—	2.8	
MC3500XB, MC3400XB		—	—	2.8	—	—	2.8	
MC3500X, MC3400X		—	—	3.0	—	—	3.0	

NOTES: (1) T_{low} = −55°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= 0°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B
T_{high} = +125°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= +70°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B

(2) The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(4) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1 — INPUT BIAS CURRENT versus TEMPERATURE

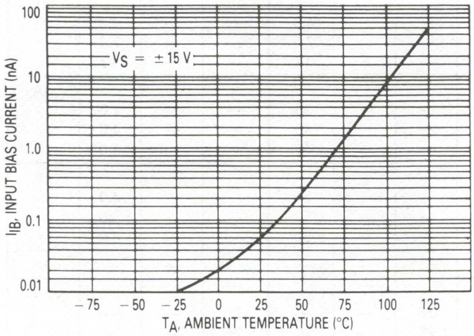


FIGURE 2 — OUTPUT VOLTAGE SWING versus FREQUENCY

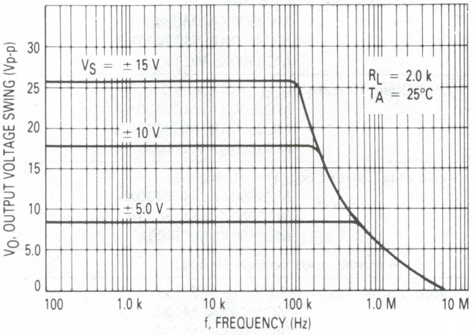


FIGURE 3 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

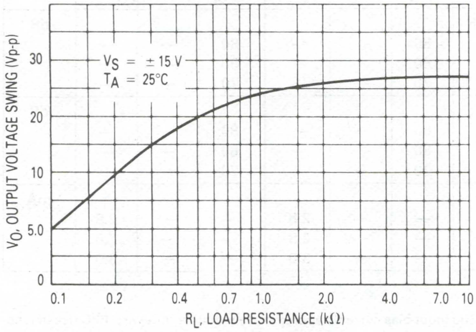


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

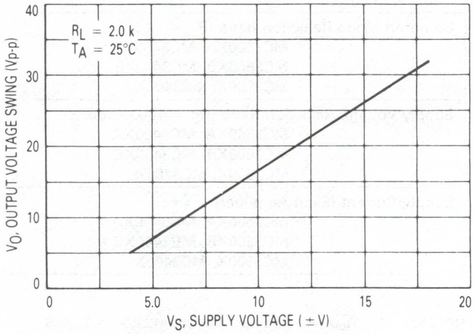


FIGURE 5 — OUTPUT VOLTAGE SWING versus TEMPERATURE

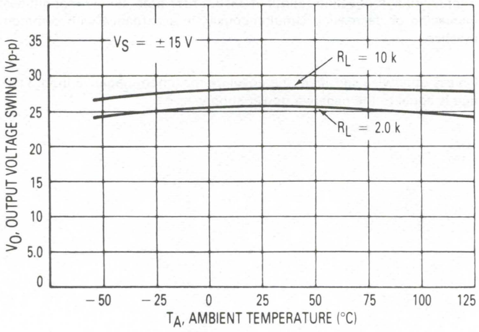


FIGURE 6 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

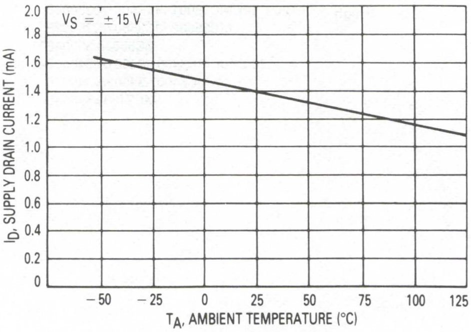


FIGURE 7 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

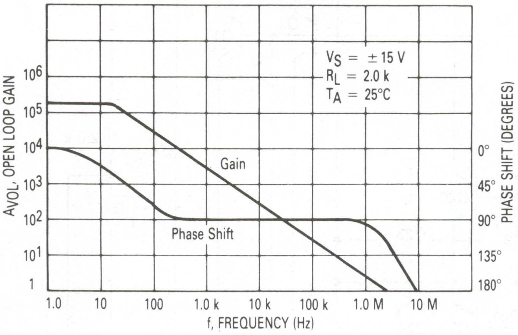


FIGURE 8 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

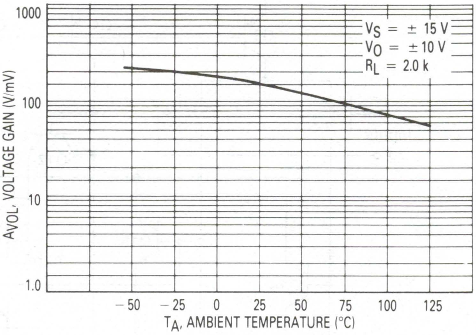


FIGURE 9 — NORMALIZED SLEW RATE versus TEMPERATURE

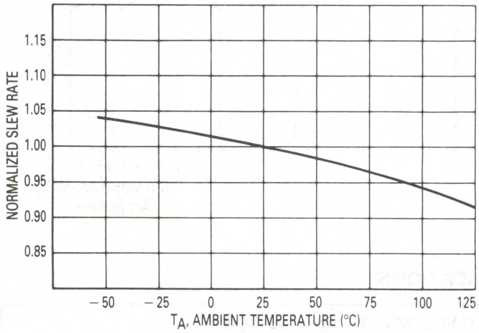


FIGURE 10 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

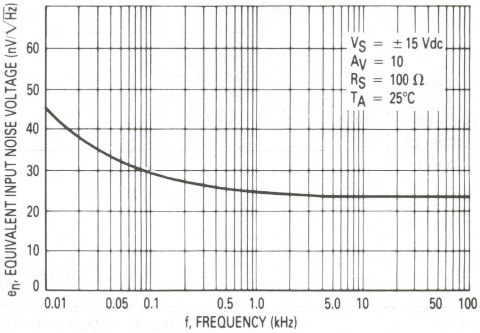
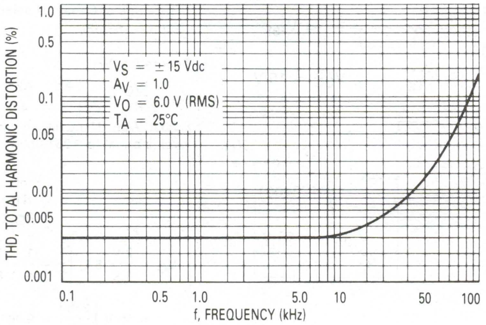
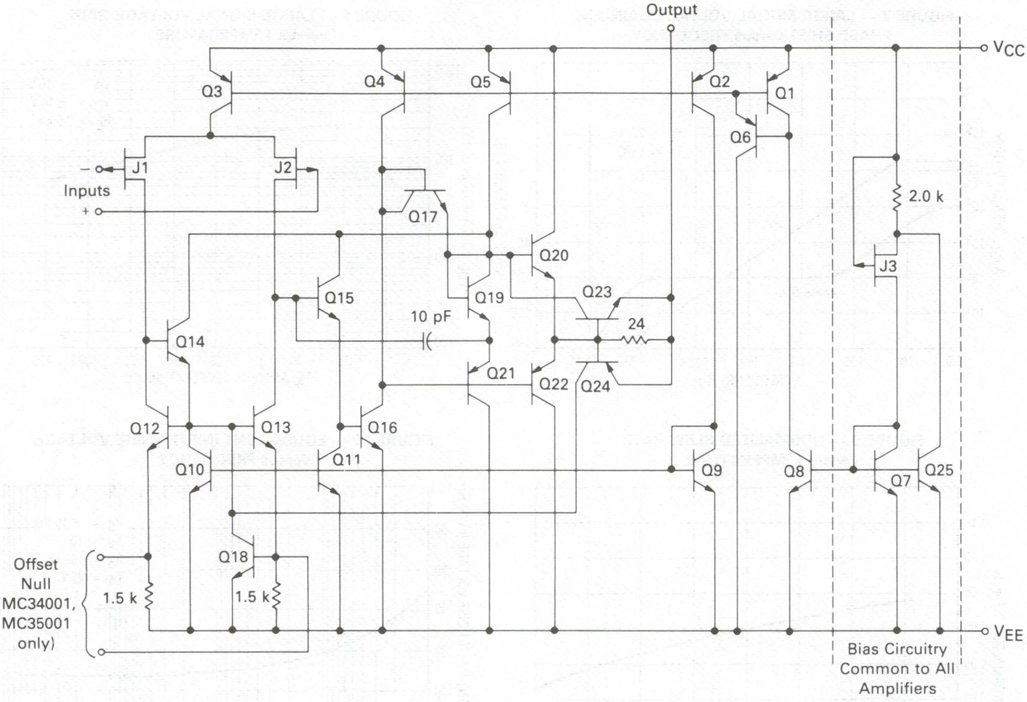


FIGURE 11 — TOTAL HARMONIC DISTORTION versus FREQUENCY

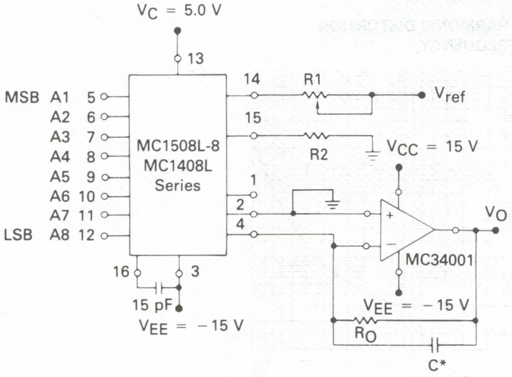


REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)


Output
VCC
Q3
Q4
Q5
Q2
Q1
Q6
J1
J2
Inputs
−
+
Q17
2.0 k
Q20
J3
Q15
Q19
Q23
10 pF
24
Q14
Q21
Q22
Q24
Q12
Q13
Q16
Q10
Q11
Q9
Q8
Q7
Q25
Offset Null (MC34001, MC35001 only)
1.5 k
Q18
1.5 k
VEE
Bias Circuitry Common to All Amplifiers

TYPICAL APPLICATIONS

FIGURE 12 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


VC = 5.0 V
13
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1508L-8
MC1408L
Series
14
R1
Vref
15
R2
VCC = 15 V
1
2
4
+
−
VO
MC34001
16
3
15 pF
VEE = −15 V
VEE = −15 V
RO
C*

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

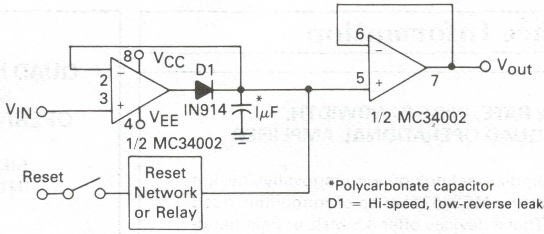
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0$ Vdc
$R1 = R2 \approx 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

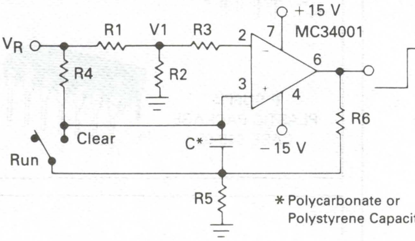
$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

FIGURE 13 — POSITIVE PEAK DETECTOR


8
VCC
D1
2
3
VIN
4
VEE
IN914
*
1μF
1/2 MC34002
6
5
7
Vout
1/2 MC34002
Reset
Reset
Network
or Relay

*Polycarbonate capacitor
D1 = Hi-speed, low-reverse leakage diode

FIGURE 14 — LONG INTERVAL RC TIMER


+15 V
VR
R1
V1
R3
2
7
MC34001
6
R4
R2
3
4
R6
Clear
C*
−15 V
Run
R5

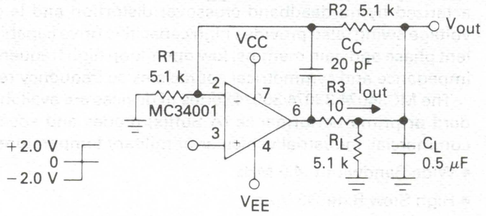
∗Polycarbonate or
Polystyrene Capacitor

Time (t) = R4 Cℓn (V_R/V_R-V_I), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 v	C = 1.0 μF	R3 = R4 = 144 M
R6 = 20 k	R5 = 2.0 k	R1 = R2 = 1.0 k

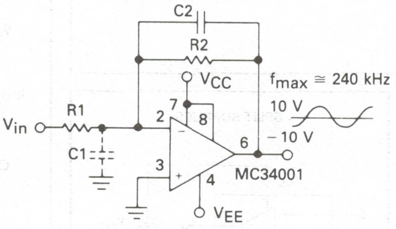
FIGURE 15 — ISOLATING LARGE CAPACITIVE LOADS


R2 5.1 k
Vout
VCC
CC
20 pF
R1
5.1 k
2
7
R3
Iout
MC34001
10
6
3
4
RL
5.1 k
CL
0.5 μF
+2.0 V
0
−2.0 V
VEE

- Overshoot <10%
- t_s = 10 μs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ \text{V}/\mu\text{s} = 0.04\ \text{V}/\mu\text{s (with } C_L \text{ shown)}$$

FIGURE 16 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER


C2
R2
VCC
fmax ≅ 240 kHz
10 V
−10 V
R1
Vin
7
2
8
6
C1
3
4
MC34001
VEE

- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance (C1 ≅ 3 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high-frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

MC34074,A
MC35074,A
MC33074,A

MOTOROLA

Advance Information

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY QUAD OPERATIONAL AMPLIFIER

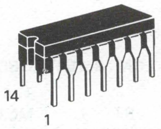
A standard low-cost Bipolar technology with innovative design concepts is employed for the MC34074 series of monolithic quad operational amplifiers. These devices offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage can economically be achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC34074/33074/35074 series of devices are available in standard or prime performance (A Suffix) grades and specified over commercial, industrial/vehicular or military temperature ranges.

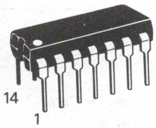
- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.10%
- Wide Single Supply Operating Range: 3.0 to 44 Volts
- Wide Input Common Mode Range Including Ground (V_{EE})
- Low Input Offset Voltage: 2.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14.0 V for $V_S = \pm 15$ V
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low T.H.D. Distortion: 0.02%
- Excellent Phase Margins: 60°
- Excellent Gain Margin: 12 dB

QUAD HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

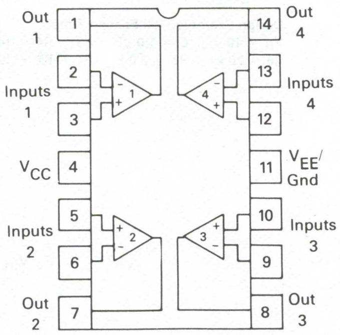


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS

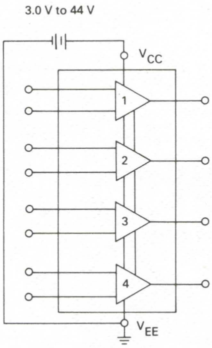


(Top View)

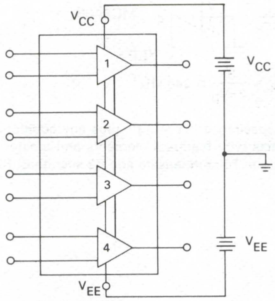
ORDERING INFORMATION

Device	Temperature Range	Package
MC35074L, AL	−55 to +125°C	Ceramic DIP
MC33074L, AL	−40 to +85°C	Ceramic DIP
MC33074P, AP	−40 to +85°C	Plastic DIP
MC34074L, AL	0 to +70°C	Ceramic DIP
MC34074P, AP	0 to +70°C	Plastic DIP

SINGLE SUPPLY



SPLIT SUPPLIES



$V_{CC} + |V_{EE}| \leq 44$ V

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Ambient Temperature Range MC35074,A MC33074,A MC34074,A	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

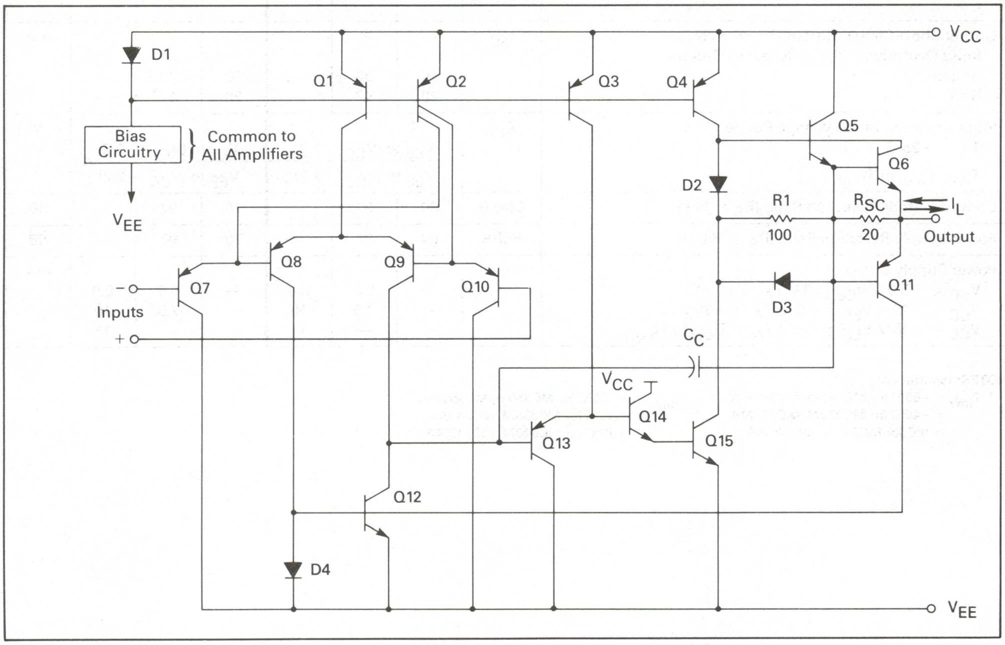
MAXIMUM DEVICE POWER DISSIPATION

Ambient Temperature	+25°C	+70°C	+85°C	+125°C	°C
Power Dissipation	1250	800	650	250	mW

NOTES:

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)


D1
Q1
Q2
Q3
Q4
Q5
Q6
V_{CC}
Bias Circuitry
Common to All Amplifiers
V_{EE}
D2
R1
100
R_{SC}
20
I_L
Output
Q7
Q8
Q9
Q10
Q11
D3
− Inputs +
C_C
V_{CC}
Q14
Q13
Q15
Q12
D4
V_{EE}

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	MC35074A/34074A/ 33074A			MC35074/34074/33074			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{CM} = 0)	V_{IO}							mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	0.5	2.0	—	2.0	4.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	0.5	2.5	—	2.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	4.0	—	—	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0)	I_{IB}							nA
T_A = +25°C		—	100	500	—	100	500	
T_A = T_{low} to T_{high}		—	—	700	—	—	700	
Input Offset Current (V_{CM} = 0)	I_{IO}							nA
T_A = +25°C		—	6.0	50	—	6.0	75	
T_A = T_{low} to T_{high}		—	—	300	—	—	300	
Large Signal Voltage Gain V_O = ±10 V, R_L = 2.0 k	A_{VOL}	50	100	—	25	100	—	V/mV
Output Voltage Swing	V_{OH}							V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 k, T_A = +25°C		3.7	4.0	—	3.7	4.0	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.7	14	—	13.7	14	—	
V_{CC} = +15 V, V_{EE} −15 V, R_L = 2.0 k, T_A = T_{low} to T_{high}		13.5	—	—	13.5	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 k, T_A = +25°C	V_{OL}	—	0.1	0.2	—	0.1	0.2	
V_{CC} = +15 V, V_{EE} + −15 V, R_L = 10 k, T_A = +25°C		—	−14.7	−14.4	—	−14.7	−14.4	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 k, T_A = T_{low} to T_{high}		—	—	−13.8	—	—	−13.8	
Output Short-Circuit Current (T_A = +25°C) Input Overdrive = 1.0 V, Output to Ground	I_{SC}							mA
Source		10	30	—	10	30	—	
Sink		20	47	—	20	47	—	
Input Common Mode Voltage Range	V_{ICR}							V
T_A = +25°C		V_{EE} to (V_{CC} − 1.8)			V_{EE} to (V_{CC} − 1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} − 2.2)			V_{EE} to (V_{CC} − 2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR	80	97	—	70	97	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	80	97	—	70	97	—	dB
Power Supply Current	I_D							mA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	6.5	8.0	—	6.5	8.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	7.5	10	—	7.5	10	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	11	—	—	11	

NOTES: (continued)

3. T_{low} = −55°C for MC35074, MC35074A　　T_{high} = +125°C for MC35074, MC35074A
= −40°C for MC33074, MC33074A　　= +85°C for MC33074, MC33074A
= 0°C for MC34074, MC34074A　　= +70°C for MC34074, MC34074A

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC35074A/34074A/33074A Min	MC35074A/34074A/33074A Typ	MC35074A/34074A/33074A Max	MC35074/34074/33074 Min	MC35074/34074/33074 Typ	MC35074/34074/33074 Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k, C_L = 500 pF)	SR							V/μs
A_V +1		8.0	10	—	—	10	—	
A_V −1		—	13	—	—	13	—	
Settling Time (10 V Step, A_V = −1.0)	t_s							μs
To 0.10% (±½ LSB of 9-Bits)		—	1.1	—	—	1.1	—	
To 0.01% (±½ LSB of 12-Bits)		—	2.2	—	—	2.2	—	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—	—	4.5	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 2.0 k, V_O = 20 V_{P-P}, THD = 5.0%)	BWp	—	200	—	—	200	—	kHz
Phase Margin	φm							Degrees
R_L = 2.0 k		—	60	—	—	60	—	
R_L = 2.0 k, C_L = 300 pF		—	40	—	—	40	—	
Gain Margin	A_m							dB
R_L = 2.0 k		—	12	—	—	12	—	
R_L = 2.0 k, C_L = 300 pF		—	4.0	—	—	4.0	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.22	—	—	0.22	—	pA/$\sqrt{Hz}$
Input Capacitance	C_i	—	0.8	—	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{P-P}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	z_o	—	30	—	—	30	—	Ω

TYPICAL PERFORMANCE CURVES

FIGURE 1—INPUT OFFSET VOLTAGE versus TEMPERATURE FOR REPRESENTATIVE UNITS

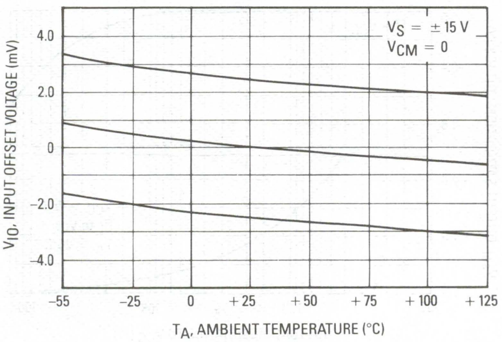


FIGURE 2—INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

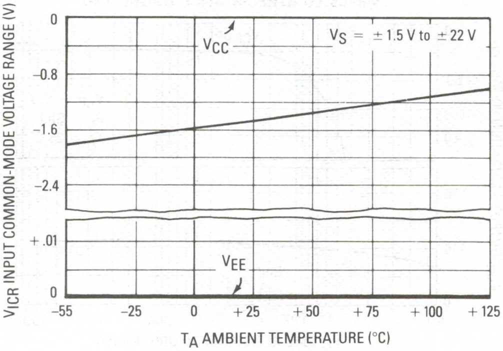


FIGURE 3—NORMALIZED INPUT BIAS CURRENT versus TEMPERATURE

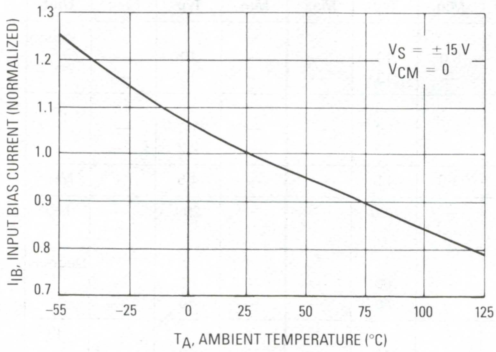


FIGURE 4—NORMALIZED INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

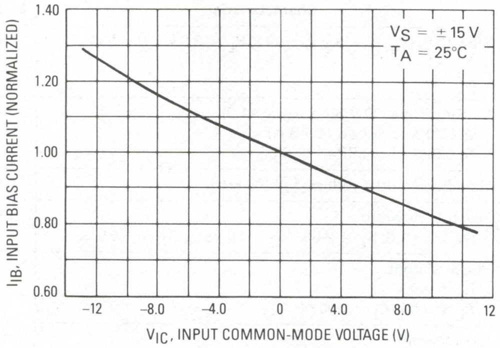


FIGURE 5—SPLIT SUPPLY OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

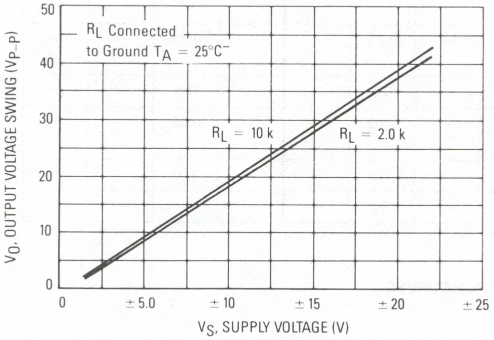


FIGURE 6—SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT

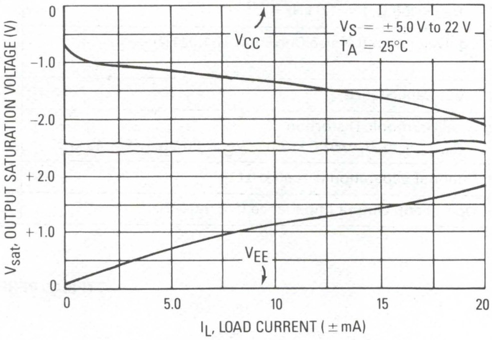


FIGURE 7—SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND

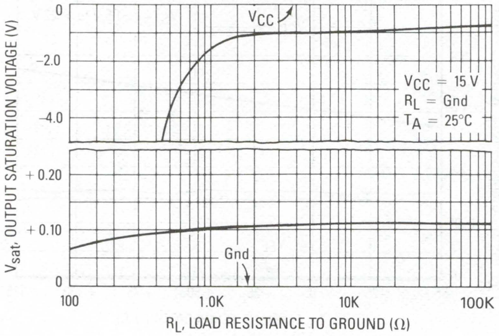


FIGURE 8—SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO V_{CC}

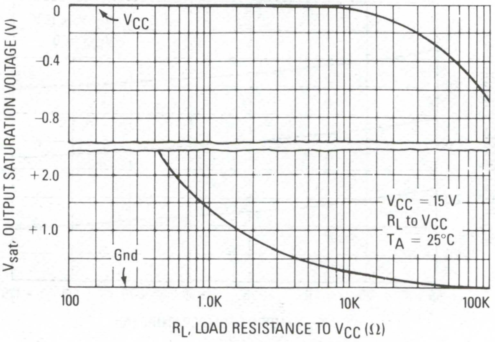


FIGURE 9—OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

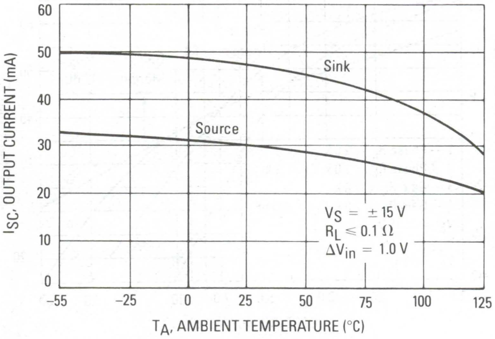


FIGURE 10—OUTPUT IMPEDANCE versus FREQUENCY

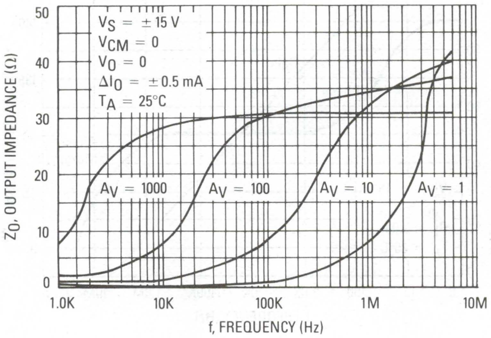


FIGURE 11—OUTPUT VOLTAGE SWING versus FREQUENCY

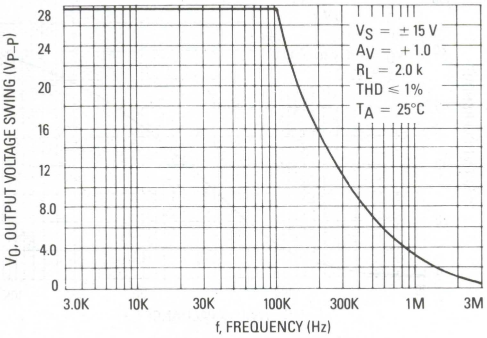


FIGURE 12—OUTPUT DISTORTION versus FREQUENCY

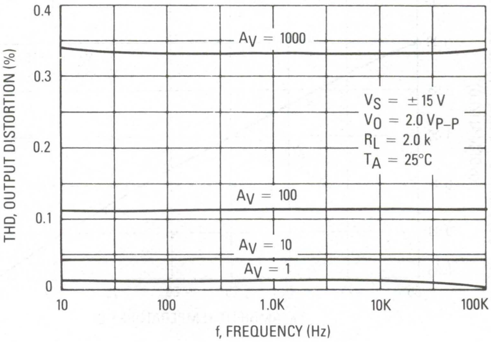


FIGURE 13—OUTPUT DISTORTION versus OUTPUT VOLTAGE SWING

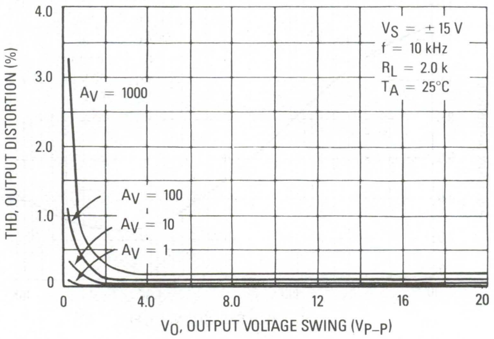


FIGURE 14—OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

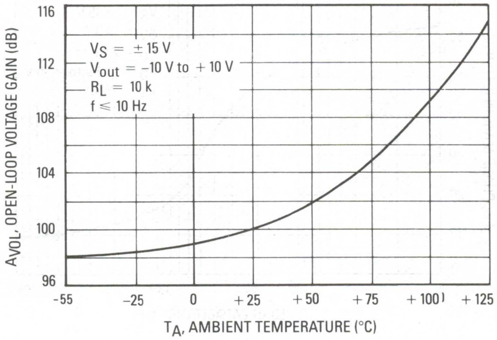


FIGURE 15—OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

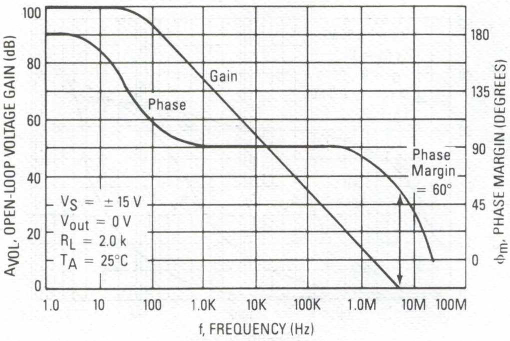


FIGURE 16—OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

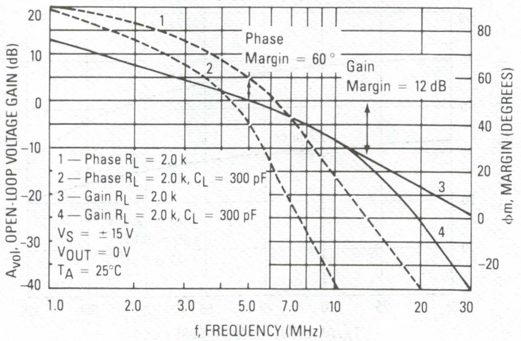


FIGURE 17—NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

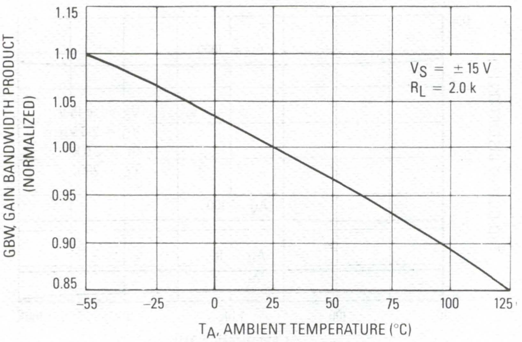


FIGURE 18—PERCENT OVERSHOOT versus LOAD CAPACITANCE

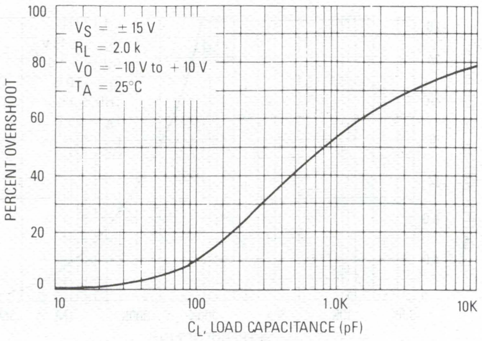


FIGURE 19—PHASE MARGIN versus LOAD CAPACITANCE

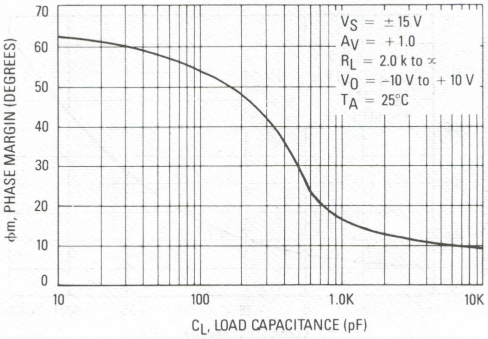


FIGURE 20—GAIN MARGIN versus LOAD CAPACITANCE

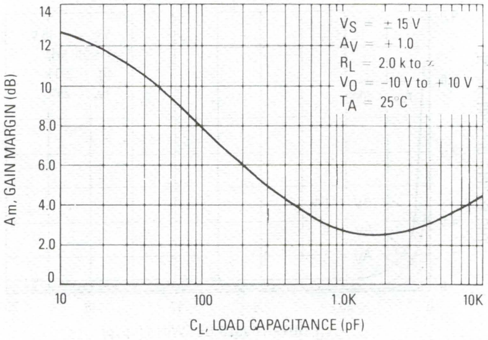


FIGURE 21—PHASE MARGIN versus TEMPERATURE

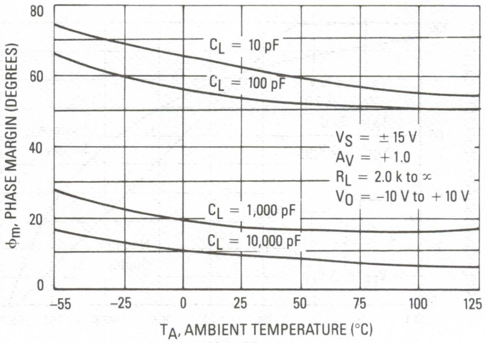


FIGURE 22—GAIN MARGIN versus TEMPERATURE

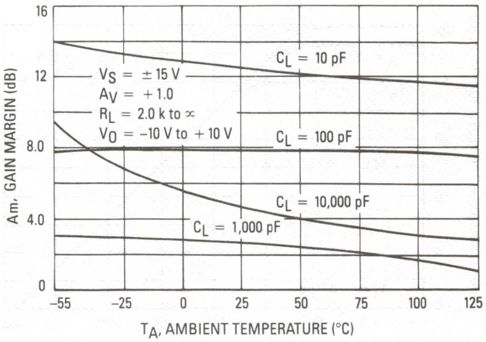


FIGURE 23—NORMALIZED SLEW RATE versus TEMPERATURE

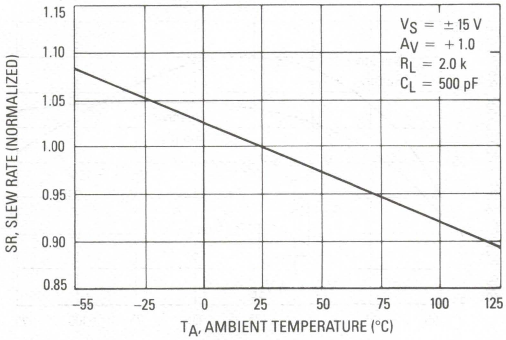


FIGURE 24—OUTPUT SETTLING TIME

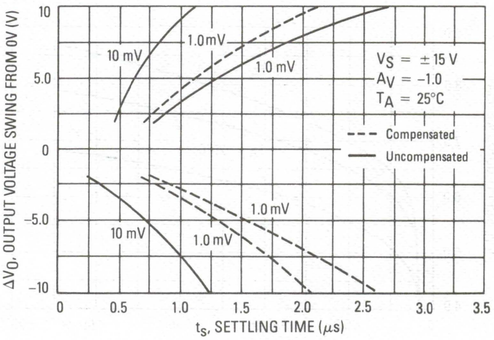


FIGURE 25—SMALL-SIGNAL TRANSIENT RESPONSE

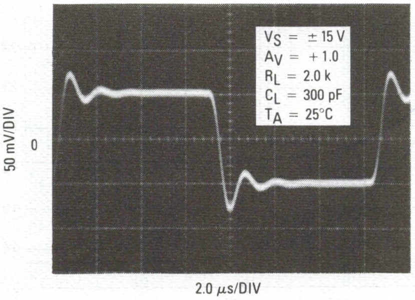


FIGURE 26—LARGE-SIGNAL TRANSIENT RESPONSE

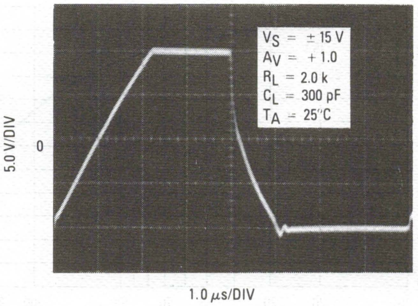


FIGURE 27—COMMON-MODE REJECTION RATIO versus FREQUENCY

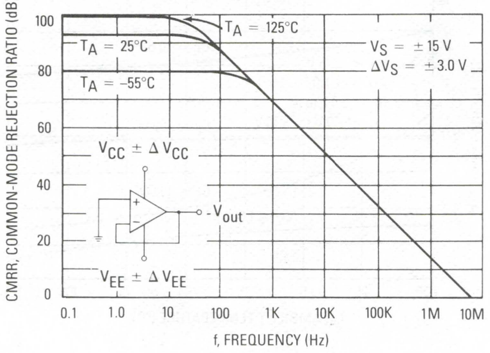


FIGURE 28—POWER SUPPLY REJECTION RATIO versus FREQUENCY

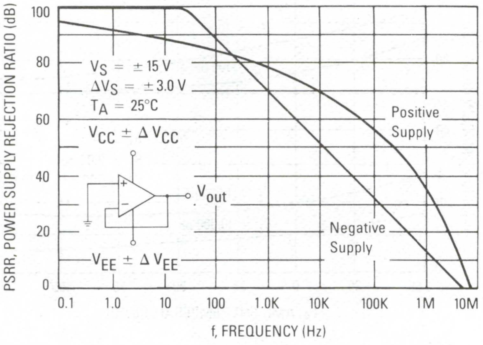


FIGURE 29—SUPPLY CURRENT versus SUPPLY VOLTAGE

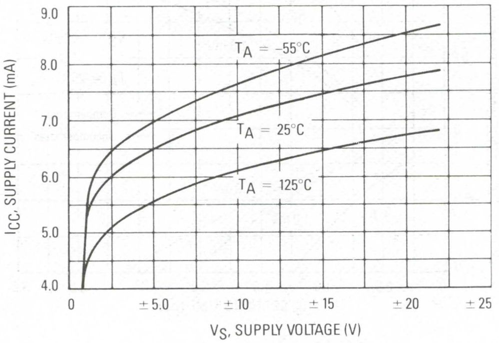


FIGURE 30—POWER SUPPLY REJECTION RATIO versus TEMPERATURE

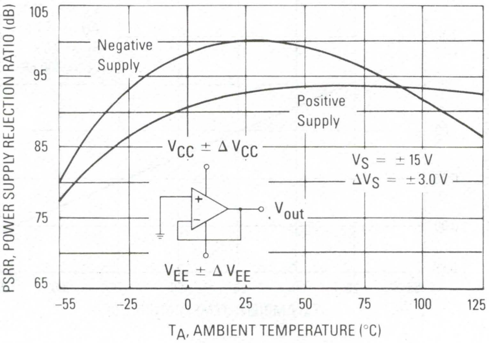


FIGURE 31—CHANNEL SEPARATION versus FREQUENCY

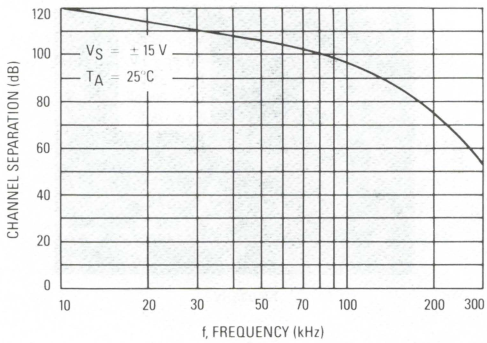
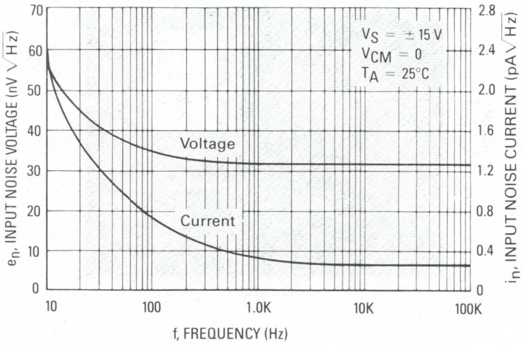


FIGURE 32—SPECTRAL NOISE DENSITY



APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION/PERFORMANCE FEATURES OF THE MC34074 FAMILY

Although the bandwidth, slew rate, and settling time of the MC34074 amplifier family is similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 volts and decrease below the V_{EE} voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either input's clamping diode without damage or latching, although phase reversal may again occur.

If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than the typical JFET input gate capacitance (3.0 pF), better frequency response for a given input source resistance can be achieved using the MC34074 amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34074 family can typically settle to within 1/2 LSB of 8 bits in 1.0 μs, and within 1/2 LSB of 12 bits in 2.2 μs for a 10 volt step. In a typical inverting unity gain fast settling configuration, the typical symmetrical slew rate is ±13 volts/μs. In the classic non-inverting unity gain configuration the typical output positive slew rate is +10 volts/μs, and the corresponding negative slew rate will typically exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are typically superior to that of JFETs, a low untrimmed maximum offset voltage of 2.0 mV prime and 4.5 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low-cost precision, high-speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 1.0 volt of the positive rail (V_{CC}), and within 0.3 volts of the negative rail (V_{EE}), providing a 28.7 Vp-p swing from ±15 volt supplies. This large output swing becomes most noticable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q4, and V_{BE} of the NPN pull up transistor Q5, and the voltage drop associated with the short circuit resistance, R_{SC}. The negative swing is limited by the saturation voltage of the pull-down transistor Q15, the voltage drop $I_L R_1$, and the voltage drop associated with resistance R_{SC}, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_1, thus limiting the negative swing to the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE}$ + 1.0 V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34074 family offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} + 1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain-bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34074 family also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to at least 3.0 volts @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ± 15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

TYPICAL SINGLE SUPPLY APPLICATIONS V_{CC} = 5.0 VOLTS

FIGURE 33 — AC COUPLED NONINVERTING AMPLIFIER

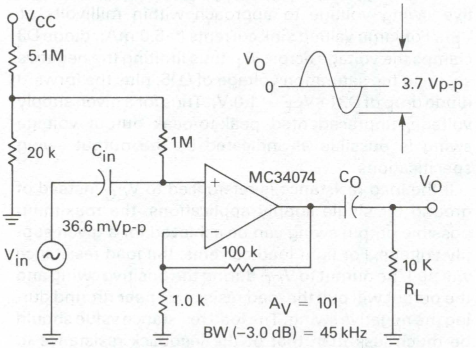

VCC
5.1M
VO
0
3.7 Vp-p
1M
20 k
Cin
MC34074
CO
VO
36.6 mVp-p
Vin
100 k
10 K
RL
1.0 k
AV = 101
BW (−3.0 dB) = 45 kHz

FIGURE 34 — AC COUPLED INVERTING AMPLIFIER

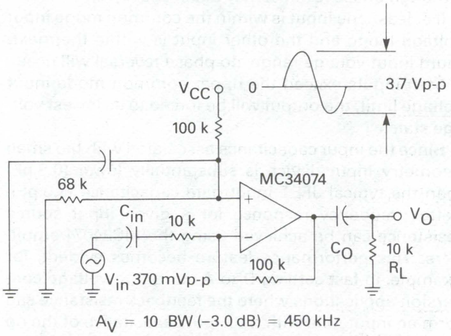

VCC
0
3.7 Vp-p
100 k
68 k
MC34074
Cin
10 k
VO
CO
10 k
RL
100 k
Vin 370 mVp-p
AV = 10 BW (−3.0 dB) = 450 kHz

FIGURE 35 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING

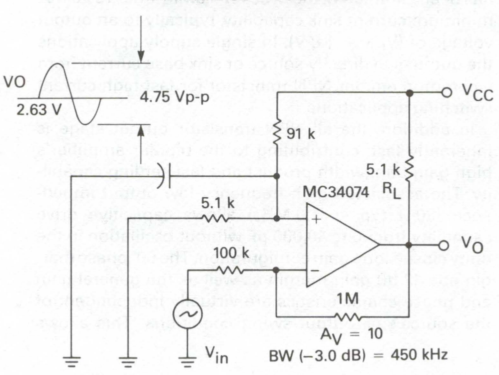

VO
2.63 V
4.75 Vp-p
VCC
91 k
5.1 k
RL
MC34074
5.1 k
100 k
VO
1M
Vin
AV = 10
BW (−3.0 dB) = 450 kHz

FIGURE 36 — UNITY GAIN BUFFER TTL DRIVER

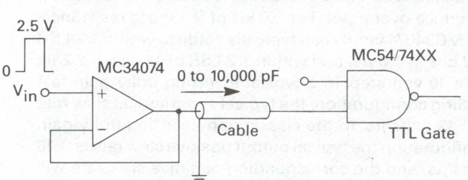
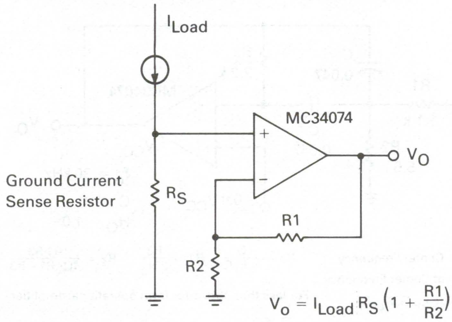

2.5 V
0
Vin
MC34074
0 to 10,000 pF
MC54/74XX
Cable
TTL Gate

FIGURE 43 — AC/DC GROUND CURRENT MONITOR



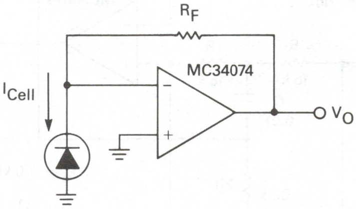
I_{Load}
MC34074
+
−
V_O
Ground Current
Sense Resistor
R_S
R1
R2

$V_o = I_{Load} R_S \left(1 + \frac{R1}{R2}\right)$

For $V_O > 0.1$ V

$BW\ (-3.0\ dB) = GBW\left(\frac{R2}{R1 + R2}\right)$

FIGURE 44 — PHOTOVOLTAIC CELL AMPLIFIER



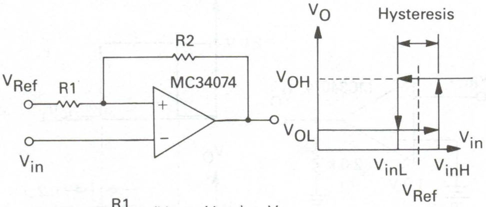
R_F
MC34074
−
+
I_{Cell}
V_O

$V_{Cell} = 0\,V$

$V_O = I_{Cell} R_F$

$V_O > 0.1\,V$

FIGURE 45 — LOW INPUT VOLTAGE COMPARATOR WITH HYSTERESIS



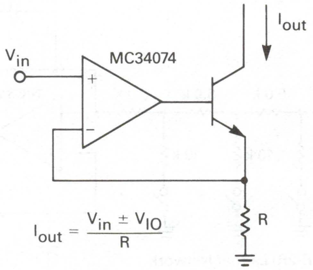
R2
V_{Ref}
R1
MC34074
+
−
V_{in}
V_O
Hysteresis
V_{OH}
V_{OL}
V_{in}
V_{inL}
V_{inH}
V_{Ref}

$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{Ref}) + V_{Ref}$

$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{Ref}) + V_{Ref}$

$V_H = \frac{R1}{R1 + R}(V_{OH} - V_{OL})$

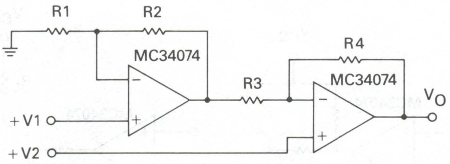
FIGURE 46 — HIGH COMPLIANCE VOLTAGE TO SINK CURRENT CONVERTER



I_{out}
V_{in}
MC34074
+
−
R

$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$

FIGURE 47 — HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER



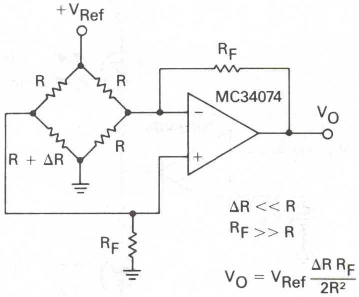
R1
R2
MC34074
−
+
+V1
+V2
R3
R4
MC34074
−
+
V_O

$\frac{R2}{R1} = \frac{R4}{R3}$ (Critical to CMRR)

$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2 - V1\middle|\frac{R4}{R3}\right)$

For $(V2 \geq V1)$, $V| > 0$

FIGURE 48 — BRIDGE CURRENT AMPLIFIER



$+V_{Ref}$
R
R
R + ΔR
R
R_F
MC34074
−
+
V_O
R_F

$\Delta R << R$

$R_F >> R$

$V_O = V_{Ref}\frac{\Delta R\, R_F}{2R^2}$

$(V_O \geq 0.1\,V)$

FIGURE 37 — ACTIVE HIGH-Q NOTCH FILTER

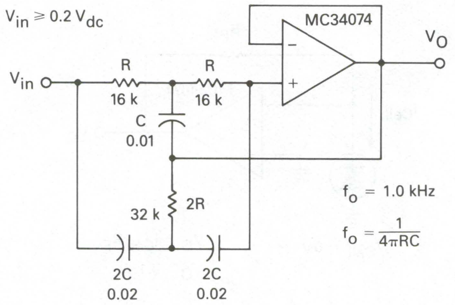
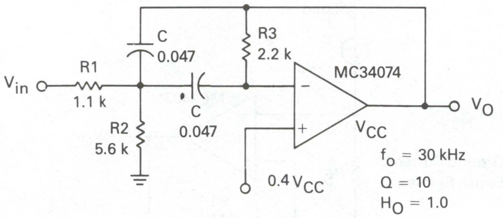

$V_{in} \geq 0.2\ V_{dc}$
MC34074
V_O
V_{in}
R
16 k
R
16 k
C
0.01
32 k
2R
2C
0.02
2C
0.02
$f_o = 1.0$ kHz
$f_o = \frac{1}{4\pi RC}$

FIGURE 38 — ACTIVE BANDPASS FILTER


C
0.047
R3
2.2 k
R1
1.1 k
V_{in}
C
0.047
MC34074
V_O
V_{CC}
R2
5.6 k
$0.4\ V_{CC}$
$f_o = 30$ kHz
Q = 10
$H_O = 1.0$

Given f_O = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_o, Q, A_o, C
Then

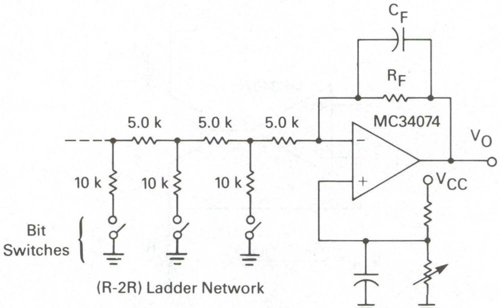
$R3 = \frac{Q}{\pi f_o C}$ $R1 = \frac{R3}{2 H_o}$ $R2 = \frac{R1\,R3}{4Q^2 R1 - R3}$

For less than 10% error from operational amplifier

$\frac{Q_o f_0}{GBW} < 0.1$

Where f_o and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

FIGURE 39 — LOW VOLTAGE FAST D/A CONVERTER


C_F
R_F
5.0 k
5.0 k
5.0 k
MC34074
V_O
10 k
10 k
10 k
V_{CC}
Bit Switches

(R-2R) Ladder Network

Settling Time
1.0 µs (8 Bits, ½ LSB)

FIGURE 40 — HIGH SPEED LOW VOLTAGE COMPARATOR

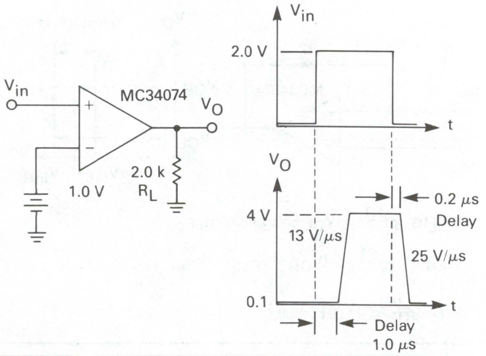

V_{in}
MC34074
V_O
2.0 k
R_L
1.0 V
V_{in}
2.0 V
t
V_O
0.2 µs
Delay
4 V
13 V/µs
25 V/µs
0.1
t
Delay
1.0 µs

FIGURE 41 — LED DRIVER

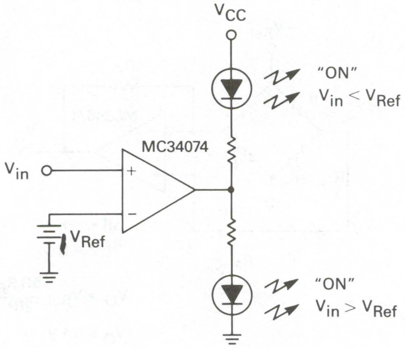
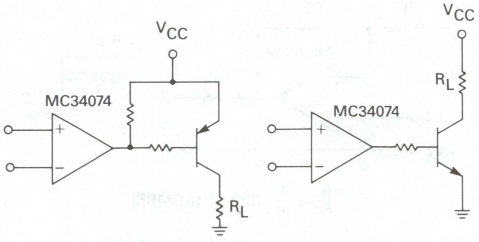

V_{CC}
"ON"
$V_{in} < V_{Ref}$
MC34074
V_{in}
V_{Ref}
"ON"
$V_{in} > V_{Ref}$

FIGURE 42 — TRANSISTOR DRIVER


V_{CC}
MC34074
R_L
V_{CC}
R_L
MC34074

(A) PNP (B) NPN

FIGURE 49 — LOW VOLTAGE PEAK DETECTOR

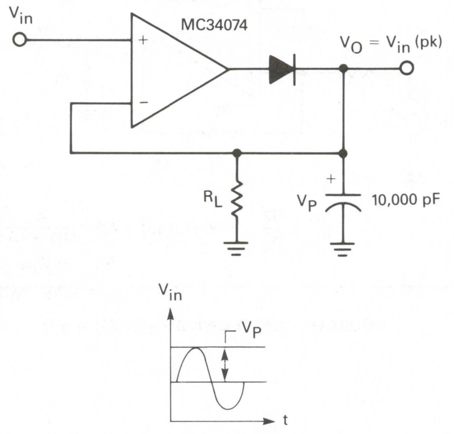
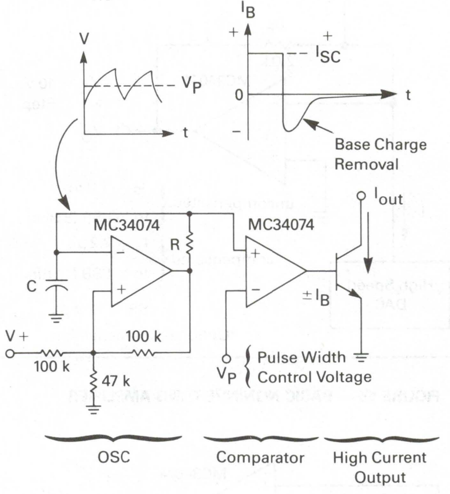

V_{in}
MC34074
+
−
$V_O = V_{in}$ (pk)
R_L
+
V_P
10,000 pF
V_{in}
V_P
t

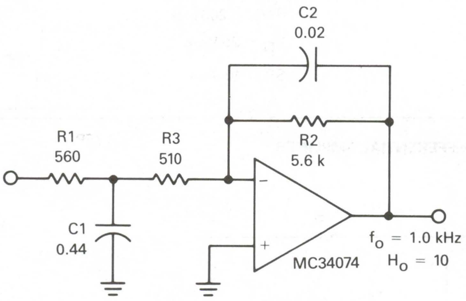
FIGURE 50 — HIGH FREQUENCY PULSE WIDTH MODULATION

$f_{OSC} \cong \frac{0.85}{RC}$


V
V_P
t
I_B
+
0
−
+
I_{SC}
t
Base Charge Removal
I_{out}
MC34074
R
C
−
+
MC34074
+
−
$\pm I_B$
V+
100 k
100 k
47 k
V_P
Pulse Width Control Voltage
OSC
Comparator
High Current Output

GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15$ VOLTS

FIGURE 51 — SECOND ORDER LOW-PASS ACTIVE FILTER


C2
0.02
R1
560
R3
510
R2
5.6 k
C1
0.44
−
+
MC34074
$f_o = 1.0$ kHz
$H_o = 10$

Choose: f_o, H_o, C2

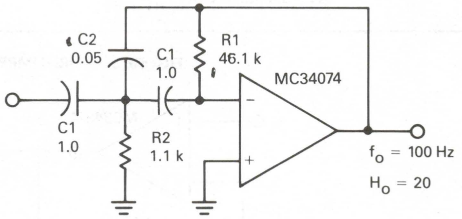
Then: $C1 = 2C2 (H_o + 1)$

$R2 = \frac{\sqrt{2}}{4\pi f_o C2}$

$R3 = \frac{R2}{H_o + 1}$

$R1 = \frac{R2}{H_o}$

FIGURE 52 — SECOND ORDER HIGH-PASS ACTIVE FILTER


C2
0.05
C1
1.0
R1
46.1 k
MC34074
C1
1.0
R2
1.1 k
−
+
$f_o = 100$ Hz
$H_o = 20$

Choose: f_o, H_o, C1

Then: $R1 = \frac{H_o + 0.5}{\pi f_o C1 \sqrt{2}}$

$R2 = \frac{\sqrt{2}}{2\pi f_o C1 (1/H_o + 2)}$

$C2 = \frac{C1}{H_o}$

FIGURE 53 — FAST SETTLING INVERTER

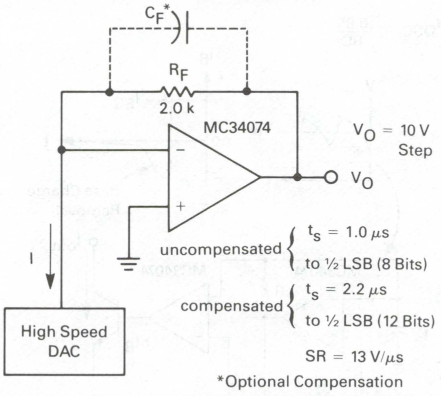

C_F*
R_F
2.0 k
MC34074
V_O = 10 V Step
V_O
I
High Speed DAC
uncompensated { t_s = 1.0 μs to ½ LSB (8 Bits)
compensated { t_s = 2.2 μs to ½ LSB (12 Bits)
SR = 13 V/μs
*Optional Compensation

FIGURE 54 — BASIC INVERTING AMPLIFIER

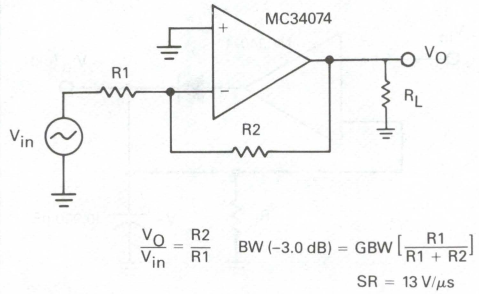

MC34074
V_O
R1
R_L
R2
V_{in}
$\frac{V_O}{V_{in}} = \frac{R2}{R1}$
BW (−3.0 dB) = GBW $\left[\frac{R1}{R1 + R2}\right]$
SR = 13 V/μs

FIGURE 55 — BASIC NONINVERTING AMPLIFIER

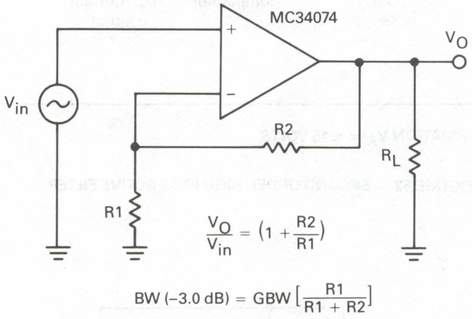

MC34074
V_O
V_{in}
R2
R_L
R1
$\frac{V_O}{V_{in}} = \left(1 + \frac{R2}{R1}\right)$
BW (−3.0 dB) = GBW $\left[\frac{R1}{R1 + R2}\right]$

FIGURE 56 — UNITY GAIN BUFFER (A_V = +1)

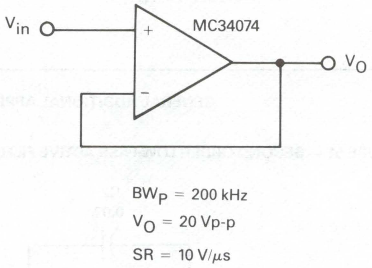

V_{in}
MC34074
V_O
BW_P = 200 kHz
V_O = 20 Vp-p
SR = 10 V/μs

FIGURE 57 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

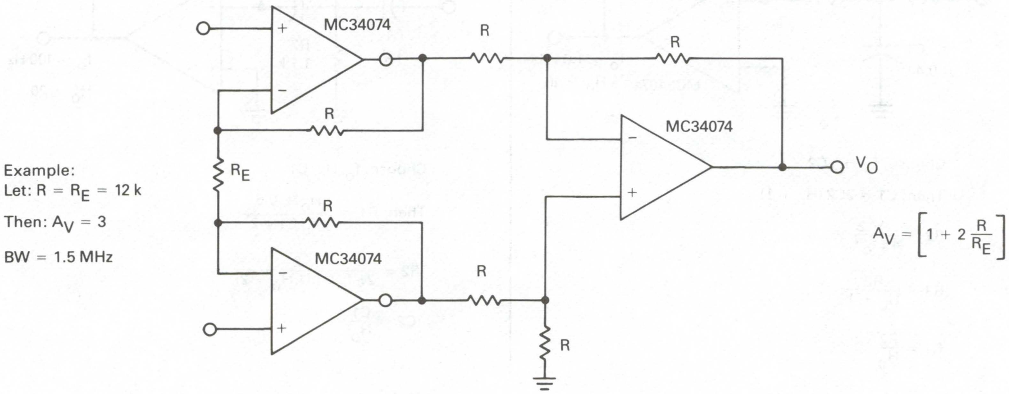
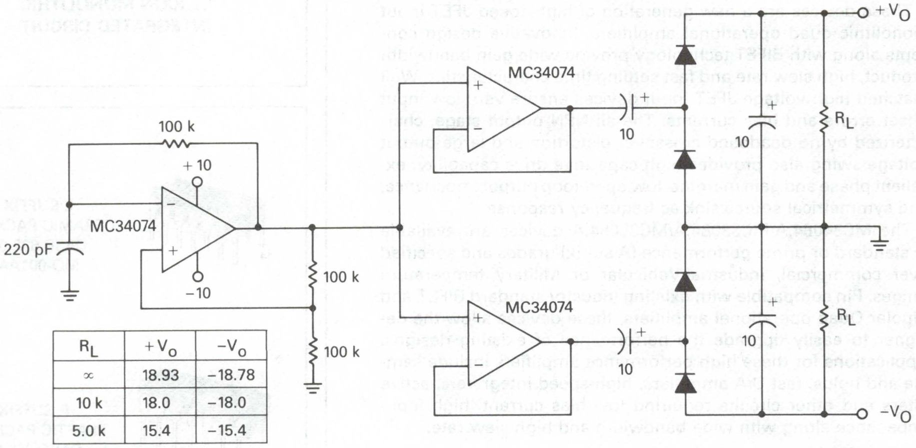

MC34074
R
R
MC34074
R
R_E
R
MC34074
R
R
V_O
Example:
Let: R = R_E = 12 k
Then: A_V = 3
BW = 1.5 MHz
$A_V = \left[1 + 2\frac{R}{R_E}\right]$

FIGURE 58 — DUAL VOLTAGE DOUBLER


100 k
+10
MC34074
220 pF
−10
100 k
100 k
MC34074
MC34074
10
10
10
10
R_L
R_L
$+V_O$
$-V_O$

R_L	$+V_O$	$-V_O$
∞	18.93	−18.78
10 k	18.0	−18.0
5.0 k	15.4	−15.4

MC34084,A
MC35084,A
MC33084,A

MOTOROLA

Product Preview

QUAD HIGH SPEED JFET INPUT OPERATIONAL AMPLIFIERS

These devices are a new generation of high-speed JFET input monolithic quad operational amplifiers. Innovative design concepts along with BIFET technology provide wide gain bandwidth product, high slew rate and fast settling time characteristics. Well matched high voltage JFET input devices ensure very low input offset errors and bias currents. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing also provides high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink ac frequency response.

The MC34084,A/MC33084,A/MC35084,A devices are available in standard or prime performance (A suffix) grades and specified over commercial, Industrial/Vehicular or Military temperature ranges. Pin compatible with existing Industry standard BIFET and Bipolar Quad operational amplifiers, these devices allow the designer to easily upgrade the performance of existing designs. Applications for these high performance amplifiers include sample and holds, fast D/A amplifiers, high-speed integraters, active filters and other circuits requiring low bias current, high input impedance along with wide bandwidth and high slew rate.

- Wide Gain Bandwidth: 10 MHz
- High Slew Rate: 40 V/μs
- Fast Settling Time: 700 ns to ±0.1% (10 V Step)
- Low Input Bias Current: 200 pA Maximum
- High Input Impedance: 10^{12} Ω
- Input Offset Voltage: MC34084A — 5.0 mV Maximum
  MC34084 — 10 mV Maximum
- Large Output Voltage Swing: −14.7 V to +14 V for V_S = ±15 V, R_L = 10 k
- Low Open Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low Equivalent Noise: Voltage — 16 nV/$\sqrt{\text{Hz}}$
  Current — 0.01 pA/$\sqrt{\text{Hz}}$
- Low THD Distortion: 0.01% (A_V = 10, f = 20 kHz, R_L = 10 k)
- Excellent Phase/Gain Margins: 55°/10 dB

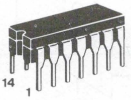
ORDERING INFORMATION

Device	Temperature Range	Package
MC35084L, AL	−55 to +125°C	Ceramic DIP
MC33084L, AL	−40 to +85°C	Ceramic DIP
MC33084P, AP	−40 to +85°C	Plastic DIP
MC34084L, AL	0 to +70°C	Ceramic DIP
MC34084P, AP	0 to +70°C	Plastic DIP

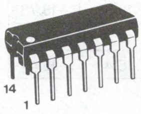
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

QUAD HIGH SPEED JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

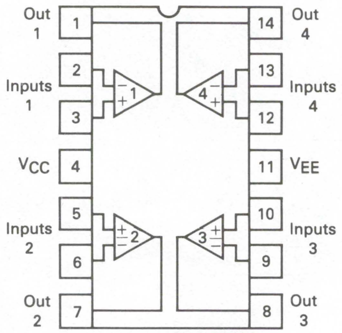


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS



(Top View)

MOTOROLA

MC34085,A
MC35085,A
MC33085,A

Product Preview

QUAD HIGH SPEED DECOMPENSATED ($A_{VCL} \geqslant 2$) JFET INPUT OPERATIONAL AMPLIFIERS

These devices are a new generation of high-speed JFET input monolithic quad operational amplifiers. Innovative design concepts along with BIFET technology provide wide gain bandwidth product and high slew rate. Well matched high voltage JFET input devices ensure very low input offset errors and bias currents. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing also provides high capacitive drive capability, low open-loop output impedance, and symmetrical source/sink ac frequency response.

The MC34085,A/MC33085,A/MC35085,A devices are available in standard or prime performance (A suffix) grades and specified over commercial, Industrial/Vehicular or Military temperature ranges. Pin compatible with existing Industry standard BIFET and Bipolar Quad operational amplifiers, these high-speed devices allow the designer to easily upgrade the performance of existing designs where closed Loop Gain is ⩾2. Applications for these high performance amplifiers include sample and holds, active filters, high-speed inverting amplifiers, and other circuits requiring low bias current, high input impedance along with wide bandwidth and high slew rate.

- Wide Gain Bandwidth: 20 MHz
- High Slew Rate: 80 V/μs
- Low Input Bias Current: 200 pA Maximum
- High Input Impedance: 10^{12} Ω
- Input Offset Voltage: MC34085A — 5.0 mV Maximum
  MC34085 — 10 mV Maximum
- Large Output Voltage Swing: −14.7 V to +14 V for $V_S = \pm 15$ V, $R_L = 10$ k
- Low Open-Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low Equivalent Noise: Voltage — 16 nV/$\sqrt{\text{Hz}}$
  Current — 0.01 pA/$\sqrt{\text{Hz}}$
- Low THD Distortion: 0.01% ($A_V = 10$, f = 20 kHz, $R_L = 10$ k)
- Decompensated Version of the MC34084 Series

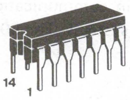
ORDERING INFORMATION

Device	Temperature Range	Package
MC35085L, AL	−55 to +125°C	Ceramic DIP
MC33085L, AL	−40 to +85°C	Ceramic DIP
MC33085P, AP	−40 to +85°C	Plastic DIP
MC34085L, AL	0 to +70°C	Ceramic DIP
MC34085P, AP	0 to +70°C	Plastic DIP

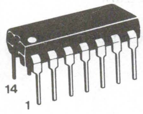
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

QUAD HIGH SPEED DECOMPENSATED ($A_{VCL} \geqslant 2$) JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

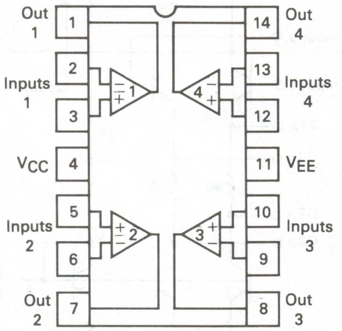


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS



(Top View)

NE592
SE592

MOTOROLA

VIDEO AMPLIFIER

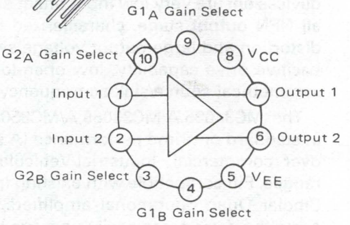
SILICON MONOLITHIC
INTEGRATED CIRCUIT

DIFFERENTIAL TWO-STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

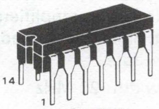
- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

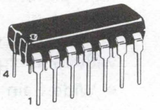
H SUFFIX
METAL PACKAGE
CASE 603-04
TO-100


G1A Gain Select
G2A Gain Select
10
9
8
VCC
Input 1
1
7
Output 1
Input 2
2
6
Output 2
G2B Gain Select
3
4
5
VEE
G1B Gain Select

(Top View)

Pin 5 connected to case

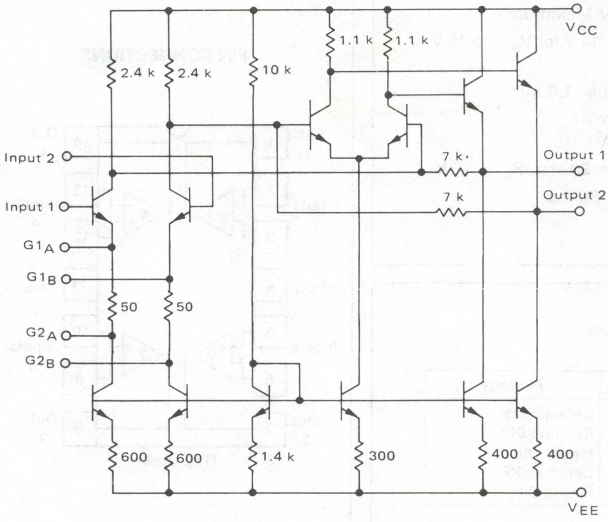


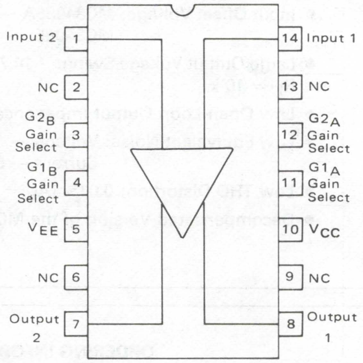


F SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

N SUFFIX
PLASTIC PACKAGE
CASE 646-05

CIRCUIT SCHEMATIC


VCC
1.1 k
1.1 k
2.4 k
2.4 k
10 k
Input 2
Input 1
7 k
7 k
Output 1
Output 2
G1A
G1B
50
50
G2A
G2B
600
600
1.4 k
300
400
400
VEE


Input 2
1
14
Input 1
NC
2
13
NC
G2B Gain Select
3
12
G2A Gain Select
G1B Gain Select
4
11
G1A Gain Select
VEE
5
10
VCC
NC
6
9
NC
Output 2
7
8
Output 1

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
NE592N	0 to 70°C	Plastic DIP
NE592H	0 to 70°C	Metal Can
NE592F	0 to 70°C	Ceramic DIP
SE592H	-55 to +125°C	Metal Can
SE592F	-55 to +125°C	Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 −8.0	Volts
Differential Input Voltages	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±6.0	Volts
Output Current	I_o	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	 −55 to +125 0 to +70	°C
Operating Junction Temperature Range Metal and Ceramic Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Metal and Ceramic Packagee Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (V_{CC} = +6.0 V, V_{EE} = −6.0 V, V_{CM} = 0)

Characteristic	Symbol	SE592			NE592			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain — Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p)	A_{vd}							V/V
(Gain 1, Note 1)		300	400	500	250	400	600	
(Gain 2, Note 2)		90	100	110	80	100	120	
Bandwidth — Figure 3	BW							MHz
(Gain 1, Note 1)		—	40	—	—	40	—	
(Gain 1, Note 2)		—	90	—	—	90	—	
Rise Time — Figure 3								ns
(Gain 1, e_{out} = 1 Vp-p, Note 1)	t_{TLH}	—	10.5	—	—	10.5	—	
(Gain 2, e_{out} = 1 Vp-p, Note 2)	t_{THL}	—	4.5	10	—	4.5	12	
Propagation Delay — Figure 3								ns
(Gain 1, e_{out} = 1 Vp-p, Note 1)	t_{PLH}	—	7.5	—	—	7.5	—	
(Gain 2, e_{out} = 1 Vp-p, Note 2)	t_{PHL}	—	6.0	10	—	6.0	10	
Input Resistance	R_{in}							kΩ
(Gain 1, Note 1)		—	4.0	—	—	4.0	—	
(Gain 2, Note 2)		20	30	—	10	30	—	
Input Capacitance (Gain 2, Note 2)	C_{in}	—	2.0	—	—	2.0	—	pF
Input Offset Current (Gain 3, Note 3) — Fig. 2	I_{IO}	—	0.4	3.0	—	0.4	5.0	µA
Input Bias Current (Gain 3, Note 3) — Fig. 2	I_{IB}	—	9.0	20	—	9.0	30	µA
Input Noise Voltage (Gain 1 and Gain 2) (BW = 1 kHz to 10 MHz) — Figure 1	V_n	—	12	—	—	12	—	µV (rms)
Input Voltage Range (Gain 2, Note 2) — Fig. 3	V_{in}	±1.0	—	—	±1.0	—	—	V
Common-Mode Rejection Ratio — Figure 3	CMRR							dB
(Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz)		60	86	—	60	86	—	
(Gain 2, V_{CM} = ±1 V, f = 5 MHz)		—	60	—	—	60	—	
Supply Voltage Rejection Ratio — Figure 2 (Gain 2, ΔV_s = ±0.5 V)	PSRR	50	70	—	50	70	—	dB
Output Offset Voltage — Figure 2 (Gain 3, $R_L = \infty$, Note 3)	V_{OO}	—	0.35	0.75	—	0.35	0.75	V
Output Common-Mode Voltage — Figure 2 ($R_L = \infty$, Gain 3, Note 3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing — Figure 3 (R_L = 2k, Gain 2, Note 2)	V_O	3.0	4.0	—	3.0	4.0	—	Vp-p
Output Resistance	r_o	—	20	—	—	20	—	Ω
Power Supply Current — Figure 2 ($R_L = \infty$, Gain 2, Note 2)	I_D	—	18	24	—	18	24	mA

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

ELECTRICAL CHARACTERISTICS $T_A = T_{high}$ to T_{low} unless otherwise noted.* (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, V_{CM} = 0)

Characteristic	Symbol	SE592 Min	SE592 Typ	SE592 Max	NE592 Min	NE592 Typ	NE592 Max	Units
Differential Voltage Gain – Figure 3 (R_L = 2 kΩ, e_{out} = 3 Vp-p)	A_{vd}							V/V
(Gain 1, Note 1)		200	–	600	250	–	600	
(Gain 2, Note 2)		80	–	120	80	–	120	
Input Resistance (Gain 2)	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3) – Figure 2	$\lvert I_{IO}\rvert$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3) – Figure 2	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2) – Figure 3	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio – Figure 3 (Gain 2, V_{CM} = ±1 V, f ⩽ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio – Figure 2 (Gain 2, Δ V_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage (Gain 3) – Figure 2	V_{OO}	–	–	1.2	–	–	1.5	V
Output Voltage Swing (Gain 2) – Figure 3	V_O	2.5	–	–	2.5	–	–	Vp-p
Power Supply Current (Gain 2) – Figure 2	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for NE592, −55°C for SE592
T_{high} = +70°C for NE592, +125°C for SE592

GENERAL TEST CIRCUITS

FIGURE 1

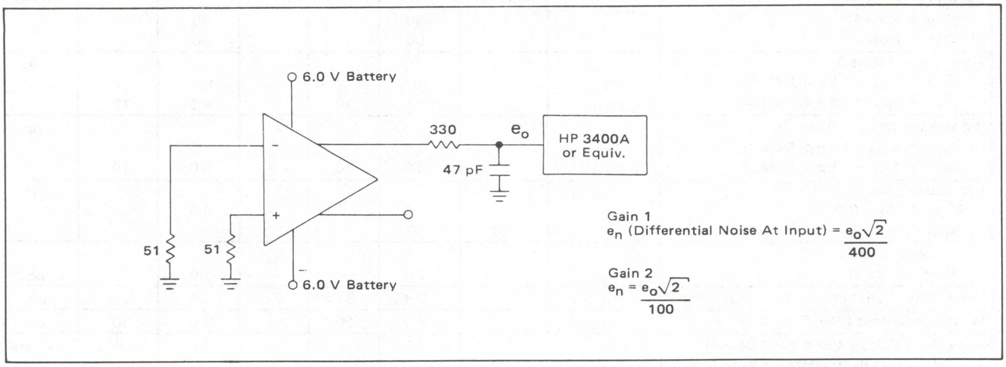

6.0 V Battery
330
e_o
47 pF
HP 3400A or Equiv.
−
+
51
51
6.0 V Battery
Gain 1
e_n (Differential Noise At Input) = $\frac{e_o\sqrt{2}}{400}$
Gain 2
$e_n = \frac{e_o\sqrt{2}}{100}$

FIGURE 2

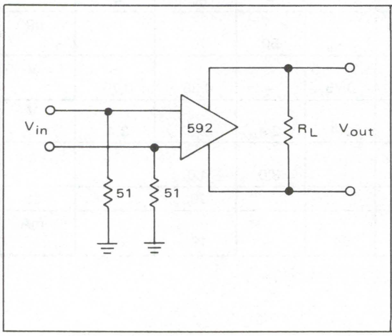

V_{in}
592
R_L
V_{out}
51
51

FIGURE 3

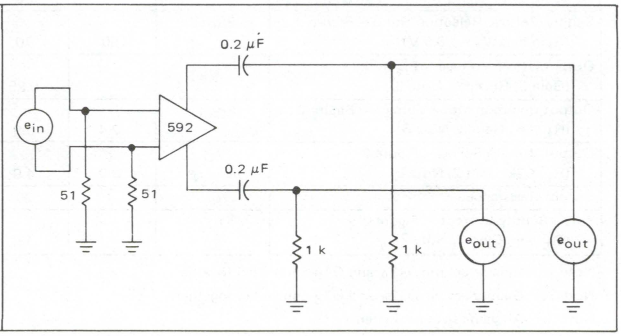

0.2 μF
e_{in}
592
0.2 μF
51
51
1 k
1 k
e_{out}
e_{out}

FIGURE 4 – GAIN 1 versus FREQUENCY

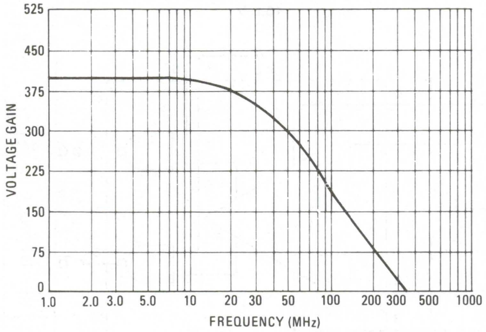


FIGURE 5 – GAIN 2 versus FREQUENCY

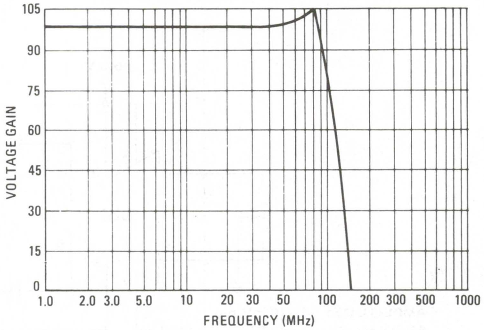


FIGURE 6 – OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

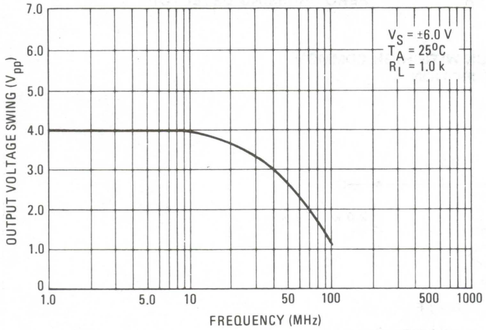


FIGURE 7 – OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

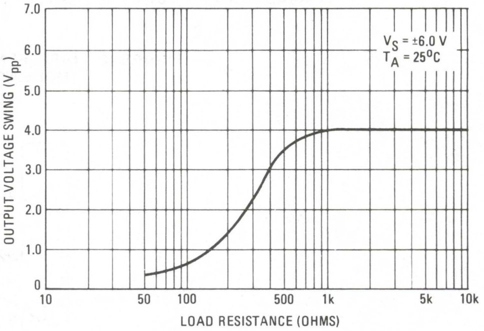


FIGURE 8 – VOLTAGE GAIN AS A FUNCTION OF R_{adj} RESISTANCE

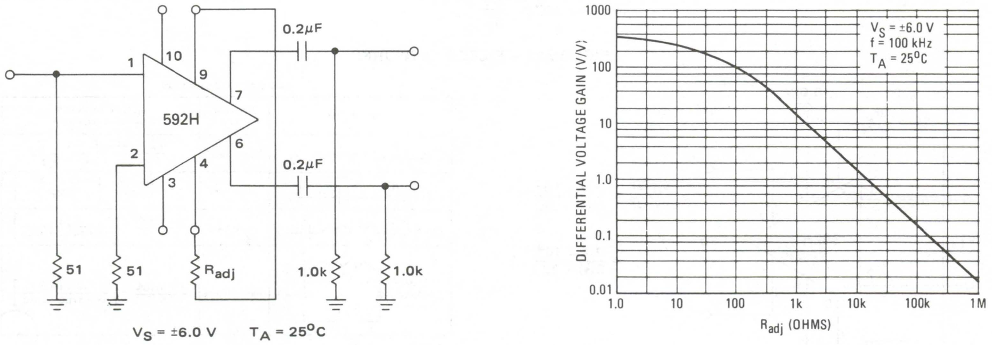


FIGURE 9 – DISK/TAPE PHASE MODULATED READBACK SYSTEMS

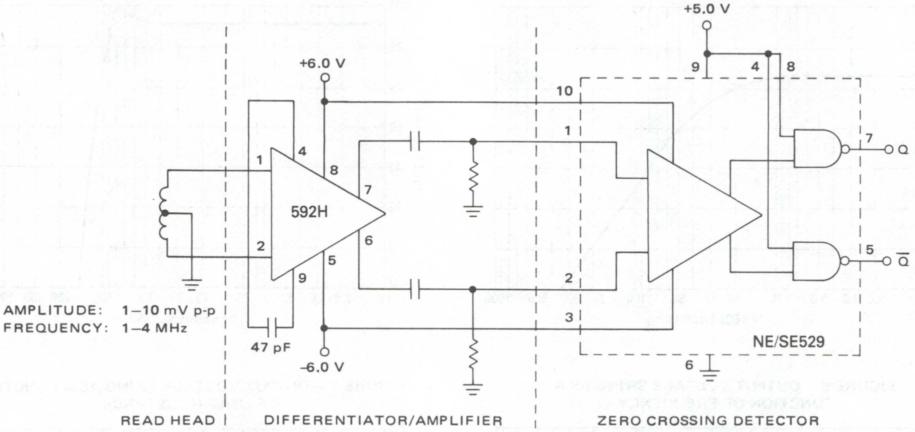
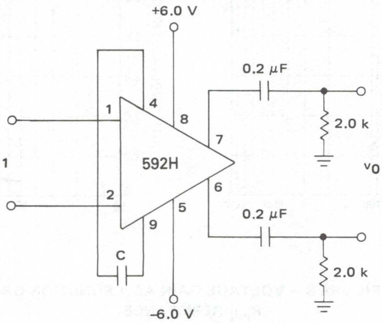

+5.0 V
9
4
8
+6.0 V
10
1
4
8
7
592H
6
5
9
1
2
2
3
7
Q
5
Q̄
NE/SE529
6
47 pF
-6.0 V
AMPLITUDE: 1–10 mV p-p
FREQUENCY: 1–4 MHz
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR

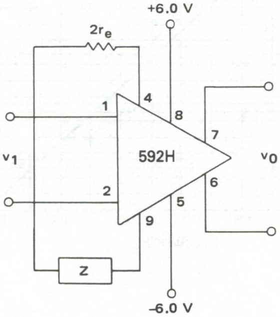
FIGURE 10 – DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION


+6.0 V
0.2 μF
2.0 k
1
4
8
7
v1
592H
vO
2
6
5
9
C
0.2 μF
2.0 k
-6.0 V

FOR FREQUENCY $f_1 << 1/2\,\pi\,(32)\cdot C$

$$v_O \cong 1.4 \times 10^4 C \frac{dv_1}{dt}$$

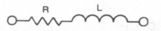
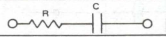
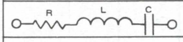
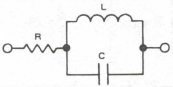
FIGURE 11 – FILTER NETWORKS


+6.0 V
2re
1
4
8
7
v1
592H
vO
2
6
5
9
Z
-6.0 V

$$\frac{v_O(s)}{v_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{v_O(s)}{v_1(s)}$ TRANSFER FUNCTION
	Low Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	High Pass	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	Band Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	Band Reject	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE:
In the networks above, the R value used is assumed to include $2\,r_e$, or approximately 30 Ohms.

MOTOROLA

OP-27
OP-37

ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIERS

The OP-27 and OP-37 are a series of monolithic operational amplifiers which combine low-noise, precision dc performance and wide bandwidth all in one device. Advanced Bipolar processing and innovative design techniques have produced the lowest noise precision operational amplifier in the industry. These devices are trimmed for extremely low initial input offset voltage by utilizing a highly stable and reliable zener zap technique during factory testing which yields guaranteed V_{IO} limits as tight as 25 µV. A unique input bias current cancellation scheme maintains low I_{IB} and I_{IO} to typically ±20 nA and 15 nA respectively over the full military temperature range. Other sources of input errors are reduced in excess of −120 dB due to extremely high common-mode and power supply rejection ratios.

Also impressive, are the slew rate and bandwidth of these devices. The OP-27 has a gain bandwidth product of 8.0 MHz and slew rate of 2.8 V/µs. While the OP-37 provides a 63 MHz gain bandwidth product and 17 V/µs slew rate for applications with closed loop gains ≥5.

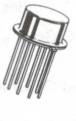
The precision, low noise and high speed characteristics of these devices make them ideal for amplifying transducer signals, RIAA phono, NAB tape head and microphone preamplifiers, wide band instrumentation amplifiers and high speed signal conditioning for data acquisition systems.

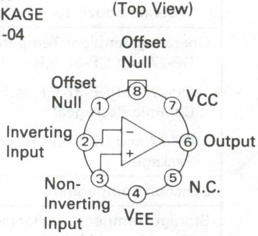
- Extremely Low-Noise — 3.0 nV/$\sqrt{\text{Hz}}$ at 1.0 kHz
  80 nVp-p, 0.1 Hz to 10 Hz
- Low Initial Input Offset Voltage — 10 µV
- Ultra Stable Input Offset Voltage — 0.2 µV/mo.
- Wide Gain Bandwidth Product and High Slew Rate:
  OP-27 — 8.0 MHz, 2.8 V/µs
  OP-37 — 63 MHz, 17 V/µs
- High Open-Loop Gain — 1.8 Million
- High Common-Mode Rejection — 126 dB
- Replaces OP-05, OP-06, OP-07, AD510, AD517, µA725 and NE5534

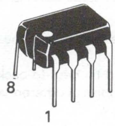
ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

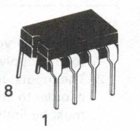
J SUFFIX
METAL PACKAGE
CASE 601-04



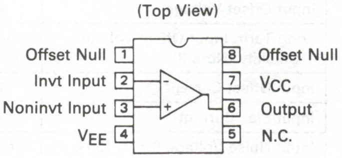




P SUFFIX
PLASTIC PACKAGE
CASE 626-04



Z SUFFIX
CERAMIC PACKAGE
CASE 693-02



ORDERING INFORMATION

Slew Rate	Device $V_{IO} \leq 25\ \mu V$	Device $V_{IO} \leq 60\ \mu V$	Device $V_{IO} \leq 100\ \mu V$	Temperature Range	Package
≥ 1.7 V/µs	OP-27AJ	OP-27BJ	OP-27CJ	−55 to +125°C	Metal Can
	OP-27AZ	OP-27BZ	OP-27CZ		Ceramic DIP
	OP-27EJ	OP-27FJ	OP-27GJ	−25 to +85°C	Metal Can
	OP-27EZ	OP-27FZ	OP-27GZ		Ceramic DIP
	OP-27EP	OP-27FP	OP-27GP	0 to +70°C	Plastic Dip
≥11 V/µs	OP-37AJ	OP-37BJ	OP-37CJ	−55 to +125°C	Metal Can
	OP-37AZ	OP-37BZ	OP-37CZ		Ceramic DIP
	OP-37EJ	OP-37FJ	OP-37GJ	−25 to +85°C	Metal Can
	OP-37EZ	OP-37FZ	OP-37GZ		Ceramic DIP
	OP-37EP	OP-37FP	OP-37GP	0 to +70°C	Plastic Dip

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	V
Input Voltage Range (Note 1)	V_{IDR}	±22	V
Differential Input Voltage (Note 2)	V_{ID}	±0.7	V
Differential Input Current (Note 2)	I_{ID}	±25	mA
Output Short-Circuit Duration	t_s	Indefinite	
Power Dissipation and Thermal Characteristics			
Plastic Package (P Suffix) $T_A = +36°C$	P_D	500	mW
Derate above $T_A = +36°C$	$1/R_{\theta JA}$	5.6	mW/°C
Metal Package (J Suffix) $T_A = +80°C$	P_D	500	mW
Derate above $T_A = +80°C$	$1/R_{\theta JA}$	7.1	mW/°C
Ceramic Package (Z Suffix) $T_A = +75°C$	P_D	500	mW
Derate above $T_A = +75°C$	$1/R_{\theta JA}$	6.7	mW/°C
Operating Ambient Temperature	T_A		°C
OP-27 and OP-37 A,B and C Grades		−55 to +125	
OP-27 and OP-37 E,F and G Grades (Metal and Ceramic Packages)		−25 to +85	
OP-27 and OP-37EP, FP and GP Grades (Plastic Package)		0 to +70	
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}		°C
Ceramic and Metal Packages		−65 to +150	
Plastic Package		−65 to +125	

NOTES:

1. For supply voltages less than ±22 V, the absolute maximum input voltage range is equal to the supply voltage.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current must be limited to 25 mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

		OP-27A/E/EP OP-37A/E/EP			OP-27B/F/FP OP-37B/F/FP			OP-27C/G/GP OP-37C/G/GP			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	—	10	25	—	20	60	—	30	100	μV
Long Term Input Offset Voltage Stability (Note 3)	V_{IO}/t	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/mo
Input Offset Current	I_{IO}	—	7.0	35	—	9.0	50	—	12	75	nA
Input Bias Current	I_{IB}	—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage 0.1 to 10 Hz (Note 4)	e_{np-p}	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μV_{p-p}
Input Noise Voltage Density	e_n										$nV/\sqrt{Hz}$
f_o = 10 Hz		—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	
f_o = 30 Hz		—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
f_o = 1000 Hz		—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
(Note 4)											
Input Noise Current Density	i_n										$pA/\sqrt{Hz}$
f_o = 10 Hz		—	1.7	4.0	—	1.7	4.0	—	1.7	—	
f_o = 30 Hz		—	1.0	2.3	—	1.0	2.3	—	1.0	—	
f_o = 1000 Hz		—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
(Note 4)											
Input Resistance — Differential Mode	r_i	1.5	6.0	—	1.2	5.0	—	0.8	4.0	—	MΩ
Input Resistance — Common Mode	R_{incm}	—	3.0	—	—	2.5	—	—	2.0	—	GΩ
Input Voltage Range	V_{IR}	±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	OP-27A/E/EP OP-37A/E/EP Min	Typ	Max	OP-27B/F/FP OP-37B/F/FP Min	Typ	Max	OP-27C/G/GP OP-37C/G/GP Min	Typ	Max	Unit
Common Mode Rejection Ratio V_{CM} = ±11 V	CMRR	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio V_S = ±4.0 V to ±18 V	PSRR	100	120	—	100	120	—	94	114	—	dB
Large-Signal Voltage Gain	A_{VOL}										V/mV
$R_L \geq 2$ kΩ, V_O = ±10 V		1000	1800	—	1000	1800	—	700	1500	—	
$R_L \geq 1$ kΩ, V_O = ±10 V		800	1500	—	800	1500	—	—	1500	—	
R_L = 600 Ω, V_O = ±1.0 V, V_S = ±4.0 V		—	700	—	—	700	—	—	500	—	
Output Voltage Swing	V_O										V
$R_L \geq 2$ kΩ		±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	
$R_L \geq 600$ Ω		±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate, $R_L \geq 2$ kΩ	SR										V/µs
OP-27		1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	
OP-37		11	17	—	11	17	—	11	17	—	
Gain Bandwidth Product	GBW										MHz
OP-27		5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	
OP-37 Av ≥ 5.0											
f_o = 10 kHz		45	63	—	45	63	—	45	63	—	
f_o = 1 MHz		—	40	—	—	40	—	—	40	—	
Open Loop Output Resistance V_O = 0, I_O = 0	r_o	—	70	—	—	70	—	—	70	—	Ω
Power Dissipation V_O = 0, No Load	P_D	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range R_P = 10 kΩ		—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES (continued)

3. Long term input offset voltage stability for the OP-27 and OP-37 series, refers to the average trend line of V_{IO} versus time over extended periods after the first 30 days of operation. Excluding the first hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 µV.
4. Sample tested.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 5])

Characteristic	Symbol	OP-27A OP-37A Min	Typ	Max	OP-27B OP-37B Min	Typ	Max	OP-27C OP-37C Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	—	30	60	—	50	200	—	70	300	µV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	µV/°C
Input Offset Current	I_{IO}	—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_{IB}	—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	V_{IR}	±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common Mode Rejection Ratio V_{CM} = ±10 V	CMRR	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio V_S = ±4.5 V to ±18 V	PSRR	96	114	—	94	114	—	86	108	—	dB
Large-Signal Voltage Gain $R_L \geq 2.0$ kΩ, V_O = ±10 V	A_{VOL}	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing $R_L \geq 2.0$ kΩ	V_O	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 5])

Characteristic	Symbol	OP-27E/EP OP-37E/EP			OP-27F/FP OP-37F/FP			OP-27G/GP OP-37G/GP			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	20	50	—	40	140	—	55	220	µV
Average Input Offset Drift (Note 6)	TCV_{IO}	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	µV/°C
Input Offset Current	I_{IO}	—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_{IB}	—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	V_{IR}	±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common Mode Rejection Ratio V_{CM} = ±10 V	CMRR	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio V_S = ±4.5 V to ±18 V	PSRR	97	114	—	96	114	—	90	114	—	dB
Large-Signal Voltage Gain $R_L \geq 2.0\ k\Omega$, V_O = ±10 V	A_{VOL}	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing $R_L \geq 2.0\ k\Omega$	V_O	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

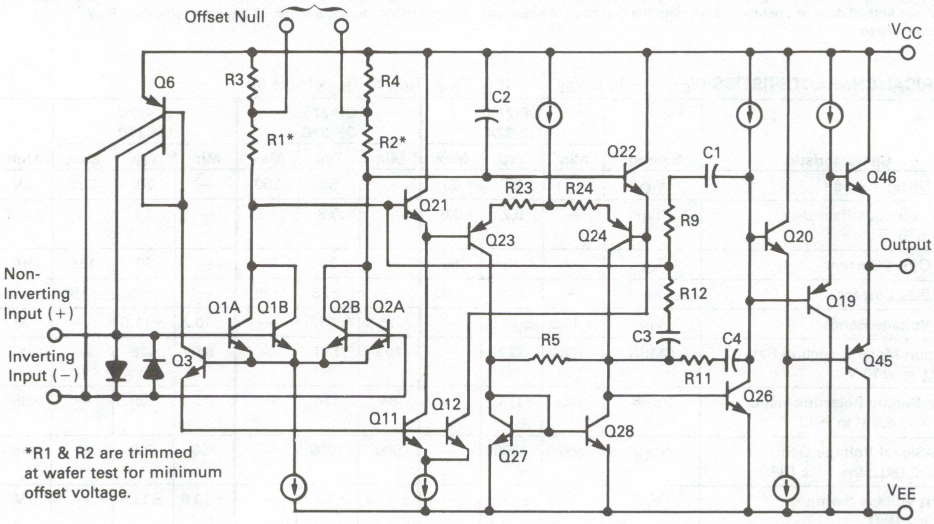
NOTES (continued)

5. T_{low} = −55°C for OP-27A/OP-37A, OP-27B/OP-37B, OP-27C/OP-37C
 = −25°C for OP-27E/OP-37E, OP-27F/OP-37F, OP-27G/OP-37G
 = 0°C for OP-27EP/OP-37EP, OP-27FP/OP-37FP, OP-27GP/OP-37GP

 T_{high} = +125°C for OP-27A/OP-37A, OP-27B/OP-37B, OP-27C/OP-37C
 = +85°C for OP-27E/OP-37E, OP-27F/OP-37F, OP-27G/OP-37G
 = +70°C for OP-27EP/OP-37EP, OP-27FP/OP-37FP, OP-27GP/OP-37GP

6. TCV_{IO} performance is within specifications unnulled or when nulled with a potentiometer R_P = 8 kΩ to 20 kΩ.

ABBREVIATED CIRCUIT SCHEMATIC



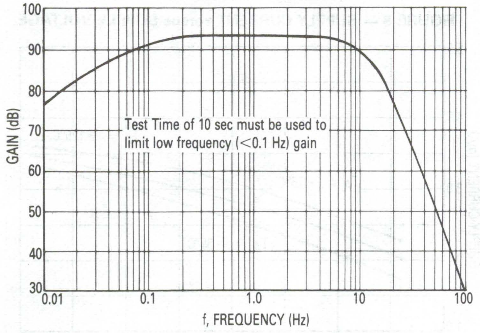
Offset Null
VCC
Q6
R3
R4
C2
R1*
R2*
Q22
C1
Q46
R23
R24
Q21
Q23
Q24
R9
Q20
Output
Non-Inverting Input (+)
Q1A
Q1B
Q2B
Q2A
R12
Q19
Inverting Input (−)
Q3
R5
C3
C4
Q45
R11
Q26
Q12
Q11
Q28
Q27
VEE

*R1 & R2 are trimmed at wafer test for minimum offset voltage.

TYPICAL CHARACTERISTICS

(Performance curves are for both OP-27 and OP-37 devices unless otherwise noted.)

FIGURE 1 — 0.1 Hz TO 10 Hz P-P NOISE TESTER FREQUENCY RESPONSE



Test Time of 10 sec must be used to limit low frequency (<0.1 Hz) gain

FIGURE 2 — VOLTAGE NOISE versus FREQUENCY

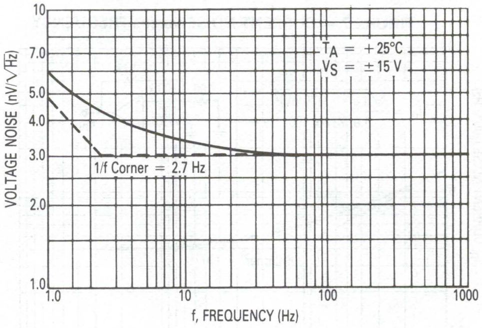


FIGURE 3 — INPUT WIDEBAND VOLTAGE NOISE versus BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)

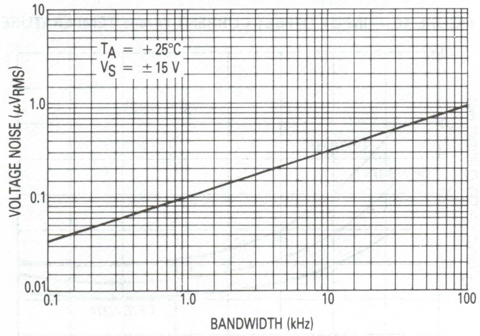


FIGURE 4 — TOTAL NOISE versus SOURCE RESISTANCE

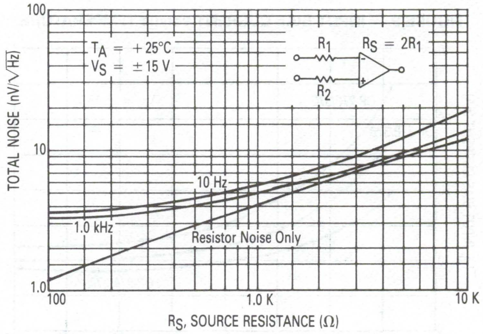


FIGURE 5 — VOLTAGE NOISE versus TEMPERATURE

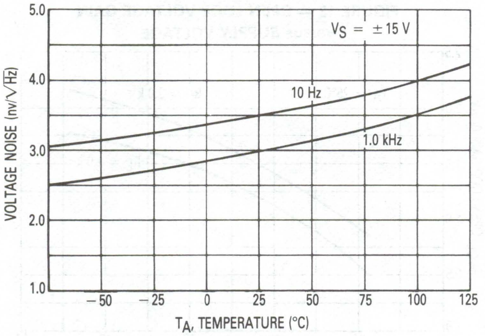


FIGURE 6 — VOLTAGE NOISE versus SUPPLY VOLTAGE

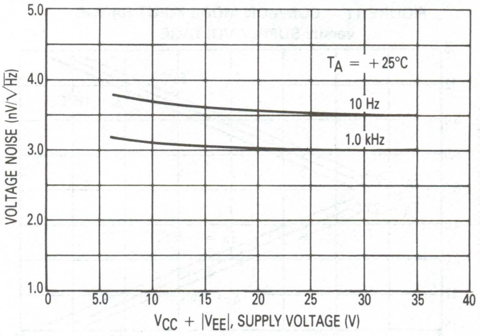


FIGURE 7 — CURRENT NOISE versus FREQUENCY

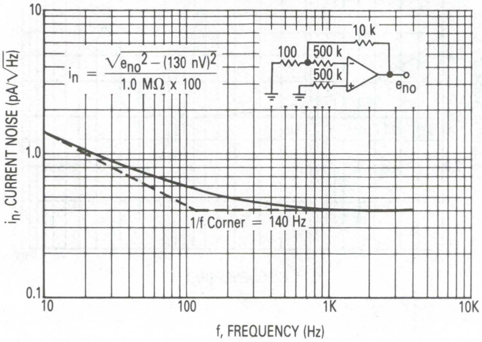


FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE

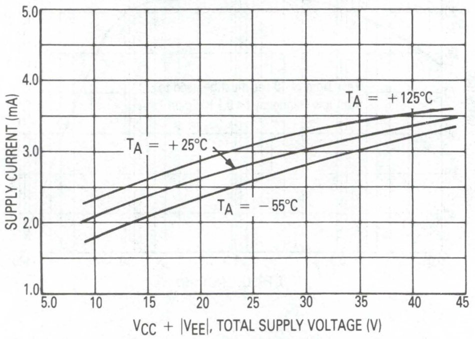


FIGURE 9 — INPUT BIAS CURRENT versus TEMPERATURE

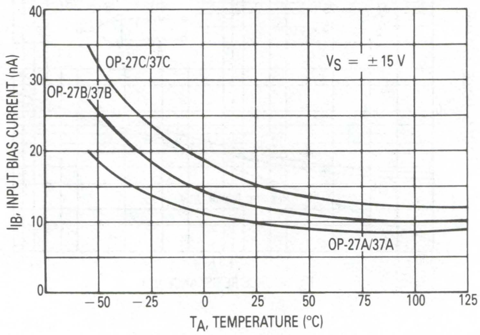


FIGURE 10 — INPUT OFFSET CURRENT versus TEMPERATURE

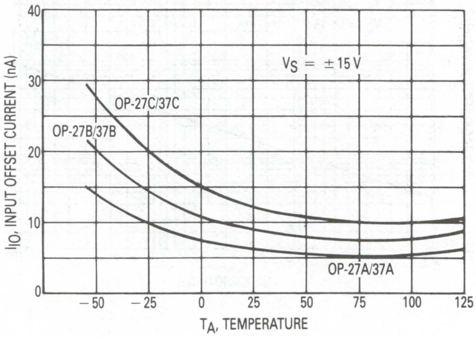


FIGURE 11 — COMMON MODE INPUT RANGE versus SUPPLY VOLTAGE

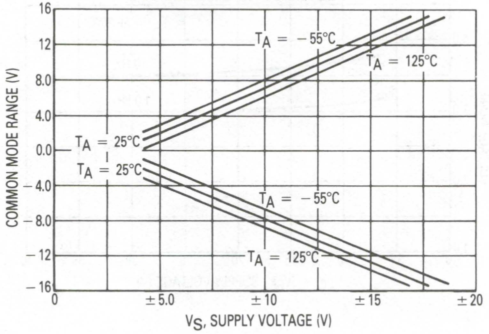


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

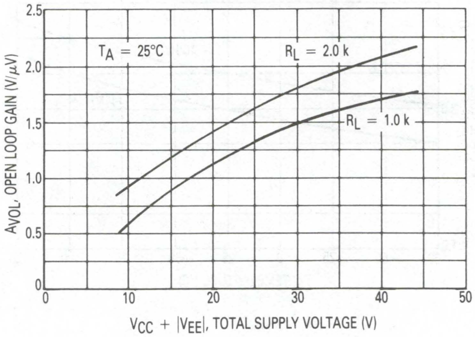


FIGURE 13 — OPEN LOOP VOLTAGE GAIN versus LOAD RESISTANCE

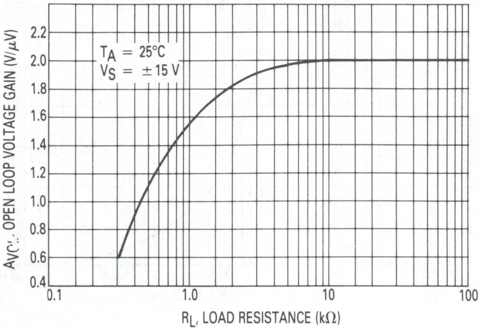


FIGURE 14 — MAXIMUM OUTPUT SWING versus RESISTIVE LOAD

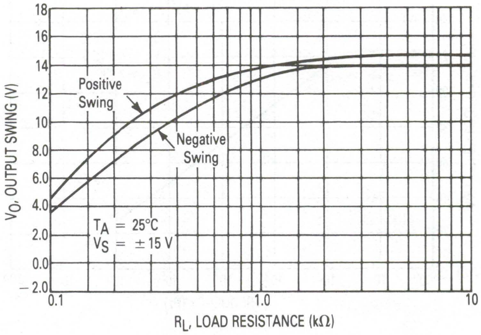


FIGURE 15 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

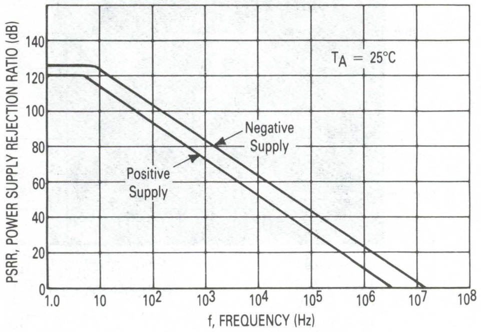


FIGURE 16 — OP-27 COMMON MODE REJECTION RATIO versus FREQUENCY

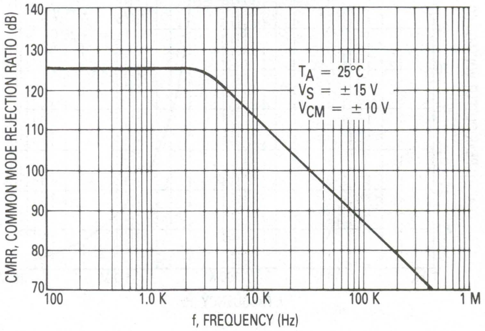


FIGURE 17 — OP-37 COMMON MODE REJECTION RATIO versus FREQUENCY

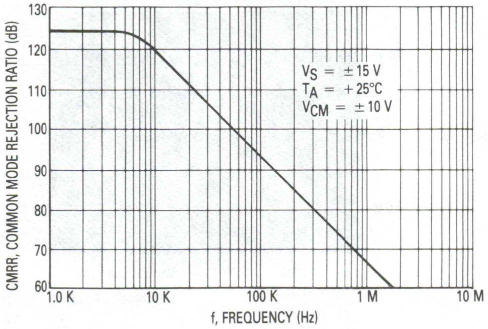


FIGURE 18 — OP-27 OPEN LOOP GAIN versus FREQUENCY

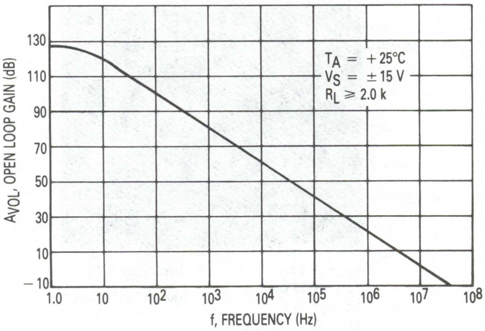


FIGURE 19 — OP-37 OPEN LOOP GAIN versus FREQUENCY

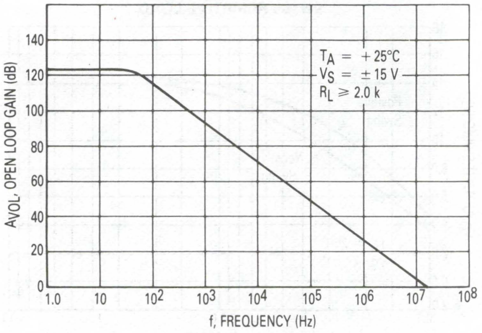


FIGURE 20 — OP-27 MAXIMUM UNDISTORTED OUTPUT versus FREQUENCY

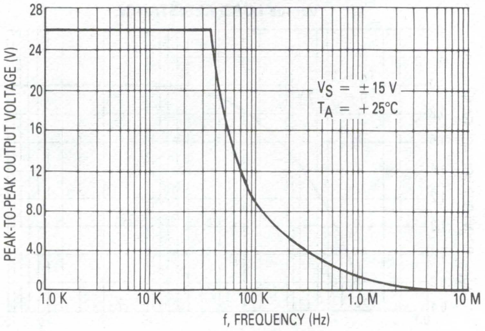


FIGURE 21 — OP-37 MAXIMUM UNDISTORTED OUTPUT versus FREQUENCY

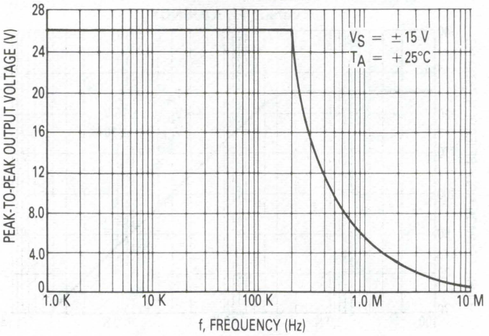
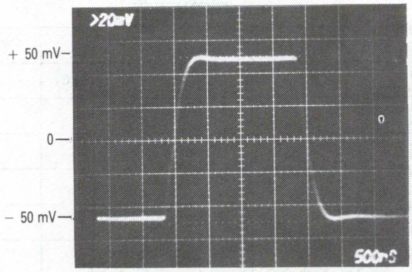


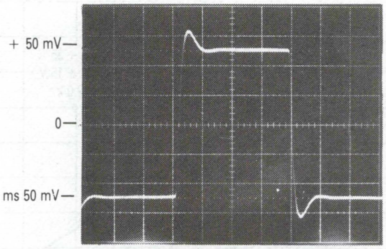
FIGURE 22 — OP-27 SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +1.0$
$T_A = +25°C$
$V_S = \pm 15$ V
$C_L = 12$ pF
$R_L = \infty$

Vertical: 20 mV/cm
Horizontal: 500 ns/cm

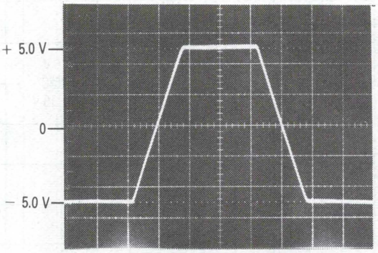
FIGURE 23 — OP-37 SMALL-SIGNAL TRANSIENT RESPONSE



$A_V = +5.0$
$T_A = +25°C$
$V_S = \pm 15$ V
$C_L = 27$ pF
$R_L = \infty$

Vertical: 20 mV/cm
Horizontal: 200 ns/cm

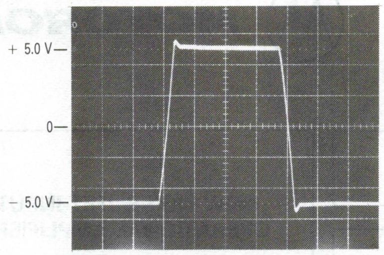
FIGURE 24 — OP-27 LARGE-SIGNAL TRANSIENT RESPONSE



$A_V = +1.0$
$T_A = +25°C$
$V_S = \pm 15$ V
$C_L = 12$ pF
$R_L = \infty$

Vertical: 2.0 V/cm
Horizontal: 2.0 μS/cm

FIGURE 25 — OP-37 LARGE-SIGNAL TRANSIENT RESPONSE



$A_V = +5.0$
$T_A = +25°C$
$V_S = \pm 15$ V
$C_L = 27$ pF
$R_L = \infty$

Vertical: 2.0 V/cm
Horizontal: 2.0 μS/cm

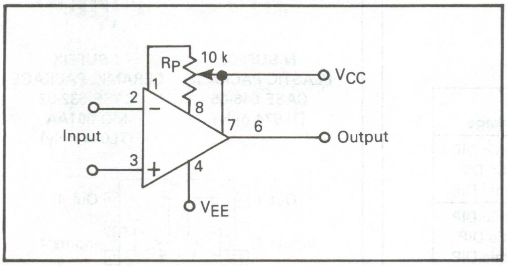
APPLICATIONS INFORMATION

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage and drift over temperature are permanently trimmed at wafer testing. However, if further adjustment of V_{IO} is required, nulling with a 10 kΩ potentiometer as shown in Figure 26 will not degrade TCV_{IO}. Other potentiometer values from 1.0 kΩ to 1.0 MΩ can be used with a slight degradation (0.1 to 0.2 μV/°C) of TCV_{IO}. Trimming to a value other than zero creates a drift of (V_{IO}/300) μV/°C, e.g. if V_{IO} is adjusted to 100 μV, the change in TCV_{IO} will be 0.33 μV/°C. The offset voltage adjustment range with a 10 kΩ potentiometer is ±4.0 mV. If a smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

FIGURE 26 — OFFSET NULLING CIRCUIT



NOISE MEASUREMENTS

The extremely low noise of these devices can make accurate measurement a difficult task. In order to realize the 80 nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following guidelines must be observed:

(1) The device has to be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4.0 μV due to its chip temperature increasing 14 to 20°C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of several nanovolts.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve (Figure 1) the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

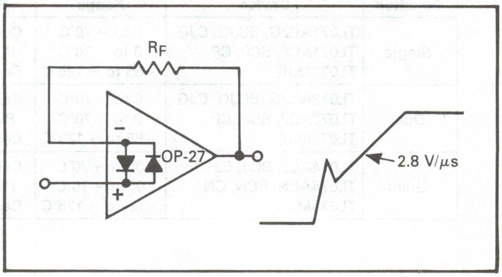
UNITY GAIN BUFFER APPLICATIONS FOR OP-27

When $R_F \leq 100$ Ω and the input is driven with a fast, large signal pulse (> 1.0 V), the output waveform will look as shown in Figure 27.

During the initial fast input step, the input protection diodes effectively short the output to the input and current limit only by the output short circuit protection of the signal generator. With $R_F \geq 500$ Ω, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2.0$ kΩ, a pole will be created with R_F and the amplifier's input capacitance (8.0 pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50 pF) in parallel with R_F will eliminate this problem.

FIGURE 27 — PULSED OPERATION



TL071
TL072
TL074

Specifications and Applications Information

MOTOROLA

LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

LOW-NOISE JFET INPUT OPERATIONAL AMPLIFIERS

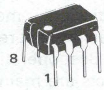
These low-noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low-noise and low harmonic distortion making them ideal for use in high-fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

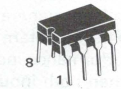
- Low Input Noise Voltage — 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion — 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance — 10^{12} Ω Typ
- High Slew Rate — 13 V/μs Typ
- Wide Gain Bandwidth — 4.0 MHz Typ
- Low Supply Current — 1.4 mA per Amp

ORDERING INFORMATION

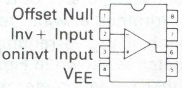
Op Amp Function	Device	Temperature Range	Package
Single	TL071ACJG, BCJG, CJG TL071ACP, BCP, CP TL071MJG	0 to +70°C 0 to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP
Dual	TL072ACJG, BCJG, CJG TL072ACP, BCP, CP TL072MJG	0 to +70°C 0 to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP
Quad	TL074ACJ, BCJ, CJ TL074ACN, BCN, CN TL074MJ	0° to +70°C 0° to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP



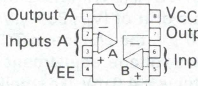
P SUFFIX
PLASTIC PACKAGE
CASE 626-04



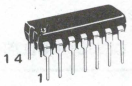
JG SUFFIX
CERAMIC PACKAGE
CASE 693-02


Offset Null
Inv+ Input
Noninvt Input
VEE
1
2
3
4
8
7
6
5
NC
VCC
Output
Offset Null

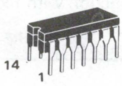
TL071 (Top View)


Output A
Inputs A
VEE
1
2
3
4
A
B
8
7
6
5
VCC
Output B
Inputs B

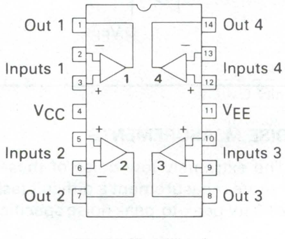
TL072 (Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646-05
(TL074 only)



J SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TL074 only)


Out 1
Inputs 1
VCC
Inputs 2
Out 2
1
2
3
4
5
6
7
1
2
3
4
14
13
12
11
10
9
8
Out 4
Inputs 4
VEE
Inputs 3
Out 3

TL074 (Top View)

MAXIMUM RATINGS

Rating	Symbol	TL07_ M	TL07_ C TL07_ AC TL07_ BC	Unit
Supply Voltage	V_{CC}	+18	+18	V
	V_{EE}	−18	−18	
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation				
Plastic Package (N,P)	P_D	—	680	mW
Derate above $T_A = +47°C$	$1/\theta_{JA}$	—	10	mW/°C
Ceramic Package (J, JG)	P_D	680	680	mW
Derate above $T_A = +82°C$	$1/\theta_{JA}$	10	10	mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = +25°$ unless otherwise noted).

		TL07_ M			TL07_ C TL07_ AC TL07_ BC			
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage ($R_S \leq 10$ k, $V_{CM} = 0$)	V_{IO}							mV
TL071, TL072		—	3.0	6.0	—	3.0	10	
TL074		—	3.0	9.0	—	3.0	10	
TL07_ A		—	—	—	—	3.0	6.0	
TL07_ B		—	—	—	—	2.0	3.0	
Average Temperature Coefficient of Input Offset Voltage $R_S = 50\ \Omega$, $T_A = T_{low}$ to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current ($V_{CM} = 0$) (Note 4)	I_{IO}							pA
TL07_		—	5.0	50	—	5.0	50	
TL07_ A, TL07_ B		—	—	—	—	5.0	50	
Input Bias Current ($V_{CM} = 0$) (Note 4)	I_{IB}							pA
TL07_		—	30	200	—	30	200	
TL07_ A, TL07_ B		—	—	—	—	30	200	
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}							V
TL07_		±11	+15, −12	—	±10	+15, −12	—	
TL07_ A, TL07_ B		—	—	—	±11	+15, −12	—	
Large-Signal Voltage Gain ($V_O = \pm 10$ V, $R_L \geq$, 2.0 k)	A_{VOL}							V/mV
TL07_		35	150	—	25	150	—	
TL07_ A, TL07_ B		—	—	—	50	150	—	
Output Voltage Swing (Peak-to-Peak) ($R_L = 10$ k)	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR							dB
TL07_		80	100	—	70	100	—	
TL07_ A, TL07_ B		—	—	—	80	100	—	
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR							dB
TL07_		80	100	—	70	100	—	
TL07_ A, TL07_ B		—	—	—	80	100	—	
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz
Slew Rate (See Figure 1) $V_{in} = 10$ V, $R_L = 2.0$ k, $C_L = 100$ pF	SR	10	13	—	—	13	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25° unless otherwise noted).

Characteristic	Symbol	TL07_ M Min	TL07_ M Typ	TL07_ M Max	TL07_ C TL07_ AC TL07_ BC Min	TL07_ C TL07_ AC TL07_ BC Typ	TL07_ C TL07_ AC TL07_ BC Max	Unit
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	—	18	—	nV/√Hz
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	—	0.01	—	pA/√Hz
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \leq$ 1.0 k $R_L \geq$ 2.0 k, f = 1000 Hz	THD	—	0.01	—	—	0.01	—	%
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 3]).

Characteristic	Symbol	TL07_ M Min	TL07_ M Typ	TL07_ M Max	TL07_ C TL07_ AC TL07_ BC Min	TL07_ C TL07_ AC TL07_ BC Typ	TL07_ C TL07_ AC TL07_ BC Max	Unit
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0)	V_{IO}							mV
TL071, TL072		—	—	9.0	—	—	13	
TL074		—	—	15	—	—	13	
TL07_ A		—	—	—	—	—	7.5	
TL07_ B		—	—	—		—	5.0	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							nA
TL07_		—	—	20	—	—	2.0	
TL07_ A, TL07_ B		—	—	—	—	—	2.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							nA
TL07_		—	—	50	—	—	7.0	
TL07_ A, TL07_ B		—	—	—	—	—	7.0	
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k)	A_{VOL}							V/mV
TL07_		20	—	—	15	—	—	
TL07_ A, TL07_ B		—	—	—	25	—	—	
Output Voltage Swing (Peak-to-Peak)	V_O							V
(RL ≥ 10 k)		24	—	—	24	—	—	
($R_L \geq$ 2.0 k)		20	—	—	20	—	—	

NOTES (Continued):

3. T_{low} = −55°C for TL071M, TL072M, TL074M
   = 0°C for TL071C, TL071AC, TL071BC
   TL072C, TL072AC, TL072BC
   TL074C, TL074AC, TL074BC

   T_{high} = +125°C for TL071M, TL072M, TL074M
   = +70°C for TL071C, TL071AC, TL071BC
   TL072C, TL072AC, TL072BC
   TL074C, TL074AC, TL074BC
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to ambient temperatures as possible, pulse techniques must be used during test.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

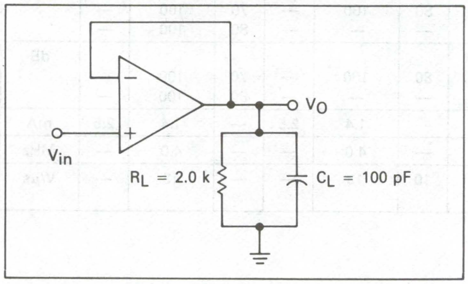


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER

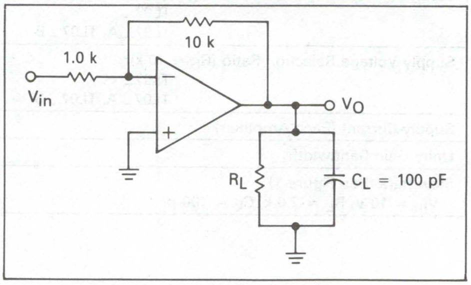


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

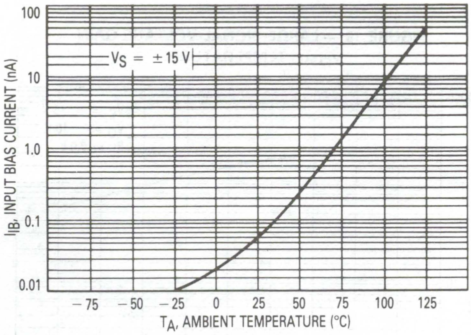


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

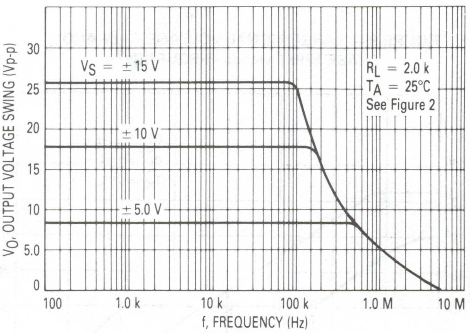


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

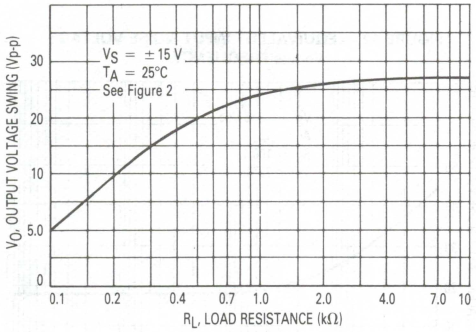


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

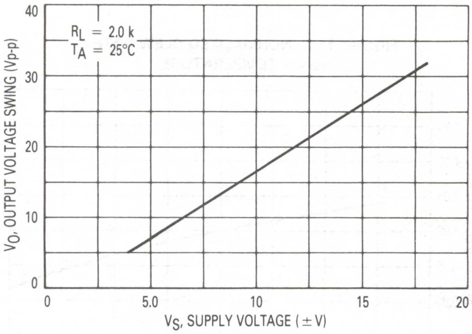


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

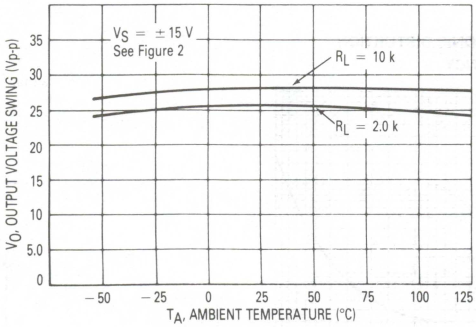


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

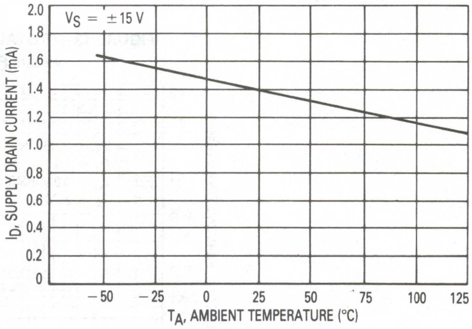


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

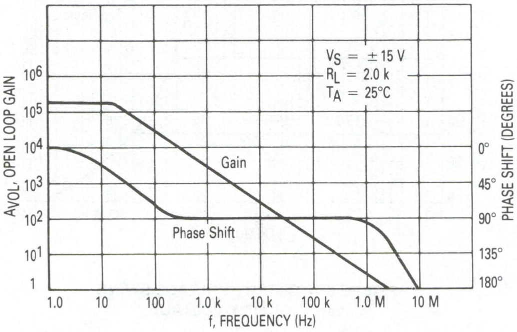


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

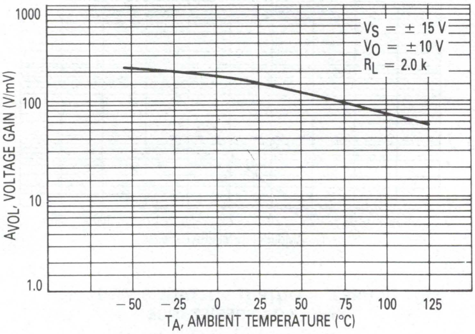


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

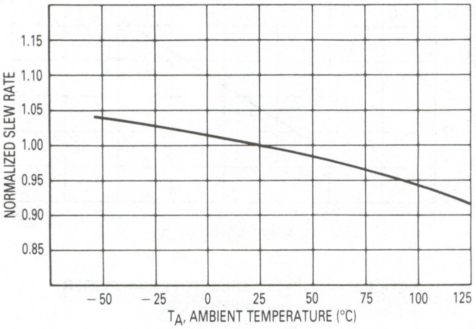


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

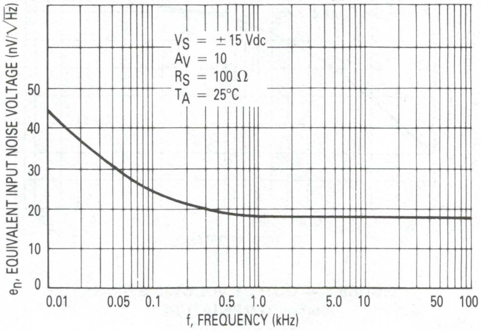
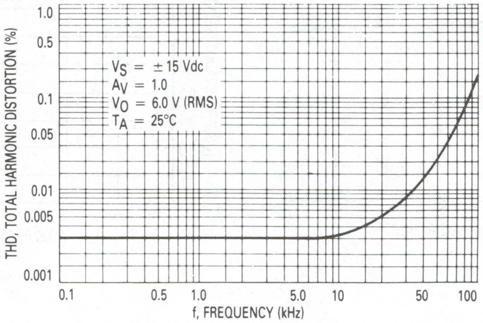


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)

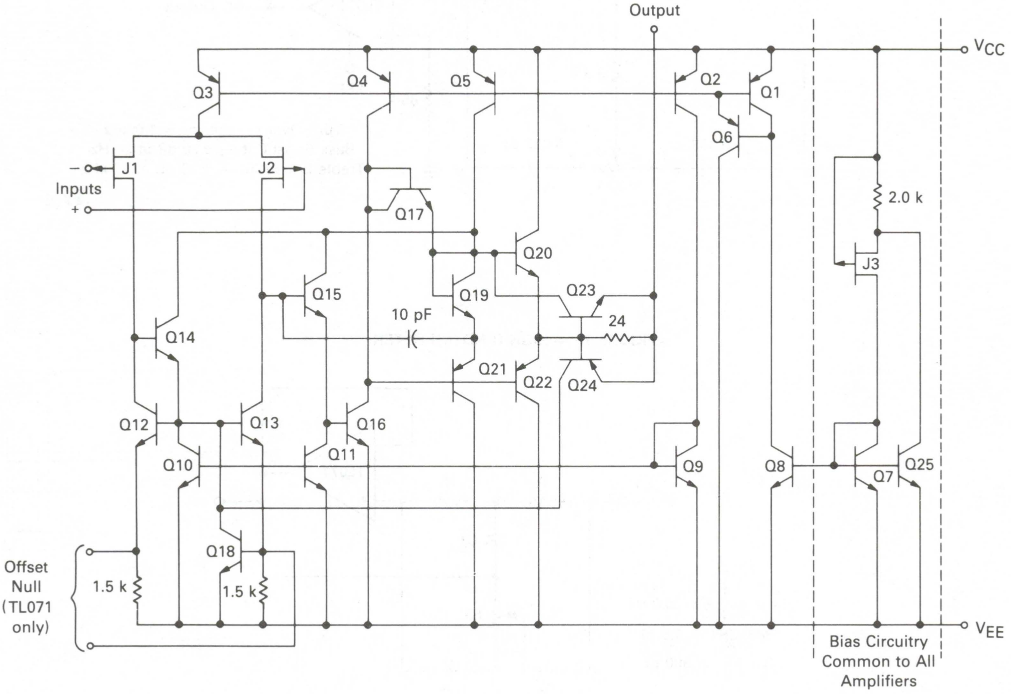
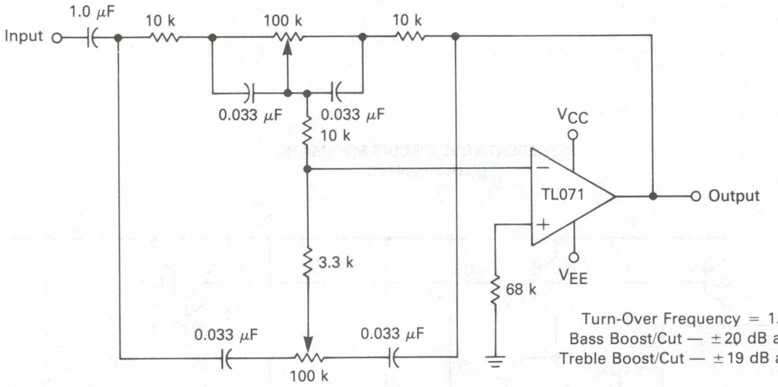
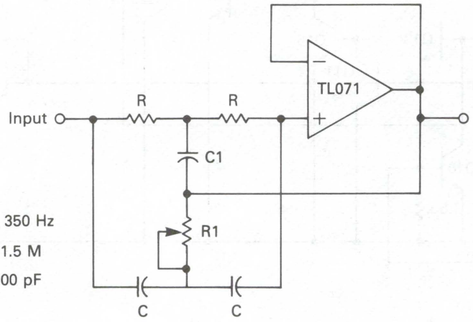

Output
VCC
VEE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
J1
J2
J3
Inputs
−
+
10 pF
24
2.0 k
1.5 k
1.5 k
Offset Null (TL071 only)
Bias Circuitry Common to All Amplifiers

FIGURE 14 — AUDIO TONE CONTROL AMPLIFIER


Input
1.0 μF
10 k
100 k
10 k
0.033 μF
0.033 μF
10 k
VCC
−
TL071
+
Output
VEE
3.3 k
68 k
0.033 μF
0.033 μF
100 k

Turn-Over Frequency = 1.0 kHz
Bass Boost/Cut — ±20 dB at 20 Hz
Treble Boost/Cut — ±19 dB at 20 kHz

FIGURE 15 — HIGH Q NOTCH FILTER


Input
R
R
−
TL071
+
C1
R1
C
C

$$f_o = \frac{1}{2\pi RC} = 350 \text{ Hz}$$
$$R = 2R1 = 1.5 \text{ M}$$
$$C = \frac{C1}{2} = 300 \text{ pF}$$

MOTOROLA

TL081
TL082
TL084

Specifications and Applications Information

JFET INPUT OPERATIONAL AMPLIFIERS

These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

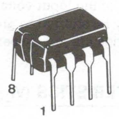
- Input Offset Voltage Options of 3.0, 6.0, and 15 mV Max
- Low Input Bias Current — 30 pA
- Low Input Offset Current — 5.0 pA
- Wide Gain Bandwidth — 3.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.4 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- Industry Standard Pinouts

ORDERING INFORMATION

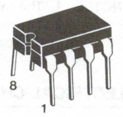
Op Amp Function	Device	Temperature Range	Package
Single	TL081ACJG, BCJG, CJG TL081ACP, BCP, CP TL081MJG	0 to +70°C 0 to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP
Dual	TL082ACJG, BCJG, CJG TL082ACP, BCP, CP TL082MJG	0 to +70°C 0 to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP
Quad	TL084ACJ, BCJ, CJ TL084ACN, BCN, CN TL084MJ	0 to +70°C 0 to +70°C −55 to +125°C	Ceramic DIP Plastic DIP Ceramic DIP

JFET-INPUT OPERATIONAL AMPLIFIERS

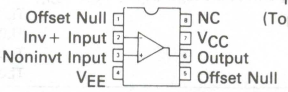
SILICON MONOLITHIC INTEGRATED CIRCUITS



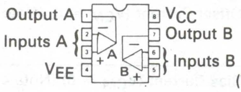
P SUFFIX
PLASTIC PACKAGE
CASE 626-04



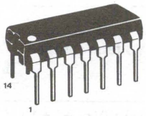
JG SUFFIX
CERAMIC PACKAGE
CASE 693-02


Offset Null
Inv+ Input
Noninvt Input
VEE
1
2
3
4
8
7
6
5
NC
VCC
Output
Offset Null

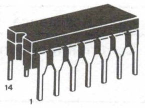
TL081
(Top View)


Output A
Inputs A
VEE
1
2
3
4
A
+
8
7
6
5
B
+
VCC
Output B
Inputs B

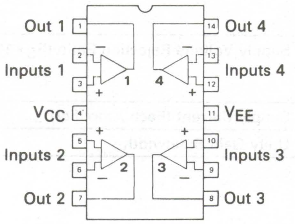
TL082
(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646-05
(TL084 only)



J SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TL084 only)


Out 1
Inputs 1
VCC
Inputs 2
Out 2
1
2
3
4
5
6
7
1
2
3
4
14
13
12
11
10
9
8
Out 4
Inputs 4
VEE
Inputs 3
Out 3

TL084 (Top View)

MAXIMUM RATINGS

Rating	Symbol	TL08__M	TL08__C TL08__AC TL08__BC	Unit
Supply Voltage	V_{CC}	+18	+18	V
	V_{EE}	−18	−18	
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation				
Plastic Package (N,P)	P_D	—	680	mW
Derate above $T_A = +47°C$	$1/\theta_{JA}$	—	10	mW/°C
Ceramic Package (J,JG)	P_D	680	680	mW
Derate above $T_A = +82°C$	$1/\theta_{JA}$	10	10	mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = +25°C$ unless otherwise noted).

Characteristic	Symbol	TL08__M			TL08__C TL08__AC TL08__BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k, $V_{CM} = 0$)	V_{IO}							mV
TL081, TL082		—	3.0	6.0	—	5.0	15	
TL084		—	3.0	9.0	—	5.0	15	
TL08__A		—	—	—	—	3.0	6.0	
TL08__B		—	—	—	—	2.0	3.0	
Average Temperature Coefficient of Input Offset Voltage $R_S = 50\ \Omega$, $T_A = T_{low}$ to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current ($V_{CM} = 0$) (Note 4)	I_{IO}							pA
TL08__		—	5.0	100	—	5.0	200	
TL08__A, TL08__B		—	—	—	—	5.0	100	
Input Bias Current ($V_{CM} = 0$) (Note 4)	I_{IB}							pA
TL08__		—	30	200	—	30	400	
TL08__A, TL08__B		—	—	—	—	30	200	
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}							V
TL08__		±11	+15, −12	—	±10	+15, −12	—	
TL08__A, TL08__B		—	—	—	±11	±15, −12	—	
Large-Signal Voltage Gain ($V_O = \pm 10$ V, $R_L \geq 2.0$ k)	A_{VOL}							V/mV
TL08__		25	150	—	25	150	—	
TL08__A, TL08__B		—	—	—	50	150	—	
Output Voltage Swing (Peak-to-Peak) $R_L = 10$ k	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR							dB
TL08__		80	100	—	70	100	—	
TL08__A, TL08__B		—	—	—	80	100	—	
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR							dB
TL08__		80	100	—	70	100	—	
TL08__A, TL08__B		—	—	—	80	100	—	
Supply Current (Each Amplifier)	I_D	—	1.4	2.8	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted).

Characteristic	Symbol	TL08__M			TL08__C TL08__AC TL08__BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	8.0	13	—	—	13	—	V/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	25	—	—	25	—	nV/$\sqrt{Hz}$
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 3].)

Characteristic	Symbol	TL08__M			TL08__C TL08__AC TL08__BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤10 k, V_{CM} = 0)	V_{IO}							mV
TL081, TL082		—	—	9.0	—	—	20	
TL084		—	—	15	—	—	20	
TL08__A		—	—	—	—	—	7.5	
TL08__B		—	—	—	—	—	5.0	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							nA
TL08__		—	—	20	—	—	5.0	
TL08__A, TL08__B		—	—	—	—	—	3.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							nA
TL08__		—	—	50	—	—	10	
TL08__A, TL08__B		—	—	—	—	—	7.0	
Large-Signal Voltage Gain (V_O = ±10 V, R_L≥2.0 k)	A_{VOL}							V/mV
TL08__		15	—	—	15	—	—	
TL08__A, TL08__B		—	—	—	25	—	—	
Output Voltage Swing (Peak-to-Peak)	V_O							V
(R_L≥10 k)		24	—	—	24	—	—	
(R_L≥2.0 k)		20	—	—	20	—	—	

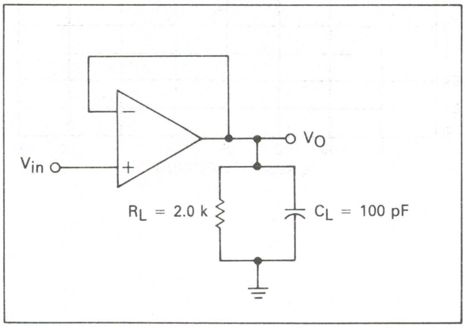
NOTES (continued):

3. T_{low} = −55°C for TL081M, TL082M, TL084M
   = 0°C for TL081C, TL081AC, TL081BC
   TL082C, TL082AC, TL082BC
   TL084C, TL084AC, TL084BC

   T_{high} = +125°C for TL081M, TL082M, TL084M
   = +70°C for TL081C, TL081AC, TL081BC
   TL082C, TL082AC, TL082BC
   TL084C, TL084AC, TL084BC
4. Input Bias currents of JFET input Op Amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during test.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER



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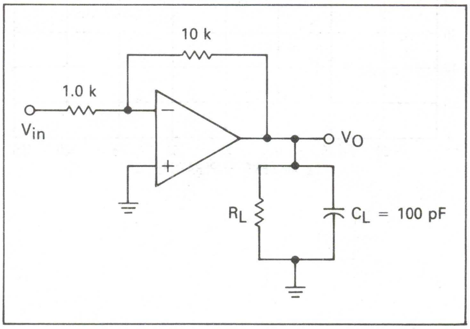


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

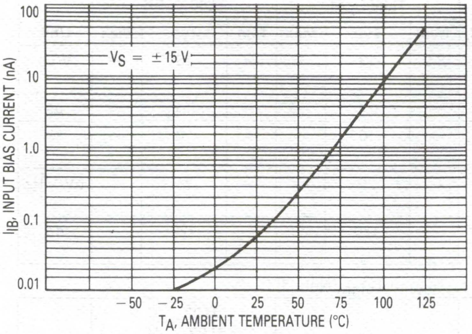


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

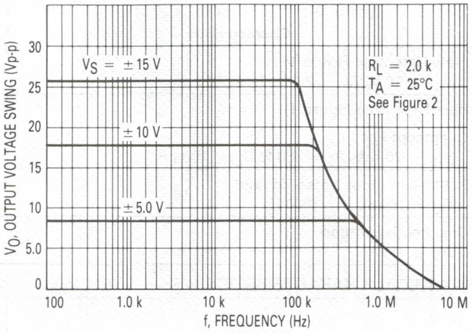


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

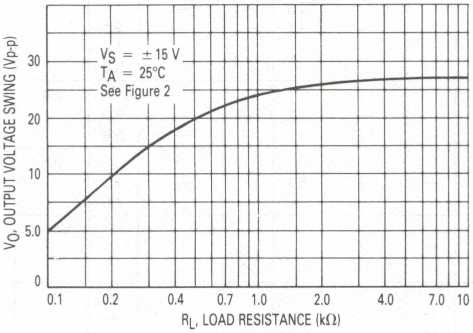


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

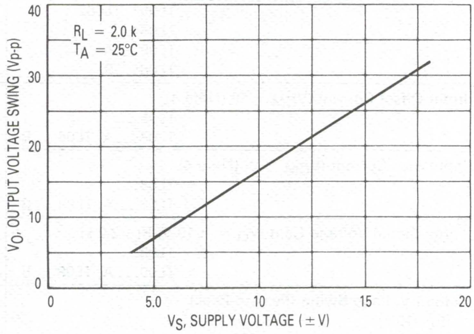


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

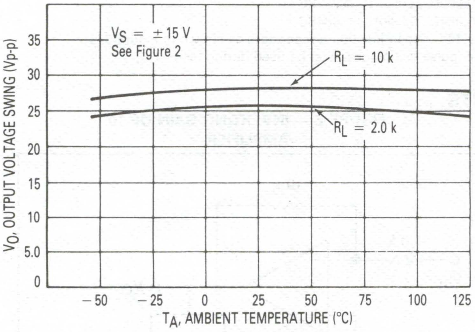


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

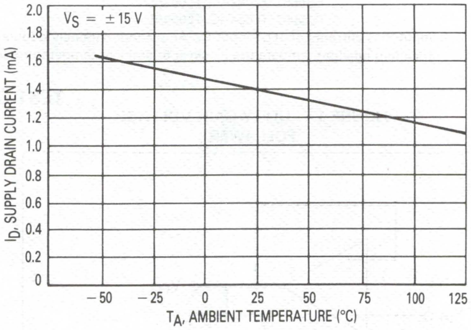


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

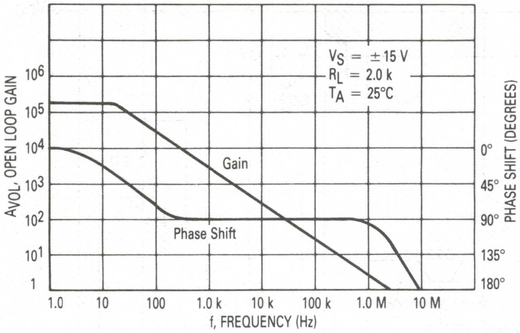


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

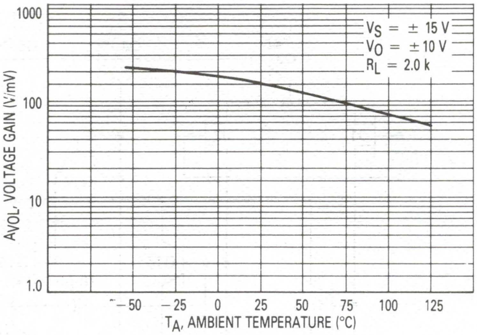


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

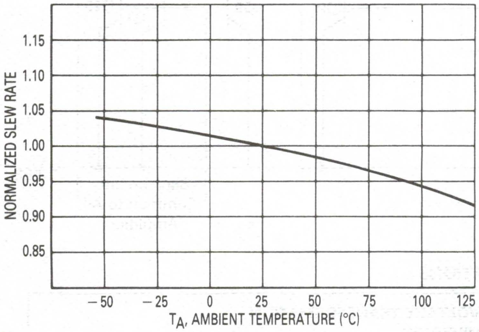


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

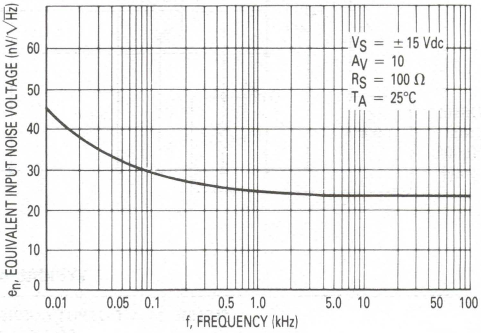
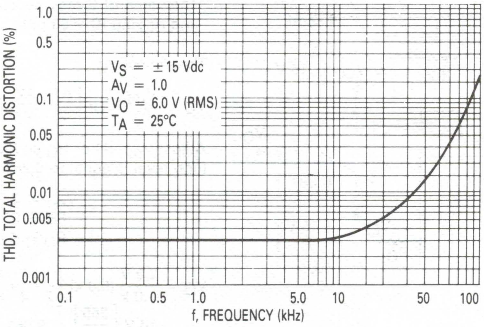
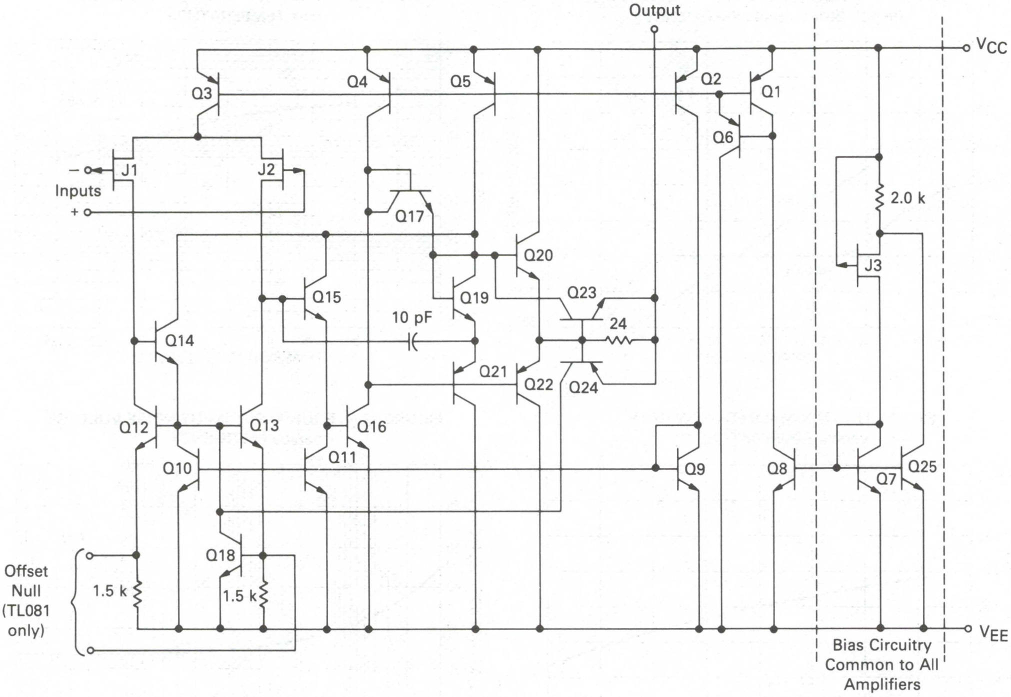


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



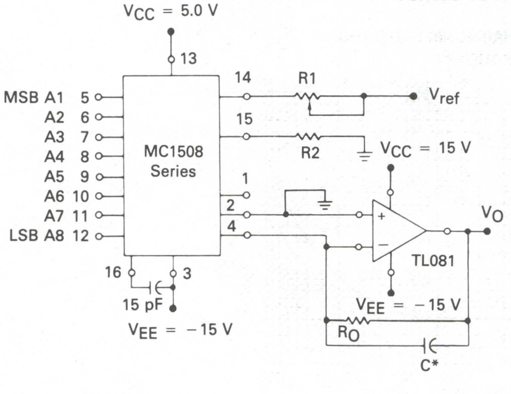
REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



Output
VCC
Q3
Q4
Q5
Q2
Q1
Q6
J1
J2
− Inputs +
Q17
2.0 k
Q20
J3
Q15
Q19
Q23
10 pF
24
Q14
Q21
Q22
Q24
Q12
Q13
Q16
Q11
Q10
Q9
Q8
Q7
Q25
Q18
Offset Null (TL081 only)
1.5 k
1.5 k
VEE
Bias Circuitry Common to All Amplifiers

TYPICAL APPLICATIONS

FIGURE 14 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



VCC = 5.0 V
13
14
R1
Vref
15
R2
VCC = 15 V
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1508 Series
1
2
4
+
−
VO
TL081
16
3
15 pF
VEE = −15 V
VEE = −15 V
RO
C*

Settling time to within ½ LSB (± 19.5 mV) is approximately 4.0 µs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

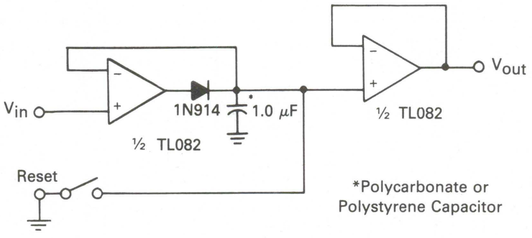
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0$ Vdc
$R_1 = R2 \approx 1.0$ kΩ
$R_O = 5.0$ kΩ

$$V_O = \frac{2.0\text{ V}}{1.0\text{ k}}(5.0\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

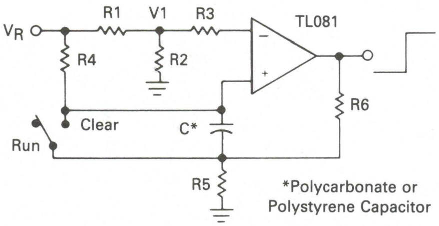
$$= 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

FIGURE 15 — POSITIVE PEAK DETECTOR


Vout
Vin
1N914
1.0 µF
½ TL082
½ TL082
Reset

*Polycarbonate or
Polystyrene Capacitor

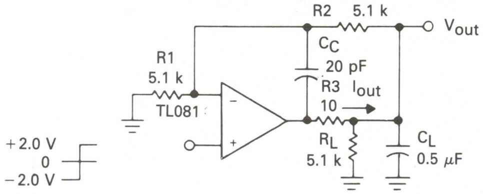
FIGURE 16 — LONG INTERVAL RC TIMER


VR
R1
V1
R3
TL081
R4
R2
R6
Clear
C*
Run
R5

*Polycarbonate or
Polystyrene Capacitor

Time (t) = R4 Cℓn ($V_R/V_R - V_1$), $R_3 = R_4$, $R_5 = 0.1$ R6
If R1 = R2: t = 0.693 R4C
Design Example: 100 Second Timer
V_R = 10 V
C = 1.0 µF
R3 = R4 = 144 M
R6 = 20 k
R5 = 2.0 k
R1 = R2 = 1.0 k

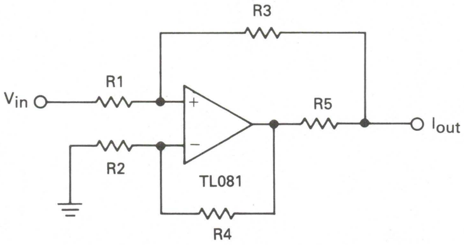
FIGURE 17 — ISOLATING LARGE CAPACITIVE LOADS


R2 5.1 k
Vout
CC
20 pF
R1
5.1 k
R3
Iout
10
TL081
+2.0 V
0
−2.0 V
RL
5.1 k
CL
0.5 µF

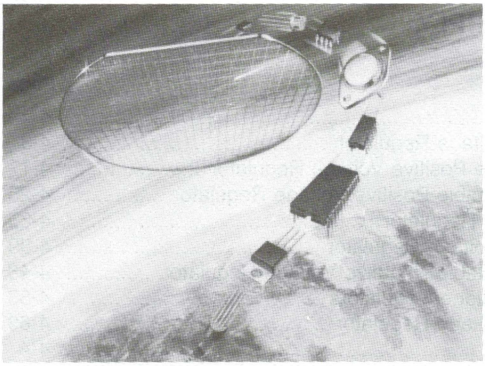
- Overshoot < 10%
- t_s = 10 µs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ \text{V}/\mu\text{s} = 0.04\ \text{V}/\mu\text{s (with } C_L \text{ shown)}$$

FIGURE 18 — VOLTAGE CONTROLLED CURRENT SOURCE


R3
Vin
R1
R5
Iout
R2
TL081
R4

If R1 through R4 >> R5 then $I_{out} = \frac{V_{in}}{R5}$



Power Supply

POWER SUPPLY

Device	Function	Page
LM109	Positive Voltage Regulator	4-4
LM117	3-Terminal Adjustable Positive Voltage Regulator	4-9
LM117L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	4-17
LM117M	Medium-Current 3-Terminal Adjustable Positive Voltage Regulator	4-25
LM123,A	3-Ampere, 5 Volt Positive Voltage Regulator	4-33
LM137	3-Terminal Adjustable Negative Voltage Regulator	4-39
LM137M	Medium-Current 3-Terminal Adjustable Negative Voltage Regulator	4-46
LM140,A	Three-Terminal Positive Fixed Voltage Regulators	4-53
LM150	3-Terminal Adjustable Positive Voltage Regulator	4-69
LM209	Positive Voltage Regulator	4-4
LM217	3-Terminal Adjustable Positive Voltage Regulator	4-9
LM217L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	4-17
LM217M	Medium-Current 3-Terminal Adjustable Positive Voltage Regulator	4-25
LM223,A	3-Ampere, 5 Volt Positive Voltage Regulator	4-33
LM237	3-Terminal Adjustable Negative Voltage Regulator	4-39
LM237M	Medium-Current 3-Terminal Adjustable Negative Voltage Regulator	4-46
LM250	3-Terminal Adjustable Positive Voltage Regulator	4-69
LM309	Positive Voltage Regulator	4-4
LM317	3-Terminal Adjustable Positive Voltage Regulator	4-9
LM317L	Low-Current 3-Terminal Adjustable Positive Voltage Regulator	4-17
LM317M	Medium-Current 3-Terminal Adjustable Positive Voltage Regulator	4-25
LM323,A	3-Ampere, 5 Volt Positive Voltage Regulator	4-33
LM337	3-Terminal Adjustable Negative Voltage Regulator	4-39
LM337M	Medium-Current 3-Terminal Adjustable Negative Voltage Regulator	4-46
LM340,A	Three-Terminal Positive Fixed Voltage Regulators	4-53
LM350	3-Terminal Adjustable Positive Voltage Regulator	4-69
MC1463	Adjustable Negative Voltage Regulator	4-77
MC1466L	Voltage and Current Regulator	4-93
MC1468	Dual ±15-Volt Tracking Regulator	4-103
MC1469	Adjustable Positive Voltage Regulator	4-109
MC1563	Adjustable Negative Voltage Regulator	4-77
MC1566L	Voltage and Current Regulator	4-93
MC1568	Dual ±15-Volt Tracking Regulator	4-103
MC1569	Adjustable Positive Voltage Regulator	4-109
MC1723,C	Adjustable Positive or Negative Voltage Regulator	4-128
MC3324,A	Power Supply Supervisory Circuit/Dual-Voltage Comparator	4-160
MC3420	Switchmode Regulator Control Circuit	4-134
MC3423	Overvoltage Sensing Circuit	4-153
MC3424,A	Power Supply Supervisory Circuit/Dual-Voltage Comparator	4-160
MC3425,A	Power Supply Supervisory/Over-Under-Voltage Protection Circuit	4-176
MC3520	Switchmode Regulator Control Circuit	4-134
MC3523	Overvoltage Sensing Circuit	4-153
MC3524,A	Power Supply Supervisory/Over-Under-Voltage Protection Circuit	4-160
MC3525,A	Power Supply Supervisory/Over-Under-Voltage Protection Circuit	4-176
MC7800 Series	3-Terminal Positive Voltage Regulators	4-186
MC78L00C,AC Series	Positive Voltage Regulators	4-198
MC78M00BC Series	Positive Voltage Regulator	4-204
MC78T00 Series	Three-Ampere Positive Voltage Regulators	4-212
MC7900C Series	Three-Terminal Negative Fixed Voltage Regulators	4-225
MC79L00C,AC Series	Three-Terminal Negative Fixed Voltage Regulators	4-234
MC79M00 Series	Three-Terminal Negative Fixed Voltage Regulators	4-240
MC33063	DC to DC Converter Control Circuits	4-273
MC34060	Switchmode Pulse Width Modulation Control Circuits	4-243
MC34061,A	Three-Terminal Programmable Overvoltage Sensing Circuit	4-255

Device	Function	Page
MC34062	Pin-Programmable Overvoltage Sensing Circuit	4-262
MC34063	DC to DC Converter Control Circuits	4-273
MC35060	Switchmode Pulse Width Modulation Control Circuits	4-243
MC35061,A	Three-Terminal Programmable Overvoltage Sensing Circuit	4-255
MC35062	Pin-Programmable Overvoltage Sensing Circuit	4-262
MC35063	DC to DC Converter Control Circuits	4-273
SG1525A	Pulse Width Modulator Control Circuits	4-279
SG1526	Pulse Width Modulation Control Circuits	4-286
SG1527A	Pulse Width Modulator Control Circuits	4-279
SG2525A	Pulse Width Modulator Control Circuits	4-279
SG2526	Pulse Width Modulation Control Circuits	4-286
SG2527A	Pulse Width Modulator Control Circuits	4-279
SG3525A	Pulse Width Modulator Control Circuits	4-279
SG3526	Pulse Width Modulation Control Circuits	4-286
SG3527A	Pulse Width Modulator Control Circuits	4-279
TCA5600	Universal Microprocessor Power Supply Controller	4-294
TCF5600	Universal Microprocessor Power Supply Controller	4-294
TDA4600	Flyback Converter Regulator Control Circuit	4-305
TL431 Series	Programmable Precision References	4-311
TL494	Switchmode Pulse Width Modulation Control Circuits	4-319
TL495	Switchmode Pulse Width Modulation Control Circuits	4-319
TL780	Three-Terminal Positive Voltage Regulators	4-330
μA78S40	Universal Switching Regulator Subsystem	4-336

LM109
LM209
LM309

MOTOROLA

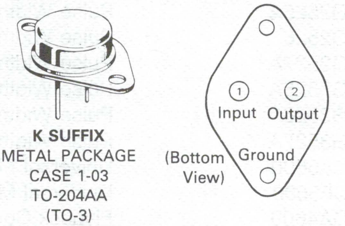
MONOLITHIC POSITIVE THREE - TERMINAL FIXED VOLTAGE REGULATOR

A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

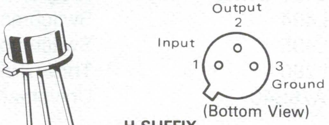
In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

- High Maximum Output Current – Over 1.0 Ampere in TO-3 type Package – Over 200 mA in TO-39 type Package.
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

POSITIVE VOLTAGE REGULATOR


1
2
Input
Output
(Bottom View)
Ground

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)

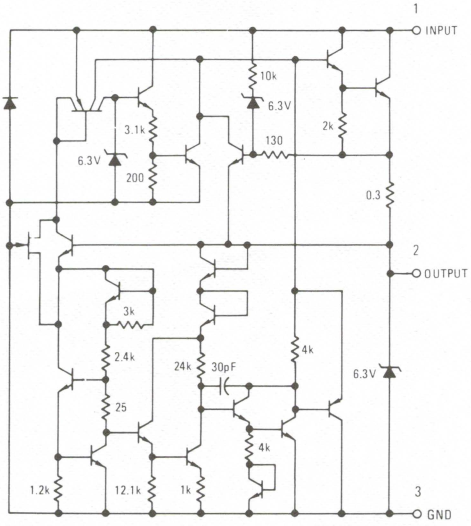

Output
2
Input
1
3
Ground
(Bottom View)

H SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO 39)

ORDERING INFORMATION

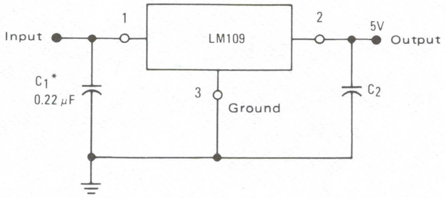
Device	Temperature Range	Package
LM109H	$T_J = -55^oC$ to $+150^oC$	Metal Can
LM109K	$T_J = -55^oC$ to $+150^oC$	Metal Power
LM209H	$T_J = -55^oC$ to $+150^oC$	Metal Can
LM209K	$T_J = -55^oC$ to $+150^oC$	Metal Power
LM309H	$T_J = 0^oC$ to $+125^oC$	Metal Can
LM309K	$T_J = 0^oC$ to $+125^oC$	Metal Power

CIRCUIT SCHEMATIC


1
INPUT
10k
6.3V
2k
3.1k
6.3V
200
130
0.3
2
OUTPUT
3k
2.4k
24k
30pF
4k
6.3V
25
4k
1.2k
12.1k
1k
3
GND

TYPICAL APPLICATION

FIXED 5.0 V REGULATOR


Input
1
LM109
2
5V
Output
C1*
0.22 μF
3
Ground
C2

*Required if regulator is located an appreciable distance from power supply filter.
Although no output capacitor is needed for stability, it does improve transient response.

LM109, LM209, LM309

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range	T_J		°C
LM109		-55 to +150	
LM209		-55 to +150	
LM309		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering, t = 60 s)	T_S	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	LM109/LM209 ①			LM309 ②			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25°C$)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation ($T_J = +25°C$) $7.0 \leqslant V_{in} \leqslant 25$ V	Reg_{line}		4.0	50		4.0	50	mV
Load Regulation ($T_J = +25°C$)	Reg_{load}							mV
Case 11-01 **(type TO-3)** $5.0 \text{ mA} \leqslant I_O \leqslant 1.5\text{A}$			50	100		50	100	
Case 79-02 **(TO-39)** $5.0 \text{ mA} \leqslant I_O \leqslant 0.5\text{A}$			20	50		20	50	
Output Voltage Range $7.0 \text{ V} \leqslant V_{in} \leqslant 25$ V $5.0 \text{ mA} \leqslant I_O \leqslant I_{max}, P \leqslant P_{max}$	V_O	4.6		5.4	4.75		5.25	Vdc
Quiescent Current ($7.0 \text{ V} \leqslant V_{in} \leqslant 25$ V)	I_B		5.2	10	–	5.2	10	mAdc
Quiescent Current Change ($7.0 \text{ V} \leqslant V_{in} \leqslant 25$ V)	ΔI_B			0.5			0.5	
$5.0 \text{ mA} \leqslant I_O \leqslant I_{max}$				0.8		–	0.8	
Output Noise Voltage ($T_A = +25°C$) $10 \text{ Hz} \leqslant f \leqslant 100$ kHz	V_N		40		–	40	–	µV
Long Term Stability	S		–	10	–	–	20	mV
Thermal Resistance, Junction to Case ③	θJC							°C/W
Case 1 (type TO-3)		–	3.0		–	3.0	–	
Case 79-02 (TO-39)			15		–	15		

NOTES:

① Unless otherwise specified, these specifications apply for $-55°C \leqslant T_J \leqslant +150°$ ($-25°C \leqslant T_J \leqslant +150°C$ for the LM209). For Case 79-02 (TO-39) $V_{in} = 10$ V, $I_O = 0.1$ A, $I_{max} = 0.2$ A and $P_{max} = 2.0$ W. For Case 1 **(type TO-3)** $V_{in} = 10$ V, $I_O = 0.5$ A, $I_{max} = 1.0$ A and $P_{max} = 20$ W.

② Unless otherwise specified, these specifications apply for $0°C \leqslant T_J \leqslant +125°C$, $V_{in} = 10$V. For Case 79-02 (TO-39) $I_O = 0.1$A, $I_{max} = 0.2$A and, $P_{max} = 2.0$ W. For Case 1 (type TO-3) $I_O = 0.5$ A, $I_{max} = 1.0$ A and $P_{max} = 20$ W.

③ Without a heat sink, the thermal resistance of the Case 79-02 **(TO-39)** package is about 150°C/W, while that of the Case 1 (type TO-3) package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

($V_{in} = 10$ V, $T_A = +25°C$ unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (LM109K, LM209K)

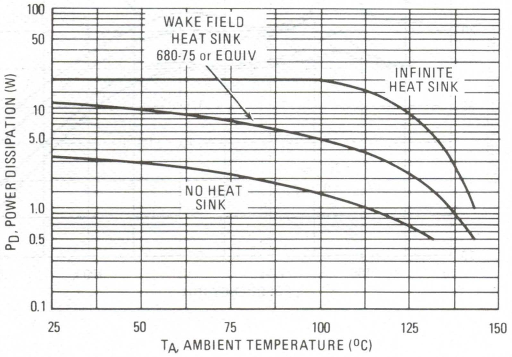
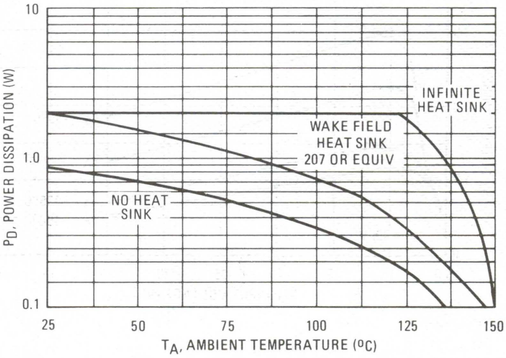


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (LM109H, LM209H)



TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

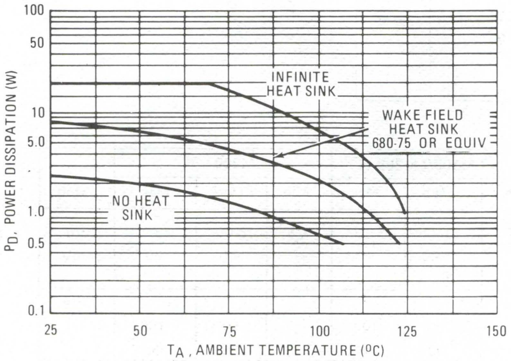


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

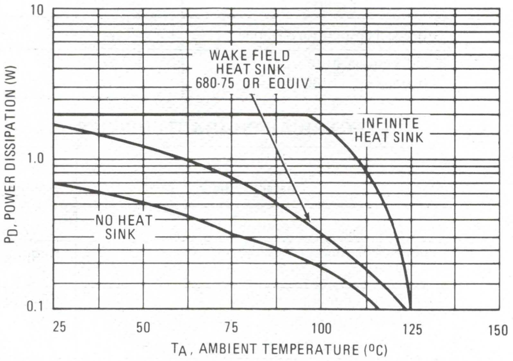


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

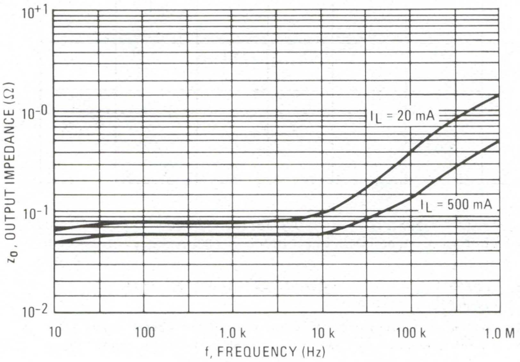


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

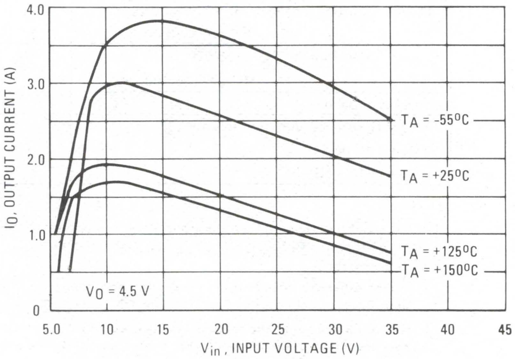


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

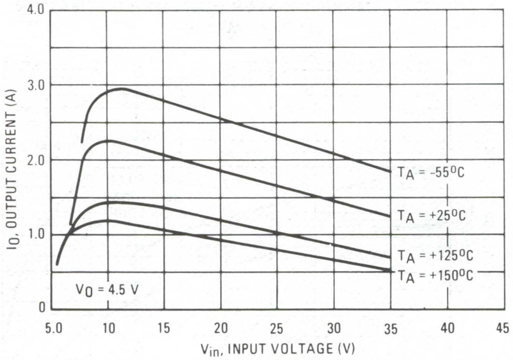
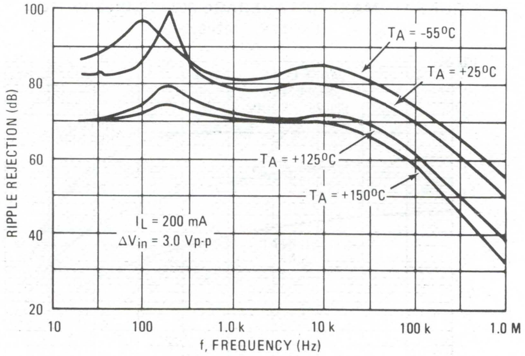


FIGURE 8 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

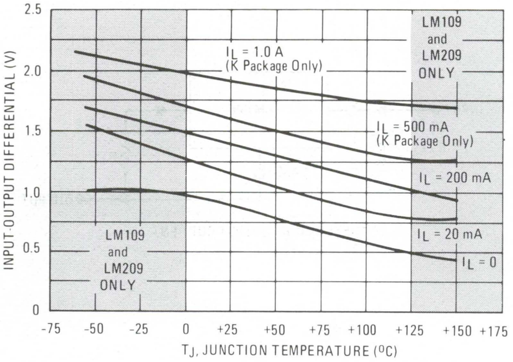


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

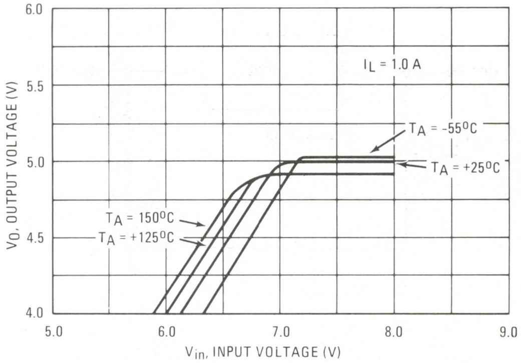


FIGURE 11 – OUTPUT VOLTAGE

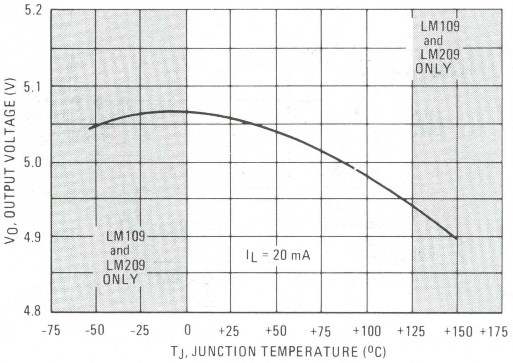


FIGURE 12 – OUTPUT NOISE VOLTAGE

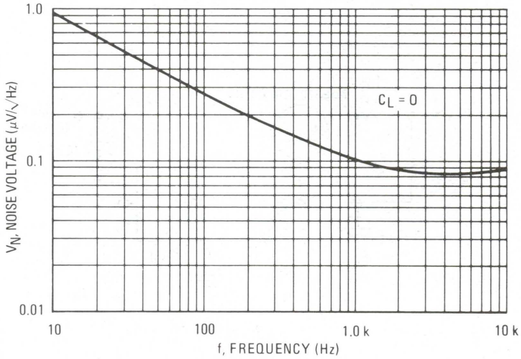


FIGURE 13 – QUIESCENT CURRENT

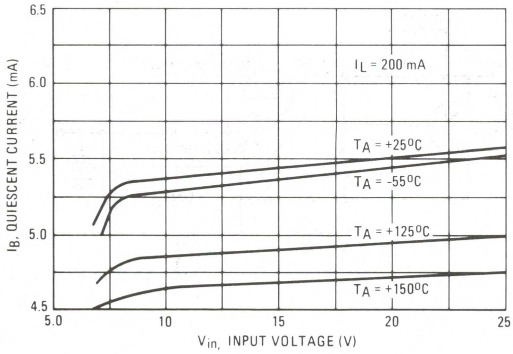
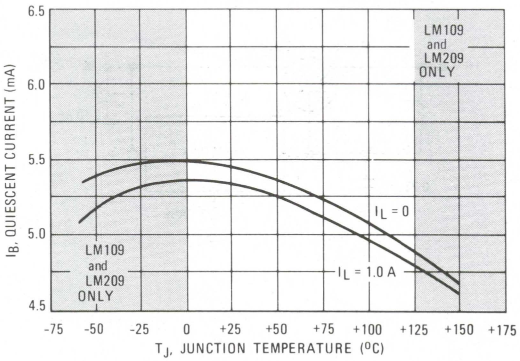


FIGURE 14 – QUIESCENT CURRENT



TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

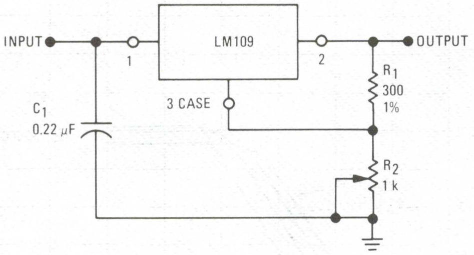
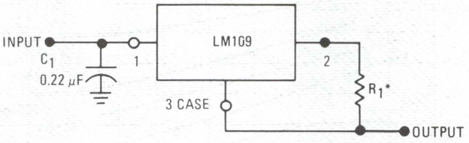

INPUT
LM109
1
2
OUTPUT
3 CASE
C_1
0.22 µF
R_1
300
1%
R_2
1 k

FIGURE 16 – CURRENT REGULATOR


INPUT
C_1
0.22 µF
1
LM109
2
3 CASE
R_1*
OUTPUT

*DETERMINES OUTPUT CURRENT.

FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

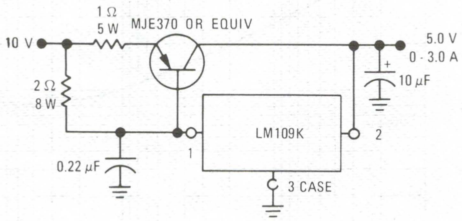

1 Ω
5 W
MJE370 OR EQUIV
10 V
5.0 V
0 - 3.0 A
10 µF
2 Ω
8 W
LM109K
1
2
0.22 µF
3 CASE

FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

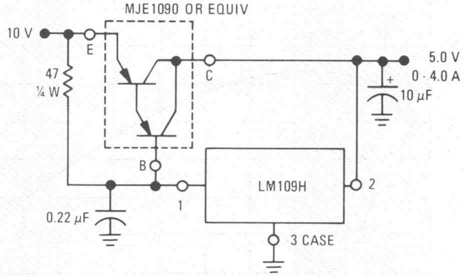

MJE1090 OR EQUIV
10 V
E
C
47
¼ W
5.0 V
0 - 4.0 A
10 µF
B
LM109H
1
2
0.22 µF
3 CASE

FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

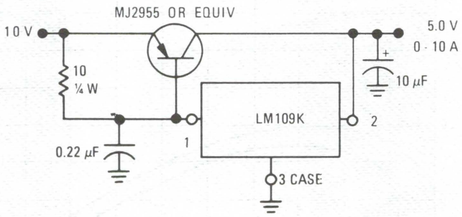
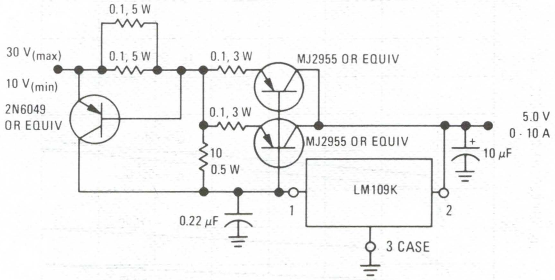

MJ2955 OR EQUIV
10 V
5.0 V
0 - 10 A
10
¼ W
10 µF
LM109K
1
2
0.22 µF
3 CASE

FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for Safe-Area Protection of pass transistors)


0.1, 5 W
30 V(max)
0.1, 5 W
0.1, 3 W
MJ2955 OR EQUIV
10 V(min)
2N6049
OR EQUIV
0.1, 3 W
10
0.5 W
MJ2955 OR EQUIV
5.0 V
0 - 10 A
10 µF
LM109K
1
2
0.22 µF
3 CASE

MOTOROLA

LM117
LM217
LM317

Specifications and Applications Information

3-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

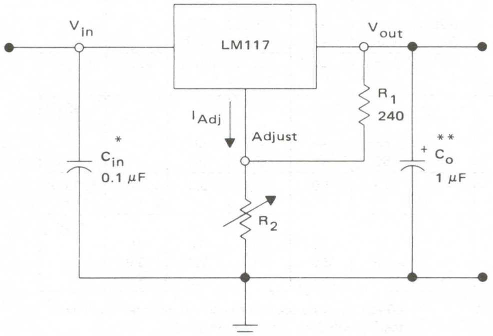
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



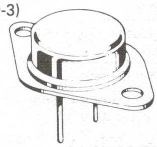
* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

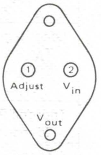
** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ \left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



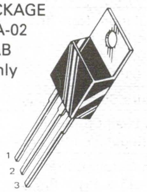


(Bottom View)

Case is output

Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

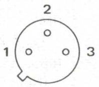
T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB
LM317 only



Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

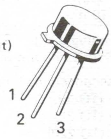
Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)



(Bottom View)

(Case is output)



Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117H	T_J = −55°C to +150°C	Metal Can
LM117K	T_J = −55°C to +150°C	Metal Power
LM217H	T_J = −25°C to +150°C	Metal Can
LM217K	T_J = −25°C to +150°C	Metal Power
LM317H	T_J = 0°C to +125°C	Metal Can
LM317K	T_J = 0°C to +125°C	Metal Power
LM317T	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J		°C
LM117		−55 to +150	
LM217		−25 to +150	
LM317		0 to +125	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_I-V_O = 5.0 V; I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217			LM317			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5.0 V			—	5.0	15	—	5.0	25	mV
V_O ≥ 5.0 V			—	0.1	0.3	—	0.1	0.5	% V_O
Thermal Regulation (T_A = +25°C) 20 ms Pulse	—	—	—	0.02	0.07	—	0.03	0.07	%/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
V_O ≤ 5.0 V			—	20	50	—	20	70	mV
V_O ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current	3	I_{max}							A
V_I-V_O ≤ 15 V, P_D ≤ P_{max}									
K and T Packages			1.5	2.2	—	1.5	2.2	—	
H Package			0.5	0.8	—	0.5	0.8	—	
V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C									
K and T Packages			0.25	0.4	—	0.15	0.4	—	
H Package			—	0.07	—	—	0.07	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{Adj}			—	65	—	—	65	—	
C_{Adj} = 10 μF			66	80	—	66	80	—	
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
H Package (TO-39)			—	12	15	—	12	15	
K Package (TO-3)			—	2.3	3.0	—	2.3	3.0	
T Package (TO-220)			—	—	—	—	5.0	—	

NOTES:
(1) T_{low} = −55°C for LM117 T_{high} = +150°C for LM117
= −25°C for LM217 = +150°C for LM217
= 0°C for LM317 = +125°C for LM317
(2) I_{max} = 1.5 A for K (TO-3) and T (TO-220) Packages
= 0.5 A for H (TO-39) Package
P_{max} = 20 W for K (TO-3) Package
= 20 W for T (TO-220) Package
= 2.0 W for H (TO-39) Package
(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
(4) Selected devices with tightened tolerance reference voltage available.
(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.
(6) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

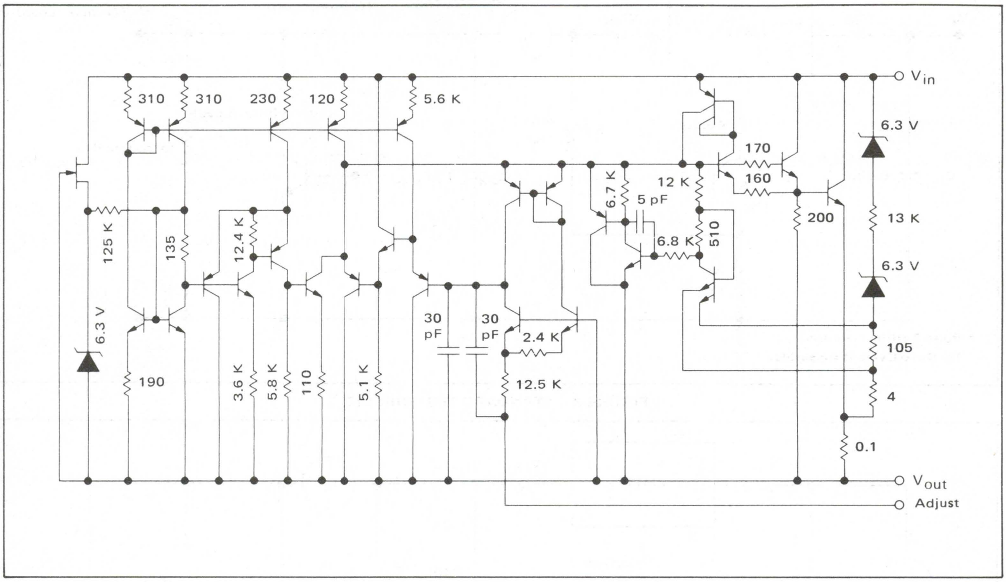

310
310
230
120
5.6 K
Vin
6.3 V
170
160
12 K
6.7 K
5 pF
200
13 K
125 K
135
12.4 K
6.8 K
510
6.3 V
6.3 V
30 pF
30 pF
2.4 K
105
190
3.6 K
5.8 K
110
5.1 K
12.5 K
4
0.1
Vout
Adjust

FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

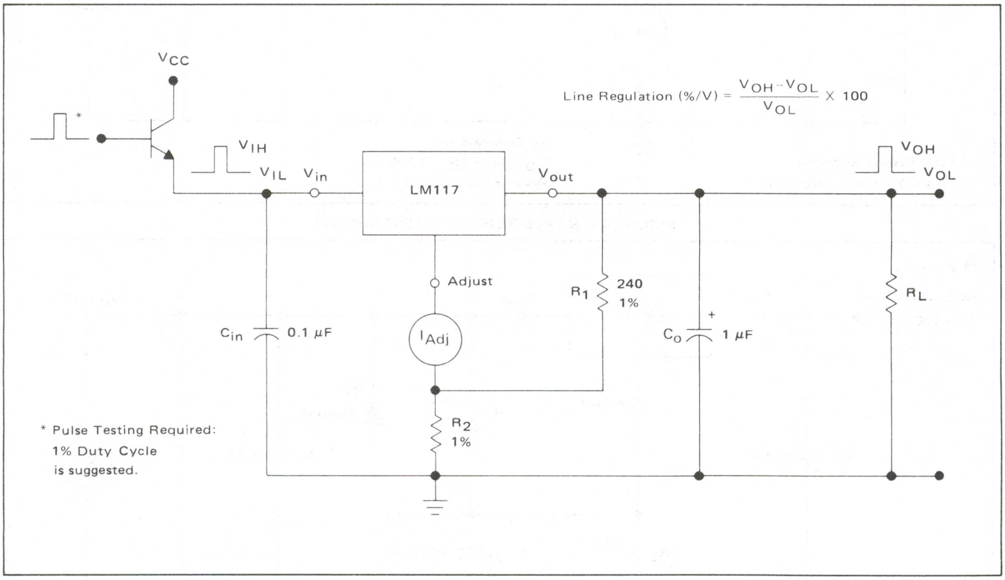
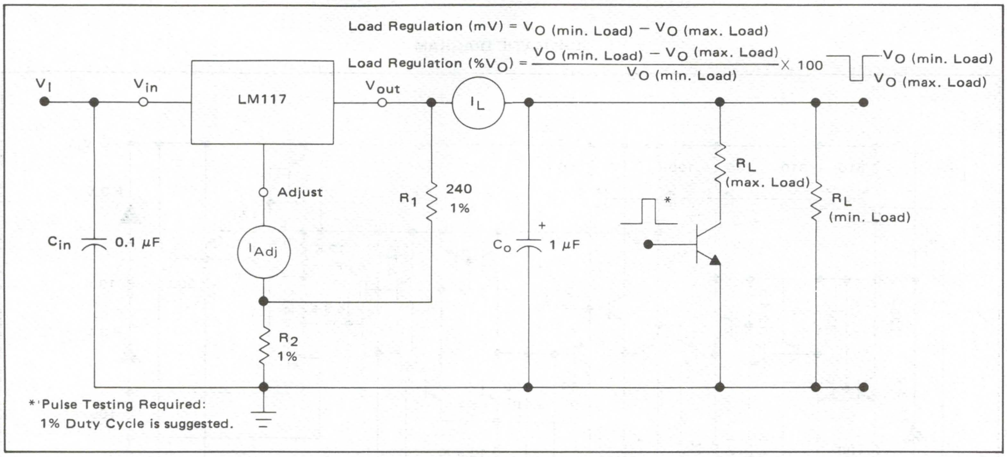

VCC
*
VIH
VIL
Vin
LM117
Vout
VOH
VOL
Line Regulation (%/V) = (VOH - VOL)/VOL × 100
Adjust
IAdj
R1
240
1%
Cin
0.1 µF
Co
+
1 µF
RL
R2
1%
* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT



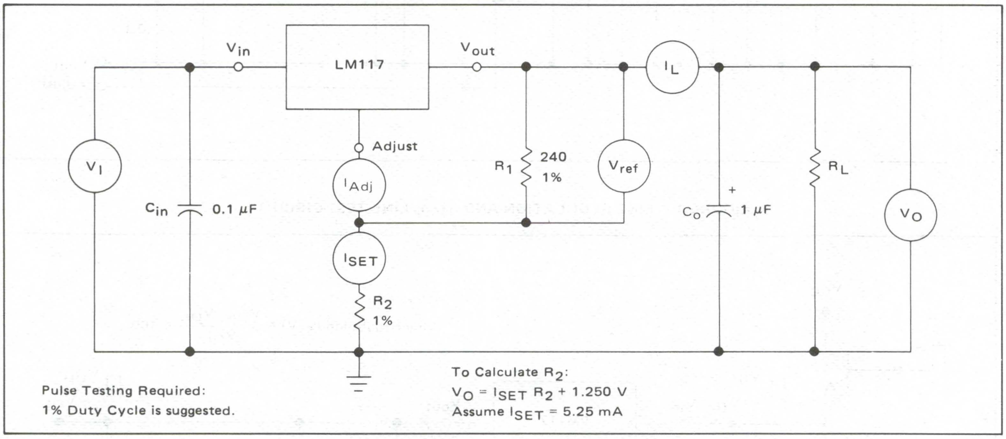
$$\text{Load Regulation (mV)} = V_O\,(\text{min. Load}) - V_O\,(\text{max. Load})$$

$$\text{Load Regulation } (\%V_O) = \frac{V_O\,(\text{min. Load}) - V_O\,(\text{max. Load})}{V_O\,(\text{min. Load})} \times 100$$

V_O (min. Load)
V_O (max. Load)
V_I
V_{in}
LM117
V_{out}
I_L
Adjust
R_1 240 1%
R_L (max. Load)
*
R_L (min. Load)
C_{in} 0.1 µF
I_{Adj}
C_O + 1 µF
R_2 1%

*Pulse Testing Required:
1% Duty Cycle is suggested.

FIGURE 3 – STANDARD TEST CIRCUIT

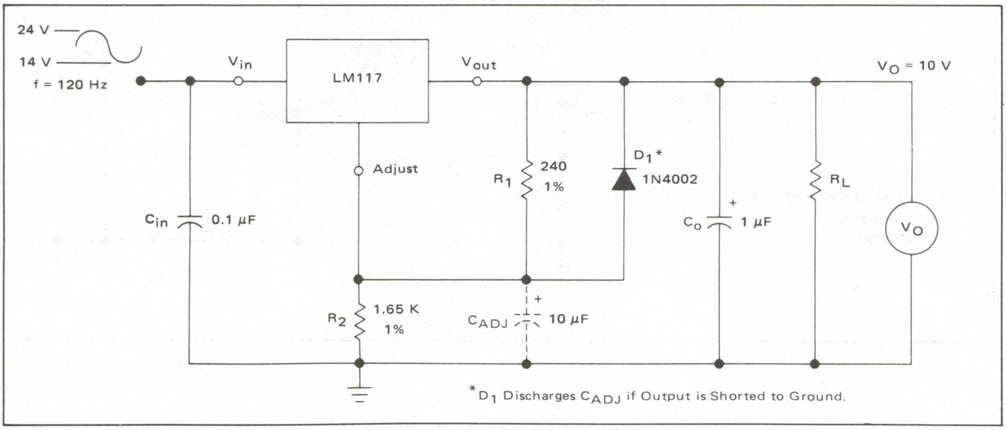


V_{in}
LM117
V_{out}
I_L
Adjust
V_I
I_{Adj}
R_1 240 1%
V_{ref}
R_L
C_{in} 0.1 µF
C_O + 1 µF
V_O
I_{SET}
R_2 1%

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT



24 V
14 V
f = 120 Hz
V_{in}
LM117
V_{out}
$V_O = 10$ V
Adjust
R_1 240 1%
D_1* 1N4002
R_L
C_{in} 0.1 µF
C_O + 1 µF
V_O
R_2 1.65 K 1%
C_{ADJ} + 10 µF

*D_1 Discharges C_{ADJ} if Output is Shorted to Ground.

FIGURE 5 — LOAD REGULATION

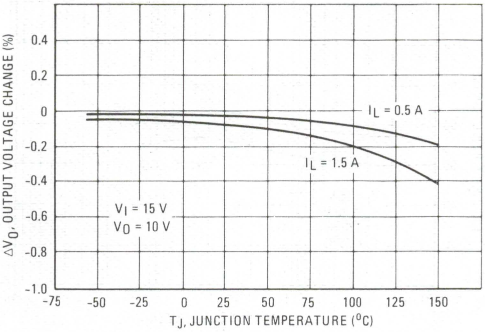


FIGURE 6 — CURRENT LIMIT

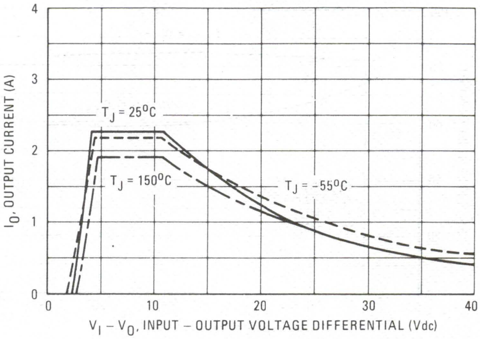


FIGURE 7 — ADJUSTMENT PIN CURRENT

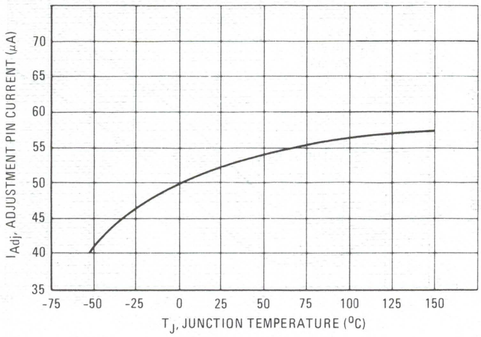


FIGURE 8 — DROPOUT VOLTAGE

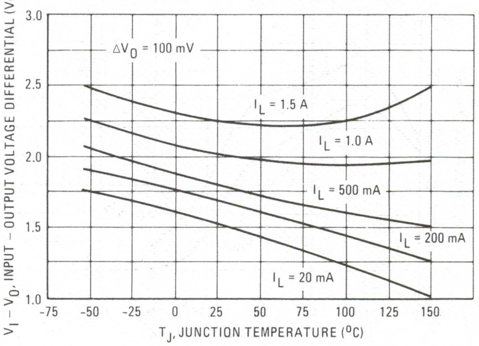


FIGURE 9 — TEMPERATURE STABILITY

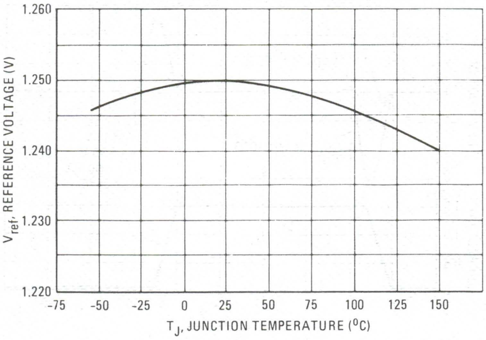


FIGURE 10 — MINIMUM OPERATING CURRENT

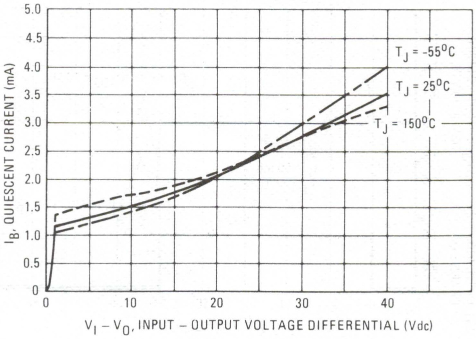


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

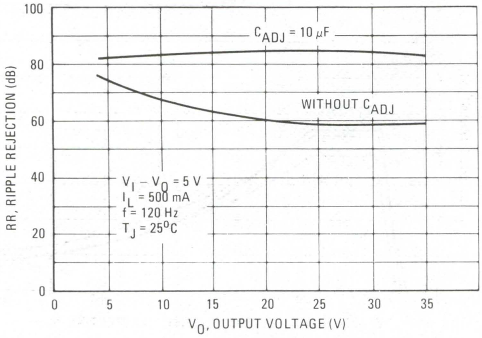


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

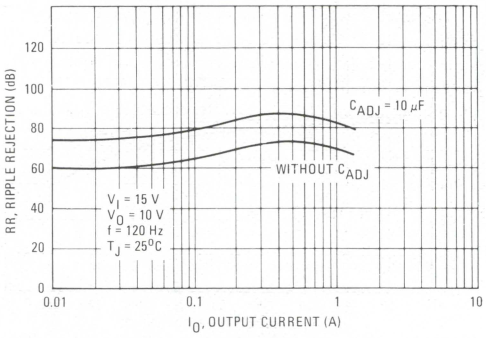


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

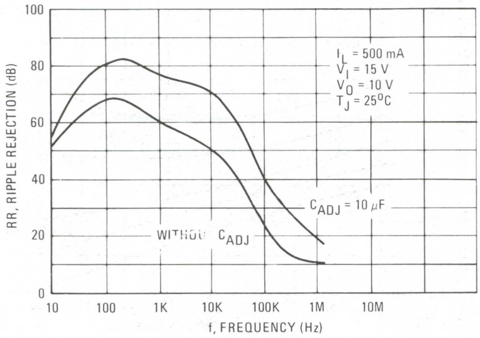


FIGURE 14 — OUTPUT IMPEDANCE

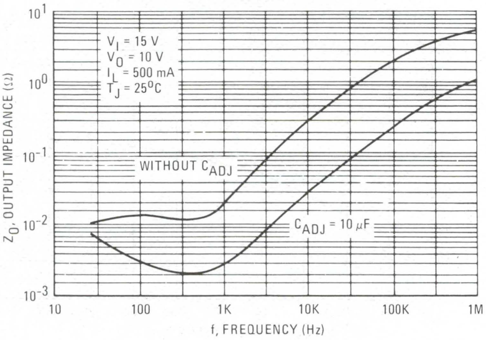


FIGURE 15 — LINE TRANSIENT RESPONSE

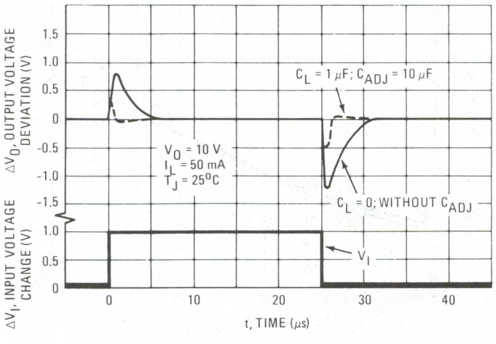
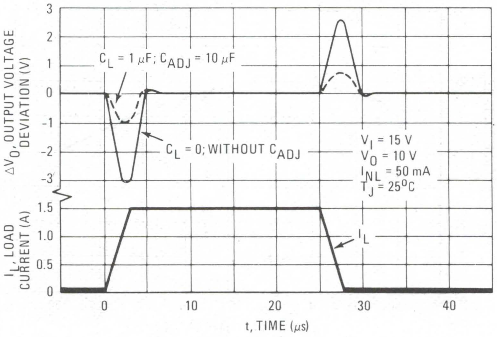


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

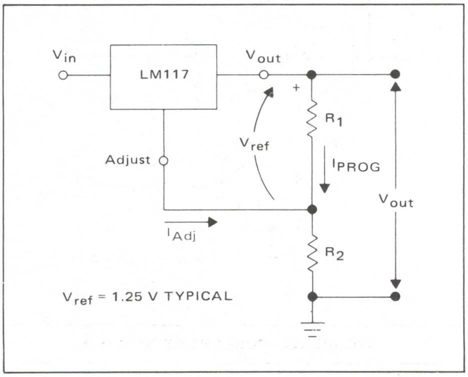
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_o) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25$ μF, $C_{ADJ} > 10$ μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

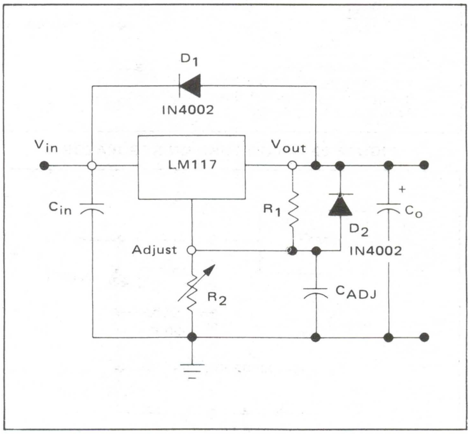
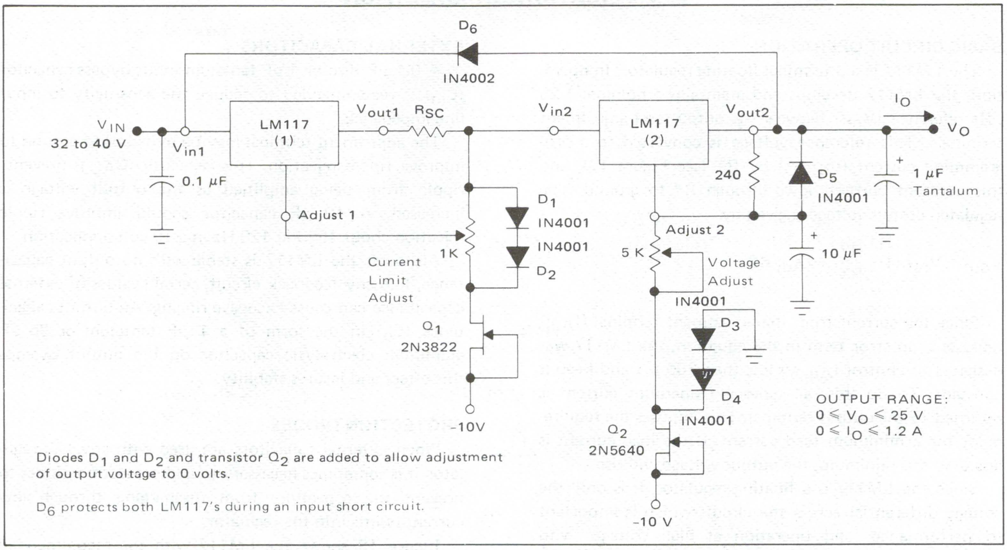


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

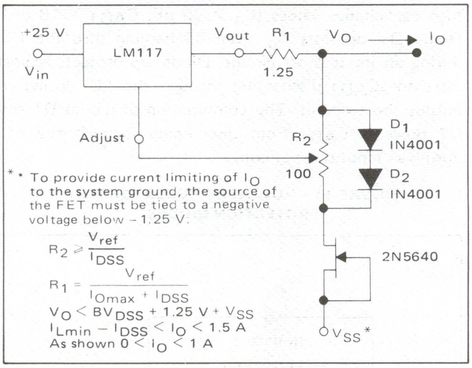

D6
IN4002
VIN
32 to 40 V
Vin1
0.1 μF
LM117
(1)
Vout1
RSC
Adjust 1
D1
IN4001
IN4001
D2
1K
Current
Limit
Adjust
Q1
2N3822
-10V
Vin2
LM117
(2)
Vout2
IO
VO
240
D5
IN4001
1 μF
Tantalum
Adjust 2
5 K
Voltage
Adjust
10 μF
IN4001
D3
D4
IN4001
Q2
2N5640
-10 V

OUTPUT RANGE:
$0 \leqslant V_O \leqslant 25$ V
$0 \leqslant I_O \leqslant 1.2$ A

Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 volts.

D_6 protects both LM117's during an input short circuit.

FIGURE 20 – ADJUSTABLE CURRENT LIMITER


+25 V
Vin
LM117
Vout
R1
1.25
VO
IO
Adjust
R2
100
D1
IN4001
D2
IN4001
2N5640
VSS *

* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below – 1.25 V.

$$R_2 \geqslant \frac{V_{ref}}{I_{DSS}}$$

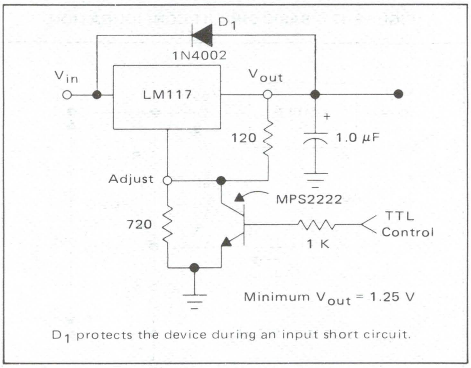
$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < BV_{DSS} + 1.25\text{ V} + V_{SS}$

$I_{Lmin} - I_{DSS} < I_O < 1.5$ A

As shown $0 < I_O < 1$ A

FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR


D1
1N4002
Vin
LM117
Vout
120
1.0 μF
Adjust
720
MPS2222
1 K
TTL
Control

Minimum $V_{out} = 1.25$ V

D_1 protects the device during an input short circuit.

FIGURE 22 – SLOW TURN-ON REGULATOR

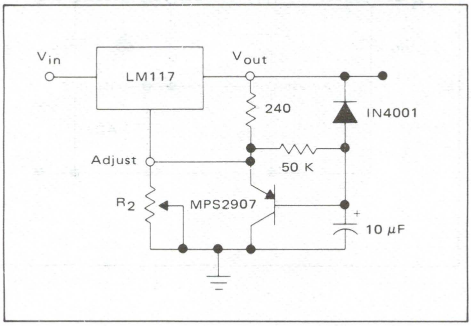
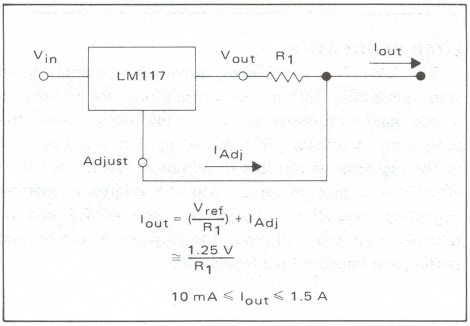

Vin
LM117
Vout
240
IN4001
Adjust
50 K
R2
MPS2907
10 μF

FIGURE 23 – CURRENT REGULATOR


Vin
LM117
Vout
R1
Iout
Adjust
IAdj

$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\text{ V}}{R_1}$$

$10\text{ mA} \leqslant I_{out} \leqslant 1.5$ A

MOTOROLA

LM117L
LM217L
LM317L

Specifications and Applications Information

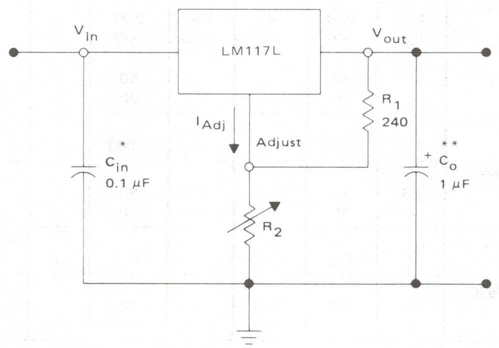
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

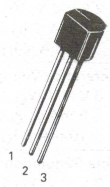
$$V_{out} = 1.25\ \text{V}\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications

LOW-CURRENT
3-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATOR

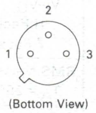
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Z SUFFIX
CASE 29-02
TO-226AA
(TO-92)
PLASTIC PACKAGE
(LM317 only)



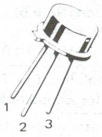
Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

H SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)



(Bottom View)

(Case is output)



Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

ORDERING INFORMATION

Device	Temperature Range	Package
LM117LH	$T_J = -55°C$ to $+150°C$	Metal Can
LM217LH	$T_J = -25°C$ to $+150°C$	Metal Can
LM317LH	$T_J = 0°C$ to $+125°C$	Metal Can
LM317LZ	$T_J = 0°C$ to $+125°C$	Plastic

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM117L LM217L LM317L	T_J	-55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_I - V_O = 5 V; I_O = 40 mA; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L			LM317L			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) T_A = 25°C, 3 V $\leqslant$ V_I-V_O $\leqslant$ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 5 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM117L/217L 10 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM317L V_O $\leqslant$ 5V V_O $\geqslant$ 5 V	2	Reg_{load}	— —	5 0.1	15 0.3	— —	5 0.1	25 0.5	mV % V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V $\leqslant$ V_I-V_O $\leqslant$ 40 V, P_D $\leqslant$ P_{max} 5 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM117L/217L 10 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM317L	1,2	ΔI_{Adj}	—	0.2	5	—	0.2	5	μA
Reference Voltage (Note 4) 3 V $\leqslant$ V_I-V_O $\leqslant$ 40 V, P_D $\leqslant$ P_{max} 5 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM117L/217L 10 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM317L	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3 V $\leqslant$ V_I-V_O $\leqslant$ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 5 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM117L/217L 10 mA $\leqslant$ I_O $\leqslant$ I_{max} — LM317L V_O $\leqslant$ 5 V V_O $\geqslant$ 5 V	2	Reg_{load}	— —	20 0.3	50 1	— —	20 0.3	70 1.5	mV %V_O
Temperature Stability (T_{low} $\leqslant$ T_J $\leqslant$ T_{high})	3	T_S	—	0.7	—	—	0.7	—	%V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	5	—	3.5	10	mA
Maximum Output Current V_I-V_O $\leqslant$ 20 V, P_D $\leqslant$ P_{max} H Package V_I-V_O $\leqslant$ 6.25 V, P_D $\leqslant$ P_{max}, Z Package V_I-V_O = 40 V, P_D $\leqslant$ P_{max}, T_A = 25°C H Package Z Package	3	I_{max}	100 100 — —	200 200 50 20	— — — —	100 1005 — —	200 200 50 20	— — — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz $\leqslant$ f $\leqslant$ 10 kHz	—	N	—	0.003	—	—	0.003	—	%V_O
Ripple Rejection (Note 5) V_O = 1.25 V, f = 120 Hz C_{ADJ} = 10 μF V_O = 10.0 V	4	RR	66 —	80 80	— —	60 —	80 80	— —	dB
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1	—	0.3	1	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package (TO-39) Z Package (TO-92)	—	$R_{\theta JC}$	— —	40 —	— —	— —	40 160	— —	°C/W

NOTES:

(1) T_{low} = -55°C for LM117L $\quad T_{high}$ = +150°C for LM117L
-25°C for LM217L $\quad$ = +150°C for LM217L
0°C for LM317L $\quad$ = +125°C for LM317L

(2) I_{max} = 100 mA
P_{max} = 2 W for H (TO-39) Package
= 625 mW for Z (TO-92) Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

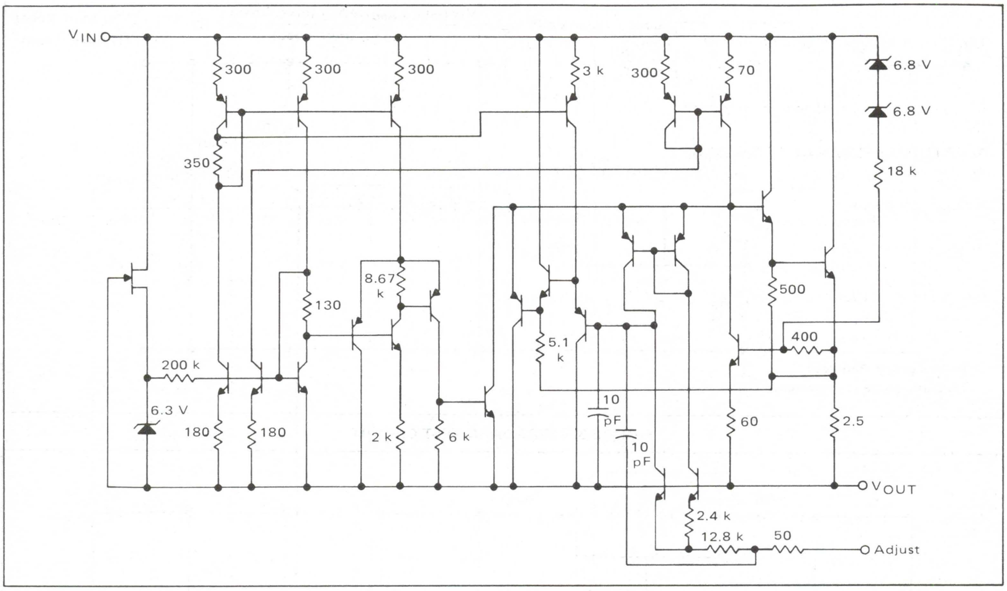
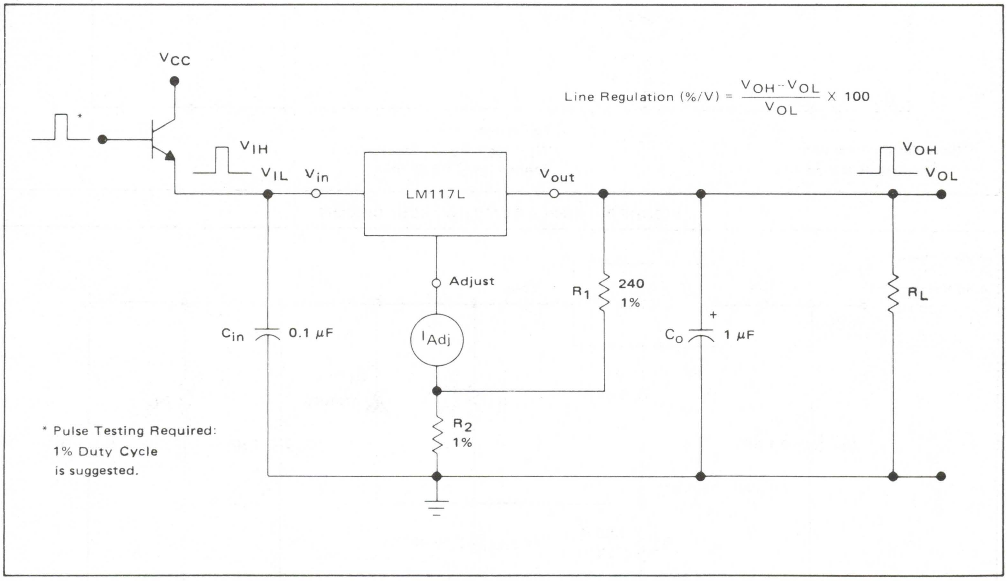

VIN
300
300
300
3 k
300
70
6.8 V
6.8 V
350
18 k
8.67 k
130
500
400
5.1 k
200 k
6.3 V
180
180
2 k
6 k
10 pF
10 pF
60
2.5
VOUT
2.4 k
12.8 k
50
Adjust

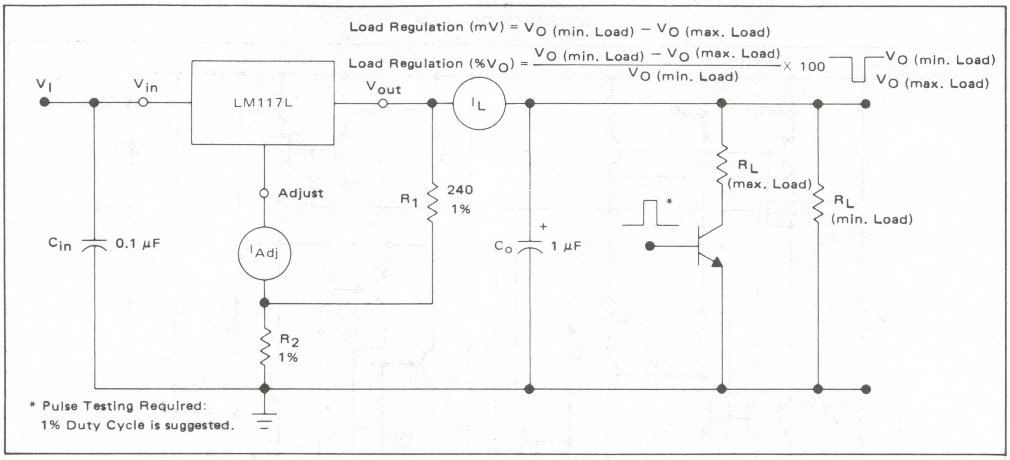
FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT


VCC
*
VIH
VIL
Vin
LM117L
Vout
VOH
VOL
Adjust
IAdj
R1
240
1%
Cin
0.1 μF
Co
+
1 μF
RL
R2
1%

$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

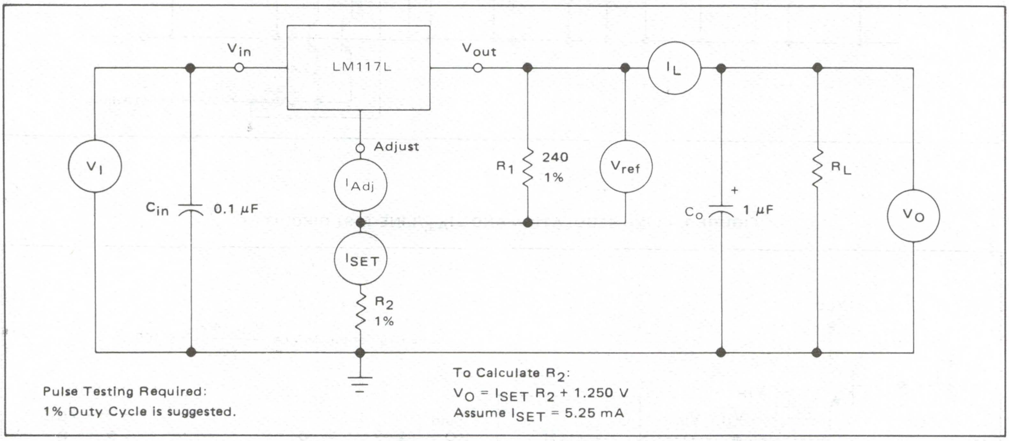

V_I
V_in
LM117L
V_out
I_L
Adjust
R_1
240
1%
C_in
0.1 μF
I_Adj
R_2
1%
C_O
1 μF
R_L (max. Load)
R_L (min. Load)
*
V_O (min. Load)
V_O (max. Load)

Load Regulation (mV) = V_O (min. Load) – V_O (max. Load)

$$\text{Load Regulation } (\%V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle is suggested.

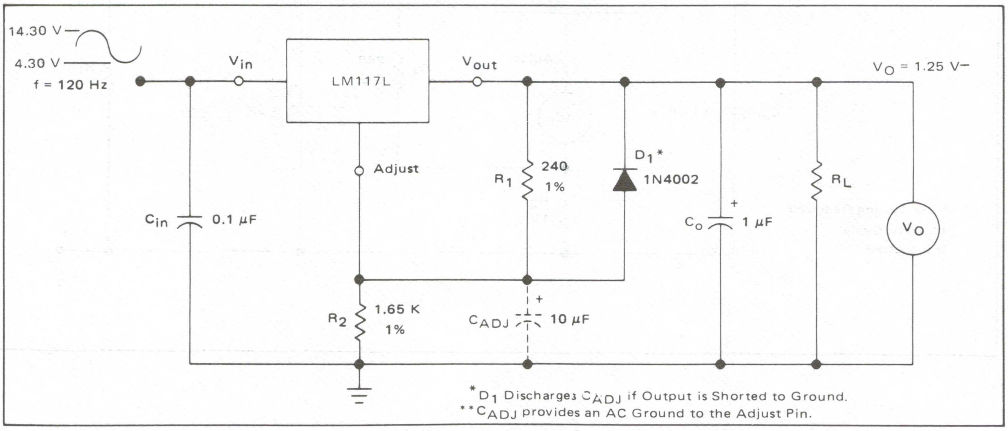
FIGURE 3 – STANDARD TEST CIRCUIT


V_in
LM117L
V_out
I_L
V_I
Adjust
I_Adj
R_1
240
1%
V_ref
C_in
0.1 μF
I_SET
R_2
1%
C_O
1 μF
R_L
V_O

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_O = I_{SET} R_2 + 1.250$ V
Assume I_{SET} = 5.25 mA

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


14.30 V
4.30 V
f = 120 Hz
V_in
LM117L
V_out
V_O = 1.25 V
Adjust
R_1
240
1%
D_1*
1N4002
R_L
C_in
0.1 μF
C_O
1 μF
V_O
R_2
1.65 K
1%
C_ADJ
10 μF

*D_1 Discharges C_{ADJ} if Output is Shorted to Ground.
**C_{ADJ} provides an AC Ground to the Adjust Pin.

FIGURE 5 — LOAD REGULATION

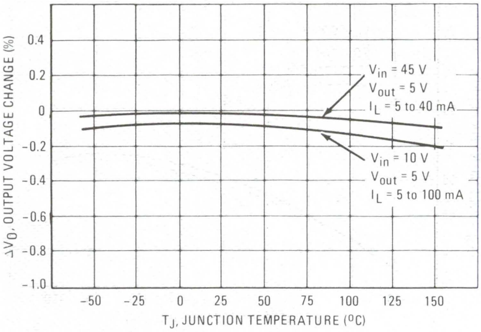


FIGURE 6 — RIPPLE REJECTION

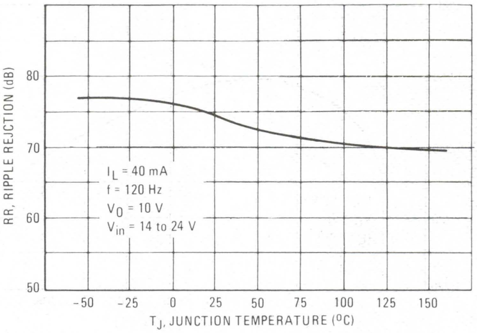


FIGURE 7 — CURRENT LIMIT

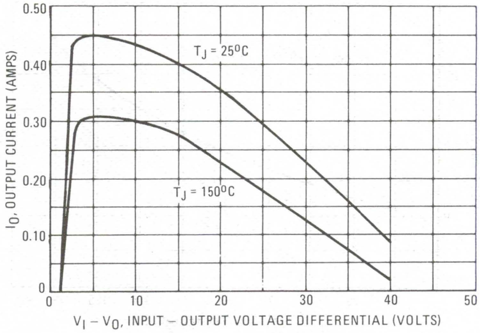


FIGURE 8 — DROPOUT VOLTAGE

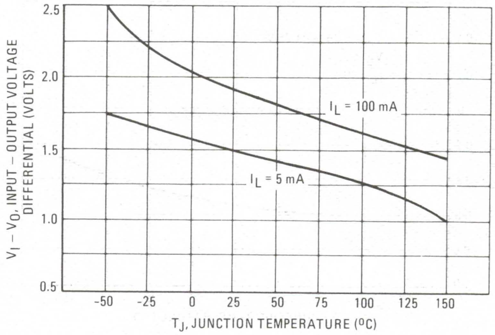


FIGURE 9 — MINIMUM OPERATING CURRENT

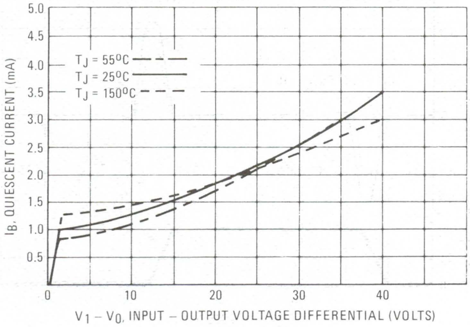
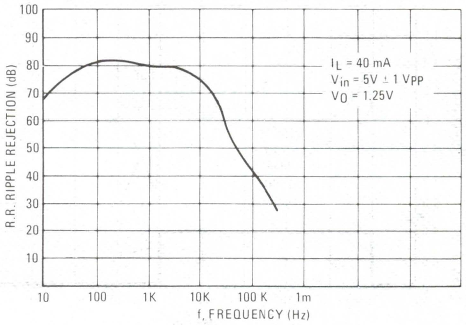


FIGURE 10 — RIPPLE REJECTION versus FREQUENCY



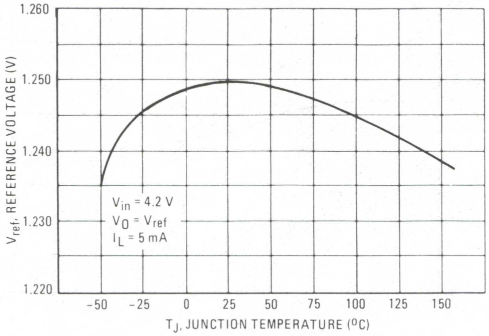


FIGURE 11 – TEMPERATURE STABILITY

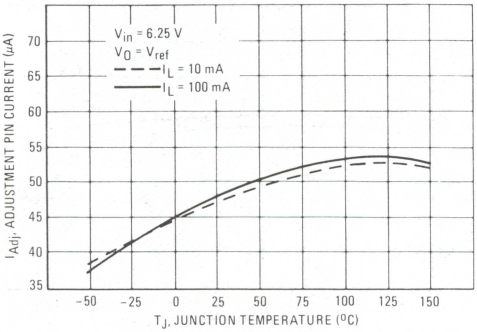


FIGURE 12 – ADJUSTMENT PIN CURRENT

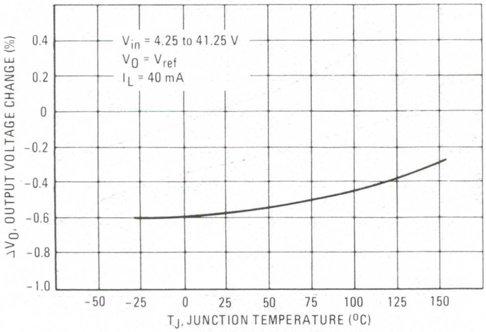


FIGURE 13 – LINE REGULATION

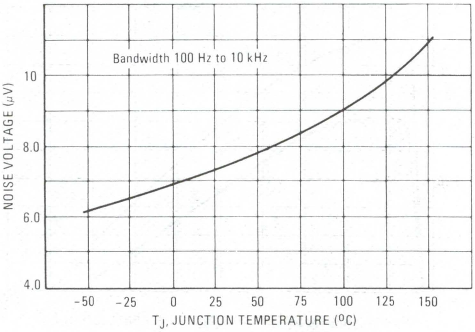


FIGURE 14 – OUTPUT NOISE

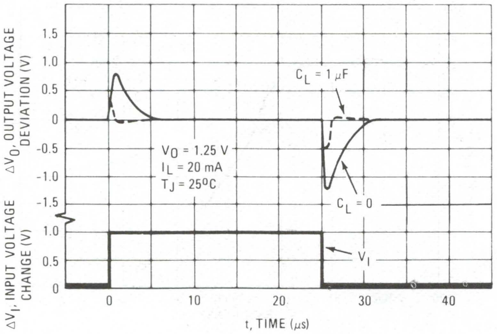


FIGURE 15 – LINE TRANSIENT RESPONSE

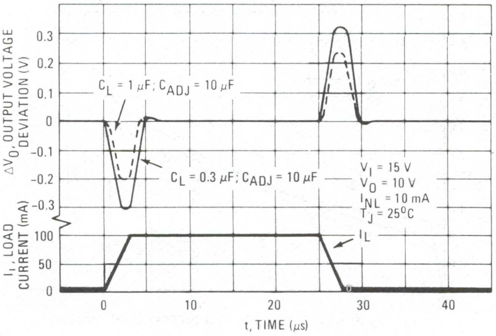


FIGURE 16 – LOAD TRANSIENT RESPONSE

APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

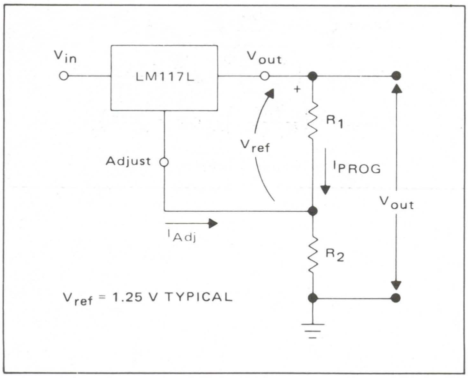
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1}\right) + I_{Adj}\, R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 µF disc or 1 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 10$ µF, $C_{ADJ} > 5$ µF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES

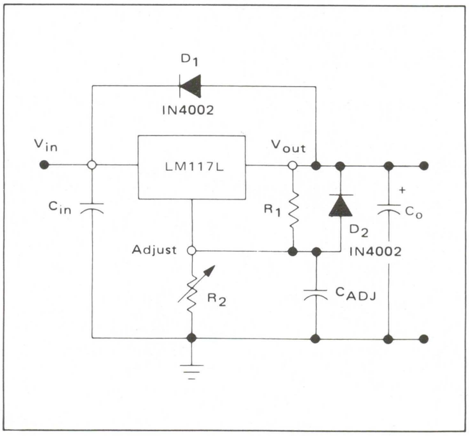
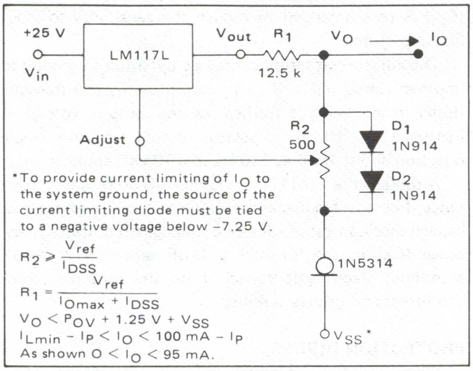


FIGURE 19 – ADJUSTABLE CURRENT LIMITER


+25 V
V_in
LM117L
V_out
R_1
12.5 k
V_O
I_O
Adjust
R_2
500
D_1
1N914
D_2
1N914
1N5314
V_SS*

*To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below −7.25 V.

$R_2 \geqslant \frac{V_{ref}}{I_{DSS}}$

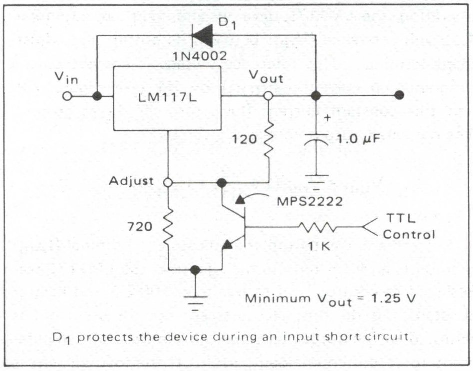
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < P_{OV} + 1.25\text{ V} + V_{SS}$

$I_{Lmin} - I_P < I_O < 100\text{ mA} - I_P$

As shown $0 < I_O < 95\text{ mA}$.

FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR


D_1
1N4002
V_in
LM117L
V_out
+
120
1.0 µF
Adjust
MPS2222
TTL
Control
720
1 K

Minimum $V_{out} = 1.25\text{ V}$

D_1 protects the device during an input short circuit.

FIGURE 21 – SLOW TURN-ON REGULATOR

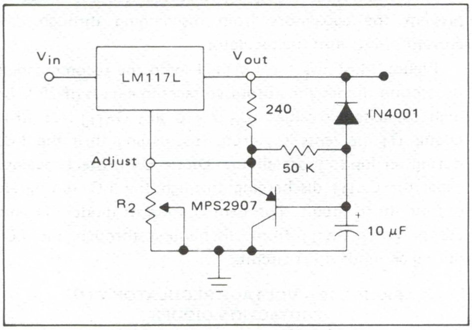
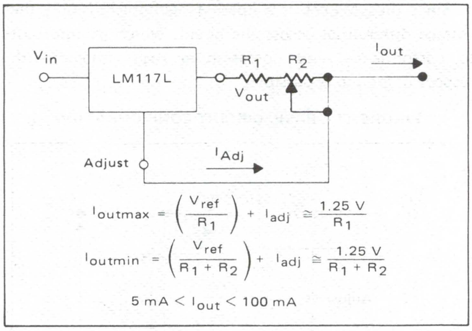

V_in
LM117L
V_out
240
1N4001
Adjust
50 K
R_2
MPS2907
+
10 µF

FIGURE 22 – CURRENT REGULATOR


V_in
LM117L
R_1
R_2
I_out
V_out
Adjust
I_Adj

$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{adj} \cong \frac{1.25\text{ V}}{R_1}$$

$$I_{outmin} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{adj} \cong \frac{1.25\text{ V}}{R_1 + R_2}$$

$5\text{ mA} < I_{out} < 100\text{ mA}$

MOTOROLA

LM117M
LM217M
LM317M

Specifications and Applications Information

MEDIUM-CURRENT 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

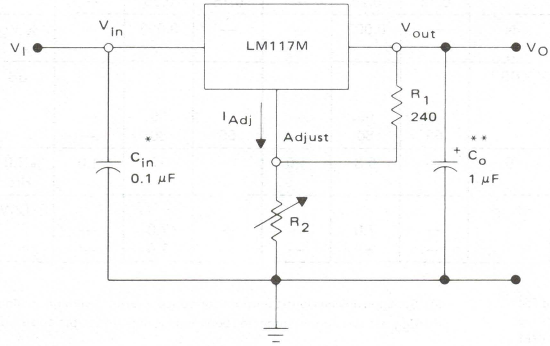
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117M/217M/317M are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117M series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117M series can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



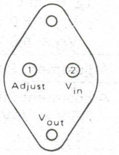
* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_o is not needed for stability, however it does improve transient response.

$$V_O = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{adj}\ R_2$$

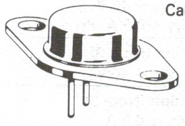
Since I_{adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications

R SUFFIX
METAL PACKAGE
CASE 80-02
TO-213AA
(TO-66)



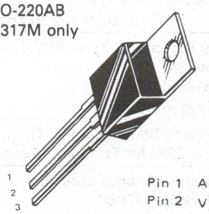
(Bottom View)

Case is output



Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB
LM317M only



Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

Heatsink surface connected to Pin 2

ORDERING INFORMATION

Device	Temperature Range	Package
LM117MR	T_J = -55°C to +150°C	Metal Power
LM217MR	T_J = -25°C to +150°C	Metal Power
LM317MR	T_J = 0°C to +125°C	Metal Power
LM317MT	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM117M LM217M LM317M	T_J	-55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_I-V_O = 5.0 V, I_O = 0.1 A, T_J = T_{low} to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

			LM117M/217M			LM317M			
Characteristic	Figure	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A	2	Reg_{load}							
V_O ≤ 5.0 V			—	5.0	15	—	5.0	25	mV
V_O ≥ 5.0 V			—	0.1	0.3	—	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	µA
Reference Voltage (Note 4) 3.0 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A	2	Reg_{load}							
V_O ≤ 5.0 V			—	20	50	—	20	70	mV
V_O ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current	3	I_{max}							A
V_I-V_O ≤ 15 V, P_D ≤ P_{max}			0.5	0.9	—	0.5	0.9	—	
V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C			0.15	0.25	—	0.15	0.25	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{Adj}			—	65	—	—	65	—	
C_{Adj} = 10 µF			66	80	—	66	80	—	
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
R Package (TO-66)			—	7.0	—	—	7.0	—	
T Package (TO-220)			—	—	—	—	7.0	—	

NOTES:

(1) T_{low} = -55°C for LM117M
= -25°C for LM217M
= 0°C for LM317M

T_{high} = +150°C for LM117M
= +150°C for LM217M
= +125°C for LM317M

(2) P_{max} = 7.5 W

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

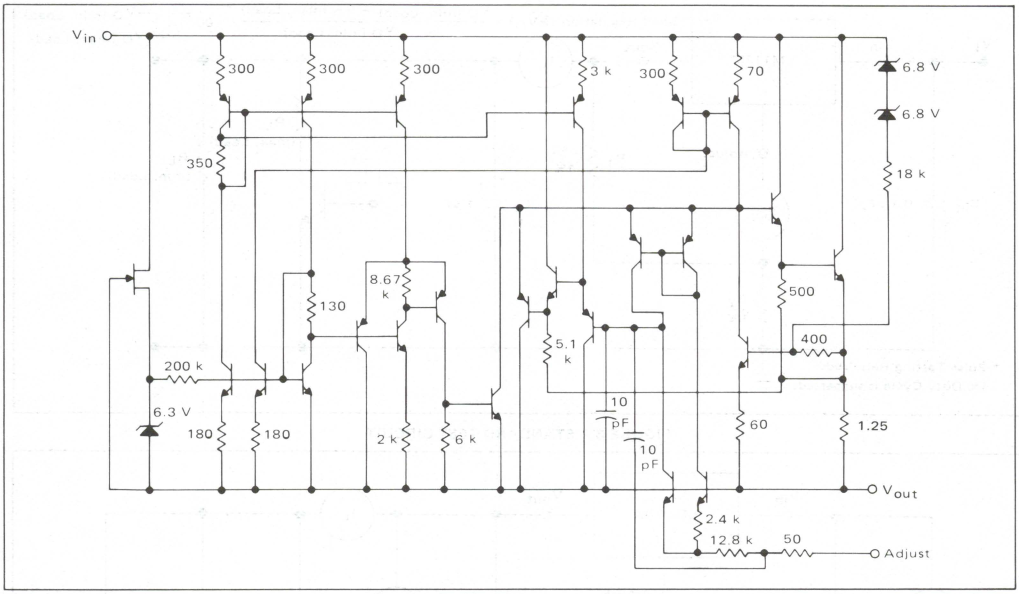

V_{in}
300
300
300
3 k
300
70
6.8 V
6.8 V
350
18 k
8.67 k
130
500
5.1 k
400
200 k
6.3 V
180
180
2 k
6 k
10 pF
10 pF
60
1.25
V_{out}
2.4 k
12.8 k
50
Adjust

FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

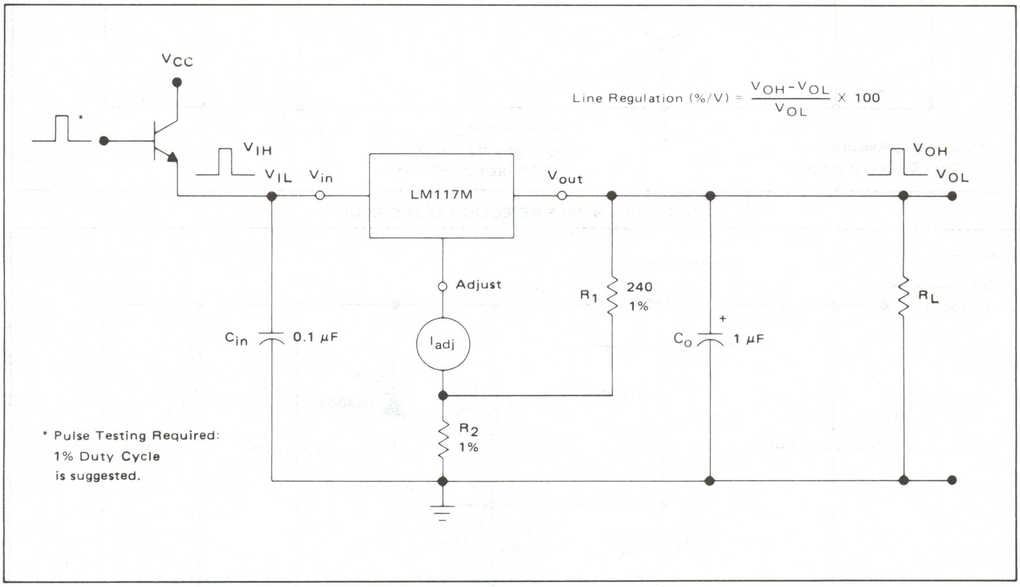
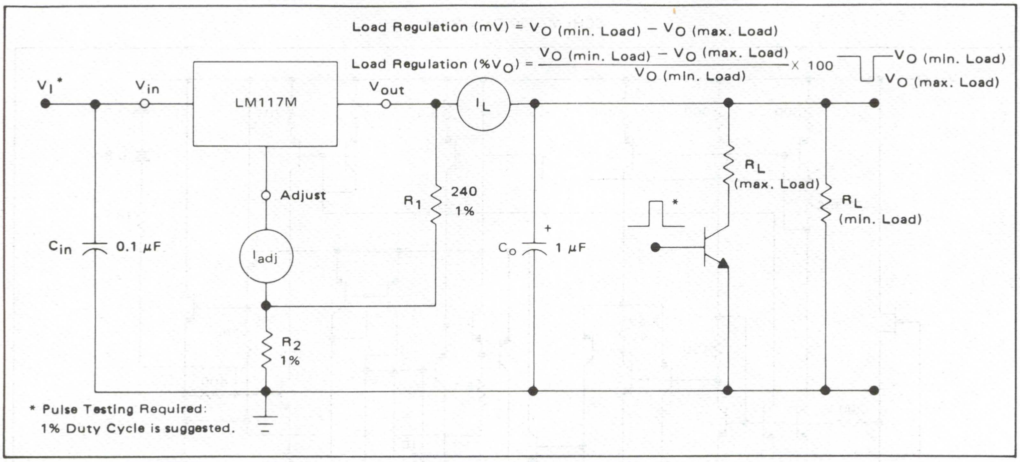

V_{CC}
*
V_{IH}
V_{IL}
V_{in}
LM117M
V_{out}
Line Regulation (%/V) = $\frac{V_{OH}-V_{OL}}{V_{OL}} \times 100$
V_{OH}
V_{OL}
Adjust
I_{adj}
R_1
240
1%
C_{in}
0.1 µF
C_O
+
1 µF
R_L
R_2
1%
* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

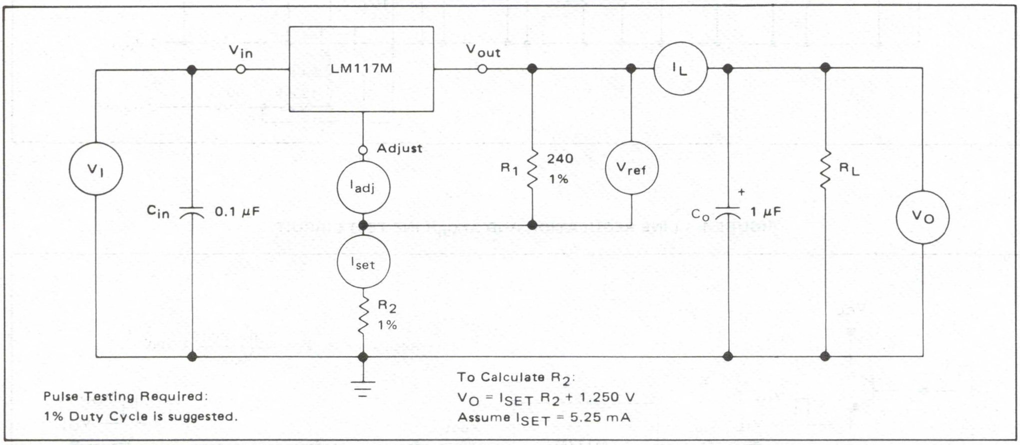

Load Regulation (mV) = V_O (min. Load) – V_O (max. Load)

Load Regulation (%V_O) = $\frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$

* Pulse Testing Required:
1% Duty Cycle is suggested.

V_O (min. Load)
V_O (max. Load)
V_I*
V_{in}
LM117M
V_{out}
I_L
Adjust
R_1
240
1%
R_L
(max. Load)
R_L
(min. Load)
*
C_{in}
0.1 μF
I_{adj}
C_O
1 μF
+
R_2
1%

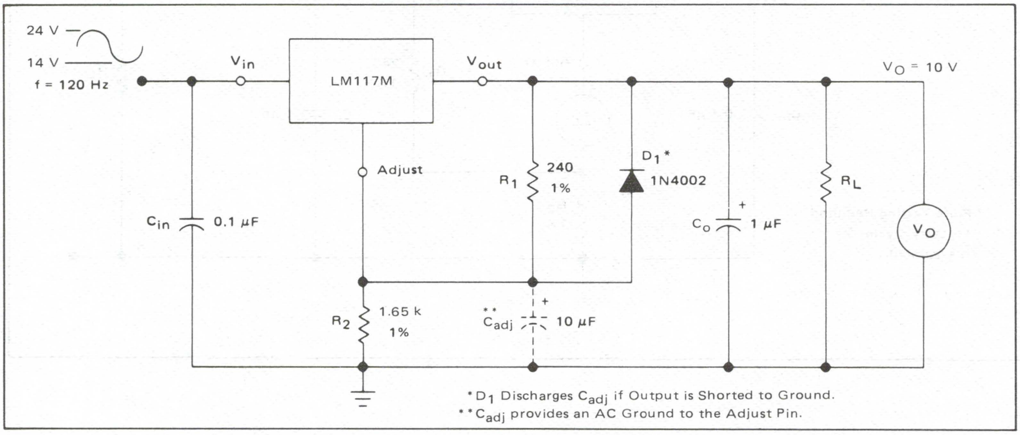
FIGURE 3 – STANDARD TEST CIRCUIT


Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_O = I_{SET} R_2 + 1.250$ V
Assume I_{SET} = 5.25 mA

V_{in}
LM117M
V_{out}
I_L
V_I
Adjust
I_{adj}
R_1
240
1%
V_{ref}
R_L
C_{in}
0.1 μF
C_O
1 μF
+
V_O
I_{set}
R_2
1%

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


*D_1 Discharges C_{adj} if Output is Shorted to Ground.
**C_{adj} provides an AC Ground to the Adjust Pin.

24 V
14 V
f = 120 Hz
V_{in}
LM117M
V_{out}
V_O = 10 V
Adjust
R_1
240
1%
D_1*
1N4002
R_L
C_{in}
0.1 μF
C_O
1 μF
+
V_O
R_2
1.65 k
1%
**
C_{adj}
10 μF
+

FIGURE 5 – LOAD REGULATION

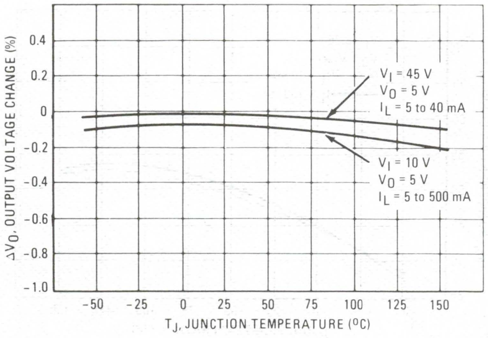


FIGURE 6 – RIPPLE REJECTION

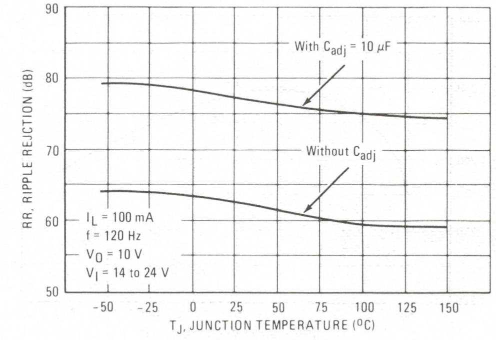


FIGURE 7 – CURRENT LIMIT

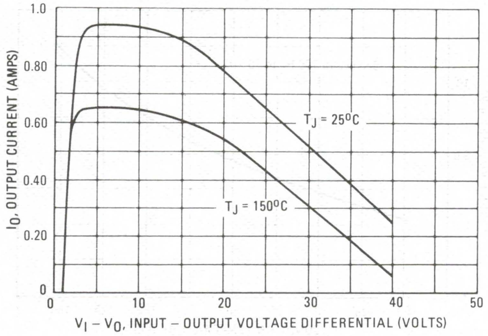


FIGURE 8 – DROPOUT VOLTAGE

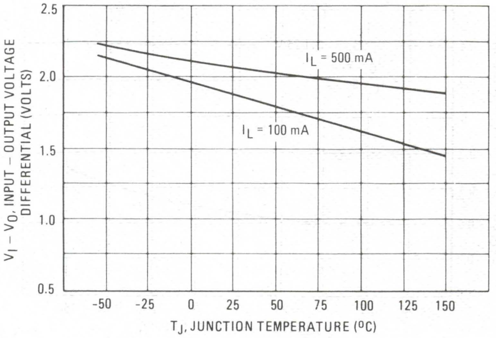


FIGURE 9 – MINIMUM OPERATING CURRENT

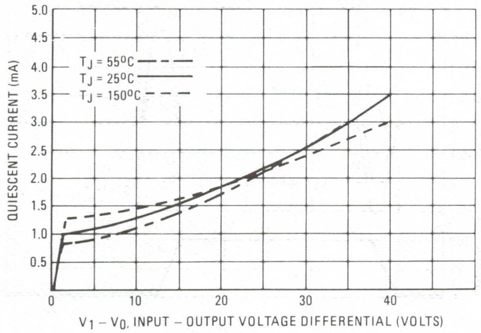


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

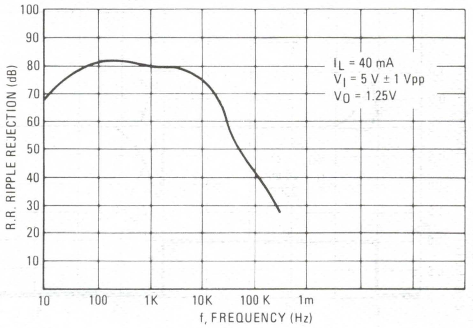


FIGURE 11 – TEMPERATURE STABILITY

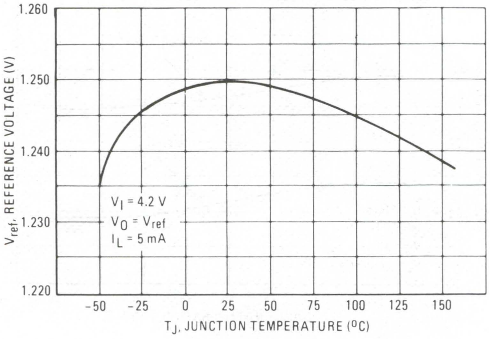


FIGURE 12 – ADJUSTMENT PIN CURRENT

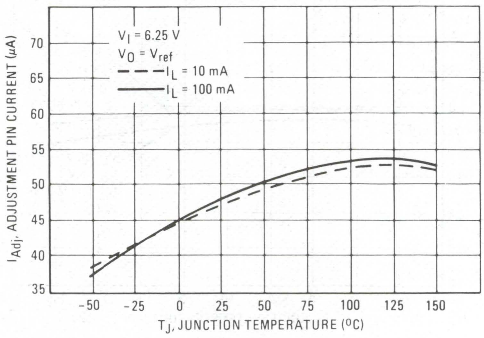


FIGURE 13 – LINE REGULATION

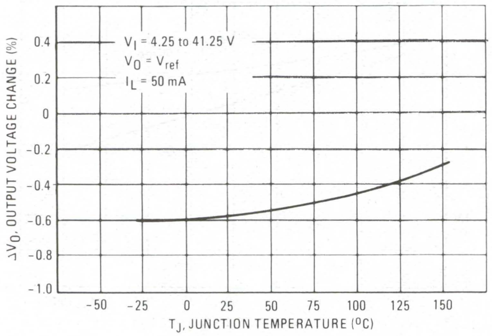


FIGURE 14 – OUTPUT NOISE

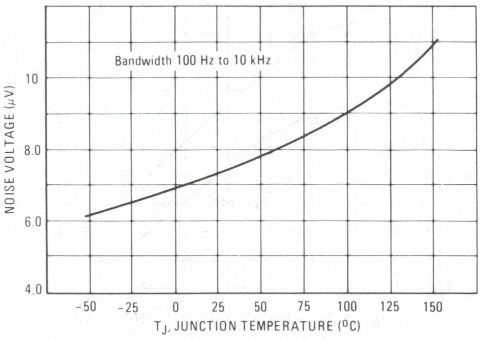


FIGURE 15 – LINE TRANSIENT RESPONSE

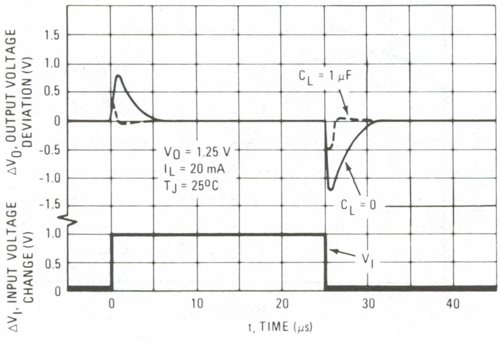
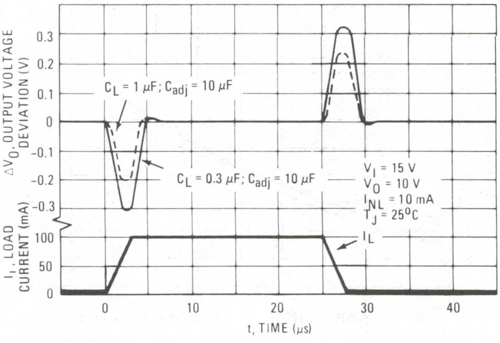


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

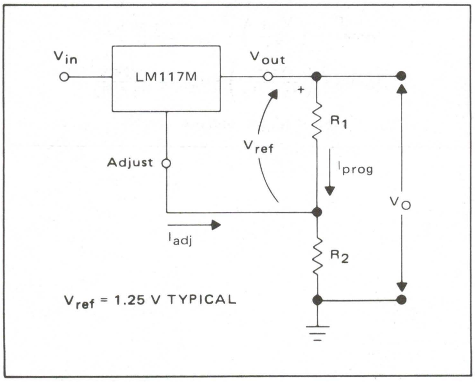
The LM117M is a 3-terminal floating regulator. In operation, the LM117M develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{prog}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{ref} (1 + \frac{R2}{R1}) + I_{adj}R2$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in the equation, the LM117M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

Although the LM117M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 10$ μF, $C_{adj} > 5$ μF). Diode D1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

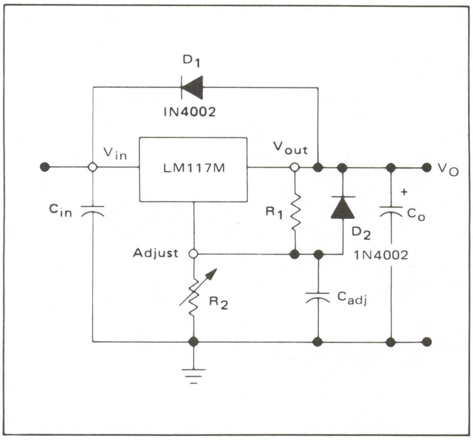
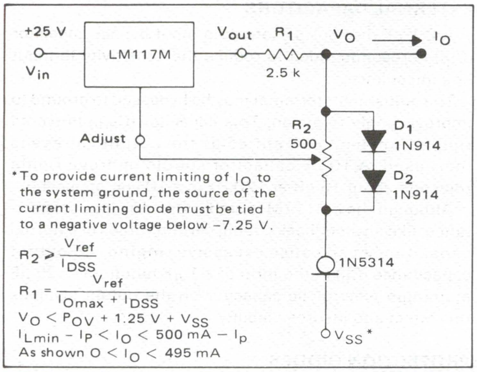


FIGURE 19 – ADJUSTABLE CURRENT LIMITER


+25 V
Vin
LM117M
Vout
R1
2.5 k
VO
IO
R2
500
D1
1N914
D2
1N914
Adjust
1N5314
VSS *

*To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below −7.25 V.

$R_2 \geqslant \frac{V_{ref}}{I_{DSS}}$

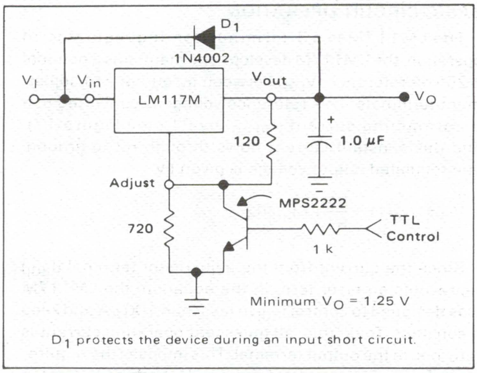
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < P_{OV} + 1.25\ V + V_{SS}$

$I_{Lmin} - I_P < I_O < 500\ mA - I_P$

As shown $0 < I_O < 495\ mA$

FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR


D1
1N4002
VI
Vin
LM117M
Vout
VO
+
120
1.0 µF
Adjust
MPS2222
720
TTL
Control
1 k
Minimum VO = 1.25 V

D_1 protects the device during an input short circuit.

FIGURE 21 – SLOW TURN-ON REGULATOR

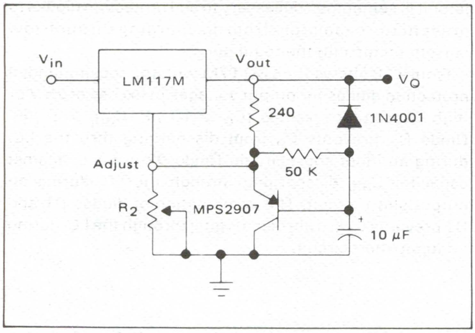
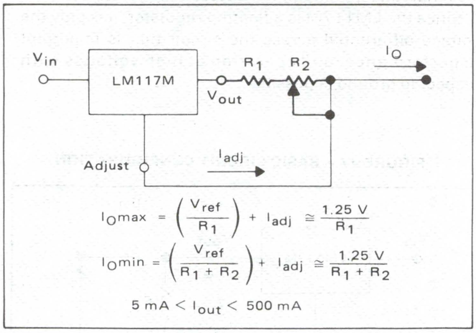

Vin
LM117M
Vout
VO
240
1N4001
Adjust
50 K
R2
MPS2907
+
10 µF

FIGURE 22 – CURRENT REGULATOR


Vin
LM117M
R1
R2
IO
Vout
Adjust
Iadj

$$I_{Omax} = \left(\frac{V_{ref}}{R_1}\right) + I_{adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{Omin} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5\ mA < I_{out} < 500\ mA$

MOTOROLA

LM123, LM123A
LM223, LM223A
LM323, LM323A

Specifications and Applications Information

3 AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATOR

The LM123, A/LM223, A/LM323, A are a family of monolithic integrated circuits which supply a fixed positive 5.0 volt output with a load driving capability in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. An improved series with superior electrical characteristics and a 2% output voltage tolerance is available as A-suffix (LM123A/LM223A/LM323A) device types.

These regulators are offered in a hermetic TO-3 metal power package in three operating temperature ranges. A 0°C to +125°C temperature range version is also available in a low cost TO-220 plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series pass transistor to supply up to 15 amperes at 5.0 volts.

- Output Current in Excess of 3.0 Amperes
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM123, A	T_J	-55 to +150	°C
LM223, A		-25 to +150	
LM323, A		0 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_{solder}	300	°C

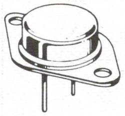
ORDERING INFORMATION

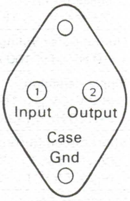
Device	Output Voltage Tolerance	Junction Temperature Range	Package
LM123K	6%	-55 to +150°C	Metal Power
LM123AK	2%		
LM223K	6%	-25 to +150°C	
LM223AK	2%		
LM323K	4%	0 to +125°C	
LM323AK	2%		
LM323T	4%		Plastic Power
LM323AT	2%		

3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



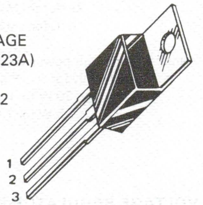


(Bottom View)

Pin 1. INPUT
2. OUTPUT
CASE GROUND

T SUFFIX
PLASTIC PACKAGE
(LM323 and LM323A)

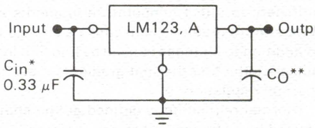
CASE 221A-02
TO-220AB



Pin 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	LM123A/LM223A/LM323A			LM123/LM223			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.7	5.0	5.3	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max} [Note 2])	V_O	4.8	5.0	5.2	4.6	5.0	5.4	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	—	1.0	15	—	1.0	25	—	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	—	10	50	—	10	100	—	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	—	0.002	0.03	%V_O/W
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	—	3.5	10	—	3.5	20	—	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	—	40	—	—	40	—	—	40	—	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0 A, f = 120 Hz, T_J = 25°C)	RR	66	75	—	62	75	—	62	75	—	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C) (V_{in} = 7.5 V, T_J = 25°C)	I_{SC}	 — —	 4.5 5.5	 — —	 — —	 4.5 5.5	 — —	 — —	 4.5 5.5	 — —	A
Long Term Stability	S	—	—	35	—	—	35	—	—	35	mV
Thermal Resistance Junction to Case (Note 4)	$R_{\theta JC}$	—	2.0	—	—	2.0	—	—	2.0	—	°C/W

Note 1. T_{low} = −55°C for LM123, A T_{high} = +150°C for LM123, A
= −25°C for LM223, A = +150°C for LM223, A
= 0°C for LM323, A = +125°C for LM323, A

Note 2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max}
P_{max} = 30 W for K (TO-3) package
P_{max} = 25 W for T (TO-220) package

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.

Note 4. Without a heat sink, the thermal resistance ($R_{\theta JA}$) is 35°C/W for the TO-3, and 65°C/W for the TO-220 packages. With a heat sink, the effective thermal resistance can approach the specified values of 2.0 °C/W, depending on the efficiency of the heat sink.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM123A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM123A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

SCHEMATIC DIAGRAM

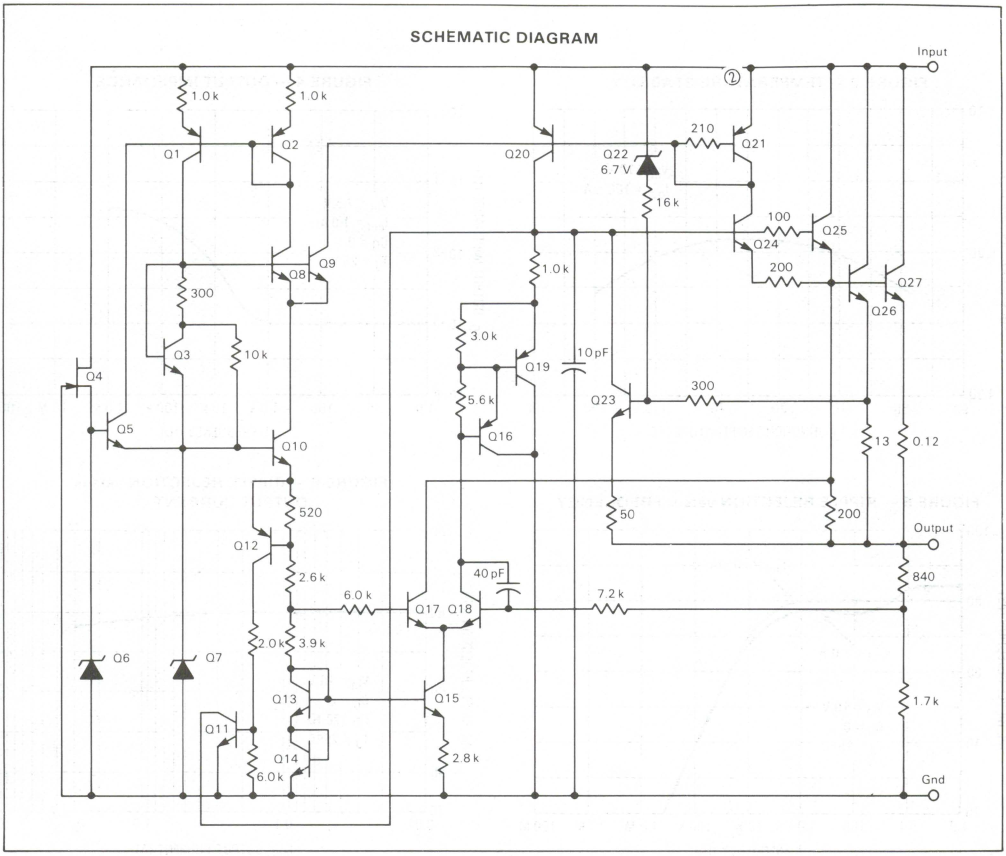
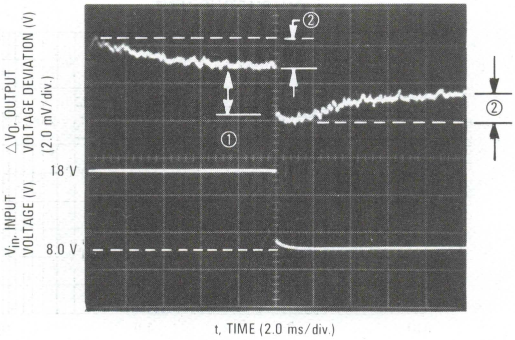
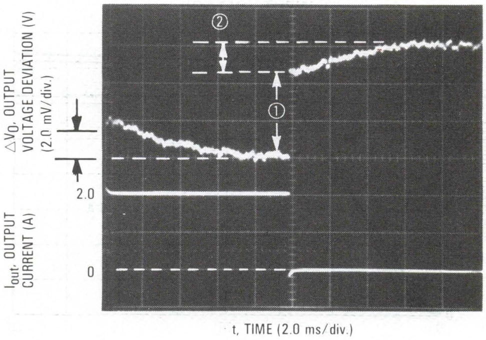

Input
②
1.0 k
1.0 k
Q1
Q2
Q20
Q22
6.7 V
210
Q21
16 k
100
Q25
Q24
200
Q27
Q26
Q9
Q8
300
1.0 k
3.0 k
Q3
10 k
Q19
10 pF
Q4
300
Q23
5.6 k
Q5
Q16
13
0.12
Q10
520
50
200
Output
Q12
40 pF
840
2.6 k
6.0 k
7.2 k
Q17
Q18
2.0 k
3.9 k
Q6
Q7
Q13
Q15
1.7 k
Q11
Q14
2.8 k
6.0 k
Gnd

FIGURE 1 — LINE AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V ① = Reg_{line} = 2.4 mV
I_{out} = 2.0 A ② = Reg_{therm} = 0.0015%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 15 ① = Reg_{load} = 4.4 mV
I_{out} = 0 A → 2.0 A → 0 A ② = Reg_{therm} = 0.0015%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

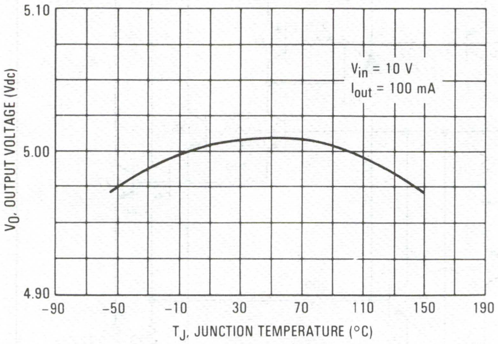


FIGURE 4 — OUTPUT IMPEDANCE

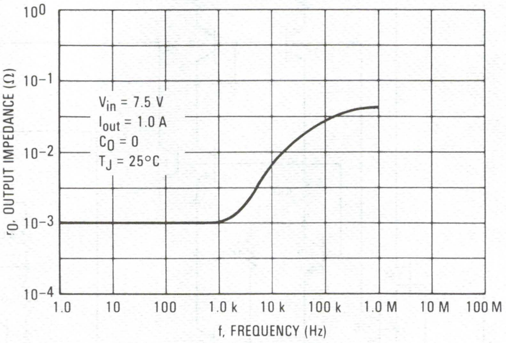


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

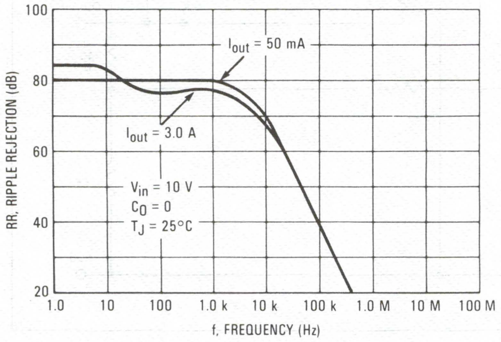


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

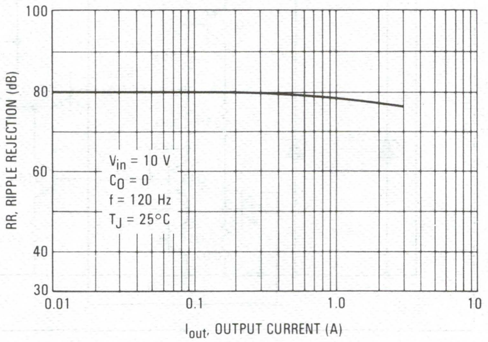


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

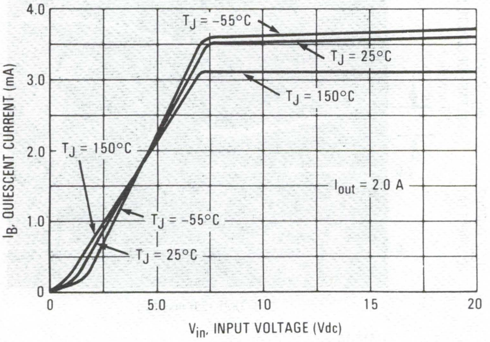


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

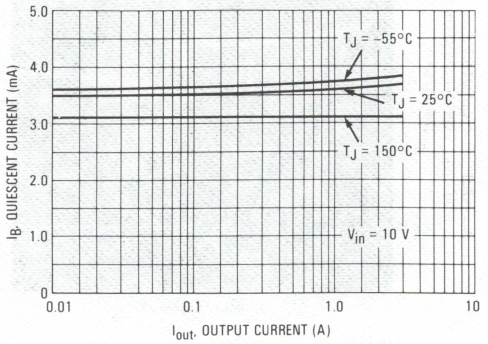


FIGURE 9 — DROPOUT VOLTAGE

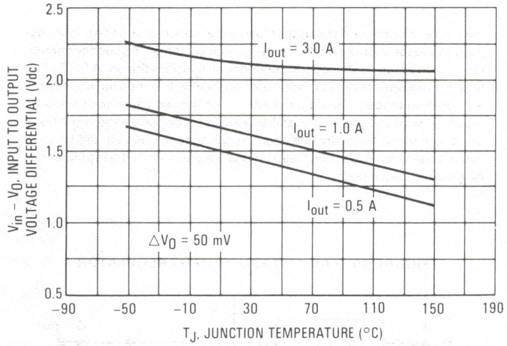


FIGURE 10 — SHORT CIRCUIT CURRENT

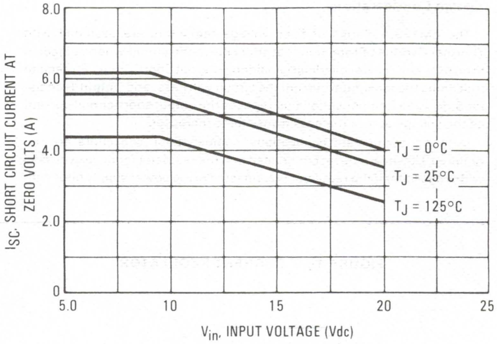


FIGURE 11 — LINE TRANSIENT RESPONSE

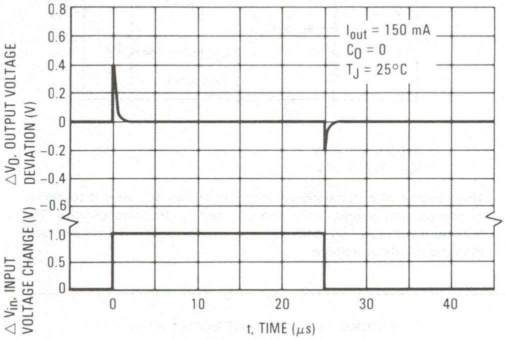


FIGURE 12 — LOAD TRANSIENT RESPONSE

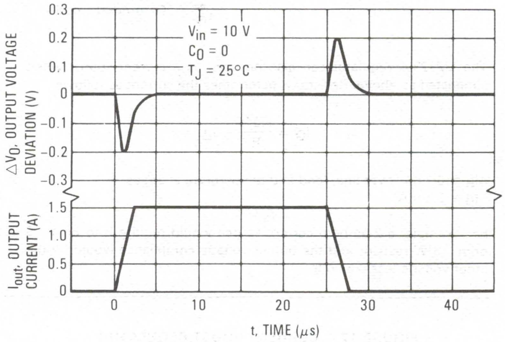


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM123K and LM223K

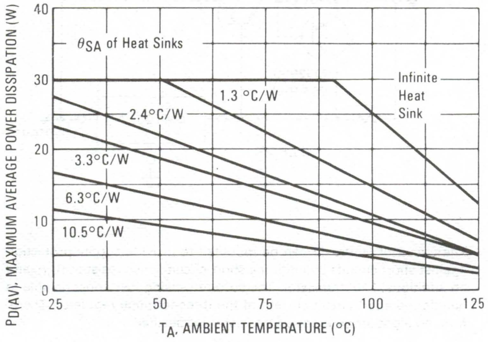
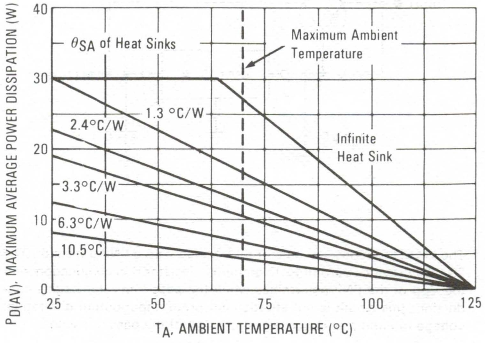


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM323K



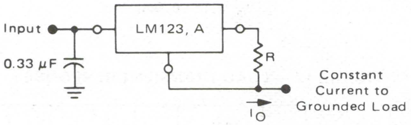
APPLICATIONS INFORMATION

Design Considerations

The LM123,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



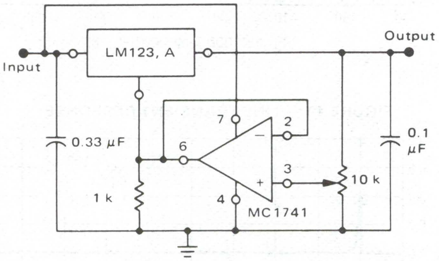
The LM123,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

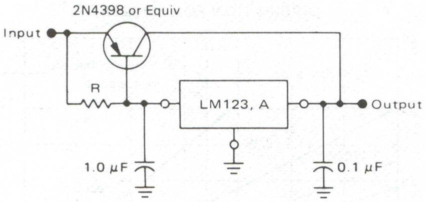
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in} - V_O \geqslant 2.5$ V

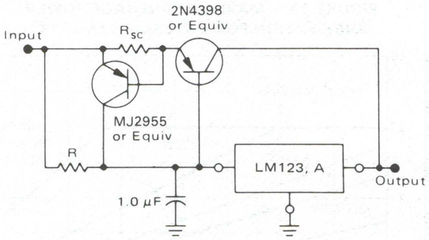
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM123,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

MOTOROLA

LM137
LM237
LM337

Specifications and Applications Information

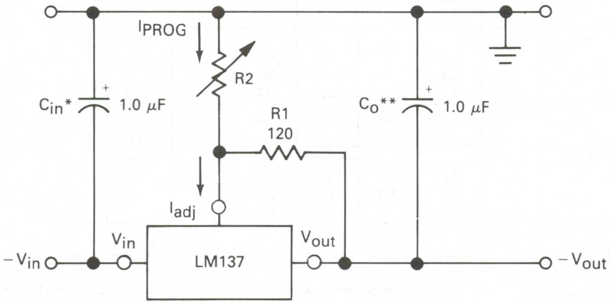
3-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

The LM137/237/337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137 series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting, Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

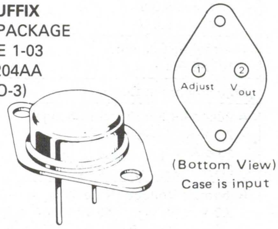
**C_O is necessary for stability. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

3-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

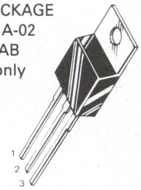
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB
LM337 only

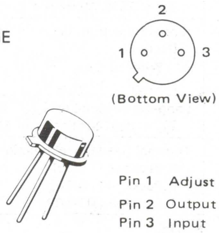


Pin 1 Adjust
Pin 2 V_{in}
Pin 3 V_{out}

Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)

(Case is input)



Pin 1 Adjust
Pin 2 Output
Pin 3 Input

ORDERING INFORMATION

Device	Temperature Range	Package
LM137H	T_J = −55°C to +150°C	Metal Can
LM137K	T_J = −55°C to +150°C	Metal Power
LM237H	T_J = −25°C to +150°C	Metal Can
LM237K	T_J = −25°C to +150°C	Metal Power
LM337H	T_J = 0°C to +125°C	Metal Can
LM337K	T_J = 0°C to +125°C	Metal Power
LM337T	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM137 LM237 LM337	T_J	−55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(|$V_I - V_O$| = 5 V, I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; $T_J = T_{low}$ to T_{high} [see Note 1], I_{max} and P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	LM137/237 Min	LM137/237 Typ	LM137/237 Max	LM337 Min	LM337 Typ	LM337 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ |V_I-V_O| ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
|V_O| ≤ 5.0 V			—	15	25	—	15	50	mV
|V_O| ≥ 5.0 V			—	0.3	0.5	—	0.3	1.0	% V_O
Thermal Regulation 10 mS Pulse, T_A = 25°C	—	Reg_{therm}	—	0.002	0.02	—	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	65	100	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ |V_I-V_O| ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = 25°C	1,2	ΔI_{Adj}	—	2.0	5.0	—	2.0	5.0	μA
Reference Voltage (Note 4) T_A = +25°C	3	V_{ref}	−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
3.0 V ≤ |V_I-V_O| ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, T_J = T_{low} to T_{high}			−1.20	−1.25	−1.30	−1.20	−1.25	−1.30	
Line Regulation (Note 3) 3.0 V ≤ |V_I-V_O| ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
|V_O| ≤ 5.0 V			—	20	50	—	20	70	mV
|V_O| ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	—	0.6	—	% V_O
Minimum Load Current to	3	I_{Lmin}							mA
Maintain Regulation (|V_I-V_O| ≤ 10 V)			—	1.2	3.0	—	1.5	6.0	
(|V_I-V_O| ≤ 40 V)			—	2.5	5.0	—	2.5	10	
Maximum Output Current |V_I-V_O| ≤ 15 V, P_D ≤ P_{max}	3	I_{max}							A
K and T Packages			1.5	2.2	—	1.5	2.2	—	
H Package			0.5	0.8	—	0.5	0.8	—	
|V_I-V_O| = 40 V, P_D ≤ P_{max}, T_J = 25°C									
K and T Packages			0.24	0.4	—	0.15	0.4	—	
H Package			0.15	0.20	—	0.10	0.20	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{Adj}			—	60	—	—	60	—	
C_{Adj} = 10 μF			66	77	—	66	77	—	
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
H Package (TO-39)			—	12	15	—	12	15	
K Package (TO-3)			—	2.3	3.0	—	2.3	3.0	
T Package (TO-220)			—	—	—	—	4.0	—	

NOTES:

(1) T_{low} = −55°C for LM137 T_{high} = +150°C for LM137
= −25°C for LM237 = +150°C for LM237
= 0°C for LM337 = +125°C for LM337

(2) I_{max} = 1.5 A for K (TO-3) and T (TO-220 Packages
= 0.5 A for H (TO-39) Package
P_{max} = 20 W for K (TO-3) and T (TO-220) Packages
= 2 W for H (TO-39) Package

(3) Load and line regulation are specified at a constant junction temperature. Pulse testing with a low duty cycle is used. Change in V_O because of heating effects is covered under the Thermal Regulation specification.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(7) Power dissipation within an I.C. voltage regulator produces a temperature gradient on the die, affecting individual I.C. components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

SCHEMATIC DIAGRAM

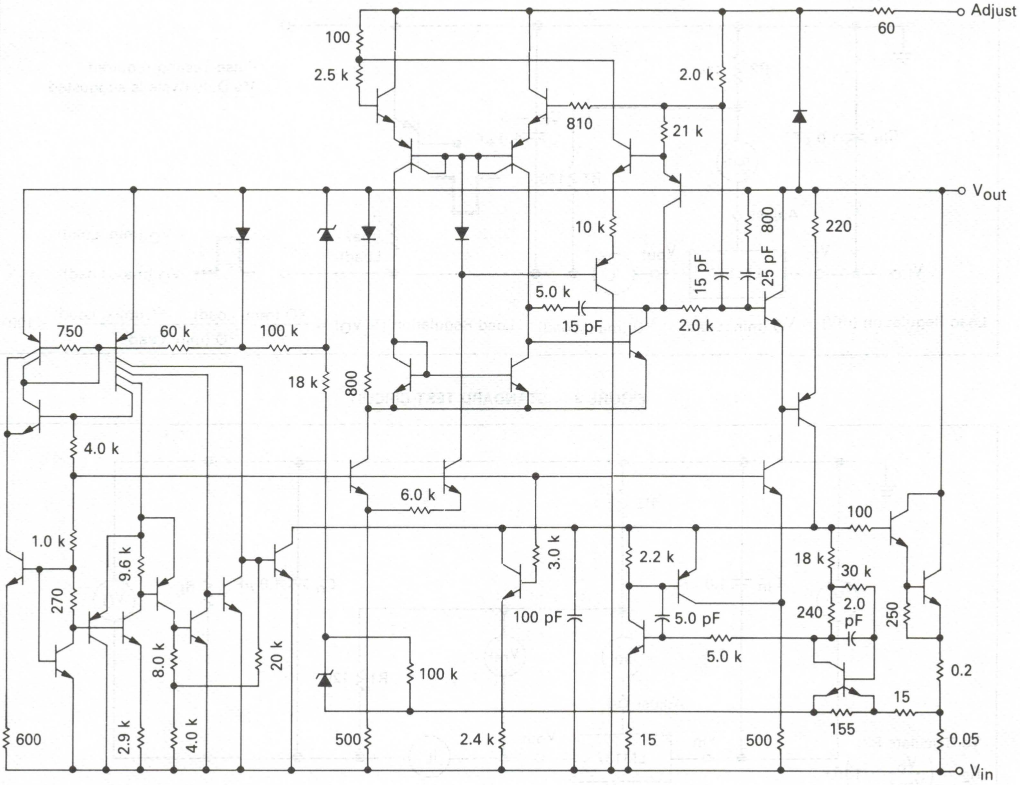
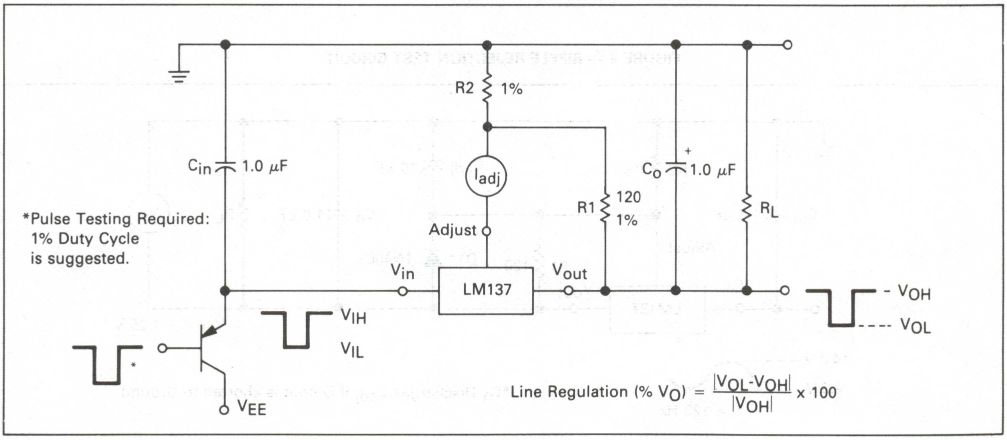

Adjust
60
100
2.5 k
810
2.0 k
21 k
Vout
10 k
800
220
15 pF
25 pF
5.0 k
15 pF
2.0 k
750
60 k
100 k
18 k
800
4.0 k
6.0 k
1.0 k
9.6 k
270
8.0 k
20 k
3.0 k
100 pF
2.2 k
5.0 pF
5.0 k
100
18 k
30 k
2.0 pF
240
250
100 k
0.2
15
155
600
2.9 k
4.0 k
500
2.4 k
15
500
0.05
Vin

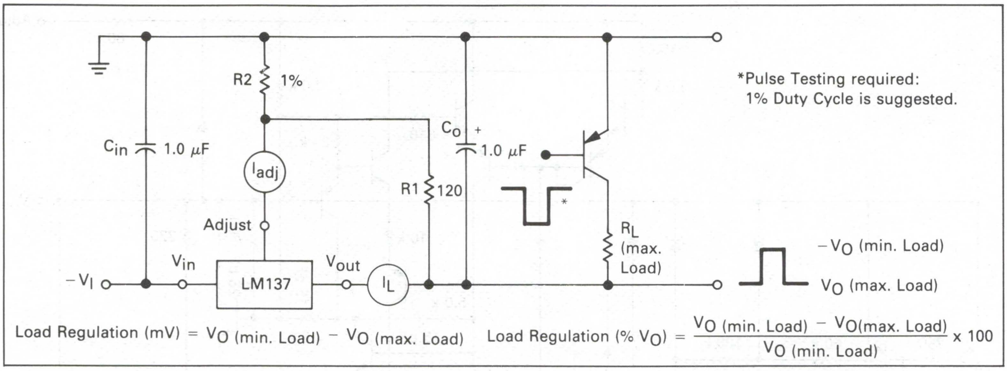
FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT


R2
1%
I_{adj}
Adjust
R1
120
1%
C_{in}
1.0 µF
C_O
+
1.0 µF
R_L
V_{in}
LM137
V_{out}
V_{IH}
V_{IL}
V_{OH}
V_{OL}
*
V_{EE}

*Pulse Testing Required:
1% Duty Cycle
is suggested.

$$\text{Line Regulation } (\% \ V_O) = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

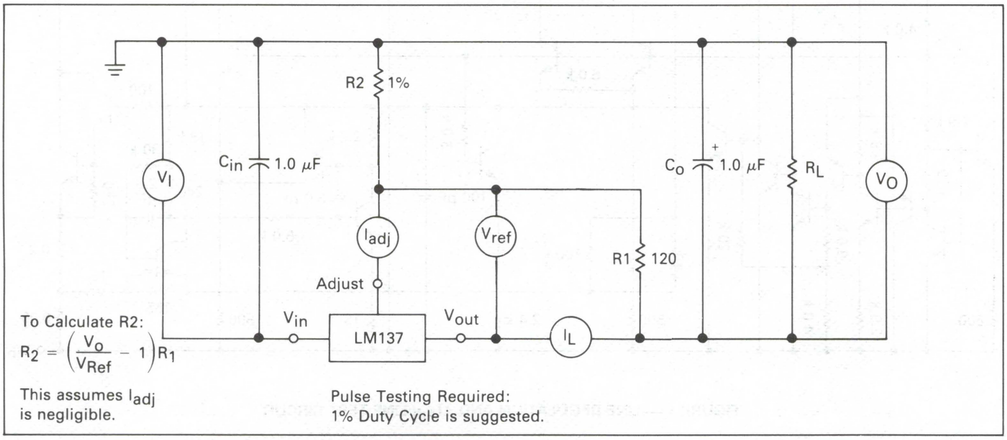

R2 1%
C_{in} 1.0 μF
I_{adj}
Adjust
C_O +
1.0 μF
R1 120
*
R_L (max. Load)
$-V_I$
V_{in}
LM137
V_{out}
I_L
$-V_O$ (min. Load)
V_O (max. Load)

*Pulse Testing required:
1% Duty Cycle is suggested.

Load Regulation (mV) = V_O (min. Load) − V_O (max. Load)

$$\text{Load Regulation } (\% V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{(max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

FIGURE 3 — STANDARD TEST CIRCUIT


R2 1%
V_I
C_{in} 1.0 μF
I_{adj}
V_{ref}
R1 120
C_O + 1.0 μF
R_L
V_O
Adjust
V_{in}
LM137
V_{out}
I_L

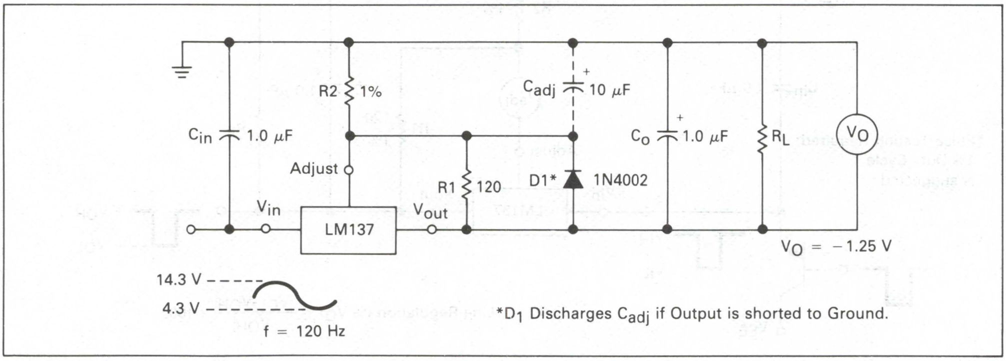
To Calculate R2:

$$R_2 = \left(\frac{V_o}{V_{Ref}} - 1\right) R_1$$

This assumes I_{adj} is negligible.

Pulse Testing Required:
1% Duty Cycle is suggested.

FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT


R2 1%
C_{in} 1.0 μF
Adjust
C_{adj} + 10 μF
R1 120
D1* 1N4002
C_O + 1.0 μF
R_L
V_O
V_{in}
LM137
V_{out}
V_O = −1.25 V
14.3 V
4.3 V
f = 120 Hz

*D_1 Discharges C_{adj} if Output is shorted to Ground.

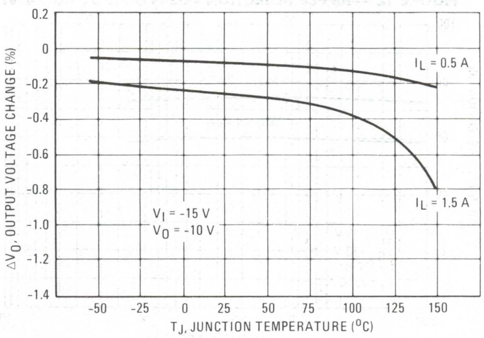


FIGURE 5 – LOAD REGULATION

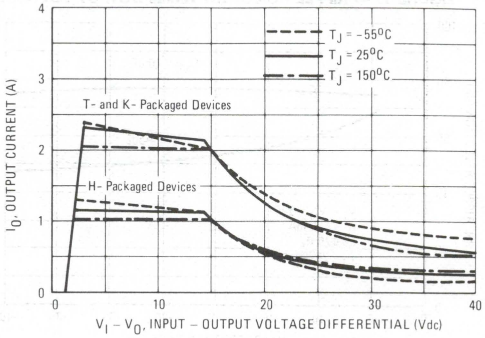


FIGURE 6 – CURRENT LIMIT

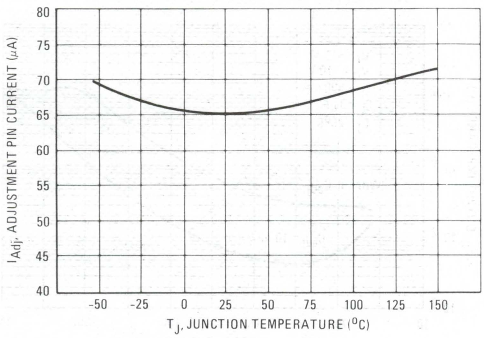


FIGURE 7 – ADJUSTMENT PIN CURRENT

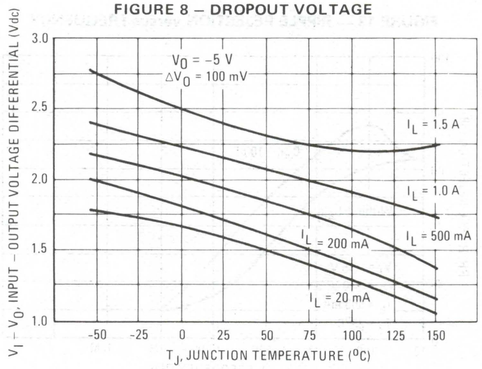


FIGURE 8 – DROPOUT VOLTAGE

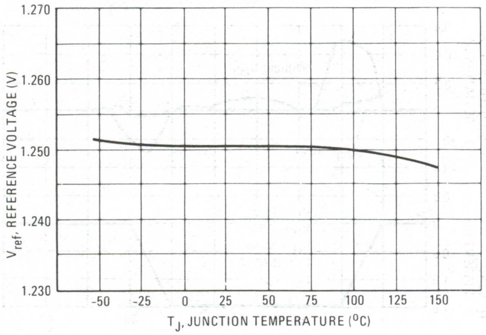


FIGURE 9 – TEMPERATURE STABILITY

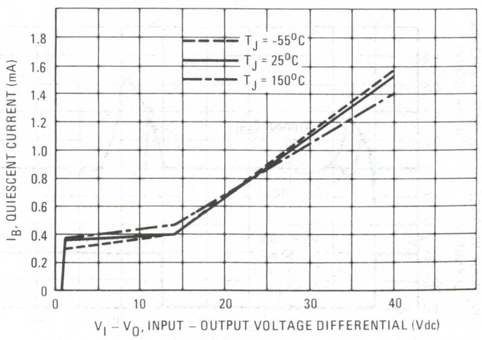


FIGURE 10 – MINIMUM OPERATING CURRENT

FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

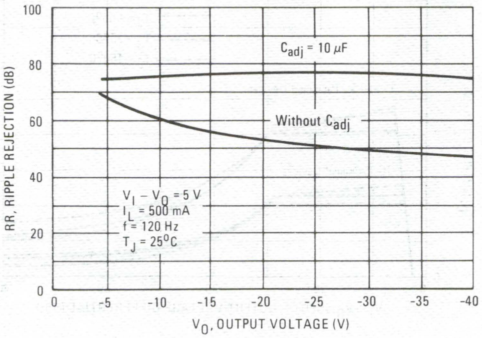


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

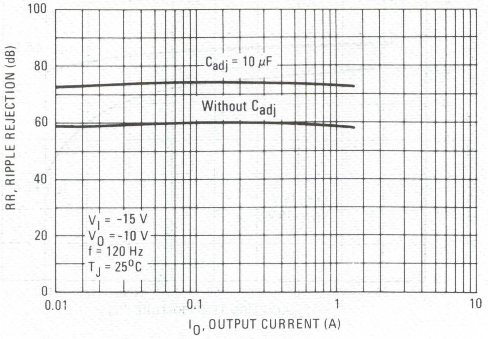


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

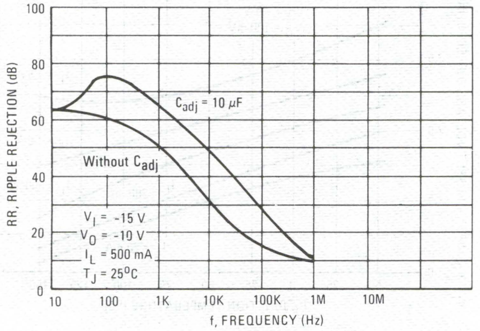


FIGURE 14 — OUTPUT IMPEDANCE

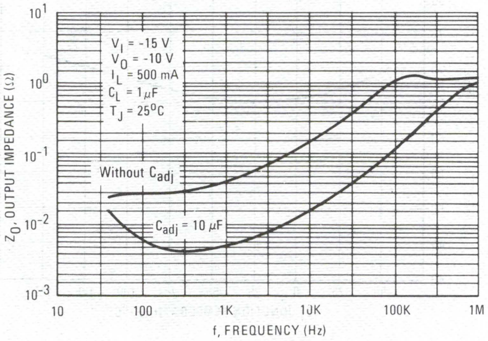


FIGURE 15 — LINE TRANSIENT RESPONSE

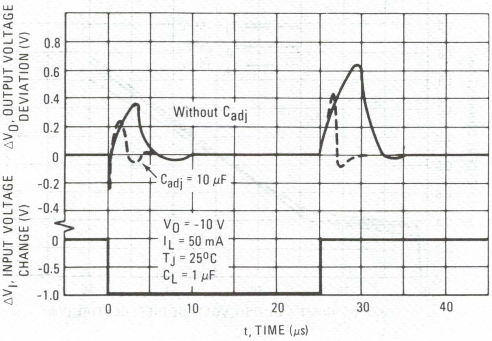
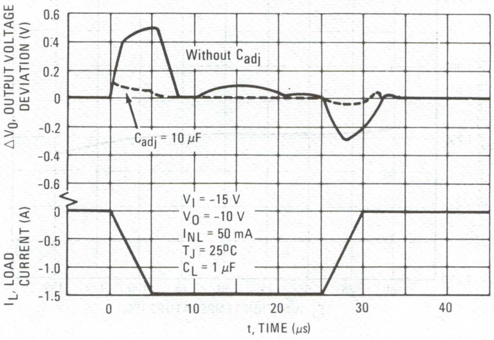


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

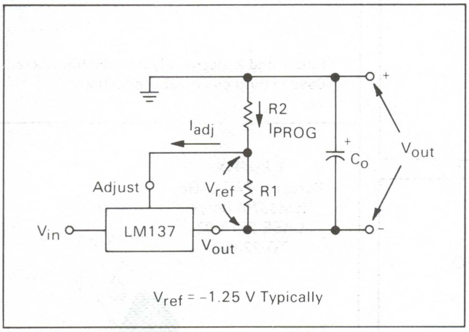
The LM137 is a 3-terminal floating regulator. In operation, the LM137 develops and maintains a nominal -1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM137 was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



V_{ref} = −1.25 V Typically

LOAD REGULATION

The LM137 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

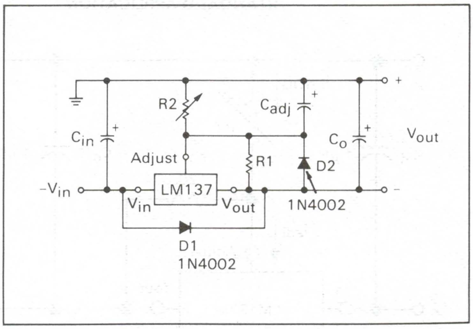
An output capacitor (C_O) in the form of a 1 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137 with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values ($C_O > 25$ μF, $C_{adj} > 10$ μF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES



LM137M
LM237M
LM337M

MOTOROLA

Specifications and Applications Information

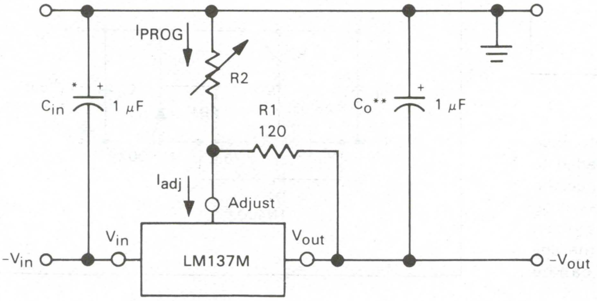
3-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

The LM137M/237M/337M are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 500 mA over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137M series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137M series can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

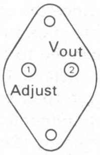
**C_O is necessary for stability. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

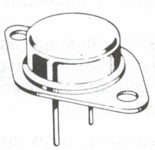
MEDIUM-CURRENT 3-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

R SUFFIX
METAL PACKAGE
CASE 80-02
TO-213AA
(TO-66)

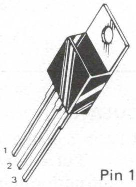


(Bottom View)
Case is Input



Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
(LM337M only)
CASE 221A-02
TO-220AB



Pin 1 Adjust
Pin 2 V_{in}
Pin 3 V_{out}

Heatsink surface connected to Pin 2

ORDERING INFORMATION

Device	Temperature Range	Package
LM137MR	T_J = −55°C to +150°C	Metal Power
LM237MR	T_J = −25°C to +150°C	Metal Power
LM337MR	T_J = 0°C to +125°C	Metal Power
LM337MT	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM137M LM237M LM337M	T_J	−55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.1$; $T_J = T_{low}$ to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	LM137M/237M			LM337M			Unit
			Min	Typ	Max	Min	Typ	Max	
Line Regulation (Note 3) $T_A = 25°C$, $3.0\text{ V} \leqslant \lvert V_I\text{-}V_O\rvert \leqslant 40\text{ V}$	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3), $T_A = 25°C$, $10\text{ mA} \leqslant I_O \leqslant 0.5\text{ A}$ $\lvert V_O\rvert \leqslant 5.0$ V $\lvert V_O\rvert \geqslant 5.0$ V	2	Reg_{load}	— —	15 0.3	25 0.5	— —	15 0.3	50 1.0	mV % V_O
Thermal Regulation 10 mS Pulse, $T_A = 25°C$	—	Reg_{therm}	—	0.002	0.02	—	0.003	0.04	$\%V_O/W$
Adjustment Pin Current	3	I_{adj}	—	65	100	—	65	100	μA
Adjustment Pin Current Change $2.5\text{ V} \leqslant \lvert V_I\text{-}V_O\rvert \leqslant 40\text{ V}$, $10\text{ mA} \leqslant I_L \leqslant 0.5\text{ A}$, $P_D \leqslant P_{max}$, $T_A = 25°C$	1,2	ΔI_{adj}	—	2.0	5.0	—	2.0	5.0	μA
Reference Voltage (Note 4) $3.0\text{ V} \leqslant \lvert V_I\text{-}V_O\rvert \leqslant 40\text{ V}$, $10\text{ mA} \leqslant I_O \leqslant 0.5\text{ A}$, $P_D \leqslant P_{max}$, $T_A = 25°C$ T_{low} to T_{high}	3	V_{ref}	−1.225 −1.20	−1.250 −1.25	−1.275 −1.30	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3) $3.0\text{ V} \leqslant \lvert V_I\text{-}V_O\rvert \leqslant 40\text{ V}$	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) $10\text{ mA} \leqslant I_O \leqslant 0.5\text{ A}$ $\lvert V_O\rvert \leqslant 5.0$ V $\lvert V_O\rvert \geqslant 5.0$ V	2	Reg_{load}	— —	20 0.3	50 1.0	— —	20 0.3	70 1.5	mV $\%V_O$
Temperature Stability ($T_{low} \leqslant T_J \leqslant T_{high}$)	3	T_S	—	0.6	—	—	0.6	—	$\%V_O$
Minimum Load Current to Maintain Regulation ($\lvert V_I\text{-}V_O\rvert \leqslant 10$ V) ($\lvert V_I\text{-}V_O\rvert \leqslant 40$ V)	3	I_{Lmin}	— —	1.2 2.5	3.0 5.0	— —	1.5 2.5	6.0 10	mA
Maximum Output Current $\lvert V_I\text{-}V_O\rvert \leqslant 15$ V, $P_D \leqslant P_{max}$ $\lvert V_I\text{-}V_O\rvert = 40$ V, $P_D \leqslant P_{max}$, $T_A = 25°C$	3	I_{max}	0.5 0.15	0.9 0.25	— —	0.5 0.1	0.9 0.25	— —	A
RMS Noise, % of V_O $T_A = 25°C$, $10\text{ Hz} \leqslant f \leqslant 10\text{ kHz}$	—	N	—	0.003	—	—	0.003	—	$\%V_O$
Ripple Rejection, $V_O = -10$ V, f = 120 Hz (Note 5) Without C_{adj} $C_{adj} = 10\ \mu F$	4	RR	— 66	60 77	— —	— 66	60 77	— —	dB
Long Term Stability, $T_J = T_{high}$ (Note 6) $T_A = 25°C$ for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case R Package (TO-66) T Package (TO-220)	—	$R_{\theta JC}$	— —	7.0 —	— —	— —	7.0 7.0	— —	°C/W

NOTES:

(1) $T_{low} = -55°C$ for LM137M $T_{high} = +150°C$ for LM137M
$= -25°C$ for LM237M $= +150°C$ for LM237M
$= 0°C$ for LM337M $= +125°C$ for LM337M

(2) $P_{max} = 7.5$ W

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

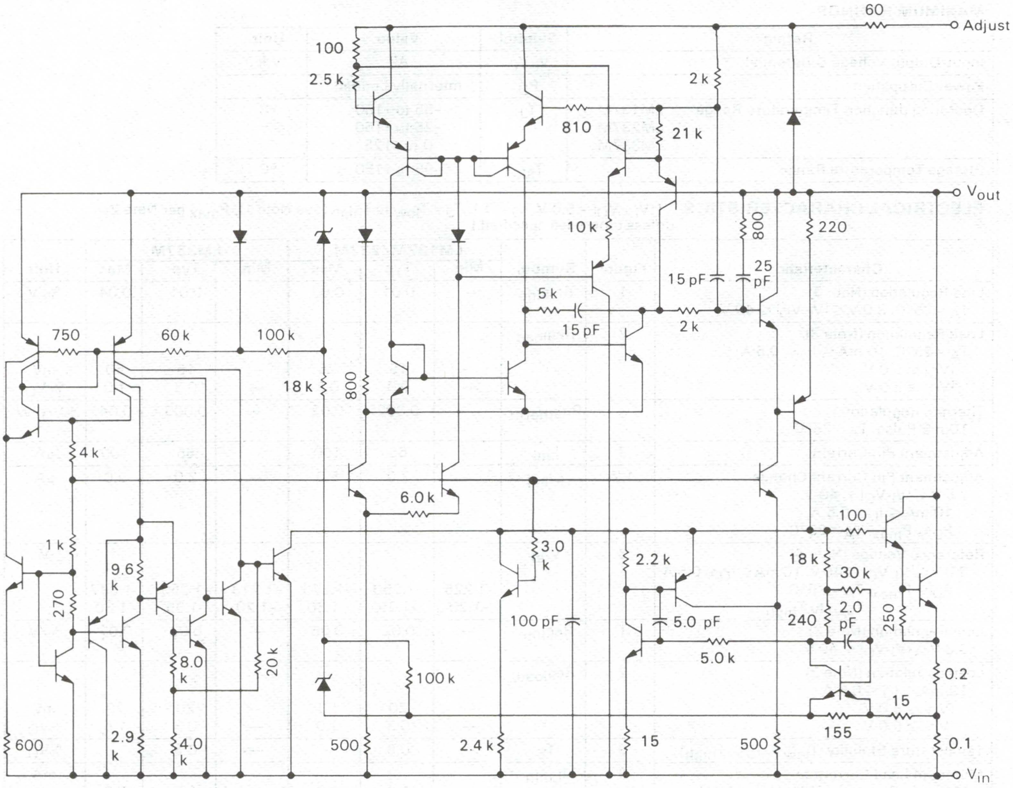
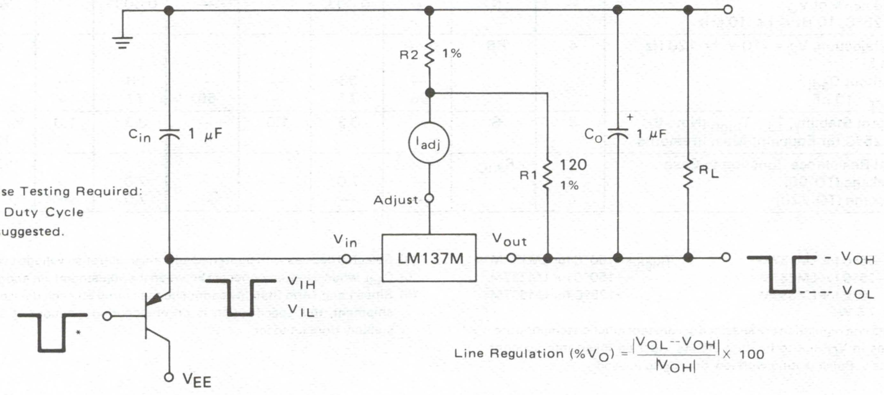

60
Adjust
100
2.5 k
2 k
810
21 k
Vout
10 k
800
220
15 pF
25 pF
5 k
15 pF
2 k
750
60 k
100 k
18 k
800
6.0 k
4 k
100
1 k
9.6 k
3.0 k
2.2 k
18 k
30 k
270
100 pF
5.0 pF
240
2.0 pF
250
5.0 k
8.0 k
20 k
100 k
0.2
15
155
600
2.9 k
4.0 k
500
2.4 k
15
500
0.1
Vin

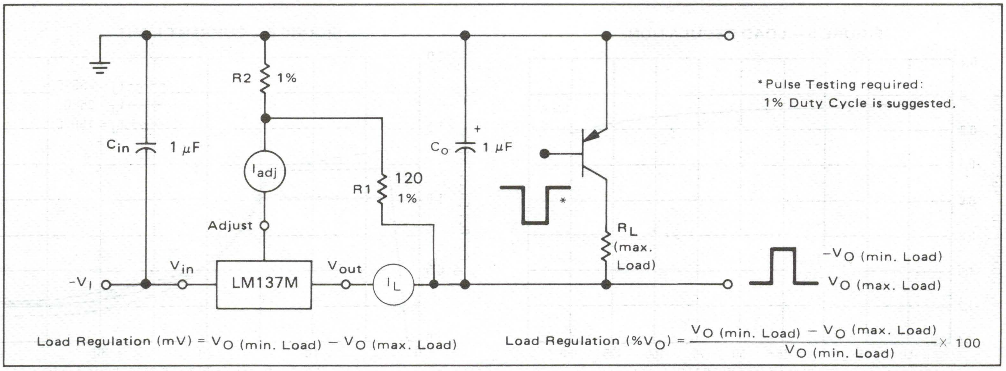
FIGURE 1 – LINE REGULATION AND ΔI_{adj}/LINE TEST CIRCUIT


R2 1%
I_{adj}
C_{in} 1 µF
C_O 1 µF
+
R1 120 1%
R_L
Adjust
V_{in}
V_{out}
LM137M
V_{IH}
V_{IL}
V_{OH}
V_{OL}
V_{EE}
*

* Pulse Testing Required:
1% Duty Cycle
is suggested.

$$\text{Line Regulation } (\%V_O) = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

FIGURE 2 – LOAD REGULATION AND ΔI_{adj}/LOAD TEST CIRCUIT

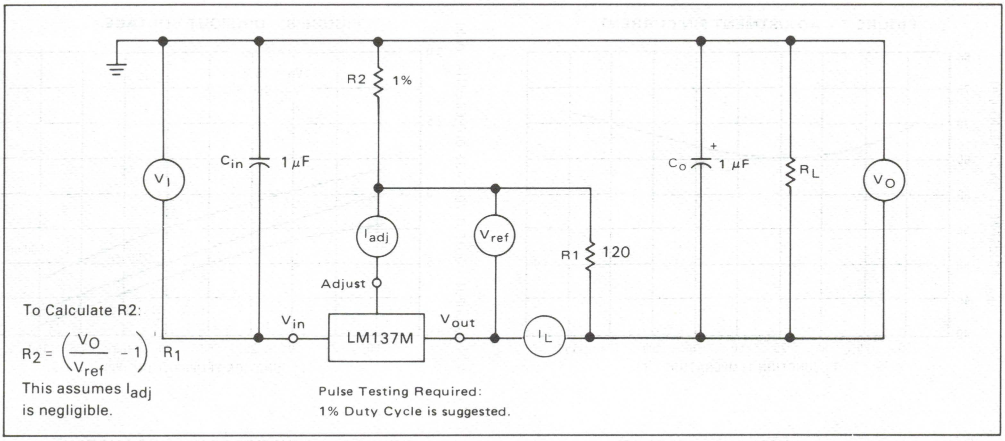

R2 1%
Cin 1 μF
Iadj
R1 120 1%
Adjust
Co + 1 μF
*
RL (max. Load)
–VI
Vin
LM137M
Vout
IL
–VO (min. Load)
VO (max. Load)

*Pulse Testing required:
1% Duty Cycle is suggested.

Load Regulation (mV) = V_O (min. Load) − V_O (max. Load)

$$\text{Load Regulation } (\%V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

FIGURE 3 – STANDARD TEST CIRCUIT


R2 1%
VI
Cin 1 μF
Co + 1 μF
RL
VO
Iadj
Vref
R1 120
Adjust
Vin
LM137M
Vout
IL

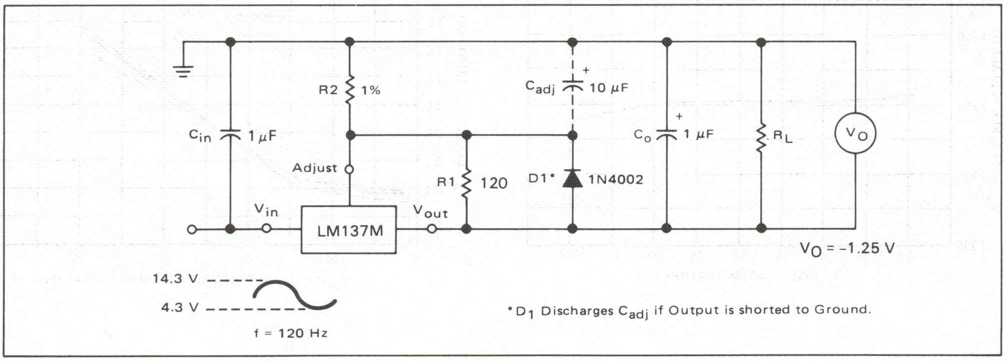
To Calculate R2:

$$R_2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$$

This assumes I_{adj} is negligible.

Pulse Testing Required:
1% Duty Cycle is suggested.

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


R2 1%
Cadj + 10 μF
Cin 1 μF
Co + 1 μF
RL
VO
Adjust
R1 120
D1* 1N4002
Vin
LM137M
Vout
VO = –1.25 V
14.3 V
4.3 V
f = 120 Hz

*D1 Discharges C_{adj} if Output is shorted to Ground.

FIGURE 5 – LOAD REGULATION

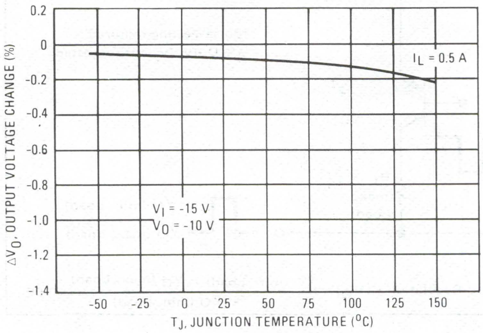


FIGURE 6 – CURRENT LIMIT

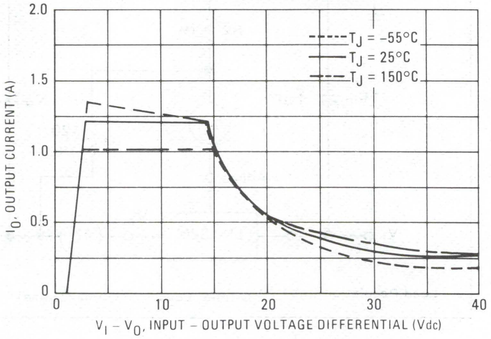


FIGURE 7 – ADJUSTMENT PIN CURRENT

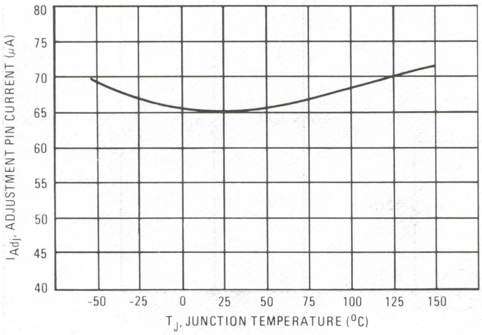


FIGURE 8 – DROPOUT VOLTAGE

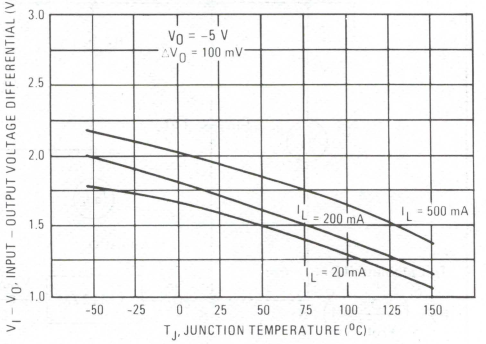


FIGURE 9 – TEMPERATURE STABILITY

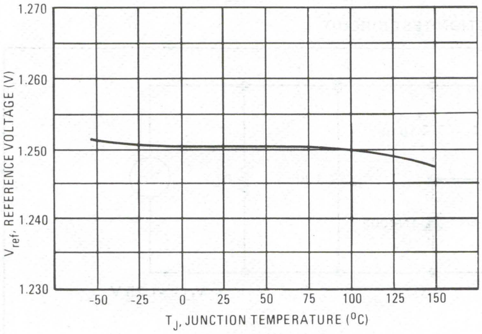


FIGURE 10 – MINIMUM OPERATING CURRENT

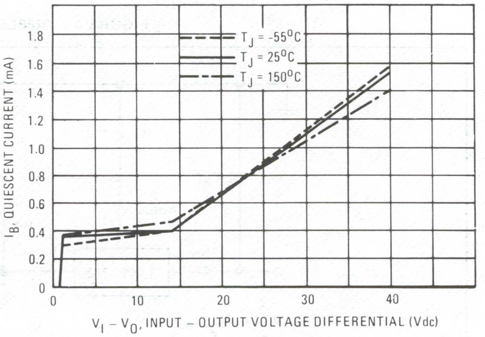


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

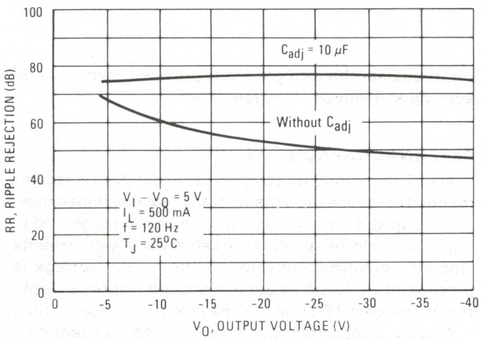


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

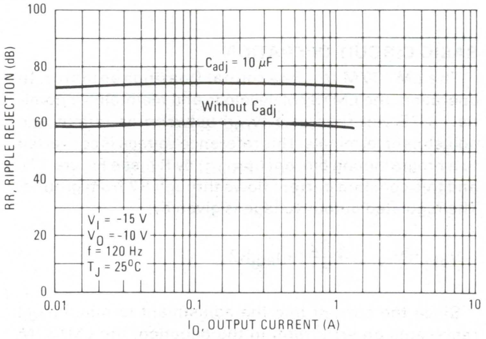


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

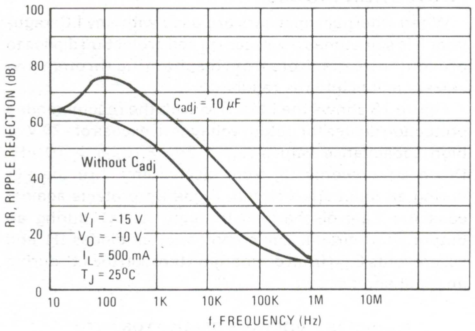


FIGURE 14 — OUTPUT IMPEDANCE

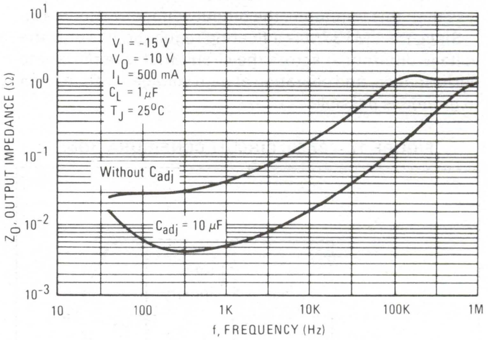


FIGURE 15 — LINE TRANSIENT RESPONSE

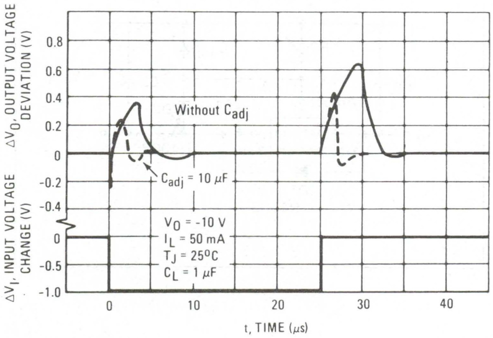
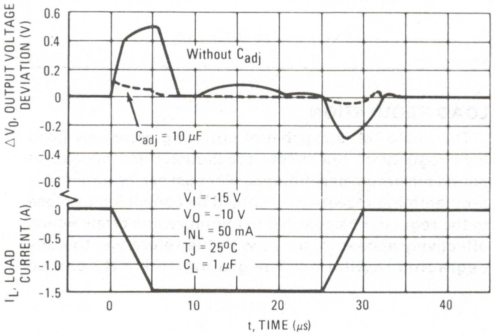


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

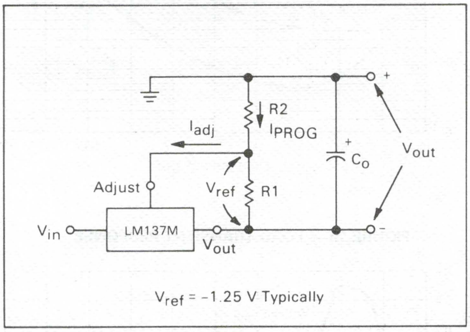
The LM137M is a 3-terminal floating regulator. In operation, the LM137M develops and maintains a nominal −1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM137M was designed to control I_{adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



V_{ref} = −1.25 V Typically

LOAD REGULATION

The LM137M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

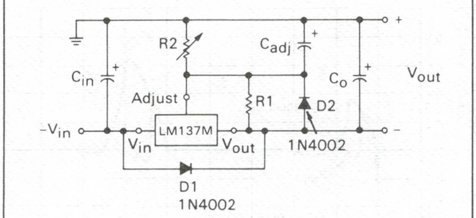
An output capacitor (C_O) in the form of a 1 µF tantalum or 10 µF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137M with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values ($C_O > 25$ µF, $C_{adj} > 10$ µF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA

LM140,A Series
LM340,A Series

Specifications and Applications Information

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 ampere. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

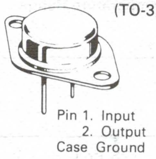
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage.

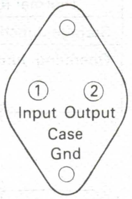
- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

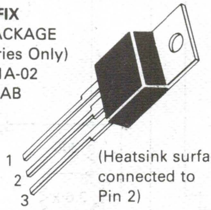
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)





T SUFFIX
PLASTIC PACKAGE
(LM340A, Series Only)
CASE 221A-02
TO-220AB

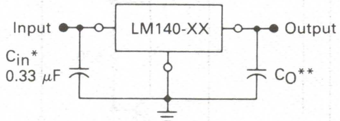


ORDERING INFORMATION

Device	Output Voltage and Tolerance	Operating Junction Temperature Range	Package
LM140K-5.0	5.0 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-5.0	5.0 V ± 2%	−55°C to +150°C	Metal Power
LM140K-6.0	6.0 V ± 4%	−55°C to +150°C	Metal Power
LM140K-8.0	8.0 V ± 4%	−55°C to +150°C	Metal Power
LM140K-12	12 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-12	12 V ± 2%	−55°C to +150°C	Metal Power
LM140K-15	15 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-15	15 V ± 2%	−55°C to +150°C	Metal Power
LM140K-18	18 V ± 4%	−55°C to +150°C	Metal Power
LM140K-24	24 V ± 4%	−55°C to +150°C	Metal Power
LM340K-5.0	5.0 V ± 4%	0°C to +125°C	Metal Power
LM340AK-5.0	5.0 V ± 2%	0°C to +125°C	
LM340T-5.0	5.0 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-5.0	5.0 V ± 2%	0°C to +125°C	
LM340K-6.0	6.0 V ± 4%	0°C to +125°C	Metal Power
LM340T-6.0	6.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-8.0	8.0 V ± 4%	0°C to +125°C	Metal Power
LM340T-8.0	8.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-12	12 V ± 4%	0°C to +125°C	Metal Power
LM340AK-12	12 V ± 2%	0°C to +125°C	
LM340T-12	12 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-12	12 V ± 2%	0°C to +125°C	
LM340K-15	15 V ± 4%	0°C to +125°C	Metal Power
LM340AK-15	15 V ± 2%	0°C to +125°C	
LM340T-15	15 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-15	15 V ± 2%	0°C to +125°C	
LM340K-18	18 V ± 4%	0°C to +125°C	Metal Power
LM340T-18	18 V ± 4%	0°C to +125°C	Plastic Power
LM340K-24	24 V ± 4%	0°C to +125°C	Metal Power
LM340T-24	24 V ± 4%	0°C to +125°C	Plastic Power

*2% regulators are available in 5, 12 and 15 volt devices

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

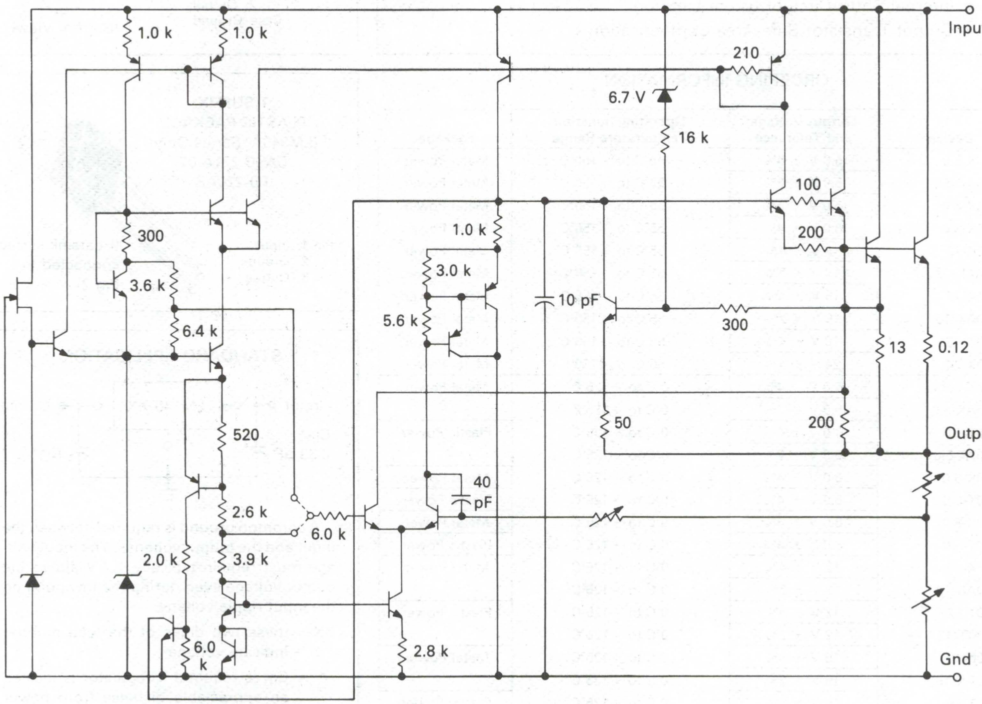
* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μF ceramic disc.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range LM140,A LM340,A	T_J	 –55 to +150 0 to +150	°C

EQUIVALENT SCHEMATIC DIAGRAM


Input
1.0 k
1.0 k
210
6.7 V
16 k
100
200
300
3.6 k
6.4 k
1.0 k
3.0 k
5.6 k
10 pF
300
13
0.12
50
200
Output
520
2.6 k
6.0 k
40 pF
2.0 k
3.9 k
6.0 k
2.8 k
Gnd

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM140/340 — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
8.0 to 20 Vdc		—	—	50	
7.0 to 25 Vdc (T_J = +25°C)		—	—	50	
8.0 to 12 Vdc, I_O = 1.0 A		—	—	25	
7.3 to 20 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	50	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	50	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	50	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	25	
Output Voltage	V_O				Vdc
LM140 8.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
LM340 7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
Quiescent Current I_O = 1.0 A	I_B				mA
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V LM140, LM340		—	—	0.5	
8.0 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM140		—	—	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		68	—	—	
LM340		62	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		68	80	—	
LM340		62	80	—	
Dropout Voltage	$V_{in}-V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	—	—	Vdc

NOTES: 1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
7.5 to 20 Vdc, I_O = 500 mA		—	—	10	
7.3 to 20 Vdc (T_J = +25°C)		—	3.0	10	
8.0 to 12 Vdc		—	—	12	
8.0 to 12 Vdc (T_J = +25°C)		—	—	4.0	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	25	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	25	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	15	
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	—	5.2	Vdc
Quiescent Current	I_B	—	—	6.5	mA
(T_J = +25°C)		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		—	—	0.5	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	—	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection 8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR				dB
I_O = 500 mA		68	—	—	
I_O = 1.0 A (T_J = +25°C)		68	80	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		7.3	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 6.0

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, $T_J = T_{low}$ to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
I_O = 5.0 mA to 1.0 A					
Line Regulation (Note 2)	Reg_{line}				mV
9.0 to 21 Vdc		—	—	60	
8.0 to 25 Vdc (T_J = +25°C)		—	—	60	
9.0 to 13 Vdc, I_O = 1.0 A		—	—	30	
8.3 to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	60	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	30	
Output Voltage	V_O				Vdc
LM140					
9.0 ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
LM340					
8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
9.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V LM140, LM340		—	—	0.5	
9.0 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM140		—	—	0.8	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		65	—	—	
LM340		59	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		65	78	—	
LM340		59	78	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.9	—	A
Output Noise Voltage (T_A = +25°C)	V_n	—	45	—	µV
10 Hz ≤ f ≤ 100 kHz					
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.7	—	mV/°C
I_O = 5.0 mA					
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		8.3	—	—	Vdc
I_O = 1.0 A					

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 8.0

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
11 to 23 Vdc		—	—	80	
10.5 to 25 Vdc (T_J = +25°C)		—	—	80	
11 to 17 Vdc, I_O = 1.0 A		—	—	40	
10.5 to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	80	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	40	
Output Voltage	V_O				Vdc
LM140 11.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
LM340 10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
Quiescent Current I_O = 1.0 A	I_B				mA
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
11.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V LM140, LM340		—	—	0.5	
11.5 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM140		—	—	0.8	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		62	—	—	
LM340		56	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		62	76	—	
LM340		56	76	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.5	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	52	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
15 to 27 Vdc		—	—	120	
14.6 to 30 Vdc (T_J = +25°C)		—	—	120	
16 to 22 Vdc, I_O = 1.0 A		—	—	60	
14.6 to 27 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	120	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	120	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	120	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	60	
Output Voltage	V_O				Vdc
LM140					
15.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
LM340					
14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V LM140, LM340		—	—	0.5	
15 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM140		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		61	—	—	
LM340		55	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		61	72	—	
LM340		55	72	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
14.8 to 27 Vdc, I_O = 500 mA		—	—	18	
14.5 to 27 Vdc (T_J = +25°C)		—	4.0	18	
16 to 22 Vdc		—	—	30	
16 to 22 Vdc (T_J = +25°C)		—	—	9.0	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	32	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	19	
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	—	12.5	Vdc
Quiescent Current	I_B	—	—	6.5	mA
(T_J = +25°C)		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		—	—	0.5	
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection 15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR				dB
I_O = 500 mA		61	—	—	
I_O = 1.0 A, (T_J = +25°C)		61	72	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
18.5 to 30 Vdc		—	—	150	
17.5 to 30 Vdc (T_J = +25°C)		—	—	150	
20 to 26 Vdc, I_O = 1.0 A		—	—	75	
17.7 to 30 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	150	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	150	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	150	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	75	
Output Voltage	V_O				Vdc
LM140 18.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
LM340 17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
Quiescent Current I_O = 1.0 A	I_B				mA
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V LM140, LM340		—	—	0.5	
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM140		—	—	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		60	—	—	
LM340		54	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		60	70	—	
LM340		54	70	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
17.9 to 30 Vdc, I_O = 500 mA		—	—	22	
17.5 to 30 Vdc (T_J = +25°C)		—	4.0	22	
20 to 26 Vdc, I_O = 1.0 A		—	—	30	
20 to 26 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	10	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	75	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	12	35	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	21	
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	—	15.6	Vdc
Quiescent Current	I_B	—	—	6.5	mA
(T_J = +25°C)		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		—	—	0.5	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	—	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection	RR				dB
18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz					
I_O = 500 mA		60	—	—	
I_O = 1.0 A, (T_J = +25°C)		60	70	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A　T_{high} = +150°C for LM140A
   = 0°C for LM340A　= +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 18

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
21.5 to 33 Vdc		—	—	180	
21 to 33 Vdc (T_J = +25°C)		—	—	180	
24 to 30 Vdc, I_O = 1.0 A		—	—	90	
21 to 33 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	180	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	180	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	180	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	90	
Output Voltage	V_O				Vdc
LM140 22 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		17.1	—	18.9	
LM340 21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		17.1	—	18.9	
Quiescent Current I_O = 1.0 A	I_B				mA
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
22 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA LM140		—	—	0.8	
21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V LM140, LM340		—	—	0.5	
22 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A LM140		—	—	0.8	
21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		59	—	—	
LM340		53	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		59	69	—	
LM340		53	69	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	500	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±2.3	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		21	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 24

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	23	24	25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
28 to 38 Vdc		—	—	240	
27 to 38 Vdc (T_J = +25°C)		—	—	240	
30 to 36 Vdc, I_O = 1.0 A		—	—	120	
27.1 to 38 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	240	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	120	
Output Voltage	V_O				Vdc
LM140					
28 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		22.8	—	25.2	
LM340					
27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		22.8	—	25.2	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
28 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA LM140		—	—	0.8	
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V LM140, LM340		—	—	0.5	
28 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A LM140		—	—	0.8	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		56	—	—	
LM340		50	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		56	66	—	
LM340		50	66	—	
Dropout Voltage	$V_{in}-V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	200	—	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±3.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		27.1	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340   = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

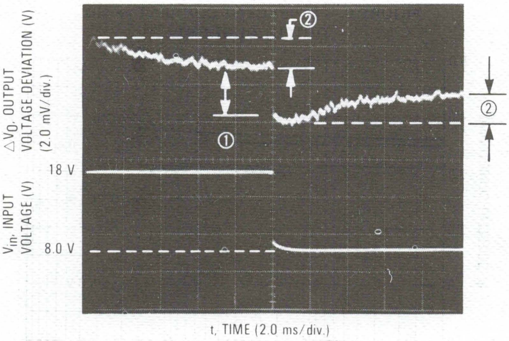
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

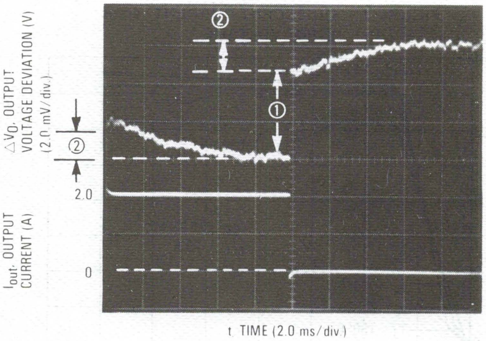
Figure 1 shows the line and thermal regulation response of a typical LM140AK-5.0 to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM140AK-5.0 to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



LM140AK-5.0
$V_O = 5.0$ V
$V_{in} = 8.0\text{ V} \rightarrow 18\text{ V} \rightarrow 8.0\text{ V}$ ① = $Reg_{line} = 2.4$ mV
$I_{out} = 1.0$ A ② = $Reg_{therm} = 0.0030\% V_O/W$

FIGURE 2 — LOAD AND THERMAL REGULATION



LM140AK-5.0
$V_O = 5.0$ V
$V_{in} = 15$ ① = $Reg_{load} = 4.4$ mV
$I_{out} = 0\text{ A} \rightarrow 1.5\text{ A} \rightarrow 0\text{ A}$ ② = $Reg_{therm} = 0.0020\% V_O/W$

FIGURE 3 — TEMPERATURE STABILITY

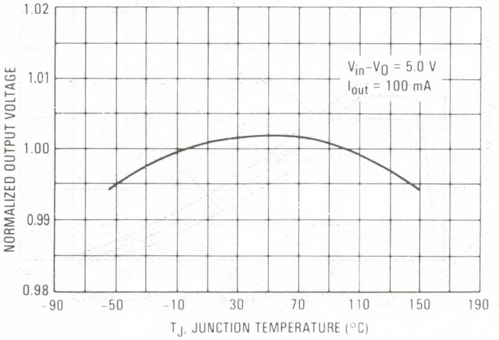


FIGURE 4 — OUTPUT IMPEDANCE

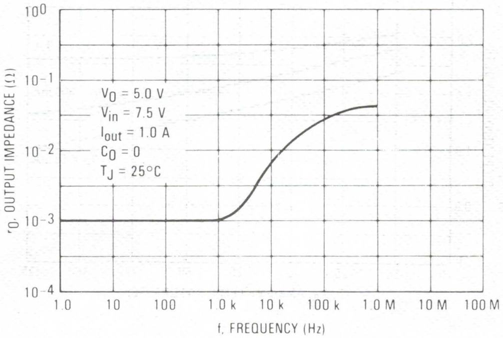


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

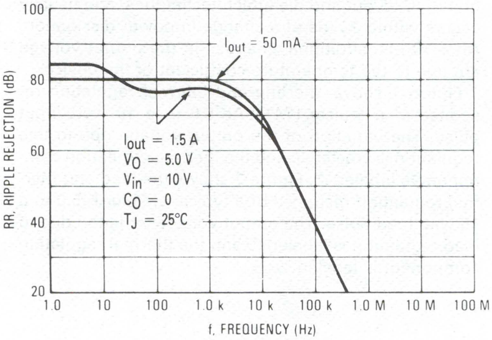


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

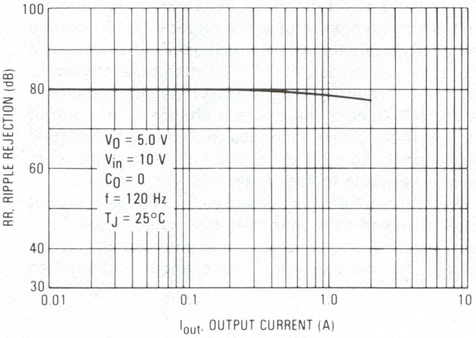


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

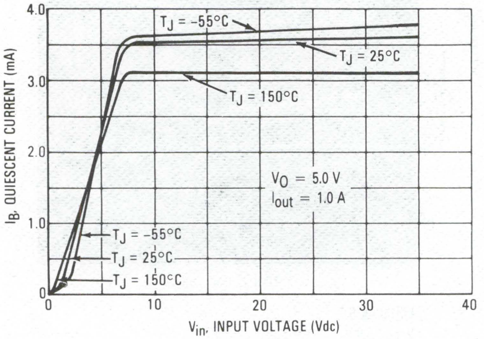


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

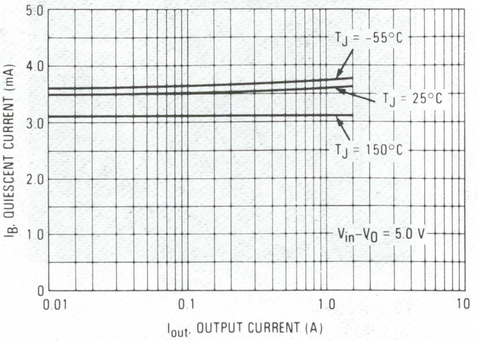


FIGURE 9 — DROPOUT VOLTAGE

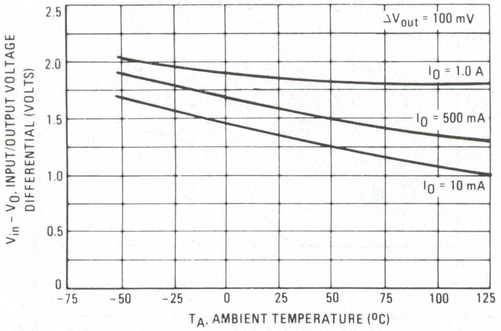


FIGURE 10 — PEAK OUTPUT CURRENT

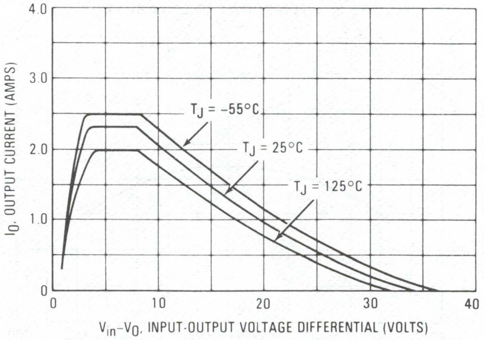


FIGURE 11 — LINE TRANSIENT RESPONSE

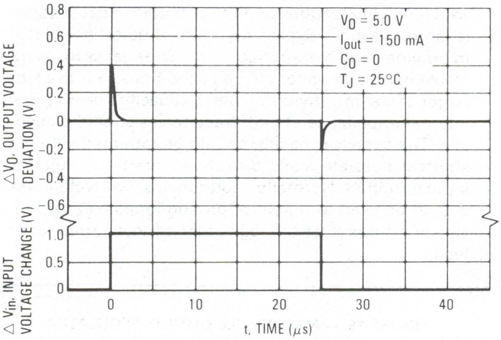


FIGURE 12 — LOAD TRANSIENT RESPONSE

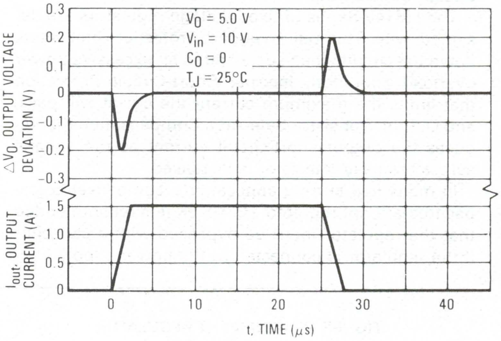


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

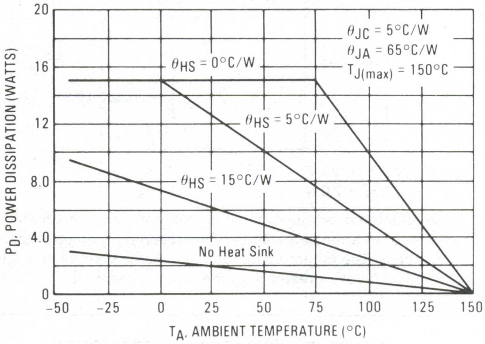
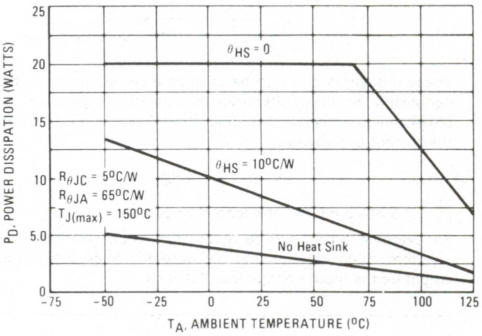


FIGURE 14 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)



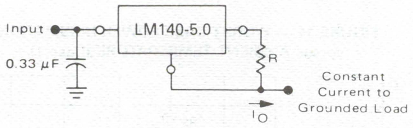
APPLICATIONS INFORMATION

Design Considerations

The LM140 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



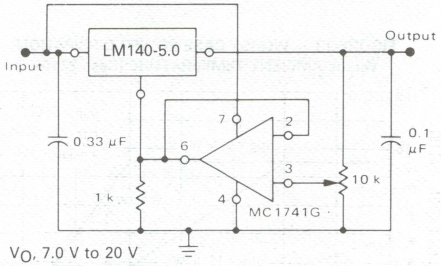
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM140-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR

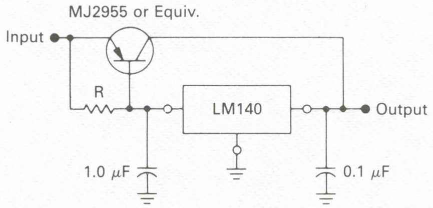


V_O, 7.0 V to 20 V

$V_{IN} - V_O \geqslant 2.0$ V

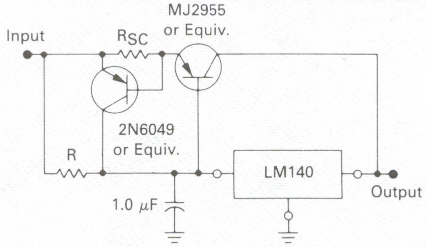
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with thi arrangement is 2.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM140 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 18 — SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, P_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

LM150
LM250
LM350

Specifications and Applications Information

3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

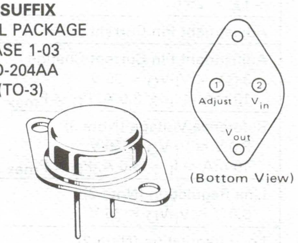
3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM150/250/350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM150 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 series can be used as a precision current regulator.

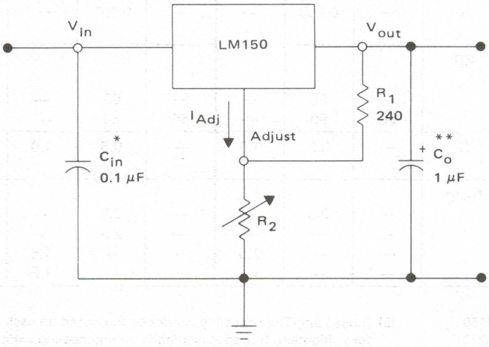
- Guaranteed 3.0 Amps Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

STANDARD APPLICATION



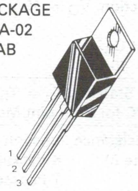
* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB



Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}

Heatsink surface connected to Pin 2

ORDERING INFORMATION

Device	Temperature Range	Package
LM150K	T_J = -55°C to +150°C	Metal Power
LM250K	T_J = -25°C to +150°C	Metal Power
LM350K	T_J = 0°C to +125°C	Metal Power
LM350T	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	35	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM150 LM250 LM350	T_J	−55 to +150 −25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Soldering Lead Temperature (10 seconds)			300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_I-V_O = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [see Note 1].)

			LM150/250			LM350			
Characteristic	Figure	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.005	0.01	—	0.005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_L ≤ 3.0 A	2	Reg_{load}							
V_O ≤ 5.0 V			—	5.0	15	—	5.0	25	mV
V_O ≥ 5.0 V			—	0.1	0.3	—	0.1	0.5	% V_O
Thermal Regulation, Pulse = 20 ms, T_A = 25°C	—	Reg_{therm}	—	0.002	—	—	0.002	—	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 3) 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A	2	Reg_{load}							
V_O ≤ 5.0 V			—	20	50	—	20	70	mV
V_O ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	1.0	—	—	1.0	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 35 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current	3	I_{max}							A
V_I-V_O ≤ 10 V, P_D ≤ P_{max}			3.0	4.5	—	3.0	4.5	—	
V_I-V_O = 30 V, P_D ≤ P_{max}, T_A = 25°C			0.3	1.0	—	0.25	1.0	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4)	4	RR							dB
Without C_{Adj}			—	65	—	—	65	—	
C_{Adj} = 10 μF			66	80	—	66	80	—	
Long-Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
Peak (Note 6) K Package (TO-3)			—	2.3	—	—	2.3	—	
T Package (TO-220)			—	—	—	—	2.3	—	
Average (Note 7) K Package (TO-3)			—	—	1.5	—	—	1.5	
T Package (TO-220)			—	—	—	—	—	1.5	

NOTES:

(1) T_{low} = −55°C for LM150 T_{high} = +150°C for LM150
−25°C for LM250 = +150°C for LM250
0°C for LM350 = +125°C for LM350
P_{max} = 30 W for K suffix (TO-3)
P_{max} = 25 W for T suffix (TO-220)

(2) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(3) Selected devices with tightened tolerance reference voltage available.

(4) C_{Adj}, when used, is connected between the adjustment pin and ground.

(5) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(6) Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to other measurement techniques.

(7) The average die temperature is used to derive the value of thermal resistance junction to case (average).

SCHEMATIC DIAGRAM

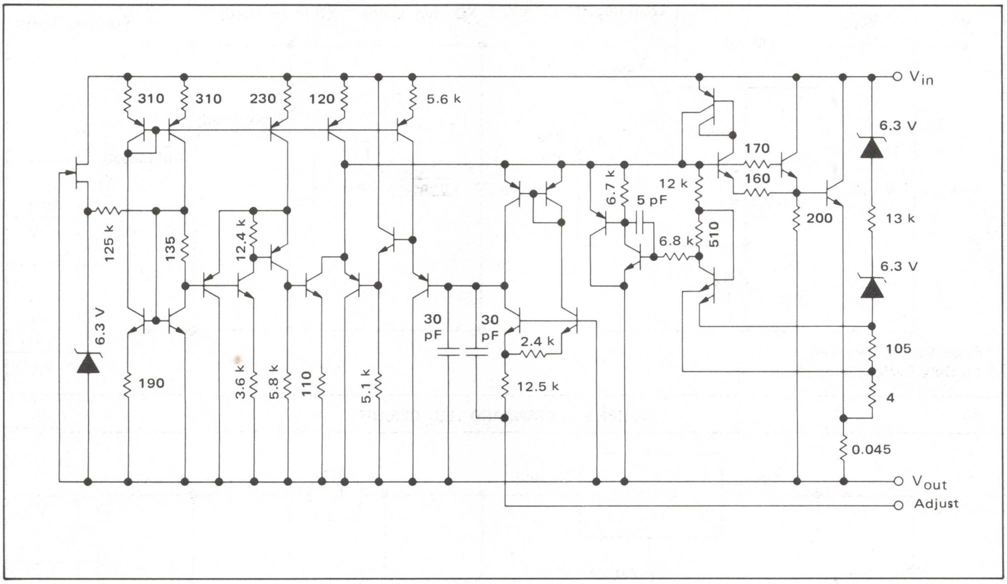
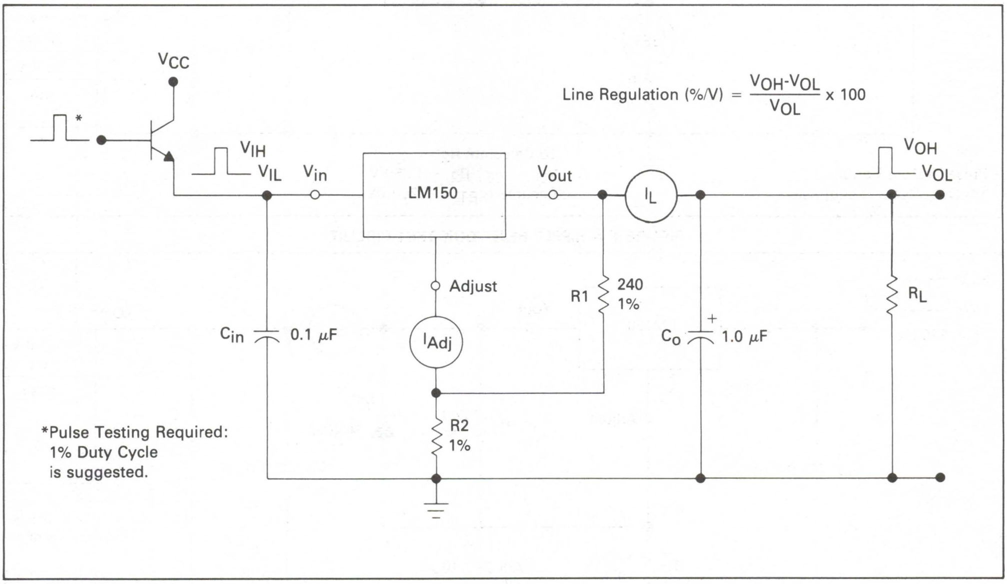

310
310
230
120
5.6 k
V in
6.3 V
170
160
12 k
6.7 k
5 pF
200
13 k
125 k
135
12.4 k
6.8 k
510
6.3 V
6.3 V
30 pF
30 pF
2.4 k
105
190
3.6 k
5.8 k
110
5.1 k
12.5 k
4
0.045
V out
Adjust

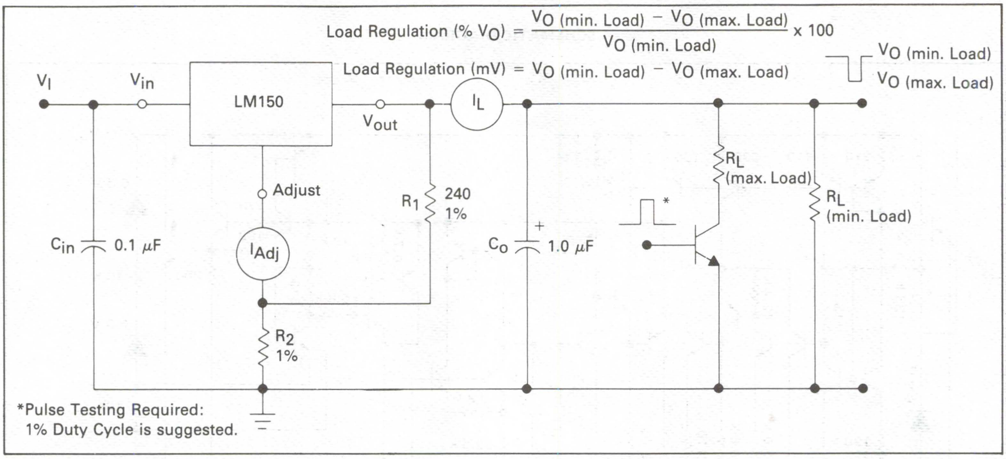
FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT


VCC
*
VIH
VIL
Vin
LM150
Vout
IL
VOH
VOL
Adjust
R1
240
1%
RL
Cin
0.1 µF
IAdj
Co
+
1.0 µF
R2
1%

$$\text{Line Regulation (\%/V)} = \frac{V_{OH}\text{-}V_{OL}}{V_{OL}} \times 100$$

*Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT



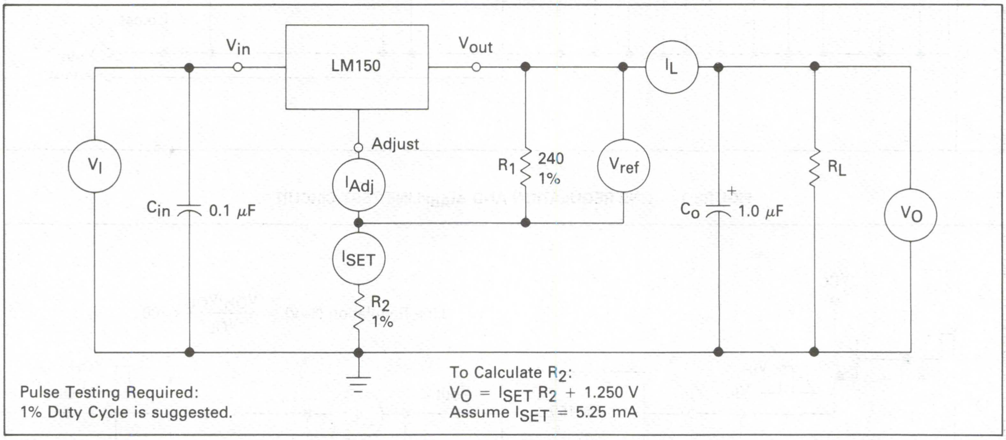
$$\text{Load Regulation } (\% \ V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

$$\text{Load Regulation (mV)} = V_O \text{ (min. Load)} - V_O \text{ (max. Load)}$$

*Pulse Testing Required:
1% Duty Cycle is suggested.

V_O (min. Load)
V_O (max. Load)
V_I
V_in
LM150
V_out
I_L
Adjust
R_1 240 1%
C_in 0.1 µF
I_Adj
R_2 1%
C_O 1.0 µF
+
*
R_L (max. Load)
R_L (min. Load)

FIGURE 3 — STANDARD TEST CIRCUIT

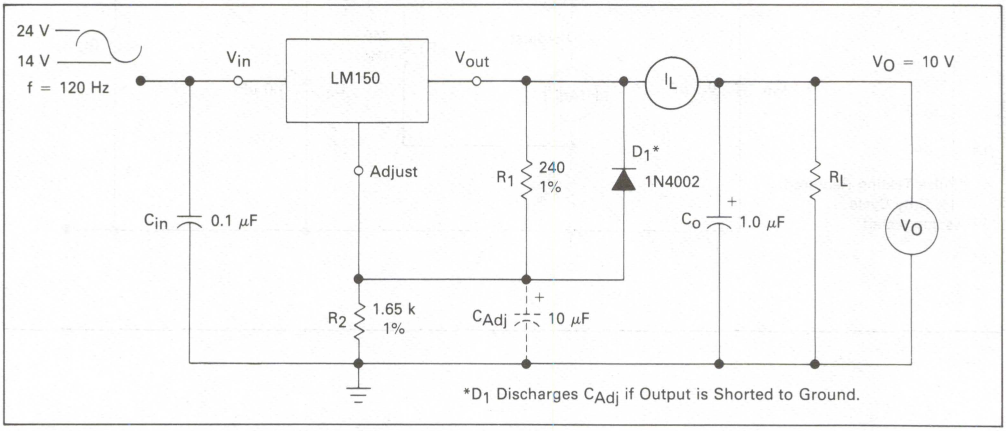


Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

V_in
LM150
V_out
I_L
V_I
Adjust
I_Adj
R_1 240 1%
V_ref
C_in 0.1 µF
I_SET
R_2 1%
C_O 1.0 µF
+
R_L
V_O

FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT



*D_1 Discharges C_{Adj} if Output is Shorted to Ground.

24 V
14 V
f = 120 Hz
V_in
LM150
V_out
I_L
V_O = 10 V
Adjust
R_1 240 1%
D_1*
1N4002
C_in 0.1 µF
C_O 1.0 µF
+
R_L
V_O
R_2 1.65 k 1%
C_Adj 10 µF
+

FIGURE 5 — LOAD REGULATION

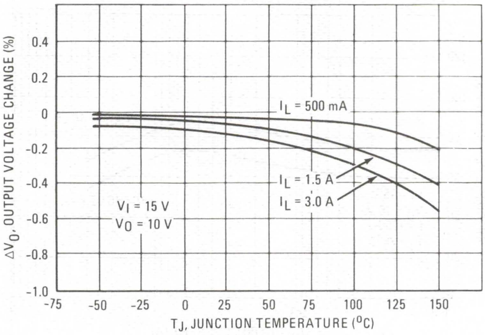


FIGURE 6 — CURRENT LIMIT

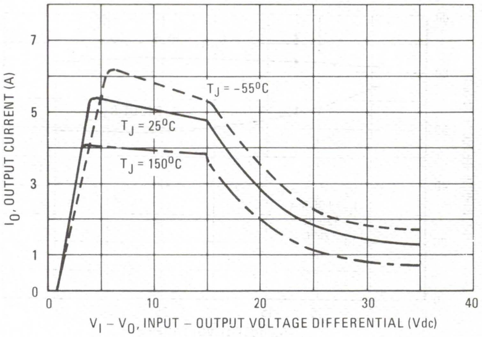


FIGURE 7 — ADJUSTMENT PIN CURRENT

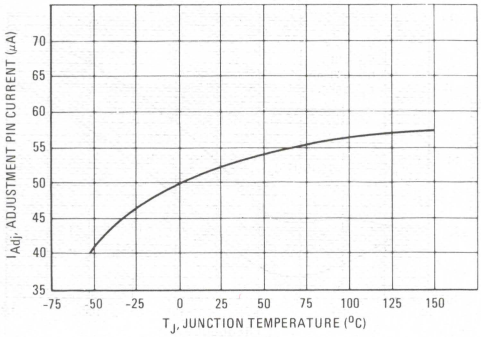


FIGURE 8 — DROPOUT VOLTAGE

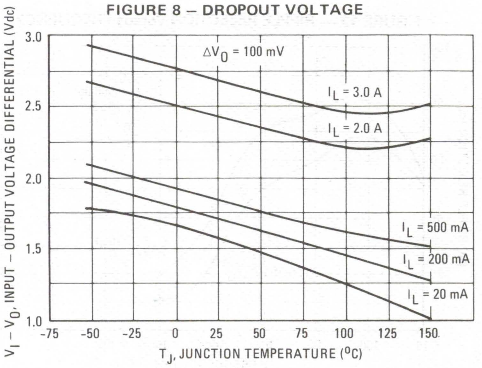


FIGURE 9 — TEMPERATURE STABILITY

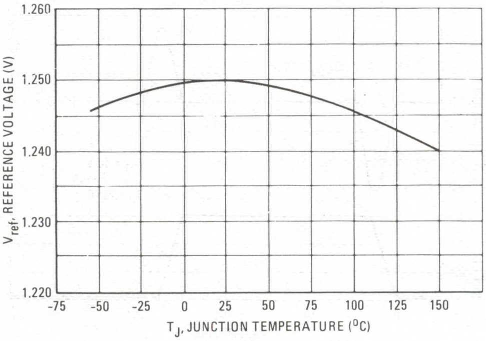


FIGURE 10 — MINIMUM OPERATING CURRENT

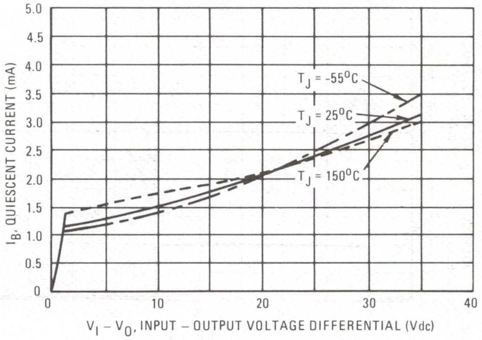


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

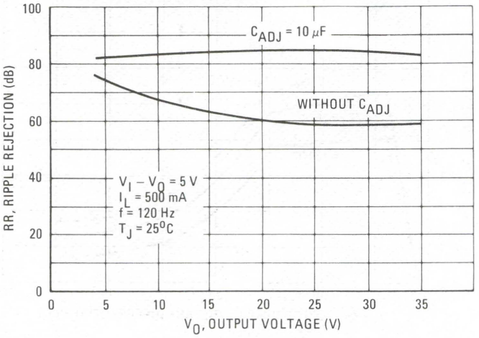


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

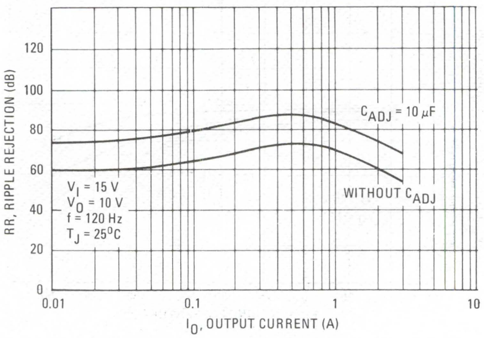


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

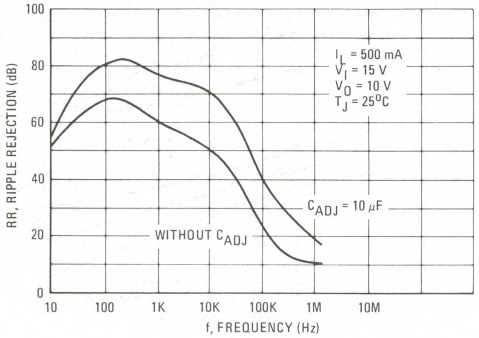


FIGURE 14 — OUTPUT IMPEDANCE

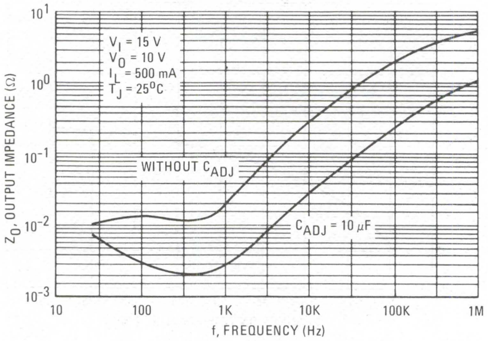


FIGURE 15 — LINE TRANSIENT RESPONSE

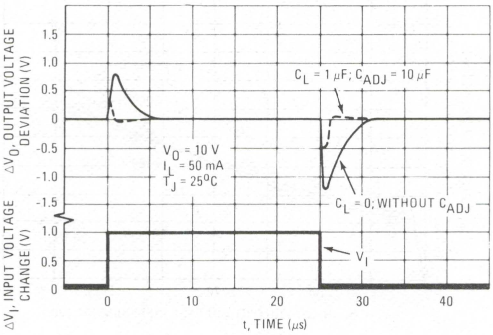
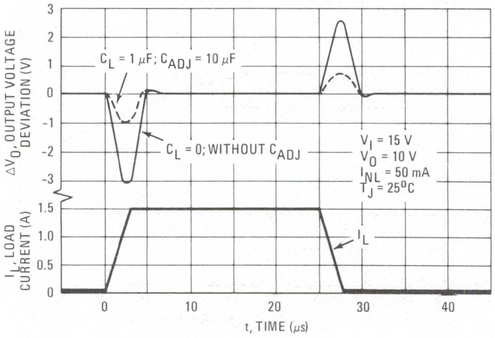


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

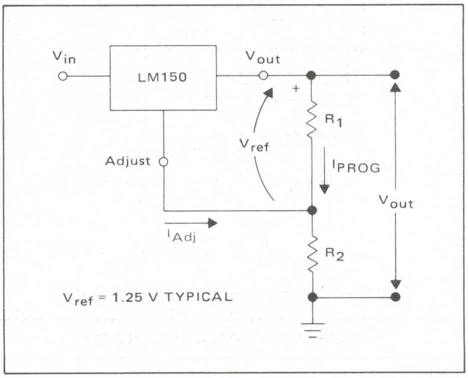
The LM150 is a 3-terminal floating regulator. In operation, the LM150 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM150 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM150 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM150 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM150 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM150 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25\ \mu F$, $C_{ADJ} > 10\ \mu F$). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

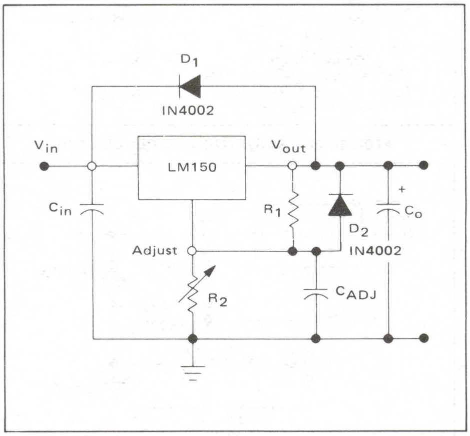
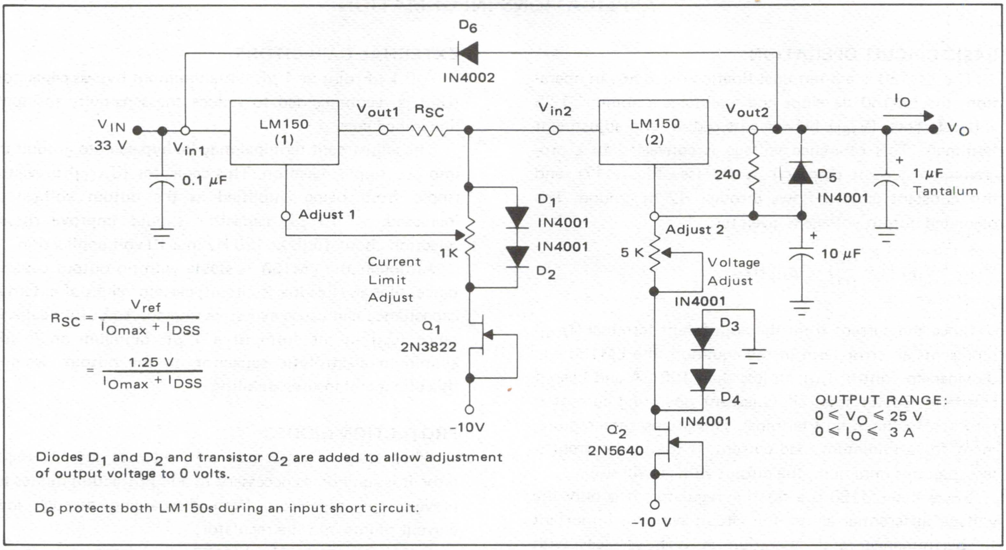


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE


D6
IN4002
VIN
33 V
Vin1
LM150
(1)
Vout1
RSC
0.1 µF
Adjust 1
1K
Current
Limit
Adjust
D1
IN4001
IN4001
D2
Q1
2N3822
-10V
Vin2
LM150
(2)
Vout2
IO
VO
240
D5
IN4001
+
1 µF
Tantalum
Adjust 2
5 K
Voltage
Adjust
+
10 µF
IN4001
D3
D4
IN4001
Q2
2N5640
-10 V

$$R_{SC} = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

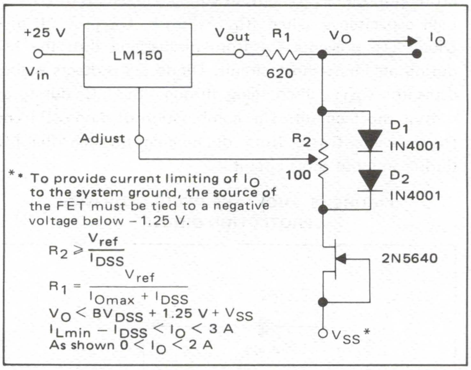
$$= \frac{1.25\ V}{I_{Omax} + I_{DSS}}$$

OUTPUT RANGE:
$0 \leq V_O \leq 25\ V$
$0 \leq I_O \leq 3\ A$

Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 volts.

D_6 protects both LM150s during an input short circuit.

FIGURE 20 – ADJUSTABLE CURRENT LIMITER


+25 V
Vin
LM150
Vout
R1
620
VO
IO
Adjust
R2
100
D1
IN4001
D2
IN4001
2N5640
VSS*

* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below −1.25 V.

$R_2 \geq \frac{V_{ref}}{I_{DSS}}$

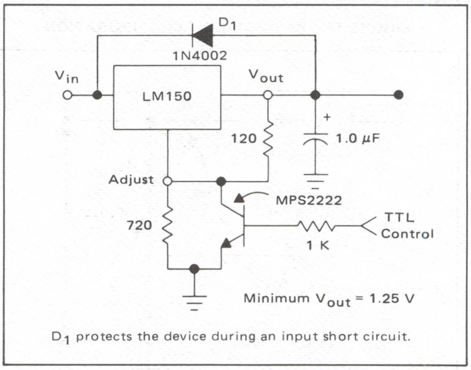
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < BV_{DSS} + 1.25\ V + V_{SS}$

$I_{Lmin} - I_{DSS} < I_O < 3\ A$

As shown $0 < I_O < 2\ A$

FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR


D1
1N4002
Vin
LM150
Vout
120
+
1.0 µF
Adjust
MPS2222
720
TTL
Control
1 K

Minimum $V_{out} = 1.25\ V$

D_1 protects the device during an input short circuit.

FIGURE 22 – SLOW TURN-ON REGULATOR

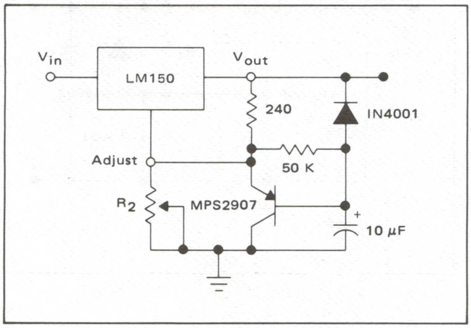
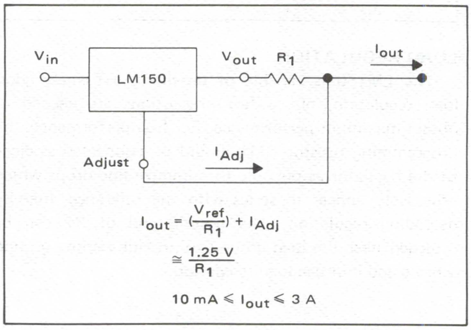

Vin
LM150
Vout
240
IN4001
Adjust
50 K
R2
MPS2907
+
10 µF

FIGURE 23 – CURRENT REGULATOR


Vin
LM150
Vout
R1
Iout
Adjust
IAdj

$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$10\ mA \leq I_{out} \leq 3\ A$

MOTOROLA

MC1463
MC1563

Specifications and Applications Information

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

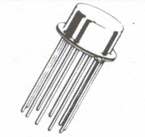
NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of −40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

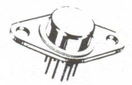
Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator.

- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance – 20 Milliohms typical
- High Power Capability – 9.0 Watts
- Excellent Temperature Stability – $\Delta V_O/\Delta T = \pm 0.002\%/^\circ C$ typical
- High Ripple Rejection – 0.002% typical
- 500 mA Current Capability

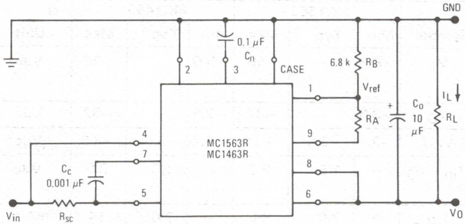


G SUFFIX
METAL PACKAGE
CASE 603-04



R SUFFIX
METAL PACKAGE
CASE 614-02

FIGURE 1 – TYPICAL CIRCUIT CONNECTION
$(|-3.5| \leqslant V_O \leqslant |-37|$ Vdc, $1 \leqslant I_L \leqslant 500$ mA)


GND
0.1 μF
C_n
2
3
CASE
6.8 k
R_B
1
V_{ref}
R_A
+
-
C_o
10
μF
I_L
R_L
4
7
9
MC1563R
MC1463R
C_c
0.001 μF
8
5
6
V_{in}
R_{sc}
V_O

Select R_A to Give Desired V_O: $R_A \approx (2|V_O|-7)$ kΩ $V_O \approx -3.5\left(1+\frac{R_A}{R_B}\right)$

FIGURE 2 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.2 Vdc, I_L = 10 Adc [max])

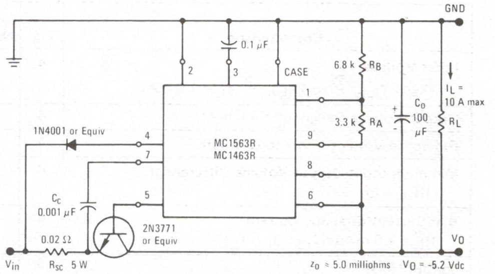
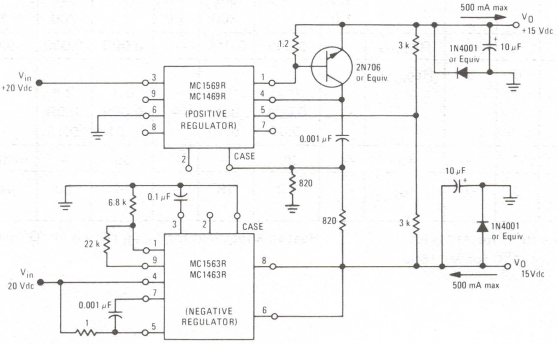

GND
0.1 μF
2
3
CASE
6.8 k
R_B
1
3.3 k
R_A
I_L = 10 A max
+
-
C_o
100
μF
R_L
1N4001 or Equiv
4
7
9
MC1563R
MC1463R
8
C_c
0.001 μF
5
6
2N3771 or Equiv
0.02 Ω
R_{sc} 5 W
V_{in}
V_O
z_o ≈ 5.0 milliohms
V_O = -5.2 Vdc

FIGURE 3 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR


500 mA max
V_O
+15 Vdc
1.2
3 k
1N4001 or Equiv
10 μF
+
2N706 or Equiv
V_{in}
+20 Vdc
3
9
6
8
MC1569R
MC1469R
(POSITIVE REGULATOR)
1
4
5
7
2
CASE
0.001 μF
820
10 μF
6.8 k
0.1 μF
3
2
CASE
820
3 k
1N4001 or Equiv
22 k
1
9
4
7
5
MC1563R
MC1463R
(NEGATIVE REGULATOR)
8
6
V_{in}
20 Vdc
0.001 μF
1
V_O
15Vdc
500 mA max

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC1463G	0° C to +70° C	Metal Can
MC1463R	0° C to +70° C	Metal Power
MC1563G	−55° C to +125° C	Metal Can
MC1563R	−55° C to +125° C	Metal Power

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage	V_I			Vdc
MC1463		−35		
MC1563		−40		
		G Package	R Package	
Load Current — Peak	I_L	250	600	mA
Current, Pin 2	I_2	10	10	mA
Power Dissipation and Thermal Characteristics				
T_A = 25°C	P_D	0.68	2.4	Watts
Derate above T_A = 25°C	$1/R_{\theta JA}$	5.44	16	mW/°C
Thermal Resistance, Junction to Air	$R_{\theta JA}$	184	62	°C/W
T_C = 25°C	P_D	1.8	9.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14.4	61	mW/°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	69.4	17	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Operating Ambient Temperature Range	T_A		°C
MC1463		0 to +70	
MC1563		-55 to +125	

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C, V_{in} = 15 V, V_O = 10 V unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1563			MC1463			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Voltage (T_A = T_{low} ① to T_{high} ② I_L = 1.0 mA)	4	1,6	V_I	−8.5	—	−40	−9.0	—	−35	Vdc
Output Voltage Range (I_L = 1.0 mA)	4	—	V_O	−3.6	—	−37	−3.8	—	−32	Vdc
Reference Voltage (Pin 1 to Ground)	4	—	V_{ref}	−3.4	−3.5	−3.6	−3.2	−3.5	−3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$\|V_{in} - V_O\|$	—	1.5	2.7	—	1.5	3.0	Vdc
Bias Current (Standby Current) (I_L = 1.0 mAdc, $I_{IB} = I_I - I_L$)	4	—	I_{IB}	—	7.0	11	—	7.0	14	mAdc
Output Noise (C_n = 0.1 µF, f = 10 Hz to 5.0 MHz)	4	—	v_N	—	120	—	—	120	—	µV(rms)
Temperature Coefficient of Output Voltage	4	3	$\Delta V_O/\Delta T$	—	±0.002	—	—	±0.002	—	%/°C
Operating Load Current Range	4	—	I_{LR}							mAdc
(R_{sc} = 0.3 ohm) R Package				1.0	—	500	1.0	—	500	
(R_{sc} = 2.0 ohms) G Package				1.0	—	200	1.0	—	200	
Input Regulation (V_{in} = 1.0 V rms, f = 1.0 kHz)	4	4	Reg_{line}	—	0.002	0.015	—	0.003	0.030	%/V_O
Load Regulation	6	5	Reg_{load}							
(T_J = Constant [1.0 mA $\leqslant I_L \leqslant$ 20 mA])				—	0.4	1.6	—	0.7	2.4	mV
(T_C = +25°C [1.0 mA $\leqslant I_L \leqslant$ 50 mA]) R Package				—	0.005	0.05	—	0.005	0.05	%
G Package				—	0.01	0.13	—	0.01	0.13	
Output Impedance (f = 1.0 kHz)	7	–	z_o	—	20	—	—	35	—	milliohms
Shutdown Current (V_I = -35 Vdc)	8	—	I_{sd}	—	7.0	15	—	14	50	µAdc

① T_{low} = 0°C for MC1463
= -55°C for MC1563

② T_{high} = +70°C for MC1463
= +125°C for MC1563

Heat sink required for T_{high} testing of "G" package.

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode.

Note 2. This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_I - V_O|$ as low as 2.7 Vdc and 3.0 Vdc respectively. **Typical units will regulate properly with $|V_I - V_O|$ as low** as 1.5 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\Delta V_O/\Delta T = \frac{\pm\,(V_O\text{ max} - V_O\text{ min})\ (100)}{\Delta\, T_A\,(V_O\ @\ T_A = +25^\circ C)}$$

where $\Delta\, T_A$ = +180°C for the MC1563
+75°C for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O\,(V_I)}\ 100\quad (\%/V_O).$$

where v_o is the change in the output voltage V_o for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$Reg_{in} = 0.015\%/V_O$$
$$V_O = 10\text{ Vdc}$$
$$v_{in} = 1.0\text{ V(rms)}$$

$$v_O = \frac{(Reg_{line})\ (V_I)\ (V_O)}{100}$$
$$= \frac{(0.015)(1.0)(10)}{100}$$
$$= 0.0015\text{ V(rms)}$$

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

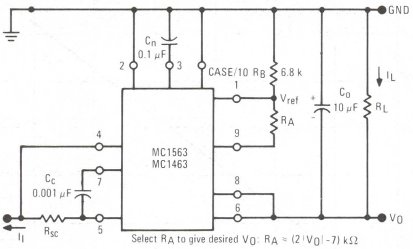
$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0\text{ mA}}| - V_O|_{I_L = 50\text{ mA}}|}{V_O|_{I_L = 1.0\text{ mA}}|} \times 100$$

Note 6. Not to exceed maximum package power dissipation.

TEST CIRCUITS

(I_L = 100 mAdc, T_C = +25°C unless otherwise noted.)

FIGURE 4 – GENERAL TEST CIRCUIT


GND
Cn
0.1 μF
2
3
CASE/10
RB
6.8 k
IL
1
Vref
Co
10 μF
RL
RA
4
9
MC1563
MC1463
Cc
0.001 μF
7
8
6
VI
II
Rsc
5
VO

Select R_A to give desired V_O: $R_A \approx (2|V_O| - 7)$ kΩ

FIGURE 5 – LOAD TRANSIENT RESPONSE

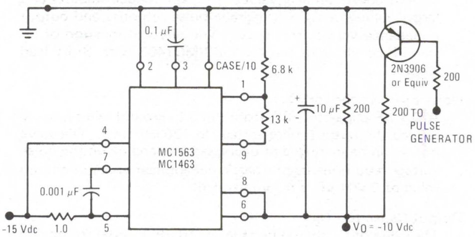

0.1 μF
2
3
CASE/10
6.8 k
2N3906
or Equiv
200
1
10 μF
200
200 TO
PULSE
GENERATOR
13 k
4
9
MC1563
MC1463
7
8
0.001 μF
6
VI = -15 Vdc
1.0
5
VO = -10 Vdc

FIGURE 6 – LOAD REGULATION

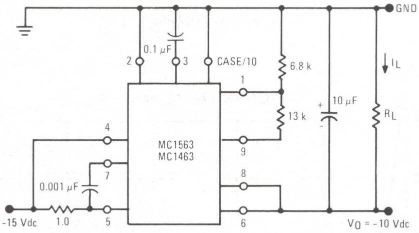

GND
0.1 μF
2
3
CASE/10
6.8 k
IL
1
10 μF
13 k
RL
4
MC1563
MC1463
9
8
7
0.001 μF
VI = -15 Vdc
1.0
5
6
VO = -10 Vdc

FIGURE 7 – OUTPUT IMPEDANCE

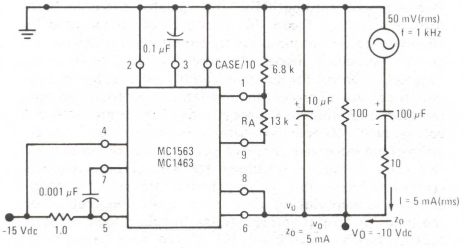
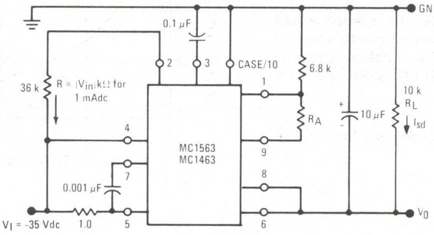

50 mV(rms)
f = 1 kHz
0.1 μF
2
3
CASE/10
6.8 k
1
10 μF
100
100 μF
RA
13 k
4
MC1563
MC1463
9
10
7
8
0.001 μF
I = 5 mA(rms)
vo
zo
VI = -15 Vdc
1.0
5
6
zo = vo / 5 mA
VO = -10 Vdc

FIGURE 8 – SHUTDOWN CURRENT


GND
0.1 μF
2
3
CASE/10
6.8 k
36 k
R ≈ |Vin| kΩ for
1 mAdc
1
10 k
RL
RA
10 μF
Isd
4
MC1563
MC1463
9
7
8
0.001 μF
VI = -35 Vdc
1.0
5
6
VO

GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) Output Voltage is set by resistors R_A and R_B (see Figure 9). Set R_B = 6.8 k ohms and determine R_A from the graph of Figure 11 or from the equation:

   $$R_A \approx (2\,|V_O| - 7)\ k\Omega$$

   b) Output voltage can be varied by making R_A adjustable as shown in Figures 9 and 10.

   c) Output voltage, V_O, is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.

   d) $V_O = V_{ref}\left(1 + \frac{R_A}{R_B}\right)$; therefore the tolerance on output voltage is determined by the tolerance of V_{ref} and R_A and R_B.

2. Short-Circuit Current, I_{SC}
   Short-Circuit Current, I_{SC} is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 11 when using the typical circuit connection of Figure 9. See Figure 27 for current limiting during NPN current boost.

3. Compensation, C_c
   A 0.001 µF capacitor (C_c, see Figure 9), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1563/MC1463 with short lead lengths.

4. Noise Filter Capacitor, C_n
   A 0.1 µF capacitor, C_n, from Pin 3 to ground will typically reduce the output noise voltage to 120 µV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 µF is recommended.

5. Output Capacitor, C_O
   The value of C_O should be at least 10 µF in order to provide good stability.

6. Shutdown Control
   One method of turning "OFF" the regulator is to draw 1 mA from Pin 2 (See Figure 8). This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shutdown for high junction temperatures (see Figure 35). This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard logic levels of MECL, MRTL, MDTL or MTTL can also be used to turn the regulator "ON" or "OFF" (see Figures 30 and 31).

7. Remote Sensing
   The connection to Pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_O can be greatly reduced (see Figure 33).

MECL, MDTL, MRTL, and MTTL are Trademarks of Motorola Inc.

FIGURE 9 – TYPICAL CIRCUIT CONNECTION

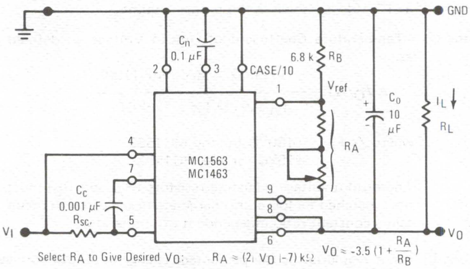


FIGURE 10 – R_A versus V_O

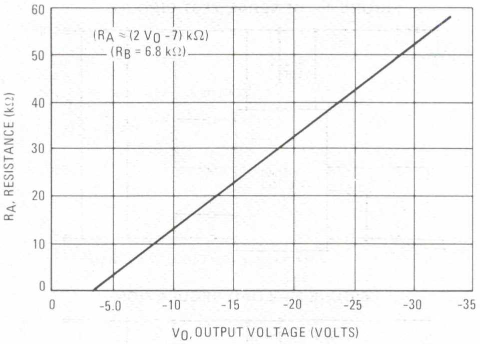
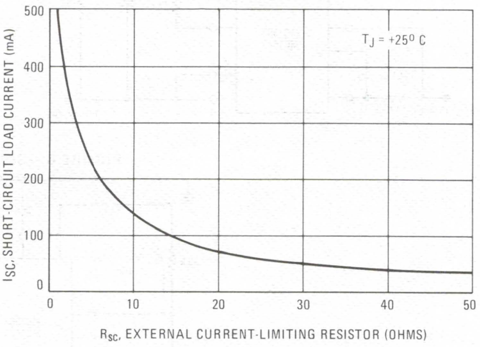


FIGURE 11 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\,\mu F$, $C_c = 0.001\,\mu F$, $C_o = 10\,\mu F$, $T_C = +25^{\circ}C$,
$V_{I(nom)} = -15$ Vdc, $V_{O(nom)} = -10$ Vdc, $I_L = 100$ mAdc.

FIGURE 12 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

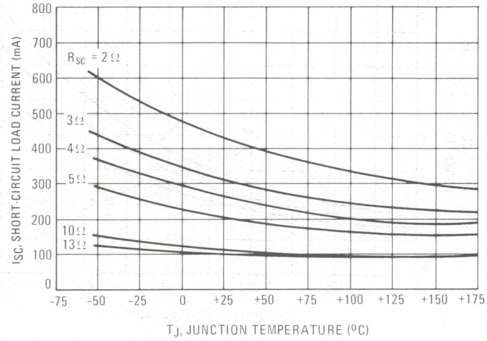


FIGURE 13 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

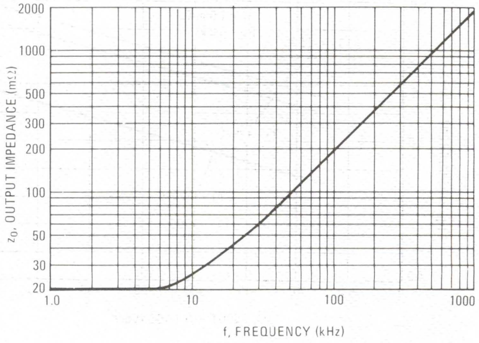


FIGURE 14 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

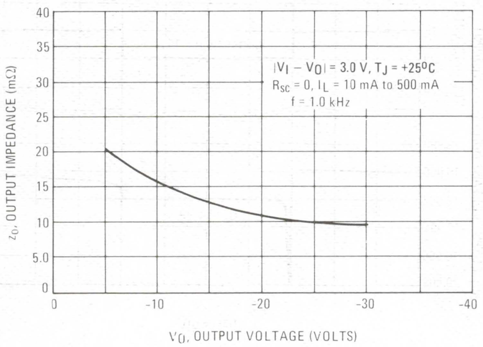


FIGURE 15 – OUTPUT IMPEDANCE versus R_{SC}

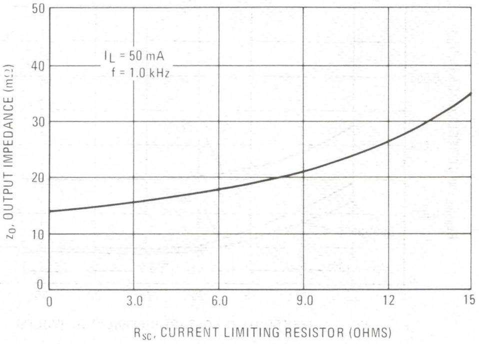
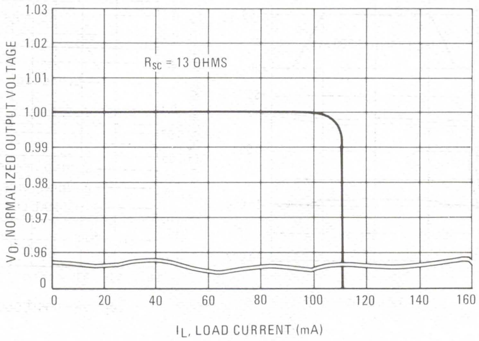


FIGURE 16 – CURRENT LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 17 – BIAS CURRENT versus INPUT VOLTAGE

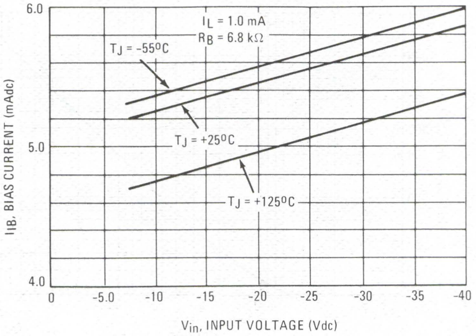


FIGURE 18 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

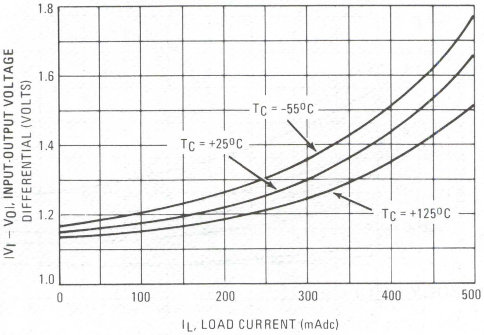


FIGURE 19 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

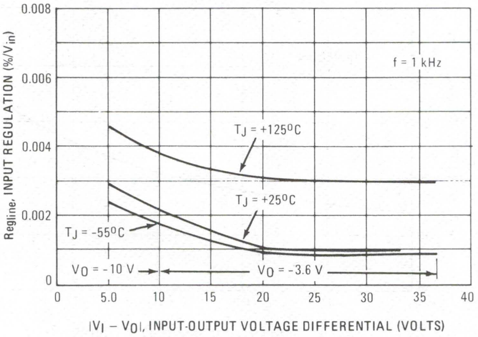


FIGURE 20 – INPUT TRANSIENT RESPONSE

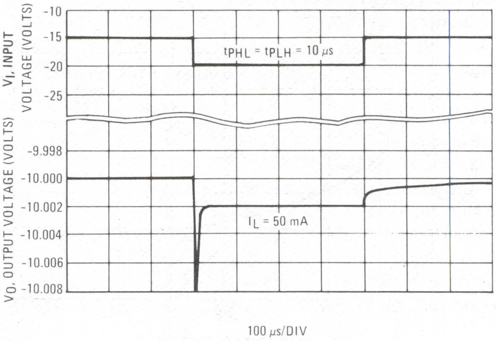


FIGURE 21 – LOAD TRANSIENT RESPONSE

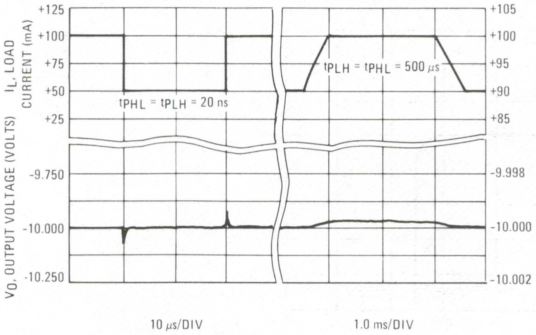
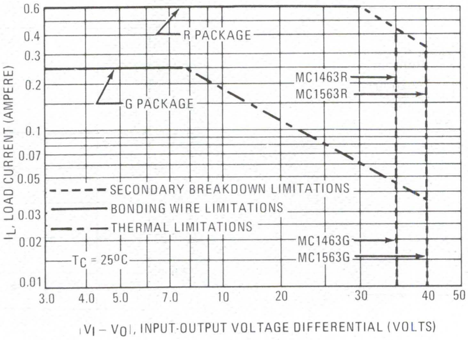


FIGURE 22 – DC OPERATING AREA



OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1563 (MC1463) negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE INDEX

	Specification Pg. No.		Specification Pg. No.
Theory of Operation	7	Remote Sensing	12
NPN Current Boosting	9	An Adjustable Zero-Temperature-Coefficient Voltage Source	13
PNP Current Boosting	10	Thermal Shutdown	13
Positive and Negative Power Supplies	11	Thermal Considerations	13
Shutdown Techniques	11	PC Board Layout and Information	15
Voltage Boosting	12		

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 23, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 24. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

FIGURE 23 — SERIES VOLTAGE REGULATOR

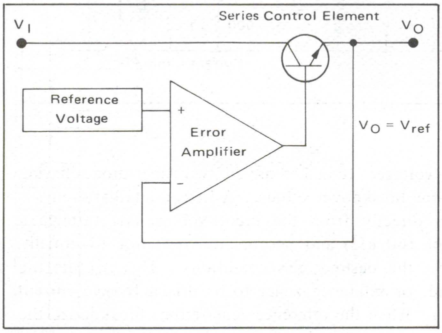


FIGURE 24 — THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

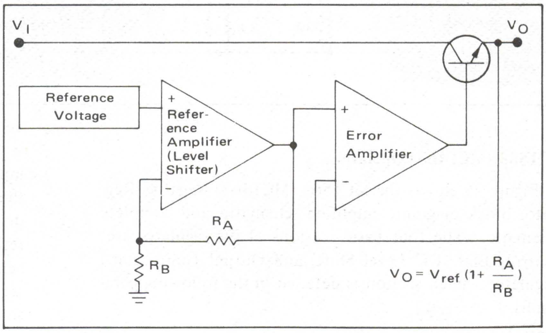
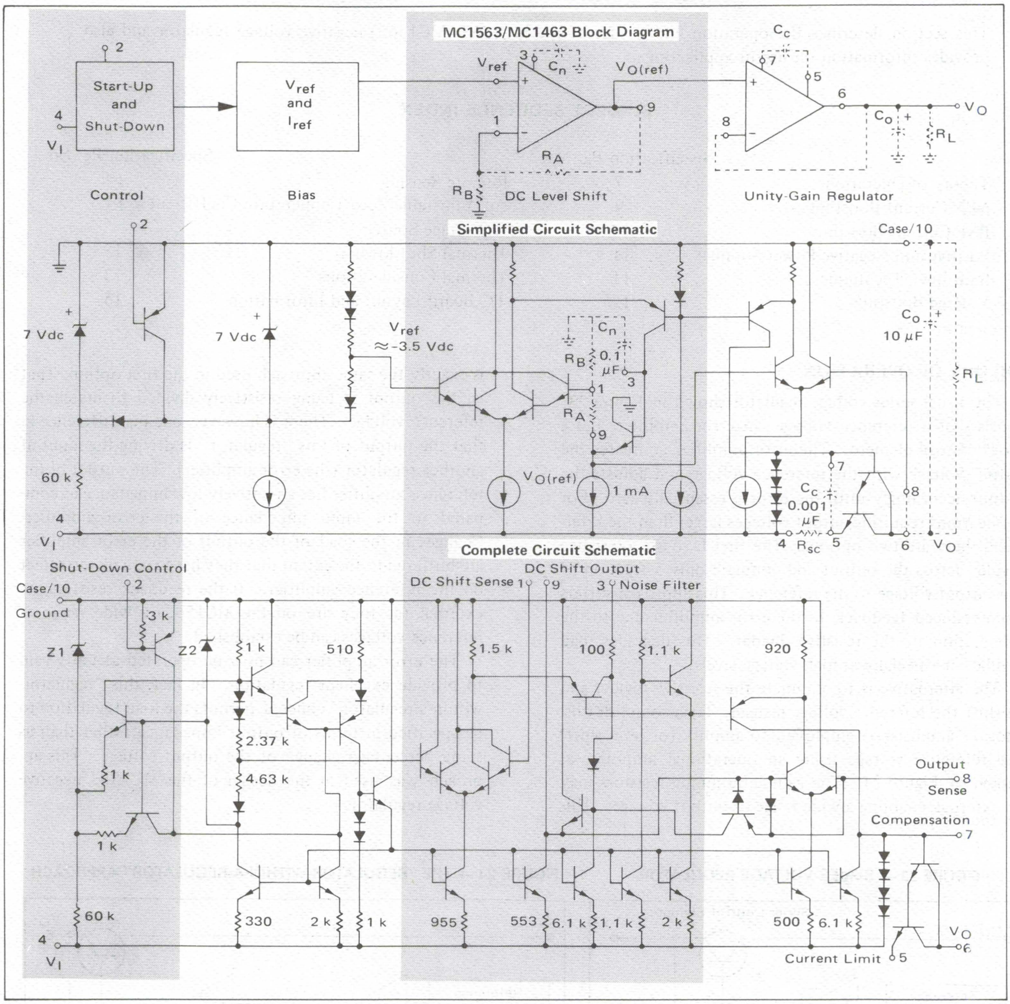

V_I
V_O
Reference Voltage
+
Reference Amplifier (Level Shifter)
−
+
Error Amplifier
−
R_A
R_B
$V_O = V_{ref}(1 + \frac{R_A}{R_B})$

FIGURE 25
(Recommended External Circuitry is Depicted With Dotted Lines.)


MC1563/MC1463 Block Diagram
2
Start-Up and Shut-Down
4
V_I
Control
V_{ref} and I_{ref}
Bias
V_{ref}
3
C_n
$V_{O(ref)}$
+
-
1
9
R_A
R_B
DC Level Shift
C_C
7
5
6
8
V_O
C_O
R_L
Unity-Gain Regulator
Simplified Circuit Schematic
Case/10
+
7 Vdc
V_{ref}
≈-3.5 Vdc
C_n
R_B
0.1 μF
3
1
R_A
9
60 k
$V_{O(ref)}$
1 mA
7
C_C
0.001 μF
8
4 R_{sc} 5
6 V_O
C_O
10 μF
R_L
Complete Circuit Schematic
Shut-Down Control
Case/10
Ground
Z1
3 k
Z2
1 k
510
2.37 k
1 k
4.63 k
1 k
60 k
DC Shift Sense 1
DC Shift Output 9
3 Noise Filter
1.5 k
100
1.1 k
920
Output Sense 8
Compensation 7
330
2 k
1 k
955
553
6.1 k
1.1 k
2 k
500
6.1 k
V_O 6
Current Limit 5

MC1563 (MC1463) Operation

Figure 25 shows the MC1563 (MC1463) Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via Pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via Pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (Pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (Pin 7) and Pin 5. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 21). It is also necessary to use an output capacitor, C_O, (typically 10 μF) directly from the output (Pin 6) to ground. When an external transistor is used to boost the current, $C_O = 100\ \mu$F is recommended (see Figure 26).

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 26, are recommended. The circuit shown in Figure 26 can supply up to approximately 4.0 amperes (subject to safe area limitations). At higher currents the V_{BE} of the pass transistor may itself exceed the threshold of the current limit even for $R_{SC} = 0$. Figure 2 illustrates the use of an additional external diode from Pin 4 for higher current operation or for pass transistors exhibiting higher V_{BE}'s. It will probably be necessary to determine R_{SC} experimentally for each case where a pass transistor is used because V_{BE} varies from device to device.

The circuit of Figure 26 when set up for a -10 V output

FIGURE 26 — TYPICAL NPN CURRENT BOOST CONNECTION

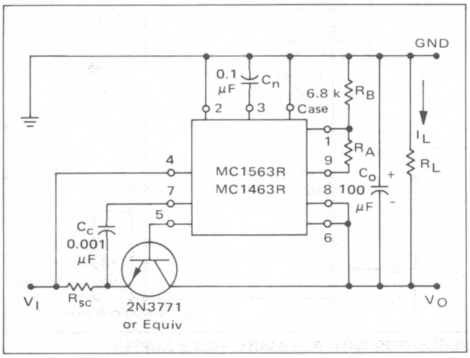
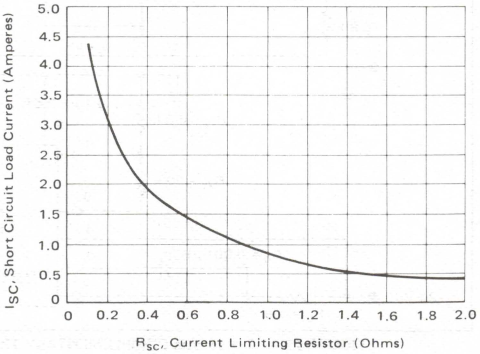


FIGURE 27 — I_{SC} versus R_{SC} (REFERENCE FIGURE 26)



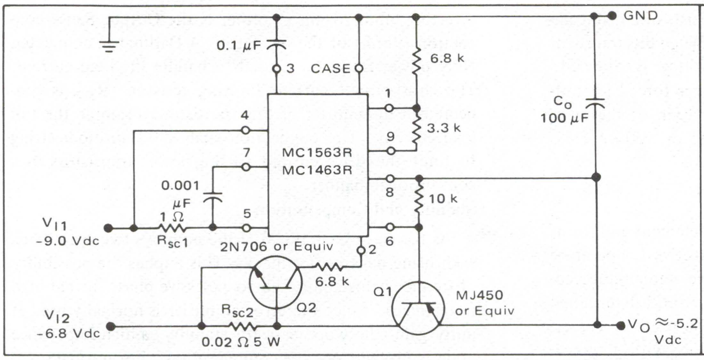

GND
0.1 µF
3
CASE
6.8 k
1
4
9
3.3 k
7
MC1563R
MC1463R
8
10 k
0.001 µF
1 Ω
5
V_{I1}
-9.0 Vdc
R_{sc1}
2N706 or Equiv
2
6
6.8 k
Q1
MJ450 or Equiv
V_{I2}
-6.8 Vdc
R_{sc2}
Q2
0.02 Ω 5 W
C_O
100 µF
V_O ≈ -5.2 Vdc

FIGURE 28 — PNP CURRENT BOOST CONNECTION

(R_A = 13 kΩ) supply and operating with a - 15 V input, with a R_{SC} of 0.1 Ω, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A. This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 27 indicates how the short circuit current varies with the value of R_{SC} for this circuit.

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 28, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 28 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 500 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 20 at 10 amperes, thus requiring only 500 mA from the MC1563R. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to Pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 11). Transistor Q2 and R_{SC2} will not be required and Pin 2 should be returned to ground.

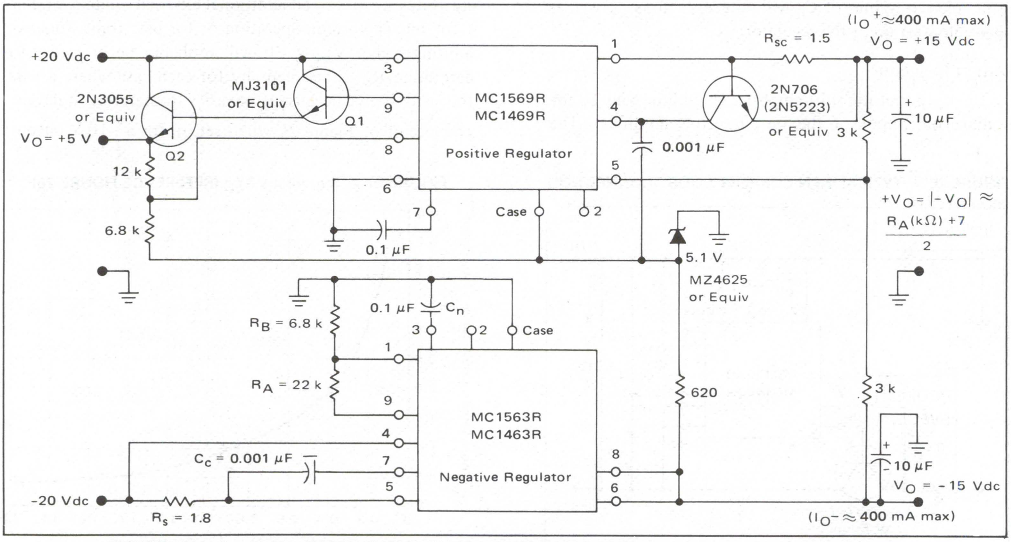
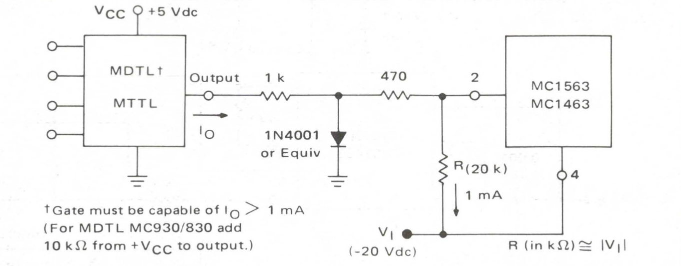

+20 Vdc
2N3055 or Equiv
V_O = +5 V
Q2
12 k
6.8 k
MJ3101 or Equiv
Q1
3
9
8
6
7
0.1 µF
MC1569R
MC1469R
Positive Regulator
Case
2
1
4
5
R_{SC} = 1.5
(I_O^+ ≈ 400 mA max)
V_O = +15 Vdc
2N706 (2N5223) or Equiv
3 k
10 µF
0.001 µF
$+V_O = |-V_O| \approx \frac{R_A(k\Omega) + 7}{2}$
5.1 V
MZ4625 or Equiv
R_B = 6.8 k
0.1 µF
C_n
3
2
Case
1
R_A = 22 k
9
4
7
5
MC1563R
MC1463R
Negative Regulator
C_c = 0.001 µF
8
6
620
3 k
10 µF
V_O = - 15 Vdc
-20 Vdc
R_s = 1.8
(I_O^- ≈ 400 mA max)

FIGURE 29 — A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY



†Gate must be capable of $I_O > 1$ mA
(For MDTL MC930/830 add
10 kΩ from $+V_{CC}$ to output.)

FIGURE 30 — SATURATED LOGIC LEVEL SHUTDOWN CIRCUIT

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance. When used in this manner a silicon diode such as the 1N4001 must be connected as a clamp on the output with the cathode to ground and the anode to the negative output voltage. This is to prevent the positive voltage in the system from forcing the output to a positive value and preventing the MC1563 from starting up.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 29 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (Pin 6 of the MC1569) and using the other side (Pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at Pin 5 will be zero. When the voltage at pin 5 equals zero, $+|V_O|$ must equal $-|V_O|$.

For the configuration shown in Figure 29, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The -15-volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300-mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged. See MC1561 data sheet or MC1569 data sheet for information concerning latch-up when using plus and minus regulations.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor; which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor ($V_{in}/60$ kΩ). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

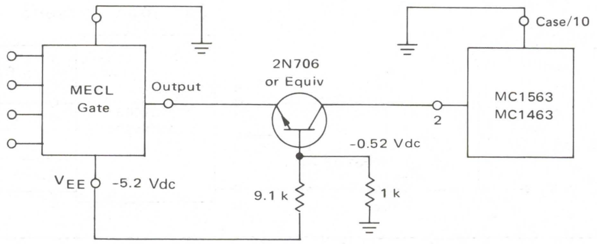


FIGURE 31 — MECL LOGIC LEVEL SHUTDOWN CIRCUIT

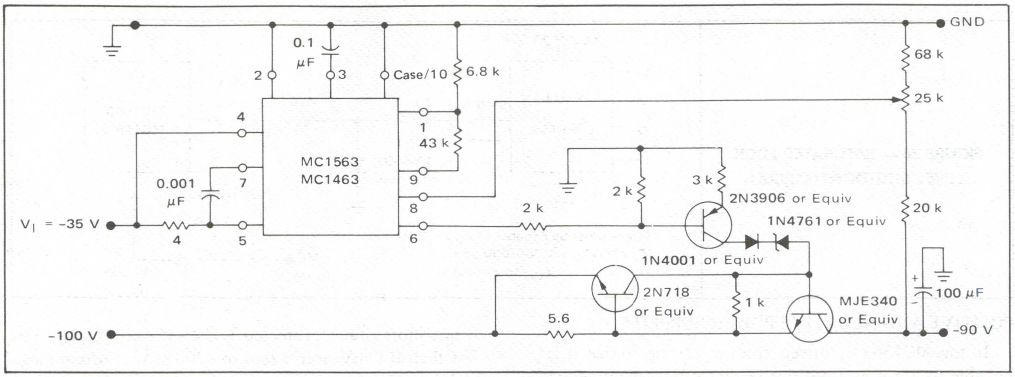

GND
0.1 µF
2
3
Case/10
6.8 k
68 k
25 k
4
1
43 k
MC1563
MC1463
0.001 µF
7
9
8
6
5
4
V_I = -35 V
2 k
2 k
3 k
2N3906 or Equiv
1N4761 or Equiv
20 k
1N4001 or Equiv
2N718 or Equiv
1 k
MJE340 or Equiv
100 µF
5.6
-100 V
-90 V

FIGURE 32 — VOLTAGE BOOSTING CIRCUIT

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 30 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 31.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (Pin 4),
2. the output voltage (Pin 6) and,
3. the output sense lead (Pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 32 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistances of the interconnecting lines (V_{EE} and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 33 shows how remote sensing is accomplished using both a separate sense line from Pin 8 and a separate ground line from the regulator to the remote load.

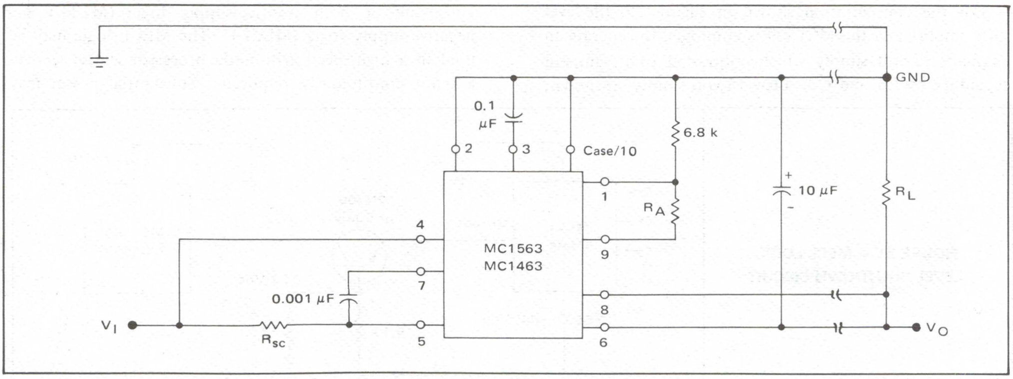

GND
0.1 µF
2
3
Case/10
6.8 k
1
R_A
10 µF
R_L
4
MC1563
MC1463
9
7
0.001 µF
8
V_I
R_SC
5
6
V_O

FIGURE 33 — REMOTE SENSING CIRCUIT

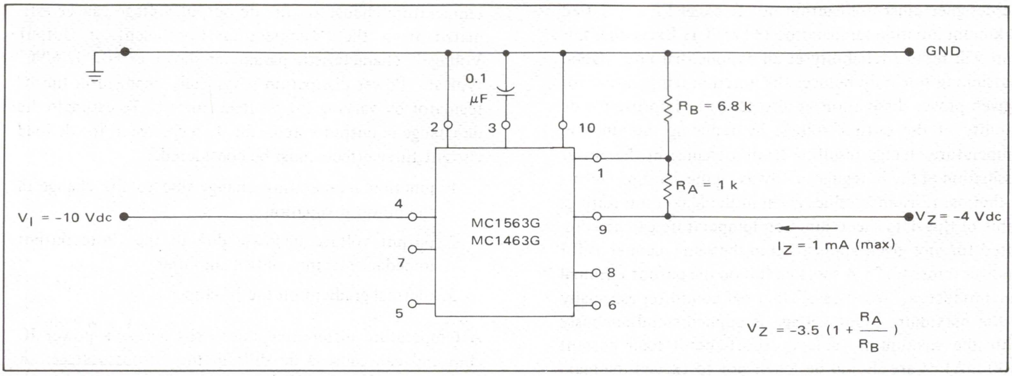


FIGURE 34 — AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then Pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R_A and R_B, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 34)

THERMAL SHUTDOWN

By setting a fixed voltage at Pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x 10^{-3}V/°C). By setting -0.61 Vdc externally, at Pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 35 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 36. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

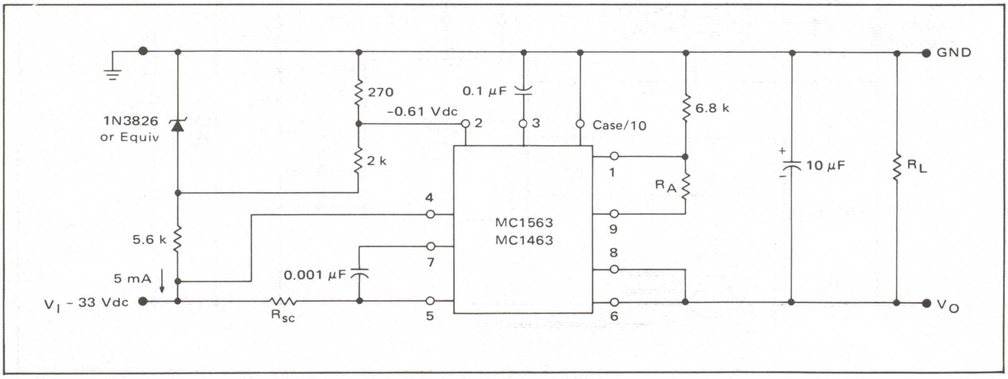


FIGURE 35 — JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

the designer must use caution not to exceed the specified maximum junction temperature (+175°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 22).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically +0.03%/watt for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563R

with $V_I = -10$ Vdc

$V_O = -5$ Vdc

and $I_L = 100$ mA to 200 mA

($\Delta I_L = 100$ mA)

assume $T_A = +25°C$

TO-66 Type Case with heatsink

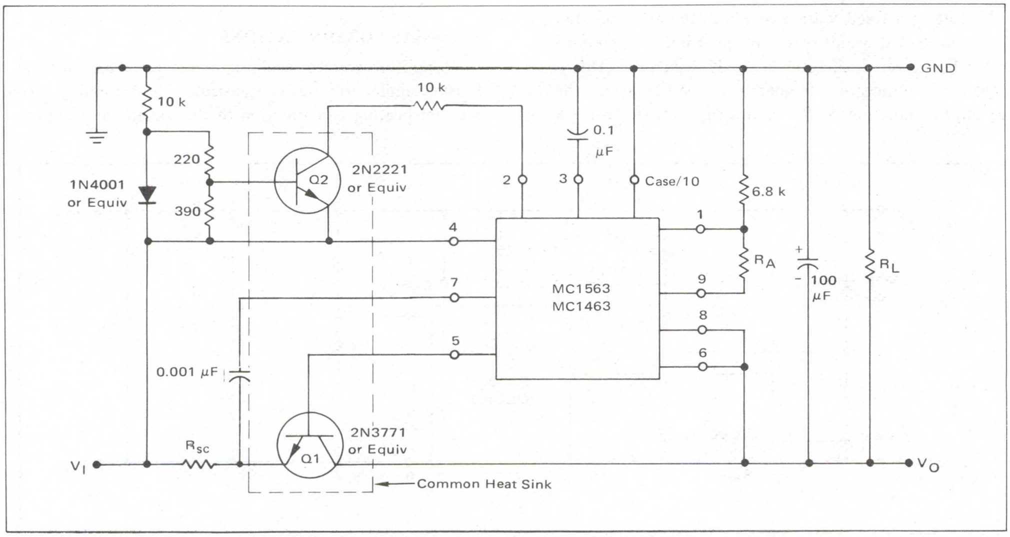


FIGURE 36 — THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

assume $R_{\theta CS} = 0.2^{\circ}C/W$

---

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

and $R_{\theta SA} = 2^{\circ}C/W$

It is desired to find the $\triangle V_O$ which results from this $\triangle I_L$. Each of the three previously stated effects on V_O can now be separately considered.

1. $\triangle V_O$ due to $\triangle T_J$

$$\triangle V_O = (V_O)(\triangle P_D)(\Delta V_O/\Delta T)(R_{\theta JC}+R_{\theta CS}+R_{\theta SA})$$

OR

$$\triangle V_O = (5\text{ V})(5\text{ V} \times 0.1\text{ A})(\pm 0.002\%/^{\circ}C)(19.2^{\circ}C/W)$$

$$\triangle V_O \approx \pm 1.0\text{ mW}$$

2. $\triangle V_O$ due to z_o

$$|\triangle V_O| = (-z_o)(I_L)$$

$$|\triangle V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\text{ mV}$$

3. $\triangle V_O$ due to gradient coefficient, $\Delta V_O/\Delta G$

$$|\Delta V_O| = (\Delta V_O/\Delta G)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (+3 \times 10^{-4}/W)(5\text{ volts})(5 \times 10^{-1}W)$$

$$|\Delta V_O| = +0.8\text{ mV}$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\text{ total}| = \pm 1.0 - 2.0 + 0.8\text{ mV}$$

OR

$$-2.2\text{ mV} \leqslant |V_O\text{ total}| \leqslant -0.2\text{ mV}$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

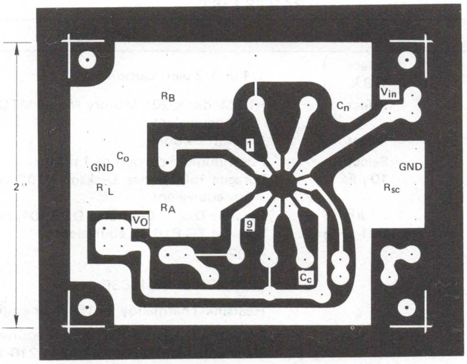
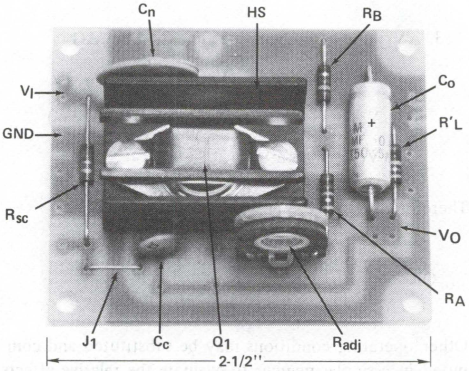


FIGURE 37 — LOCATION OF COMPONENTS



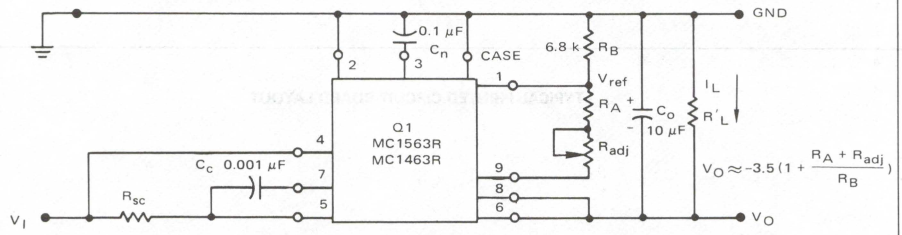
Note 1:
When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj}.

Note 2:
Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{sc}.

Note 3:
If Pin 2 is used to shut down the regulator, remove the copper which shorts Pin 2 to ground.

Note 4:
Remote sensing can be achieved by removing the copper which shorts Pin 8 to Pin 6 and connecting Pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal.

TYPICAL CIRCUIT CONNECTION FOR OUTPUT VOLTAGES BETWEEN −3.5 AND −37 VOLTS



$$V_O \approx -3.5\left(1 + \frac{R_A + R_{adj}}{R_B}\right)$$

Select $R_A + R_{adj}$ to Give Desired V_O: $R_A + R_{adj} \approx (2|V_O| - 7)$ kΩ with $R_B = 6.8$ kΩ

PARTS LIST

Component	Value	Description
R_A	Select	1/4 or 1/2 watt carbon
R_B	6.8 k	
R_{adj}	Select	IRC Model X-201, Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
R'_L	Select	For minimum current of 1 mAdc
C_o	10 µF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n	0.1 µF	Ceramic Disc — Centralab DDA104, or equivalent
C_C	0.001 µF	Sprague TG-P10, or equivalent
J_1		Jumper
Q1		MC1563R or MC1463R
*HS		Heatsink Thermalloy #6168B or equivalent
*Socket	(Not Shown)	Robinson Nugent #0001306 or equivalent Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 or equivalent
PC Board		Circuit DOT, Inc. #PC1113 or equivalent 1155 W. 23rd St. Tempe, Arizona 85281

*Optional

MOTOROLA

MC1466L
MC1566L

Specifications and Applications Information

MONOLITHIC VOLTAGE AND CURRENT REGULATOR

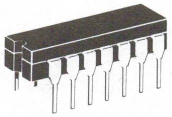
This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.02% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

CERAMIC PACKAGE
CASE 632-02
MO-001AA

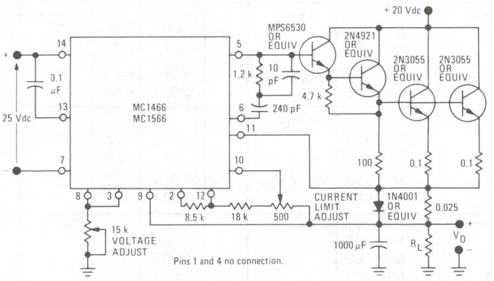


ORDERING INFORMATION

Device	Temperature Range	Package
MC1466L	0°C to +70° C	Ceramic DIP
MC1566L	−55°C to +125°C	Ceramic DIP

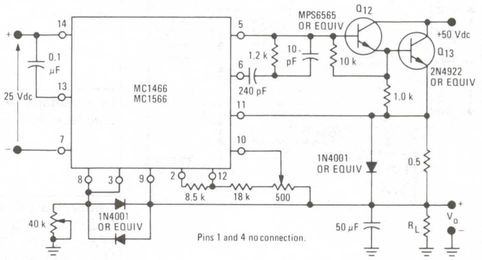
TYPICAL APPLICATIONS

FIGURE 1 — 0-TO-15 VDC, 10-AMPERES REGULATOR


+ 20 Vdc
MPS6530 OR EQUIV
2N4921 OR EQUIV
2N3055 OR EQUIV
2N3055 OR EQUIV
MC1466
MC1566
25 Vdc
0.1 μF
1.2 k
10 pF
240 pF
4.7 k
100
0.1
0.1
0.025
1N4001 OR EQUIV
CURRENT LIMIT ADJUST
8.5 k
18 k
500
15 k VOLTAGE ADJUST
1000 μF
R_L
V_O
14
13
7
5
6
11
10
8
3
9
2
12

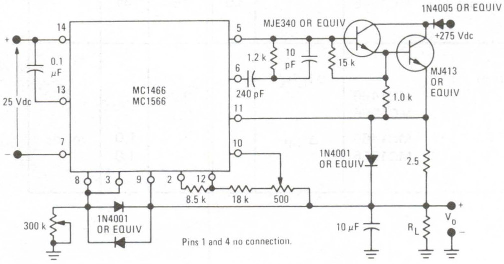
Pins 1 and 4 no connection.

FIGURE 2 — 0-TO-40 VDC, 0.5-AMPERE REGULATOR


MPS6565 OR EQUIV
Q12
+50 Vdc
Q13
2N4922 OR EQUIV
MC1466
MC1566
25 Vdc
0.1 μF
1.2 k
10 pF
10 k
240 pF
1.0 k
1N4001 OR EQUIV
0.5
8.5 k
18 k
500
40 k
1N4001 OR EQUIV
50 μF
R_L
V_O
14
13
7
5
6
11
10
8
3
9
2
12

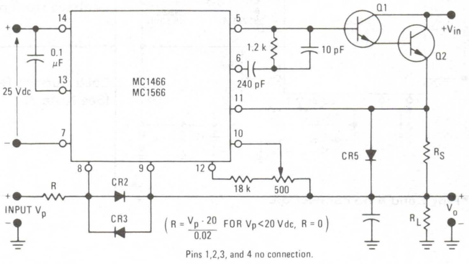
Pins 1 and 4 no connection.

FIGURE 3 — 0-TO-250 VDC, 0.1-AMPERE REGULATOR


1N4005 OR EQUIV
MJE340 OR EQUIV
+275 Vdc
MJ413 OR EQUIV
MC1466
MC1566
25 Vdc
0.1 μF
1.2 k
10 pF
15 k
240 pF
1.0 k
1N4001 OR EQUIV
2.5
8.5 k
18 k
500
300 k
1N4001 OR EQUIV
10 μF
R_L
V_O
14
13
7
5
6
11
10
8
3
9
2
12

Pins 1 and 4 no connection.

FIGURE 4 — REMOTE PROGRAMMING


Q1
Q2
$+V_{in}$
MC1466
MC1566
25 Vdc
0.1 μF
1.2 k
10 pF
240 pF
CR5
R_S
18 k
500
R
INPUT V_p
CR2
CR3
R_L
V_O
14
13
7
5
6
11
10
8
9
12

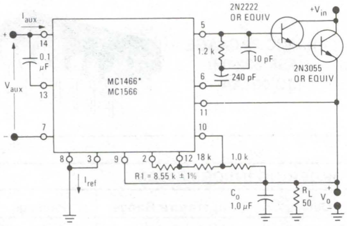
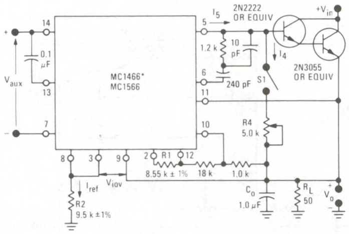
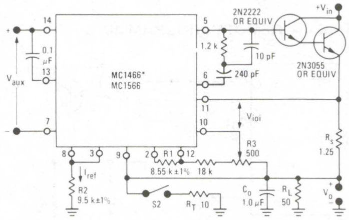
$\left(R = \frac{V_p - 20}{0.02} \text{ FOR } V_p < 20\text{ Vdc, } R = 0\right)$

Pins 1,2,3, and 4 no connection.

MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

Rating		Symbol	Value	Unit
Auxiliary Voltage		V_{aux}		Vdc
	MC1466		30	
	MC1566		35	
Power Dissipation (Package Limitation)		P_D	750	mW
Derate above T_A = +50°C		$1/\theta_{JA}$	6.0	mW/°C
Operating Temperature Range		T_A		°C
	MC1466		0 to +70	
	MC1566		−55 to +125	
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic		Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2)		V_{aux}				Vdc
	(Voltage from pin 14 to pin 7)	MC1466		21	–	30	
		MC1566		20	–	35	
	Auxiliary Current		I_{aux}				mAdc
		MC1466		–	9.0	12	
		MC1566		–	7.0	10	
	Internal Reference Voltage		V_{IR}				Vdc
	(Voltage from pin 12 to pin 7)	MC1466		17.3	18.2	19.7	
		MC1566		17.5	18.2	19	
	Reference Current (See Note 3)		I_{ref}				mAdc
		MC1466		0.8	1.0	1.2	
		MC1566		0.9	1.0	1.1	
	Input Current-Pin 8		I_8				µAdc
		MC1466		–	6.0	12	
		MC1566		–	3.0	8.0	
	Power Dissipation		P_D				mW
		MC1466		–	–	360	
		MC1566		–	–	300	
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)		V_{iov}				mVdc
		MC1466		0	15	40	
		MC1566		3.0	15	35	
	Load Voltage Regulation (See Note 5)		ΔV_{iov}				
		MC1466		–	1.0	3.0	mV
		MC1566		–	0.7	1.0	
		MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
		MC1566		–	0.004	0.01	
	Line Voltage Regulation (See Note 6)		ΔV_{iov}				
		MC1466		–	1.0	3.0	mV
		MC1566		–	0.7	2.0	
		MC1466	$\Delta V_{ref}/V_{ref}$	–	0.015	0.03	%
		MC1566		–	0.004	0.02	
	Temperature Coefficient of Output Voltage		TC_{V_o}				%/°C
	(T_A = 0 to +75°C)	MC1466		–	0.01	–	
	(T_A = −55 to +25°C)	MC1566		–	0.006	–	
	(T_A = +25 to +125°C)	MC1566		–	0.004	–	
	Input Offset Voltage, Current Control Amplifier (See Note 4)		V_{ioi}				mVdc
	(Voltage from pin 10 to pin 11)	MC1466		0	15	40	
		MC1566		3.0	15	35	
	Load Current Regulation (See Note 7)		$\Delta I_L/I_L$				
		MC1466		–	0.2	–	%
		MC1566		–	0.1	–	
		MC1466	ΔI_{ref}	–	–	1.0	mAdc
		MC1566		–	–	1.0	

*Pins 1 and 4 no connection.

NOTE 1:

The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 **volts** for the MC1466 or 35 **volts** for the MC1566. The instantaneous value of V_{aux} must be greater than 20 **volts** for the MC1566 or 21 **volts** for the MC1466 for proper internal regulation.

NOTE 2:

The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3:

Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\,(mA) = \frac{8.55}{R_1\,(k\Omega)}\,.$$

NOTE 4:

A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:

Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open ($I_4 = 0$) measure the value of $V_{iov}\,(1)$ and $V_{ref}\,(1)$

b. Close S1, adjust R4 so that $I_4 = 500\ \mu A$ and note $V_{iov}\,(2)$ and $V_{ref}\,(2)$.

Then $\Delta V_{iov} = V_{iov}\,(1) - V_{iov}\,(2)$

% Reference Regulation =

$$\frac{[V_{ref}\,(1) - V_{ref}\,(2)]}{V_{ref}\,(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\,.$$

NOTE 6:

Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see note 5). The measurement procedure is:

a. **Set the auxiliary voltage, V_{aux}, to 22 volts for the MC1566 or the MC1466. Read the value of $V_{iov\,(1)}$ and $V_{ref\,(1)}$.**

b. **Change the V_{aux} to 28 volts for the MC1566 or the MC1466 and note the value of $V_{iov\,(2)}$ and $V_{ref(2)}$. Then compute Line Voltage Regulation:**

$$\Delta V_{iov} = \Delta V_{iov}\,(1) - V_{iov}\,(2)$$

% Reference Regulation =

$$\frac{[V_{ref}\,(1) - V_{ref}\,(2)]}{V_{ref}\,(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\,.$$

NOTE 7:

Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_o is 8.0 Vdc.

b. With S2 closed, adjust R_T for $V_o = 1.0$ Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\,(100\%) + I_{ref}$$

where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S.

FIGURE 5

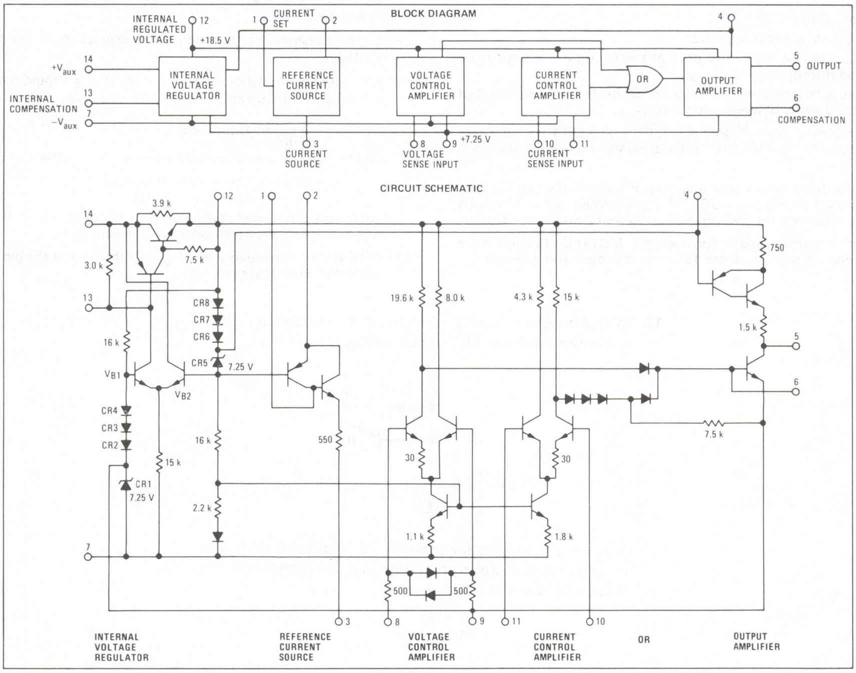
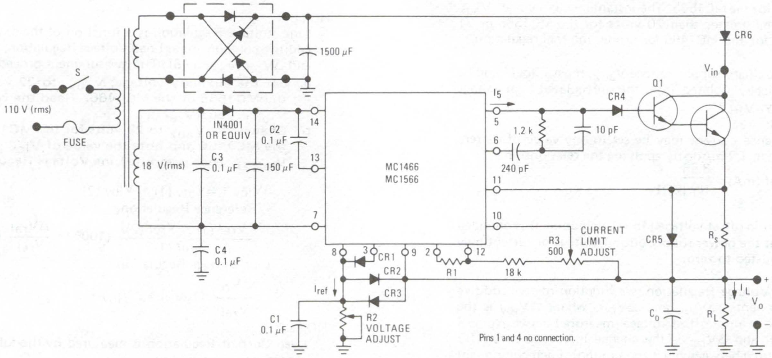

BLOCK DIAGRAM
INTERNAL REGULATED VOLTAGE
12
+18.5 V
1
CURRENT SET
2
4
+Vaux
14
INTERNAL COMPENSATION
13
7
−Vaux
INTERNAL VOLTAGE REGULATOR
REFERENCE CURRENT SOURCE
VOLTAGE CONTROL AMPLIFIER
CURRENT CONTROL AMPLIFIER
OR
OUTPUT AMPLIFIER
5
OUTPUT
6
COMPENSATION
3
CURRENT SOURCE
8
9
+7.25 V
VOLTAGE SENSE INPUT
10
11
CURRENT SENSE INPUT
CIRCUIT SCHEMATIC
3.9 k
7.5 k
3.0 k
CR8
CR7
CR6
CR5
7.25 V
16 k
VB1
VB2
CR4
CR3
CR2
15 k
CR1
7.25 V
16 k
2.2 k
550
19.6 k
8.0 k
4.3 k
15 k
30
30
1.1 k
1.8 k
500
500
750
1.5 k
7.5 k
INTERNAL VOLTAGE REGULATOR
REFERENCE CURRENT SOURCE
VOLTAGE CONTROL AMPLIFIER
CURRENT CONTROL AMPLIFIER
OR
OUTPUT AMPLIFIER

FIGURE 6 — TYPICAL CIRCUIT CONNECTION



Pins 1 and 4 no connection.

NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:

   For constant voltage operation, output voltage V_o is given by:

   $V_o = (I_{ref})\ (R_2)$

   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.

   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:

   $$I_{ref} = \frac{8.5}{R_1}$$

   where R1 is the resistance between pins 2 and 12.

2. Constant Current:

   For constant current operation:

   (a) Select R_s for a 250 mV drop at the maximum desired regulated output current, I_{max}.

   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.

3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.

4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.

5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.

6. The RC network (10 pF, 240 pF, 1.2 kΩ) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.

7. For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.

8. C_o may be selected by using the relationship:

   $C_o = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.

9. C2 is necessary for the internal compensation of the MC1466/MC1566.

10. For optimum regulation, current out of Pin 5, I_5 should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:

    $$\frac{I_{max}}{\beta 1 \beta 2} \leqslant 0.5 \text{ mAdc}$$

    where: I_{max} = maximum short-circuit load current (mAdc)

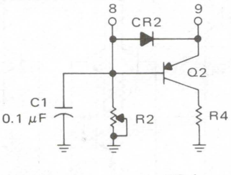
    $\beta 1$ = minimum beta of Q1

    $\beta 2$ = minimum beta of Q2

    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.

11. CR6 is recommended when $V_o > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_o$.

12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_o. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$V_{(BR)CEO} \text{ of Q2} \geq V_o$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current-Mode Indicator

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2\ (V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_o. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

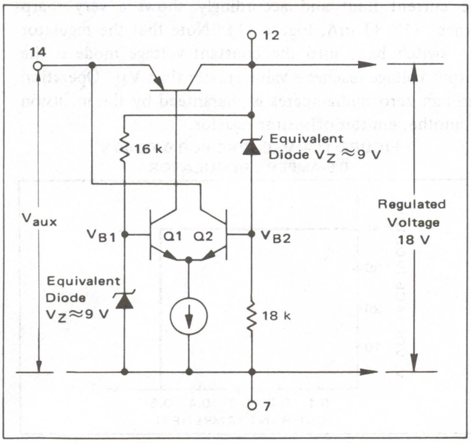
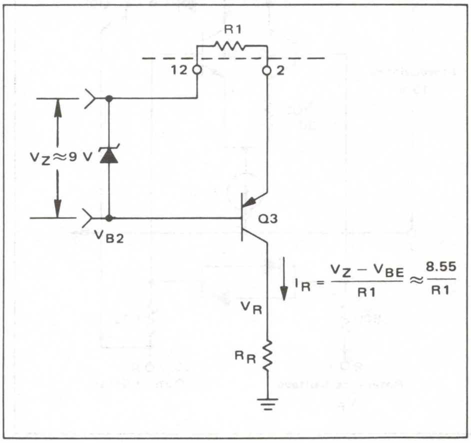

12
14
16 k
Equivalent Diode $V_Z \approx 9$ V
V_{aux}
V_{B1}
Q1 Q2
V_{B2}
Regulated Voltage 18 V
Equivalent Diode $V_Z \approx 9$ V
18 k
7

FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For I_E = 0.5 mA,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

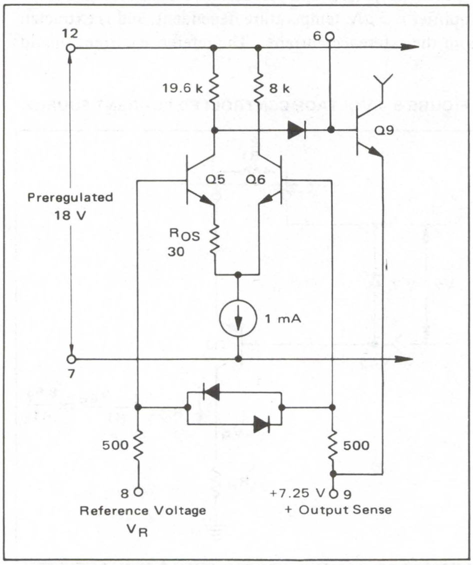
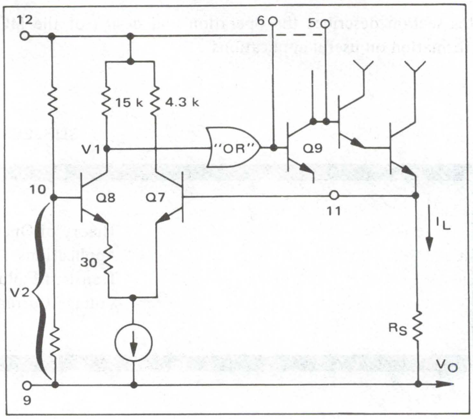


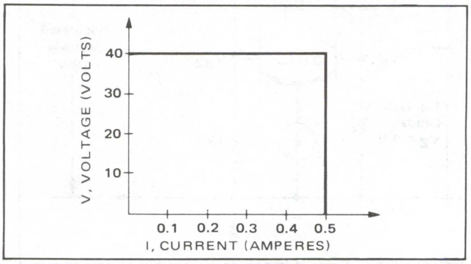
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

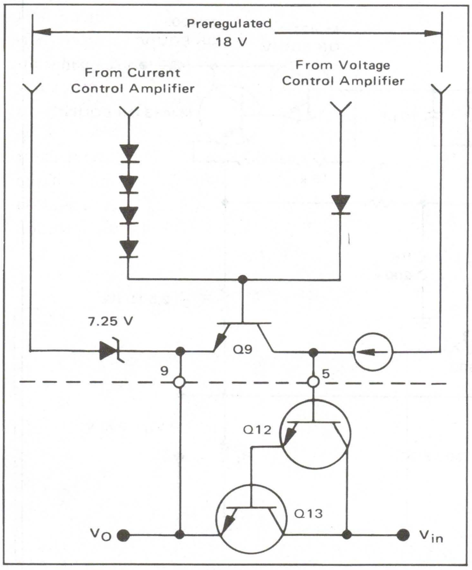
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300\text{ mA/volt} = 120\text{ A/volt}. \qquad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2\text{ mV}. \qquad (4)$$

FIGURE 12 – MC1566 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by ≈0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20\text{ V }(8\text{ mA}) + (11\text{ V} \times 3\text{ mA}) = 193\text{ mW}. \qquad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35\text{ V }(8\text{ mA}) + 26\text{ V }(3\text{ mA}) = 358\text{ mW}. \qquad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_O higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_S.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance, The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

$$\text{Let } R_2\ (k\Omega) = V_O$$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}\ .$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413

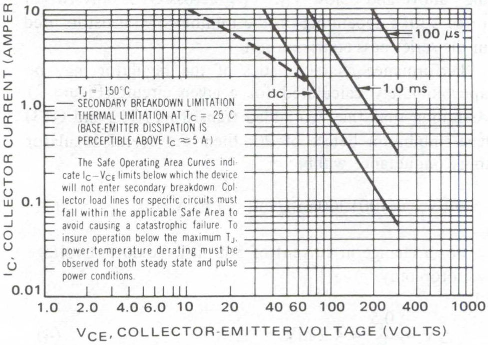
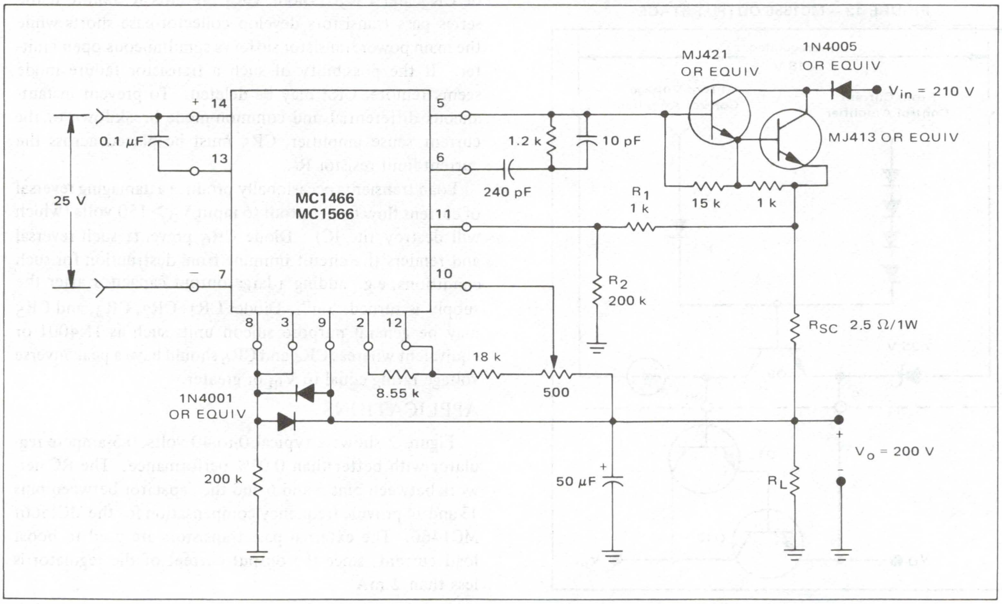


FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

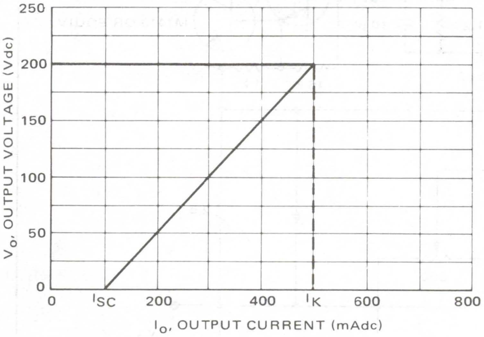


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/MC1466.

TRANSIENT FAILURES

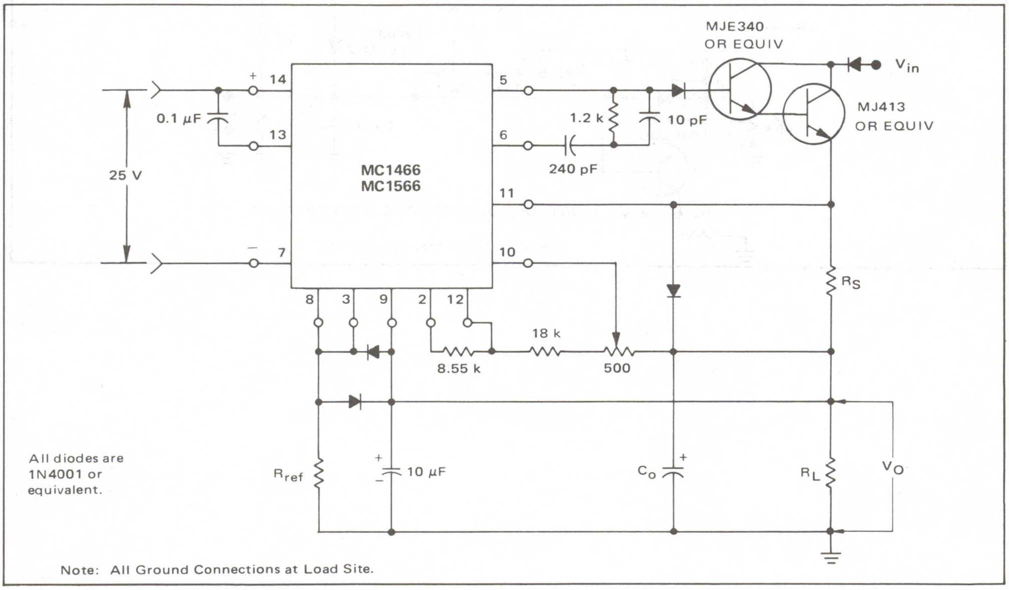
In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection doide between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE



All diodes are 1N4001 or equivalent.

Note: All Ground Connections at Load Site.

FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

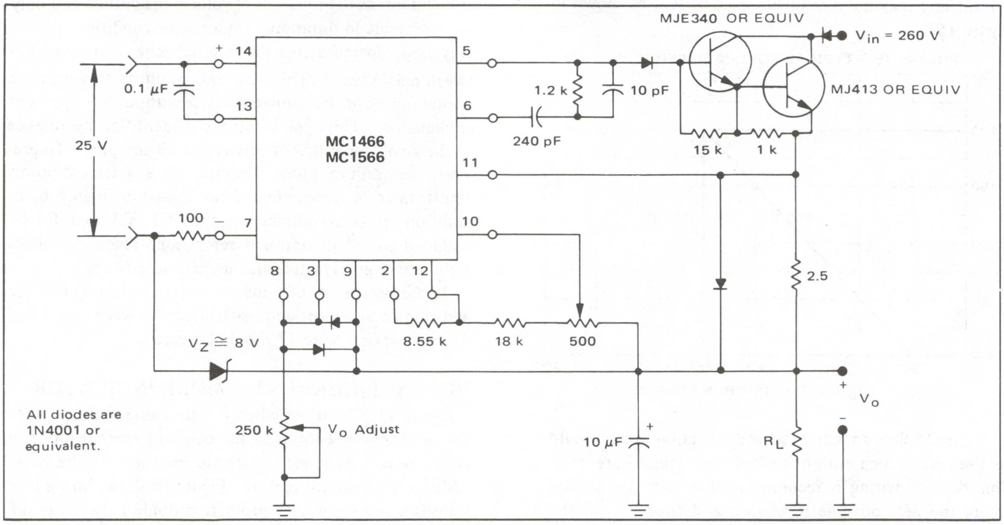
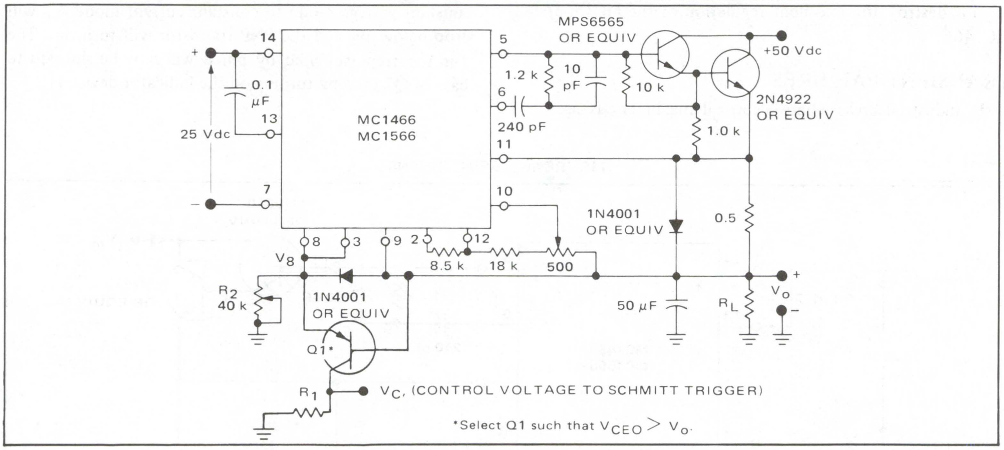

MJE340 OR EQUIV
V_{in} = 260 V
MJ413 OR EQUIV
+ 14
5
0.1 µF
13
6
1.2 k
10 pF
240 pF
15 k
1 k
25 V
MC1466
MC1566
11
100
– 7
10
8
3
9
2
12
2.5
V_Z ≅ 8 V
8.55 k
18 k
500
+
V_o
–
All diodes are 1N4001 or equivalent.
250 k
V_o Adjust
10 µF
+
R_L

FIGURE 18 – 0-TO--40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR


MPS6565 OR EQUIV
+50 Vdc
14
5
+
1.2 k
10 pF
10 k
0.1 µF
6
2N4922 OR EQUIV
13
MC1466
MC1566
240 pF
1.0 k
25 Vdc
11
7
10
1N4001 OR EQUIV
0.5
–
8
3
9
2
12
V_8
8.5 k
18 k
500
+
V_o
–
R_2 40 k
1N4001 OR EQUIV
50 µF
R_L
Q1*
R_1
V_C, (CONTROL VOLTAGE TO SCHMITT TRIGGER)
*Select Q1 such that $V_{CEO} > V_o$.

MOTOROLA

MC1468
MC1568

DUAL ±15-VOLT TRACKING REGULATOR

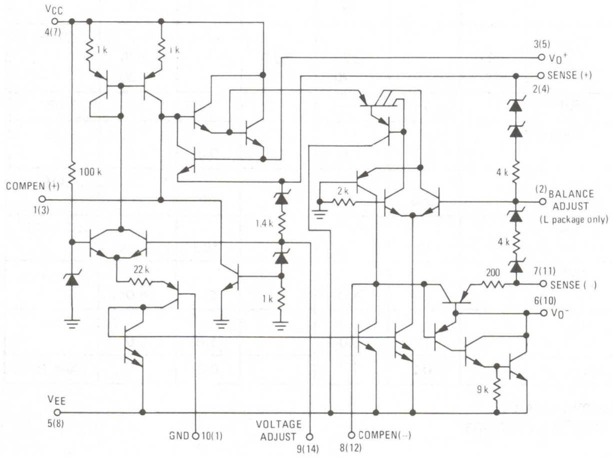
SILICON MONOLITHIC
INTEGRATED CIRCUIT

DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting. The device is available in three package types to accomodate various power requirements.

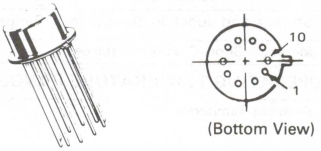
- Internally set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1% (MC1568)
- Line and Load Regulation of 0.06%
- 1% Maximum Output Variation due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions
- Case is at Ground Potential (R suffix package)

CIRCUIT SCHEMATIC

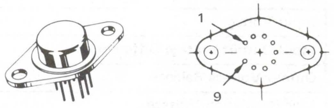

VCC
4(7)
1 k
1 k
100 k
COMPEN (+)
1(3)
22 k
1.4 k
1 k
2 k
4 k
4 k
200
9 k
3(5)
VO+
SENSE (+)
2(4)
(2) BALANCE
ADJUST
(L package only)
7(11)
SENSE (−)
6(10)
VO−
VEE
5(8)
GND
10(1)
VOLTAGE
ADJUST
9(14)
COMPEN(−)
8(12)

Pin numbers adjacent to terminals are for the G and R suffix packages only. Pin numbers in parentheses are for the L suffix package only.

Pin 10 is ground for the G suffix package only. For the R package, the case is ground.

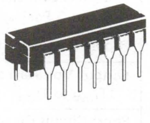

10
1
(Bottom View)

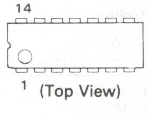
G SUFFIX
METAL PACKAGE
CASE 603C-01
TO-100



R SUFFIX
METAL PACKAGE
CASE 614-02

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA




14
1
(Top View)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC1468G	0° C to +70° C	Metal Can
MC1468L	0° C to +70° C	Ceramic DIP
MC1468R	0° C to +70° C	Metal Power
MC1568G	−55° C to +125° C	Metal Can
MC1568L	−55° C to +125° C	Ceramic DIP
MC1568R	−55° C to −125° C	Metal Power

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Input Voltage	$V_{CC}, \|V_{EE}\|$	30			Vdc
Peak Load Current	I_{PK}	100			mA
Power Dissipation and Thermal Characteristics		G Package	R Package	L Package	
T_A = +25°C	P_D	0.8	2.4	1.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	28.5	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	35	100	°C/W
T_C = +25°C	P_D	2.1	9.0	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14	61	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	17	50	°C/W
Storage and Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C
Minimum Short-Circuit Resistance	R_{SC}(min)	4.0			Ohms

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1468		0 to +70	
MC1568		-55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = −20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^-$ = 4.0 Ω, $I_L^+ = I_L^-$ = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

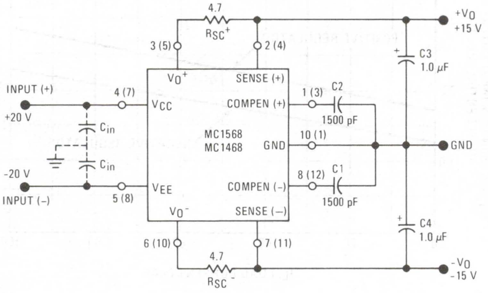
		MC1568			MC1468			
Characteristic	Symbol*	Min	Typ	Max	Min	Typ	Max	Unit
Output Voltage	V_O	±14.8	±15	±15.2	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	–	–	±30	–	–	±30	Vdc
Input-Output Voltage Differential	$\|V_{in} - V_O\|$	2.0	–	–	2.0	–	–	Vdc
Output Voltage Balance	V_{Bal}	–	±50	±150	–	±50	±300	mV
Line Regulation Voltage	Reg_{line}							mV
(V_{in} = 18 V to 30 V)		–	–	10	–	–	10	
(T_{low}① to T_{high}②)		–	–	20	–	–	20	
Load Regulation Voltage	Reg_{load}							mV
(I_L = 0 to 50 mA, T_J = constant)		–	–	10	–	–	10	
($T_A = T_{low}$ to T_{high})		–	–	30	–	–	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4.)		±8.0	–	±20	±8.0	–	±20	
R and G Packages (See Figures 2 and 13.)		±14.5	–	±20	±14.5	–	±20	
Ripple Rejection (f = 120 Hz)	RR	–	75	–	–	75	–	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\|TSV_O\|$	–	0.3	1.0	–	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{sc}	–	60	–	–	60	–	mA
Output Noise Voltage (BW = 100 Hz - 10 kHz)	V_n	–	100	–	–	100	–	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	–	2.4	4.0	–	2.4	4.0	mA
Negative Standby Current (V_{in} = −30 V)	I_B^-	–	1.0	3.0	–	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	–	0.2	–	–	0.2	–	%/k Hr

① T_{low} = 0°C for MC1468
= −55°C for MC1568

② T_{high} = +70°C for MC1468
= +125°C for MC1568

TYPICAL APPLICATIONS

FIGURE 1 – BASIC 50-mA REGULATOR

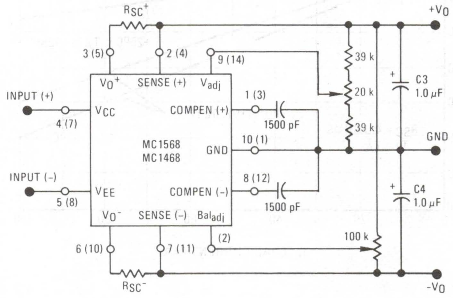

4.7
R_{SC}^+
3 (5)
2 (4)
+VO
+15 V
C3
1.0 μF
INPUT (+)
+20 V
4 (7)
VCC
SENSE (+)
COMPEN (+)
1 (3)
C2
1500 pF
Cin
MC1568
MC1468
GND
10 (1)
GND
-20 V
INPUT (–)
Cin
5 (8)
VEE
COMPEN (–)
8 (12)
C1
1500 pF
VO-
SENSE (–)
C4
1.0 μF
6 (10)
7 (11)
4.7
R_{SC}^-
-VO
-15 V

C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 – VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT

$(14.5\ V \leqslant V_{out} \leqslant 20\ V)$


R_{SC}^+
+VO
3 (5)
2 (4)
9 (14)
39 k
20 k
39 k
C3
1.0 μF
VO+
SENSE (+)
Vadj
INPUT (+)
VCC
COMPEN (+)
1 (3)
1500 pF
4 (7)
MC1568
MC1468
10 (1)
GND
GND
INPUT (–)
8 (12)
VEE
COMPEN (–)
1500 pF
5 (8)
C4
1.0 μF
VO-
SENSE (–)
Baladj
(2)
100 k
6 (10)
7 (11)
R_{SC}^-
-VO

Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 – ±1.5-AMPERE REGULATOR

(Short-Circuit Protected, with Proper Heatsinking)
(Metal-Packaged Devices Only, R Suffix)

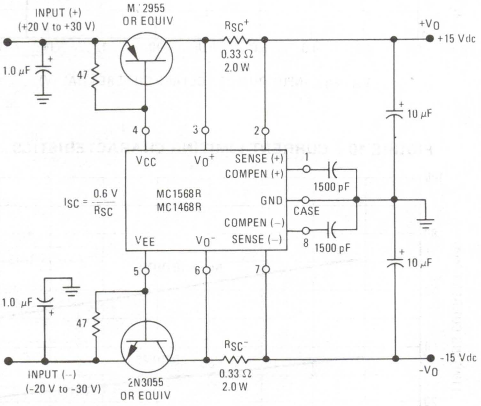
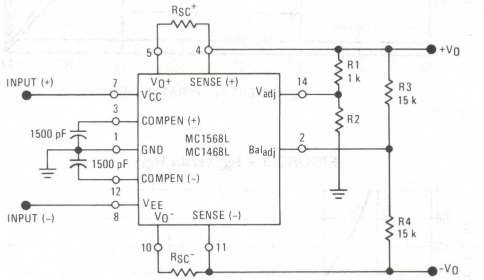

INPUT (+)
(+20 V to +30 V)
MJ2955
OR EQUIV
R_{SC}^+
+VO
+15 Vdc
1.0 μF
47
0.33 Ω
2.0 W
10 μF
4
3
2
VCC
VO+
SENSE (+)
COMPEN (+)
1
1500 pF
$I_{SC} = \frac{0.6\ V}{R_{SC}}$
MC1568R
MC1468R
GND
CASE
COMPEN (–)
SENSE (–)
8
1500 pF
VEE
VO-
5
6
7
10 μF
1.0 μF
47
R_{SC}^-
-15 Vdc
-VO
INPUT (–)
(-20 V to -30 V)
2N3055
OR EQUIV
0.33 Ω
2.0 W

FIGURE 4 – OUTPUT VOLTAGE ADJUSTMENT FOR $8.0\ V \leqslant |\pm V_O| \leqslant 14.5\ V$

(Ceramic-Packaged Devices Only, L Suffix.)


R_{SC}^+
5
4
+VO
INPUT (+)
7
VO+
SENSE (+)
14
R1
1 k
R3
15 k
VCC
Vadj
3
COMPEN (+)
R2
1500 pF
1
2
GND
MC1568L
MC1468L
Baladj
1500 pF
COMPEN (–)
12
INPUT (–)
8
VEE
VO-
SENSE (–)
R4
15 k
10
11
R_{SC}^-
-VO

The presence of the Bal_{adj}, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can calculated from

$$R2 = \frac{R1\ R_{int}\ (\phi + V_Z)}{R_{int}\ (V_O - \phi - V_Z) - \phi\ R1}$$

Where: R_{int} = An Internal Resistor = R1 = 1 kΩ
$\phi = 0.68\ V$
$V_Z = 6.6\ V$

Some common design values are listed below:

$\pm V_O$, V)	R2	$T_C\ V_O$ (%/°C)	I_B + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – LOAD REGULATION

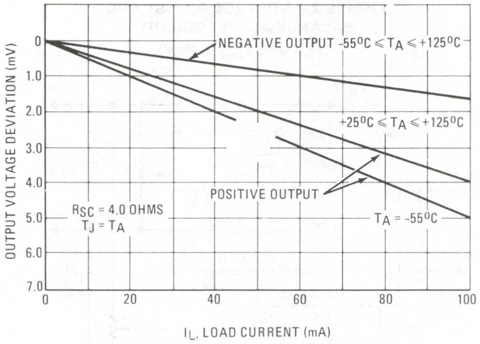


FIGURE 6 – REGULATOR DROPOUT VOLTAGE

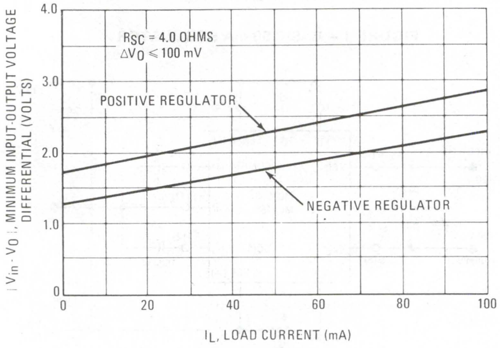


FIGURE 7 – MAXIMUM CURRENT CAPABILITY

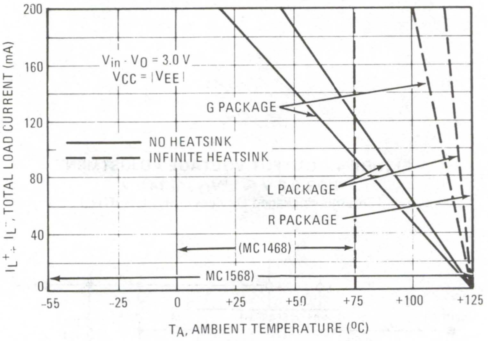


FIGURE 8 – MAXIMUM CURRENT CAPABILITY

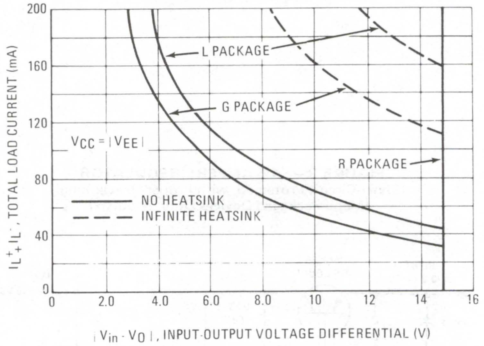


FIGURE 9 – I_{SC} versus R_{SC}

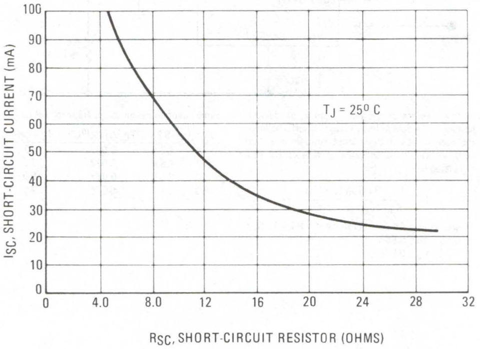
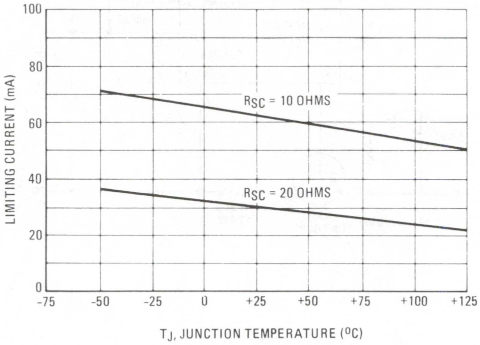


FIGURE 10 – CURRENT-LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – STANDBY CURRENT DRAIN

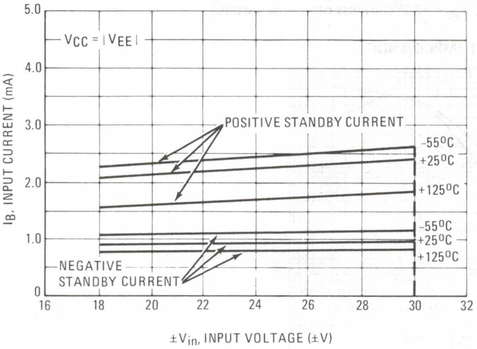


FIGURE 12 – STANDBY CURRENT DRAIN

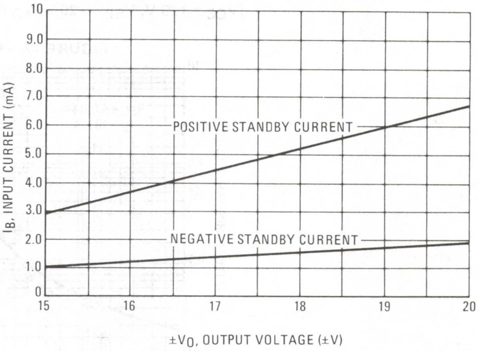


FIGURE 13 – TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

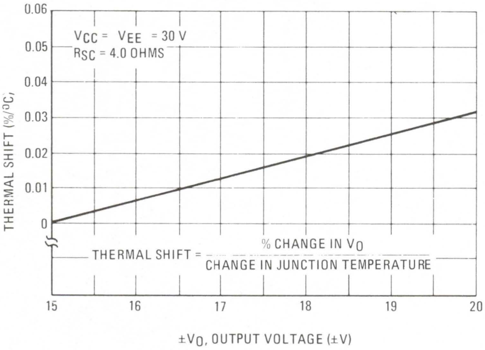


FIGURE 14 – LOAD TRANSIENT RESPONSE

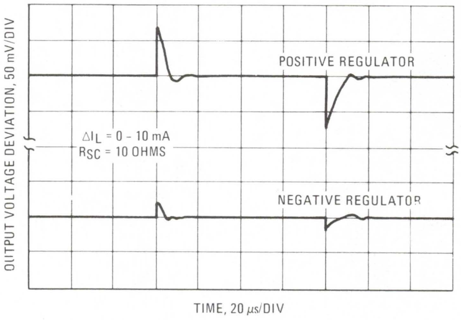


FIGURE 15 – LINE TRANSIENT RESPONSE

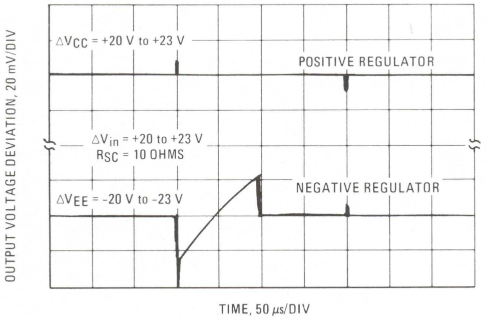
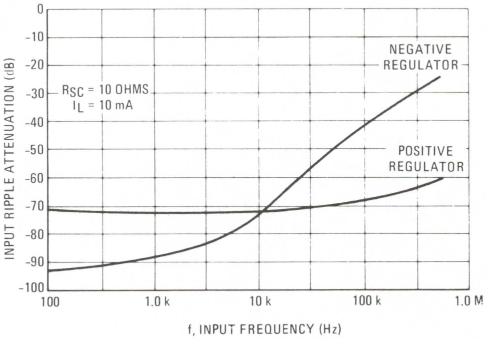


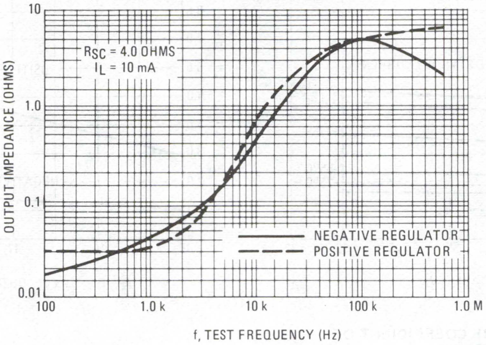
FIGURE 16 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 17 – OUTPUT IMPEDANCE



MOTOROLA

MC1469
MC1569

Specifications and Applications Information

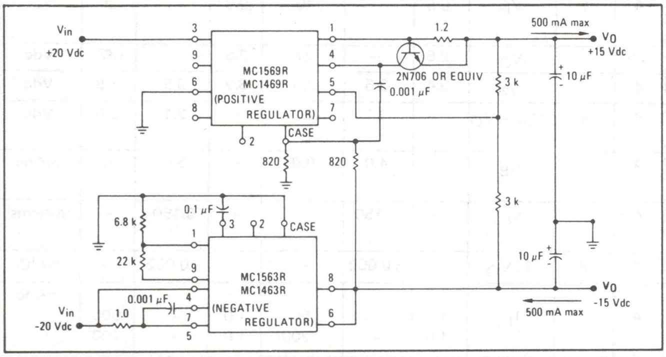
MONOLITHIC VOLTAGE REGULATOR

The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (−55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

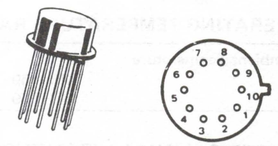
- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance – 20 milliohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: ±0.002 %/°C typ
- High Ripple Rejection: 0.002 %/V typ

FIGURE 1 – ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR

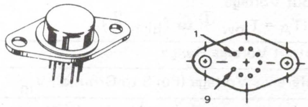

Vin
+20 Vdc
MC1569R
MC1469R
(POSITIVE REGULATOR)
CASE
1.2
2N706 OR EQUIV
0.001 µF
3 k
10 µF
500 mA max
VO
+15 Vdc
820
820
0.1 µF
6.8 k
22 k
0.001 µF
1.0
Vin
-20 Vdc
MC1563R
MC1463R
(NEGATIVE REGULATOR)
CASE
3 k
10 µF
VO
-15 Vdc
500 mA max

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED


(Bottom View)

G SUFFIX
METAL PACKAGE
CASE 603-04


1
9
(Bottom View)

R SUFFIX
METAL PACKAGE
CASE 614-02

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC1469G	0° C to +70°C	Metal Can
MC1469R	0° C to +70° C	Metal Power
MC1569G	−55° C to +125° C	Metal Can
MC1569R	−55° C to +125° C	Metal Power

FIGURE 2 – TYPICAL CIRCUIT CONNECTION
($3.5 \leqslant V_O \leqslant 37$ Vdc, $1 \leqslant I_L \leqslant 500$ mA)

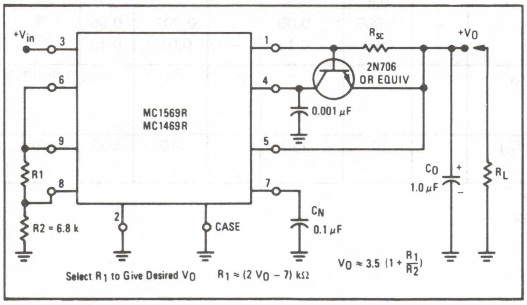
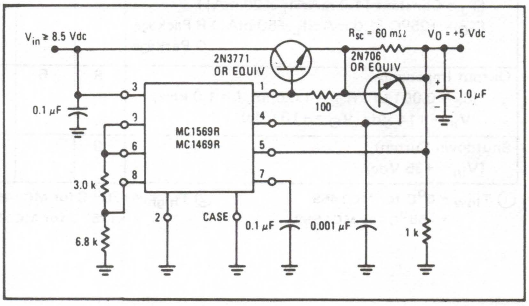

+Vin
MC1569R
MC1469R
RSC
+VO
2N706
OR EQUIV
0.001 µF
CO
1.0 µF
RL
CN
0.1 µF
R1
R2 = 6.8 k
CASE
Select R1 to Give Desired VO
R1 ≈ (2 VO − 7) kΩ
VO ≈ 3.5 (1 + R1/R2)

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.0 Vdc, I_L = 10 Adc [max])


Vin ≥ 8.5 Vdc
2N3771
OR EQUIV
RSC = 60 mΩ
VO = +5 Vdc
2N706
OR EQUIV
1.0 µF
100
0.1 µF
MC1569R
MC1469R
3.0 k
6.8 k
CASE
0.1 µF
0.001 µF
1 k

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage MC1469 MC1569	V_{in}	 35 40		Vdc
		G Package	R Package	
Peak Load Current	I_{PK}	250	600	mA
Current, Pin 2 Current, Pin 9	$I_{pin\ 2}$ $I_{pin\ 9}$	10 5.0	10 5.0	mA
Power Dissipation and Thermal Characteristics				
T_A = +25°C	P_D	0.68	3.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = +25°C	P_D	1.8	14	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature MC1469 MC1569	T_A	 0 to +70 -55 to +125	°C

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device,
= 10 mA for "G" Package device, unless otherwise noted)

Characteristic	Fig.	Note	Symbol	MC1569			MC1469			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	8.5	–	40	9.0	–	35	Vdc
Output Voltage Range	4,5		V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground, V_{in} = 15 V	4		V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (V_{in} = 15 V) (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, $I_{IB} = I_{in} - I_L$)	4		I_{IB}	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_N = 0.1 μF, f = 10 Hz to 5.0 MHz)	4		V_n	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range										mAdc
($R_{sc} \leqslant$ 0.3 ohms) R Package	4		I_L	1.0	–	500	1.0	–	500	
($R_{sc} \leqslant$ 2.0 ohms) G Package				1.0	–	200	1.0	–	200	
Input Regulation	6	4	Reg_{line}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation	7	5	Reg_{load}							
(T_J = Constant [1.0 mA $\leq I_L \leq$ 20 mA])				–	0.4	1.6	–	0.7	2.4	mV
(T_C = +25°C [1.0 mA $\leq I_L \leq$ 50 mA]) R Package				–	0.005	0.05	–	0.005	0.05	%
G Package				–	0.01	0.13	–	0.01	0.13	
Output Impedance (C_c = 0.001 μF, R_{sc} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	8	6	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = +35 Vdc)	9		I_{sd}	–	70	150	–	140	500	μAdc

① T_{low} = 0°C for MC1469
= -55°C for MC1569

② T_{high} = +70° C for MC1469
= +125°C for MC1569

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1569, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(180^\circ C)\ (V_O @ 25^\circ C)} = \%/^\circ C$$

$$\text{MC1469, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min})\ (100)}{(75^\circ C)\ (V_O @ 25^\circ C)} = \%/^\circ C$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_O}{V_O\ (v_{in})}\ 100\ (\%/V_O),$$

where v_O is the change in the output voltage V_O for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$Reg_{line} = 0.015\ \%/V_O$$
$$V_O = 10\ \text{Vdc}$$
$$v_{in} = 1.0\ \text{V(rms)}$$
$$v_o = \frac{(Reg_{line})\ (v_{in})\ (V_O)}{100}$$
$$= \frac{(0.015)\ (1.0)\ (10)}{100}$$
$$= 0.0015\ \text{V(rms)}$$

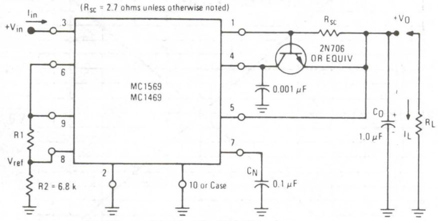
Note 5. Load regulation is specified for small ($\leqslant$+17°C) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{[V_O|I_L = 1.0\ \text{mA}] - [V_O|I_L = 50\ \text{mA}]}{V_O\,|I_L = 1.0\ \text{mA}} \times 100$$

Note 6. The resulting low level output signal (v_o) will require the use of a tuned voltmeter to obtain a reading. Special care should be used to insure that the measurement technique does not include connection resistance, wire resistance, and wire lead inductance (i.e., measure close to the case). Note that No. 22 AWG hook-up wire has approximately 4.0 milliohms/in. dc resistance and an inductive reactance of approximately 10 milliohms/in. at 100 kHz. Avoid use of alligator clips or banana plug-jack combination.

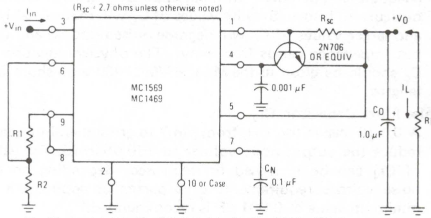
TEST CIRCUITS

FIGURE 4 – CONNECTION FOR $V_O \geqslant 3.5$ Vdc


(R_{sc} = 2.7 ohms unless otherwise noted)
I_{in}
$+V_{in}$
3
1
R_{sc}
$+V_O$
4
2N706
OR EQUIV
6
MC1569
MC1469
0.001 μF
5
C_O
9
1.0 μF
I_L
R_L
R1
V_{ref}
8
7
2
C_N
R2 = 6.8 k
10 or Case
0.1 μF

Select R1 to give desired V_O: R1 ≈ ($2 V_O - 7$) kΩ

FIGURE 5 – CONNECTION FOR 2.5 Vdc $\geqslant V_O \leqslant$ 3.5 Vdc


(R_{sc} = 2.7 ohms unless otherwise noted)
I_{in}
$+V_{in}$
3
1
R_{sc}
$+V_O$
4
2N706
OR EQUIV
6
MC1569
MC1469
0.001 μF
I_L
5
C_O
R_L
1.0 μF
R1
9
8
7
2
C_N
R2
10 or Case
0.1 μF

Select R2 to give desired V_O: R2 ≈ ($2 V_O$) kΩ Select R1: R1 ≈ (7.0 kΩ – R2) kΩ

FIGURE 6 – INPUT REGULATION

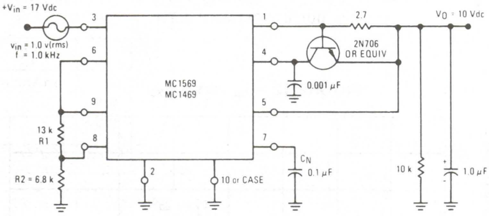

$+V_{in}$ = 17 Vdc
3
1
2.7
V_O = 10 Vdc
v_{in} = 1.0 v(rms)
f = 1.0 kHz
6
4
2N706
OR EQUIV
MC1569
MC1469
0.001 μF
9
5
13 k
R1
8
7
C_N
2
R2 = 6.8 k
10 or CASE
0.1 μF
10 k
1.0 μF

FIGURE 7 – LOAD REGULATION

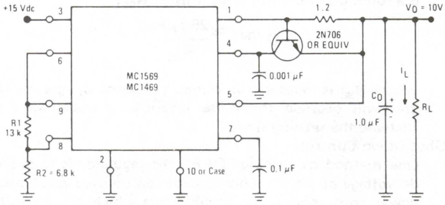

+15 Vdc
3
1
1.2
V_O = 10V
2N706
OR EQUIV
4
6
MC1569
MC1469
0.001 μF
I_L
5
C_O
R_L
9
1.0 μF
R1
13 k
7
8
2
R2 = 6.8 k
10 or Case
0.1 μF

FIGURE 8 – OUTPUT IMPEDANCE

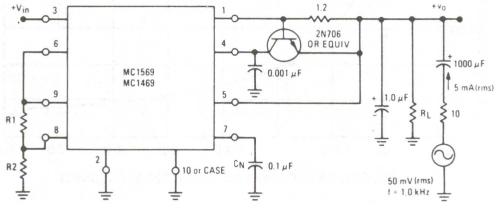
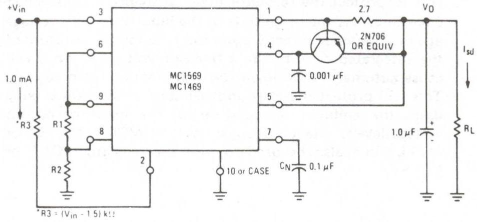

$+V_{in}$
3
1
1.2
$+V_O$
2N706
OR EQUIV
6
4
1000 μF
0.001 μF
MC1569
MC1469
5 mA(rms)
9
5
1.0 μF
R_L
10
R1
8
7
2
C_N
R2
10 or CASE
0.1 μF
50 mV(rms)
f = 1.0 kHz

FIGURE 9 – SHUTDOWN CURRENT


$+V_{in}$
3
1
2.7
V_O
2N706
OR EQUIV
6
4
I_{sd}
0.001 μF
MC1569
MC1469
1.0 mA
9
5
*R3
R1
8
1.0 μF
R_L
7
R2
2
10 or CASE
C_N
0.1 μF

*R3 = (V_{in} – 1.5) kΩ

GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) For $V_O \geqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:

   $$R1 \approx (2\ V_O - 7)\ k\Omega$$

   b) For $2.5 \leqslant V_O \leqslant 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:

   $$R2 \approx 2\ (V_O)\ k\Omega$$
   $$R1 \approx (7\ k\Omega - R2)\ k\Omega$$

   c) Output voltage, V_O, is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
   d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
   e) If V_O = 3.5 Vdc (to supply MRTL* for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{sc}

   Short Circuit Current, I_{sc}, is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 12 or the expression:

   $$R_{sc} \approx \frac{0.6}{I_{sc}}\ \text{ohm}$$

   where I_{sc} is measured in amperes. This expression is also valid when current is boosted as shown in Figure 2.
3. Compensation, C_c

   A 0.001 µF capacitor, C_c, from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_N

   A 0.1 µF capacitor, C_N, from pin 7 to ground will typically reduce the output noise voltage to 150 µV(rms). The value of C_N can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 µF is recommended.
5. Output Capacitor, C_O

   The value of C_O should be at least 1.0 µF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{sc}:

   $$C_O\ \text{max} \approx \frac{250\ \mu F}{R_{sc}}$$

   where R_{sc} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.
6. Shut-Down Control

   One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures. This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard Logic levels of MRTL, MDTL* or MTTL* can also be used to turn the regulator "ON" or "OFF".
7. Remote Sensing

   The connection to pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_o can be greatly reduced.

FIGURE 10 – R1 versus V_O
($V_O \geqslant 3.5$ Vdc, See Figure 4)

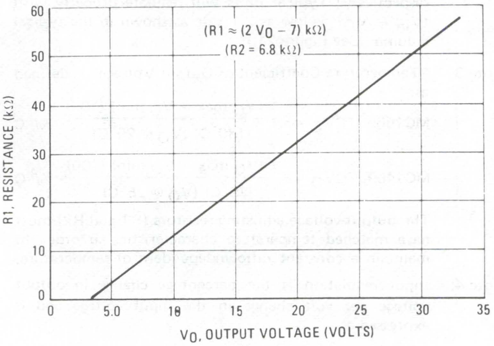


FIGURE 11 – R1 and R2 versus V_O
($2.5 \leqslant V_O \leqslant 3.5$ Vdc, See Figure 5)

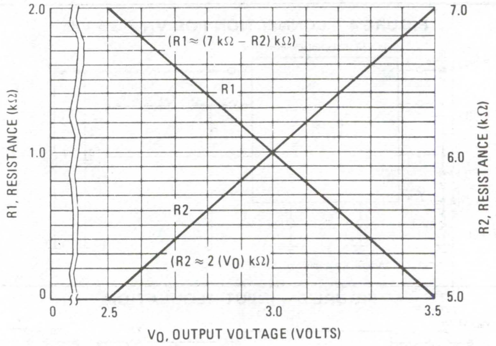
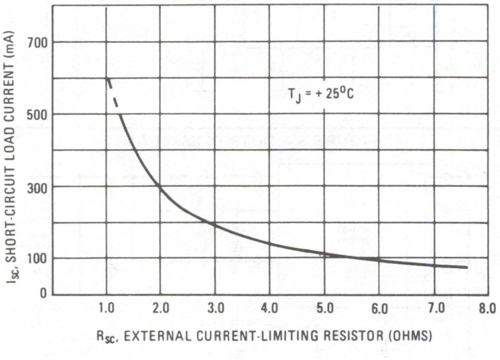


FIGURE 12 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_N = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_O = 1.0\ \mu F$, $T_C = +25^{\circ}C$,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
$I_L > 200$ mA for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

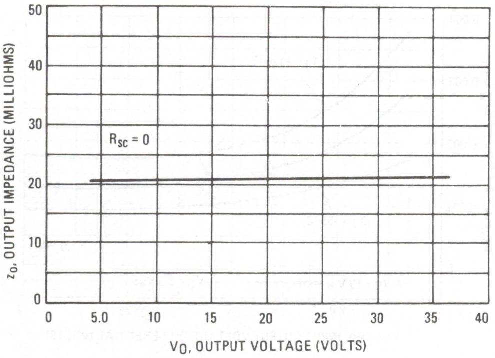


FIGURE 14 – OUTPUT IMPEDANCE versus R_{sc}

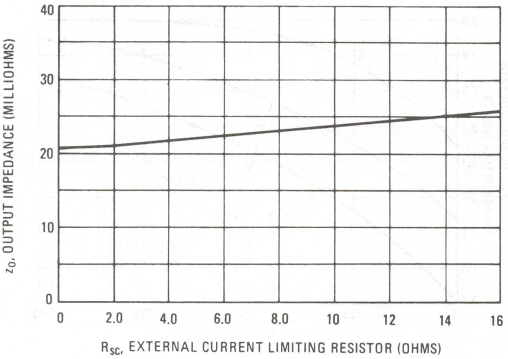


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 10\ \mu F$

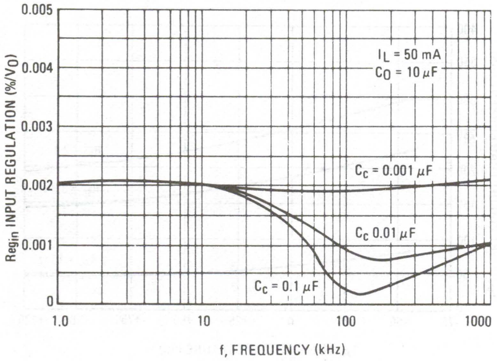


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 2.0\ \mu F$

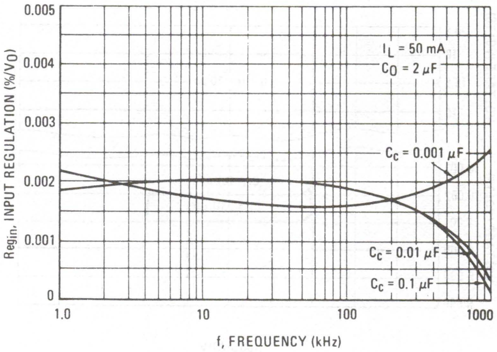


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

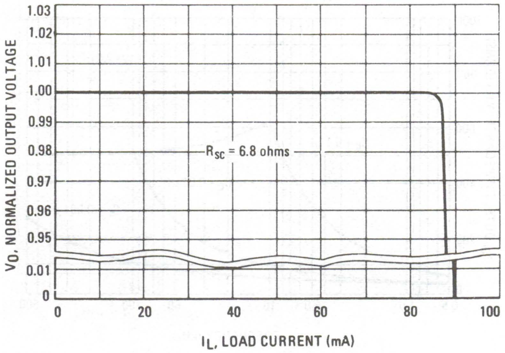
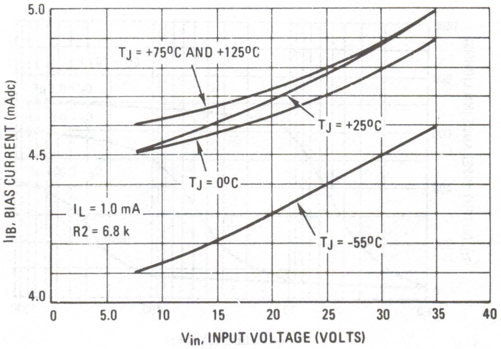


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: $C_N = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_O = 1.0\ \mu F$, $T_C = +25^\circ C$,
V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc,
$I_L > 200$ mA for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

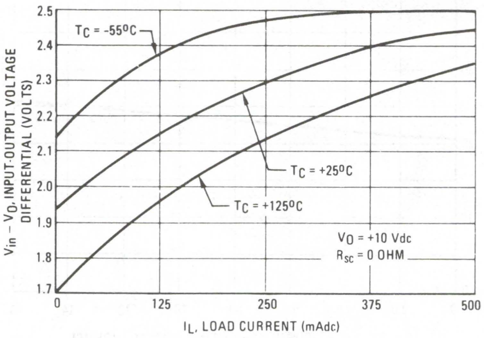


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

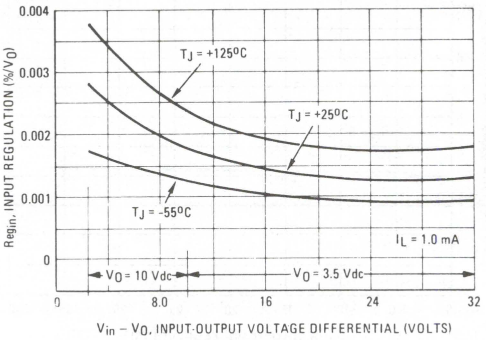


FIGURE 21 – INPUT TRANSIENT RESPONSE

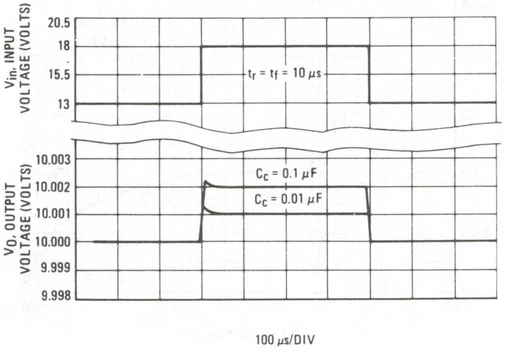


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

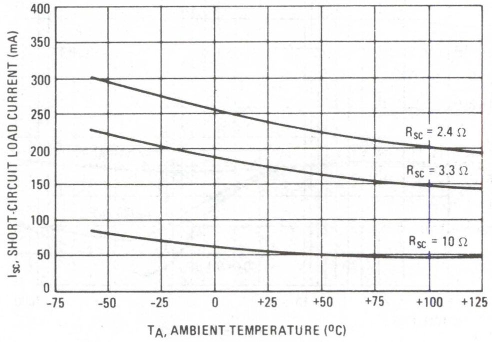


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_O = 10\ \mu F$

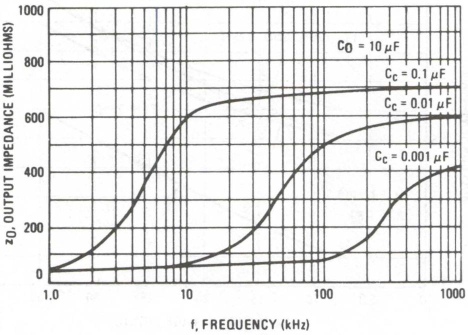
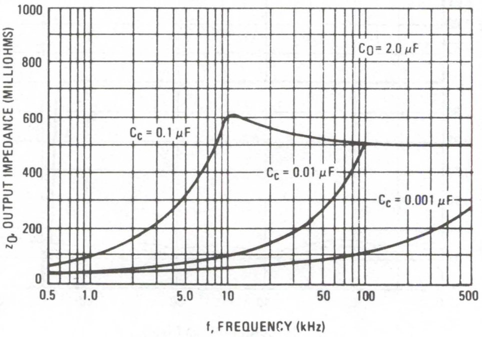


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, $C_O = 2.0\ \mu F$



OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

- Theory of Operation
- NPN Current Boosting
- PNP Current Boosting
- Switching Regulator
- Positive and Negative Power Supplies
- Shutdown Techniques
- Voltage Boosting
- Remote Sensing
- An Adjustable-Zero-Temperature-Coefficient Voltage Source
- Thermal Shutdown
- Thermal Considerations
- Latch-Up

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 – SERIES VOLTAGE REGULATOR

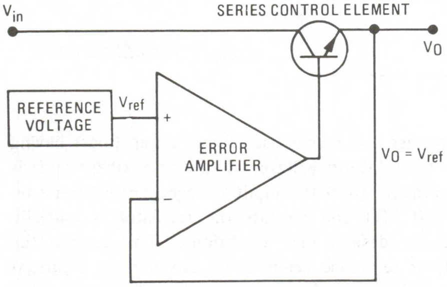
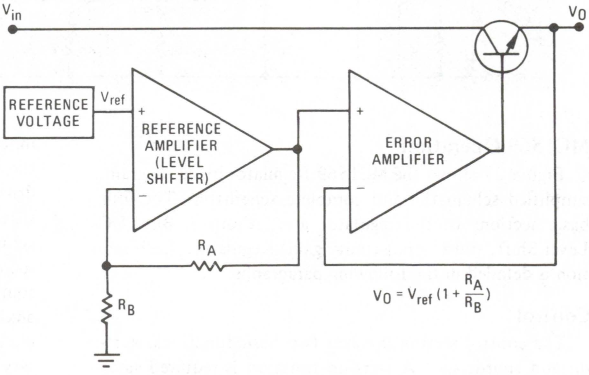


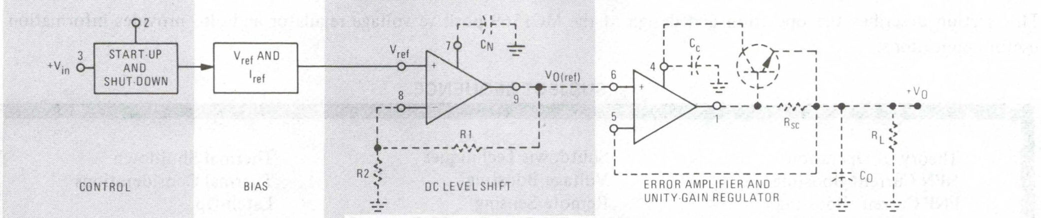
FIGURE 26 – THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH



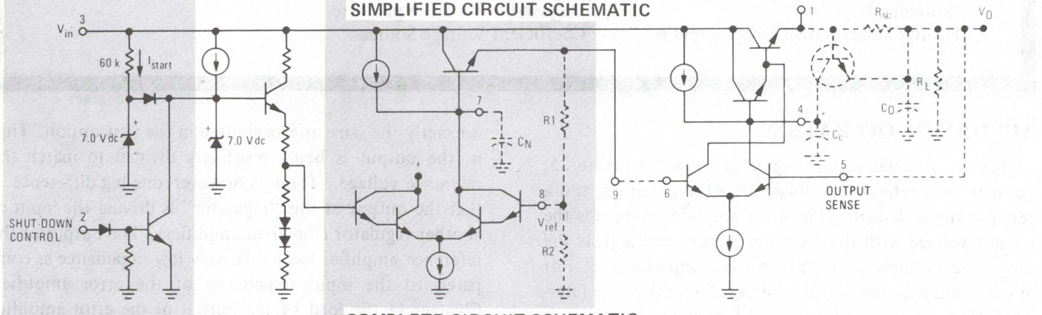
V_{in}
V_O
REFERENCE VOLTAGE
V_{ref}
+
−
REFERENCE AMPLIFIER (LEVEL SHIFTER)
+
−
ERROR AMPLIFIER
R_A
R_B
$V_O = V_{ref}(1 + \frac{R_A}{R_B})$

FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)

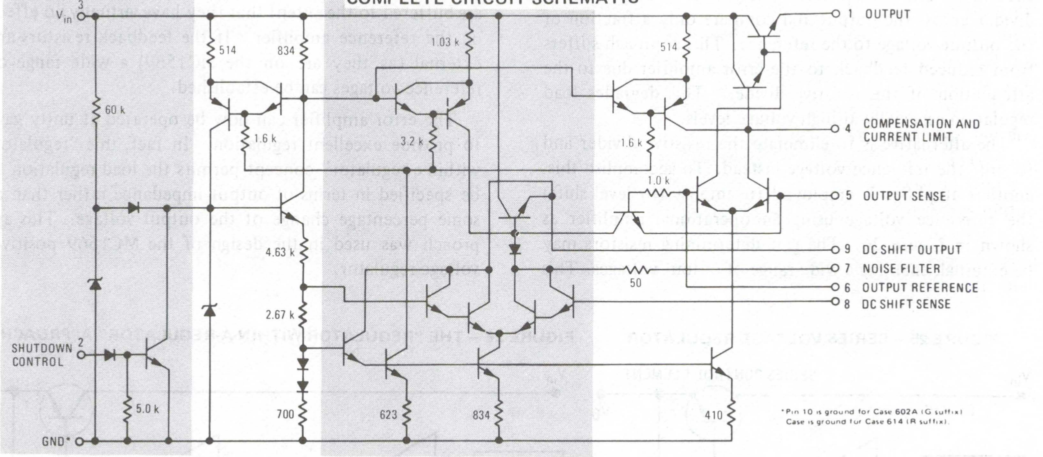
MC1569/MC1469 BLOCK DIAGRAM


2
3
+Vin
START-UP AND SHUT-DOWN
Vref AND Iref
Vref
7
CN
VO(ref)
8
9
R1
R2
CONTROL
BIAS
DC LEVEL SHIFT
6
5
4
Cc
1
Rsc
+VO
RL
CO
ERROR AMPLIFIER AND UNITY-GAIN REGULATOR

SIMPLIFIED CIRCUIT SCHEMATIC


3
Vin
60 k
Istart
7.0 Vdc
7.0 Vdc
7
CN
R1
8
Vref
R2
SHUT-DOWN CONTROL
2
9
6
1
Rsc
VO
4
Cc
CO
RL
5
OUTPUT SENSE

COMPLETE CIRCUIT SCHEMATIC


3
Vin
514
834
1.03 k
60 k
1.6 k
3.2 k
4.63 k
2.67 k
SHUTDOWN CONTROL
2
5.0 k
700
623
834
GND*
514
1.6 k
1.0 k
50
410
1 OUTPUT
4 COMPENSATION AND CURRENT LIMIT
5 OUTPUT SENSE
9 DC SHIFT OUTPUT
7 NOISE FILTER
6 OUTPUT REFERENCE
8 DC SHIFT SENSE

*Pin 10 is ground for Case 602A (G suffix)
Case is ground for Case 614 (R suffix).

MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60\ k\Omega$ or 500 μA for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of 0.002 %/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_N, is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_N will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{SC} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_L \max \approx \frac{0.6}{R_{SC}} \text{ or } R_{SC} = \frac{0.6}{I_L \max}$$

where I_L max is the maximum load current (amperes) and R_{SC} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_O (typically 1.0 μF) from the output, V_O, to ground. When an external transistor is used to boost the current, C_O = 1.0 μF is also recommended (see Figure 2).

FIGURE 28A – LOAD TRANSIENT RESPONSE

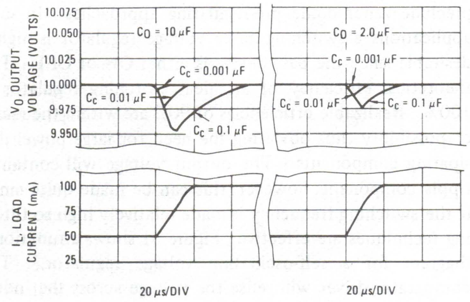
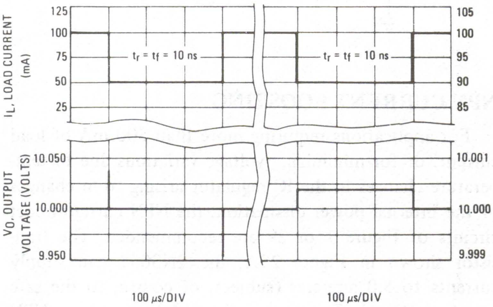
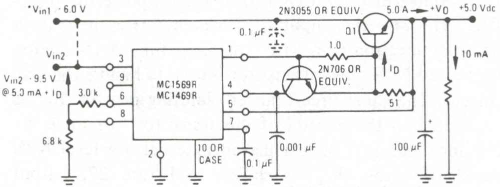


FIGURE 28B – LOAD TRANSIENT RESPONSE



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A – 5 VOLT 5-AMPERE REGULATOR


*Vin1 · 6.0 V
2N3055 OR EQUIV.
5.0 A
+VO
+5.0 Vdc
*0.1 µF
Q1
1.0
Vin2
3
9
6
8
1
4
5
7
2N706 OR EQUIV.
ID
10 mA
Vin2 · 9.5 V @ 5.0 mA + ID
3.0 k
MC1569R
MC1469R
51
6.8 k
2
10 OR CASE
0.1 µF
0.001 µF
100 µF

*For ripple reduction or increased efficiency at low output voltages, the collector of Q1 can tie to a separate low-voltage supply as shown.

FIGURE 29B – 5-VOLT 5-AMPERE REGULATOR

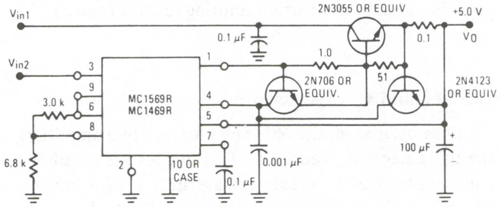
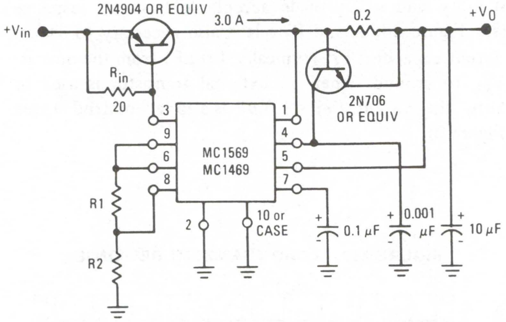

Vin1
2N3055 OR EQUIV
+5.0 V
0.1 µF
0.1
VO
Vin2
1.0
2N706 OR EQUIV.
51
2N4123 OR EQUIV
3
9
6
8
1
4
5
7
3.0 k
MC1569R
MC1469R
100 µF
6.8 k
2
10 OR CASE
0.1 µF
0.001 µF

FIGURE 30 – PNP CURRENT BOOST CONNECTION


2N4904 OR EQUIV
3.0 A
0.2
+VO
+Vin
Rin
20
2N706 OR EQUIV
3
9
6
8
1
4
5
7
MC1569
MC1469
R1
R2
2
10 or CASE
0.1 µF
0.001 µF
10 µF

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 3 or 29 are recommended. The transistor shown in Figure 29A, the 2N3055 can supply currents to 5.0 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 9.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 5.0 ampere regulator of Figure 29 this represents a savings of 17.5 watts when compared with operating the regulator from the single 9.5 V supply. It can supply current to 5.0 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 5.0 amperes by the added short-circuit current network in its emitter (R_{SC}), (Figure 29B).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_{IB}) the resistor R_{in} must meet the following condition

$$R_{in} < \frac{V_{BE}}{I_{IB}}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L, by

$$L \frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, when:

$$\beta_1 V_{in} = \frac{V_{ref}R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}.$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref}R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_O\,(V_{in} - V_O)}{L\,V_C\,I(max) - I_O)} \qquad (1)$$

where

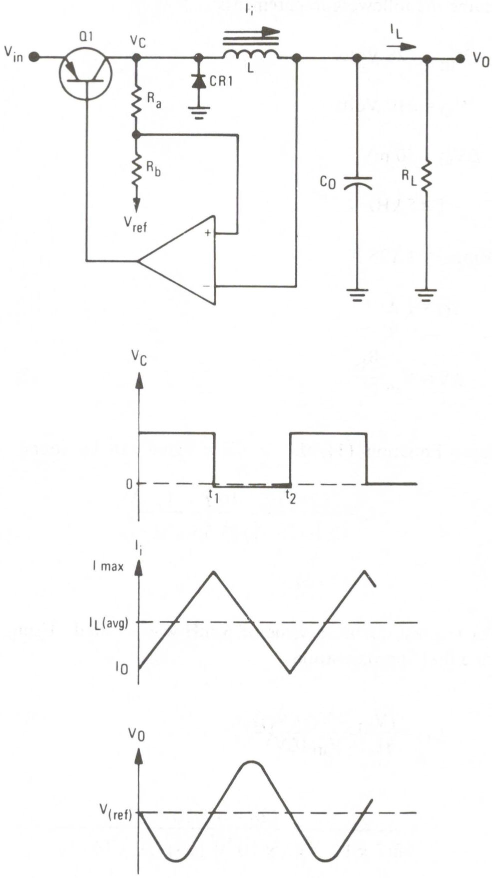
$I(max)$ = The maximum value of inductor current

I_O = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

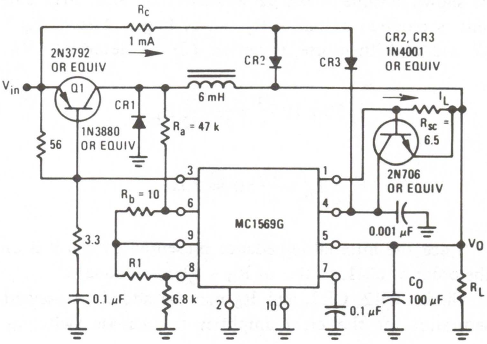
Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref}. Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

FIGURE 31 – BASIC SELF-OSCILLATING SWITCHING REGULATOR



I_i
Q1
V_C
I_L
V_{in}
V_O
CR1
L
R_a
R_b
V_{ref}
C_O
R_L
+
–
V_C
0
t_1
t_2
I_i
I max
$I_{L(avg)}$
I_O
V_O
$V_{(ref)}$

FIGURE 32 – MC1569 SELF-OSCILLATING SWITCHING REGULATOR



R_C
1 mA
2N3792 OR EQUIV
CR2
CR3
CR2, CR3 1N4001 OR EQUIV
V_{in}
Q1
CR1
6 mH
I_L
R_{sc} = 6.5
56
1N3880 OR EQUIV
R_a = 47 k
3
1
2N706 OR EQUIV
R_b = 10
6
4
MC1569G
0.001 µF
3.3
9
5
V_O
R1
8
7
0.1 µF
6.8 k
2
10
0.1 µF
C_O 100 µF
R_L

As a design center is required for a practical circuit, assume the following requirements:

$V_{in} = +28$ Volts

$V_O = +10$ Volts

$\Delta V_O = 50$ mV

$f \cong 5$ kHz

$I(max) = 1.125$ A

$I_O = 1$ A

$$\Delta V \approx V_{in} \frac{R_b}{R_a}. \qquad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3}\right)$$

$$\approx 7 \text{ mH}.$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_O = \frac{(V_{in} - V_O)(V_O)}{8L f^2 V_{in} (\Delta V)}$$

$$= \frac{(28-10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})}$$

$$\approx 95\ \mu F.$$

As shown, a value of 100 µF was selected. Since little current is required at pin 6, R_a can be large. Assume R_a = 47 kΩ and then use Equation (2) to determine R_b:

$$50 \times 10^{-3} = \frac{28}{47 \text{ k}\Omega} R_b$$

$$R_b = \frac{47}{28} 50 \approx 85\Omega.$$

Since the internal impedance presented by pin 9 is on the order of 60Ω, a value of R_b = 10Ω is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mAdc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

$V_{in} = +28\ (\pm 1\%)$ Volts

$V_O = +10$ Volts

$\Delta V_O = 60$ mV

$f = 7$ kHz

$@\ I_L = 1$A

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{SC} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100$ mA and $R_{SC} = 6.5\Omega$.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 1 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $|-V_O|$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The −15-volt supply varies less than 0.1 mV over a zero to −300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leqslant I_L \leqslant 200$ mA with the other two voltages remaining unchanged. See page 19 for additional information.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1569 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of an NPN transistor; which, if turned "ON", will turn the zener "OFF" and deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60-k-ohm start resistor $(V_{in}/60\ k\Omega)$. This feature provides additional versatility in the applications of the MC1569. Various subsystems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as overheating, over-voltage, shorted output, etc.

To activate shutdown, one simply applies a potential greater than two diode drops with a current capability of 1 mA. Note that if a hard supply (i.e., +3 V) is applied directly to pin 2, the shutdown circuitry will be destroyed since there is no inherent current limiting. Maximum rating for the drive current into pin 2 is 10 mA, while 1 mA is adequate for shutdown.

FIGURE 33 – A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY

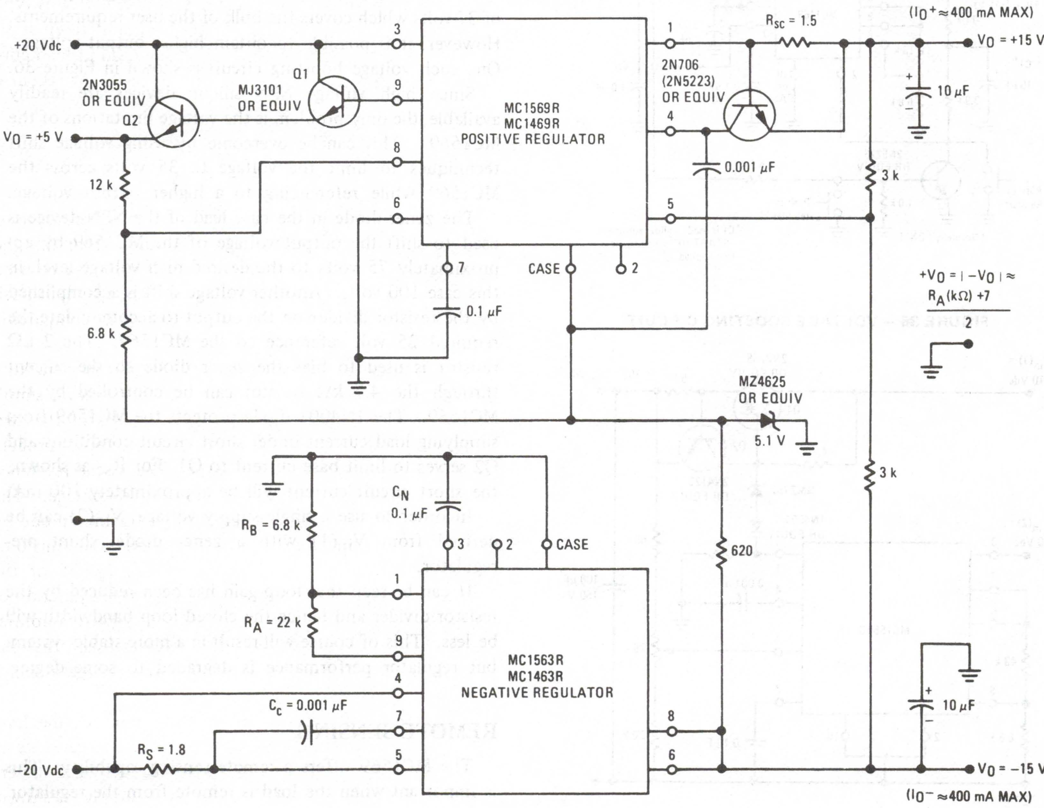
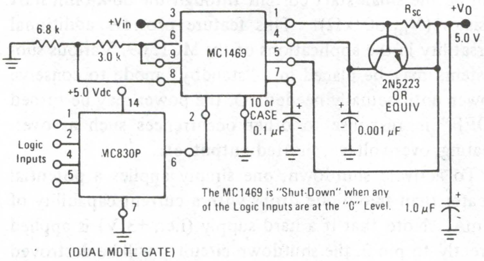
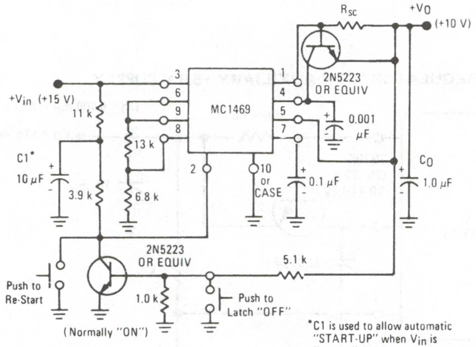

+20 Vdc
2N3055
OR EQUIV
Q2
MJ3101
OR EQUIV
Q1
VO = +5 V
12 k
6.8 k
0.1 µF
3
9
8
6
7
CASE
2
MC1569R
MC1469R
POSITIVE REGULATOR
1
4
5
2N706
(2N5223)
OR EQUIV
RSC = 1.5
0.001 µF
(IO+ ≈ 400 mA MAX)
VO = +15 Vdc
10 µF
3 k
+VO = | −VO | ≈ RA(kΩ) +7 / 2
MZ4625
OR EQUIV
5.1 V
3 k
620
CN
0.1 µF
RB = 6.8 k
RA = 22 k
CC = 0.001 µF
RS = 1.8
−20 Vdc
MC1563R
MC1463R
NEGATIVE REGULATOR
10 µF
VO = −15 Vdc
(IO− ≈ 400 mA MAX)

FIGURE 34 – ELECTRONIC SHUT-DOWN USING A MDTL GATE


+Vin
6.8 k
3.0 k
3
6
9
8
1
4
5
7
MC1469
Rsc
+VO
5.0 V
2N5223
OR
EQUIV
+5.0 Vdc
14
2
10 or
CASE
0.1 µF
0.001 µF
1.0 µF
1
2
4
5
Logic
Inputs
MC830P
6
7
(DUAL MDTL GATE)

The MC1469 is "Shut-Down" when any of the Logic Inputs are at the "0" Level.

FIGURE 35 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START


Rsc
+VO
(+10 V)
2N5223
OR EQUIV
3
6
9
8
1
4
5
7
MC1469
+Vin (+15 V)
11 k
13 k
C1*
10 µF
3.9 k
6.8 k
2
10
or
CASE
0.001
µF
0.1 µF
CO
1.0 µF
2N5223
OR EQUIV
5.1 k
Push to
Re-Start
1.0 k
Push to
Latch "OFF"
(Normally "ON")

*C1 is used to allow automatic "START-UP" when V_{in} is first applied.

FIGURE 36 – VOLTAGE BOOSTING CIRCUIT

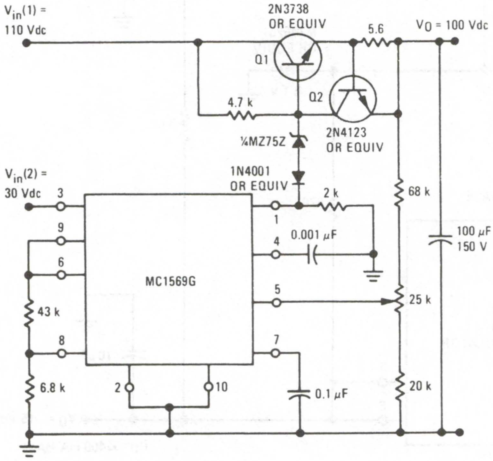

Vin(1) =
110 Vdc
2N3738
OR EQUIV
5.6
VO = 100 Vdc
Q1
Q2
4.7 k
¼MZ75Z
2N4123
OR EQUIV
Vin(2) =
30 Vdc
1N4001
OR EQUIV
2 k
68 k
3
9
6
8
1
4
5
7
0.001 µF
100 µF
150 V
MC1569G
25 k
43 k
6.8 k
2
10
0.1 µF
20 k

Figure 34 shows how the regulator can be controlled by a logic gate. Here, it is assumed that the regulator operates in its normal mode – as a positive regulator referenced to ground – and that the logic gate is of the saturating type, operating from a positive supply to ground. The high logic level should be greater than about 1.5 V and should source no more than 10 mA into pin 2.

The gate shown is of the MDTL type. MRTL and MTTL can also be used as long as the drive current is within safe limits (this is important when using MTTL, where the output stage uses an active pull-up).

In some cases a regulator can be designed which can handle the power dissipation resulting from normal operation but cannot safely dissipate the power resulting from a sustained short-circuit. The circuit of Figure 35 solves this problem by shutting down the regulator when the output is short-circuited.

VOLTAGE BOOSTING

The MC1569 has a maximum output voltage capability of 37 volts which covers the bulk of the user requirements. However, it is possible to obtain higher output voltages. One such voltage boosting circuit is shown in Figure 36.

Since high voltage NPN silicon devices are readily available, the only problem is the voltage limitations of the MC1569. This can be overcome by using voltage shift techniques to limit the voltage to 35 volts across the MC1569 while referencing to a higher output voltage.

The zener diode in the base lead of the NPN device is used to shift the output voltage of the MC1569 by approximately 75 volts to the desired high voltage level, in this case 100 volts. Another voltage shift is accomplished by the resistor divider on the output to accommodate the required 25 volt reference to the MC1569. The 2 kΩ resistor is used to bias the zener diode so the current through the 4.7 kΩ resistor can be controlled by the MC1569. The 1N4001 diode protects the MC1569 from supplying load current under short circuit conditions and Q2 serves to limit base current to Q1. For R_{SC} as shown, the short circuit current will be approximately 100 mA.

In order to use a single supply voltage, $V_{in}(2)$ can be derived from $V_{in}(1)$ with a zener diode, shunt preregulator.

It can be seen that loop gain has been reduced by the resistor divider and hence the closed loop bandwidth will be less. This of course will result in a more stable system, but regulator performance is degraded to some degree.

REMOTE SENSING

The MC1569 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

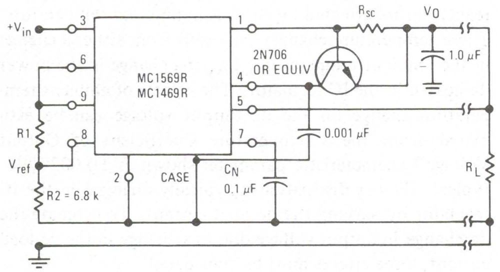
AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE.

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

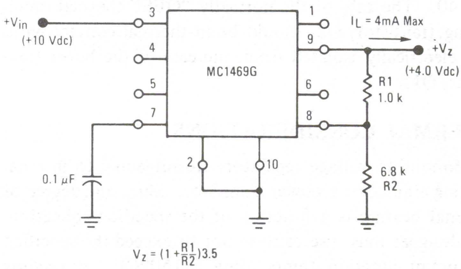
By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 (-3.4×10^{-3}V/°C). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

FIGURE 37 – REMOTE SENSING CIRCUIT



+Vin
3
6
9
8
R1
Vref
R2 = 6.8 k
2
CASE
MC1569R
MC1469R
1
4
5
7
Rsc
VO
2N706
OR EQUIV
1.0 µF
0.001 µF
CN
0.1 µF
RL

FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE



+Vin
(+10 Vdc)
3
4
5
7
0.1 µF
MC1469G
2
10
1
9
6
8
IL = 4mA Max
+Vz
(+4.0 Vdc)
R1
1.0 k
6.8 k
R2
$V_z = (1 + \frac{R1}{R2})3.5$

FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

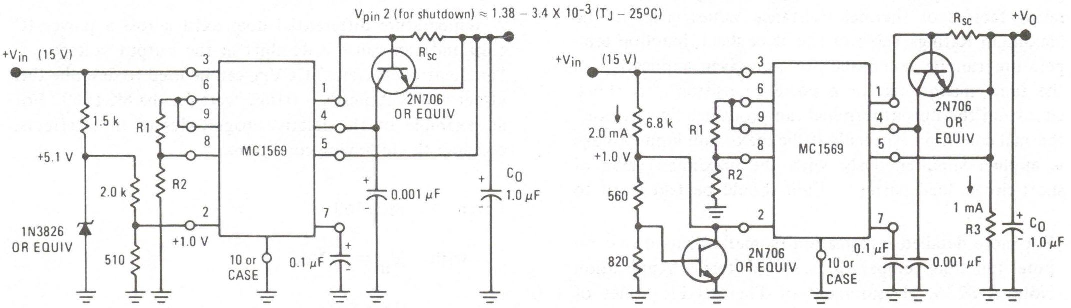


FIGURE 39A – USING A ZERO TC REFERENCE

FIGURE 39B – USING A T_A REFERENCE

$V_{pin\ 2\ (for\ shutdown)} \approx 1.38 - 3.4 \times 10^{-3}\ (T_J - 25°C)$
+Vin (15 V)
1.5 k
+5.1 V
2.0 k
1N3826
OR EQUIV
510
R1
R2
+1.0 V
3
6
9
8
2
MC1569
10 or
CASE
1
4
5
7
0.1 µF
Rsc
2N706
OR EQUIV
0.001 µF
CO
1.0 µF
+Vin (15 V)
2.0 mA
6.8 k
+1.0 V
560
820
R1
R2
2N706
OR EQUIV
MC1569
10 or
CASE
0.1 µF
0.001 µF
Rsc
+VO
2N706
OR
EQUIV
1 mA
R3
CO
1.0 µF

FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

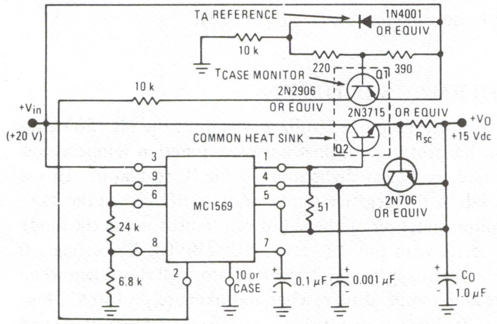
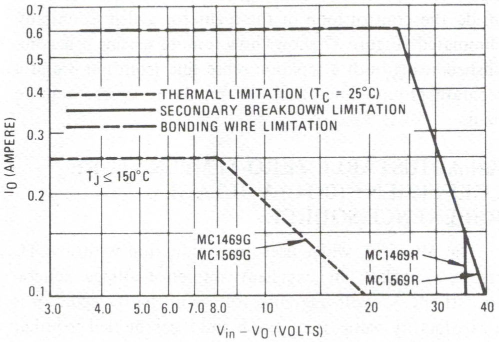


FIGURE 41 – DC SAFE OPERATING AREA



In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically –0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with $V_{in} = 10$ Vdc

$V_O = 5$ Vdc

---

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

and $I_L = 100$ mA to 200 mA

$(\Delta I_L = 100 \text{ mA})$

assume $T_A = +25°C$

TO-66 Case with heatsink

assume $\theta_{CS} = 0.2°C/W$

and $\theta_{SA} = 2°C/W$

$\theta_{JC} = 7.15°C/W$ (from maximum ratings table)

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5V)(5\ V \times 0.1A)(\pm 0.002\%/°C)(9.35°C/W)$$

$$\Delta V_O \approx \pm 0.5 \text{ mV}$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2 \text{ mV}$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (-6 \times 10^{-4}/W)(5 \text{ volts})(5 \times 10^{-1} W)$$

$$|\Delta V_O| = -1.6 \text{ mV}$$

Therefore the total ΔV_O is given by

$$|\Delta V_O \text{ total}| = \pm 0.5 - 2.0 - 1.6 \text{ mV}$$

OR

$$-4.1 \text{ mV} \leqslant |V_O \text{ total}| \leqslant -3.1 \text{ mV}$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

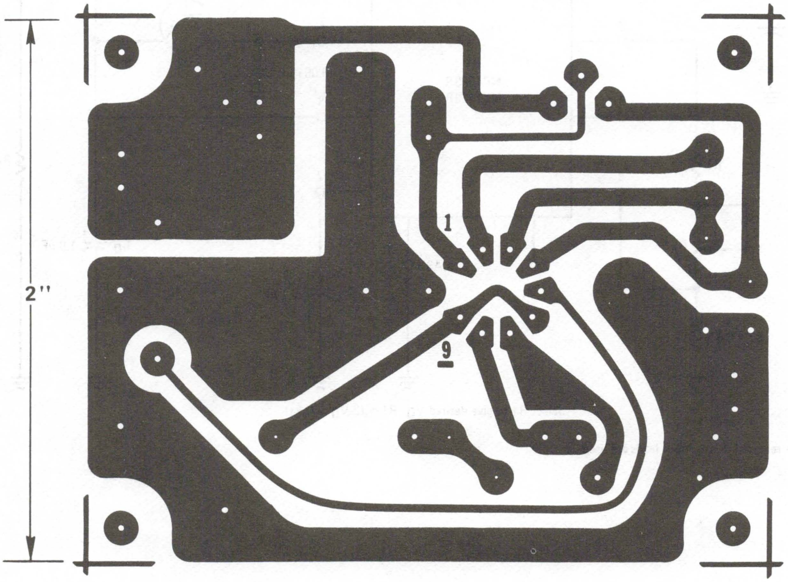
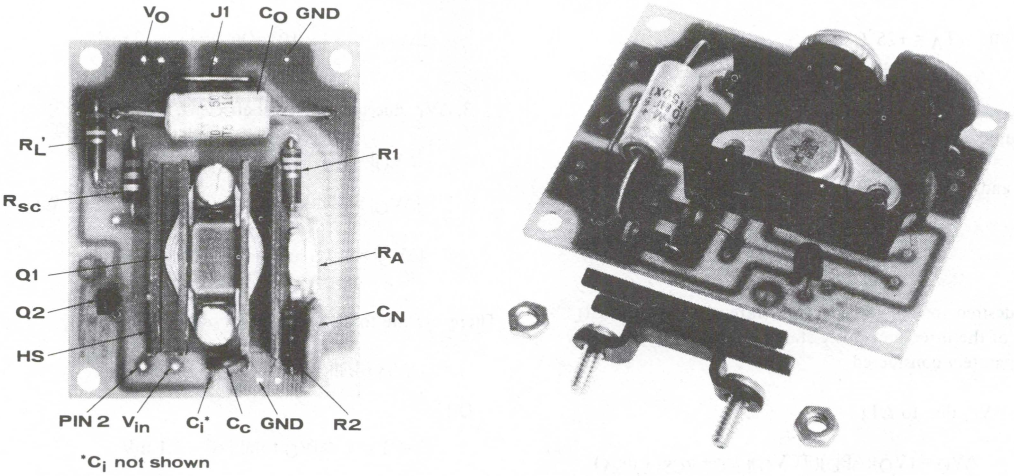


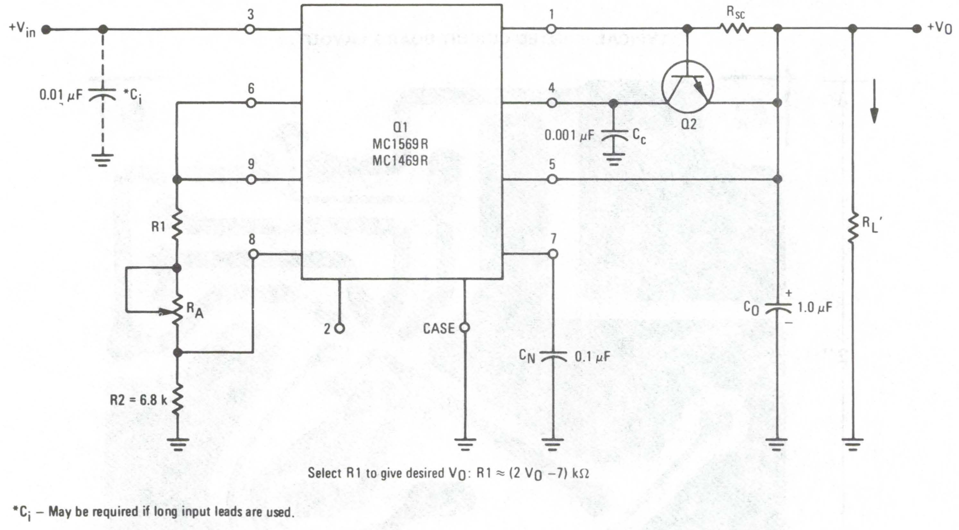
FIGURE 42 – LOCATION OF COMPONENTS


VO
J1
CO GND
RL'
RSC
R1
RA
Q1
Q2
CN
HS
PIN 2
Vin
Ci*
CC
GND
R2

*Ci not shown

FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)

$3.5\ V \leq V_O \leq 37\ V,\ 1\ mA \leq I_L \leq 500\ mA$


+Vin
3
0.01 μF
*Ci
6
9
R1
RA
8
R2 = 6.8 k
Q1
MC1569R
MC1469R
2
CASE
1
4
0.001 μF
Cc
5
7
CN
0.1 μF
Q2
Rsc
+VO
CO
1.0 μF
RL'

Select R1 to give desired V_O: $R1 \approx (2\ V_O - 7)\ k\Omega$

*C_i – May be required if long input leads are used.

PARTS LIST

Component	Value	Description
R1	Select	1/4 or 1/2 watt carbon
R2	6.8 k	
*R$_A$	Select	IRC Model X-201 Mallory Model MTC-1 or equivalent
R$_{sc}$	Select	1/2 watt carbon
*R$_L$'	Select	For minimum current of 1 mAdc
C$_O$	1.0 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C$_N$	0.1 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or equivalent
C$_c$	0.001 μF	
*C$_i$	0.01 μF	
Q1	MC1569R or MC1469R	
Q2	2N5223, 2N706, or equivalent	
*HS	–	Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board	–	Circuit Dot, Inc. #PC1113 1155 W. 23rd St., Tempe, Ariz. 85281
*Optional		

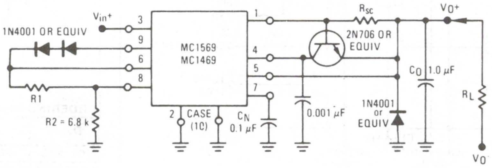
LATCH-UP

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between V_O^+ and V_O^- (This "common load" may be something inconspicuous – e.g. an operational amplifier. Nearly everyone who uses + and – voltages will have a common load from V_{CC} to V_{EE}.)
3. V_{in}^+ and V_{in}^- are not applied at the same time.

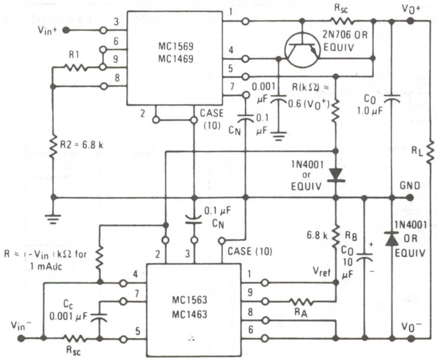
The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning ON. Latch-up can be prevented by the circuit configurations shown in Figures 44 and 45.

FIGURE – 44


Vin+
1N4001 OR EQUIV
R1
R2 = 6.8 k
MC1569
MC1469
3
9
6
8
2
CASE (10)
CN 0.1 μF
1
4
5
7
Rsc
2N706 OR EQUIV
0.001 μF
1N4001 or EQUIV
CO 1.0 μF
RL
VO+
VO

Note: This configuration increases minimum input-output differential voltage by ≈ 0.7 V.

FIGURE – 45


Vin+
R1
R2 = 6.8 k
MC1569
MC1469
3
6
9
8
2
CASE (10)
CN
0.1 μF
0.001 μF
1
4
5
7
Rsc
2N706 OR EQUIV
R(kΩ) ≈ 0.6 (VO+)
CO 1.0 μF
RL
VO+
1N4001 or EQUIV
GND
0.1 μF CN
R ≈ (-Vin) kΩ for 1 mAdc
Cc 0.001 μF
Vin−
Rsc
MC1563
MC1463
4
7
5
2
3
CASE (10)
1
9
8
6
6.8 k RB
CO 10 μF
Vref
RA
1N4001 OR EQUIV
VO−

MC1723
MC1723C

MOTOROLA

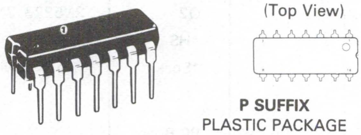
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

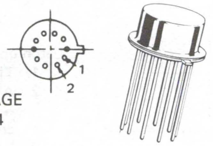
VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

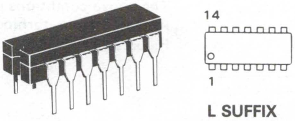


P SUFFIX
PLASTIC PACKAGE
CASE 646-05

(Top View)



G SUFFIX
METAL PACKAGE
CASE 603-04
(TO-100)

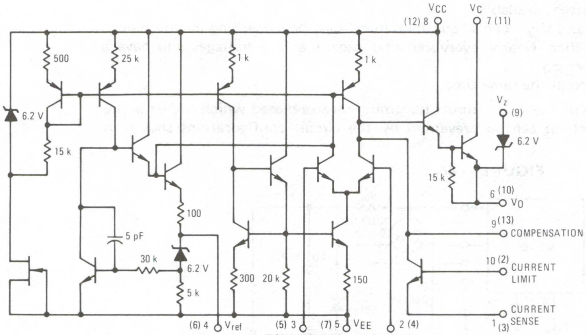


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

ORDERING INFORMATION

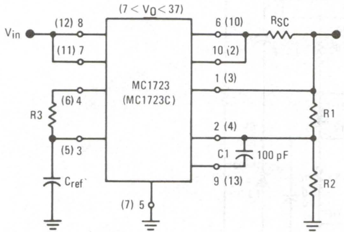
Device	Alternate	Temperature Range	Package
MC1723CG	LM723CH, μA723HC	0°C to 70°C	Metal Can
MC1723CL	LM723CD, μA723DC	0°C to +70°C	Ceramic DIP
MC1723CP	LM723CN, μA723PC	0°C to +70°C	Plastic DIP
MC1723G	–	-55°C to +125°C	Metal Can
MC1723L	–	-55°C to +125°C	Ceramic DIP

FIGURE 1 – CIRCUIT SCHEMATIC


VCC
(12) 8
VC
7 (11)
500
25 k
1 k
1 k
6.2 V
15 k
Vz
(9)
6.2 V
15 k
6 (10)
VO
9 (13)
COMPENSATION
100
5 pF
30 k
6.2 V
5 k
300
20 k
150
10 (2)
CURRENT LIMIT
CURRENT SENSE
1 (3)
(6) 4
Vref
(5) 3
NON-INVERTING INPUT
(7) 5
VEE
2 (4)
INVERTING INPUT

PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE;
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN-LINE PACKAGES.

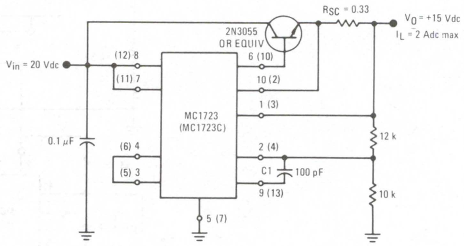
FIGURE 2 – TYPICAL CIRCUIT CONNECTION


(7 < VO < 37)
Vin
(12) 8
(11) 7
(6) 4
R3
(5) 3
Cref
MC1723
(MC1723C)
(7) 5
6 (10)
RSC
VO
10 (2)
1 (3)
R1
2 (4)
C1
100 pF
9 (13)
R2

$$V_O \cong 7\left(\frac{R1 + R2}{R2}\right) \qquad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}} \text{ at } T_J = +25^{\circ}C$$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION


RSC = 0.33
VO = +15 Vdc
IL = 2 Adc max
2N3055
OR EQUIV
Vin = 20 Vdc
(12) 8
(11) 7
0.1 μF
(6) 4
(5) 3
MC1723
(MC1723C)
5 (7)
6 (10)
10 (2)
1 (3)
12 k
2 (4)
C1
100 pF
9 (13)
10 k

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Non-Inverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	1.25	W
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Metal Package			
T_A = +25°C	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
Dual In-Line Ceramic Package			
P_D		1.5	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		−65 to +150	
Dual In-Line Ceramic and Ceramic Flat Packages		−65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +70	
MC1723		−55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							µV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 µF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① $< T_A < T_{high}$ ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{line}							%V_O
(T_A = +25°C) 12 V $< V_{in} <$ 15 V		–	0.01	0.1	–	0.01	0.1	
12 V $\leq V_{in} <$ 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① $< T_A < T_{high}$ ②) 12 V $< V_{in} <$ 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA $< I_L <$ 50 mA)	Reg_{load}							%V_O
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① $< T_A < T_{high}$ ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	RR							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 µF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{sc}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= −55°C for MC1723

② T_{high} = +70° C for MC1723C
= +125°C for MC1723

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

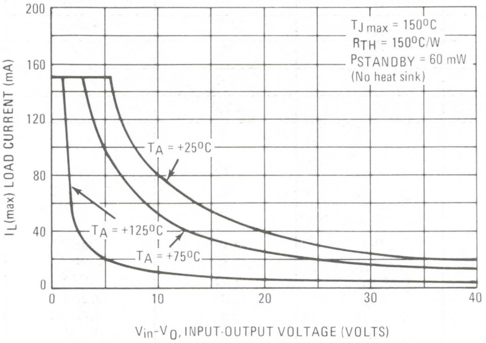


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

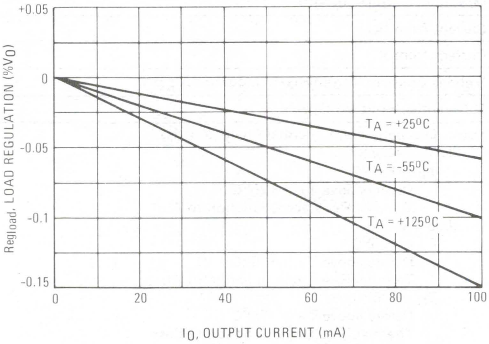


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

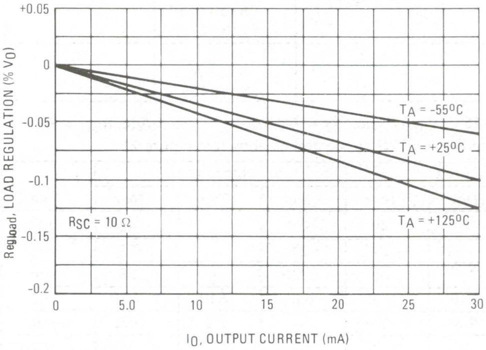


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

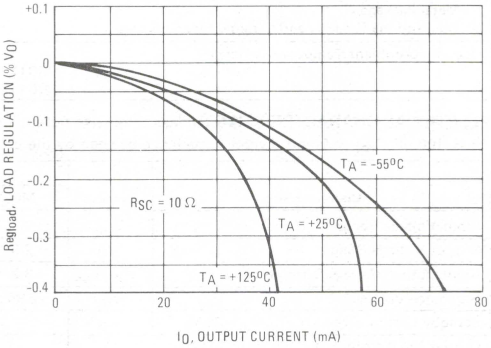


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

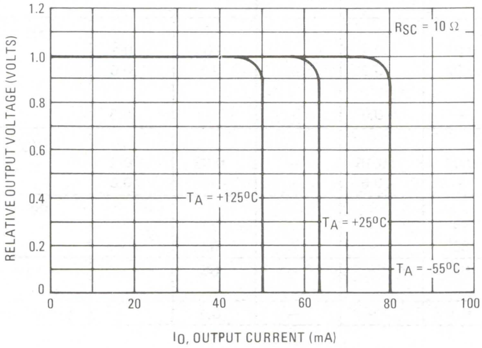
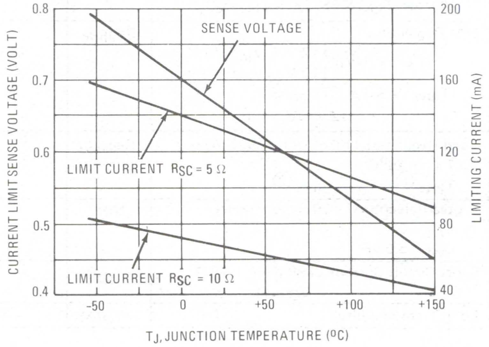


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

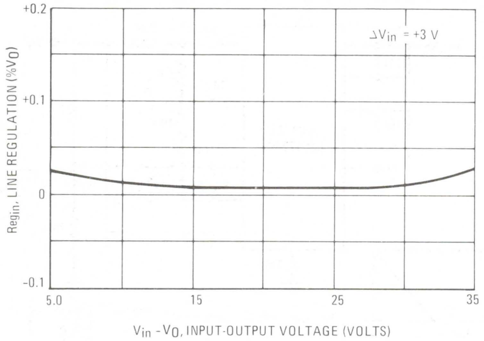


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

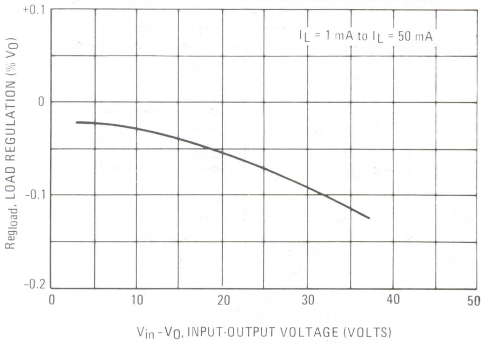


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

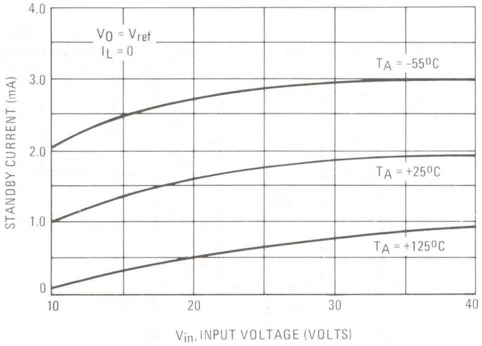


FIGURE 13 – LINE TRANSIENT RESPONSE

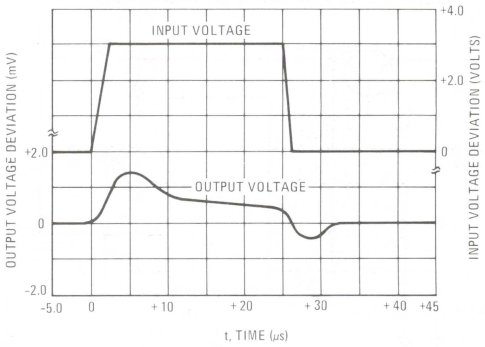


FIGURE 14 – LOAD TRANSIENT RESPONSE

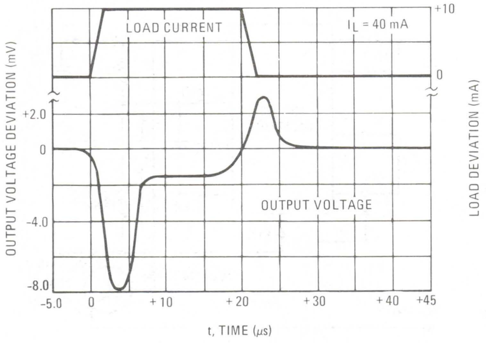
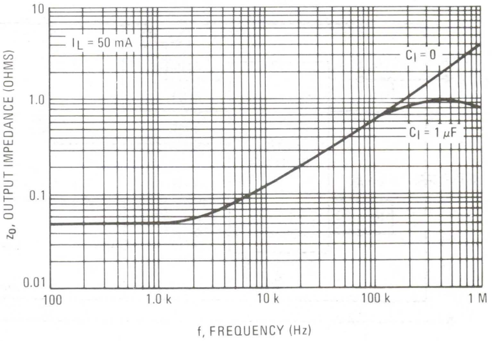


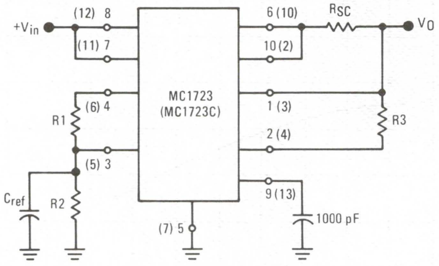
FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package;
pin numbers in parenthesis are for the dual in-line packages.

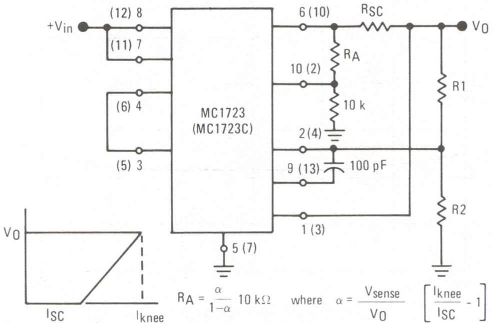
FIGURE 16 – TYPICAL CONNECTION FOR 2 < V_O < 7


+Vin
(12) 8
(11) 7
(6) 4
R1
(5) 3
Cref
R2
(7) 5
MC1723
(MC1723C)
6 (10)
RSC
VO
10 (2)
1 (3)
2 (4)
R3
9 (13)
1000 pF

$V_O \cong 7\left[\frac{R2}{R1 + R2}\right]$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at $T_J = +25^{o}C$

For best results 10 k < R1 + R2 < 100 k.
For minimum drift R3 = R1||R2.

FIGURE 17 – MC1723,C FOLDBACK CONNECTION


+Vin
(12) 8
(11) 7
(6) 4
(5) 3
MC1723
(MC1723C)
6 (10)
RSC
VO
RA
10 (2)
10 k
2 (4)
9 (13)
100 pF
1 (3)
5 (7)
R1
R2
VO
ISC
Iknee
IL

$R_A = \frac{\alpha}{1-\alpha}\ 10\ k\Omega$ where $\alpha = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-\alpha)\ I_{SC}}$

FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

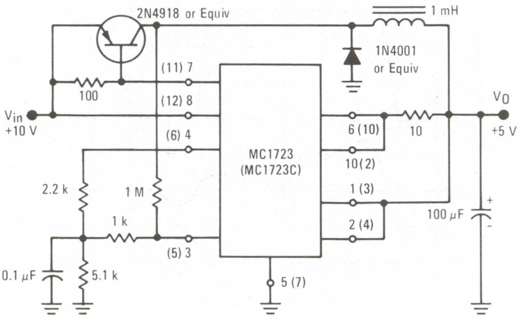

2N4918 or Equiv
1 mH
1N4001
or Equiv
100
(11) 7
(12) 8
(6) 4
Vin
+10 V
2.2 k
1 M
1 k
(5) 3
0.1 μF
5.1 k
MC1723
(MC1723C)
6 (10)
10
10 (2)
1 (3)
2 (4)
5 (7)
VO
+5 V
100 μF

FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

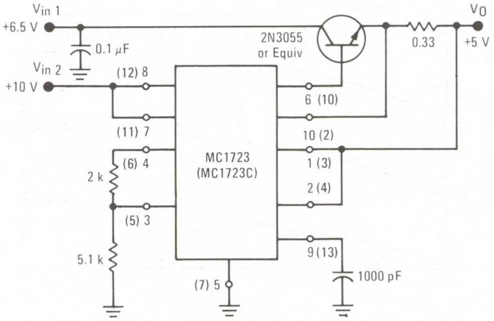

Vin 1
+6.5 V
0.1 μF
Vin 2
+10 V
(12) 8
(11) 7
(6) 4
2 k
(5) 3
5.1 k
(7) 5
MC1723
(MC1723C)
2N3055
or Equiv
6 (10)
10 (2)
1 (3)
2 (4)
9 (13)
1000 pF
0.33
VO
+5 V

FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

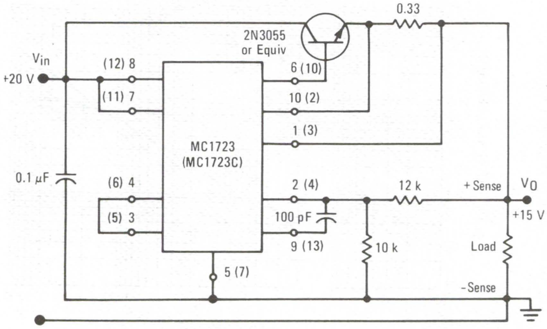
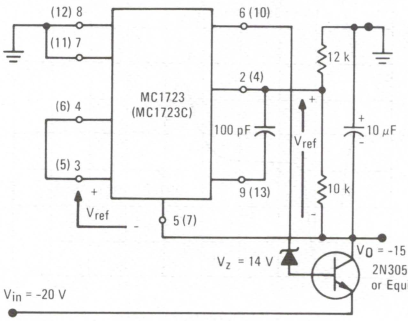
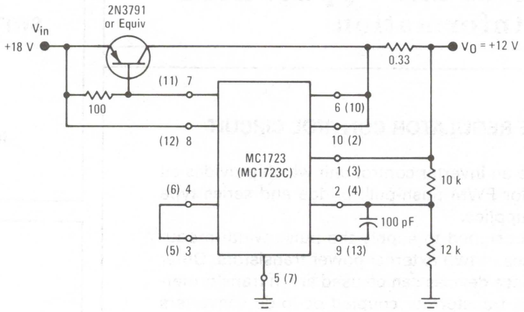

Vin
+20 V
(12) 8
(11) 7
0.1 μF
(6) 4
(5) 3
MC1723
(MC1723C)
2N3055
or Equiv
0.33
6 (10)
10 (2)
1 (3)
2 (4)
100 pF
9 (13)
5 (7)
12 k
10 k
+ Sense
VO
+15 V
Load
-Sense

FIGURE 21 – –15 V NEGATIVE REGULATOR


(12) 8
(11) 7
(6) 4
(5) 3
Vref
MC1723
(MC1723C)
6 (10)
2 (4)
100 pF
9 (13)
5 (7)
Vref
12 k
10 k
10 μF
Vz = 14 V
VO = -15 V
2N3055
or Equiv
Vin = -20 V

TYPICAL APPLICATIONS (continued)

FIGURE 22 — +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST


2N3791
or Equiv
V_{in}
+18 V
V_O = +12 V
0.33
100
(11) 7
(12) 8
6 (10)
10 (2)
MC1723
(MC1723C)
1 (3)
2 (4)
(6) 4
(5) 3
9 (13)
5 (7)
10 k
100 pF
12 k

MC3420
MC3520

MOTOROLA

Specifications and Applications Information

SWITCHMODE REGULATOR CONTROL CIRCUIT

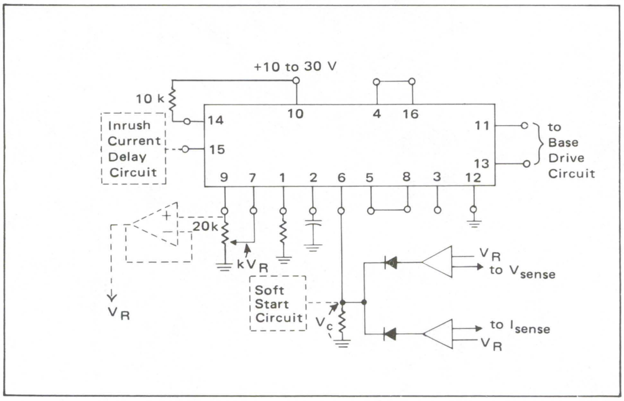
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the bases of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of −55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

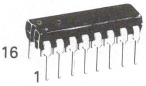
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2.0 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1—TYPICAL APPLICATION

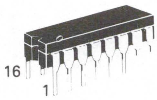

+10 to 30 V
10 k
Inrush Current Delay Circuit
14
15
10
4
16
11
13
to Base Drive Circuit
9
7
1
2
6
5
8
3
12
20k
kV_R
V_R
Soft Start Circuit
V_c
V_R
to V_sense
to I_sense
V_R

SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUITS

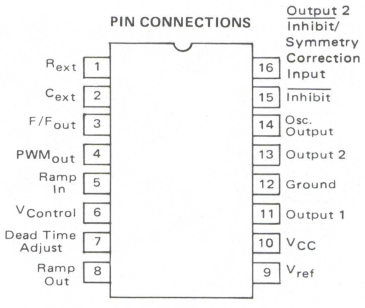


P SUFFIX
PLASTIC PACKAGE
CASE 648-05
(MC3420
only)



L SUFFIX
CERAMIC PACKAGE
CASE 620-02

PIN CONNECTIONS


R_ext 1
C_ext 2
F/F_out 3
PWM_out 4
Ramp In 5
V_Control 6
Dead Time Adjust 7
Ramp Out 8
16 Output 2 Inhibit/ Symmetry Correction Input
15 Inhibit
14 Osc. Output
13 Output 2
12 Ground
11 Output 1
10 V_CC
9 V_ref

(Top View)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature	T_J			°C
Plastic Package		–	125	
Ceramic Package		150	150	
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 to 30 V, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520			MC3420			Unit
			Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION									
Reference Voltage (I_{ref} = 400 μA)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage (V_{CC} = 15 V, I_{ref} = 400 μA)	5	TCV_{ref}	–	0.008	0.03	–	0.008	0.03	%/°C
Input Regulation of Reference Voltage	5	Reg_{line}							mV/V
(I_{ref} = 400 μA)			–	3.0	7.5	–	4.0	7.5	
(I_{ref} = 1.0 mA)			–	5.0	–	–	5.0	–	
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	–	30	10	–	30	V
Supply Current (R_{ext} = 10 kΩ, excluding load and current and reference current)	5	I_D	–	–	16	–	–	22	mA
OSCILLATOR SECTION									
Line Frequency Stability	5								
(f = 20 kHz)		Δf	–	–	3.0	–	–	5.0	%
(f = 20 kHz, V_{CC} = 15 V, T_{low} to T_{high})		Δf	–	0.03	–	–	0.04	–	%/°C
Maximum Output Frequency (V_{CC} = 15 V)	6	f_{max}	100	200	–	100	200	–	kHz
Minimum Output Frequency (V_{CC} = 15 V)	6	f_{min}	–	2.0	5.0	–	2.0	5.0	kHz
Oscillator Output Saturation Voltage ($I_{14\ sink}$ = 5.0 mA)	11	$V_{osc(sat)}$	–	0.2	0.5	–	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage	7	$V_{CE(sat)}$							V
(I_L = 40 mA, T_{high} to T_{low})			–	0.33	0.5	–	0.33	0.5	
(I_L = 25 mA, T_{high} to T_{low})			–	0.22	–	–	0.22	–	
Output Leakage Current (V_{CE} = 40 V, Pins 11 and 13)	8	I_{CE}	–	–	50	–	–	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	–	100	0	–	100	%
Dead Time Adjustment Range	9	ΔDT	0	–	100	0	–	100	%
Temperature Coefficient of Dead Time	–	TCDT	–	0.1	–	–	0.1	–	%/°C
Comparator Bias Currents	12, 13	I_{IB}	–	5.0	15	–	5.0	15	μA
	14	I_{IB}	–	10	30	–	10	30	μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
AUXILIARY INPUTS/OUTPUTS									
Ramp Voltage Peak High Peak Low	5	 $V_{ramp(Hi)}$ $V_{ramp(Low)}$	 5.5 2.0	 6.0 2.4	 6.5 2.8	 5.5 2.0	 6.0 2.4	 6.5 2.8	V
Ramp Voltage Change ($V_{ramp\ Hi} - V_{ramp\ Low}$)	5	ΔV_{ramp}	3.0	3.5	4.0	3.0	3.5	4.0	V
Ramp Out Sink Current	5	I_{sink}	—	400	—	—	400	—	µA
Ramp Out Source Current	5	I_{source}	—	3.0	—	—	3.0	—	mA
$\overline{\text{Inhibit}}$ Input Current — High (V_{IH} = 2.0 V)	10	I_{IH}	—	—	40	—	—	40	µA
$\overline{\text{Inhibit}}$ Input Current — Low (V_{IL} = 0.8 V)	10	I_{IL}	—	-25	-180	—	-25	-180	µA
Symmetry Correction Input/Output 2 Inhibit Current — High (V_{SY} = 2.0 V, Pin 16)	10	$I_{SY/H}$	—	—	40	—	—	40	µA
Symmetry Correction Input/Output 2 Inhibit Current — Low (V_{SY} = 0.8 V, Pin 16)	10	$I_{SY/L}$	—	-10	-180	—	-10	-180	µA
F/F$_{out}$ Source Current	—	I_{source}	—	2.0	—	—	2.0	—	mA
OUTPUT AC CHARACTERISTICS ($T_A = T_{high}$, V_{CC} = +15 V, f = 20 kHz)									
Rise Time	15	t_r	—	40	—	—	40	—	ns
Fall Time	15	t_f	—	150	—	—	150	—	ns
Overlap Time	15	t_{ov}	—	275	—	—	275	—	ns
Assymmetry (Duty Cycle = 50%)	15	$\frac{t_{on1} - t_{on2}}{t_{on1}}$	—	±1.0	—	—	±1.0	—	%

NOTE:

T_{high} = +125°C for MC3520
+70°C for MC3420

T_{low} = -55°C for MC3520
0°C for MC3420

FIGURE 2—EQUIVALENT CIRCUIT

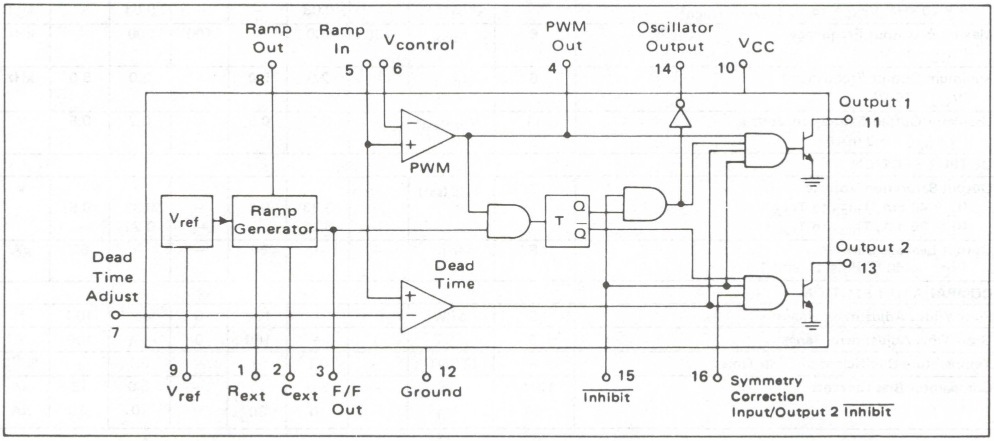
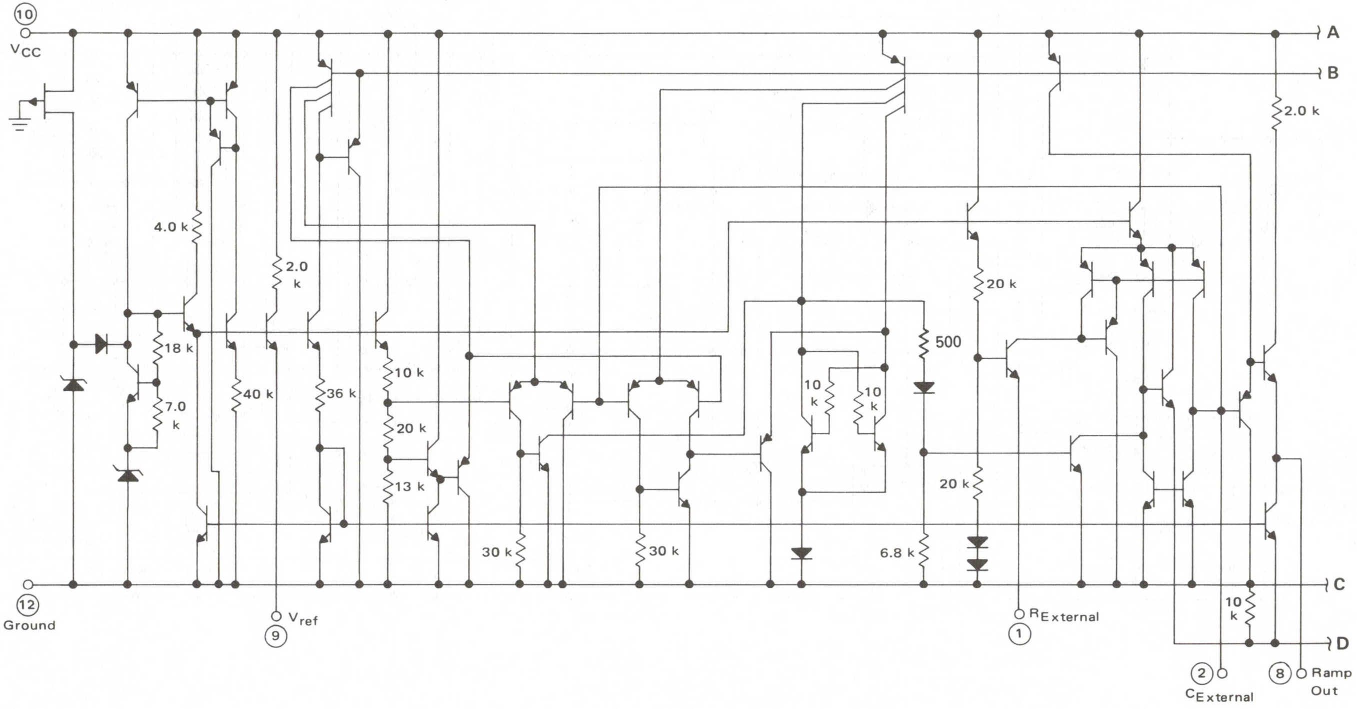
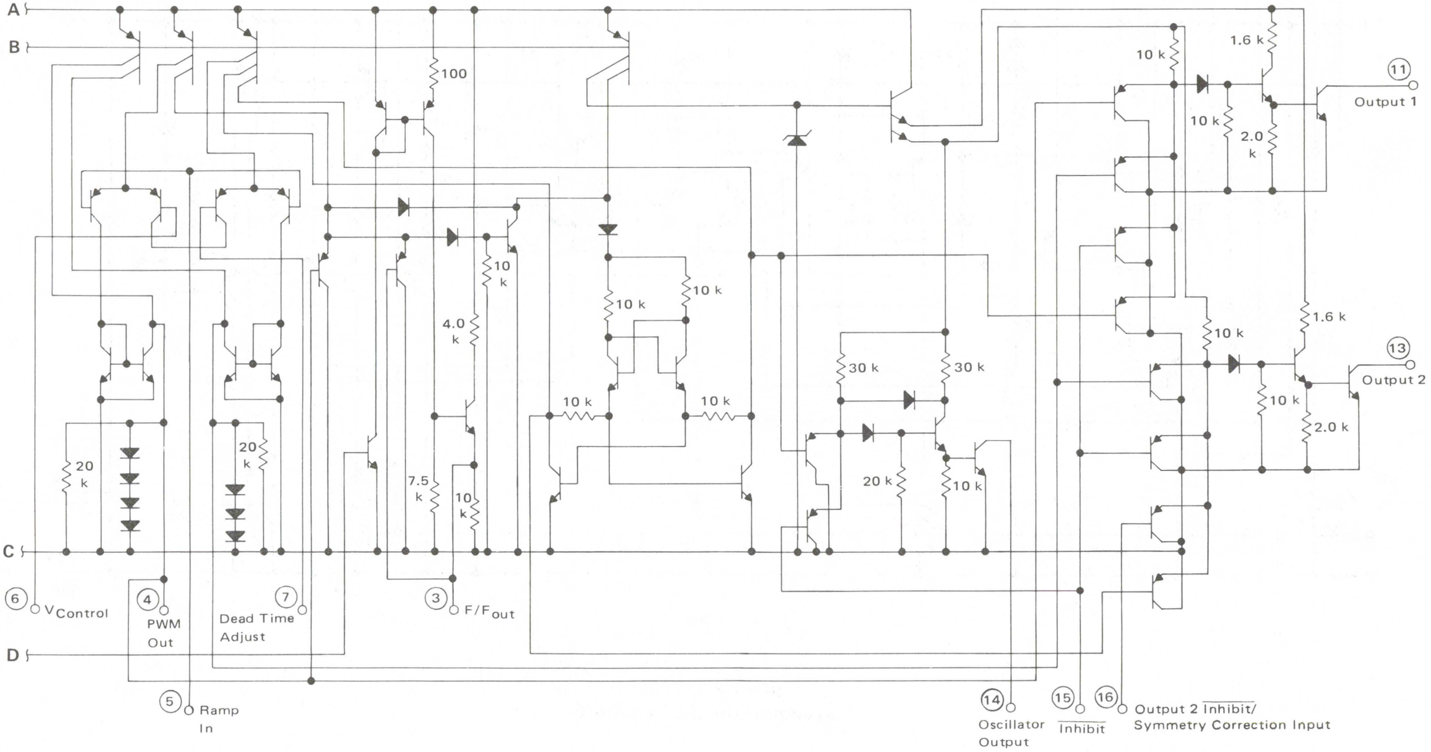

Ramp Out
8
Ramp In
5
$V_{control}$
6
PWM Out
4
Oscillator Output
14
V_{CC}
10
Output 1
11
PWM
V_{ref}
Ramp Generator
T
Q
$\overline{Q}$
Dead Time
Output 2
13
Dead Time Adjust
7
9
V_{ref}
1
R_{ext}
2
C_{ext}
3
F/F Out
12
Ground
15
$\overline{\text{Inhibit}}$
16
Symmetry Correction Input/Output 2 $\overline{\text{Inhibit}}$

FIGURE 3 – CIRCUIT SCHEMATIC

(continued next page)


10
VCC
A
B
2.0 k
4.0 k
2.0 k
18 k
7.0 k
40 k
36 k
10 k
20 k
13 k
30 k
30 k
10 k
10 k
500
20 k
20 k
6.8 k
C
10 k
D
12
Ground
9
Vref
1
RExternal
2
CExternal
8
Ramp Out

(continued) FIGURE 3 – CIRCUIT SCHEMATIC


A
B
C
D
100
10 k
1.6 k
10 k
10 k
2.0 k
11
Output 1
13
Output 2
10
k
10 k
10 k
4.0
k
10 k
10 k
30 k
30 k
1.6 k
10 k
10 k
2.0 k
20
k
20
k
7.5
k
10
k
20 k
10 k
6
VControl
4
PWM
Out
7
Dead Time
Adjust
3
F/Fout
5
Ramp
In
14
Oscillator
Output
15
$\overline{\text{Inhibit}}$
16
Output 2 $\overline{\text{Inhibit}}$/
Symmetry Correction Input

GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

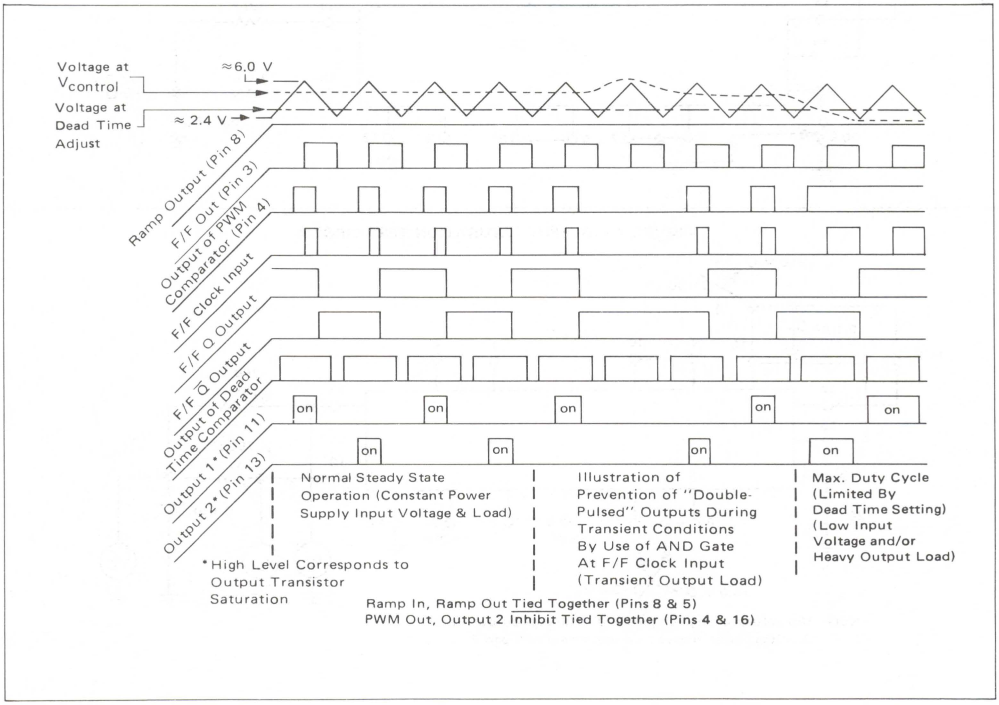
Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS


Voltage at
$V_{control}$
Voltage at
Dead Time
Adjust
≈6.0 V
≈ 2.4 V
Ramp Output (Pin 8)
F/F Out (Pin 3)
Output of PWM Comparator (Pin 4)
F/F Clock Input
F/F Q Output
F/F $\bar{Q}$ Output
Output of Dead Time Comparator
Output 1* (Pin 11)
Output 2* (Pin 13)
on
on
on
on
on
on
on
on
on
Normal Steady State Operation (Constant Power Supply Input Voltage & Load)
Illustration of Prevention of "Double-Pulsed" Outputs During Transient Conditions By Use of AND Gate At F/F Clock Input (Transient Output Load)
Max. Duty Cycle (Limited By Dead Time Setting) (Low Input Voltage and/or Heavy Output Load)

*High Level Corresponds to Output Transistor Saturation

Ramp In, Ramp Out Tied Together (Pins 8 & 5)
PWM Out, Output 2 Inhibit Tied Together (Pins 4 & 16)

FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

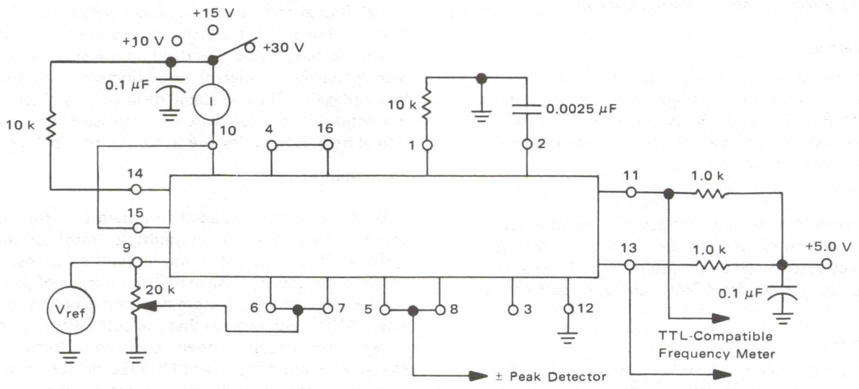

+15 V
+10 V
+30 V
0.1 µF
I
10 k
10
4
16
10 k
0.0025 µF
1
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
Vref
20 k
6
7
5
8
3
12
TTL-Compatible
Frequency Meter
± Peak Detector

FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

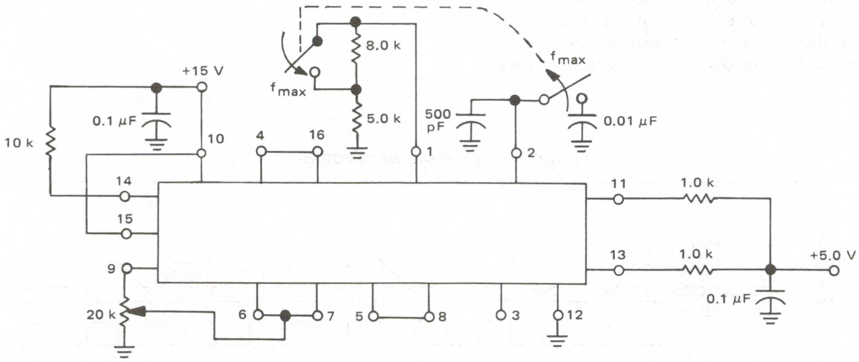
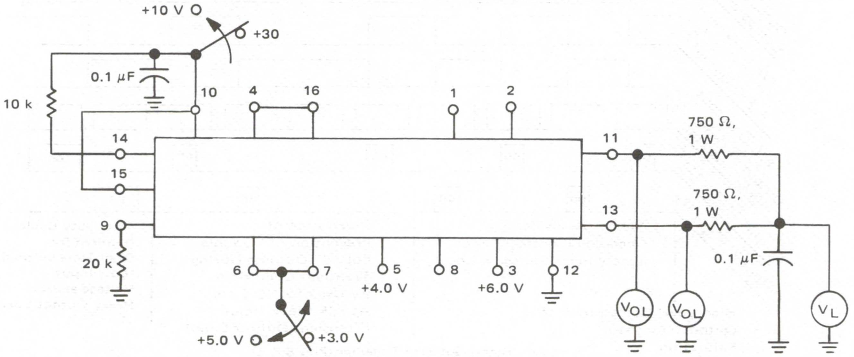
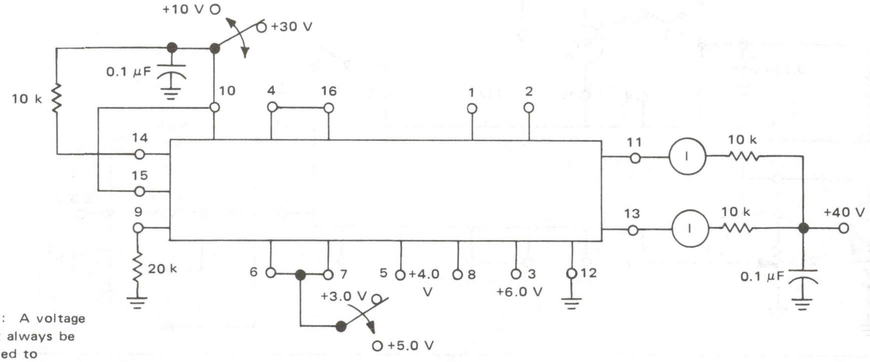

8.0 k
fmax
fmax
+15 V
0.1 µF
10 k
5.0 k
500 pF
0.01 µF
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
20 k
6
7
5
8
3
12

FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT


+10 V
+30
0.1 µF
10 k
10
4
16
1
2
14
15
9
20 k
11
750 Ω,
1 W
13
750 Ω,
1 W
0.1 µF
6
7
5
+4.0 V
8
3
+6.0 V
12
VOL
VOL
VL
+5.0 V
+3.0 V

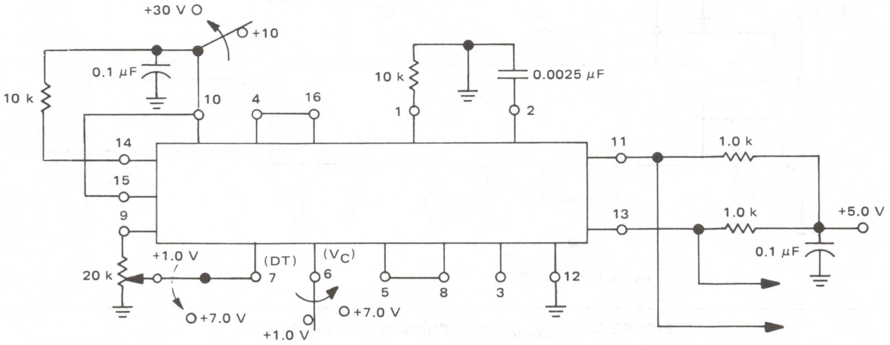
Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT


+10 V
+30 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
13
10 k
10 k
+40 V
20 k
6
7
5
+4.0 V
8
3
+6.0 V
12
+3.0 V
+5.0 V
0.1 µF

Note: A voltage must always be applied to pins 6 and 7.

FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT


+30 V
+10
0.1 µF
10 k
10
4
16
10 k
1
0.0025 µF
2
14
15
9
11
13
1.0 k
1.0 k
+5.0 V
0.1 µF
20 k
+1.0 V
(DT)
7
(V_C)
6
5
8
3
12
+7.0 V
+7.0 V
+1.0 V

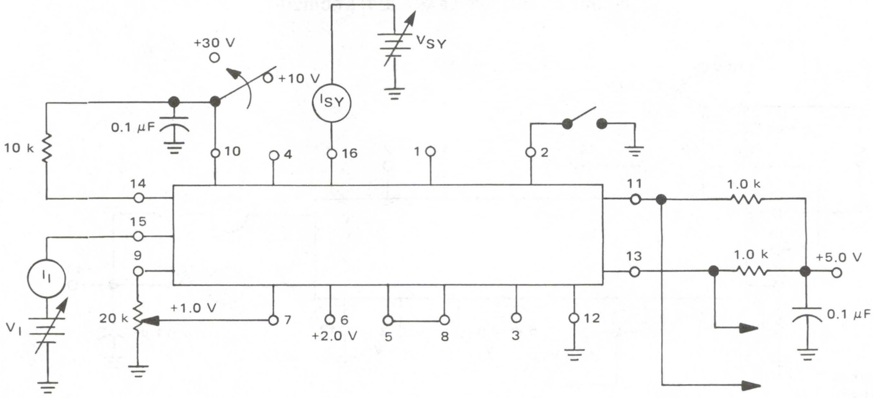
TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{control}$ = 2.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50
2.5	46
3.0	40
3.5	33
4.0	26
4.5	18
5.0	11
5.5	4.0
6.0	0

TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$)	
PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50
2.5	46
3.0	40
3.5	33
4.0	26
4.5	18
5.0	11
5.5	4.0
6.0	0

	V_6	V_7	
	Volts		
100% Adjust			
Dead Time	1.0	1.0	(Pin 11 + Pin 13 = Logic "1")
Pulse Width	1.0	1.0	
0% Adjust			
Dead Time	7.0	1.0	(Pin 11)(Pin 13) = Logic "1"
Pulse Width	1.0	7.0	

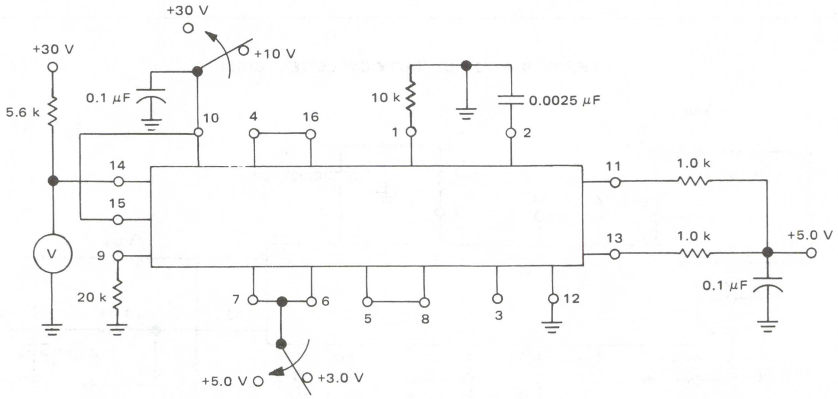
NOTE: Logic "1" is TTL-Compatible V_{OH}.

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT



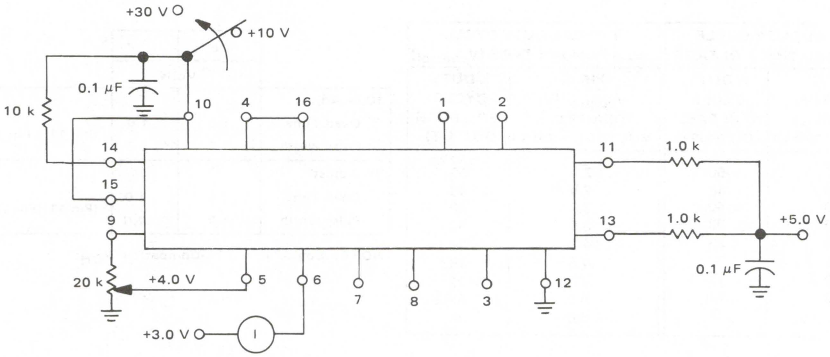
+30 V
+10 V
V_{SY}
I_{SY}
0.1 μF
10 k
10
4
16
1
2
14
11
1.0 k
15
9
13
1.0 k
+5.0 V
I_I
20 k
+1.0 V
7
6
+2.0 V
5
8
3
12
0.1 μF
V_I

FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT



+30 V
+30 V
+10 V
5.6 k
0.1 μF
10
4
16
10 k
1
0.0025 μF
2
14
11
1.0 k
15
V
9
13
1.0 k
+5.0 V
0.1 μF
20 k
7
6
5
8
3
12
+5.0 V
+3.0 V

FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT



+30 V
+10 V
0.1 μF
10 k
10
4
16
1
2
14
11
1.0 k
15
9
13
1.0 k
+5.0 V
20 k
+4.0 V
5
6
7
8
3
12
0.1 μF
+3.0 V
I

FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

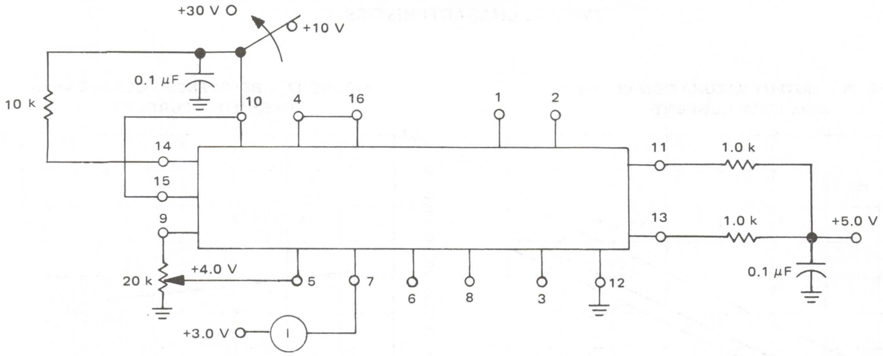

+30 V
+10 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
20 k
+4.0 V
5
7
6
8
3
12
+3.0 V
I

FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

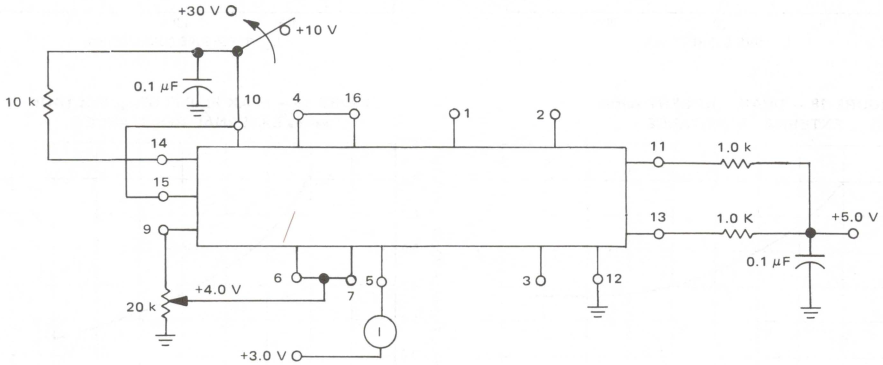
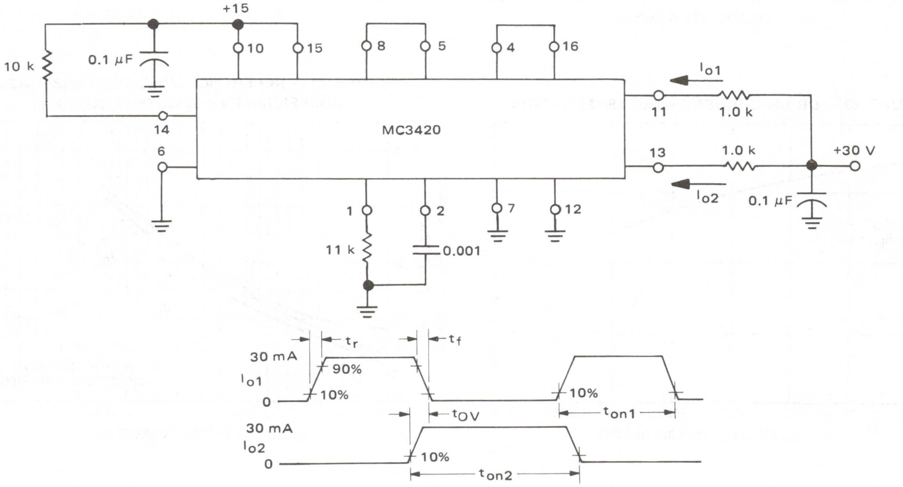

+30 V
+10 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 K
+5.0 V
0.1 µF
6
7
5
3
12
+4.0 V
20 k
I
+3.0 V

FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS


+15
10 k
0.1 µF
10
15
8
5
4
16
Io1
11
1.0 k
14
MC3420
6
13
1.0 k
+30 V
Io2
0.1 µF
1
2
7
12
11 k
0.001
tr
tf
30 mA
90%
Io1
0
10%
10%
tOV
ton1
30 mA
Io2
0
10%
ton2

TYPICAL CHARACTERISTICS

FIGURE 16 – OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

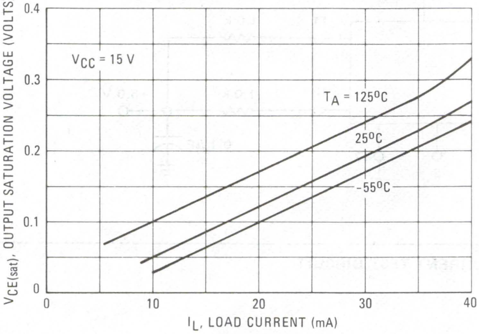


FIGURE 17 – REFERENCE VOLTAGE versus REFERENCE CURRENT

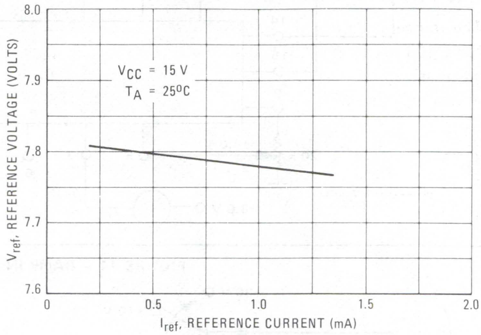


FIGURE 18 – DRAIN CURRENT versus EXTERNAL RESISTANCE

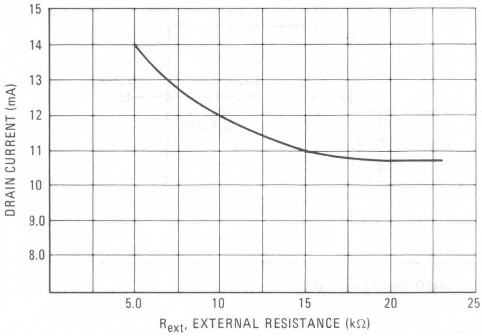


FIGURE 19 – PEAK FLIP-FLOP$_{out}$ VOLTAGE versus EXTERNAL RESISTANCE

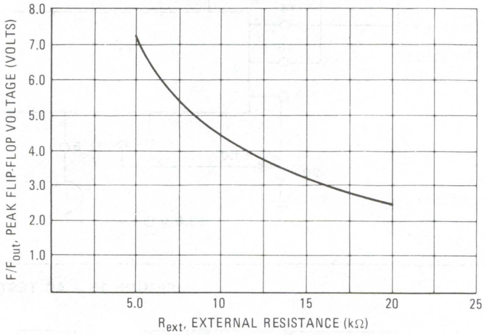


FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

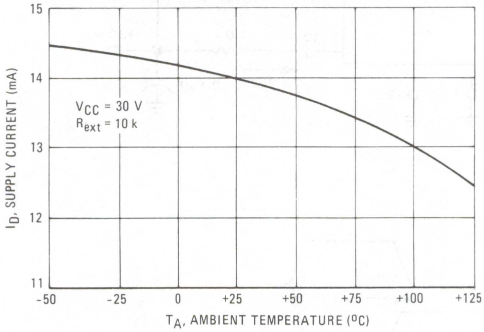
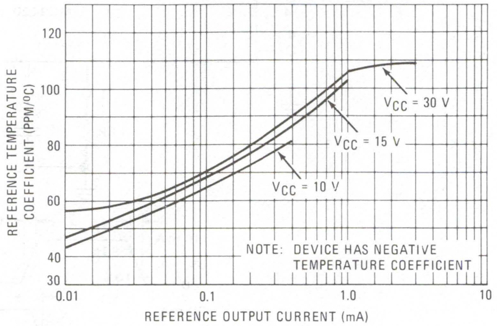


FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE COEFFICIENT versus OUTPUT CURRENT

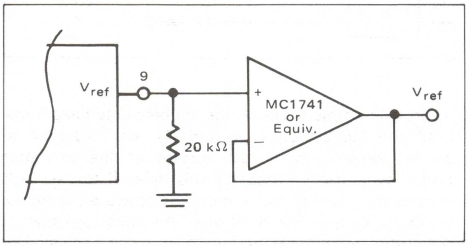


OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a 400 μA ($\cong$20 kΩ) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22


Vref
9
+
MC1741
or
Equiv.
−
20 kΩ
Vref

Output Frequency

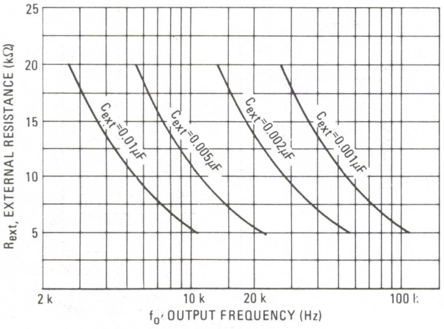
The values of R_{ext} and C_{ext} for a given output frequency, f_o, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}}\;;\; 5.0\text{ k}\Omega \leqslant R_{ext} \leqslant 20\text{ k}\Omega \quad \text{(Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o.

FIGURE 23

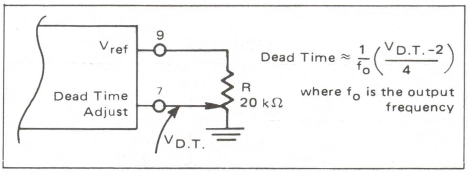


Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

Pin 7 should always be tied to some voltage between Gnd and V_{ref}.

FIGURE 24


Vref
9
Dead Time
Adjust
7
R
20 kΩ
VD.T.
Dead Time ≈ 1/fo ((VD.T. − 2)/4)
where fo is the output frequency

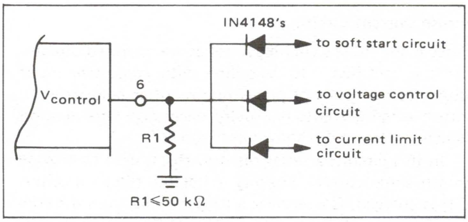
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is $\leqslant$ 50 kΩ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \cong \frac{V_{Control} - 2}{4} \times 100 \qquad \text{(Eq. 2)}$$

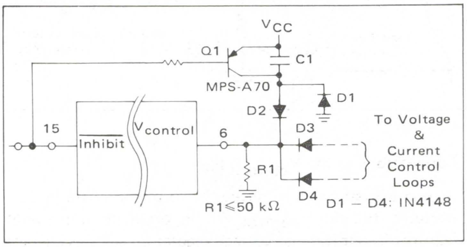
FIGURE 25


IN4148's
to soft start circuit
Vcontrol
6
to voltage control circuit
R1
to current limit circuit
R1⩽50 kΩ

Soft Start

In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 26.

FIGURE 26

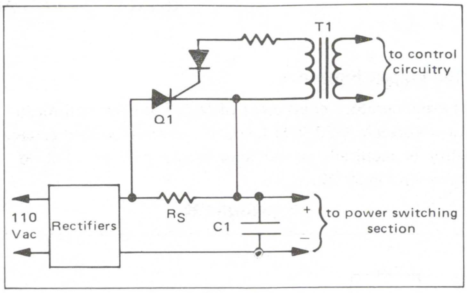

V_CC
Q1
C1
MPS-A70
D1
D2
D3
15
Inhibit
V_control
6
R1
D4
To Voltage & Current Control Loops
R1≤50 kΩ
D1 – D4: IN4148

After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from V_{CC} toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power (V_{CC}) is turned off.

Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 27.

FIGURE 27

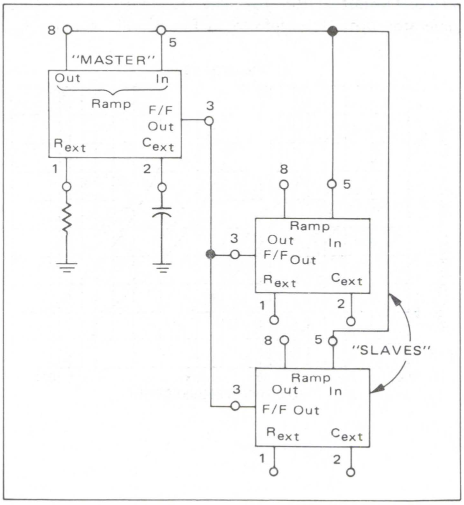

T1
to control circuitry
Q1
110 Vac
Rectifiers
R_S
C1
+
–
to power switching section

In this circuit, a series resistor, R_S, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts R_S out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 28. By omitting their R_{ext} and C_{ext}, up to two MC3420s may be slaved to a master MC3420.

FIGURE 28 – SLAVING THE MC3420


8
5
"MASTER"
Out
In
Ramp
F/F Out
3
R_ext
C_ext
1
2
8
5
Ramp
Out
In
3
F/F Out
R_ext
C_ext
1
2
8
5
"SLAVES"
Ramp
Out
In
3
F/F Out
R_ext
C_ext
1
2

15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in}, at a frequency of ≅ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, fo is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o.

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC}, Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC}; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≅ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≅ 5 µs each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

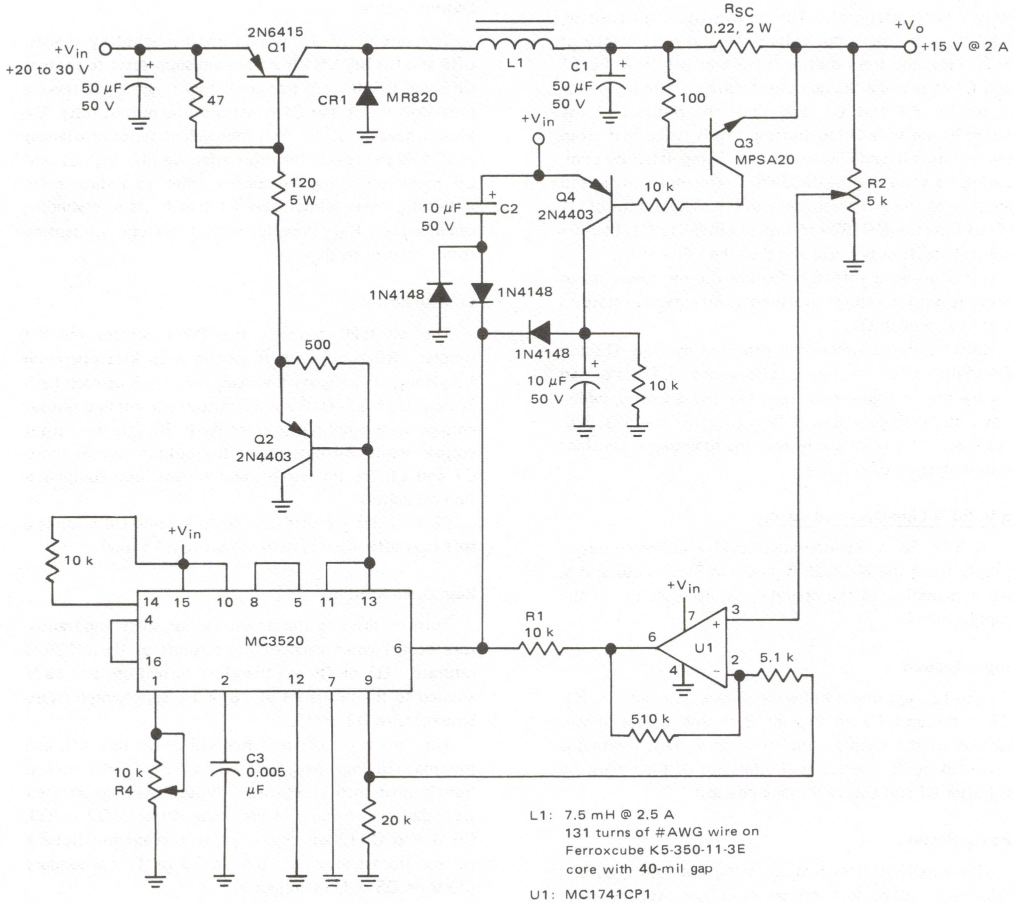
Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

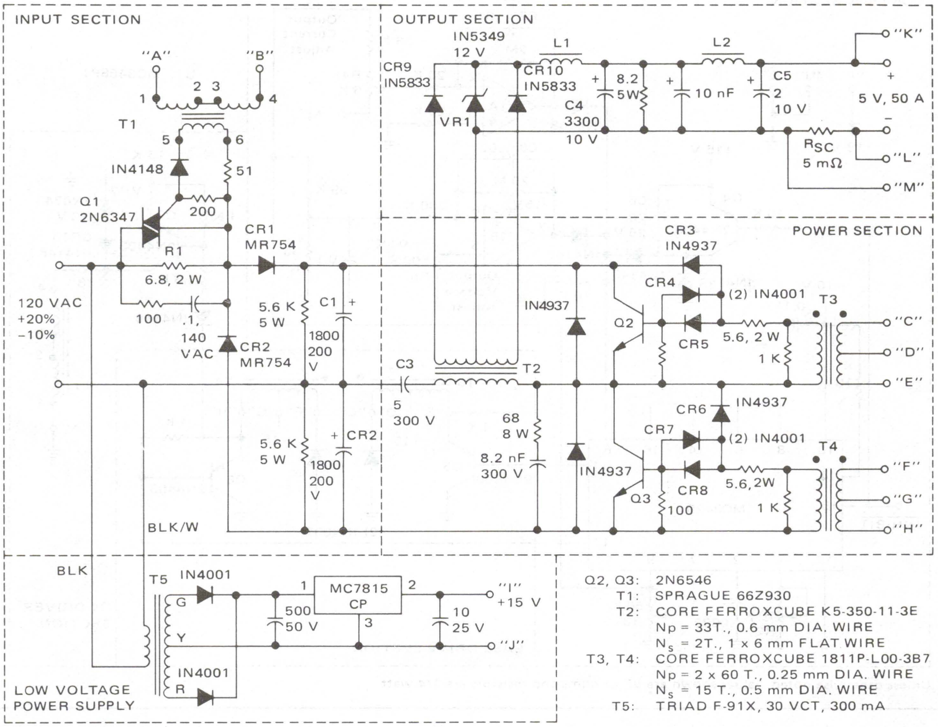
FIGURE 29 – 15 V, 2A DC-TO-DC CONVERTER


+Vin
+20 to 30 V
50 μF
50 V
47
2N6415
Q1
CR1
MR820
L1
C1
50 μF
50 V
RSC
0.22, 2 W
+Vo
+15 V @ 2 A
100
Q3
MPSA20
+Vin
Q4
2N4403
10 k
R2
5 k
120
5 W
10 μF
50 V
C2
1N4148
1N4148
1N4148
10 μF
50 V
10 k
500
Q2
2N4403
+Vin
10 k
MC3520
14 15 10 8 5 11 13
4
16
1 2 12 7 9
6
R1
10 k
+Vin
U1
7
3
6
4
2
5.1 k
510 k
10 k
R4
C3
0.005
μF
20 k

L1: 7.5 mH @ 2.5 A
131 turns of #AWG wire on
Ferroxcube K5-350-11-3E
core with 40-mil gap

U1: MC1741CP1

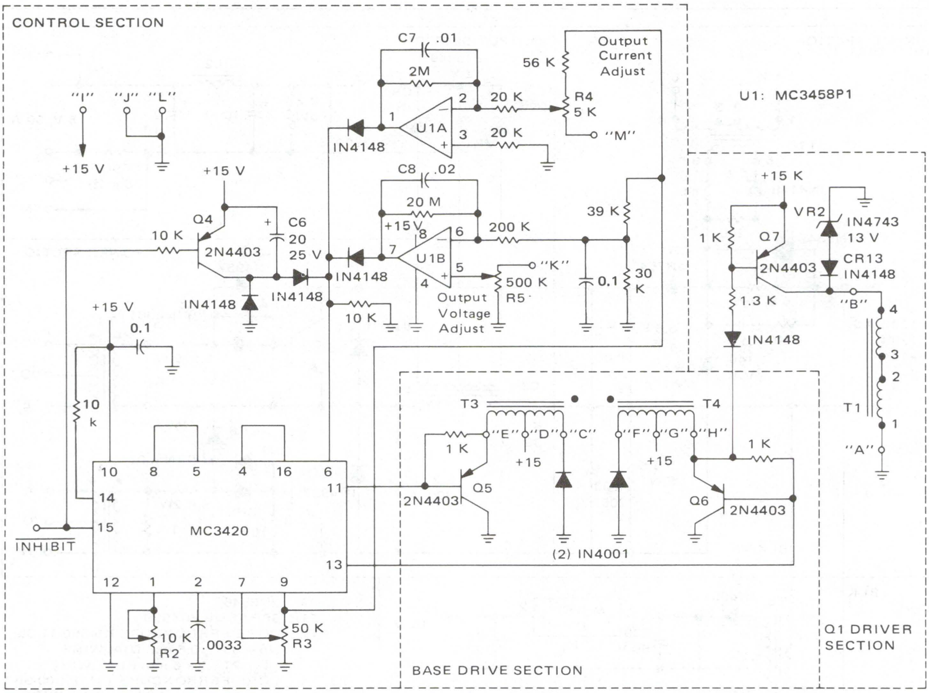
FIGURE 30a – 5 V, 50A LINE-OPERATED SUPPLY (continued on following page)


INPUT SECTION
"A"
"B"
1
2 3
4
T1
5
6
IN4148
51
Q1
2N6347
200
R1
6.8, 2 W
CR1
MR754
120 VAC
+20%
–10%
100
.1,
140 VAC
CR2
MR754
5.6 K
5 W
C1
1800
200 V
5.6 K
5 W
CR2
1800
200 V
BLK/W
OUTPUT SECTION
IN5349
12 V
CR9
IN5833
VR1
CR10
IN5833
L1
L2
C4
3300
10 V
8.2
5W
10 nF
C5
2
10 V
"K"
5 V, 50 A
RSC
5 mΩ
"L"
"M"
POWER SECTION
CR3
IN4937
CR4
(2) IN4001
T3
IN4937
Q2
CR5
5.6, 2 W
1 K
"C"
"D"
"E"
C3
5
300 V
T2
68
8 W
8.2 nF
300 V
CR6
IN4937
CR7
(2) IN4001
T4
IN4937
Q3
CR8
100
5.6,2W
1 K
"F"
"G"
"H"
BLK
T5
IN4001
G
Y
R
IN4001
1
MC7815
CP
2
3
500
50 V
10
25 V
"I"
+15 V
"J"
LOW VOLTAGE
POWER SUPPLY
Q2, Q3: 2N6546
T1: SPRAGUE 66Z930
T2: CORE FERROXCUBE K5-350-11-3E
Np = 33T., 0.6 mm DIA. WIRE
Ns = 2T., 1 x 6 mm FLAT WIRE
T3, T4: CORE FERROXCUBE 1811P-L00-3B7
Np = 2 x 60 T., 0.25 mm DIA. WIRE
Ns = 15 T., 0.5 mm DIA. WIRE
T5: TRIAD F-91X, 30 VCT, 300 mA

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

Performance	
Line Regulation:	0.4%
Load Regulation:	0.25%
Output Ripple and Noise:	60 mV p-p 25 mV rms
Line current surge at turn-on:	35 A max
Efficiency:	80%

FIGURE 30b


CONTROL SECTION
C7 .01
2M
56 K
Output Current Adjust
R4 5 K
"M"
20 K
20 K
U1A
IN4148
"I" "J" "L"
+15 V
+15 V
U1: MC3458P1
C8 .02
20 M
+15 V
U1B
200 K
39 K
"K"
500 K R5
0.1
30 K
Output Voltage Adjust
10 K
Q4
2N4403
10 K
C6 20 25 V
IN4148
IN4148
IN4148
+15 V
0.1
10 k
+15 K
VR2
IN4743 13 V
CR13 IN4148
1 K
Q7
2N4403
1.3 K
IN4148
"B"
4
3
2
1
T1
"A"
T3
T4
"E" "D" "C"
"F" "G" "H"
1 K
+15
+15
1 K
Q5
2N4403
Q6
2N4403
(2) IN4001
MC3420
10 8 5 4 16 6
11
14
15
13
12 1 2 7 9
INHIBIT
10 K R2
.0033
50 K R3
BASE DRIVE SECTION
Q1 DRIVER SECTION

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

Series Configuration

The single transistor series configuration is shown in Figure 1A. This configuration is usually limited to applications in which $0.2\ V_{CC} < V_o < 0.8\ V_{CC}$ and where input-output isolation is not required.

Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC}, and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors which have twice the current and half the voltage requirements as those of the push-pull configuration.

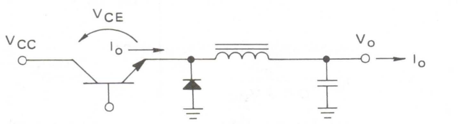
Full-Bridge Configuration

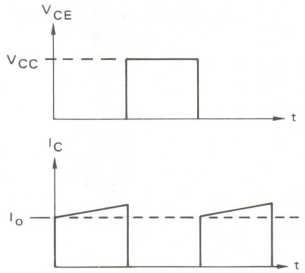
By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C:	Switching transistor collector current
V_{CE}:	Switching transistor collector-to-emitter-voltage
P_{in}:	Average input power
D.C.:	Inverter duty cycle
V_{CC}:	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX}:	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A – SERIES CONFIGURATION





TRANSISTOR REQUIREMENTS*

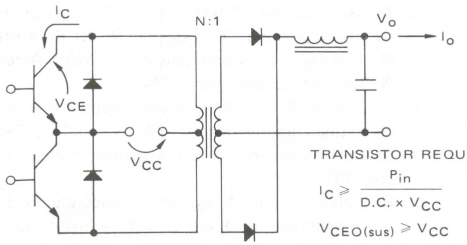
$I_C \geqslant I_O$

$V_{CEO(sus)} \geqslant V_{CC}$

$V_{CEX} \geqslant V_{CC}$

*See explanation of abbreviations in text.

FIGURE 2A – PUSH-PULL CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geqslant \frac{P_{in}}{D.C. \times V_{CC}}$$

$V_{CEO(sus)} \geqslant V_{CC}$

$V_{CEX} \geqslant 2\,V_{CC}$

*See explanation of abbreviations in text.

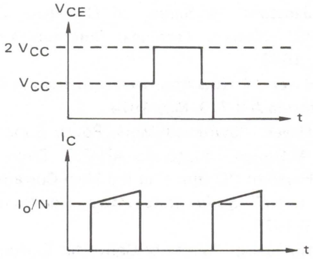
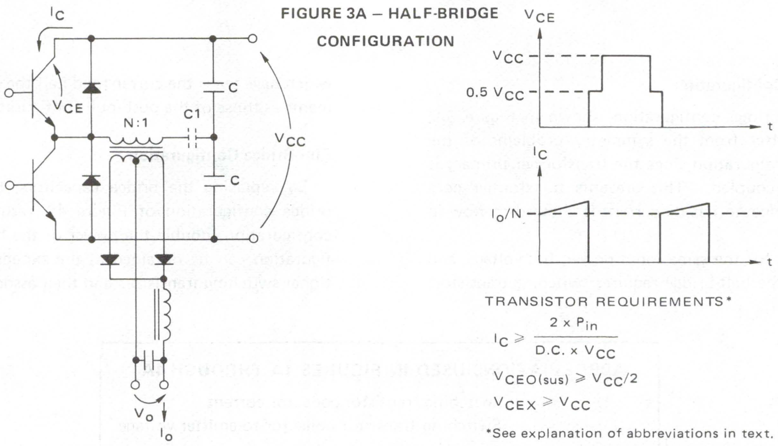


FIGURE 3A – HALF-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

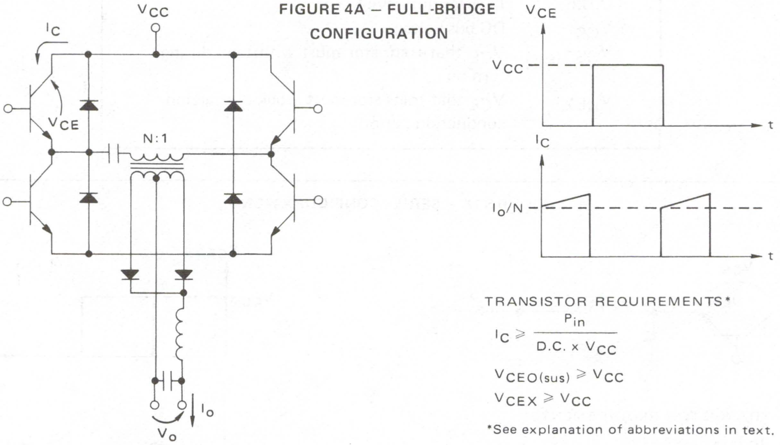
$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}/2$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

FIGURE 4A – FULL-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion,* March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion,* March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hetterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2,* October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3,* June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.

MOTOROLA

MC3423
MC3523

Specifications and Applications Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

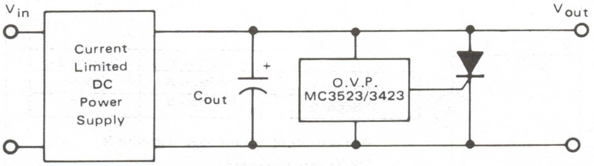
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 −55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

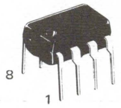
TYPICAL APPLICATION



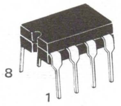
OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT

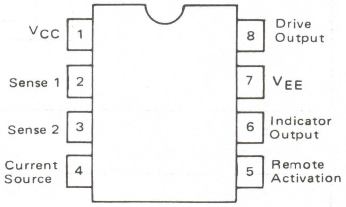
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(MC3423 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3423P1	0 to +70°C	Plastic DIP
MC3423U	0 to +70°C	Ceramic DIP
MC3523U	−55 to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS ($5\ V \leq V_{CC} - V_{EE} \leq 36\ V$, $T_{low} < T_A < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}-V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}-2.2	V_{CC}-1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	V_{OL}(Ind)	–	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	$V_{Sense\ 1}$, $V_{Sense\ 2}$	2.45	2.6	2.75	Vdc
Temperature Coefficient of $V_{Sense\ 1}$ (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current					μA
(V_{IH} = 2.0 V, V_{CC}-V_{EE} = 5.0 V)	I_{IH}	–	5.0	40	
(V_{IL} = 0.8 V, V_{CC}-V_{EE} = 5.0 V)	I_{IL}	–	-120	-180	
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay Time (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current	I_D				mA
MC3423		–	6.0	10	
MC3523		–	5.0	7.0	

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

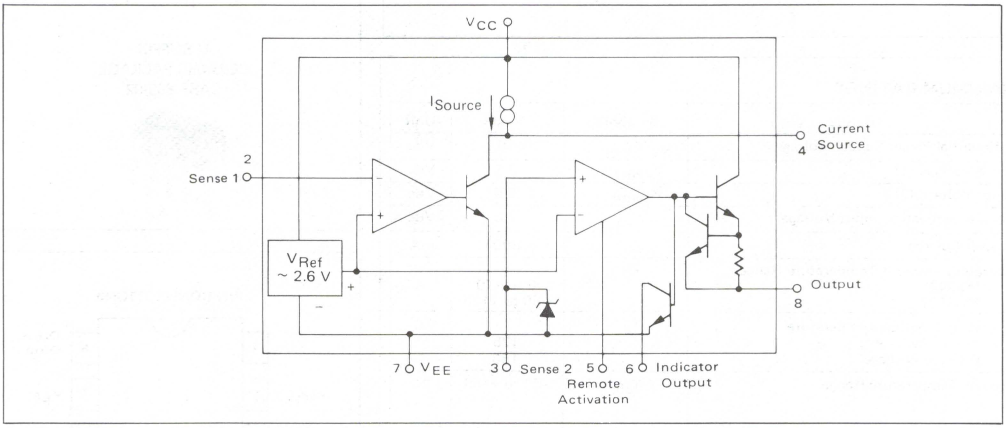
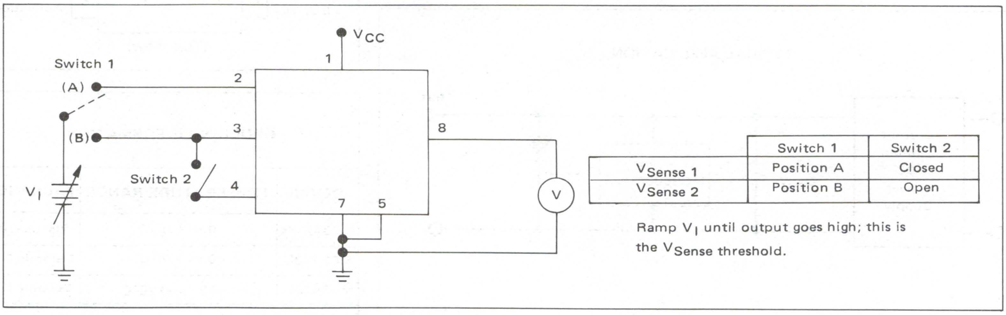

V_{CC}
I_{Source}
Current Source
4
2
Sense 1
V_{Ref}
~ 2.6 V
+
-
+
-
+
-
Output
8
7
V_{EE}
3
Sense 2
5
Remote Activation
6
Indicator Output

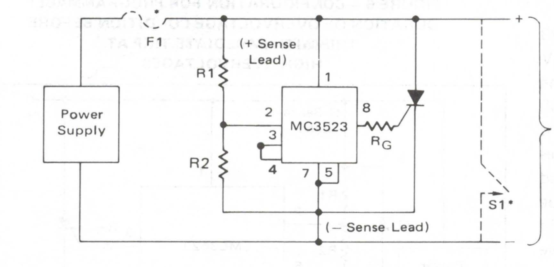
FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT


V_{CC}
1
Switch 1
(A)
(B)
2
3
Switch 2
4
V_I
8
7
5
V

	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

FIGURE 3 — BASIC CIRCUIT CONFIGURATION


F1
(+ Sense Lead)
R1
1
Power Supply
2
MC3523
3
8
R_G
R2
4
7
5
To Load
S1*
(— Sense Lead)
+

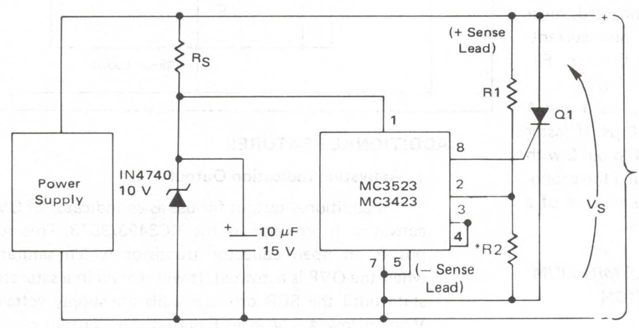
$$V_{trip} = V_{ref}\left(1+\frac{R1}{R2}\right) \approx 2.6\ V\left(1+\frac{R1}{R2}\right)$$

$R2 \leqslant 10\ k\Omega$ for minimum drift

For minimum value of R_G, see Figure 9

*See text for explanation

FIGURE 4 — CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V


R_S
(+ Sense Lead)
+
R1
Q1
1
8
Power Supply
IN4740 10 V
MC3523 MC3423
2
3
10 μF 15 V
4
*R2
V_S
7
5
(— Sense Lead)
To Load

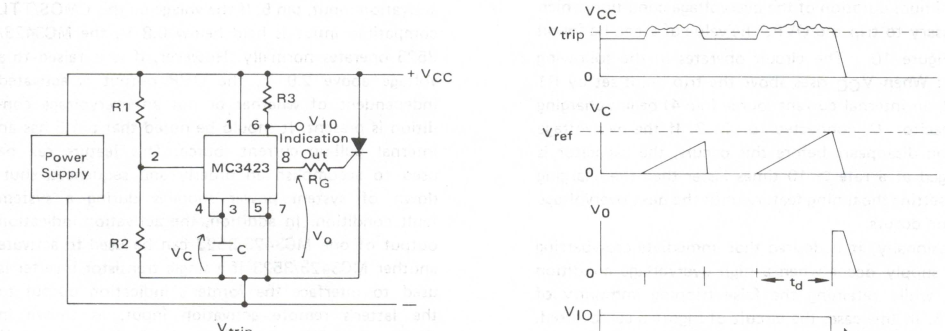
$$R_S = \left(\frac{V_S - 10}{25}\right)\ k\Omega$$

$$V_{trip} = V_{ref}\left(1+\frac{R1}{R2}\right) \approx 2.6\ V\left(1+\frac{R1}{R2}\right)$$

$*R2 \leqslant 10\ k\Omega$

Q1: $V_S \leqslant 50$ V; 2N6504 or equivalent
$V_S \leqslant 100$ V; 2N6505 or equivalent
$V_S \leqslant 200$ V; 2N6506 or equivalent
$V_S \leqslant 400$ V; 2N6507 or equivalent
$V_S \leqslant 600$ V; 2N6508 or equivalent
$V_S \leqslant 800$ V; 2N6509 or equivalent

FIGURE 5 — BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP


+ V_CC
R1
R3
1
6
V_IO Indication Out
Power Supply
2
8
MC3423
R_G
4
3
5
7
V_o
R2
V_C
C
V_CC
V_trip
0
V_C
V_ref
0
V_O
0
t_d
V_IO

$$R3 \geqslant \frac{V_{trip}}{10\ mA}$$

$$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C \text{ (See Figure 10)}$$

APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

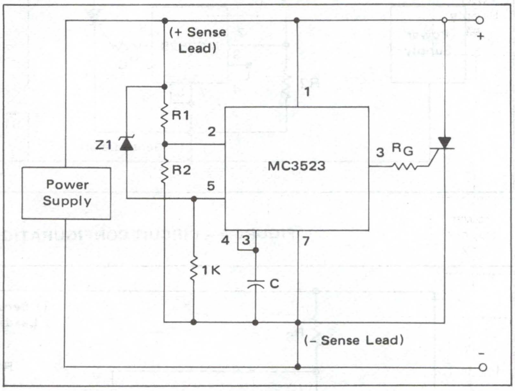
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds $V_{Z1} + 1.4$ V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

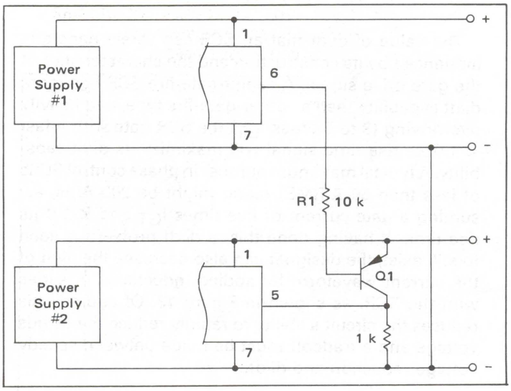
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 5. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

FIGURE 8 – R1 versus TRIP VOLTAGE

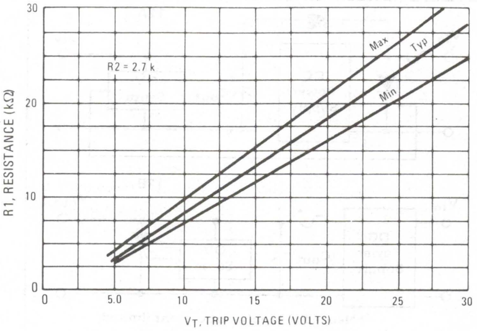


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

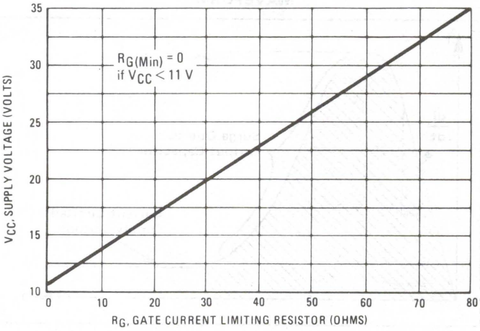


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION

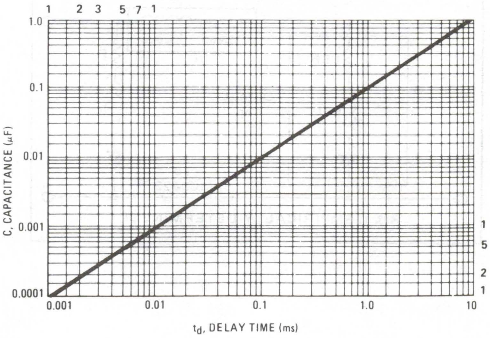
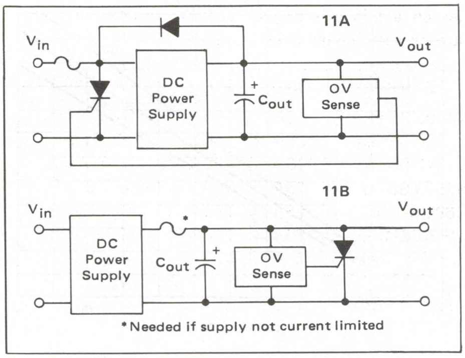


FIGURE 11 — TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

FIGURE 12 — CROWBAR SCR SURGE CURRENT WAVEFORM

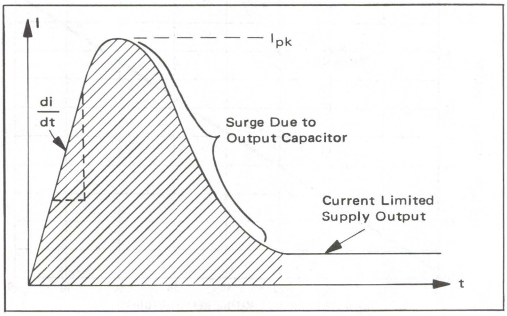
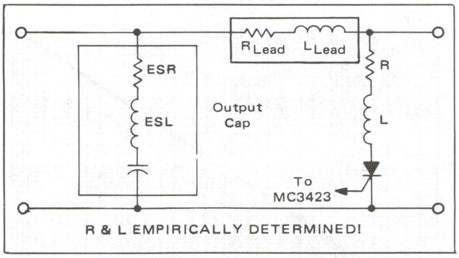


FIGURE 13 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



R & L EMPIRICALLY DETERMINED!

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 μs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and < 1.0 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

MC3424, MC3424A
MC3524, MC3524A
MC3324, MC3324A

MOTOROLA

Advance Information

POWER SUPPLY SUPERVISORY CIRCUIT/DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

POWER SUPPLY SUPERVISORY CIRCUIT/ DUAL-VOLTAGE COMPARATOR

The MC3424 series is a dual-channel supervisory circuit, consisting of two uncommitted input comparators, a reference, output comparators, with high current Drive and Indicator outputs for each channel. The input comparators feature programmable hysteresis, high common-mode rejection, and wide common-mode range, capable of comparing at ground potential with single-supply operation. Separate Delay pins are provided to increase noise immunity by delaying activation of the outputs. A 2.5 V bandgap voltage reference is pinned-out for referencing the input comparators, or other external functions. Independent high current Drive and Indicator outputs for each channel can source and sink up to 300 mA and 30 mA respectively. CMOS/TTL compatible digital inputs provide Remote Activation of each channel's outputs. An Input Enable pin allows control of the input comparators.

Although this device is intended for power supply supervision, the pinned-out reference, uncommitted input comparators, and many other features, enable the MC3424 series to be utilized for a wide range of applications.

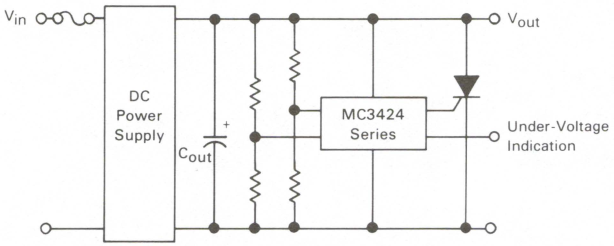
- Pinned-Out 2.5 V Reference
- Wide Common-Mode Range
- Programmable Hysteresis
- Programmable Time Delays
- Two 300 mA Drive Outputs
- Remote Activation Capability
- Wide Supply Range: 4.5 V $\leqslant V_{CC} \leqslant$ 40 V

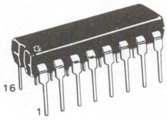
APPLICATIONS

- Dual Over-Voltage "Crowbar" Protection
- Dual Under-Voltage Supervision
- Over/Under Voltage Protection
- Split-Supply Supervision
- Line-Loss Sensing
- Proportional Controller
- Programmable Frequency Switch
- Battery Charger

TYPICAL APPLICATION

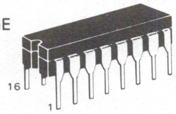
Over-Voltage Crowbar Protection, Under-Voltage Indication



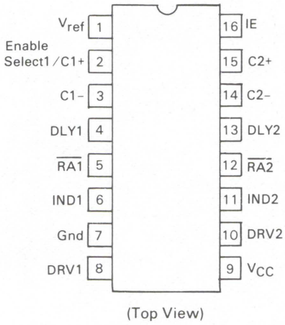


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

L SUFFIX
CERAMIC PACKAGE
CASE 620-02



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3524L, AL	−55 to +125°C	Ceramic DIP
MC3324L, AL	−40 to +85°C	Ceramic DIP
MC3324P, AP		Plastic DIP
MC3424L, AL	0 to +70°C	Ceramic DIP
MC3424P, AP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Differential Voltage Range	V_{IDR}	±40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Input Enable Voltage Range	V_{IE}	−0.3 to +40	Vdc
Remote Activation Input Voltage Range	V_{RA}	−0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Reference Short-Circuit Current	$I_{OS(ref)}$	Internally Limited	mA
Power Dissipation and Thermal Characteristics Ceramic Package Maximum Power Dissipation @ T_A = 95°C Thermal Resistance Junction to Air Plastic Package Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1000 80 1000 80	 mW °C/W mW °C/W
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Operating Ambient Temperature Range MC3524, MC3524A MC3324, MC3324A MC3424, MC3424A	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +175 −55 to +150	°C

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ V_{CC} ≤ 40 V; T_A = T_{low} to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage V_{CC} = 15V; I_L = 0 mA	V_{ref}							Vdc
T_A = 25°C		2.475	2.5	2.525	2.4	2.5	2.6	
T_{low} to T_{high} (Note 1)		2.45	2.5	2.55	2.33	2.5	2.63	
Line Regulation 4.5 V ≤ V_{CC} ≤ 40 V; I_L = 0 mA; T_J = 25°C	Reg_{line}	—	7.0	15	—	7.0	15	mV
Load Regulation 0 mA ≤ I_L ≤ 10 mA; V_{CC} = 15 V; T_J = 25°C	Reg_{load}	—	4.0	12	—	4.0	12	mV
Output Short-Circuit Current (T_A = 25°C)	$I_{OS(ref)}$	—	23	—	—	23	—	mA
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	4.5	—	40	Vdc
Power Supply Current V_{CC} = 40 V; T_A = 25°C; No Output Loads V_{C1-}, V_{C2-} = V_{CC}; V_{C1+}, V_{C2+} = 0 V	$I_{CC(off)}$	—	12	15	—	12	15	mA
V_{C1+}, V_{C2+} = V_{CC}; V_{C1-}, V_{C2-} = 0 V	$I_{CC(on)}$	—	27	32	—	27	32	mA

NOTES:

(1) T_{low} = −55°C for MC3524, MC3524A
= −40°C for MC3324, MC3324A
= 0°C for MC3424, MC3424A

T_{high} = +125°C for MC3524, MC3524A
= +85°C for MC3324, MC3324A
= +70°C for MC3424, MC3424A

(2) The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 300 mV. The upper functional limit of the common-mode voltage range is typically V_{CC} −1.4 volts, but either or both inputs can go to 40 volts, independent of V_{CC}, without device destruction.

(3) The $V_{th(ES1)}$ limits are approximately 0.9 times the V_{ref} limits over the applicable temperature range.

(4) The $V_{th(OC)}$ limits are approximately the V_{ref} limits over the applicable temperature range.

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{CC} ≤ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT SECTION								
Input Offset Voltage $T_A = 25°C$ T_{low} to T_{high} (Note 1)	V_{IO}	 — —	 ±3.0 ±3.0	 ±8.0 ±12	 — —	 ±5.0 ±5.0	 ±10 ±15	mV
Input Offset Current $T_A = 25°C$ T_{low} to T_{high} (Note 1)	I_{IO}	 — —	 ±3.0 ±3.0	 ±25 ±250	 — —	 ±3.0 ±3.0	 ±25 ±250	nA
Input Bias Current $T_A = 25°C$ T_{low} to T_{high} (Note 1)	I_{IB}	 — —	 50 500	 250 1000	 — —	 50 500	 250 1000	nA
Comparator Input Functional Common Mode Range ($T_A = 25°C$, Note 2)	V_{ICR}	-0.1	V_{CC}-1.4	—	-0.1	V_{CC}-1.4	—	V
Hysteresis Activation Voltage $V_{CC} = 15$ V; V_{C1+}, $V_{C2+} = V_{CC}$; $T_A = 25°C$ $I_H = 10\%$ $I_H = 90\%$	$V_{H(act)}$	 — —	 1.2 1.4	 — —	 — —	 1.2 1.4	 — —	V
Hysteresis Current $V_{CC} = 15$ V; V_{C1-}, $V_{C2-} = 2.5$ V; V_{C1+}, $V_{C2+} = V_{CC}$; $T_A = 25°C$	I_H	10	12.5	15	9.0	12.5	16	µA
Common Mode Rejection Ratio	CMRR	60	72	—	60	72	—	dB
Power Supply Rejection Ratio	PSRR	—	95	—	—	95	—	dB
Input Enable Threshold (Pin 16; Note 3)	$V_{th(IE)}$	0.9	1.4	1.9	0.9	1.4	1.9	V
Input Enable Current (Pin 16) $V_{IL(IE)} = 0$ V $V_{IH(IE)} = 40$ V	 $I_{IL(IE)}$ $I_{IH(IE)}$	 — —	 -0.5 0.05	 -2.5 1.0	 — —	 -0.5 0.05	 -2.5 1.0	µA
Enable Select 1 Threshold Voltage (Pin 2)	$V_{th(ES1)}$	2.2	2.25	2.3	2.1	2.25	2.4	V
Delay Pin Voltage ($I_{DLY} = 0$ mA) Low State High State	 $V_{OL(DLY)}$ $V_{OH(DLY)}$	 — V_{CC}-0.5	 0.2 V_{CC}-0.15	 0.5 —	 — V_{CC}-0.5	 0.2 V_{CC}-0.15	 0.5 —	V
Delay Pin Source Current $V_{CC} = 15$ V; V_{DLY1}, $V_{DLY2} = 0$ V	$I_{DLY(source)}$	150	200	250	140	200	260	µA
Delay Pin Sink Current $V_{CC} = 15$ V; V_{DLY1}, $V_{DLY2} = 2.5$ V	$I_{DLY(sink)}$	1.8	3.0	—	1.8	3.0	—	mA
OUTPUT SECTION								
Drive Output Peak Current ($T_A = 25°C$)	$I_{DRV(peak)}$	200	300	—	200	300	—	mA
Drive Output V ($I_{DRV} = 100$ mA; $T_A = 25°C$)	$V_{OH(DRV)}$	V_{CC}-2.5	V_{CC}-2.0	—	V_{CC}-2.5	V_{CC}-2.0	—	V
Drive Output Leakage Current ($V_{DRV} = 0$ V)	$I_{DRV(leak)}$	—	15	200	—	15	200	nA
Drive Output Current Slew Rate ($T_A = 25°C$)	di/dt	—	2.0	—	—	2.0	—	A/µS
Drive Output Transient Rejection ($T_A = 25°C$) $V_{CC} = 0$ V to 15 V at dV/dt = 200 V/µs; V_{C1-}, $V_{C2-} = V_{ref}$; V_{C1+}, $V_{C2+} = 0$ V	$I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage $I_{IND} = 30$ mA; $T_A = 25°C$	$V_{IND(sat)}$	—	560	800	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)} = 40$ V	$I_{IND(leak)}$	—	25	200	—	25	200	nA
Output Comparator Threshold V (Note 4)	$V_{th(OC)}$	2.45	2.5	2.55	2.33	2.5	2.63	V
Remote Activation Threshold Voltage	$V_{th(RA)}$	1.3	1.4	1.5	1.1	1.4	1.7	V
Remote Activation Current $V_{IL(RA)} = 0$ V $V_{IH(RA)} = 40$ V	 $I_{IL(RA)}$ $I_{IH(RA)}$	 — —	 -100 70	 -250 250	 — —	 -100 70	 -250 250	µA
Propagation Delay ($V_{CC} = 15$ V; $T_A = 25°C$) Input to Drive Output 100 mV Overdrive, $C_{DLY} = 0$ µF	$t_{PLH(IN/DRV)}$	—	1.0	—	—	1.0	—	µs
Remote Activation to Drive Output 1.4 V Overdrive (2.5 V to 0 V Step)	$t_{PLH(RA/DRV)}$	—	600	—	—	600	—	ns

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

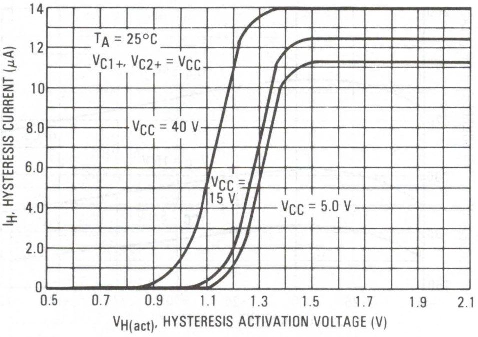


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

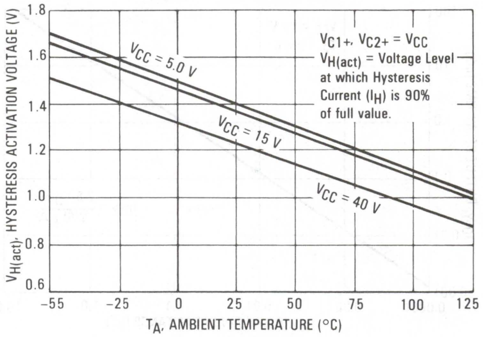


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

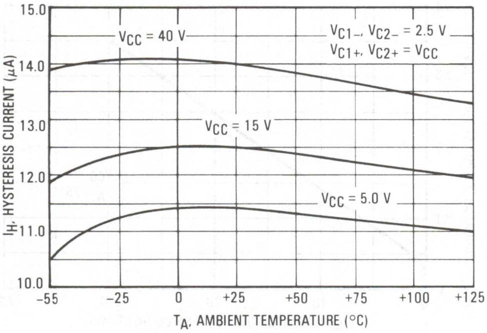


FIGURE 4 — REFERENCE VOLTAGE CHANGE versus OUTPUT CURRENT

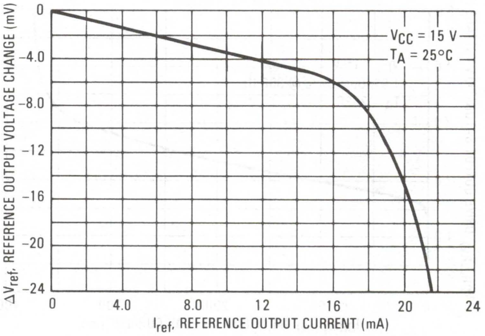


FIGURE 5 — REFERENCE VOLTAGE CHANGE versus TEMPERATURE

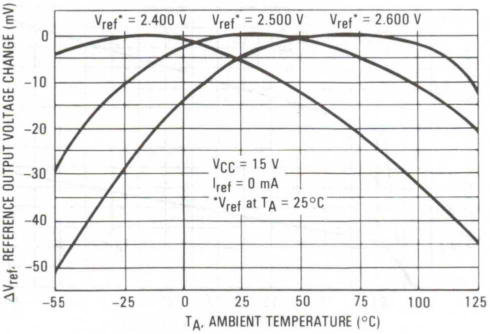


FIGURE 6 — REFERENCE SHORT-CIRCUIT CURRENT versus TEMPERATURE

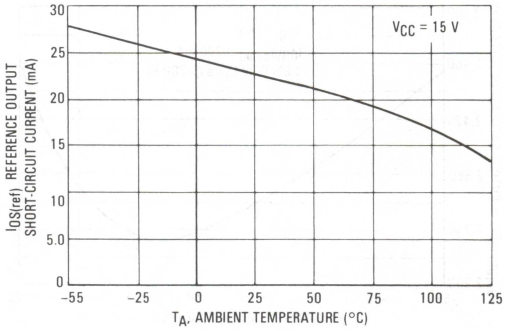


FIGURE 7 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

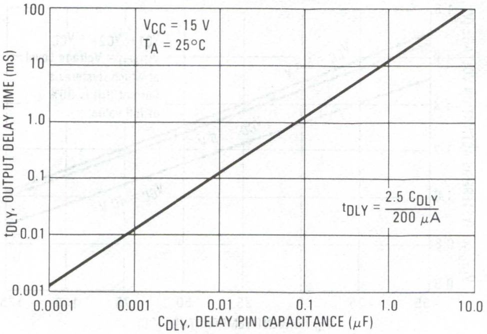


FIGURE 8 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

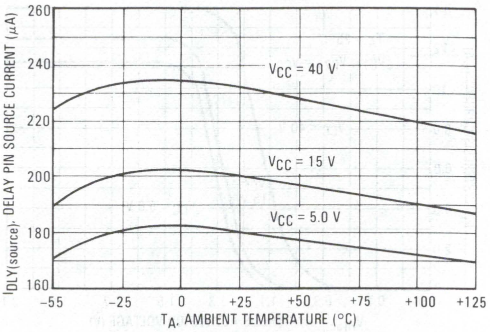


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

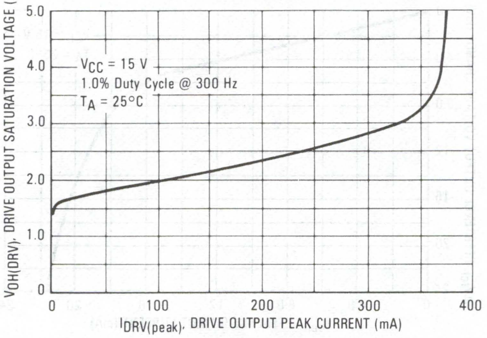


FIGURE 10 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

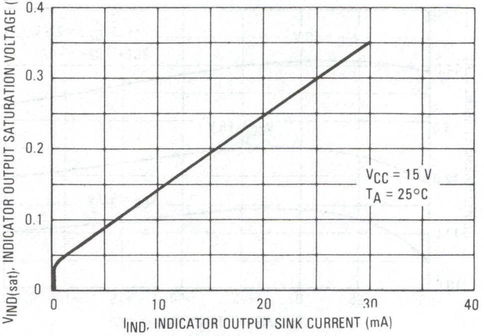


FIGURE 11 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

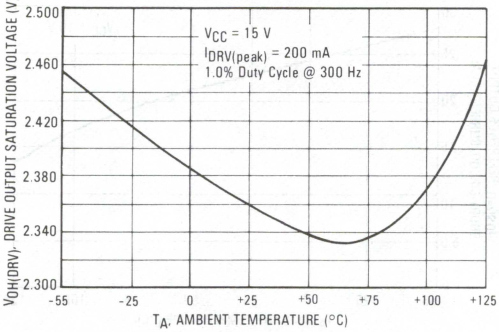


FIGURE 12 — POWER SUPPLY CURRENT versus VOLTAGE

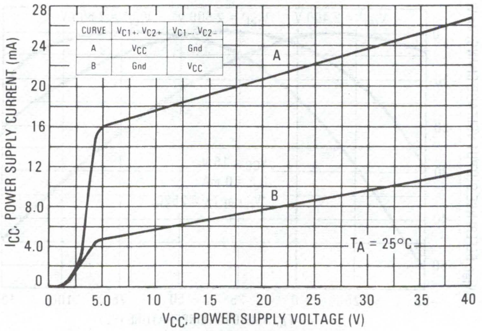
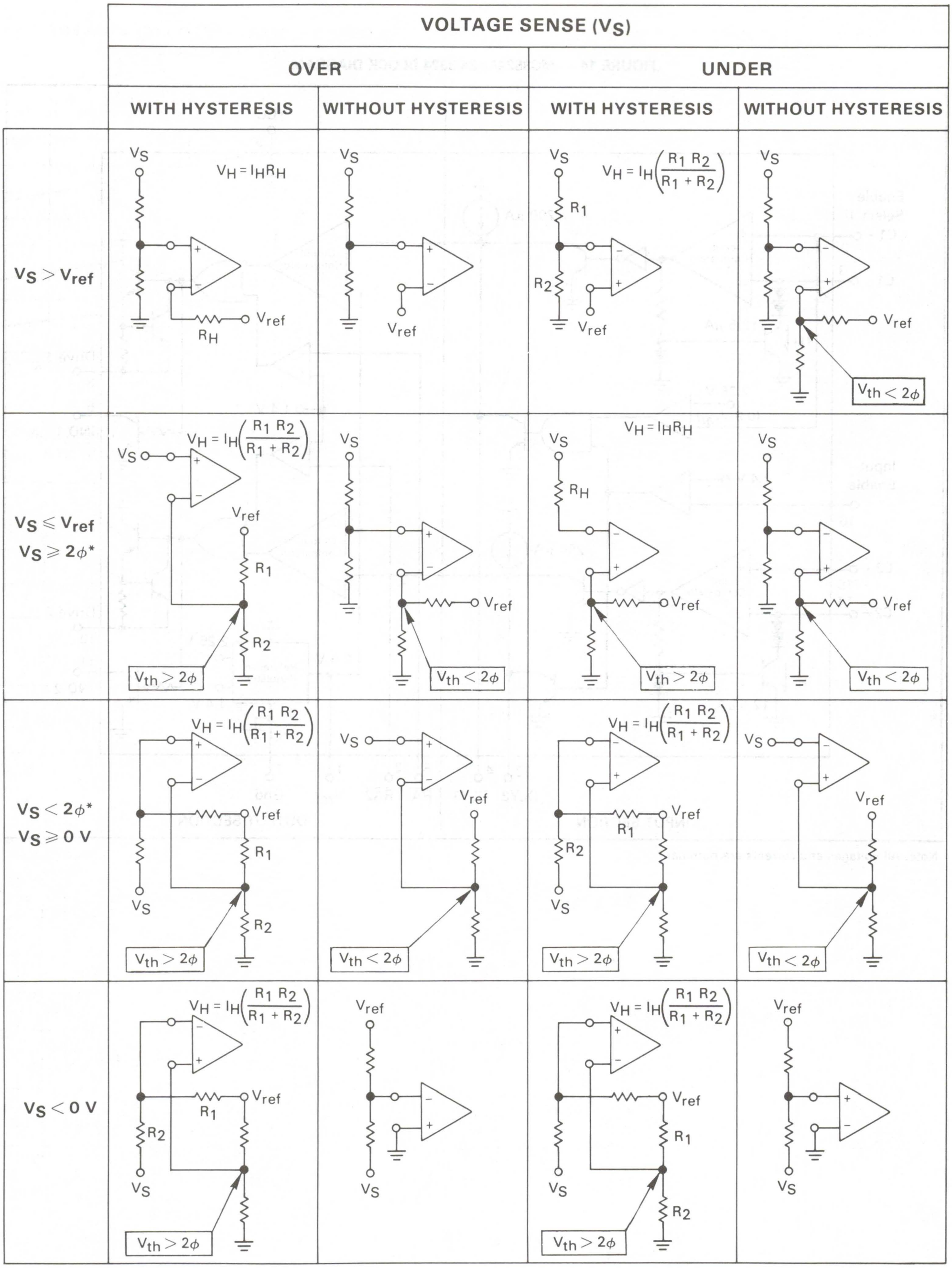
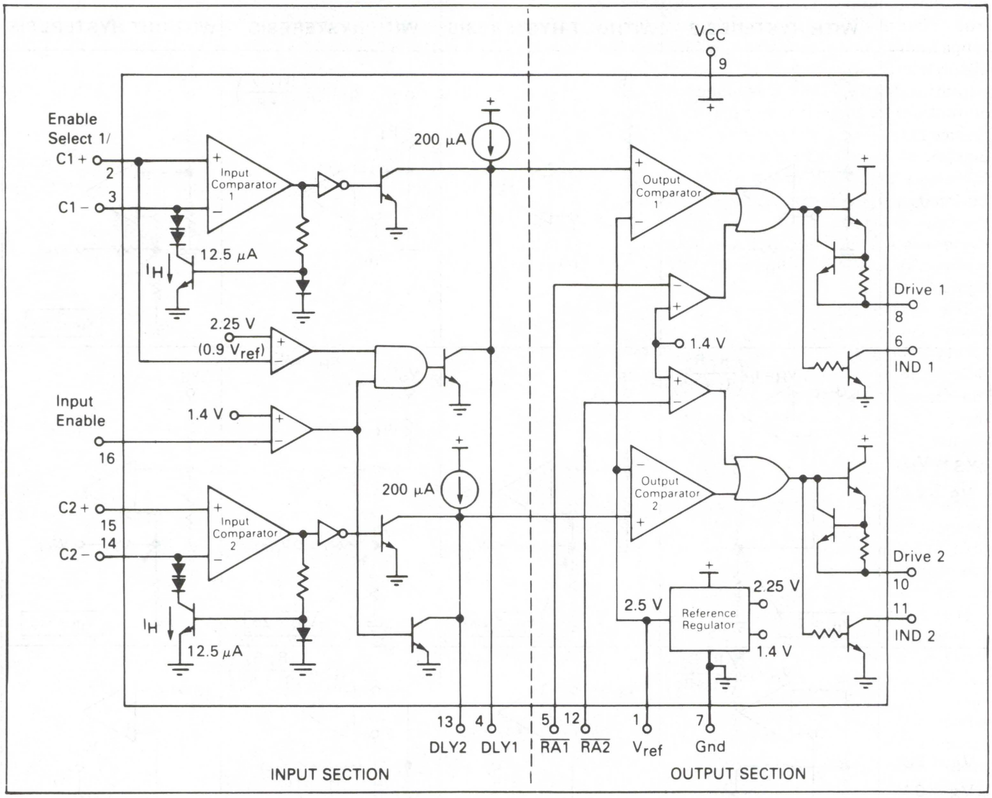


FIGURE 13 — THE COMPLETE VOLTAGE SENSE CAPABILITY OF THE INPUT COMPARATORS, WITH OR WITHOUT PROGRAMMABLE HYSTERESIS.


VOLTAGE SENSE (V_S)
OVER
UNDER
WITH HYSTERESIS
WITHOUT HYSTERESIS
WITH HYSTERESIS
WITHOUT HYSTERESIS
$V_S > V_{ref}$
$V_S \leqslant V_{ref}$
$V_S \geqslant 2\phi$*
$V_S < 2\phi$*
$V_S \geqslant 0$ V
$V_S < 0$ V
V_S
V_{ref}
$V_H = I_H R_H$
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2} \right)$
R_H
R_1
R_2
$V_{th} > 2\phi$
$V_{th} < 2\phi$
+
−

*$2\phi \simeq 1.1$ Volts at $T_J = 25°C$

FIGURE 14 — MC3524/3424/3324 BLOCK DIAGRAM


VCC
9
Enable
Select 1/
C1 +
2
3
C1 −
Input Comparator 1
200 μA
Output Comparator 1
12.5 μA
IH
Drive 1
8
6
IND 1
2.25 V
(0.9 Vref)
1.4 V
Input
Enable
16
1.4 V
200 μA
Output Comparator 2
C2 +
15
14
C2 −
Input Comparator 2
Drive 2
10
11
IND 2
2.25 V
2.5 V
Reference Regulator
1.4 V
IH
12.5 μA
13
DLY2
4
DLY1
5
RA1
12
RA2
1
Vref
7
Gnd
INPUT SECTION
OUTPUT SECTION

Note: All voltages and currents are nominal.

CIRCUIT DESCRIPTION

The MC3424 series is a high current output, dual channel power supply supervisory circuit. Basic circuit configuration is shown in Figure 14. Each channel features a true differential input comparator with a common-mode range from ground potential to V_{CC} - 1.4 volts, with single supply operation. The inverting inputs of each input comparator (C1–, C2–) have a feedback activated 12.5 μA current sink for programming input comparator hysteresis. Source resistance of the inverting inputs determines the amount of hysteresis for each input comparator. The hysteresis feature can be defeated by reducing the inverting input voltage of the respective input comparator to less than two diode drops ($2\ \phi \simeq 1.1$ volts) above Gnd (See Hysteresis Activation Voltage specification). A complete matrix of various input comparator conditions is shown in Figure 13.

The digital Input Enable (IE) pin provides full enable/disable control of one or both of the input comparators. Input Comparator 1 enable control is allowed if the Enable Select1/Non-Inverting Input (pin 2) is less than 90% of the internal 2.5 volts reference ($0.9\ V_{ref} \cong 2.25$ V). If the Input Enable Select1/Non-Inverting Input (pin 2) is greater than 0.9 V_{ref}, Comparator 1 is not affected by the logic state of the Input Enable pin and always remains enabled.

The voltage threshold of the Input Enable pin is TTL-compatible. A logic level "1" permits normal operation of input comparators, as stated above. A logic "0" forces the respective Delay pin (DLY1, DLY2) to a low state, independent of the input comparator's state.

The selective enabling feature of Input Comparator 1 is directly applicable when the MC3424 series is used as an over- and under-voltage supervisory circuit, where channel 2 (Input Comparator 2) is monitoring under-voltage conditions, and channel 1 is utilized for over-voltage protection. The ability to keep channel 1 (Input Comparator 1) active, while disabling channel 2, provides immediate over-voltage protection during power supply turn-on, while the under-voltage channel (2) can be disabled during the power supply turn-on rise time to the regulated level, preventing false indication of an under-voltage condition. If it is desired to monitor two independent voltages for an under-voltage condition, both channels can be selectively disabled until the slowest supply reaches its regulated voltage.

Separate Delay pins (DLY1, DLY2) are provided for each channel to independently delay the Drive and Indicator Outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source of typically 200 μA when the non-inverting input voltage is greater than the inverting input level ($V_{C1+} > V_{C1-}$; $V_{C2+} > V_{C2-}$).

A capacitor (C_{DLY}) tied to these Delay pins will establish a predictable delay time (t_{DLY}) of the Drive and Indicator outputs for the respective channel. The Delay pins are internally tied to the non-inverting input of Output Comparators 1 and 2, which are referenced to 2.5 volts. Therefore, delay time (t_{DLY}) is based on the constant current $I_{DLY(source)}$ charging the external delay capacitor (C_{DLY}) to 2.5 volts or:

$$t_{DLY} = \frac{V_{ref}\ C_{DLY}}{I_{DLY(source)}} = \frac{2.5\ C_{DLY}}{200\ \mu A} = 12500\ C_{DLY}.$$

Figure 7 provides C_{DLY} values for a wide range of time delays.

The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input ($V_{C1+} < V_{C1-}$; $V_{C2+} < V_{C2-}$), or when the Input Enable pin is at a low logic level. The sink current ($\geqslant$ 1.8 mA) capability of the Delay pins is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

Each independent channel of the MC3424 series has a Drive (DRV) and Indicator output (IND) which respectively source and sink current simultaneously. The Drive outputs are current-limited emitter-followers capable of sourcing 300 mA at a turn-on slew rate of 2.0A/μS, ideal for driving "Crowbar" SCR's. The Indicator outputs are open collector, NPN transistors, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or regular shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

Separate TTL-compatible Remote Activation inputs ($\overline{RA1}$, $\overline{RA2}$) for each channel will activate the Drive and Indicator outputs of the respective channel, independent of the input comparator state, when a low logic level is applied. The active low for remote activation permits latching of the respective outputs by connecting the Indicator output, via a $\leqslant$ 5.0 K resistor to the Remote Activation input of the same channel, as shown in Figure 18. Latching will now occur by either of the Remote Activation inputs with a short duration low logic level, or by the input comparators. Unlatching of each channel is accomplished with a short duration, high logic level at the Remote Activation pin.

The MC3424 series has an internal 2.5 V bandgap reference capable of sourcing up to 10 mA of load current for external bias circuits. This reference has an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

CROWBAR SCR CONSIDERATIONS

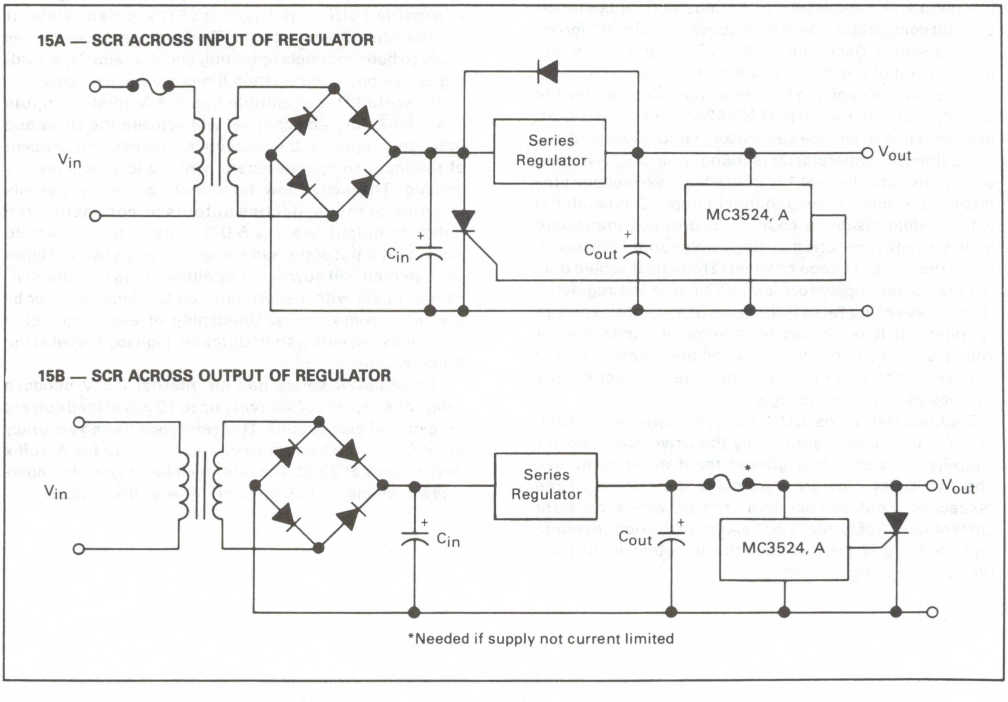
Referring to Figure 15, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 15A, the supply's input filter capacitors. This surge current is illustrated in Figure 16, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

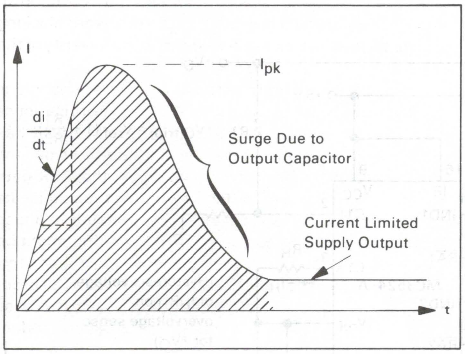
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 17. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 15 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

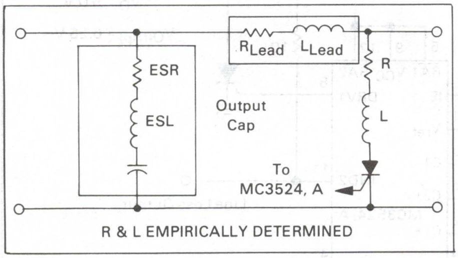
FIGURE 16 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 17) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 17 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 15A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 15B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

APPLICATIONS INFORMATION

FIGURE 18 — OVERVOLTAGE PROTECTION OF SPLIT SUPPLIES WITH DELAY AND LATCHED-FAULT INDICATION.

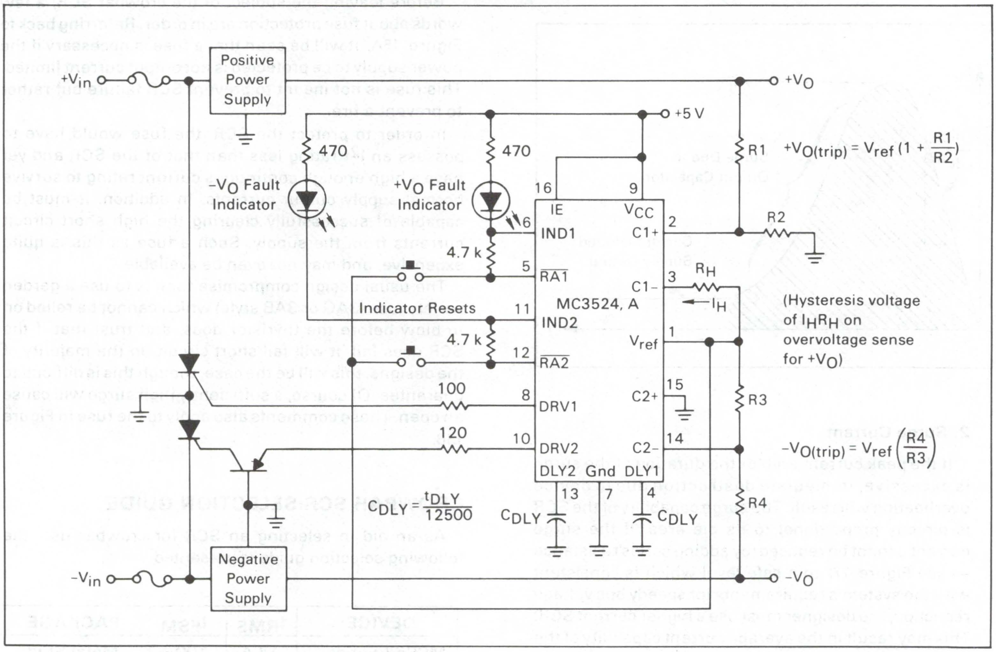

+Vin
Positive Power Supply
+VO
+5 V
470
470
−VO Fault Indicator
+VO Fault Indicator
4.7 k
4.7 k
Indicator Resets
100
120
16
9
IE
VCC
6
IND1
2
C1+
5
RA1
3
C1−
11
MC3524, A
IND2
1
Vref
12
RA2
8
DRV1
15
C2+
10
DRV2
14
C2−
DLY2
Gnd
DLY1
13
7
4
CDLY
CDLY
$C_{DLY} = \frac{t_{DLY}}{12500}$
R1
R2
$+V_{O(trip)} = V_{ref}\left(1 + \frac{R1}{R2}\right)$
RH
IH
(Hysteresis voltage of IHRH on overvoltage sense for +VO)
R3
R4
$-V_{O(trip)} = V_{ref}\left(\frac{R4}{R3}\right)$
Negative Power Supply
−Vin
−VO

FIGURE 19 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

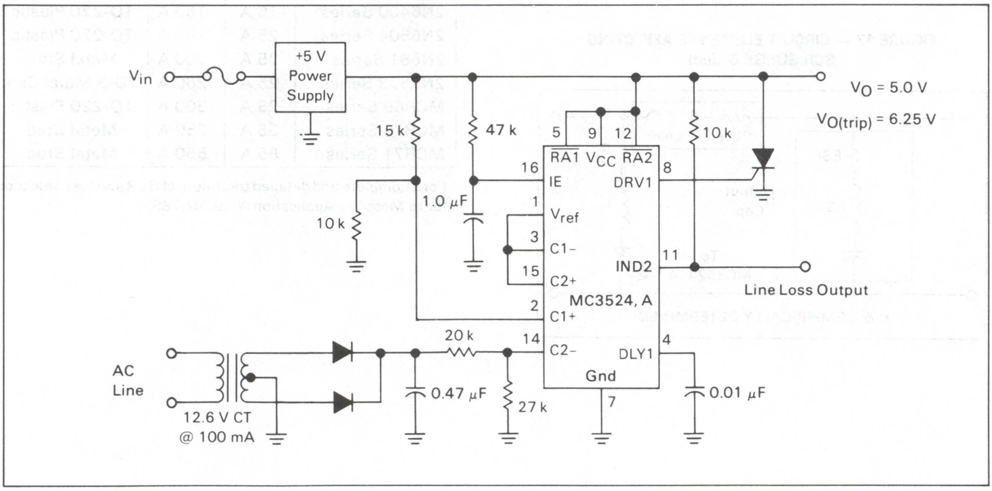

Vin
+5 V Power Supply
VO = 5.0 V
VO(trip) = 6.25 V
15 k
47 k
10 k
1.0 µF
10 k
5
9
12
RA1
VCC
RA2
16
IE
DRV1
8
1
Vref
3
C1−
15
C2+
IND2
11
2
C1+
MC3524, A
Line Loss Output
14
C2−
DLY1
4
Gnd
7
20 k
0.47 µF
27 k
0.01 µF
AC Line
12.6 V CT @ 100 mA

FIGURE 20 — LATCHING OVERVOLTAGE SENSING CIRCUIT WITH INTERMITTENT AUDIO ALARM

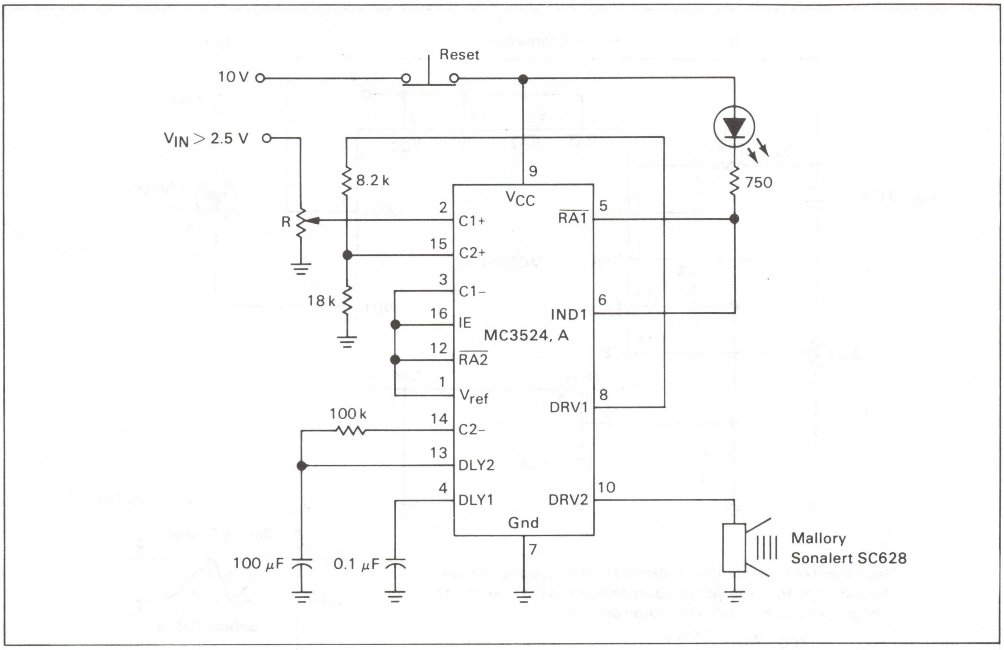
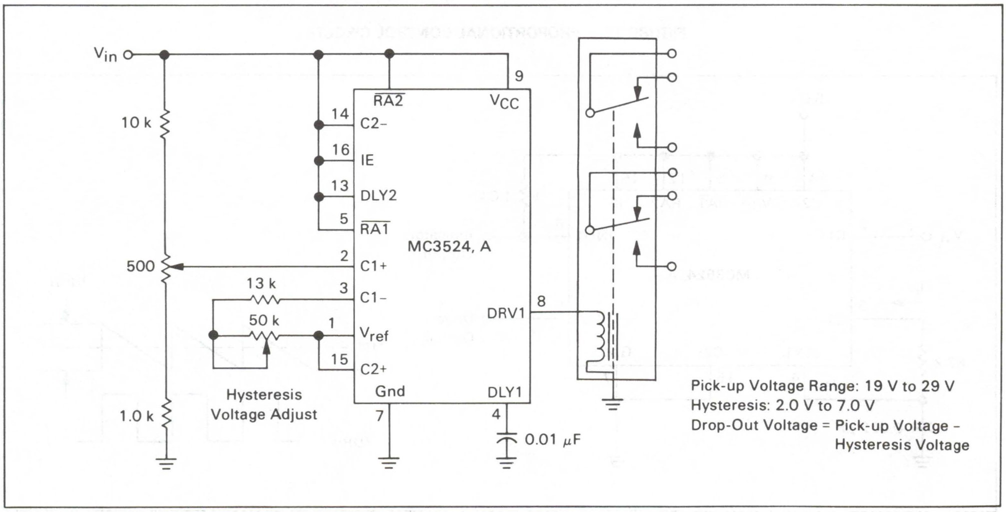
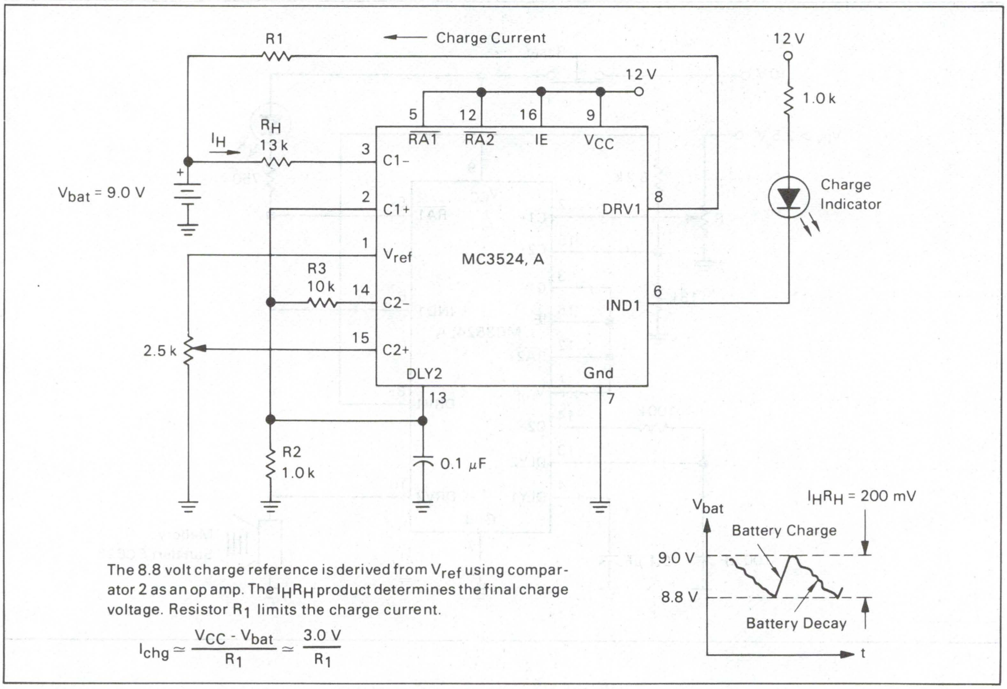

Reset
10 V
$V_{IN} > 2.5$ V
8.2 k
R
18 k
750
9
V_{CC}
2
C1+
15
C2+
3
C1−
16
IE
12
$\overline{RA2}$
1
V_{ref}
14
C2−
13
DLY2
4
DLY1
5
$\overline{RA1}$
6
IND1
MC3524, A
8
DRV1
10
DRV2
Gnd
7
100 k
100 µF
0.1 µF
Mallory
Sonalert SC628

FIGURE 21 — ADJUSTABLE D.C. PICK-UP/DROP-OUT RELAY CIRCUIT


V_{in}
10 k
500
1.0 k
9
$\overline{RA2}$
V_{CC}
14
C2−
16
IE
13
DLY2
5
$\overline{RA1}$
MC3524, A
2
C1+
13 k
3
C1−
50 k
1
V_{ref}
15
C2+
8
DRV1
Gnd
DLY1
7
4
0.01 µF
Hysteresis
Voltage Adjust

Pick-up Voltage Range: 19 V to 29 V
Hysteresis: 2.0 V to 7.0 V
Drop-Out Voltage = Pick-up Voltage − Hysteresis Voltage

FIGURE 22 — 9.0 V BATTERY CHARGER with ZERO SENSE LOAD CURRENT


R1
Charge Current
12 V
12 V
1.0 k
5
12
16
9
RA1
RA2
IE
VCC
IH
RH
13 k
3
C1−
Vbat = 9.0 V
2
C1+
DRV1
8
Charge
Indicator
1
Vref
MC3524, A
R3
10 k
14
C2−
IND1
6
2.5 k
15
C2+
DLY2
Gnd
13
7
R2
1.0 k
0.1 μF
Vbat
IHRH = 200 mV
Battery Charge
9.0 V
8.8 V
Battery Decay
t

The 8.8 volt charge reference is derived from V_{ref} using comparator 2 as an op amp. The $I_H R_H$ product determines the final charge voltage. Resistor R_1 limits the charge current.

$$I_{chg} \simeq \frac{V_{CC} - V_{bat}}{R_1} \simeq \frac{3.0\ V}{R_1}$$

FIGURE 23 — PROPORTIONAL CONTROL CIRCUIT

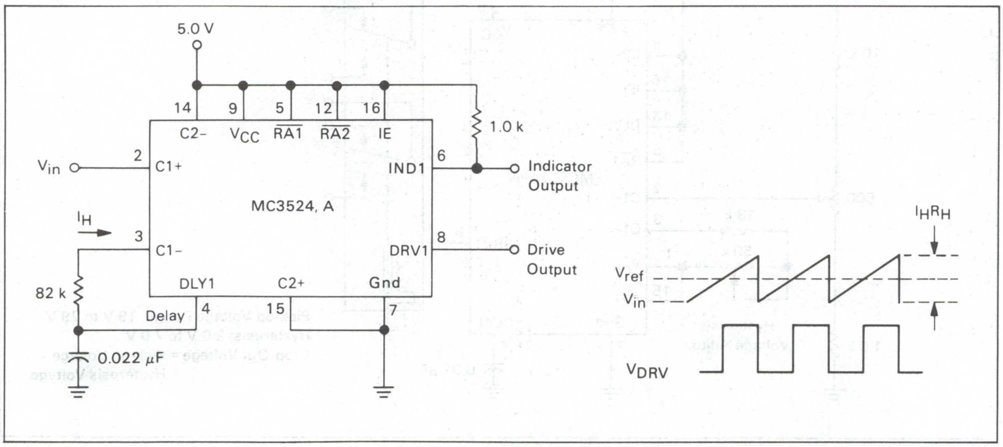

5.0 V
14
9
5
12
16
C2−
VCC
RA1
RA2
IE
1.0 k
Vin
2
C1+
IND1
6
Indicator
Output
MC3524, A
IH
3
C1−
DRV1
8
Drive
Output
82 k
DLY1
C2+
Gnd
Delay
4
15
7
0.022 μF
IHRH
Vref
Vin
VDRV

FIGURE 24 — ALTERNATING TWO TONE GENERATOR (EUROPEAN SIREN)

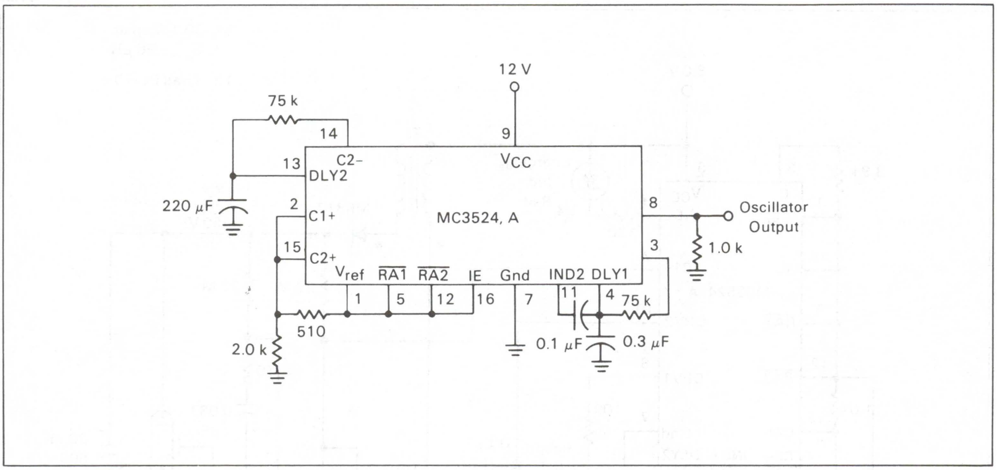

12 V
75 k
14
9
13
C2–
DLY2
VCC
220 μF
2
C1+
MC3524, A
8
Oscillator
Output
15
C2+
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
75 k
510
2.0 k
0.1 μF
0.3 μF

FIGURE 25 — TONE BURST GENERATOR

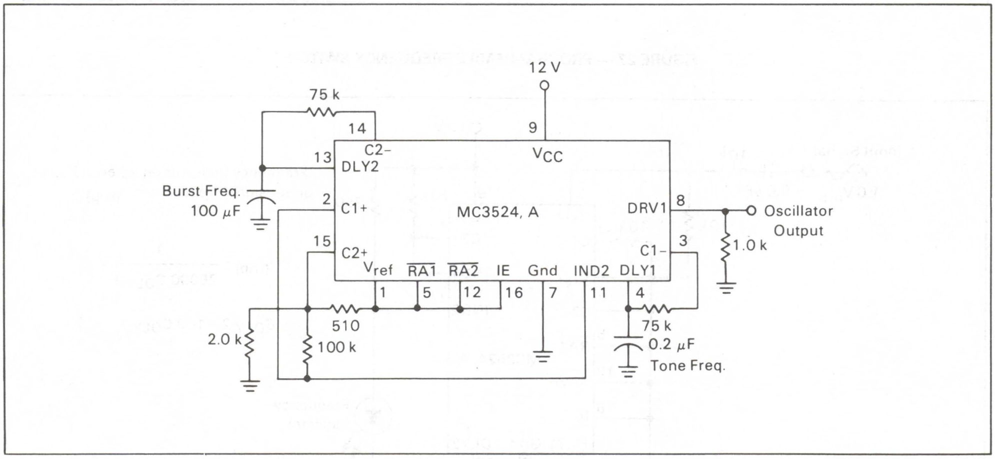

12 V
75 k
14
9
13
C2–
DLY2
VCC
Burst Freq.
100 μF
2
C1+
MC3524, A
DRV1
8
Oscillator
Output
15
C2+
C1–
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
510
75 k
2.0 k
100 k
0.2 μF
Tone Freq.

FIGURE 26 — PHOTOFLASH CONVERTER

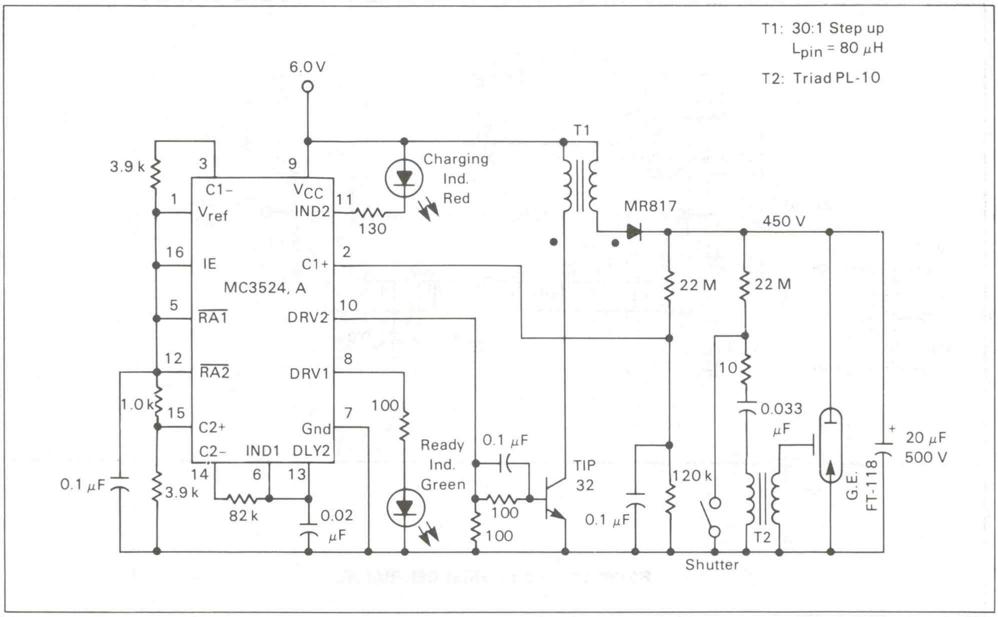
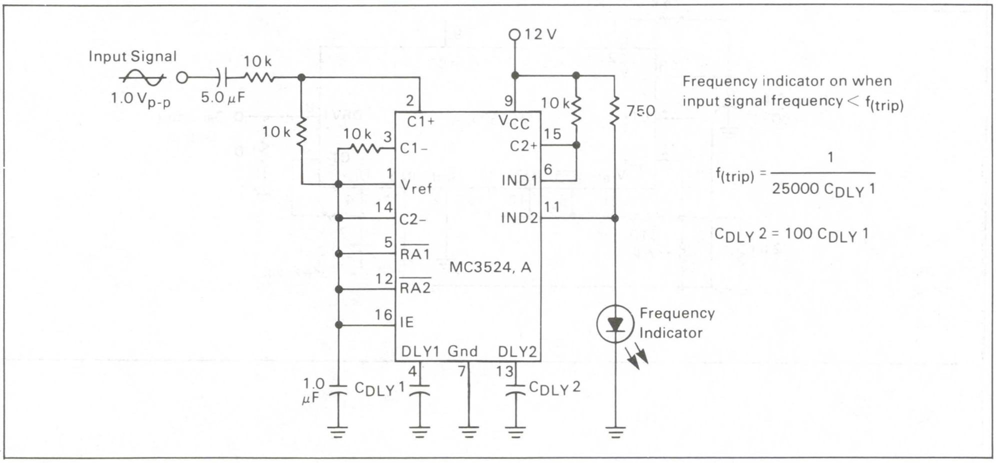

T1: 30:1 Step up
L_{pin} = 80 μH
T2: Triad PL-10
6.0 V
T1
3.9 k
3
9
C1−
V_{CC}
1
V_{ref}
IND2
11
130
Charging
Ind.
Red
MR817
450 V
16
IE
C1+
2
MC3524, A
5
$\overline{RA1}$
DRV2
10
22 M
22 M
12
$\overline{RA2}$
DRV1
8
10
1.0 k
15
C2+
7
Gnd
100
0.033
μF
C2−
IND1
DLY2
Ready
Ind.
Green
0.1 μF
TIP
32
20 μF
500 V
G.E.
FT-118
0.1 μF
14
6
13
120 k
3.9 k
82 k
0.02
μF
100
100
0.1 μF
T2
Shutter

FIGURE 27 — PROGRAMMABLE FREQUENCY SWITCH

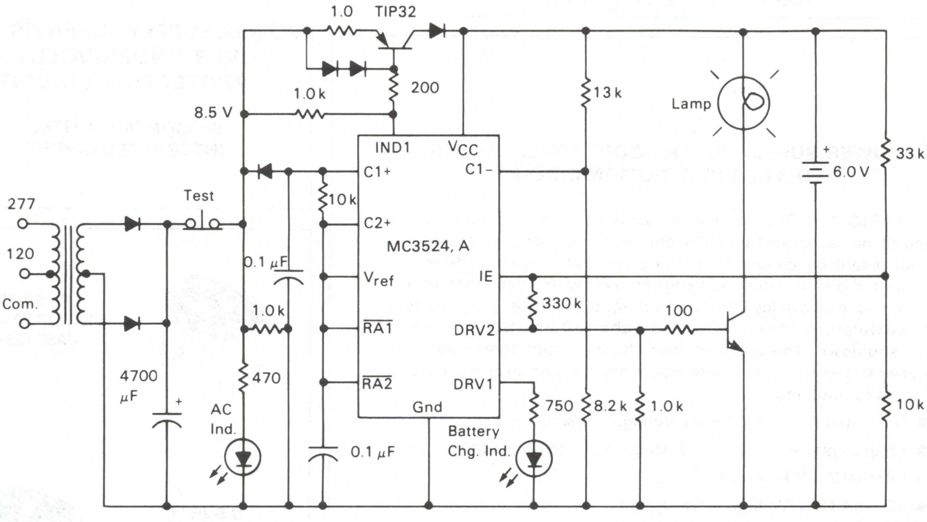

12 V
Input Signal
10 k
1.0 V_{p-p}
5.0 μF
2
9
10 k
750
C1+
V_{CC}
10 k
10 k
3
C1−
15
C2+
1
V_{ref}
6
IND1
14
C2−
11
IND2
5
$\overline{RA1}$
12
$\overline{RA2}$
MC3524, A
16
IE
Frequency
Indicator
DLY1
Gnd
DLY2
4
7
13
1.0
μF
C_{DLY} 1
C_{DLY} 2

Frequency indicator on when input signal frequency $< f_{(trip)}$

$$f_{(trip)} = \frac{1}{25000\, C_{DLY}1}$$

$$C_{DLY}2 = 100\, C_{DLY}1$$

FIGURE 28 — EMERGENCY LIGHTING SYSTEM

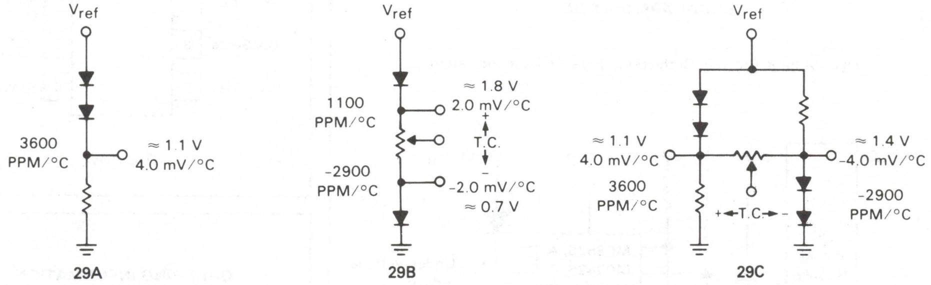

1.0
TIP32
1.0 k
200
8.5 V
13 k
Lamp
33 k
6.0 V
IND1
VCC
C1+
C1–
10 k
C2+
MC3524, A
Vref
IE
RA1
DRV2
RA2
DRV1
Gnd
277
120
Com.
Test
0.1 µF
1.0 k
330 k
100
470
4700 µF
AC Ind.
0.1 µF
Battery Chg. Ind.
750
8.2 k
1.0 k
10 k

All diodes are 1N4001.

1. Battery charge current ≈ 0.6 A. Charger will cycle OFF at 6.6 V, ON at 6.4 V.

2. Lamp is ON with loss of ac and battery voltage ⩾ 5.7 V. As battery discharges to < 5.3 V, lamp will turn OFF.

FIGURE 29 — REFERENCE TEMPERATURE COEFFICIENT MODIFICATIONS


Vref
3600 PPM/°C
≈ 1.1 V
4.0 mV/°C
29A
Vref
1100 PPM/°C
≈ 1.8 V
2.0 mV/°C
+
T.C.
–
-2900 PPM/°C
-2.0 mV/°C
≈ 0.7 V
29B
Vref
≈ 1.1 V
4.0 mV/°C
3600 PPM/°C
+ T.C. –
≈ 1.4 V
-4.0 mV/°C
-2900 PPM/°C
29C

All diodes are 1N4001.

29A. Fixed positive T.C.
29B. Variable positive or negative T.C.
29C. Variable positive or negative T.C. with almost constant voltage.

MC3425 MC3425A
MC3525 MC3525A

MOTOROLA

Advance Information

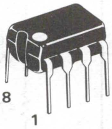
POWER SUPPLY SUPERVISORY/ OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

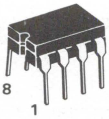
The MC3425/3525 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

- Dedicated Over- And Under-Voltage Sensing
- Programmable Hysteresis Of Under-Voltage Comparator
- Internal 2.5 V Reference
- 300 mA Over-Voltage Drive Output
- 30 mA Under-Voltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

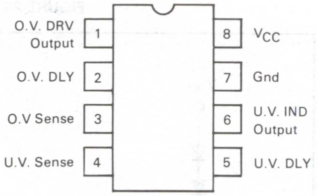


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



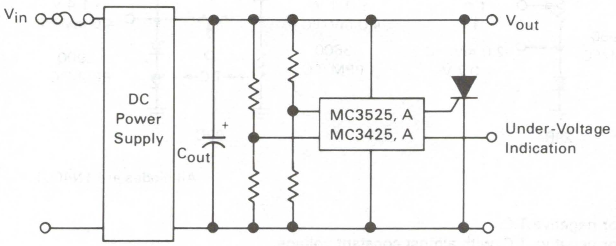
PIN CONNECTIONS



(Top View)

TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



ORDERING INFORMATION

Device	Temperature Range	Package
MC3525U, AU	-55 to +125°C	Ceramic DIP
MC3425P1, AP1	0 to +70°C	Plastic DIP
MC3425U, AU		Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 2)	V_{IR}	−0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics			
Ceramic Package			
Maximum Power Dissipation @ $T_A = 95°C$	P_D	1000	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	80	°C/W
Plastic Package			
Maximum Power Dissipation @ $T_A = 70°C$	P_D	1000	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	80	°C/W
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	
Operating Ambient Temperature Range	T_A		°C
MC3425, MC3425A		0 to +70	
MC3525, MC3525A		−55 to +125	
Storage Temperature Range	T_{stg}		°C
Ceramic Package		−65 to +175	
Plastic Package		−55 to +150	

ELECTRICAL CHARACTERISTICS ($4.5\ V \leqslant V_{CC} \leqslant 40\ V$; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3525A/3425A			MC3525/3425			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Sense Trip Voltage (Reference Voltage)	V_{Sense}							Vdc
$V_{CC} = 15\ V$								
$T_A = 25°C$		2.475	2.5	2.525	2.4	2.5	2.6	
T_{low} to T_{high} (Note 1)		2.45	2.5	2.55	2.33	2.5	2.63	
Line Regulation of V_{Sense} $4.5\ V \leqslant V_{CC} \leqslant 40\ V$; $T_J = 25°C$	Reg_{line}	—	7.0	15	—	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	4.5	—	40	Vdc
Power Supply Current $V_{CC} = 40\ V$; $T_A = 25°C$; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	—	8.5	10	—	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	—	16.5	19	—	16.5	19	mA

NOTES:

(1) T_{low} = −55°C for MC3525, MC3525A
= 0°C for MC3425, MC3425A

T_{high} = +125°C for MC3525, MC3525A
= +70°C for MC3425, MC3425A

(2) The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

(3) The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

ELECTRICAL CHARACTERISTICS (4.5 V $\leq V_{CC} \leq$ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3525A/3425A			MC3525/3425			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT SECTION								
Input Bias Current, O.V. and U.V. Sense	I_{IB}	—	1.0	2.0	—	1.0	2.0	μA
Hysteresis Activation Voltage, U.V. Sense V_{CC} = 15 V; T_A = 25°C;	$V_{H(act)}$							V
I_H = 10%		—	0.6	—	—	0.6	—	
I_H = 90%		—	0.8	—	—	0.8	—	
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	10	12.5	15	9.0	12.5	16	μA
Delay Pin Voltage (I_{DLY} = 0 mA)								V
Low State	$V_{OL(DLY)}$	—	0.2	0.5	—	0.2	0.5	
High State	$V_{OH(DLY)}$	V_{CC}-0.5	V_{CC}-0.15	—	V_{CC}-0.5	V_{CC}-0.15	—	
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} = 0 V	$I_{DLY(source)}$	150	200	250	140	200	260	μA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} = 2.5 V	$I_{DLY(sink)}$	1.8	3.0	—	1.8	3.0	—	mA
OUTPUT SECTION								
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	200	300	—	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25°C	$V_{OH(DRV)}$	V_{CC}-2.5	V_{CC}-2.0	—	V_{CC}-2.5	V_{CC}-2.0	—	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	—	15	200	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	—	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.45	2.5	2.55	2.33	2.5	2.63	V
Propagation Delay Time (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 μF	$t_{PLH(IN/OUT)}$	—	1.7	—	—	1.7	—	μs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN/DLY)}$	—	700	—	—	700	—	ns

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

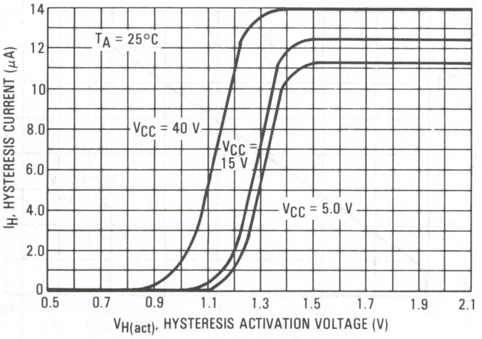


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

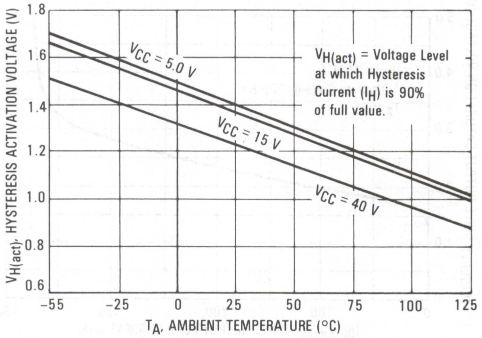


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

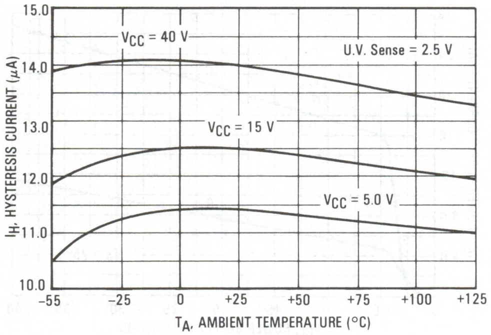


FIGURE 4 — SENSE TRIP VOLTAGE CHANGE versus TEMPERATURE

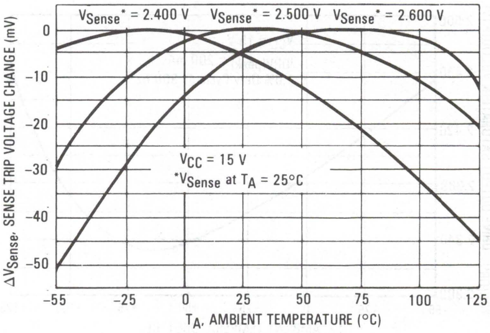


FIGURE 5 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

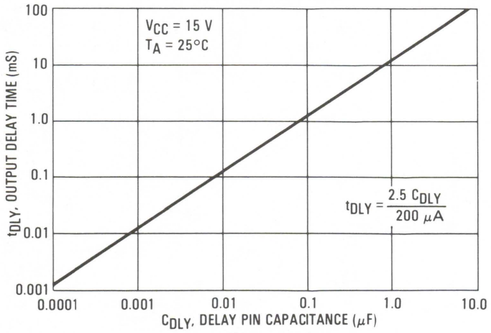


FIGURE 6 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

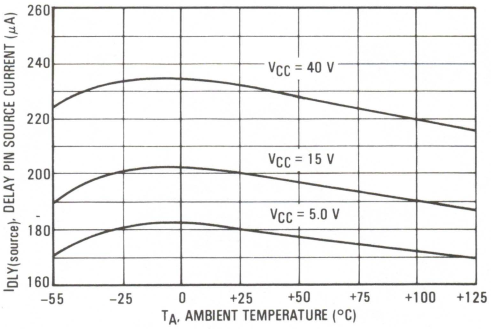


FIGURE 7 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

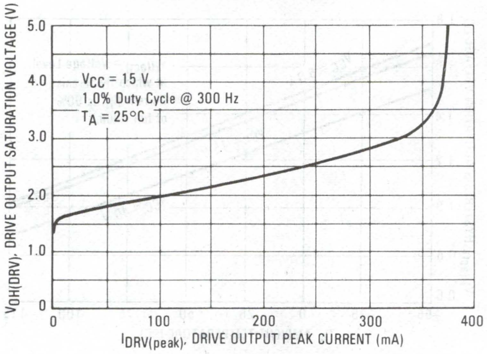


FIGURE 8 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

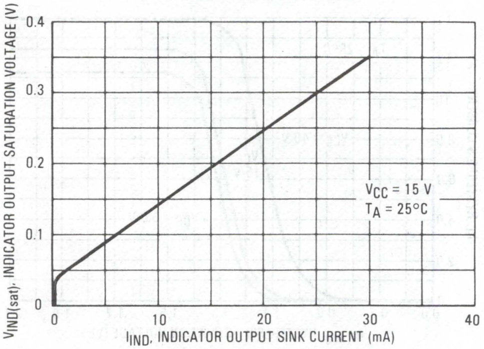


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

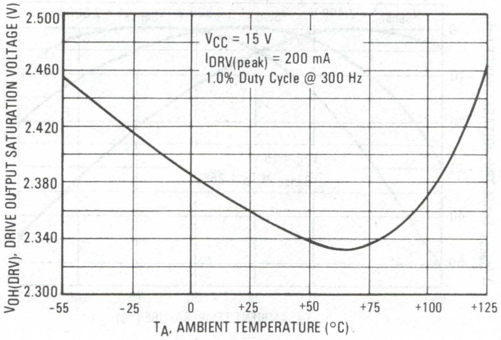
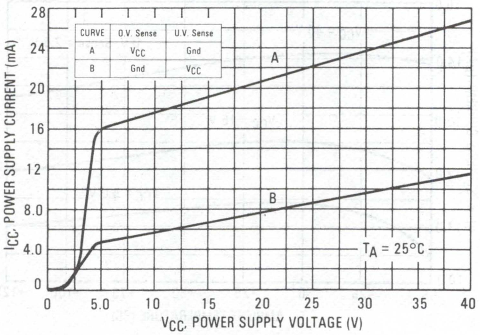


FIGURE 10 — POWER SUPPLY CURRENT versus VOLTAGE



APPLICATIONS INFORMATION

FIGURE 11 — OVERVOLTAGE PROTECTION AND UNDER VOLTAGE FAULT INDICATION WITH PROGRAMMABLE DELAY

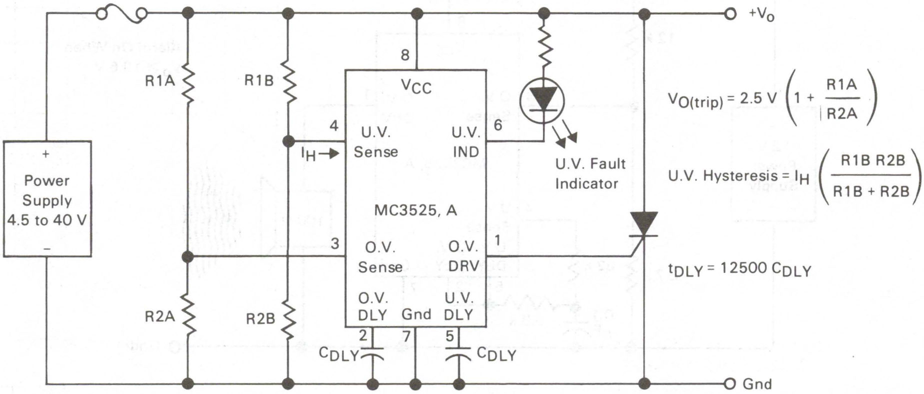

+Vo
Gnd
R1A
R1B
R2A
R2B
+
Power
Supply
4.5 to 40 V
–
8
VCC
4
U.V.
Sense
IH
6
U.V.
IND
MC3525, A
3
O.V.
Sense
1
O.V.
DRV
O.V.
DLY
Gnd
U.V.
DLY
2
7
5
CDLY
CDLY
U.V. Fault
Indicator
VO(trip) = 2.5 V (1 + R1A/R2A)
U.V. Hysteresis = IH (R1B R2B / R1B + R2B)
tDLY = 12500 CDLY

FIGURE 12 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

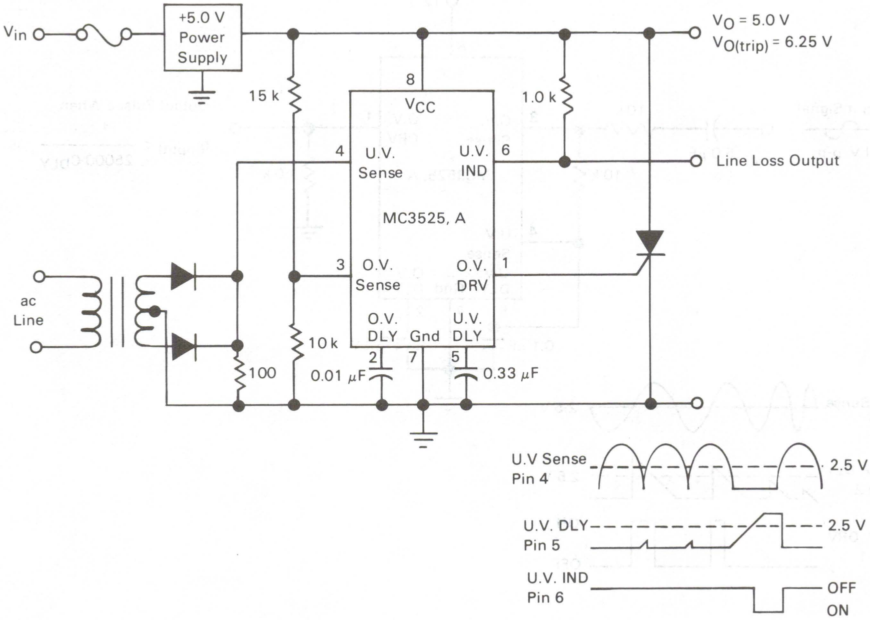

Vin
+5.0 V
Power
Supply
VO = 5.0 V
VO(trip) = 6.25 V
15 k
8
VCC
1.0 k
4
U.V.
Sense
6
U.V.
IND
Line Loss Output
MC3525, A
3
O.V.
Sense
1
O.V.
DRV
ac
Line
O.V.
DLY
Gnd
U.V.
DLY
10 k
100
2
7
5
0.01 μF
0.33 μF
U.V Sense
Pin 4
2.5 V
U.V. DLY
Pin 5
2.5 V
U.V. IND
Pin 6
OFF
ON

FIGURE 13 — OVERVOLTAGE AUDIO ALARM CIRCUIT

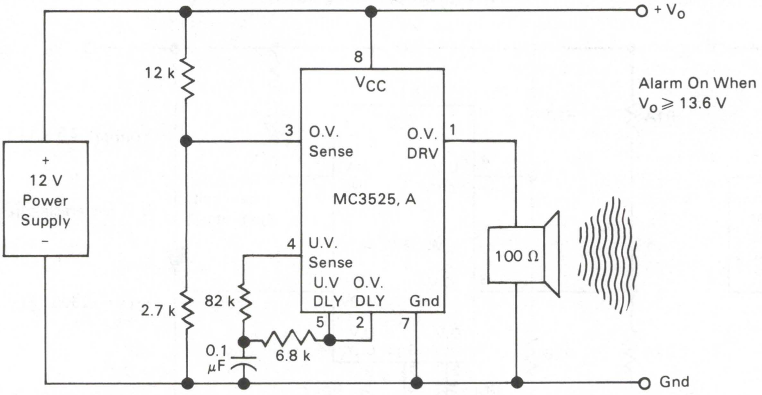
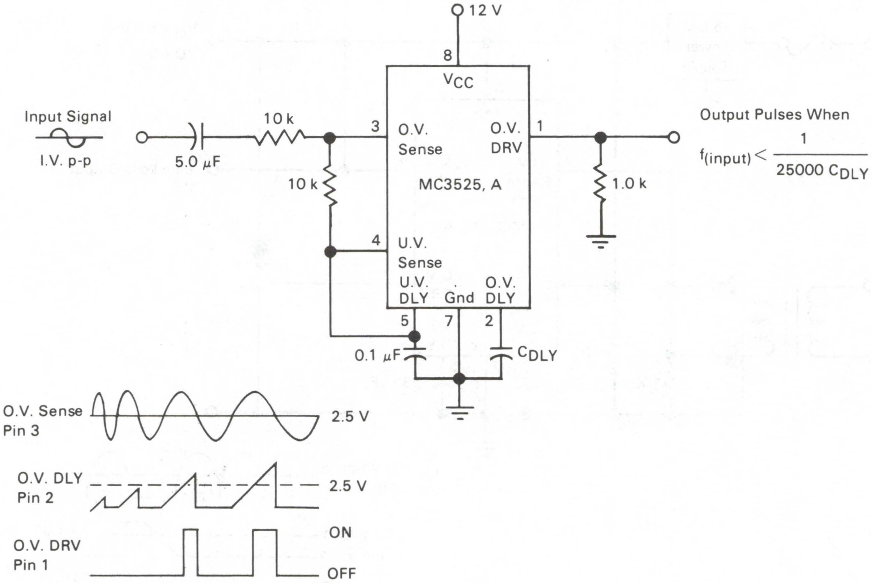

+ V$_o$
8
V$_{CC}$
12 k
Alarm On When
V$_o$ ≥ 13.6 V
3 O.V. Sense
O.V. DRV 1
+ 12 V Power Supply −
MC3525, A
4 U.V. Sense
U.V DLY
O.V. DLY
Gnd
100 Ω
2.7 k
82 k
5
2
7
0.1 µF
6.8 k
Gnd

FIGURE 14 — PROGRAMMABLE FREQUENCY SWITCH


12 V
8
V$_{CC}$
Input Signal
I.V. p-p
5.0 µF
10 k
3 O.V. Sense
O.V. DRV 1
MC3525, A
10 k
1.0 k
Output Pulses When
$f_{(input)} < \frac{1}{25000 C_{DLY}}$
4 U.V. Sense
U.V. DLY
Gnd
O.V. DLY
5
7
2
0.1 µF
C$_{DLY}$
O.V. Sense Pin 3
2.5 V
O.V. DLY Pin 2
2.5 V
O.V. DRV Pin 1
ON
OFF

CIRCUIT DESCRIPTION

The MC3425/MC3525 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. The block diagram is shown below in Figure 15. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6}\ R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 volts.

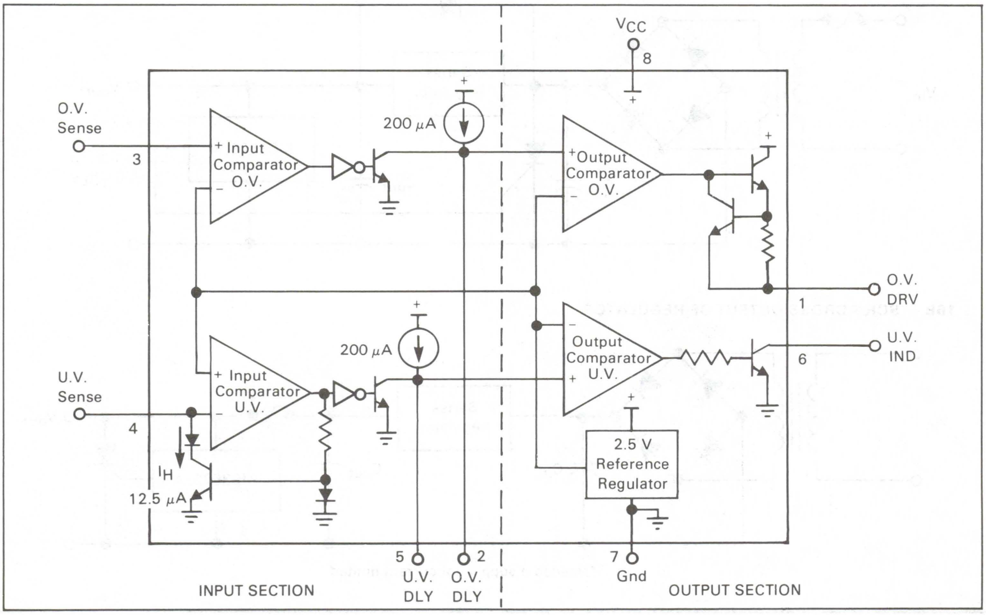
$$t_{DLY} = \frac{V_{ref}\,C_{DLY}}{I_{DLY(source)}} = \frac{2.5\,C_{DLY}}{200\,\mu A} = 12500\,C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is $\geqslant$ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425/MC3525 has an internal 2.5 V bandgap reference regulator with an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

FIGURE 15 — MC3425/MC3525 BLOCK DIAGRAM



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and <1.0 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 16 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

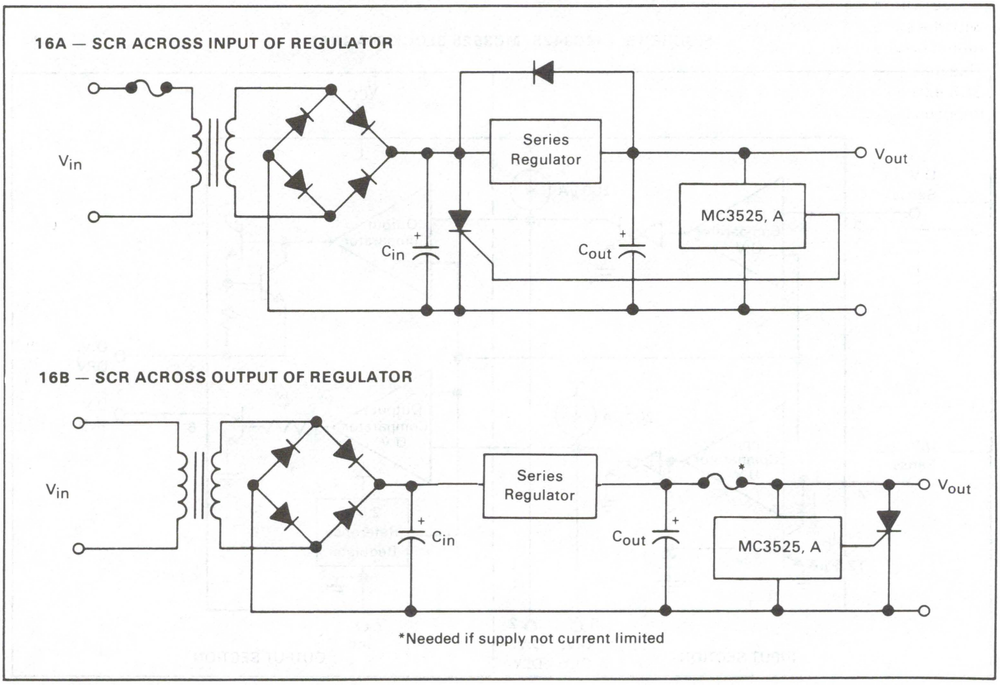
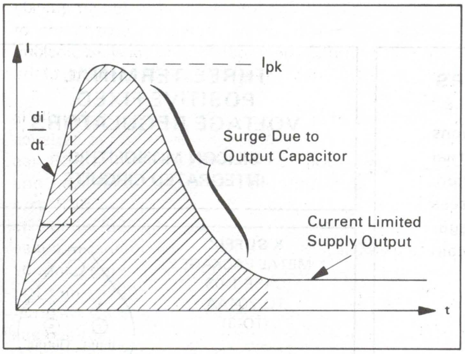

16A — SCR ACROSS INPUT OF REGULATOR
Vin
Series Regulator
Vout
MC3525, A
Cin
Cout
+
16B — SCR ACROSS OUTPUT OF REGULATOR
Vin
Series Regulator
Vout
MC3525, A
Cin
Cout
*
*Needed if supply not current limited

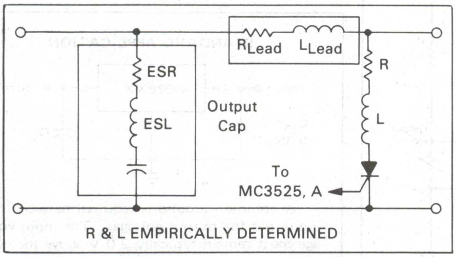
FIGURE 17 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 18 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

MC7800 Series

MOTOROLA

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

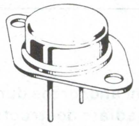
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

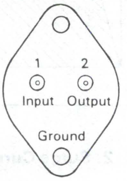
- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)

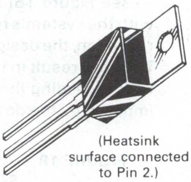




(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

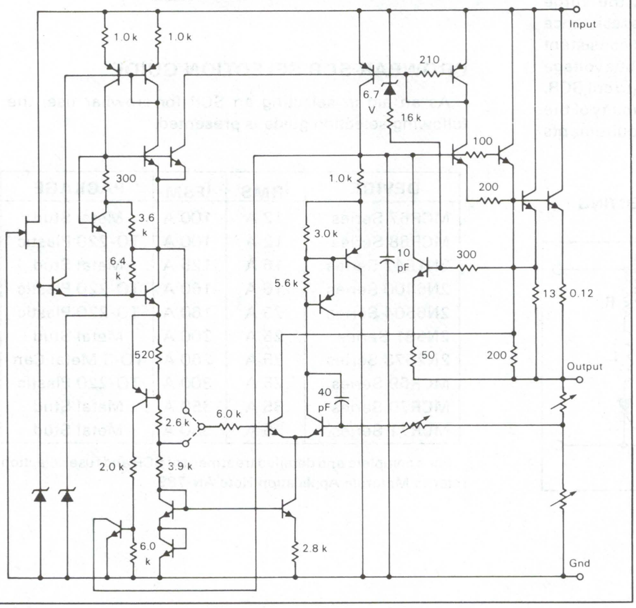
T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB



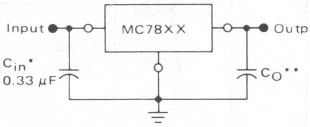
Pin 1. Input
2. Ground
3. Output

(Heatsink surface connected to Pin 2.)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

ORDERING INFORMATION

Device	Output Voltage Tolerance	Temperature Range	Package
MC78XXK	4%	-55 to +150°C	Metal Power
MC78XXAK	2%		
MC78XXBK	4%	-40 to +125°C	
MC78XXCK	4%	0 to +125°C	
MC78XXACK	2%		
MC78XXCT	4%		Plastic Power
MC78XXACT	2%		
MC78XXBT	4%	-40 to +125°C	

TYPE NO /VOLTAGE			
MC7805	5.0 Volts	MC7815	15 Volts
MC7806	6.0 Volts	MC7818	18 Volts
MC7808	8.0 Volts	MC7824	24 Volts
MC7812	12 Volts		

MC7800 Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V)	V_{in}	35	Vdc
(24 V)		40	
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J		°C
MC7800, A		-55 to +150	
MC7800C, AC		0 to +150	
MC7800, B		-40 to +150	

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7805, B, C
ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage	V_O										Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)											
7.0 Vdc ≤ V_{in} ≤ 20 Vdc		—	—	—	—	—	—	4.75	5.0	5.25	
8.0 Vdc ≤ V_{in} ≤ 20 Vdc		4.65	5.0	5.35	4.75	5.0	5.25	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	2.0	50	—	7.0	100	—	7.0	100	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		—	1.0	25	—	2.0	50	—	2.0	50	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	25	100	—	40	100	—	40	100	
250 mA ≤ I_O ≤ 750 mA		—	8.0	25	—	15	50	—	15	50	
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change	ΔI_B										mA
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	—	—	—	—	—	—	—	1.3	
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	0.3	0.8	—	—	1.3	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	68	75	—	—	68	—	—	68	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	—	-1.1	—	mV/ °C

MC7805A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2)	Reg_{line}							mV
7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	2.0	10	—	7.0	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		—	3.0	10	—	10	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C		—	1.0	4.0	—	2.0	25	
7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C		—	2.0	10	—	7.0	50	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	25	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	25	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	8.0	50	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
T_J = +25°C		—	3.2	4.0	—	4.3	6.0	
Quiescent Current Change	ΔI_B							mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C		68	75	—	—	—	—	
8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA		68	75	—	—	68	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	mV/°C

NOTES: 1. T_{low} = –55°C for MC78XX, A
= 0° for MC78XXC, AC
= –40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7806, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7806			MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)	V_O										Vdc
8.0 Vdc ≤ V_{in} ≤ 21 Vdc		—	—	—	—	—	—	5.7	6.0	6.3	
9.0 Vdc ≤ V_{in} ≤ 21 Vdc		5.65	6.0	6.35	5.7	6.0	6.3	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	3.0	60	—	9.0	120	—	9.0	120	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		—	2.0	30	—	3.0	60	—	3.0	60	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	27	100	—	43	120	—	43	120	
250 mA ≤ I_O ≤ 750 mA		—	9.0	30	—	16	60	—	16	60	
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change	ΔI_B										mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	—	—	—	—	—	—	—	1.3	
9.0 Vdc ≤ V_{in} ≤ 25 Vdc		—	0.3	0.8	—	—	1.3	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	65	73	—	—	65	—	—	65	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.7	—	—	-0.8	—	—	-0.8	—	mV/ °C

MC7806A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7806A			MC7806AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.88	6.0	6.12	5.88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	5.76	6.0	6.24	5.76	6.0	6.24	Vdc
Line Regulation (Note 2)	Reg_{line}							mV
8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	3.0	11	—	9.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		—	5.0	15	—	11	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = +25°C		—	2.0	5.0	—	3.0	30	
8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C		—	4.0	11	—	9.0	60	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	43	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	43	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	16	50	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
T_J = +25°C		—	3.2	4.0	—	4.3	6.0	
Quiescent Current Change	ΔI_B							mA
9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, T_J = +25°C		65	73	—	—	—	—	
9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA		65	73	—	—	65	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.7	—	—	-0.8	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7808, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7808			MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage	V_O										Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)											
10.5 Vdc ≤ V_{in} ≤ 23 Vdc		—	—	—	—	—	—	7.6	8.0	8.4	
11.5 Vdc ≤ V_{in} ≤ 23 Vdc		7.6	8.0	8.4	7.6	8.0	8.4	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		—	3.0	80	—	12	160	—	12	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		—	2.0	40	—	5.0	80	—	5.0	80	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	28	100	—	45	160	—	45	160	
250 mA ≤ I_O ≤ 750 mA		—	9.0	40	—	16	80	—	16	80	
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change	ΔI_B										mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		—	—	—	—	—	—	—	—	1.0	
11.5 Vdc ≤ V_{in} ≤ 25 Vdc		—	0.3	0.8	—	—	1.0	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	62	70	—	—	62	—	—	62	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.0	—	—	-0.8	—	—	-0.8	—	mV/ °C

MC7808A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7808A			MC7808AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.84	8.0	8.16	7.84	8.0	8.16	Vdc
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)		7.7	8.0	8.3	7.7	8.0	8.3	
10.6 Vdc ≤ V_{in} ≤ 23 Vdc								
Line Regulation (Note 2)	Reg_{line}							mV
10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	4.0	13	—	12	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		—	6.0	20	—	15	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = +25°C		—	2.0	6.0	—	5.0	40	
10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C		—	4.0	13	—	12	80	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	45	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	45	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	16	50	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
T_J = +25°C		—	3.2	4.0	—	4.3	6.0	
Quiescent Current Change	ΔI_B							mA
11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
10.6 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, T_J = +25°C		62	70	—	—	—	—	
11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA		62	70	—	—	62	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.0	—	—	-0.8	—	mV/°C

NOTES: 1. T_{low} = –55°C for MC78XX, A
= 0° for MC78XXC, AC
= –40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7812, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7812			MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage	V_O										Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)											
14.5 Vdc ≤ V_{in} ≤ 27 Vdc		—	—	—	—	—	—	11.4	12	12.6	
15.5 Vdc ≤ V_{in} ≤ 27 Vdc		11.4	12	12.6	11.4	12	12.6	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
14.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	5.0	120	—	13	240	—	13	240	
16 Vdc ≤ V_{in} ≤ 22 Vdc		—	3.0	60	—	6.0	120	—	6.0	120	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	30	120	—	46	240	—	46	240	
250 mA ≤ I_O ≤ 750 mA		—	10	60	—	17	120	—	17	120	
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change	ΔI_B										mA
14.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	—	—	—	—	—	—	—	1.0	
15 Vdc ≤ V_{in} ≤ 30 Vdc		—	0.3	0.8	—	—	1.0	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection	RR	61	68	—	—	60	—	—	60	—	dB
15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz											
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	—	-1.0	—	mV/ °C

MC7812A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7812A			MC7812AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)		11.5	12	12.5	11.5	12	12.5	
14.8 Vdc ≤ V_{in} ≤ 27 Vdc								
Line Regulation (Note 2)	Reg_{line}							mV
14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	5.0	18	—	13	120	
16 Vdc ≤ V_{in} ≤ 22 Vdc		—	8.0	30	—	16	120	
16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = +25°C		—	3.0	9.0	—	6.0	60	
14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C		—	5.0	18	—	13	120	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	46	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	46	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	17	50	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
T_J = +25°C		—	3.4	4.0	—	4.4	6.0	
Quiescent Current Change	ΔI_B							mA
15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, T_J = +25°C		61	68	—	—	—	—	
15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA		61	68	—	—	60	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7815, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7815			MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage	V_O										Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)											
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	—	—	—	—	—	14.25	15	15.75	
18.5 Vdc ≤ V_{in} ≤ 30 Vdc		14.25	15	15.75	14.25	15	15.75	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	6.0	150	—	13	300	—	13	300	
20 Vdc ≤ V_{in} ≤ 26 Vdc		—	3.0	75	—	6.0	150	—	6.0	150	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	32	150	—	52	300	—	52	300	
250 mA ≤ I_O ≤ 750 mA		—	10	75	—	20	150	—	20	150	
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change	ΔI_B										mA
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	—	—	—	—	—	—	—	1.0	
18.5 Vdc ≤ V_{in} ≤ 30 Vdc		—	0.3	0.8	—	—	1.0	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	60	66	—	—	58	—	—	58	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	—	-1.0	—	mV/ °C

MC7815A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7815A			MG7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)		14.4	15	15.6	14.4	15	15.6	
17.9 Vdc ≤ V_{in} ≤ 30 Vdc								
Line Regulation (Note 2)	Reg_{line}							mV
17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	6.0	22	—	13	150	
20 Vdc ≤ V_{in} ≤ 26 Vdc		—	6.0	22	—	16	150	
20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C		—	3.0	10	—	6.0	75	
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C		—	6.0	22	—	13	150	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	52	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	52	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	20	50	
Quiescent Current	I_B	—	—	5.5	—	—	6.0	mA
T_J = +25°C		—	3.4	4.5	—	4.4	6.0	
Quiescent Current Change	ΔI_B							mA
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C		60	66	—	—	—	—	
18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA		60	66	—	—	58	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7818, B, C
ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7818			MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage	V_O										Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)											
21 Vdc ≤ V_{in} ≤ 33 Vdc		—	—	—	—	—	—	17.1	18	18.9	
22 Vdc ≤ V_{in} ≤ 33 Vdc		17.1	18	18.9	17.1	18	18.9	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
21 Vdc ≤ V_{in} ≤ 33 Vdc		—	7.0	180	—	25	360	—	25	360	
24 Vdc ≤ V_{in} ≤ 30 Vdc		—	4.0	90	—	10	180	—	10	180	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	35	180	—	55	360	—	55	360	
250 mA ≤ I_O ≤ 750 mA		—	12	90	—	22	180	—	22	180	
Quiescent Current (T_J = +25°C)	I_B	—	3.5	6.0	—	4.5	8.0	—	4.5	8.0	mA
Quiescent Current Change	ΔI_B										mA
21 Vdc ≤ V_{in} ≤ 33 Vdc		—	—	—	—	—	—	—	—	1.0	
22 Vdc ≤ V_{in} ≤ 33 Vdc		—	0.3	0.8	—	—	1.0	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz	RR	59	65	—	—	57	—	—	57	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/ V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±2.3	—	—	-1.0	—	—	-1.0	—	mV/ °C

MC7818A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 1.0 A, $T_J = T_{low}$ to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7818A			MC7818AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.64	18	18.36	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	17.3	18	18.7	17.3	18	17.3	Vdc
Line Regulation (Note 2)	Reg_{line}							mV
21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA		—	7.0	31	—	25	180	
24 Vdc ≤ V_{in} ≤ 30 Vdc		—	12	45	—	28	180	
24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C		—	4.0	15	—	10	90	
20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C		—	7.0	31	—	25	180	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	55	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	55	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	22	50	
Quiescent Current	I_B	—	—	5.5	—	—	6.0	mA
T_J = +25°C		—	3.4	4.5	—	4.5	6.0	
Quiescent Current Change	ΔI_B							mA
21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, T_J = +25°C		59	65	—	—	—	—	
22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA		59	65	—	—	57	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±2.3	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7824, B, C
ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7824			MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W)	V_O										Vdc
27 Vdc ≤ V_{in} ≤ 38 Vdc		—	—	—	—	—	—	22.8	24	25.2	
28 Vdc ≤ V_{in} ≤ 38 Vdc		22.8	24	25.2	22.8	24	25.2	—	—	—	
Line Regulation (T_J = +25°C, Note 2)	Reg_{line}										mV
27 Vdc ≤ V_{in} ≤ 38 Vdc		—	10	240	—	31	480	—	31	480	
30 Vdc ≤ V_{in} ≤ 36 Vdc		—	5.0	120	—	14	240	—	14	240	
Load Regulation (T_J = +25°C, Note 2)	Reg_{load}										mV
5.0 mA ≤ I_O ≤ 1.5 A		—	40	240	—	60	480	—	60	480	
250 mA ≤ I_O ≤ 750 mA		—	15	120	—	25	240	—	25	240	
Quiescent Current (T_J = +25°C)	I_B	—	3.6	6.0	—	4.6	8.0	—	4.6	8.0	mA
Quiescent Current Change	ΔI_B										mA
27 Vdc ≤ V_{in} ≤ 38 Vdc		—	—	—	—	—	—	—	—	1.0	
28 Vdc ≤ V_{in} ≤ 38 Vdc		—	0.3	0.8	—	—	1.0	—	—	—	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.5	—	—	0.5	—	—	0.5	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	56	62	—	—	54	—	—	54	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	µV/V_O
Output Resistance f = 1.0 kHz	r_O	—	20	—	—	20	—	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±3.0	—	—	-1.5	—	—	-1.5	—	mV/°C

MC7824A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7824A			MC7824AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23.5	24	24.5	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	23	24	25	23	24	25	Vdc
Line Regulation (Note 2)	Reg_{line}							mV
27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		—	10	36	—	31	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc		—	15	60	—	35	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = +25°C		—	5.0	19	—	14	120	
26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C		—	10	36	—	31	240	
Load Regulation (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		—	2.0	25	—	60	100	
5.0 mA ≤ I_O ≤ 1.0 A		—	2.0	25	—	60	100	
250 mA ≤ I_O ≤ 750mA, T_J = +25°C		—	1.0	15	—	—	—	
250 mA ≤ I_O ≤ 750 mA		—	1.0	25	—	25	50	
Quiescent Current	I_B	—	—	6.0	—	—	6.0	mA
T_J = +25°C		—	3.6	5.0	—	4.6	6.0	
Quiescent Current Change	ΔI_B							mA
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		—	0.3	0.5	—	—	0.8	
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C		—	0.2	0.5	—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	0.04	0.2	—	—	0.5	
Ripple Rejection	RR							dB
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, T_J = +25°C		56	62	—	—	—	—	
28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA		56	62	—	—	54	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±3.0	—	—	-1.5	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

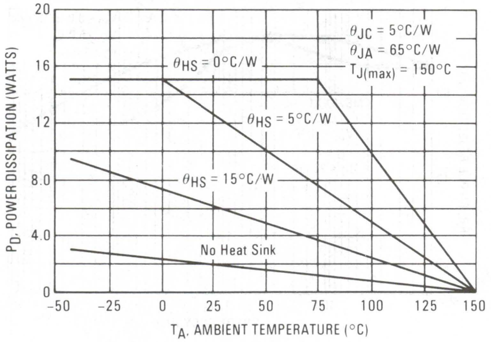


FIGURE 2 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)

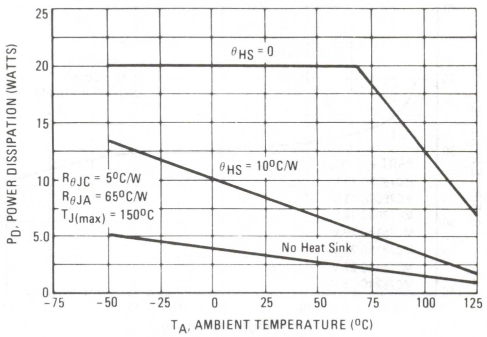


FIGURE 3 — INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

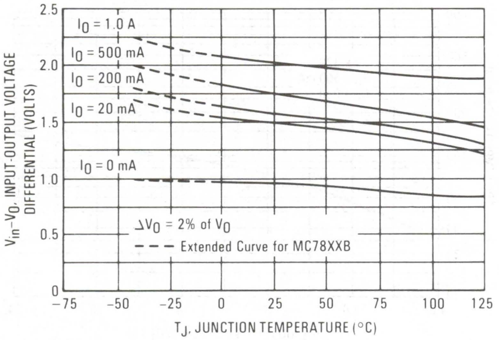


FIGURE 4 — INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XX, A)

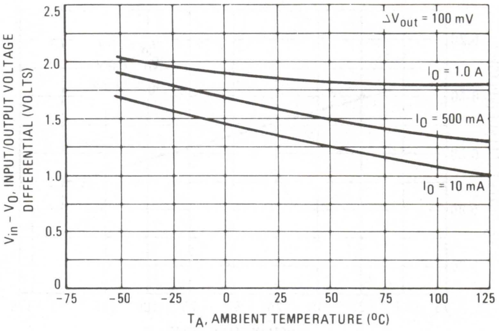


FIGURE 5 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XXC, AC, B)

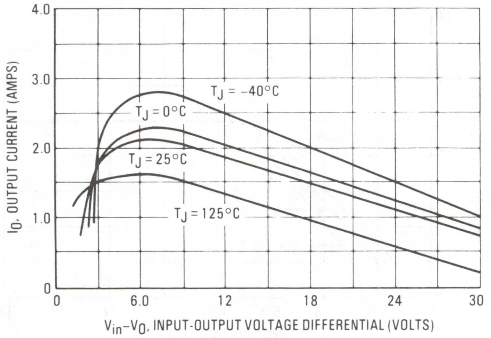
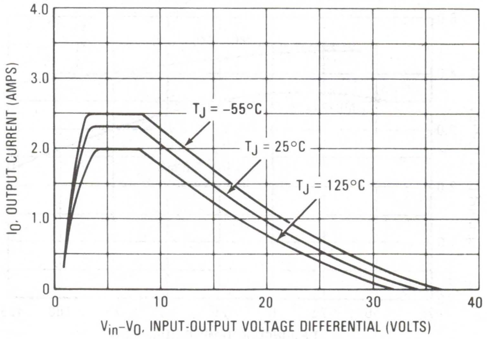


FIGURE 6 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XX, A)



TYPICAL CHARACTERISTICS (continued)
(T_A = 25°C unless otherwise noted.)

FIGURE 7 — RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

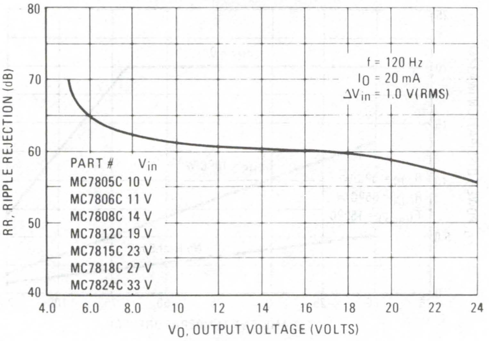


FIGURE 8 — RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC, A)

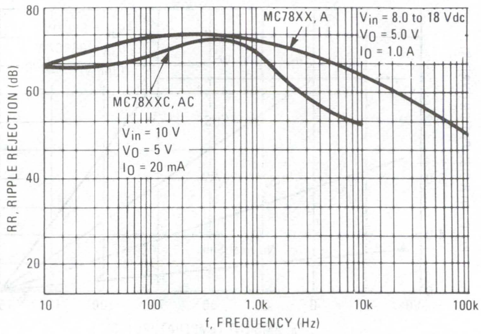


FIGURE 9 — OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

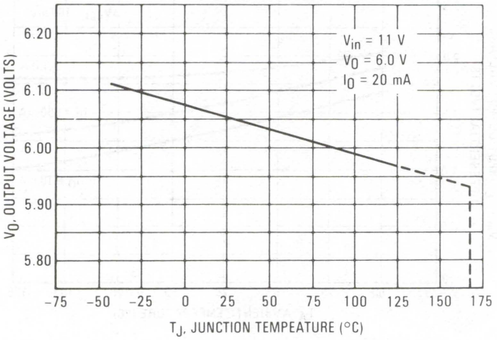


FIGURE 10 — OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

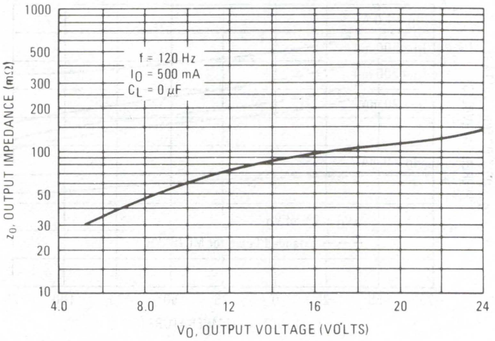


FIGURE 11 — QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC, B)

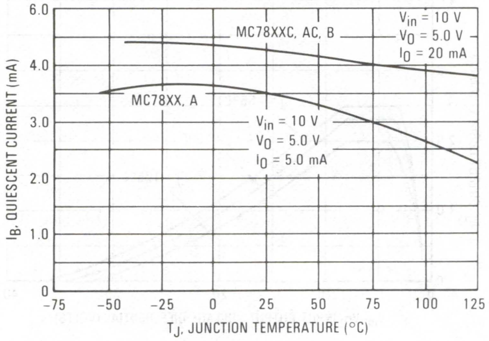
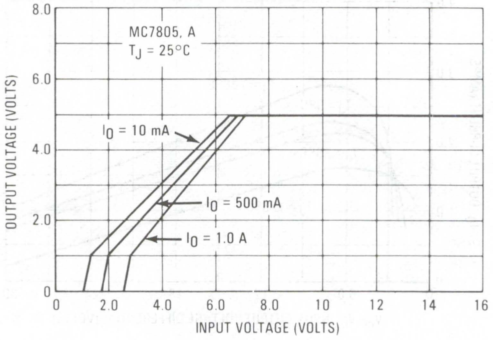


FIGURE 12 — DROPOUT CHARACTERISTICS (MC78XX, A)



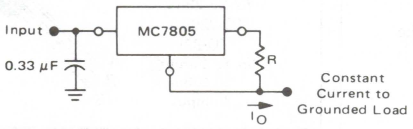
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 13 – CURRENT REGULATOR



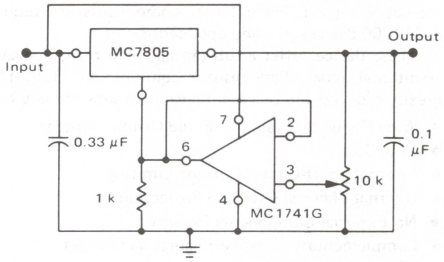
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

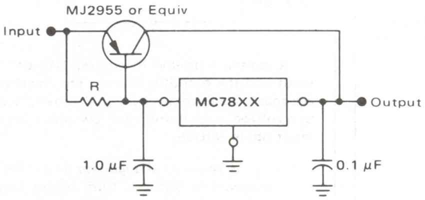
FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geqslant 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

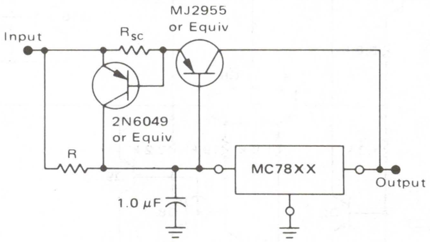
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MC78L00C,AC Series

MOTOROLA

THREE-TERMINAL LOW CURRENT POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

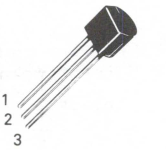
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL LOW CURRENT POSITIVE FIXED VOLTAGE REGULATORS

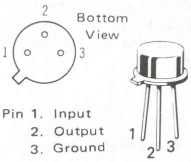
P SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)

Pin 1. Output
2. Ground
3. Input



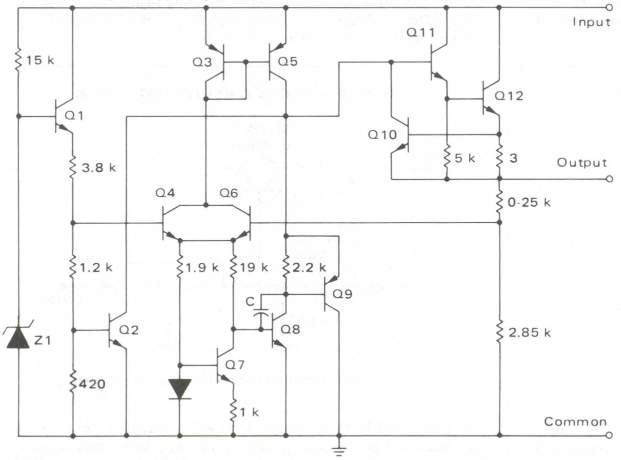
G SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)

(Case connected to Pin 3)

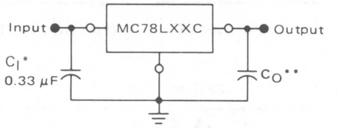


Pin 1. Input
2. Output
3. Ground

REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

ORDERING INFORMATION

Device	Junction Temperature Range	Package
MC78LXXACG	$T_J = 0°C$ to $+125°C$	Metal Can
MC78LXXACP	$T_J = 0°C$ to $+125°C$	Plastic Transistor
MC78LXXCG	$T_J = 0°C$ to $+125°C$	Metal Can
MC78LXXCP	$T_J = 0°C$ to $+125°C$	Plastic Transistor

XX indicates nominal voltage

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V)	V_I	30	Vdc
(12 V – 18 V)		35	
(24 V)		40	
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05C			MC78L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
7.0 Vdc ≤ V_I ≤ 20 Vdc		–	55	200	–	55	150	
8.0 Vdc ≤ V_I ≤ 20 Vdc		–	45	150	–	45	100	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	11	60	–	11	60	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	5.0	30	–	5.0	30	
Output Voltage	V_O							Vdc
(7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		4.5	–	5.5	4.75	–	5.25	
(V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)		4.5	–	5.5	4.75	–	5.25	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.8	6.0	–	3.8	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(8.0 Vdc ≤ V_I ≤ 20 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08C			MC78L08AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
10.5 Vdc ≤ V_I ≤ 23 Vdc		–	20	200	–	20	175	
11 Vdc ≤ V_I ≤ 23 Vdc		–	12	150	–	12	125	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	80	–	15	80	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	6.0	40	–	8.0	40	
Output Voltage	V_O							Vdc
(10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		7.2	–	8.8	7.6	–	8.4	
(V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)		7.2	–	8.8	7.6	–	8.4	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	–	60	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	20	–	–	20	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	36	55	–	37	57	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L12C			MC78L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^oC$)	V_O	11.1	12	12.9	11.5	12	12.5	Vdc
Line Regulation	Reg_{line}							mV
($T_J = +25^oC$, I_O = 40 mA)								
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
($T_J = +25^oC$, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
($T_J = +25^oC$, 1.0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		10.8	–	13.2	11.4	–	12.6	
(V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)		10.8	–	13.2	11.4	–	12.6	
Input Bias Current	I_{IB}							mA
($T_J = +25^oC$)		–	4.2	6.5	–	4.2	6.5	
($T_J = +125^oC$)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, $T_J = +25^oC$)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential ($T_J = +25^oC$)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L15C			MC78L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^oC$)	V_O	13.8	15	16.2	14.4	15	15.6	Vdc
Line Regulation	Reg_{line}							mV
($T_J = +25^oC$, I_O = 40 mA)								
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	130	300	–	130	300	
20 Vdc ≤ V_I ≤ 30 Vdc		–	110	250	–	110	250	
Load Regulation	Reg_{load}							mV
($T_J = +25^oC$, 1.0 mA ≤ I_O ≤ 100 mA)		–	25	150	–	25	150	
($T_J = +25^oC$, 1.0 mA ≤ I_O ≤ 40 mA)		–	12	75	–	12	75	
Output Voltage	V_O							Vdc
(17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		13.5	–	16.5	14.25	–	15.75	
(V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)		13.5	–	16.5	14.25	–	15.75	
Input Bias Current	I_{IB}							mA
($T_J = +25^oC$)		–	4.4	6.5	–	4.4	6.5	
($T_J = +125^oC$)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(20 Vdc ≤ V_I ≤ 30 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, $T_J = +25^oC$)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential ($T_J = +25^oC$)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L18C			MC78L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	16.6	18	19.4	17.3	18	18.7	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
21.4 Vdc ≤ V_I ≤ 33 Vdc		–	32	325				
20.7 Vdc ≤ V_I ≤ 33 Vdc					–	45	325	
22 Vdc ≤ V_I ≤ 33 Vdc		–	27	275				
21 Vdc ≤ V_I ≤ 33 Vdc					–	35	275	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	30	170	–	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	15	85	–	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		16.2	–	17.8				
(20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					17.1	–	18.9	
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)		16.2	–	17.8				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					17.1	–	18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)		–	–	1.5				
(21 Vdc ≤ V_I = 33 Vdc)					–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	22.1	24	25.9	23	24	25	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	35	350	–	–	–	
28 Vdc ≤ V_I ≤ 38 Vdc		–	30	300	–	50	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	60	350	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					22.8	–	25.2	
(28 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)					22.8	–	25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	30	43	–	31	45	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

TYPICAL CHARACTERISTICS

($T_A = +25^{\circ}C$ unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

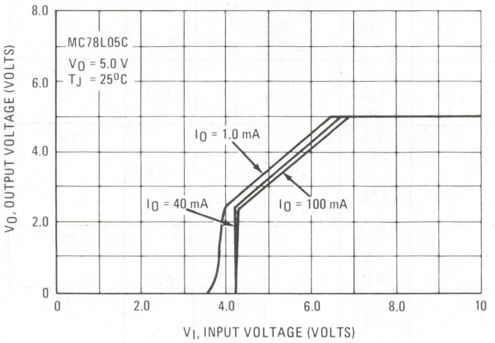


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

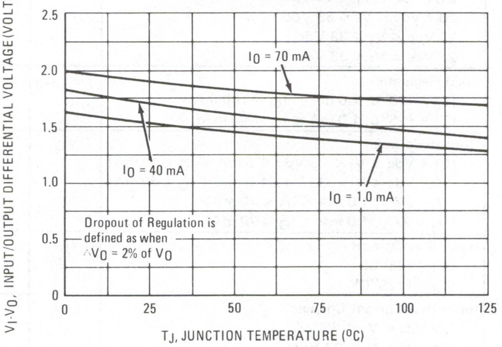


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

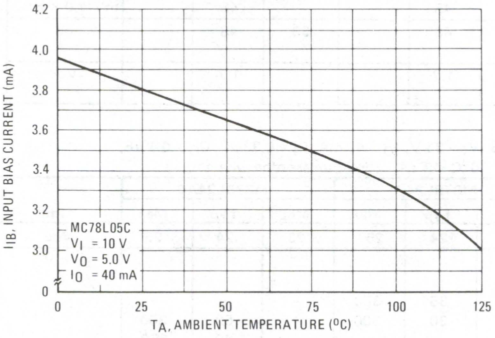


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

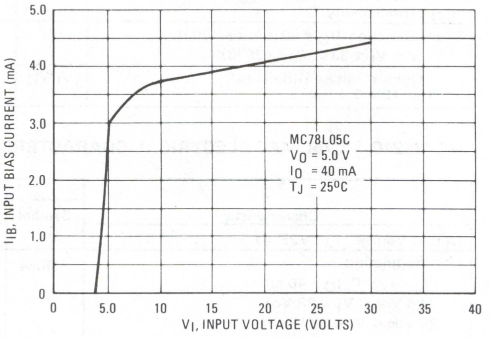


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

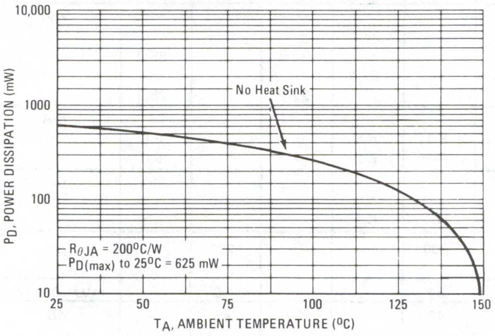
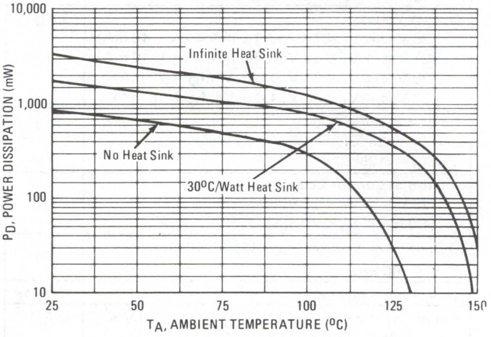


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



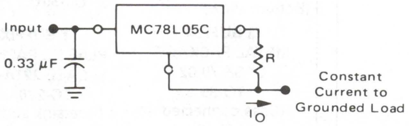
APPLICATIONS INFORMATION

Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 — CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ \text{V}}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 — ±15 V TRACKING VOLTAGE REGULATOR

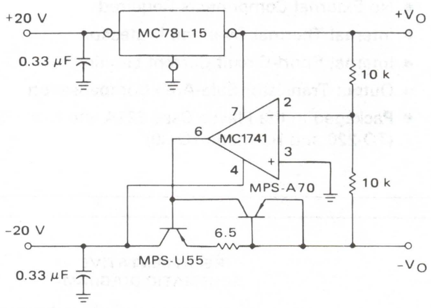
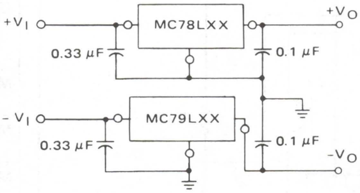


FIGURE 9 — POSITIVE AND NEGATIVE REGULATOR



MC78M00 Series

MOTOROLA

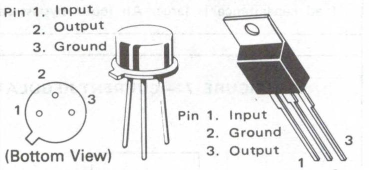
THREE-TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

MC78M00 SERIES THREE-TERMINAL MEDIUM CURRENT POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

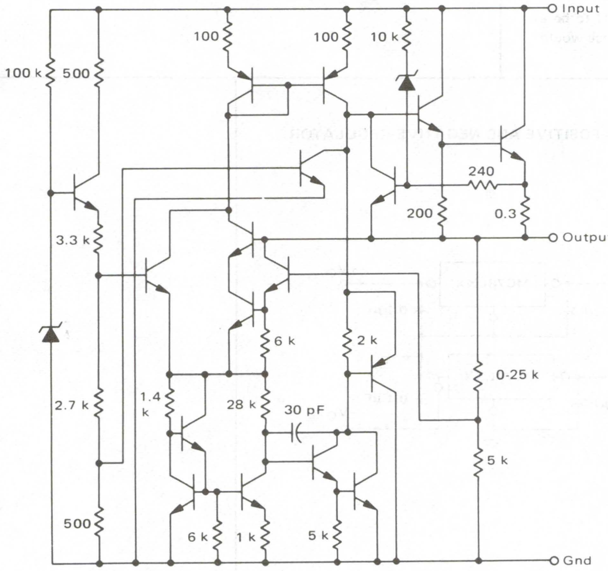
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 79 (TO-220 and Hermetic TO-39)



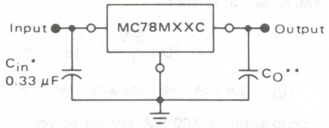
G SUFFIX
METAL PACKAGE
CASE 79-02
TO-39
(Case connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB
(Heatsink surface connected to Pin 2)

REPRESENTATIVE SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
MC78MXXCG	$T_J = 0°C$ to $+125°C$	Metal Can
MC78MXXCT	$T_J = 0°C$ to $+125°C$	Plastic Power
MC78MXXBT	$T_J = -40°C$ to $+125°C$	Plastic Power

TYPE NO./VOLTAGE

MC7805MB,C	5.0 Volts	MC7815MB,C	15 Volts
MC7806MB,C	6.0 Volts	MC7818MB,C	18 Volts
MC7808MB,C	8.0 Volts	MC7820MB,C	20 Volts
MC7812MB,C	12 Volts	MC7824MB,C	24 Volts

MC78M00 Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (20 V – 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation)			
Plastic Package			
T_A = 25°C	P_D	Internally Limited	
Derate above T_A = 25°C	θ_{JA}	70	°C/W
T_C = 25°C	P_D	Internally Limited	
Derate above T_C = 110°C	θ_{JC}	5.0	°C/W
Metal Package			
T_A = 25°C	P_D	Internally Limited	
Derate above T_A = 25°C	θ_{JA}	185	°C/W
T_C = 25°C	P_D	Internally Limited	
Derate above T_C = 85°C	θ_{JC}	25	°C/W
Operating Junction Temperature Range MC78MXXC MC78MXXB	T_J	0 to +125 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

MC78M05 ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 200 mA, $^*T_{low} < T_J < +125$°C, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C)					
(7.0 Vdc $\leq V_I \leq$ 25 Vdc)		—	3.0	100	
(8.0 Vdc $\leq V_I \leq$ 25 Vdc)		—	1.0	50	
Load Regulation	Reg_{load}				mV
(T_J = +25°C, 5.0 mA $\leq I_O \leq$ 500 mA)		—	20	100	
(T_J = +25°C, 5.0 mA $\leq I_O \leq$ 200 mA)		—	10	50	
Output Voltage (8.0 Vdc $\leq V_I \leq$ 25 Vdc, 5.0 mA $\leq I_O \leq$ 200 mA)	V_O	4.75	—	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.5	6.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(8.0 Vdc $\leq V_I \leq$ 25 Vdc)		—	—	0.8	
(5.0 mA $\leq I_O \leq$ 200 mA)		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leq$ f $\leq$ 100 kHz)	V_n	—	40	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	20	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 8.0 V $\leq V_I \leq$ 18 V)	RR	—	80	—	dB
(I_O = 300 mA, f = 120 Hz, 8.0 $\leq V_I \leq$ 18 V, T_J = 25°C)		—	80	—	
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	300	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

$^*T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

MC78M06 ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C) (8.0 Vdc ≤ V_I ≤ 25 Vdc) (9.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 — —	 5.0 1.5	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 20 10	 120 60	mV
Output Voltage (9.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	5.7	—	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.5	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	45	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	24	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	— —	80 80	— —	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	270	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M08 ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C) (10.5 Vdc ≤ V_I ≤ 25 Vdc) (11 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 — —	 6.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 160 80	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	7.6	—	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.6	6.0	mA
Quiescent Current Change (11.5 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	52	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	32	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	 — —	 80 80	 — —	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	250	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

*T_{low} = −40°C for MC78MXXB
= 0°C for MC78MXXC

MC78M12 ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 200 mA, *T_{low} < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C)	Reg_{line}				mV
(14.5 Vdc ≤ V_I ≤ 30 Vdc)		—	8.0	100	
(16 Vdc ≤ V_I ≤ 22 Vdc)		—	2.0	50	
Load Regulation	Reg_{load}				mV
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA)		—	25	240	
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)		—	10	120	
Output Voltage (15.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	11.4	—	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.8	6.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(15.5 Vdc ≤ V_I ≤ 30 Vdc)		—	—	0.8	
(5.0 mA ≤ I_O ≤ 200 mA)		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	48	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V)	RR	—	80	—	dB
(I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)		—	80	—	
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M15 ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 200 mA, *T_{low} < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}				mV
(17.5 Vdc ≤ V_I ≤ 30 Vdc)		—	10	100	
(20 Vdc ≤ V_I ≤ 30 Vdc)		—	3.0	50	
Load Regulation	Reg_{load}				mV
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA)		—	25	300	
(T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)		—	10	150	
Output Voltage (18.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	14.25	—	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.8	6.0	mA
Quiescent Current Change	ΔI_{IB}				
(18.5 Vdc ≤ V_I ≤ 30 Vdc)		—	—	0.8	
(5.0 mA ≤ I_O ≤ 200 mA)		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	60	mV/1.0 k Hrs.
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V)		—	70	—	
(I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)		—	70	—	
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

*T_{low} = −40°C for MC78MXXB
= 0°C for MC78MXXC

MC78M18 ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C) (21 Vdc ≤ V_I ≤ 33 Vdc) (24 Vdc ≤ V_I ≤ 33 Vdc)	Reg_{line}	— —	10 40	100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	360 180	mV
Output Voltage (22 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	17.1	—	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.8	6.5	mA
Quiescent Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	100	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	72	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	— —	70 70	— —	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M20 ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C) (23 Vdc ≤ V_I ≤ 35 Vdc) (24 Vdc ≤ V_I ≤ 35 Vdc)	Reg_{line}	— —	10 5.0	100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	400 200	mV
Output Voltage (24 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	19	—	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.9	6.5	mA
Quiescent Current Change (24 Vdc ≤ V_I ≤ 35 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	110	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	80	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	— —	70 70	— —	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	−1.1	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

*T_{low} = −40°C for MC78MXXB
= 0°C for MC78MXXC

MC78M24 ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 200 mA, *T_{low} < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C) (27 Vdc ≤ V_I ≤ 38 Vdc) (28 Vdc ≤ V_I ≤ 38 Vdc)	Reg_{line}	 — —	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 480 240	mV
Output Voltage (28 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	22.8	—	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	5.0	7.0	mA
Quiescent Current Change (28 Vdc ≤ V_I ≤ 38 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	170	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	96	mV/1.0 k Hrs.
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	— —	70 70	— —	dB
Input-Output Voltage Differential (I_O = 5.0 mA)	V_I-V_O	—	2.0	—	Vdc
Short-Circuit Current Limit (T_J = +25°C)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C)	$\Delta V_O/\Delta T$	—	−1.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

*T_{low} = −40°C for MC78MXXB
= 0°C for MC78MXXC

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220 (CASE 221A)

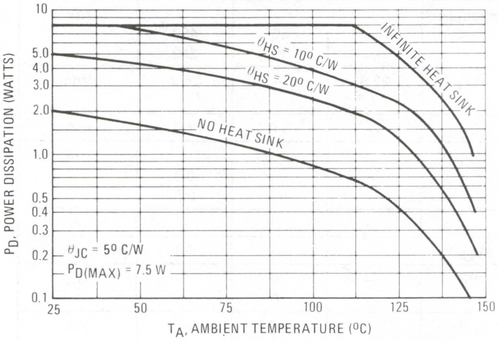


FIGURE 2 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-39 (CASE 79)

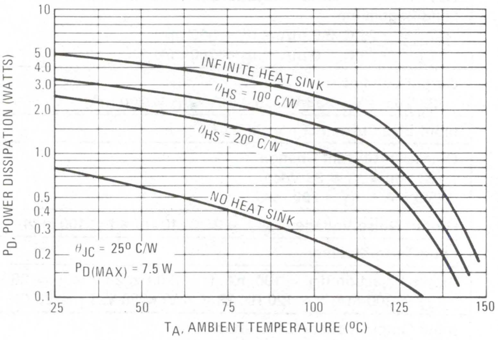


FIGURE 3 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

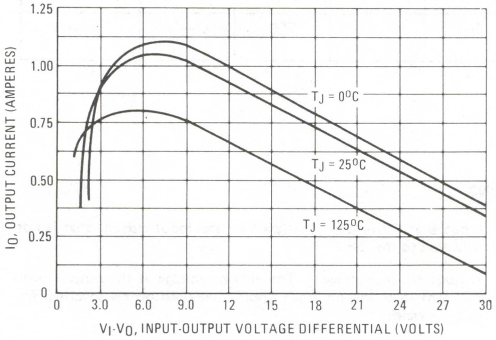
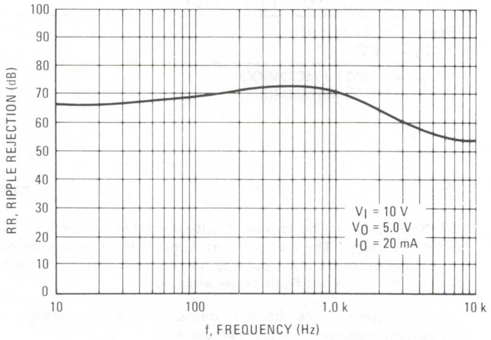


FIGURE 4 — RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



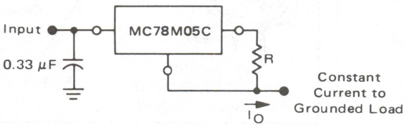
APPLICATIONS INFORMATION

Design Considerations

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the reulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 — CURRENT REGULATOR



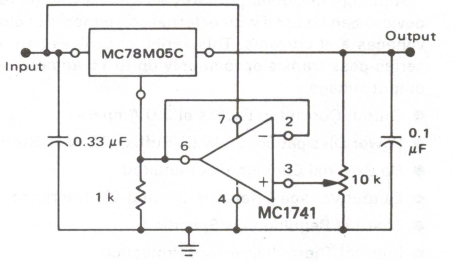
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

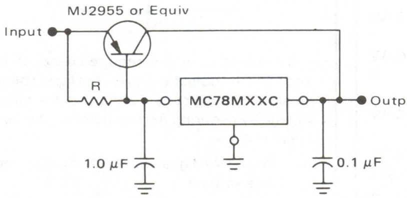
FIGURE 6 — ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geqslant 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

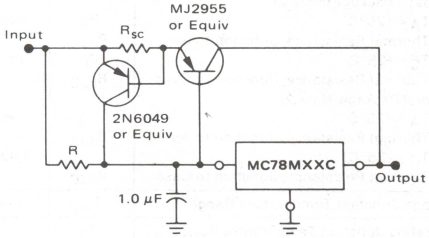
FIGURE 7 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 8 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

MC78T00
Series

MOTOROLA

Specifications and Applications Information

THREE-AMPERE POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

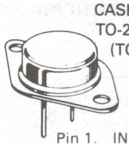
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 amperes at the nominal output voltage.

- Output Current in Excess of 3.0 Amperes
- Power Dissipation: 30 W (K-Suffix), 25 W (T-Suffix)
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

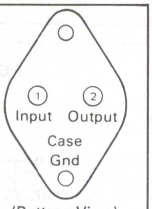
THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



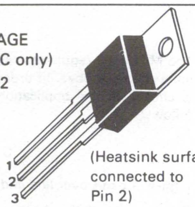
Pin 1. INPUT
2. OUTPUT
CASE GROUND



(Bottom View)

T SUFFIX
PLASTIC PACKAGE
(MC78TXXC and AC only)
CASE 221A-02
TO-220AB

Pin 1. INPUT
2. GROUND
3. OUTPUT

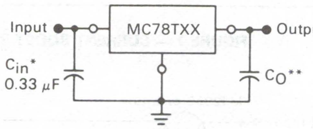


(Heatsink surface connected to Pin 2)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–12 V) (15 V–24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package (Note 2)			
T_A = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	65	°C/W
T_C = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Metal Package (Note 2)			
T_A = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Air	$R_{\theta JA}$	35	°C/W
T_C = +25°C	P_D	Internally Limited	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range MC78T00, A MC78T00C, AC	T_J	 −55 to +150 0 to +125	°C

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details).

** = C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Junction Temperature Range	Package
MC78TXXK	4%	−55 to +150°C	Metal Power
MC78TXXAK	2%*		
MC78TXXCK	4%	0 to +125°C	
MC78TXXACK	2%*		
MC78TXXCT	4%		Plastic Power
MC78TXXACT	2%*		

XX Indicates nominal voltage *2% regulators are available in 5, 12 and 15 volt devices

TYPE NO./VOLTAGE			
MC78T05	5.0 Volts	MC78T15	15 Volts
MC78T06	6.0 Volts	MC78T18	18 Volts
MC78T08	8.0 Volts	MC78T24	24 Volts
MC78T12	12 Volts		

MC78T05, A, AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 3.0 A, T_J = T_{low} to T_{high} [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T05A, AC			MC78T05, C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		4.9	5.0	5.1	4.8	5.0	5.2	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20 Vdc)		4.8	5.0	5.2	4.75	5.0	5.25	
Line Regulation (Note 3) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 2.0 A; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A)	Reg_{line}	—	3.0	10	—	3.0	25	mV
Load Regulation (Note 3)	Reg_{load}							mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	10	25	—	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	15	50	—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	$\%V_O/W$
Quiescent Current	I_B							mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	3.5	5.0	—	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	4.0	6.0	—	4.0	6.0	
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 2.0 A; 5.0 mA ≤ I_O ≤ 3.0 A)	ΔI_B	—	0.1	0.5	—	0.1	0.8	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	68	75	—	65	75	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	2.5	—	1.5	2.5	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O							mV/°C
MC78T05, MC78T05A		—	0.2	1.0	—	0.2	1.0	
MC78T05AC, C		—	0.2	—	—	0.2	—	

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T06, C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 3.0 A, T_J = T_{low} to T_{high} [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T06, C			Unit
		Min	Typ	Max	
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		5.75	6.0	6.25	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 8.3 Vdc ≤ V_{in} ≤ 21 Vdc)		5.7	6.0	6.3	
Line Regulation (Note 3) (8.25 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 8.25 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, I_O = 2.0 A; 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, I_O = 3.0 A)	Reg_{line}	—	4.0	30	mV
Load Regulation (Note 3)	Reg_{load}				mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	%V_O/W
Quiescent Current	I_B				mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	4.0	6.0	
Quiescent Current Change (8.25 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, I_O = 2.0 A; 5.0 mA ≤ I_O ≤ 3.0 A)	ΔI_B	—	0.1	0.8	mA
Ripple Rejection (9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	63	73	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}-V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	2.5	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O				mV/°C
MC78T06		—	0.3	1.2	
MC78T06C		—	0.3	—	

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T08, C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 3.0 A, T_J = T_{low} to T_{high} [Note 1], $P_O \leq P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T08, C			Unit
		Min	Typ	Max	
Output Voltage	V_O				Vdc
(5.0 mA $\leq I_O \leq$ 3.0 A, T_J = +25°C)		7.7	8.0	8.3	
(5.0 mA $\leq I_O \leq$ 3.0 A; 5.0 mA $\leq I_O \leq$ 2.0 A, 10.4 Vdc $\leq V_{in} \leq$ 23 Vdc)		7.6	8.0	8.4	
Line Regulation (Note 3) (10.3 Vdc $\leq V_{in} \leq$ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 10.3 Vdc $\leq V_{in} \leq$ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 10.7 Vdc $\leq V_{in} \leq$ 23 Vdc, I_O = 2.0 A; 11 Vdc $\leq V_{in} \leq$ 17 Vdc, I_O = 3.0 A)	Reg_{line}	—	4.0	35	mV
Load Regulation (Note 3)	Reg_{load}				mV
(5.0 mA $\leq I_O \leq$ 3.0 A, T_J = +25°C)		—	10	30	
(5.0 mA $\leq I_O \leq$ 3.0 A)		—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	$\%V_O/W$
Quiescent Current	I_B				mA
(5.0 mA $\leq I_O \leq$ 3.0 A, T_J = +25°C)		—	3.5	5.0	
(5.0 mA $\leq I_O \leq$ 3.0 A)		—	4.0	6.0	
Quiescent Current Change (10.3 Vdc $\leq V_{in} \leq$ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 10.7 Vdc $\leq V_{in} \leq$ 23 Vdc, I_O = 2.0 A; 5.0 mA $\leq I_O \leq$ 3.0 A)	ΔI_B	—	0.1	0.8	mA
Ripple Rejection (11 Vdc $\leq V_{in} \leq$ 21 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	61	71	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz $\leq$ f $\leq$ 100 kHz, T_J = +25°C)	V_n	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	2.5	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O				mV/°C
MC78T08		—	0.3	1.6	
MC78T08C		—	0.3	—	

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T12, A, AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 3.0 A, T_J = T_{low} to T_{high} [Note 1], $P_O \le P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T12A, AC			MC78T12, C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		11.75	12	12.25	11.5	12	12.5	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27 Vdc)		11.5	12	12.5	11.4	12	12.6	
Line Regulation (Note 3) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 2.0 A; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A)	Reg_{line}	—	6.0	18	—	6.0	45	mV
Load Regulation (Note 3)	Reg_{load}							mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	10	25	—	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	15	50	—	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	$\%V_O/W$
Quiescent Current	I_B							mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		—	3.5	5.0	—	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		—	4.0	6.0	—	4.0	6.0	
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 2.0 A; 5.0 mA ≤ I_O ≤ 3.0 A)	ΔI_B	—	0.1	0.5	—	0.1	0.8	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	61	67	—	57	67	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	2.5	—	1.5	2.5	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O							mV/°C
MC78T12, MC78T12A		—	0.5	2.4	—	0.5	2.4	
MC78T12AC, MC7812C		—	0.5	—	—	0.5	—	

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC   = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T15, A, AC, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 23$ V, $I_O = 3.0$ A, $T_J = T_{low}$ to T_{high} [Note 1], $P_O \leq P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T15A, AC			MC78T15, C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA $\leq I_O \leq 3.0$ A, $T_J = +25°C$) (5.0 mA $\leq I_O \leq 3.0$ A; 5.0 mA $\leq I_O \leq 2.0$ A, 17.5 Vdc $\leq V_{in} \leq 30$ Vdc)	V_O	14.7 14.4	15 15	15.3 15.6	14.4 14.25	15 15	15.6 15.75	Vdc
Line Regulation (Note 3) (17.6 Vdc $\leq V_{in} \leq 40$ Vdc, $I_O = 5.0$ mA, $T_J = +25°C$; 17.6 Vdc $\leq V_{in} \leq 40$ Vdc, $I_O = 1.0$ A, $T_J = +25°C$; 18 Vdc $\leq V_{in} \leq 30$ Vdc, $I_O = 2.0$ A; 20 Vdc $\leq V_{in} \leq 26$ Vdc, $I_O = 3.0$ A)	Reg_{line}	—	7.5	22	—	7.5	55	mV
Load Regulation (Note 3) (5.0 mA $\leq I_O \leq 3.0$ A, $T_J = +25°C$) (5.0 mA $\leq I_O \leq 3.0$ A)	Reg_{load}	— —	10 15	25 50	— —	10 15	30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, $T_A = +25°C$)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	$\%V_O/W$
Quiescent Current (5.0 mA $\leq I_O \leq 3.0$ A, $T_J = +25°C$) (5.0 mA $\leq I_O \leq 3.0$ A)	I_B	— —	3.5 4.0	5.0 6.0	— —	3.5 4.0	5.0 6.0	mA
Quiescent Current Change (17.6 Vdc $\leq V_{in} \leq 40$ Vdc, $I_O = 5.0$ mA, $T_J = +25°C$; 18 Vdc $\leq V_{in} \leq 30$ Vdc, $I_O = 2.0$ A; 5.0 mA $\leq I_O \leq 3.0$ A)	ΔI_B	—	0.1	0.5	—	0.1	0.8	mA
Ripple Rejection (18.5 Vdc $\leq V_{in} \leq 28.5$ Vdc, f = 120 Hz, $I_O = 2.0$ A)	RR	60	65	—	55	65	—	dB
Dropout Voltage ($I_O = 3.0$ A, $T_J = +25°C$)	$V_{in}-V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz $\leq$ f $\leq$ 100 kHz, $T_J = +25°C$)	V_n	—	10	—	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit ($V_{in} = 40$ Vdc, $T_J = +25°C$)	I_{SC}	—	1.0	2.0	—	1.0	2.0	A
Peak Output Current ($T_J = +25°C$)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage ($I_O = 5.0$ mA) MC78T15, MC78T15A MC78T15AC, MC7815C	TCV_O	— —	0.6 0.6	3.0 —	— —	0.6 0.6	3.0 —	mV/°C

Note 1. $T_{low} = -55°C$ for MC78TXX, A
= 0°C for MC78TXXC, AC
$T_{high} = +150°C$ for MC78TXX, A
= +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$
$P_{max} = 30$ W for K(TO-3) package
$P_{max} = 25$ W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T18, C

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 3.0 A, $T_J = T_{low}$ to T_{high} [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

Characteristic	Symbol	MC78T18, C			Unit
		Min	Typ	Max	
Output Voltage (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, T_J = +25°C) (5.0 mA $\leqslant I_O \leqslant$ 3.0 A; 5.0 mA $\leqslant I_O \leqslant$ 2.0 A, 20.6 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc)	V_O	 17.3 17.1	 18 18	 18.7 18.9	Vdc
Line Regulation (Note 3) (20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 21.2 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc, I_O = 2.0 A; 24 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc, I_O = 3.0 A)	Reg_{line}	—	9.0	80	mV
Load Regulation (Note 3) (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, T_J = +25°C) (5.0 mA $\leqslant I_O \leqslant$ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, T_J = +25°C) (5.0 mA $\leqslant I_O \leqslant$ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 21.2 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc, I_O = 2.0 A; 5.0 mA $\leqslant I_O \leqslant$ 3.0 A)	ΔI_B	—	0.1	0.8	mA
Ripple Rejection (22 Vdc $\leqslant V_{in} \leqslant$ 32 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	54	64	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}-V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz $\leqslant$ f $\leqslant$ 100 kHz, T_J = +25°C)	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	—	1.0	2.0	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA) MC78T18 MC78T18C	TCV_O	 — —	 0.7 0.7	 3.6 —	mV/°C

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T24, C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 3.0 A, $T_J = T_{low}$ to T_{high} [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

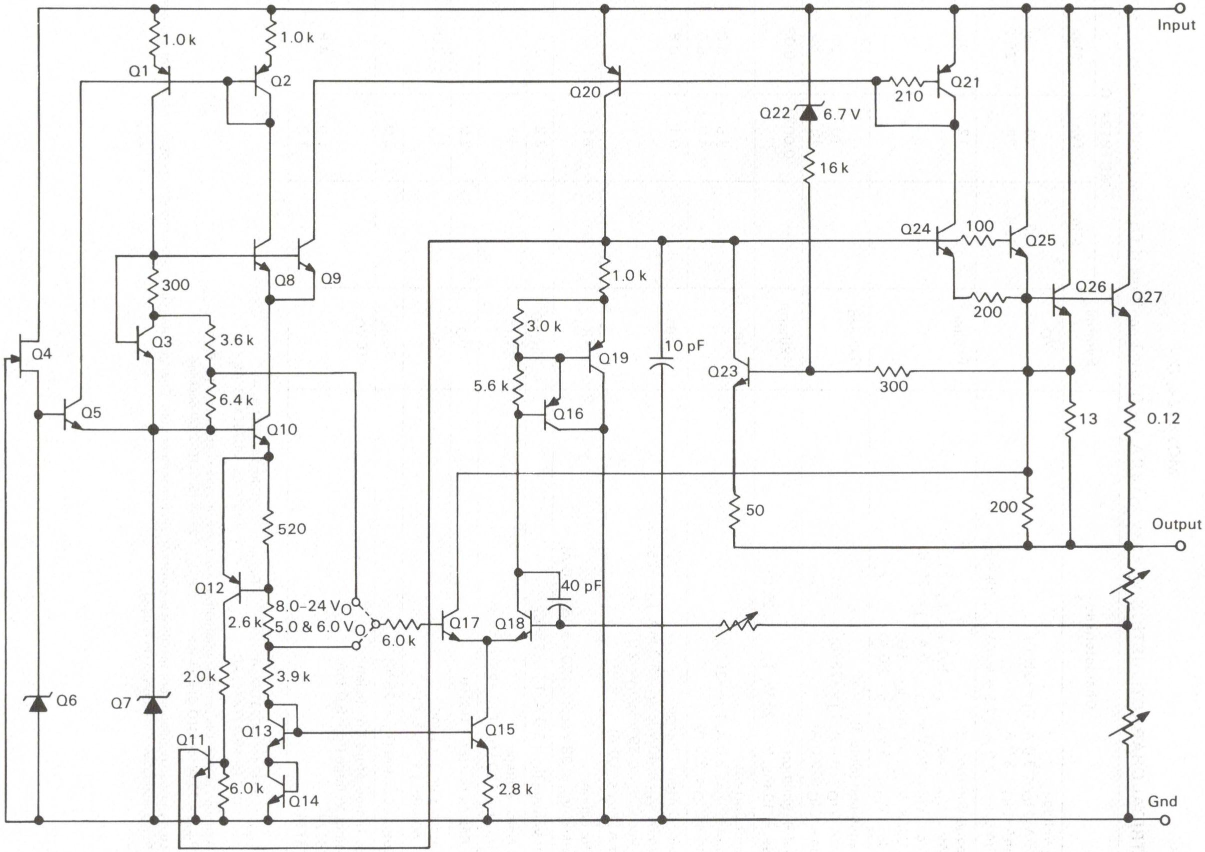
Characteristic	Symbol	MC78T24, C			Unit
		Min	Typ	Max	
Output Voltage (5.0 mA ⩽ I_O ⩽ 3.0 A, T_J = +25°C) (5.0 mA ⩽ I_O ⩽ 3.0 A; 5.0 mA ⩽ I_O ⩽ 2.0 A, 27.3 Vdc ⩽ V_{in} ⩽ 39 Vdc)	V_O	 23 22.8	 24 24	 25 25.2	Vdc
Line Regulation (Note 3) (27 Vdc ⩽ V_{in} ⩽ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 27 Vdc ⩽ V_{in} ⩽ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 27.5 Vdc ⩽ V_{in} ⩽ 39 Vdc, I_O = 2.0 A; 30 Vdc ⩽ V_{in} ⩽ 36 Vdc, I_O = 3.0 A)	Reg_{line}	—	12	90	mV
Load Regulation (Note 3) (5.0 mA ⩽ I_O ⩽ 3.0 A, T_J = +25°C) (5.0 mA ⩽ I_O ⩽ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	$\%V_O$/W
Quiescent Current (5.0 mA ⩽ I_O ⩽ 3.0 A, T_J = +25°C) (5.0 mA ⩽ I_O ⩽ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (27 Vdc ⩽ V_{in} ⩽ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 27.5 Vdc ⩽ V_{in} ⩽ 39 Vdc, I_O = 2.0 A; 5.0 mA ⩽ I_O ⩽ 3.0 A)	ΔI_B	—	0.1	0.8	mA
Ripple Rejection (28 Vdc ⩽ V_{in} ⩽ 38 Vdc, f = 120 Hz, I_O = 2.0 A)	RR	51	61	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}-V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ⩽ f ⩽ 100 kHz, T_J = +25°C)	V_n	—	10	—	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	—	1.0	2.0	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA) MC78T24 MC78T24C	TCV_O	 — —	 1.0 1.0	 4.8 —	mV/°C

Note 1. T_{low} = −55°C for MC78TXX, A T_{high} = +150°C for MC78TXX, A
= 0°C for MC78TXXC, AC = +125°C for MC78TXXC, AC

Note 2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
P_{max} = 30 W for K(TO-3) package P_{max} = 25 W for T(TO-220) package.

Note 3. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

SCHEMATIC DIAGRAM


Input
1.0 k
1.0 k
Q1
Q2
Q20
Q21
210
Q22
6.7 V
16 k
Q24
100
Q25
Q26
Q27
200
300
Q8
Q9
Q3
3.6 k
Q4
6.4 k
Q5
Q10
1.0 k
3.0 k
Q19
10 pF
Q23
300
5.6 k
Q16
13
0.12
520
50
200
Output
40 pF
Q12
8.0–24 V
2.6 k
5.0 & 6.0 V
6.0 k
Q17
Q18
2.0 k
3.9 k
Q6
Q7
Q13
Q15
Q11
6.0 k
Q14
2.8 k
Gnd

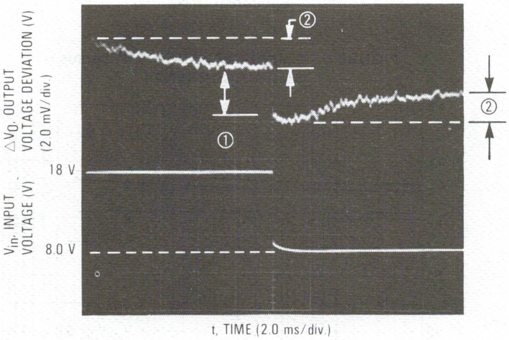
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100\ \mu s$) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

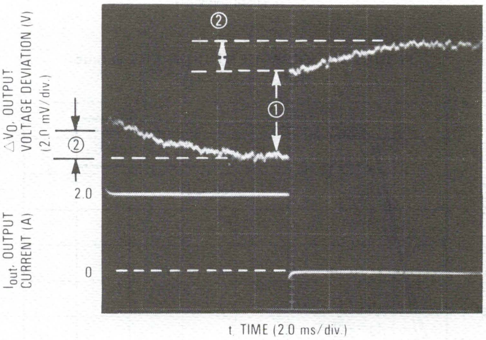
Figure 1 shows the line and thermal regulation response of a typical MC78T05A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



MC78T05A
$V_O = 5.0$ V
$V_{in} = 8.0\ V \rightarrow 18\ V \rightarrow 8.0\ V$ ① = $Reg_{line} = 2.4$ mV
$I_{out} = 2.0$ A ② = $Reg_{therm} = 0.0015\% V_O/W$

FIGURE 2 — LOAD AND THERMAL REGULATION



MC78T05A
$V_O = 5.0$ V
$V_{in} = 15$ ① = $Reg_{load} = 4.4$ mV
$I_{out} = 0\ A \rightarrow 2.0\ A \rightarrow 0\ A$ ② = $Reg_{therm} = 0.0015\% V_O/W$

FIGURE 3 — TEMPERATURE STABILITY

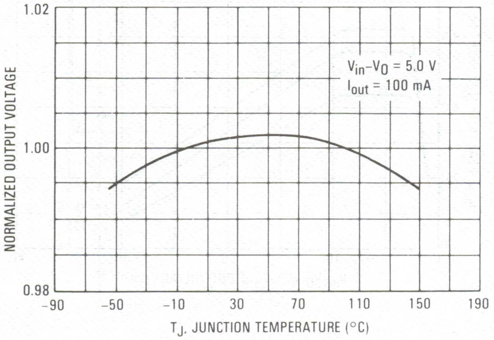


FIGURE 4 — OUTPUT IMPEDANCE

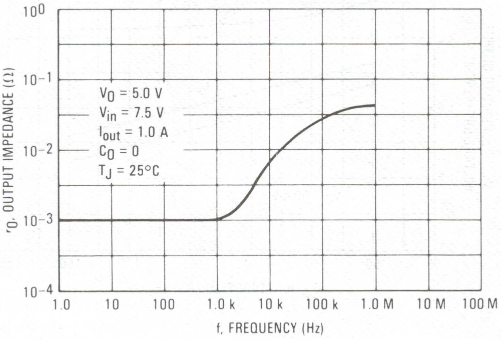


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

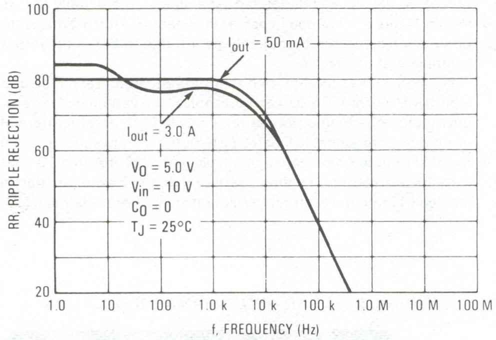


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

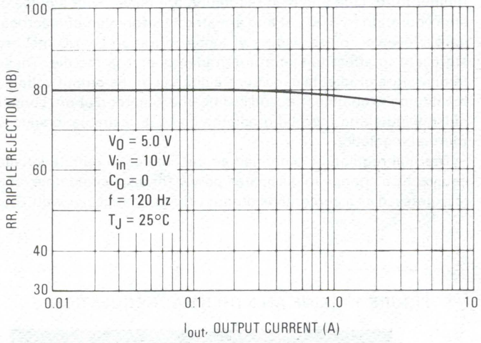


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

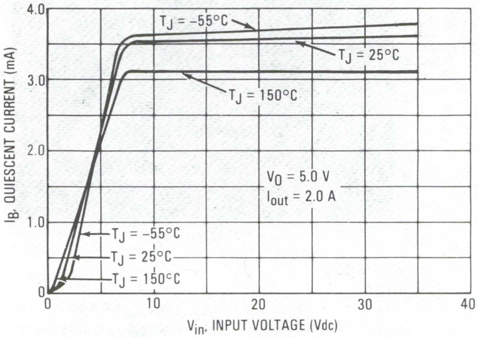


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

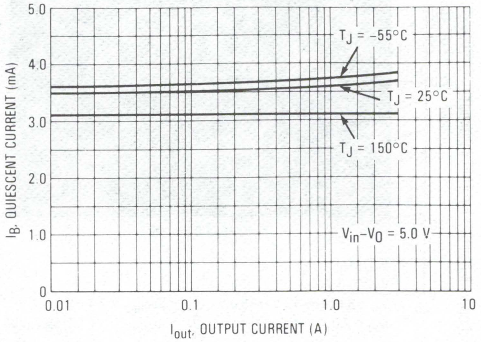


FIGURE 9 — DROPOUT VOLTAGE

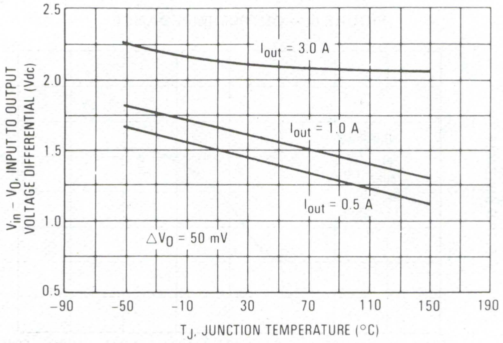


FIGURE 10 — PEAK OUTPUT CURRENT

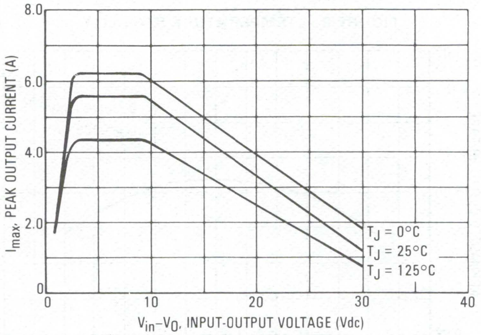


FIGURE 11 — LINE TRANSIENT RESPONSE

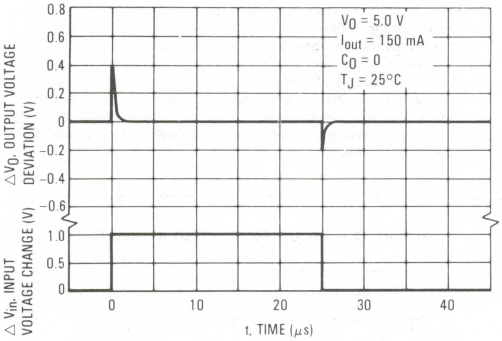


FIGURE 12 — LOAD TRANSIENT RESPONSE

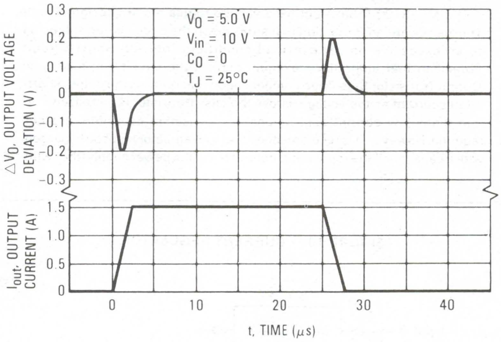


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00K, AK

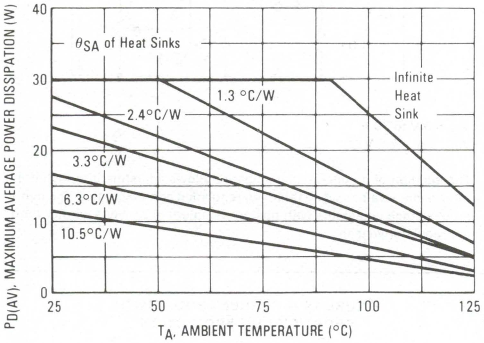


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CK, ACK

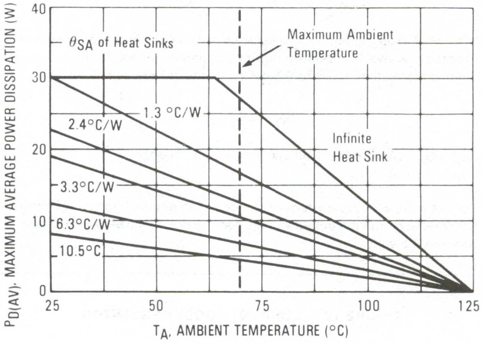
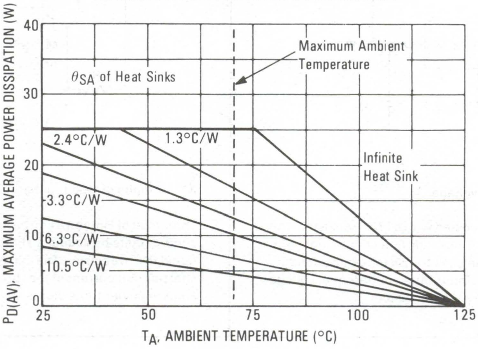


FIGURE 15 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CT, ACT



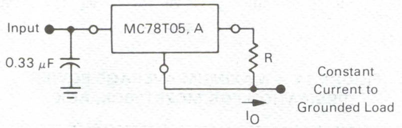
APPLICATIONS INFORMATION

Design Considerations

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 16 — CURRENT REGULATOR



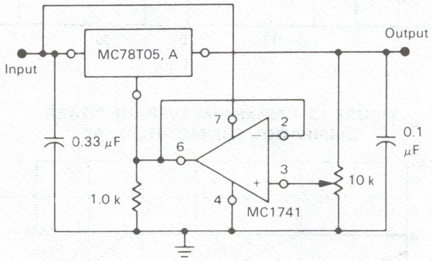
The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\text{ V}}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

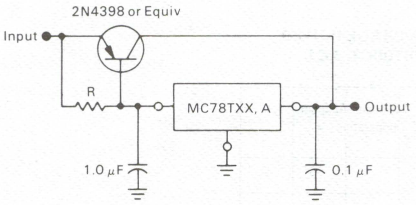
FIGURE 17 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in} - V_O \geqslant 2.5$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

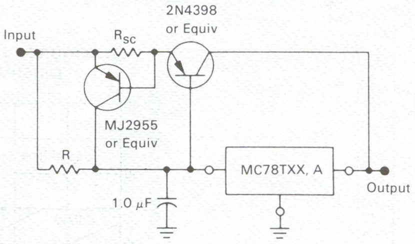
FIGURE 18 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78T00, A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

FIGURE 19 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 18 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

MOTOROLA

MC7900C Series

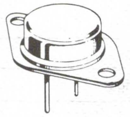
THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

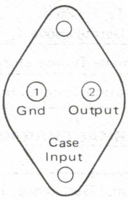
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from −2.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

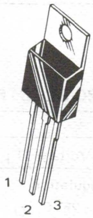


K SUFFIX
METAL PACKAGE
CASE 1
TO-3



(Bottom View)

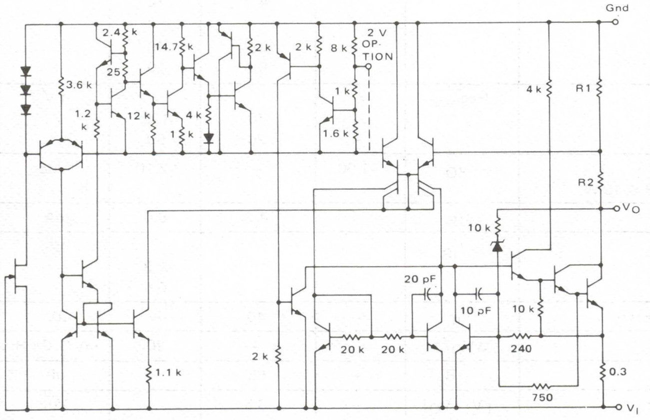
T SUFFIX
PLASTIC PACKAGE
CASE 221A
TO-220



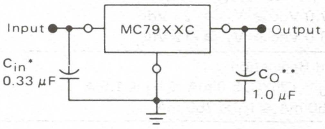
Pin 1. Ground
2. Input
3. Output

(Heatsink surface connected to Pin 2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C − 2.0 Volts	MC7906C − 6.0 Volts	MC7915C − 15 Volts
MC7905C − 5.0 Volts	MC7908C − 8.0 Volts	MC7918C − 18 Volts
MC7905.2C — 5.2 Volts	MC7912C − 12 Volts	MC7924C − 24 Volts

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	T_J = 0° C to +125°C	Metal Power
MC79XXCT	T_J = 0° C to +125°C	Plastic Power

XX indicates nominal voltage

MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_I	–35 –40	Vdc
Power Dissipation			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/R_{\theta JA}$	15.4	mW/°C
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +95°C (See Figure 1)	$1/R_{\theta JC}$	200	mW/°C
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/R_{\theta JA}$	28.6	mW/°C
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C	$1/R_{\theta JC}$	182	mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient – Plastic Package – Metal Package	$R_{\theta JA}$	65 35	°C/W
Thermal Resistance, Junction to Case – Plastic Package – Metal Package	$R_{\theta JC}$	5.0 5.5	°C/W

MC7902C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	8.0	20	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	4.0	10	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	18	40	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	8.0	20	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	70	120	
250 mA ≤ I_O ≤ 750 mA		–	20	60	
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-1.90	–	-2.10	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^{\circ}C < T_J < +125^{\circ}C$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^{\circ}C$)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation	Reg_{line}				mV
($T_J = +25^{\circ}C$, I_O = 100 mA)					
-7.0 Vdc $\geqslant V_I \geqslant$ -25 Vdc		–	7.0	50	
-8.0 Vdc $\geqslant V_I \geqslant$ -12 Vdc		–	2.0	25	
($T_J = +25^{\circ}C$, I_O = 500 mA)					
-7.0 Vdc $\geqslant V_I \geqslant$ -25 Vdc		–	35	100	
-8.0 Vdc $\geqslant V_I \geqslant$ -12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
$T_J = +25^{\circ}C$, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	11	100	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	4.0	50	
Output Voltage -7.0 Vdc $\geqslant V_I \geqslant$ -20 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-4.75	–	-5.25	Vdc
Input Bias Current ($T_J = +25^{\circ}C$)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.0 Vdc $\geqslant V_{in} \geqslant$ -25 Vdc		–	–	1.3	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^{\circ}C$, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	40	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^{\circ}C$	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^{\circ}C < T_J < +125^{\circ}C$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^{\circ}C$)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation	Reg_{line}				mV
($T_J = +25^{\circ}C$, I_O = 100 mA)					
-7.2 Vdc $\geqslant V_I \geqslant$ -25 Vdc		–	8.0	52	
-8.0 Vdc $\geqslant V_I \geqslant$ -12 Vdc		–	2.2	27	
($T_J = +25^{\circ}C$, I_O = 500 mA)					
-7.2 Vdc $\geqslant V_I \geqslant$ -25 Vdc		–	37	105	
-8.0 Vdc $\geqslant V_I \geqslant$ -12 Vdc		–	8.5	52	
Load Regulation	Reg_{load}				mV
$T_J = +25^{\circ}C$, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	12	105	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	4.5	52	
Output Voltage -7.2 Vdc $\geqslant V_I \geqslant$ -20 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-4.94	–	-5.46	Vdc
Input Bias Current ($T_J = +25^{\circ}C$)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.2 Vdc $\geqslant V_I \geqslant$ -25 Vdc		–	–	1.3	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^{\circ}C$, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	42	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^{\circ}C$	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^{\circ}C \leqslant T_A \leqslant +125^{\circ}C$	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-8.0 Vdc ⩾ V_I ⩾ -25 Vdc		–	9.0	60	
-9.0 Vdc ⩾ V_I ⩾ -13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
-8.0 Vdc ⩾ V_I ⩾ -25 Vdc		–	43	120	
-9.0 Vdc ⩾ V_I ⩾ -13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ⩽ I_O ⩽ 1.5 A		–	13	120	
250 mA ⩽ I_O ⩽ 750 mA		–	5.0	60	
Output Voltage -8.0 Vdc ⩾ V_I ⩾ -21 Vdc, 5.0 mA ⩽ I_O ⩽ 1.0 A, P ⩽ 15 W)	V_O	-5.7	–	-6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-8.0 Vdc ⩾ V_I ⩾ -25 Vdc		–	–	1.3	
5.0 mA ⩽ I_O ⩽ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_n	–	45	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ⩽ T_A ⩽ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-10.5 Vdc ⩾ V_I ⩾ -25 Vdc		–	12	80	
-11 Vdc ⩾ V_I ⩾ -17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
-10.5 Vdc ⩾ V_I ⩾ -25 Vdc		–	50	160	
-11 Vdc ⩾ V_I ⩾ -17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ⩽ I_O ⩽ 1.5 A		–	26	160	
250 mA ⩽ I_O ⩽ 750 mA		–	9.0	80	
Output Voltage -10.5 Vdc ⩾ V_I ⩾ -23 Vdc, 5.0 mA ⩽ I_O ⩽ 1.0 A, P ⩽ 15 W	V_O	-7.6	–	-8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-10.5 Vdc ⩾ V_I ⩾ -25 Vdc		–	–	1.0	
5.0 mA ⩽ I_O ⩽ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_n	–	52	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ⩽ T_A ⩽ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C $< T_J <$ +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	13	120	
-16 Vdc $\geqslant V_I \geqslant$ -22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	55	240	
-16 Vdc $\geqslant V_I \geqslant$ -22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	46	240	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	17	120	
Output Voltage -14.5 Vdc $\geqslant V_I \geqslant$ -27 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-11.4	–	-12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-14.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	75	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C $< T_J <$ +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	14	150	
-20 Vdc $\geqslant V_I \geqslant$ -26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	57	300	
-20 Vdc $\geqslant V_I \geqslant$ -26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	68	300	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	25	150	
Output Voltage -17.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-14.25	–	-15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	90	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C $\leqslant T_A \leqslant$ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation	Reg_{line}				mV
($T_J = +25^oC$, I_O = 100 mA)					
-21 Vdc $\geqslant V_I \geqslant$ -33 Vdc		–	25	180	
-24 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	10	90	
($T_J = +25^oC$, I_O = 500 mA)					
-21 Vdc $\geqslant V_I \geqslant$ -33 Vdc		–	90	360	
-24 Vdc $\geqslant V_I \geqslant$ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
$T_J = +25^oC$, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A		–	110	360	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	55	180	
Output Voltage -21 Vdc $\geqslant V_I \geqslant$ -33 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-17.1	–	-18.9	Vdc
Input Bias Current ($T_J = +25^oC$)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc $\geqslant V_I \geqslant$ -33 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 1.0 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	110	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^oC$	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \leqslant T_A \leqslant +125^oC$	$\Delta V_O/\Delta T$	–	-1.0	–	mV/^oC

MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^oC$)	V_O	-23	-24	-25	Vdc
Line Regulation	Reg_{line}				mV
($T_J = +25^oC$, I_O = 100 mA)					
-27 Vdc $\geqslant V_I \geqslant$ -38 Vdc		–	31	240	
-30 Vdc $\geqslant V_I \geqslant$ -36 Vdc		–	14	120	
($T_J = +25^oC$, I_O = 500 mA)					
-27 Vdc $\geqslant V_I \geqslant$ -38 Vdc		–	118	480	
-30 Vdc $\geqslant V_I \geqslant$ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
$T_J = +25^oC$, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A		–	150	480	
250 mA $\leqslant I_O \leqslant$ 750 mA		–	85	240	
Output Voltage -27 Vdc $\geqslant V_I \geqslant$ -38 Vdc, 5.0 mA $\leqslant I_O \leqslant$ 1.0 A, P $\leqslant$ 15 W	V_O	-22.8	–	-25.2	Vdc
Input Bias Current ($T_J = +25^oC$)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc $\geqslant V_I \geqslant$ -38 Vdc		–	–	1.0	
5.0 mA $\leqslant I_O \leqslant$ 1.0 A		–	–	0.5	
Output Noise Voltage ($T_A = +25^oC$, 10 Hz $\leqslant$ f $\leqslant$ 100 kHz)	V_n	–	170	–	µV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential I_O = 1.0 A, $T_J = +25^oC$	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, $0^oC \leqslant T_A \leqslant +125^oC$	$\Delta V_O/\Delta T$	–	-1.0	–	mV/^oC

TYPICAL CHARACTERISTICS

($T_A = +25^oC$ unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

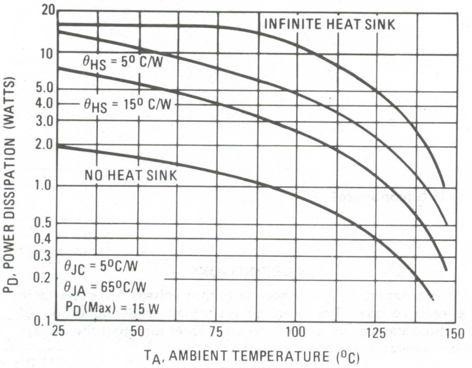


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

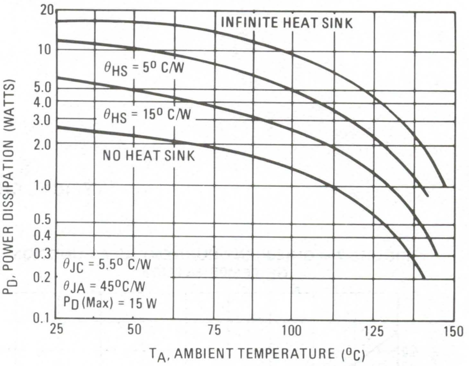


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

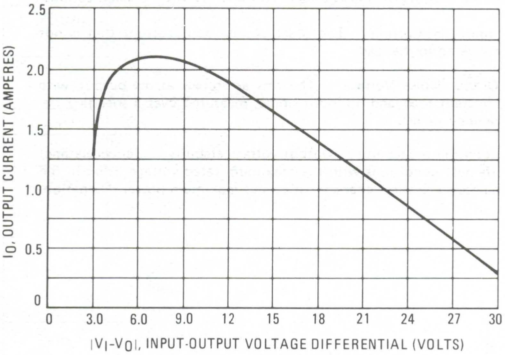


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

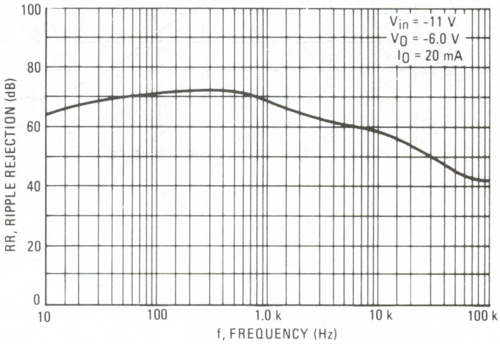


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

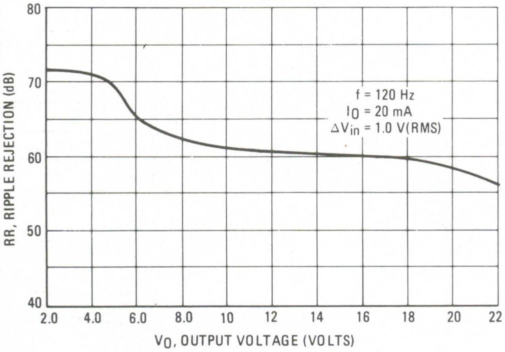
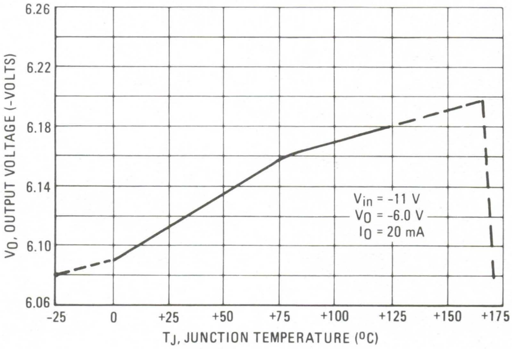
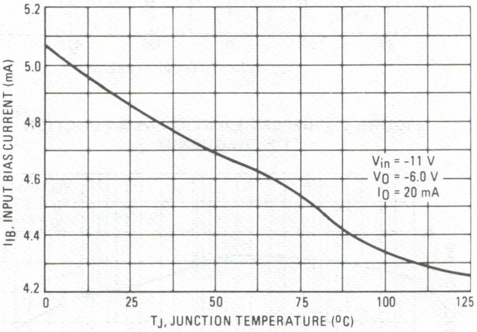


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

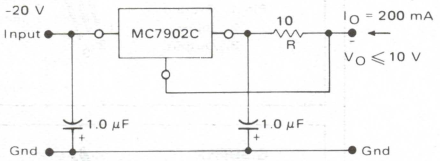
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR


-20 V
Input
MC7902C
10
R
I_O = 200 mA
$V_O \leqslant 10$ V
1.0 μF
+
1.0 μF
+
Gnd
Gnd

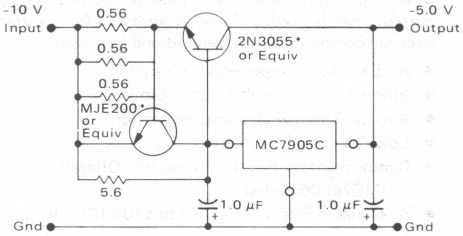
The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

FIGURE 9 – CURRENT BOOST REGULATOR

(-5.0 V @ 4.0 A, with 5.0 A current limiting)

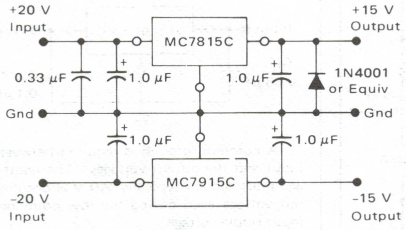

-10 V
Input
0.56
0.56
0.56
2N3055*
or Equiv
MJE200*
or
Equiv
MC7905C
5.6
1.0 μF
+
1.0 μF
+
-5.0 V
Output
Gnd
Gnd

*Mounted on common heat sink, Motorola MS-10 or equivalent.

When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY

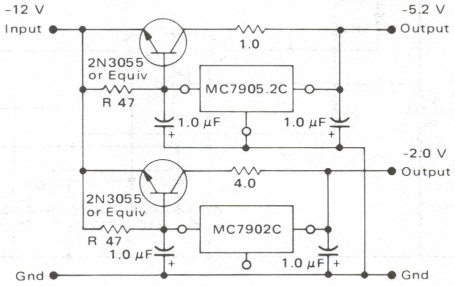
(±15 V @ 1.0 A)


+20 V
Input
MC7815C
+15 V
Output
0.33 μF
1.0 μF
+
1.0 μF
+
1N4001
or Equiv
Gnd
Gnd
1.0 μF
+
1.0 μF
+
MC7915C
-20 V
Input
-15 V
Output

The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY

(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)


-12 V
Input
1.0
-5.2 V
Output
2N3055
or Equiv
MC7905.2C
R 47
1.0 μF
+
1.0 μF
+
-2.0 V
Output
4.0
2N3055
or Equiv
MC7902C
R 47
1.0 μF
+
1.0 μF
+
Gnd
Gnd

When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

MC79L00C,AC Series

MOTOROLA

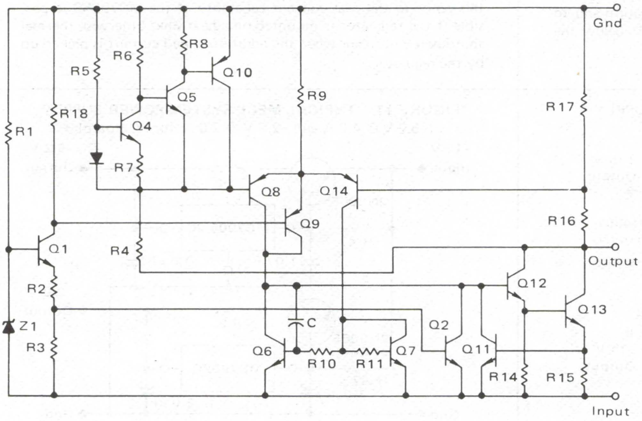
THREE-TERMINAL LOW CURRENT NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC

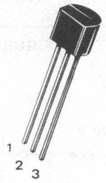


Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L03C	MC79L03AC	−3.0
MC79L05C	MC79L05AC	−5.0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

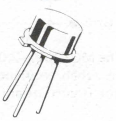
THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

P SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)

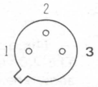
Pin 1. Ground
2. Input
3. Output



G SUFFIX
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)

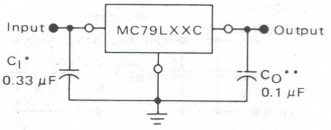


Pin 1. Ground
2. Output
3. Input



(Case connected to Pin 3) (Bottom View)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
MC79LXXACG	$T_J = 0^oC$ to $+125^oC$	Metal Can
MC79LXXACP	$T_J = 0^oC$ to $+125^oC$	Plastic Power
MC79LXXCG	$T_J = 0^oC$ to $+125^oC$	Metal Can
MC79LXXCP	$T_J = 0^oC$ to $+125^oC$	Plastic Power

XX indicates nominal voltage

MC79L00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-3,-5 V)	V_I	-30	Vdc
(-12,-15,-18 V)		-35	
(-24 V)		-40	
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

MC79L03C, AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L03C			MC79L03AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-2.76	-3.00	-3.24	-2.88	-3.0	-3.12	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-7.0 Vdc ⩾ V_I ⩾ -20 Vdc		–	–	80	–	–	60	
-8.0 Vdc ⩾ V_I ⩾ -20 Vdc		–	–	60	–	–	40	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ⩽ I_O ⩽ 100 mA		–	–	72	–	–	72	
1.0 mA ⩽ I_O ⩽ 40 mA		–	–	36	–	–	36	
Output Voltage	V_O							Vdc
-7.0 Vdc ⩾ V_I ⩾ -20 Vdc, 1.0 mA ⩽ I_O ⩽ 40 mA		-2.7	–	-3.3	-2.85	–	-3.15	
V_I = -10 Vdc, 1.0 mA ⩽ I_O ⩽ 70 mA		-2.7	–	-3.3	-2.85	–	-3.15	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
-8.0 Vdc ⩾ V_I ⩾ -20 Vdc		–	–	-1.5	–	–	-1.5	
1.0 mA ⩽ I_O ⩽ 40 mA		–	–	-0.2	–	–	-0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ⩽ f ⩽ 100 kHz)	V_n	–	30	–	–	30	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	10	–	–	10	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ⩾ V_I ⩾ -18 Vdc, f = 120 Hz, T_J = 25°C)	RR	44	51	–	45	51	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-7.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	200	–	–	150	
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	150	–	–	100	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	60	–	–	60	
1.0 mA ≤ I_O ≤ 40 mA		–	–	30	–	–	30	
Output Voltage	V_O							Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-4.5	–	-5.5	-4.75	–	-5.25	
V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-4.5	–	-5.5	-4.75	–	-5.25	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 kHz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-14.5 Vdc ≥ V_I ≥ -27 Vdc		–	–	250	–	–	250	
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	200	–	–	200	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	100	–	–	100	
1.0 mA ≤ I_O ≤ 40 mA		–	–	50	–	–	50	
Output Voltage	V_O							Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-10.8	–	-13.2	-11.4	–	-12.6	
V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-10.8	–	-13.2	-11.4	–	-12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	300	—	—	300	
-20 Vdc ≥ V_I ≥ -30 Vdc		—	—	250	—	—	250	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		—	—	150	—	—	150	
1.0 mA ≤ I_O ≤ 40 mA		—	—	75	—	—	75	
Output Voltage	V_O							Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-13.5	—	-16.5	-14.25	—	-15.75	
V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-13.5	—	-16.5	-14.25	—	-15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		—	—	6.5	—	—	6.5	
(T_J = +125°C)		—	—	6.0	—	—	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-20 Vdc ≥ V_I ≥ -30 Vdc		—	—	1.5	—	—	1.5	
1.0 mA ≤ I_O ≤ 40 mA		—	—	0.2	—	—	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	—	90	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	30	—	—	30	—	mV/1.0 k Hrs.
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	—	34	39	—	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\|V_I - V_O\|$	—	1.7	—	—	1.7	—	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-20.7 Vdc ≥ V_I ≥ -33 Vdc		—	—	—	—	—	325	
-21.4 Vdc ≥ V_I ≥ -33 Vdc		—	—	325	—	—	—	
-22 Vdc ≥ V_I ≥ -33 Vdc		--	—	275	—	—	—	
-21 Vdc ≥ V_I ≥ -33 Vdc		—	—	—	—	—	275	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		--	—	170	—	—	170	
1.0 mA ≤ I_O ≤ 40 mA		—	—	85	—	—	85	
Output Voltage	V_O							Vdc
-20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		—	—	—	-17.1	—	-18.9	
-21.4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-16.2	—	-19.8	—	—	—	
V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-16.2	—	-19.8	-17.1	—	-18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		—	—	6.5	—	—	6.5	
(T_J = +125°C)		—	—	6.0	—	—	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-21 Vdc ≥ V_I ≥ -33 Vdc		—	—	—	—	—	1.5	
-27 Vdc ≥ V_I ≥ -33 Vdc		—	—	1.5	—	—	—	
1.0 mA ≤ I_O ≤ 40 mA		—	—	0.2	—	—	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	150	—	—	150	—	µV
Long-Term Stability	$\Delta V_O/\Delta t$	—	45	—	—	45	—	mV/1.0 k Hrs.
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	—	33	48	—	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\|V_I - V_O\|$	—	1.7	—	—	1.7	—	Vdc

MC79L24C, AC ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L24C Min	MC79L24C Typ	MC79L24C Max	MC79L24AC Min	MC79L24AC Typ	MC79L24AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-27 Vdc ≥ V_I ≥ -38 V		–	–	–	–	–	350	
-27.5 Vdc ≥ V_I ≥ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ≥ V_I ≥ -38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-22.8	–	-25.2	
-28 Vdc ≥ V_I ≥ -38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-21.4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (-29 ≤ V_I ≤ -35 Vdc, f = 120 Hz, T_J = 25°C)	RR	30	43	–	31	47	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$\|V_I - V_O\|$	–	1.7	–	–	1.7	–	Vdc

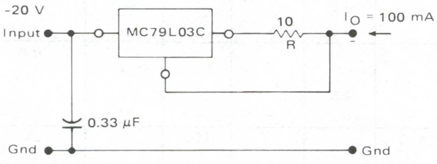
APPLICATIONS INFORMATION

Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR

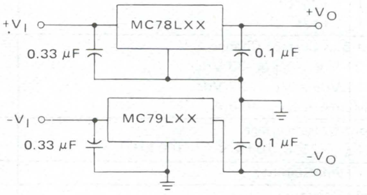


The MC79L03, -3.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{3\text{ V}}{R} + I_B$$

The quiescent current for this regulator is typically 3.8 mA. The -3.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

FIGURE 8 – POSITIVE AND NEGATIVE REGULATOR



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

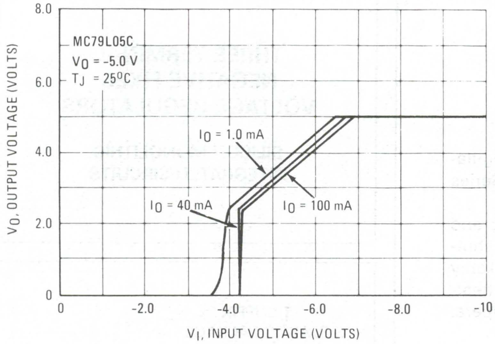


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

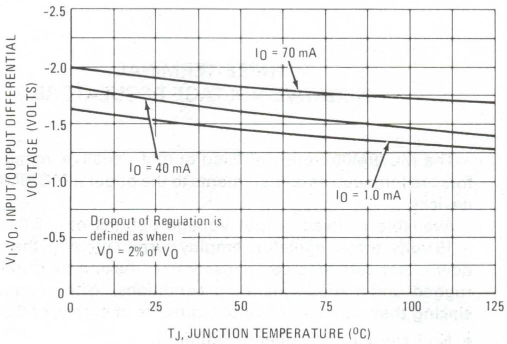


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

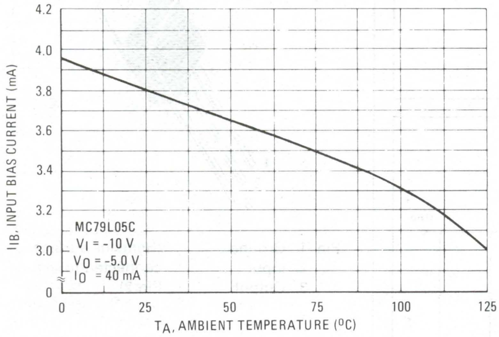


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

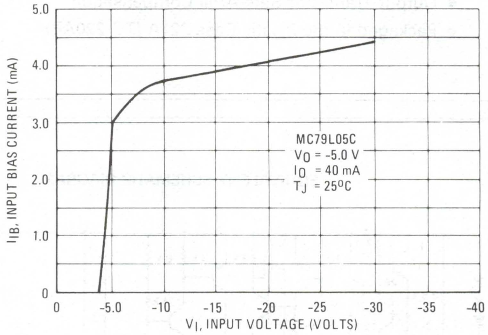


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

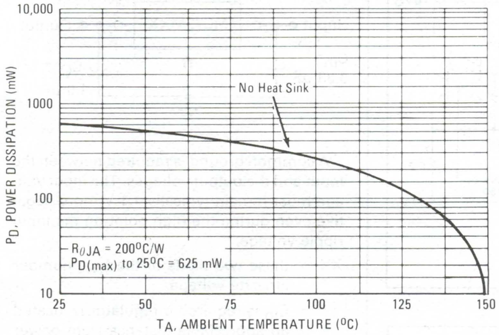
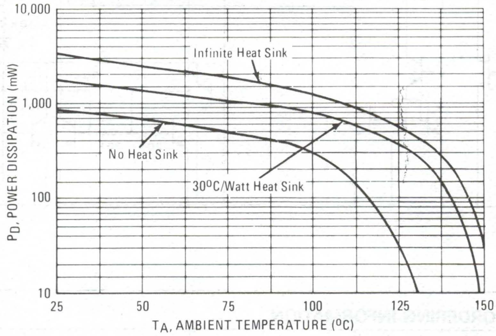


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



MC79M00
Series

MOTOROLA

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

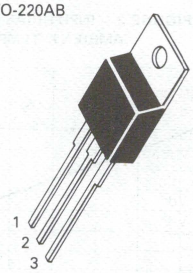
Available in fixed output voltage options of −5.0, −12 and −15 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A (TO-220AB)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

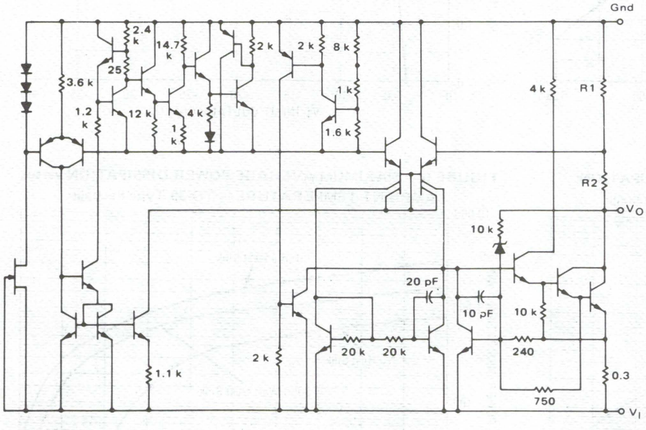
SILICON MONOLITHIC INTEGRATED CIRCUITS

T SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB

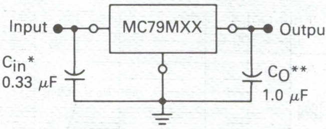


Pin 1. Ground 2. Input 3. Output	(Heatsink surface connected to Pin 2)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage	Operating Junction Temperature Range	Package
MC79M05CT	−5.0 Volts	0°C to +125°C	Plastic Power
MC79M12CT	−12 Volts		
MC79M15CT	−15 Volts		

MC79MXX Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	−35	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C	 P_D $1/R\theta_{JA}$ P_D $1/R\theta_{JC}$	 Internally Limited 14.2 Internally Limited 200	 Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	65	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	5.0	°C/W

MC79M05C ELECTRICAL CHARACTERISTICS (V_I = −10 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−4.8	−5.0	−5.2	Vdc
Line Regulation (T_J = +25°C) (Note 1) −7.0 Vdc ≥ V_I ≥ −25 Vdc −8.0 Vdc ≥ V_I ≥ −18 Vdc	Reg_{line}	 — —	 7.0 2.0	 50 30	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	100	mV
Output Voltage −7.0 Vdc ≥ V_I ≥ −25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−4.75	—	−5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change −8.0 Vdc ≥ V_I ≥ −25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −10 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	µV
Ripple Rejection (f = 120 Hz)	RR	54	66	—	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$\|V_I\text{-}V_O\|$	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	0.2	—	mV/°C

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC79M12C ELECTRICAL CHARACTERISTICS (V_I = −19 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−11.5	−12	−12.5	Vdc
Line Regulation (T_J = +25°C) (Note 1) −14.5 Vdc ≥ V_I ≥ −30 Vdc −15 Vdc ≥ V_I ≥ −25 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −14.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−11.4	—	−12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −14.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −19 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$\lvert V_I\text{-}V_O\rvert$	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−0.8	—	mV/°C

MC79M15C ELECTRICAL CHARACTERISTICS (V_I = −23 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−14.4	−15	−15.6	Vdc
Line Regulation (T_J = +25°) (Note 1) −17.5 Vdc ≥ V_I ≥ −30 Vdc −18 Vdc ≥ V_I ≥ −28 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −17.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−14.25	—	−15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −17.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −23 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	$\lvert V_I\text{-}V_O\rvert$	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MOTOROLA

MC34060
MC35060

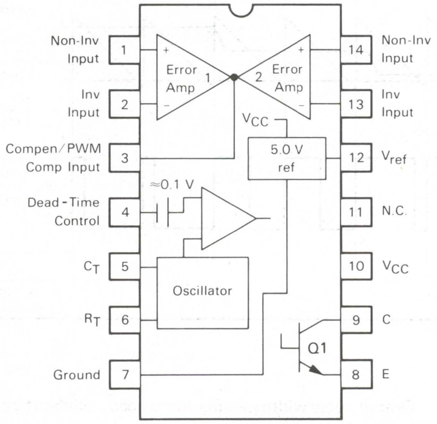
Specifications and Applications Information

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060 and MC34060 are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink

PIN CONNECTIONS



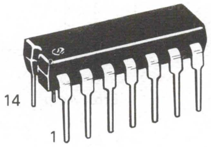
Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead-Time Control 4
C_T 5
R_T 6
Ground 7
14 Non-Inv Input
13 Inv Input
12 V_{ref}
11 N.C.
10 V_{CC}
9 C
8 E
Error Amp 1
Error Amp 2
+
−
V_{CC}
5.0 V ref
≈0.1 V
Oscillator
Q1

(Top View)

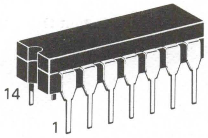
The MC34060 is specified over the commercial operating range of 0°C to +70°C. The MC35060 is specified over the full military range of -55 to +125°C.

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC34060 only)



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060L	-55 to +125°C	Ceramic DIP
MC34060P	0 to +70°C	Plastic DIP
MC34060L	0 to +70°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

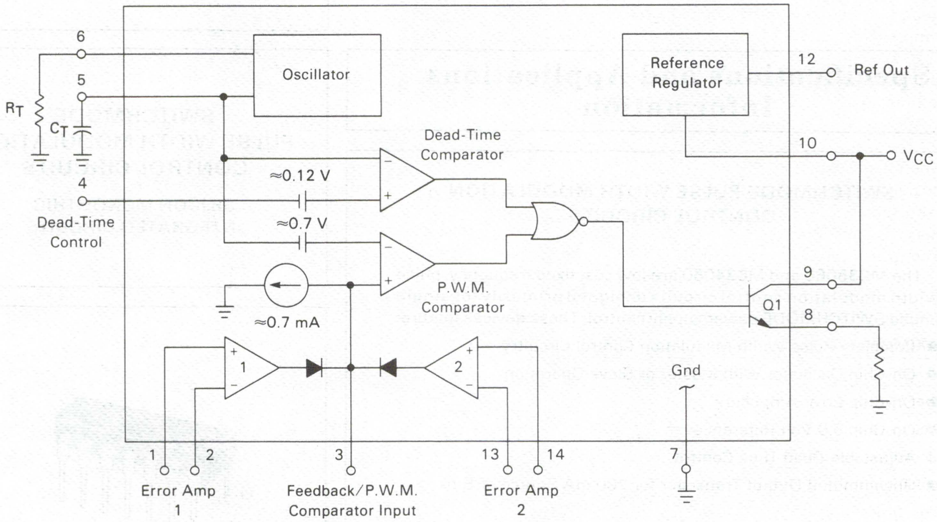
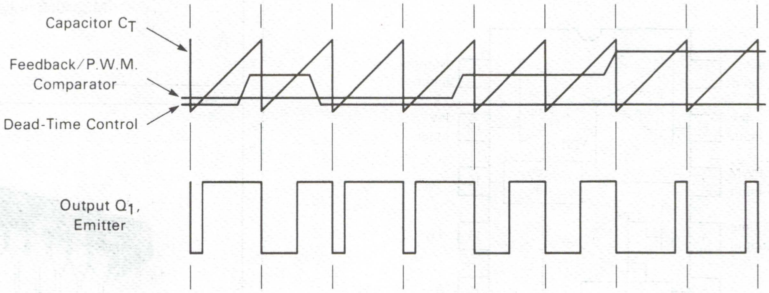

6
5
4
R_T
C_T
Dead-Time Control
Oscillator
Reference Regulator
12
Ref Out
10
V_{CC}
Dead-Time Comparator
≈0.12 V
≈0.7 V
≈0.7 mA
P.W.M. Comparator
9
Q1
8
1
2
Gnd
1
2
3
13
14
7
Error Amp 1
Feedback/P.W.M. Comparator Input
Error Amp 2

FIGURE 2 — TIMING DIAGRAM


Capacitor C_T
Feedback/P.W.M. Comparator
Dead-Time Control
Output Q_1, Emitter

Description

The MC35060/34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to $(V_{CC} - 2\ V)$, and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060/34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a thermal drift of less than 50 mV over an operating temperature range of 0 to +70°C.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060	MC34060	Unit
Power Supply Voltage	V_{CC}	42	42	V
Collector Output Voltage	V_C	42	42	V
Collector Output Current	I_C	250	250	mA
Amplifier Input Voltage	V_{in}	$V_{CC} + 0.3$	$V_{CC} + 0.3$	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	mW
Operating Junction Temperature	T_J	150	150	°C
Operating Ambient Temperature Range	T_A	−55 to 125	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to 150	−65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	°C/W
Power Derating Factor	$1/R_{\theta JA}$	10	12.5	mW/°C
Derating Ambient Temperature	T_A	50	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	$V_{CC} - 2.0$	V
Current Into Feedback Terminal	$I_{f.b.}$	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, f_{osc} = 25 kHz unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Characteristic	Symbol	MC35060			MC34060			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Reference Voltage Change with Temperature (ΔT_A = Min to Max)	$V_{ref(\Delta T)}$	—	0.2	2.0	—	1.3	2.6	%
Input Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Output Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V, T_A = 25°C)	I_{SC}	10	35	50	—	35	—	mA
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−150	—	—	−100	μA
Collector-Emitter Saturation Voltage Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.5	—	1.1	1.3	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Voltage Rise time (T_A = 25°C)	t_r							ns
Common-Emitter (See Figure 12)		—	100	200	—	100	200	
Emitter-Follower (See Figure 13)		—	100	200	—	100	200	
Output Voltage Fall Time (T_A = 25°C)	t_f							ns
Common-Emitter (See Figure 12)		—	25	100	—	25	100	
Emitter-Follower (See Figure 13)		—	40	100	—	40	100	

Characteristic	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	0.1	1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 7.0 V to 40 V)	V_{ICR}	-0.3	—	V_{CC}-2.0	V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, f_{osc} = 25 kHz unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Characteristic	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency (V_O = 0.5, to 3.5 V, R_L = 2.0 kΩ)	f_c	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O+	−2.0	−4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB(DT)}$	—	−2.0	−10	μA
Maximum Output Duty Cycle	DC_{max}				%
(V_{in} = 0 V, C_T = 0.1 μF, R_T = 12 kΩ)		90	96	100	
(V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)		—	92	100	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		—	2.8	3.3	
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 47 kΩ)	f_{osc}	—	25	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency Change with Temperature (ΔT_A = T_{Alow} to T_{Ahigh})	$\Delta f_{osc}(\Delta T)$	—	±1.0	±2.0	%
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open)	I_{CC}				mA
(V_{CC} = 15 V)		—	5.5	10	
(V_{CC} = 40 V)		—	7.0	15	
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\dfrac{\sum\limits_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

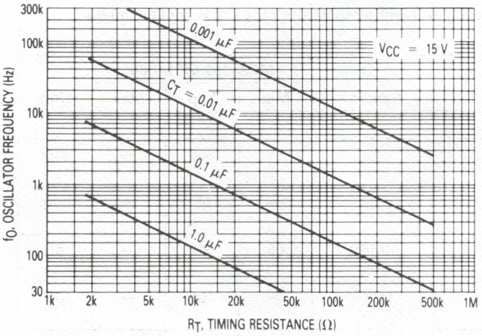


FIGURE 4 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

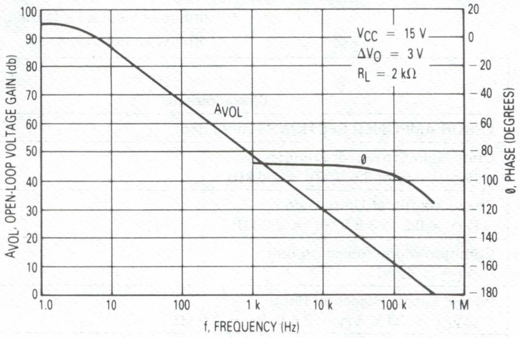


FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

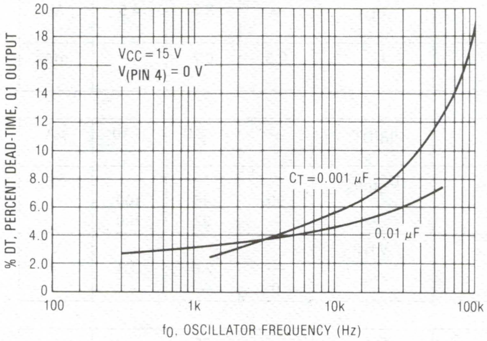


FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

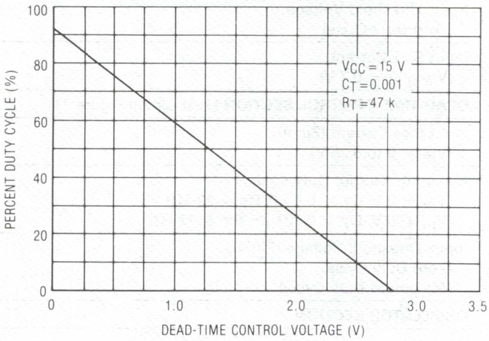


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT

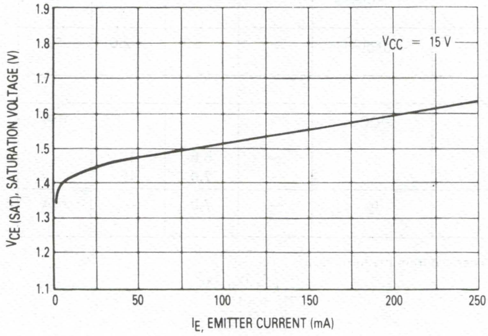


FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT

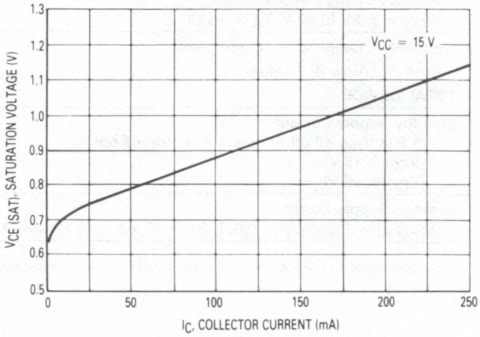


FIGURE 9 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

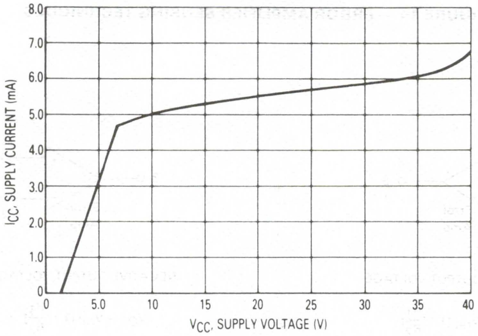


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

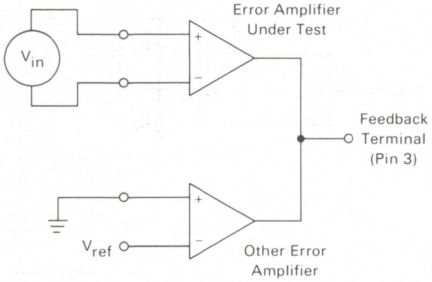

V_{in}
+
−
Error Amplifier
Under Test
Feedback
Terminal
(Pin 3)
+
−
V_{ref}
Other Error
Amplifier

FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

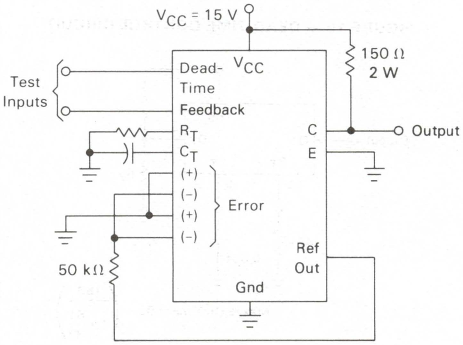

V_{CC} = 15 V
150 Ω
2 W
Test
Inputs
Dead-
Time
V_{CC}
Feedback
R_T
C_T
C
E
Output
(+)
(−)
(+)
(−)
Error
50 kΩ
Ref
Out
Gnd

FIGURE 12 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

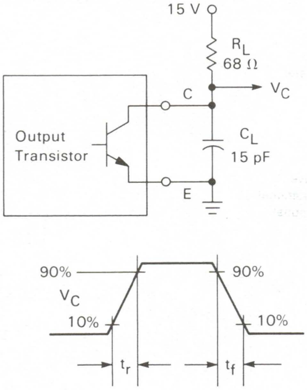

15 V
R_L
68 Ω
V_C
Output
Transistor
C
C_L
15 pF
E
90%
V_C
10%
90%
10%
t_r
t_f

FIGURE 13 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

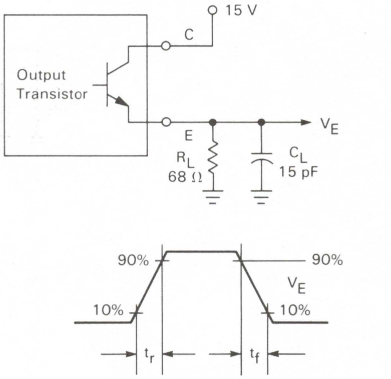
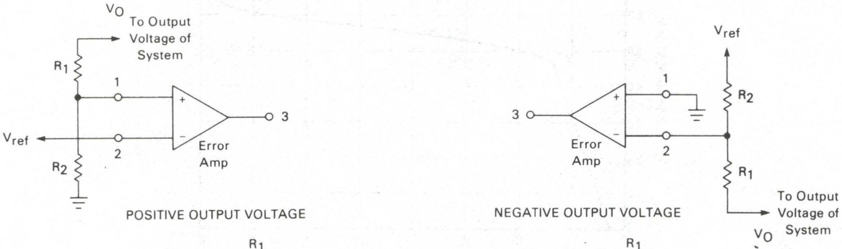

15 V
C
Output
Transistor
V_E
E
R_L
68 Ω
C_L
15 pF
90%
90%
V_E
10%
10%
t_r
t_f

FIGURE 14 — ERROR AMPLIFIER SENSING TECHNIQUES



V_O
To Output Voltage of System
R_1
1
2
V_{ref}
R_2
+
−
3
Error Amp
V_{ref}
R_2
1
2
3
Error Amp
R_1
To Output Voltage of System
V_O

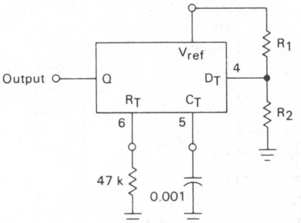
POSITIVE OUTPUT VOLTAGE

$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$

NEGATIVE OUTPUT VOLTAGE

$V_O = -V_{ref}\left(1 + \frac{R_1}{R_2}\right)$

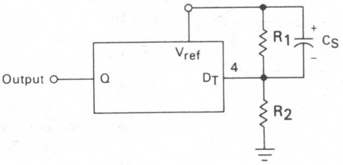
FIGURE 15 — DEAD-TIME CONTROL CIRCUIT



Output
Q
V_{ref}
D_T
4
R_1
R_2
R_T
C_T
6
5
47 k
0.001

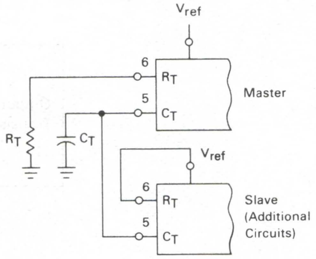
$$\text{Max \% On Time} \approx 92 - \left(\frac{160}{1 + \frac{R1}{R2}}\right)$$

FIGURE 16 — SOFT-START CIRCUIT



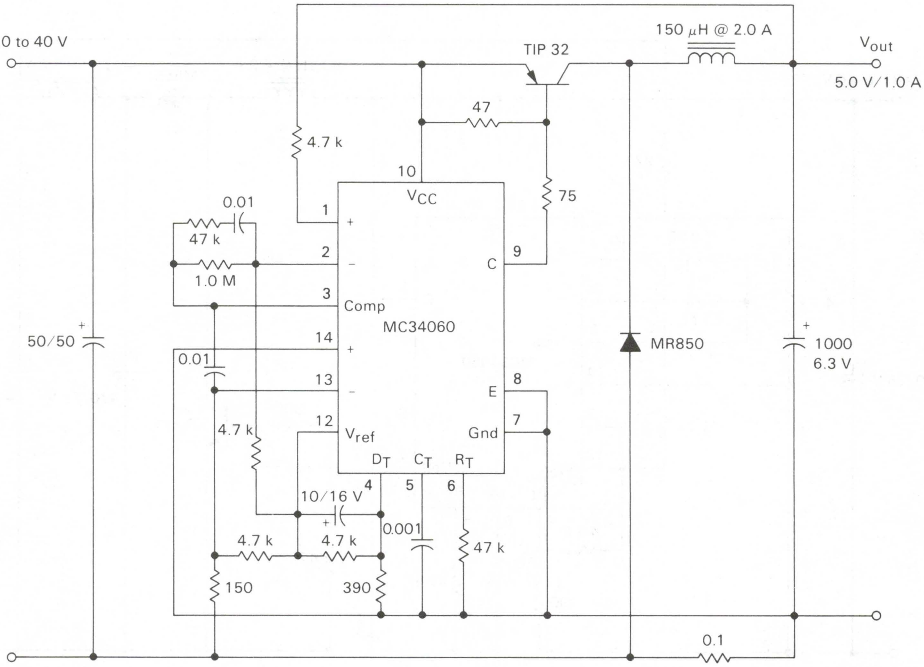
Output
Q
V_{ref}
D_T
4
R_1
C_S
+
−
R_2

FIGURE 17 — SLAVING TWO OR MORE CONTROL CIRCUITS



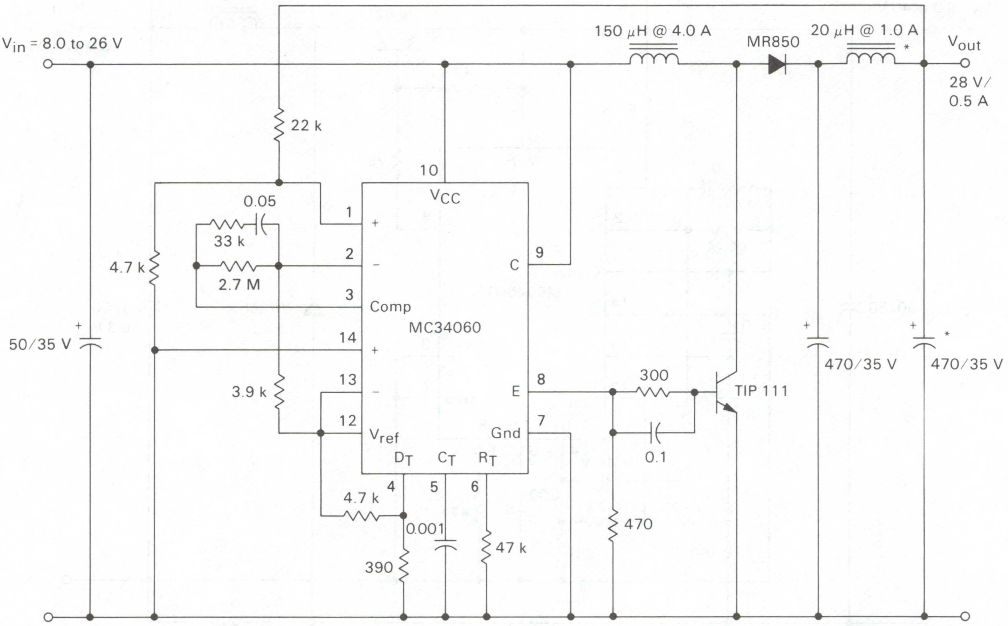
V_{ref}
6
R_T
5
C_T
Master
R_T
C_T
V_{ref}
6
R_T
5
C_T
Slave (Additional Circuits)

FIGURE 18 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING


V_{in} = 8.0 to 40 V
TIP 32
150 µH @ 2.0 A
V_{out}
5.0 V/1.0 A
47
4.7 k
10
V_{CC}
75
0.01
47 k
1.0 M
1
2
3
Comp
MC34060
C
9
50/50
14
0.01
13
4.7 k
12
V_{ref}
E
8
Gnd
7
D_T
C_T
R_T
4
5
6
10/16 V
0.001
47 k
4.7 k
4.7 k
150
390
MR850
1000
6.3 V
0.1

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

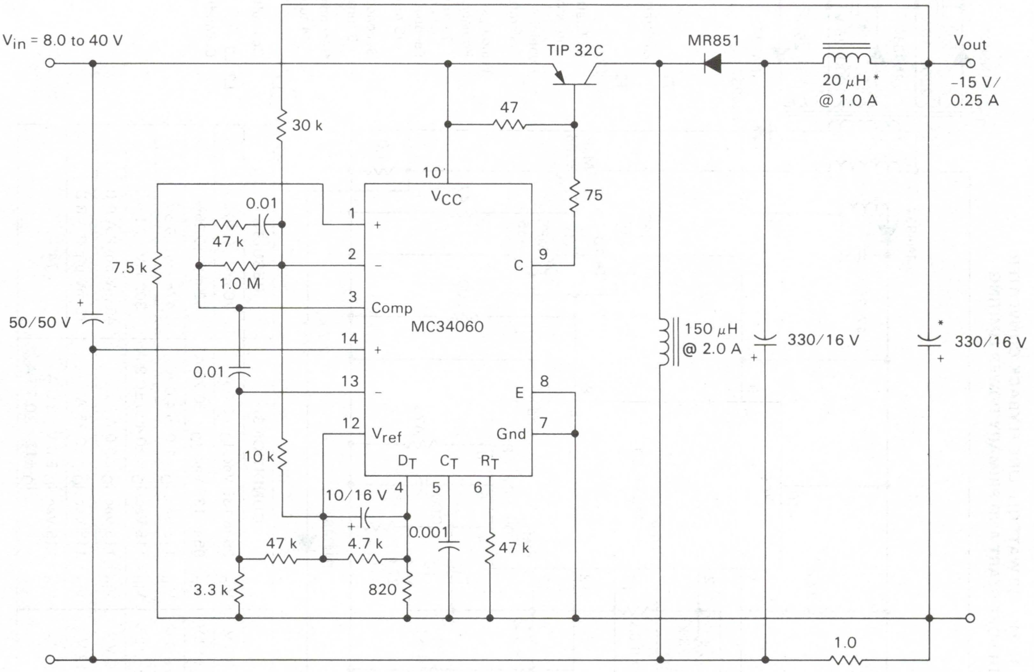
FIGURE 19 — STEP-UP CONVERTER


Vin = 8.0 to 26 V
150 μH @ 4.0 A
MR850
20 μH @ 1.0 A
*
Vout
28 V/
0.5 A
22 k
10
VCC
0.05
33 k
1
+
2
−
9
C
4.7 k
2.7 M
3
Comp
MC34060
50/35 V
+
14
+
13
−
8
E
300
TIP 111
3.9 k
12
Vref
7
Gnd
0.1
DT
CT
RT
4
5
6
4.7 k
0.001
47 k
470
390
+
470/35 V
+
470/35 V
*

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

*Optional circuit to minimize output ripple.

FIGURE 20 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING

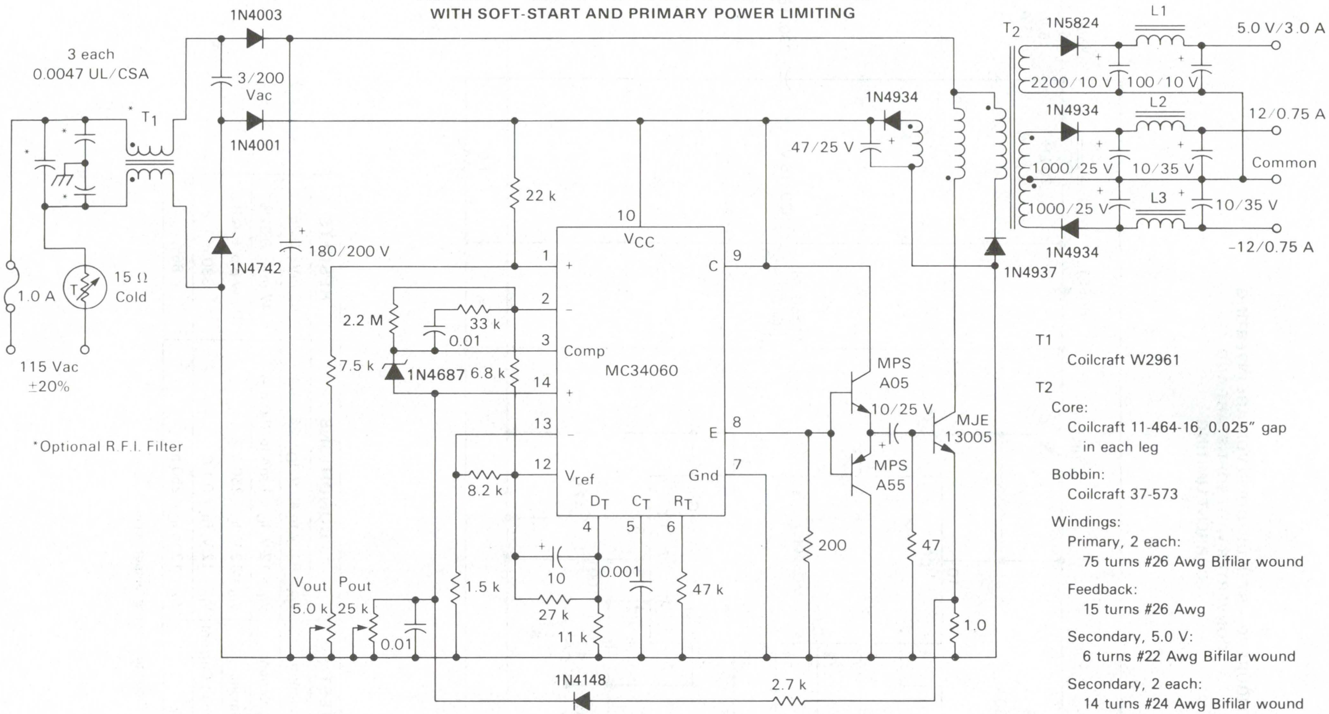


V_{in} = 8.0 to 40 V
TIP 32C
MR851
V_{out}
-15 V/ 0.25 A
20 µH * @ 1.0 A
47
30 k
10
V_{CC}
75
0.01
47 k
1.0 M
7.5 k
1
2
3
14
13
12
+
−
Comp
MC34060
C
9
E
8
Gnd
7
V_{ref}
D_T
C_T
R_T
4
5
6
50/50 V
0.01
10 k
10/16 V
0.001
47 k
4.7 k
47 k
3.3 k
820
150 µH @ 2.0 A
330/16 V
330/16 V
1.0

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p.p. P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

*Optional circuit to minimize output ripple.

FIGURE 21 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING


3 each
0.0047 UL/CSA
*T1
*
*
*
1.0 A
15 Ω Cold
115 Vac ±20%
*Optional R.F.I. Filter
1N4003
3/200 Vac
1N4001
1N4742
180/200 V
22 k
10
VCC
MC34060
1
2
3
14
13
12
9
8
7
4
5
6
C
E
Gnd
Comp
Vref
DT
CT
RT
2.2 M
33 k
0.01
7.5 k
1N4687
6.8 k
8.2 k
1.5 k
10
0.001
47 k
27 k
11 k
Vout 5.0 k
Pout 25 k
0.01
1N4148
2.7 k
1N4934
47/25 V
MPS A05
10/25 V
MPS A55
MJE 13005
200
47
1.0
1N4937
T2
1N5824
L1
2200/10 V
100/10 V
5.0 V/3.0 A
1N4934
L2
1000/25 V
10/35 V
12/0.75 A
Common
1000/25 V
L3
10/35 V
1N4934
-12/0.75 A

T1
Coilcraft W2961

T2
Core:
Coilcraft 11-464-16, 0.025″ gap in each leg

Bobbin:
Coilcraft 37-573

Windings:
Primary, 2 each:
75 turns #26 Awg Bifilar wound

Feedback:
15 turns #26 Awg

Secondary, 5.0 V:
6 turns #22 Awg Bifilar wound

Secondary, 2 each:
14 turns #24 Awg Bifilar wound

L1
Coilcraft Z7156, 15 μH @ 5.0 A

L2, L3
Coilcraft Z7157, 25 μH @ 1.0 A

TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 = ±0.75 A	74%

MOTOROLA

MC34061, MC34061A
MC35061, MC35061A

Advance Information

THREE-TERMINAL OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34061/35061 overvoltage protection (OVP) circuits, in combination with two external programming resistors and a "crowbar" SCR, protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar", or short circuit, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

These three-terminal circuits provide a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061/35061 eliminates trip voltage and temperature drift errors due to SCR gate variations.

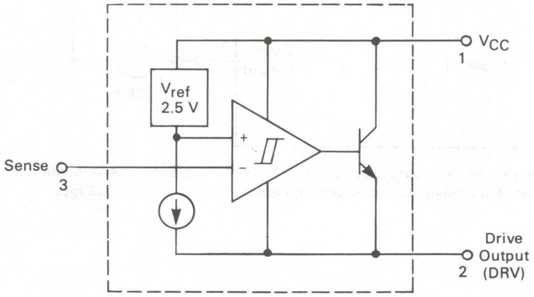
The basic MC34061/35061 devices offer a ±2% tolerance on the sense trip voltage. The A-suffix devices have a ±1% sense trip voltage specification and other key parameters have tightened limits. The series is available in a low-cost plastic TO-92 package, dual-in-line plastic or ceramic packages, and feature:

- Unique Three-Terminal Design
- SCR Gate Drive Output of 200 mA
- Sense Voltage of 2.5 V ±1% or ±2%
- Hysteresis of 250 mV
- Wide Supply Range: $4.0\ V \leqslant V_{CC} \leqslant 41\ V$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature Range MC34061, MC34061A MC35061, MC35061A	T_A	 0 to +70 −55 to +125	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

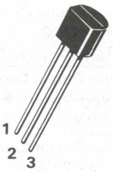
FUNCTIONAL BLOCK DIAGRAM



THREE-TERMINAL PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

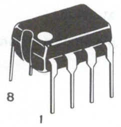
SILICON MONOLITHIC INTEGRATED CIRCUIT

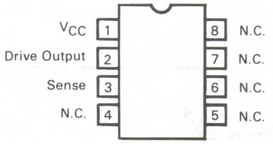
P SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)
(MC34061,A only)



Pin 1. V_{CC}
2. Drive Output
3. Sense

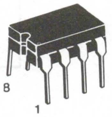
P1 SUFFIX
PLASTIC DUAL-IN-LINE PACKAGE
CASE 626-04
(MC34061,A only)





(Top View)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



ORDERING INFORMATION

Device	Temperature Range	Package
MC35061U, AU	−55 to +125°C	Ceramic DIP
MC34061P, AP	0 to +70°C	Plastic TO-92
MC34061P1, AP1		Plastic DIP
MC34061U, AU		Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC}–V_{DRV} = 5.0 V; T_A = T_{low} to T_{high} [see Note 1] unless otherwise specified)

Characteristic	Symbol	MC35061A/34061A			MC35061/34061			Unit
		Min	Typ	Max	Min	Typ	Max	
Operating Voltage Range	V_{CC}–V_{DRV}	3.0	—	40	3.0	—	40	Vdc
Sense Trip Voltage	V_{Sense}							Vdc
T_A = 25°C		2.475	2.5	2.525	2.45	2.5	2.55	
T_{low} to T_{high} (Note 1)		2.45	2.5	2.55	2.4	2.5	2.6	
Line Regulation, V_{Sense} (3.0 ≤ V_{CC} –V_{DRV} ≤ 40 V)	Reg_{line}							%/V
T_A = 25°C		—	0.001	0.005	—	0.001	0.01	
T_{low} to T_{high} (Note 1)		—	0.001	0.01	—	0.001	0.02	
Input Bias Current, Sense Pin	I_{IB}							μA
At Trip Point (Note 2)		—	0.3	1.0	—	0.3	2.0	
After Trip (V_{Sense} = 3.0 V)		—	0.9	3.0	—	0.9	6.0	
Hysteresis Voltage, Sense Pin	V_H	—	250	—	—	250	—	mV
Drive Output Current, ON State	$I_{DRV(on)}$							mA
T_J = 25°C		170	200	300	120	200	300	
T_{low} to T_{high} (Note 1)		100	200	350	80	200	350	
Drive Output Current, OFF State	$I_{DRV(off)}$							mA
V_{CC}–V_{DRV} = 5.0 V		0.2	0.6	1.0	0.2	0.6	1.0	
3.0 V ≤ V_{CC} –V_{DRV} ≤ 40 V		0.2	0.6	1.5	0.2	0.6	1.5	
Drive Output Current Slew Rate T_A = 25°C	di/dt	—	2.0	—	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC}–V_{DRV} = 0 V to 15 V at dV/dt = 200 V/μs; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C) 500 mV Overdrive	t_{PLH}	—	500	—	—	500	—	ns

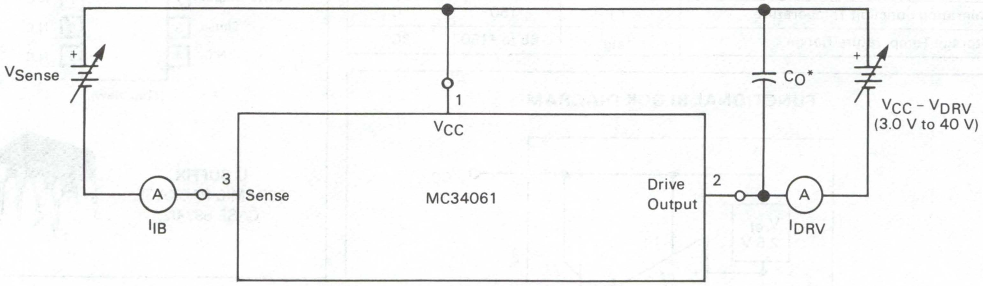
NOTES:

(1) T_{low} = –55°C for MC35061, MC35061A
= 0°C for MC34061, MC34061A

T_{high} = +125°C for MC35061, MC35061A
= +70°C for MC34061, MC34061A

(2) This specification is an engineering estimate based on design parameters, and is not tested.

FIGURE 1 — STANDARD TEST CIRCUIT



*A 1.0 μF tantalum or 10 μF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

FIGURE 2 — DRIVE CURRENT versus SENSE VOLTAGE

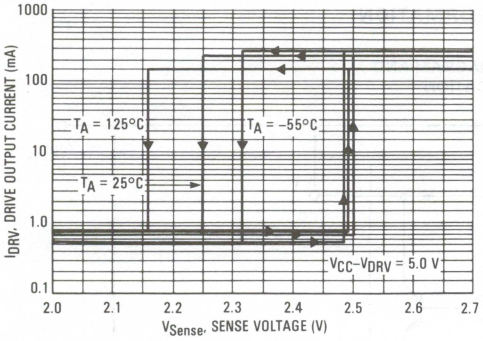


FIGURE 3 — SENSE TRIP VOLTAGE versus TEMPERATURE

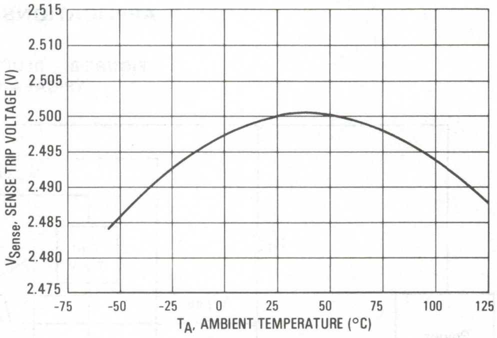


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

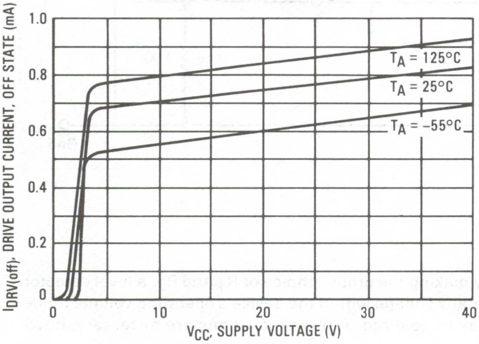


FIGURE 5 — INPUT BIAS CURRENT versus SENSE VOLTAGE

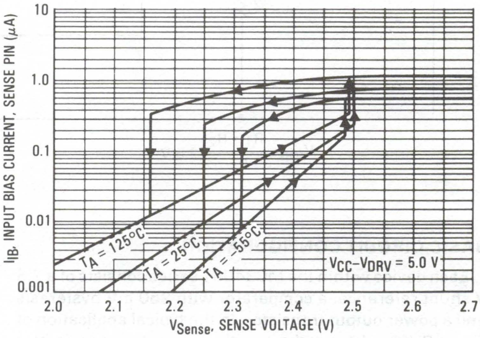


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME

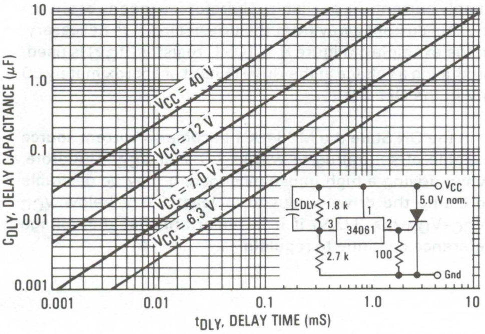
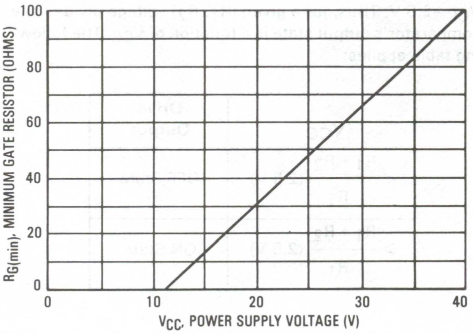
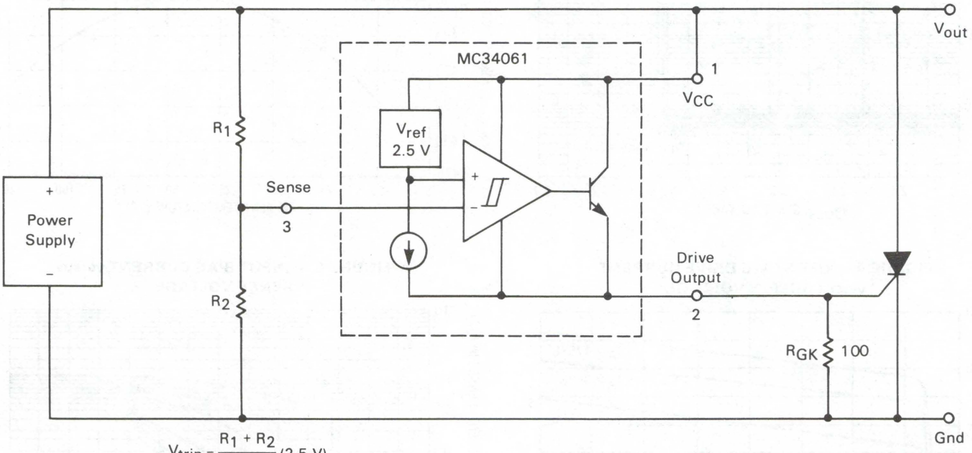


FIGURE 7 — MINIMUM R_G versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — BLOCK DIAGRAM AND TYPICAL APPLICATION



$$V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$$

BASIC CIRCUIT CONFIGURATION

Each device within the MC34061 series consists of a 2.5 V shunt reference, a comparator with 250 mV hysteresis and a power output transistor. In the typical application of Figure 8, the voltage at the inverting input of the comparator is $\frac{V_{CC}\ R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is V_{CC} −2.5 V. Thus, for a given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

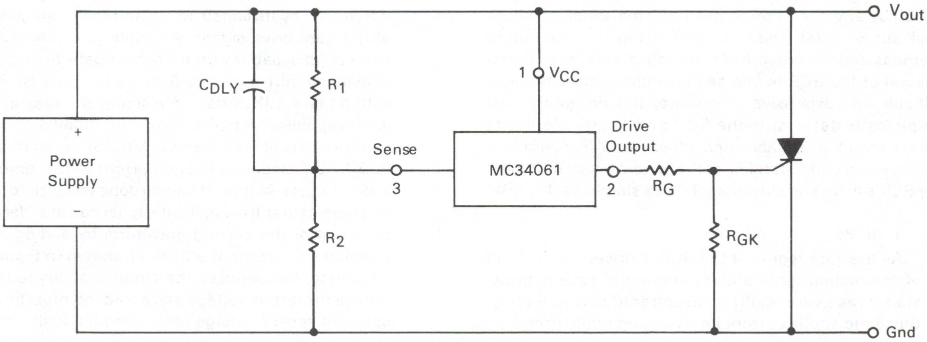
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage within the device's operating voltage range may be realized. A few precautions are necessary, however.

Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 8, a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34061 becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} (V_{CC}–$V_{DRV} \geqslant$ 3.0 V) if it is important that the voltage reference continue to regulate.

FIGURE 9 — OVERVOLTAGE PROTECTION WITH TIME DELAY



PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34061/35061 series to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 9. The time delay obtained by this technique is a function of R_1, R_2, and C_{DLY} as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltaged supply voltage, V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, $V_{ref} = 2.5$ V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, t_{DLY}, is:

$$t_{DLY} = \frac{R_1R_2C_{DLY}}{R_1 + R_2}\ \ln\left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}}\right]$$

where:

$$V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$$

Figure 6 shows the C_{DLY} values versus delay time (t_{DLY}) for a typical 5.0 V power supply protection circuit. The figure also shows the change in t_{DLY} with variations in the overvoltaged supply, V_{CC}. In this example $R_1 = 1.8$ k, $R_2 = 2.7$ k, $V_{CC(nom)} = 5.0$ V, and $V_{trip} = 6.25$ V.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34061/35061 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 7 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 10, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 10A, the supply's input filter capacitors. This surge current is illustrated in Figure 11, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

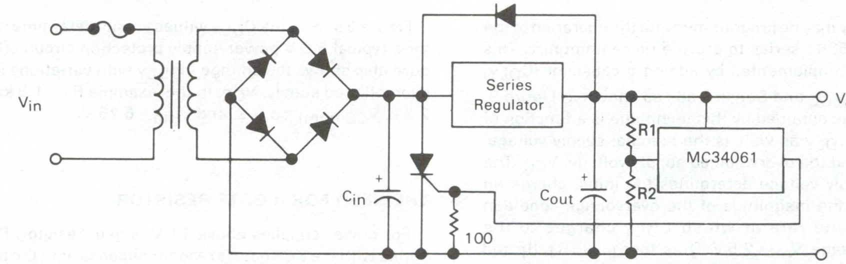
1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

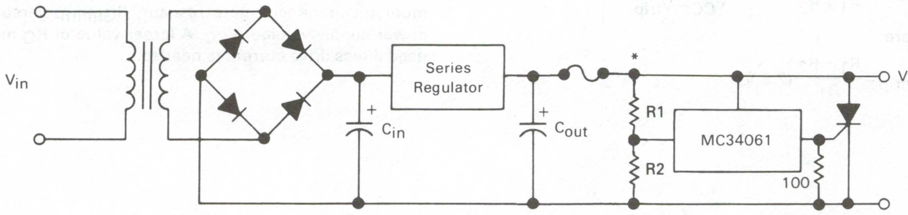
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 12. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 10 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

10A — SCR ACROSS INPUT OF REGULATOR

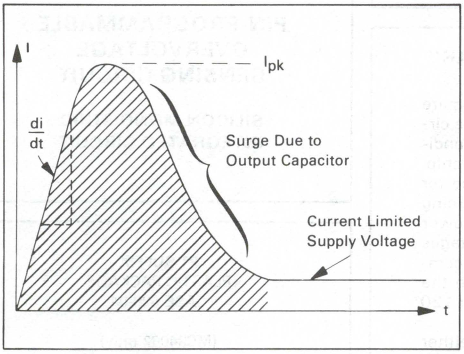


10B — SCR ACROSS OUTPUT OF REGULATOR



* Needed if supply not current limited

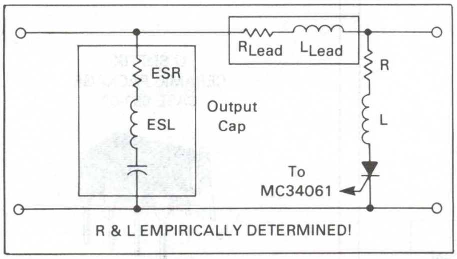
FIGURE 11 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 12) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 12 — CIRCUIT ELEMENTS AFFECTING SCR SURGE AND di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 10A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 10B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

MC34062
MC35062

MOTOROLA

Advance Information

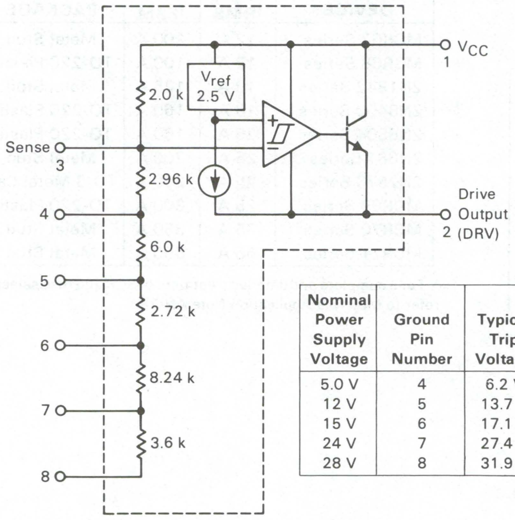
PIN-PROGRAMMABLE OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34062/35062 overvoltage protection (OVP) circuits require only an external "crowbar" SCR to protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar", or short circuit, the supply. An on-chip, tapped resistor network allows the device to be programmed for trip voltages ranging from 3.5 to 40 V. Each of the five programming pins provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. Many other trip voltages may be programmed by interconnecting and grounding various combinations of these programming pins. Tables are provided in the Applications Information which show connection schemes for 120 trip voltages.

These circuits provide a cost-effective means of protecting either positive or negative power supplies. In addition, an external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity. The unique design of the MC34062/35062 eliminates voltage and temperature drift errors due to SCR gate variations.

- Unique Pin-Programmable Trip Voltage from 3.5 to 40 V
- One-Pin Programming for 5.0, 12, 15, 24 and 28 V Power Supplies
- SCR Gate Drive Output of 200 mA
- Built-In Hysteresis Voltage
- Wide Supply Range: 4.0 V ≤ V_{CC} ≤ 40 V

FUNCTIONAL BLOCK DIAGRAM



Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

Pins 4 through 8 are used to program the Trip Voltage, V_{trip}

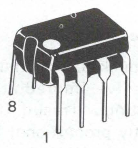
This document contains information on a new product. Specifications and information herein are subject to change without notice.

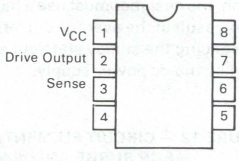
PIN-PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

(MC34062 only)

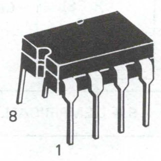




Note: Pins 4 thru 8 are used to program the Trip Voltage, V_{trip}

(Top View)

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



ORDERING INFORMATION

Device	Temperature Range	Package
MC35062U	-55 to +125°C	Ceramic DIP
MC34062P1	0 to +70°C	Plastic DIP
MC34062U		Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Voltage Across Any Internal Resistor In Network	V_{RN}	40	Vdc
Current Through Any Resistor In Network	I_{RN}	10	mA
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature	T_A		°C
MC34062		0 to +70	
MC35062		−55 to +125	
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150°C	°C

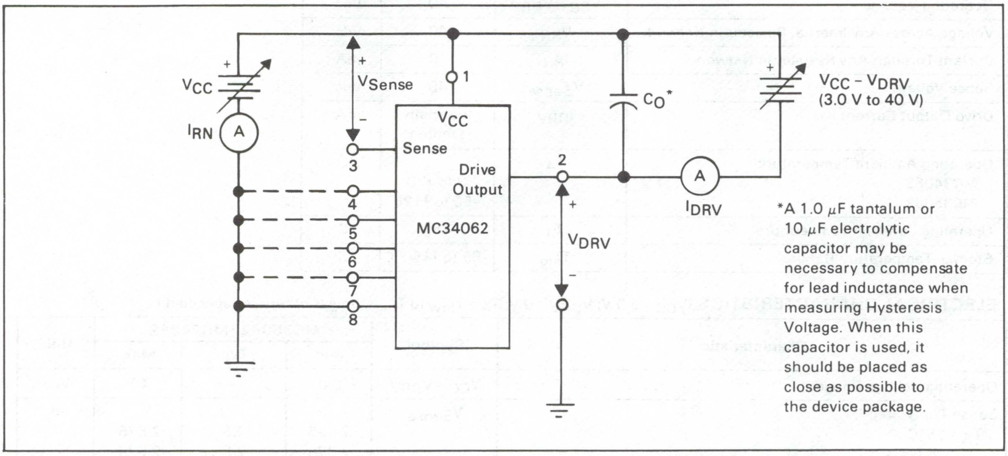
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; V_{DRV} = 0 V; $T_A = T_{low}$ to T_{high} unless otherwise specified.)

Characteristic	Symbol	MC35062/MC34062			Unit
		Min	Typ	Max	
Operating Voltage Range	$V_{CC} - V_{DRV}$	3.0	—	40	Vdc
Sense Trip Voltage	V_{Sense}				Vdc
T_A = 25°C		2.425	2.5	2.575	
T_{low} to T_{high}		2.375	2.5	2.625	
Line Regulation, V_{Sense} ($3.0\ V \leqslant V_{CC} - V_{DRV} \leqslant 40\ V$)	Reg_{line}				%/V
T_A = 25°C		—	0.001	0.01	
T_{low} to T_{high}		—	0.001	0.02	
Trip Voltage (Pin 4 = Gnd; V_{DRV} = 0 V)	$V_{trip(4)}$				V
T_A = 25°C		6.01	6.2	6.39	
T_{low} to T_{high}		5.89	6.2	6.51	
Hysteresis Voltage (Pin 4 = Gnd; V_{DRV} = 0 V)	$V_{H(4)}$	—	0.62	—	V
Trip Voltage (Pin 5 = Gnd; V_{DRV} = 0 V)	$V_{trip(5)}$				V
T_A = 25°C		13.3	13.7	14.1	
T_{low} to T_{high}		13.0	13.7	14.4	
Hysteresis Voltage (Pin 5 = Gnd; V_{DRV} = 0 V)	$V_{H(5)}$	—	1.37	—	V
Trip Voltage (Pin 6 = Gnd; V_{DRV} = 0 V)	$V_{trip(6)}$				V
T_A = 25°C		16.6	17.1	17.6	
T_{low} to T_{high}		16.2	17.1	18.0	
Hysteresis Voltage (Pin 6 = Gnd; V_{DRV} = 0 V)	$V_{H(6)}$	—	1.71	—	V
Trip Voltage (Pin 7 = Gnd; V_{DRV} = 0 V)	$V_{trip(7)}$				V
T_A = 25°C		26.6	27.4	28.2	
T_{low} to T_{high}		26.0	27.4	28.8	
Hysteresis Voltage (Pin 7 = Gnd; V_{DRV} = 0 V)	$V_{H(7)}$	—	2.74	—	V
Trip Voltage (Pin 8 = Gnd; V_{DRV} = 0 V)	$V_{trip(8)}$				V
T_A = 25°C		30.9	31.9	32.9	
T_{low} to T_{high}		30.3	31.9	33.5	
Hysteresis Voltage (Pin 8 = Gnd; V_{DRV} = 0 V)	$V_{H(8)}$	—	3.19	—	V
Resistor Network Current at Nominal Power Supply Voltage V_{CC} = 28 V; V_{DRV} = 0 V; Pin 8 = Gnd	I_{RN}	0.5	1.1	2.0	mA
Drive Output Current, ON State	$I_{DRV(on)}$				mA
T_J = 25°C		170	200	300	
T_{low} to T_{high}		100	200	350	
Drive Output Current, OFF State	$I_{DRV(off)}$				mA
V_{CC} = 5.0 V; V_{DRV} = 0 V		0.2	0.6	1.0	
$3.0\ V \leqslant V_{CC} - V_{DRV} \leqslant 40\ V$		0.2	0.6	1.5	
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; V_{DRV} = 0 V; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C; 500 mV Overdrive)	t_{PLH}	—	500	—	ns

T_{low} = −55°C for MC35062
= 0°C for MC34062

T_{high} = +125°C for MC35062
= + 70°C for MC34062

FIGURE 1 — STANDARD TEST CIRCUIT


VCC
+
IRN
A
+
VSense
–
1
VCC
3
Sense
Drive
Output
2
4
5
6
7
8
MC34062
+
VDRV
–
CO*
+
VCC - VDRV
(3.0 V to 40 V)
A
IDRV

*A 1.0 µF tantalum or 10 µF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

FIGURE 2 — DRIVE CURRENT versus NORMALIZED RESISTOR DIVIDER VOLTAGE (Normalized to V_{trip} at T_A = 25°C)

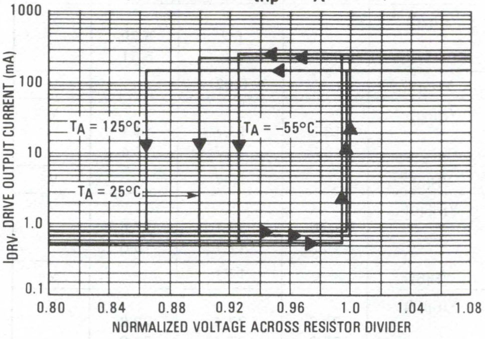


FIGURE 3 — NORMALIZED TRIP VOLTAGE versus TEMPERATURE (Normalized to T_A = 25°C)

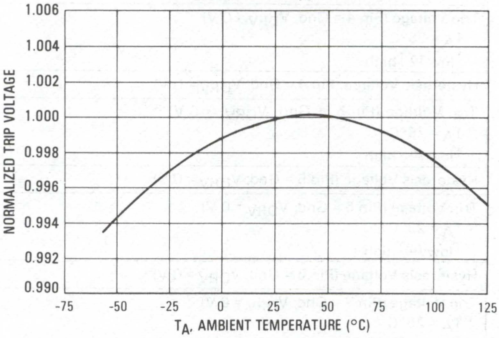


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

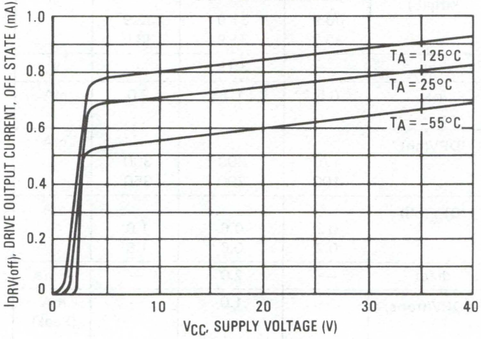


FIGURE 5 — MINIMUM R_G versus SUPPLY VOLTAGE

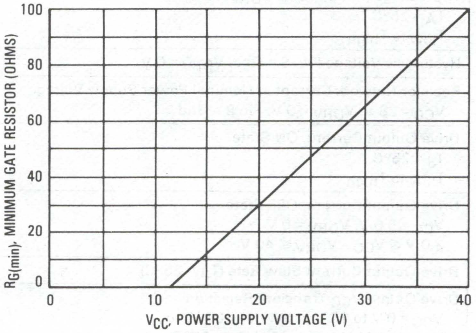


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 5.0 V POWER SUPPLY

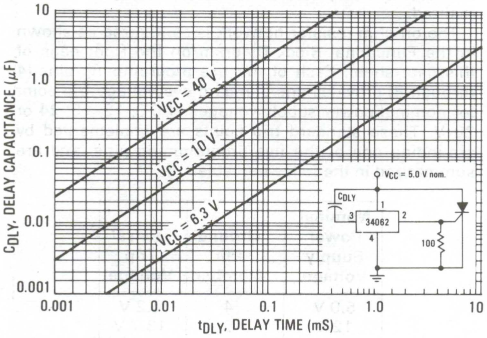


FIGURE 7 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 12 V POWER SUPPLY

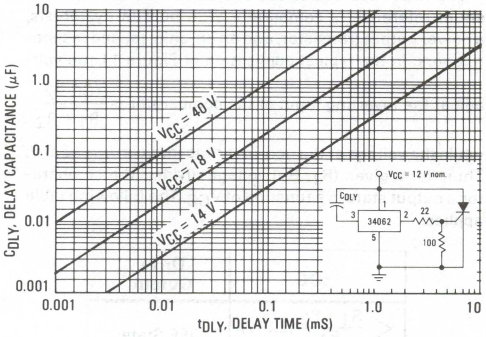


FIGURE 8 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 15 V POWER SUPPLY

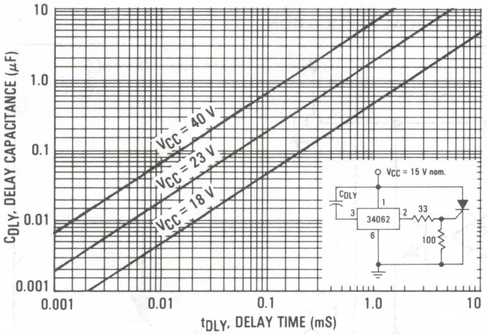


FIGURE 9 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 24 V POWER SUPPLY

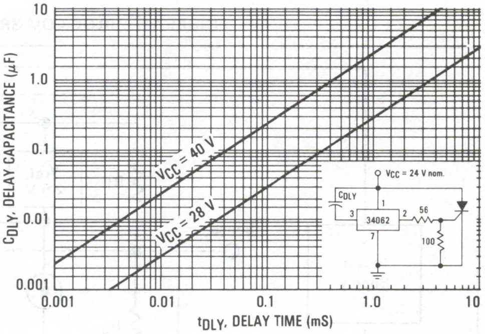
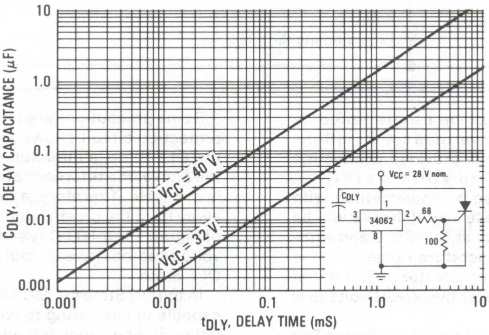


FIGURE 10 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 28 V POWER SUPPLY



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The MC34062 and MC35062 each consist of a 2.5 V shunt reference, a comparator with built-in hysteresis, a power output transistor, and an on-chip, tapped resistor network. In the typical application of Figure 11 the voltage at the inverting input of the comparator is $\frac{V_{CC}\,R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, for a given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

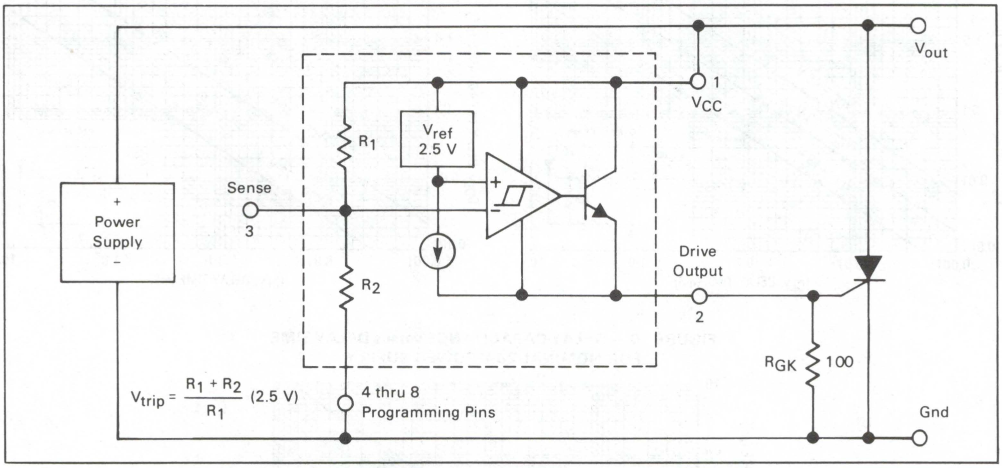
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}(2.5\ \text{V})$	OFF State
$> \frac{R_1 + R_2}{R_1}(2.5\ \text{V})$	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage from 3.5 to 40 V may be realized.

The on-chip resistor network is configured as shown in the Functional Block Diagram on the front page of this data sheet. Each of the five programming pins (4 through 8) provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. These standard trip points are implemented by grounding one of the five programming pins, and are summarized in the following table:

Nominal Power Supply Voltage	Ground Pin Number	Typical Trip Voltage
5.0 V	4	6.2 V
12 V	5	13.7 V
15 V	6	17.1 V
24 V	7	27.4 V
28 V	8	31.9 V

FIGURE 11 — BLOCK DIAGRAM AND TYPICAL APPLICATION



Many other trip voltages may be programmed by interconnecting and grounding various combinations of the programming pins. Table 1 provides connection schemes for 120 nominal Trip Voltages (V_{trip}). Additional Trip Voltages may also be implemented with other pin connections. All of these Trip Voltages will be within ±3.0% of the nominal value at $T_A = 25°C$ and within ±5.0% over the operating temperature range.

The hysteresis built into the comparator is 250 mV at the inverting input. This comparator hysteresis voltage is multiplied by the ratio $\frac{R_1 + R_2}{R_1}$, just as the 2.5 V Sense Trip Voltage (V_{Sense}) is multiplied by the same ratio to define the Trip Voltage (V_{trip}). Thus, the Hysteresis Voltage (V_H) is approximately 10% of the Trip Voltage for any Trip Voltage.

Some precautions are necessary in the operation of the protection circuit shown in Figure 11. Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 11; a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34062 becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geqslant 3.0$ V) if it is important that the reference continue to regulate.

PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34062/35062 to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 12. The time delay obtained by this technique is a function of the internal resistors (R_1, R_2) and C_{DLY}, as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltaged supply voltage V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, $V_{ref} = 2.5$ V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, t_{DLY} is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}}\right]$$

$$\text{where: } V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\text{ V})$$

Figures 6 through 10 show the C_{DLY} values versus delay time (t_{DLY}) for nominal 5.0, 12, 15, 24 and 28 V power supply protection circuits, each using a one-pin MC34062/35062 programming scheme. These figures also show the change in t_{DLY} with variations in the overvoltaged supply, V_{CC}.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34062/35062 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 5 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

FIGURE 12 — OVERVOLTAGE PROTECTION WITH TIME DELAY

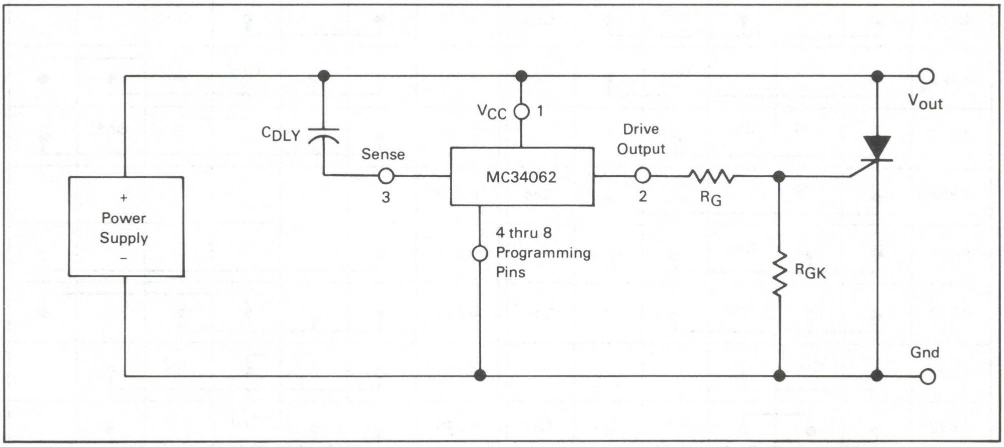
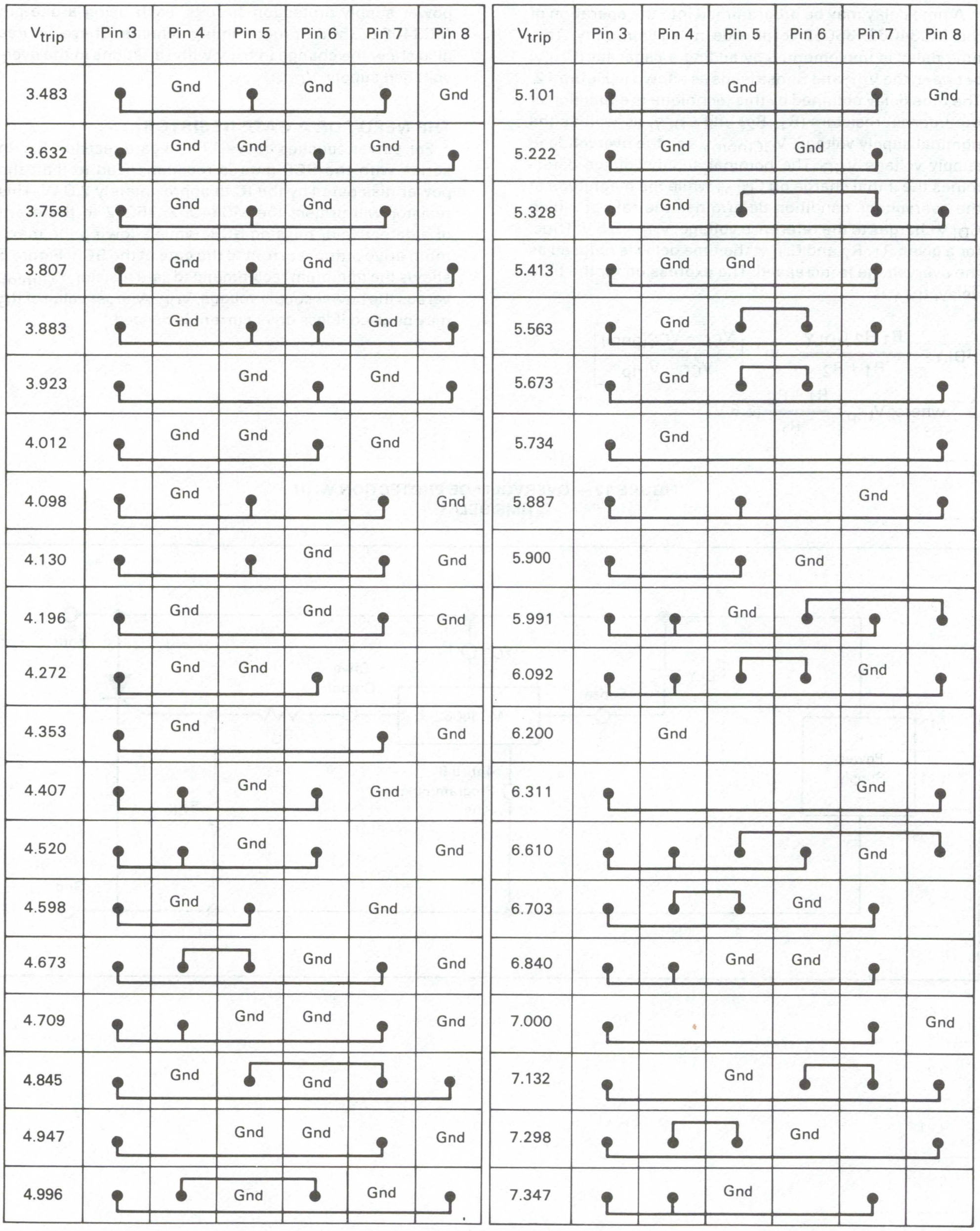


TABLE 1 — PIN-PROGRAMMING OF RESISTOR NETWORK FOR NOMINAL TRIP VOLTAGES



V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
3.483	●	Gnd	●	Gnd	●	Gnd
3.632	●	Gnd	Gnd	●	Gnd	●
3.758	●	Gnd	●	Gnd	●	
3.807	●	Gnd	●	Gnd		●
3.883	●	Gnd	●	●	Gnd	●
3.923	●		Gnd	●	Gnd	●
4.012	●	Gnd	Gnd	●	Gnd	
4.098	●	Gnd	●		●	Gnd
4.130	●		●	Gnd	●	Gnd
4.196	●	Gnd		Gnd	●	Gnd
4.272	●	Gnd	Gnd	●		
4.353	●	Gnd			●	Gnd
4.407	●	●	Gnd	●	Gnd	
4.520	●	●	Gnd	●		Gnd
4.598	●	Gnd	●		Gnd	
4.673	●	●	●	Gnd	●	Gnd
4.709	●	●	Gnd	Gnd	●	Gnd
4.845	●	Gnd	●	Gnd	●	●
4.947	●		Gnd	Gnd	●	Gnd
4.996	●	●	Gnd	●	Gnd	●
5.101	●		Gnd		●	Gnd
5.222	●	Gnd		Gnd	●	
5.328	●	Gnd	●		●	●
5.413	●	Gnd	Gnd		●	
5.563	●	Gnd	●	●	●	
5.673	●	Gnd	●	●		●
5.734	●	Gnd				●
5.887	●		●		Gnd	●
5.900	●		●	Gnd		
5.991	●	●	Gnd	●	●	●
6.092	●	●	●	●	Gnd	●
6.200		Gnd				
6.311	●				Gnd	●
6.610	●	●	●	●	Gnd	●
6.703	●	●	●	Gnd	●	
6.840	●	●	Gnd	Gnd	●	
7.000	●				●	Gnd
7.132	●		Gnd	●	●	●
7.298	●	●	●	Gnd		●
7.347	●	●	Gnd		●	

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
7.478	●	●	Gnd	Gnd		●
7.799	●	●	Gnd	●		●
8.106		●	Gnd	●	Gnd	
8.220		●	Gnd	●		Gnd
8.409		●	Gnd	Gnd	●	Gnd
8.539		●	Gnd	●		
8.633		●		Gnd	●	Gnd
8.756		●	●	Gnd	●	
8.870	●	●	Gnd	Gnd	●	●
8.906	●	●	●	●	●	Gnd
9.013		●	Gnd		Gnd	●
9.178	●	●		●	●	Gnd
9.331	●	V_{CC}	●	Gnd		
9.377	●	●	Gnd		●	●
9.385		●		Gnd	Gnd	●
9.433	●		Gnd			●
9.600		●	●	Gnd		
9.826	●	●		Gnd	●	●
9.912		●			Gnd	●
10.000	●	●	Gnd			
10.400	●		●	●	●	Gnd
10.540		●	Gnd	Gnd	●	
10.700		●			●	Gnd
11.047		●	Gnd		●	
11.178		●	Gnd	Gnd		●
11.496		●		Gnd	●	
11.630	●	●	●	Gnd	●	Gnd
11.895	●			Gnd	●	V_{CC}
11.937	●	●	●	Gnd	Gnd	●
12.086	●		Gnd		●	V_{CC}
12.477		●		Gnd		●
12.556	●	●	●	Gnd	●	
12.732		●	●	●	Gnd	●
12.800	●			●	Gnd	
13.387	●	●	●		Gnd	●
13.400	●	●		Gnd		
13.700			Gnd			
14.233	●	●	●	●	Gnd	
14.500	●	●	●		●	Gnd
15.330			●	Gnd	●	Gnd

TABLE 1 — (Continued)

V_{trip}	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
15.637			●	Gnd	Gnd	●
16.200	●		●		Gnd	
16.256			●	Gnd	●	
16.465			●	Gnd		●
16.500		●		●	Gnd	
16.532	●	●		●	Gnd	●
16.832			●	●	Gnd	●
17.087			●		Gnd	●
17.100				Gnd		
17.300	●			●		Gnd
17.900	●	●		●	●	Gnd
18.200			●		●	Gnd
18.733	●	●	●	●		Gnd
19.900		●	●		Gnd	
20.232				●	Gnd	●
20.300	●	●	●	●	Gnd	
20.700	●		●			Gnd
21.000		●		●		Gnd
21.600				●	●	Gnd
22.122	●	V_{CC}		●	Gnd	
22.673	●		V_{CC}	●	Gnd	
23.700	●	●			Gnd	
23.807	●	●	V_{CC}	●	Gnd	
24.000			●	●	Gnd	
24.283		●	V_{CC}	●		Gnd
24.400		●	●			Gnd
24.800	●	●	●	●		Gnd
25.211	●			Gnd	V_{CC}	●
27.333	●	V_{CC}	V_{CC}	●	Gnd	
27.400					Gnd	
28.200	●	●				Gnd
28.500			●	●		Gnd
30.023	●	V_{CC}	●		Gnd	
30.694	●	V_{CC}		●		Gnd
31.486	●		V_{CC}	●		Gnd
31.900						Gnd
32.233	●	V_{CC}	●	●		Gnd
33.116	●	●	V_{CC}	●		Gnd
38.182	●	V_{CC}	V_{CC}	●		Gnd
39.064	●	V_{CC}	●			Gnd

CROWBAR SCR CONSIDERATIONS

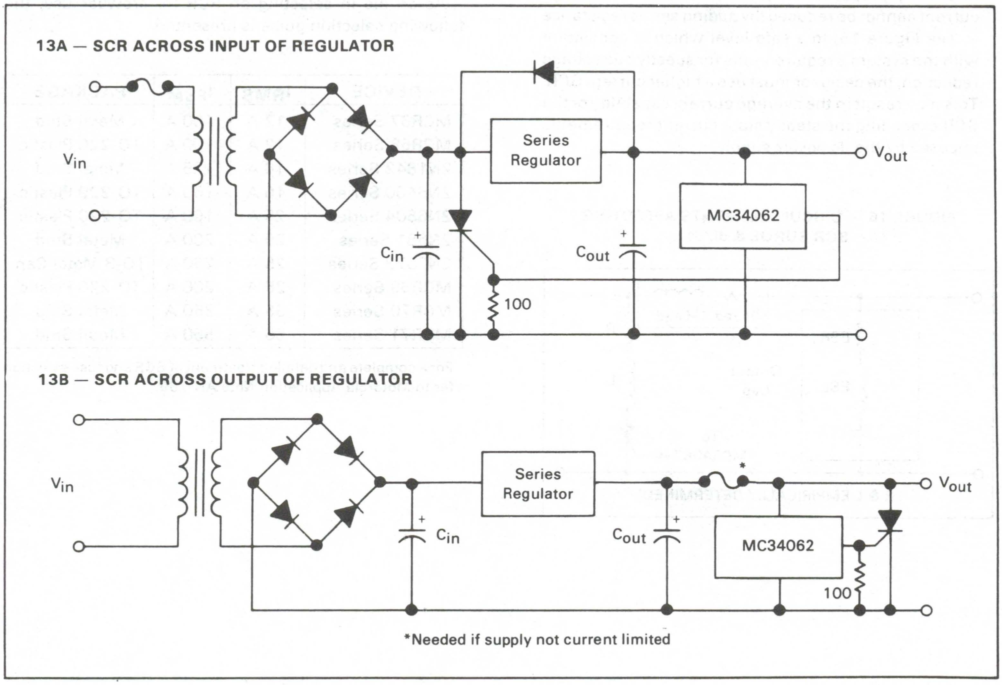
Referring to Figure 13, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 13A, the supply's input filter capacitors. This surge current is illustrated in Figure 14, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

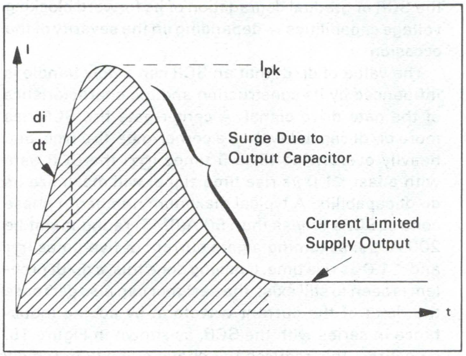
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be $200\ A/\mu s$, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 15. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 13 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

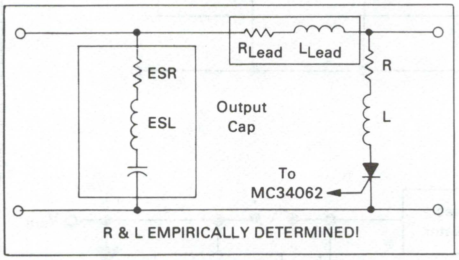
FIGURE 14 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 15) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 15 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 13A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 13B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

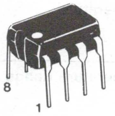
MOTOROLA

MC34063
MC35063
MC33063

Advance Information

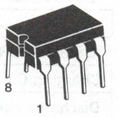
DC TO DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

U SUFFIX
CERAMIC PACKAGE
CASE 693-02

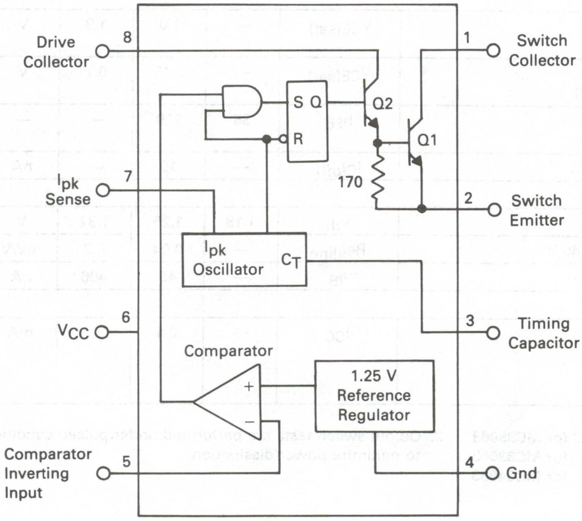


DC TO DC CONVERTER CONTROL CIRCUITS

The MC34063 Series is a monolithic control circuit containing the primary functions required for dc-to-dc converters. The device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down (Buck) and Step-Up (Boost) applications with a minimum number of external components.

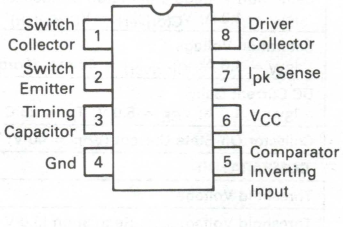
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current of 1.5 A
- Output Voltage Adjustable from 1.25 to 40 V
- Frequency Operation from 100 Hz to 100 kHz

FUNCTIONAL BLOCK DIAGRAM



Drive Collector
8
1
Switch Collector
S Q
R
Q2
Q1
170
Ipk Sense
7
2
Switch Emitter
Ipk Oscillator
CT
6
VCC
3
Timing Capacitor
Comparator
+
−
1.25 V Reference Regulator
Comparator Inverting Input
5
4
Gnd

PIN CONNECTIONS



Switch Collector
1
Switch Emitter
2
Timing Capacitor
3
Gnd
4
8
Driver Collector
7
Ipk Sense
6
VCC
5
Comparator Inverting Input

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063U	−55 to +125°C	Ceramic DIP
MC33063U	−40 to +85°C	Ceramic DIP
MC33063P1		Plastic DIP
MC34063U	0 to +70°C	Ceramic DIP
MC34063P1		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics Ceramic Package $T_A = +25°C$ Derate above $T_A = +25°C$ Plastic Package $T_A = +25°C$ Derate above $T_A = +25°C$	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 1.25 10 1.0 10	 W mW/°C W mW/°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +150 +125	°C
Operating Ambient Temperature Range MC35063 MC33063 MC34063	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ V; $T_A = T_{low}$ to T_{high} [Note 1] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (5.0 V ≤ V_{CC} ≤ 40 V, $T_A = 25°C$)	I_{chg}	20	35	50	μA
Discharge current (5.0 V ≤ V_{CC} ≤ 40 V; $T_A = 25°C$)	I_{dischg}	150	200	250	μA
Voltage Swing ($T_A = 25°C$)	V_{osc}	—	0.5	—	V_{p-p}
Discharge to Charge Current Ratio ($I_{pk(sense)} = V_{CC}$, $T_A = 25°C$)	I_{dischg}/I_{chg}	—	6.0	—	—
Current Limit Sense Voltage $I_{chg} = I_{dischg}$, $T_A = 25°C$	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation Voltage, Darlington Connection $I_{SW} = 1.0$ A; $V_{C(driver)} = V_{C(switch)}$	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage $I_{SW} = 1.0$ A; $I_{C(driver)} = 50$ mA, (Forced B ≈ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain $I_{SW} = 1.0$ A; $V_{CE} = 5.0$ V; $T_A = 25°C$	h_{FE}	35	120	—	—
Collector Off-State Current ($V_{CE} = 40$ V; $T_A = 25°C$)	$I_{C(off)}$	—	10	—	nA
COMPARATOR					
Threshold Voltage	V_{th}	1.18	1.25	1.32	V
Threshold Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V)	Reg_{line}	—	0.04	0.2	mV/V
Input Bias Current ($V_{in} = 0$ V)	I_{IB}	—	40	400	nA
TOTAL DEVICE					
Supply Current 5.0 V ≤ V_{CC} ≤ 40 V, $C_T = 0.001$ μF $I_{pk(sense)} = V_{CC}$, V pin 5 > V_{th}, Pin 2 = Gnd, Remaining pins open	I_{CC}	—	2.4	3.5	mA

NOTES:

1. T_{low} = −55°C for MC35063 T_{high} = +125°C for MC35063
   −40°C for MC33063 +85°C for MC33063
   0°C for MC34063 +70°C for MC34063
2. Output switch tests are performed under pulsed conditions to minimize power dissipation.

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

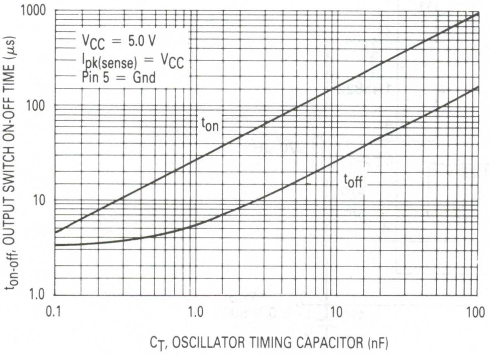


FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

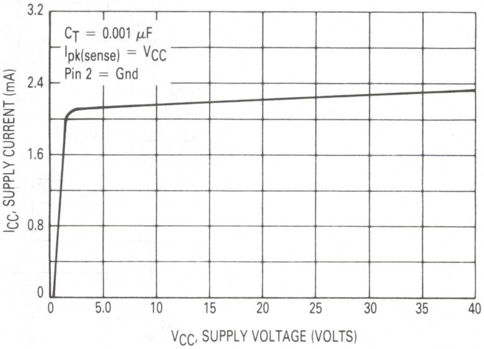


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT

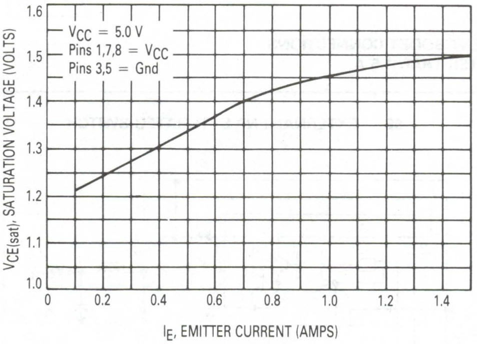


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

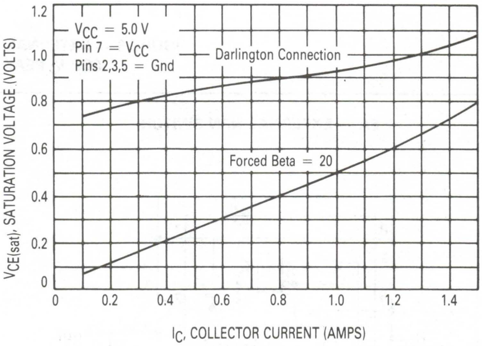
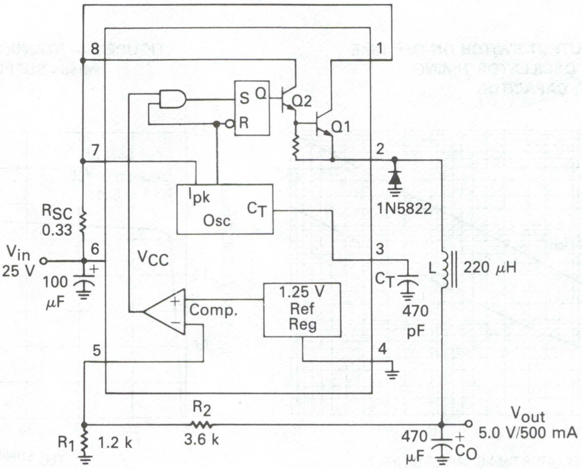
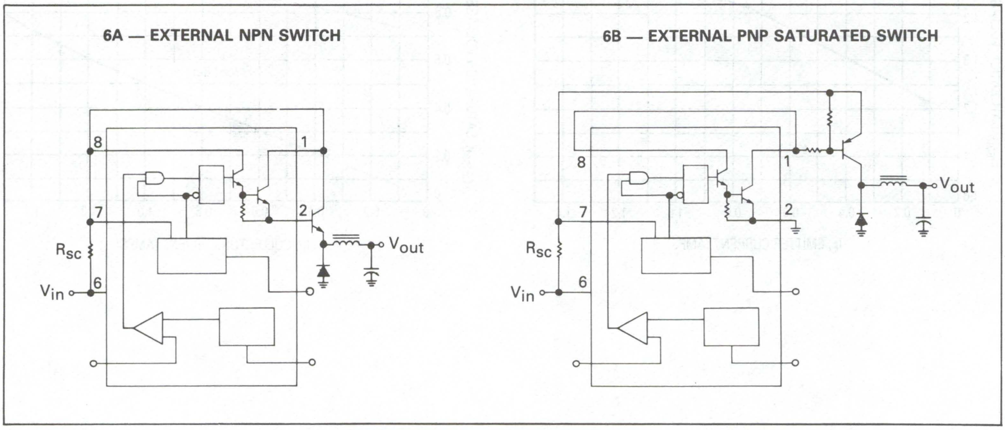


FIGURE 5 — STEP-DOWN CONVERTER


8
1
S
Q
R
Q2
Q1
7
2
I_{pk}
Osc
C_T
1N5822
R_{SC}
0.33
V_{in}
25 V
6
V_{CC}
3
100
µF
L
220 µH
C_T
470
pF
+
−
Comp.
1.25 V
Ref
Reg
5
4
R_2
3.6 k
V_{out}
5.0 V/500 mA
R_1
1.2 k
470
µF
C_O

Test	Conditions	Results
Line Regulation	V_{in} = 15 to 25 V, I_O = 500 mA	15 mV
Load Regulation	V_{in} = 25 V, I_O = 50 to 500 mA	5.0 mV
Output Ripple	V_{in} = 25 V, I_O = 500 mA	40 mV_{p-p}
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	2.3 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	84.7%

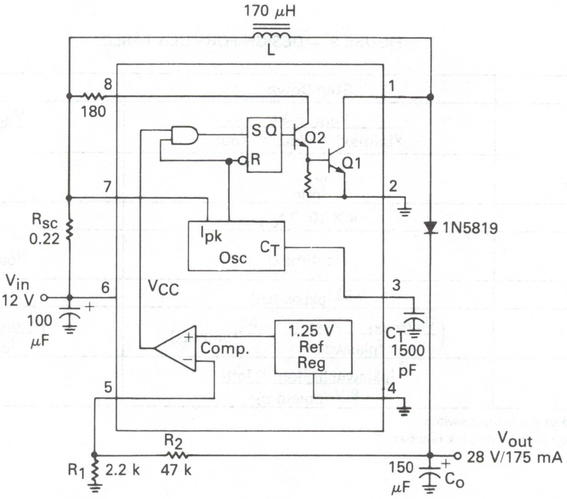
FIGURE 6 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A


6A — EXTERNAL NPN SWITCH

6B — EXTERNAL PNP SATURATED SWITCH

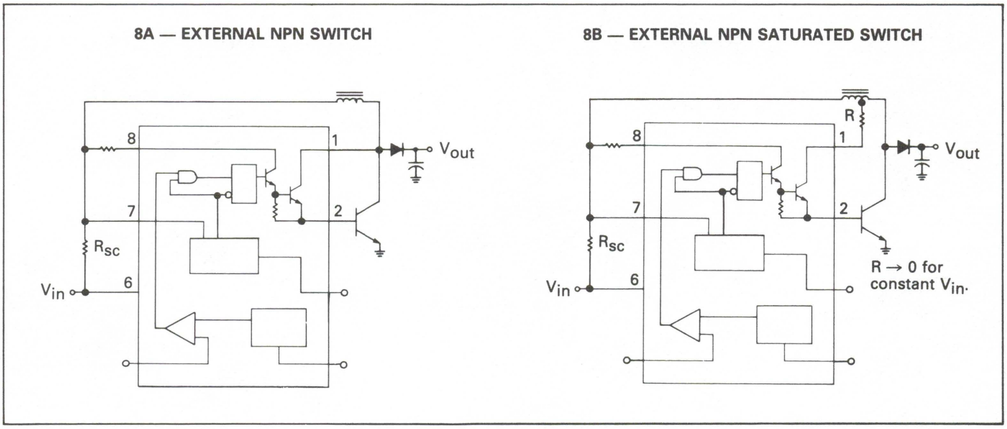
8
1
7
2
R_{sc}
V_{in}
6
V_{out}
8
1
7
2
R_{sc}
V_{in}
6
V_{out}

FIGURE 7 — STEP-UP CONVERTER


170 µH
L
8
180
1
S Q
R
Q2
Q1
7
2
Rsc
0.22
Ipk
Osc
CT
1N5819
Vin
12 V
6
VCC
3
100
µF
+
1.25 V
Ref
Reg
Comp.
CT
1500
pF
5
4
R2
47 k
R1
2.2 k
Vout
28 V/175 mA
150
µF
Co

Test	Conditions	Results
Line Regulation	V_{in} = 8.0 to 16 V, I_o = 175 mA	12 mV
Load Regulation	V_{in} = 12 V, I_o = 75 to 175 mA	45 mV
Output Ripple	V_{in} = 12 V, I_o = 175 mA	150 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	2.0 A
Efficiency	V_{in} = 12 V, I_o = 175 mA	93%

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A


8A — EXTERNAL NPN SWITCH

8B — EXTERNAL NPN SATURATED SWITCH

8
1
7
2
Rsc
6
Vin
Vout
R
8
1
7
2
Rsc
6
Vin
Vout
R → 0 for constant Vin.

FIGURE 9 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(max)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$0.33/I_{pk(switch)}$	$0.33/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(max)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on\,(max)}$
C_O	$\frac{I_{pk(switch)}\,(t_{on} + t_{off})}{8\, V_{ripple(p\text{-}p)}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(p\text{-}p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

MOTOROLA

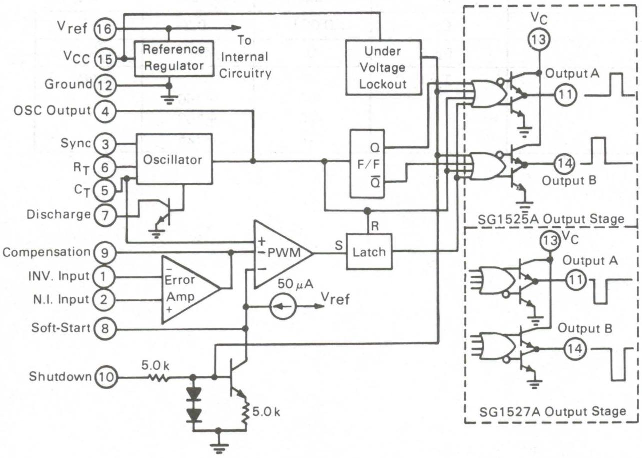
SG1525A/SG1527A
SG2525A/SG2527A
SG3525A/SG3527A

PULSE WIDTH MODULATOR CONTROL CIRCUITS

The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The device includes a +5.1 volt ±1% reference and an error amplifier with a common-mode range including the reference voltage to eliminate external divider resistors. A sync input to the oscillator enables multiple units to be slaved together, or a single unit can be synchronized to an external system clock. A wide range of dead time is programmable with a single resistor between the C_T pin and the Discharge pin. Other features included are soft-start circuitry requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, allowing fast output turn-off with soft-start recycle turn-on. Undervoltage lockout keeps the outputs off when V_{CC} is less than the required level for normal operation. The output stages are a totem-pole design capable of sinking and sourcing in excess of 200 mA. The SG1525A series output stage features NOR Logic, giving a low output for an off state. The SG1527A utilizes OR Logic which results in a high output level when off. These devices are available in Military, Industrial and Commercial temperature ranges and feature:

- 8.0 to 35 Volt Operation
- 5.1 Volt ±1% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Current: ±400 mA Peak

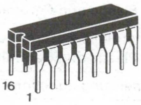
FUNCTIONAL BLOCK DIAGRAM

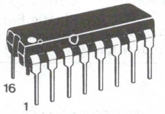

Vref 16
VCC 15
Ground 12
OSC Output 4
Sync 3
RT 6
CT 5
Discharge 7
Compensation 9
INV. Input 1
N.I. Input 2
Soft-Start 8
Shutdown 10
Reference Regulator
To Internal Circuitry
Under Voltage Lockout
Oscillator
Q
F/F
Q̄
R
S
Latch
PWM
Error Amp
50 µA
Vref
5.0 k
5.0 k
VC
13
Output A
11
14
Output B
SG1525A Output Stage
SG1527A Output Stage

PULSE WIDTH MODULATOR CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

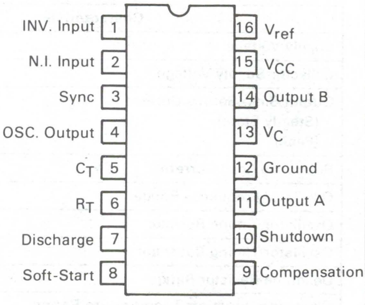
J SUFFIX
CERAMIC PACKAGE
CASE 620-02





N SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS


INV. Input 1
N.I. Input 2
Sync 3
OSC. Output 4
CT 5
RT 6
Discharge 7
Soft-Start 8
16 Vref
15 VCC
14 Output B
13 VC
12 Ground
11 Output A
10 Shutdown
9 Compensation

(Top View)

ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1525AJ	−55 to +150°C	Ceramic DIP
SG1527AJ	−55 to +150°C	Ceramic DIP
SG2525AJ	−25 to +150°C	Ceramic DIP
SG2525AN	−25 to +150°C	Plastic DIP
SG2527AJ	−25 to +150°C	Ceramic DIP
SG2527AN	−25 to +150°C	Plastic DIP
SG3525AJ	0 to +125°C	Ceramic DIP
SG3525AN	0 to +125°C	Plastic DIP
SG3527AJ	0 to +125°C	Ceramic DIP
SG3527AN	0 to +125°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	−0.3 to +5.5	V
Analog Inputs	—	−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) Note 2, $T_A = +25°C$ Note 3, $T_C = +25°C$	P_D	 1000 2000	mW
Thermal Resistance Junction to Air Plastic and Ceramic Package	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case Plastic and Ceramic Package	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	−65 to +150 −55 to +125	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	+300	°C

NOTES:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 16 mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Junction Temperature Range SG1525A, SG1527A SG2525A, SG2527A SG3525A, SG3527A	T_J	 −55 −25 0	 +150 +150 +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_J = T_{low} to T_{high} [Note 4], unless otherwise specified)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.05	5.10	5.15	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	20	50	—	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	20	50	—	20	50	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	5.00	—	5.20	4.95	—	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	—	80	100	—	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	—	40	200	—	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	—	20	50	—	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise specified)								
Initial Accuracy (T_J = +25°C)	—	—	±2.0	±6.0	—	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	±0.3	±1.0	—	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	—	±3.0	±6.0	—	±3.0	±6.0	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	—	—	100	—	—	100	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	—	—	400	—	—	kHz
Current Mirror (I_{RT} = 2.0 mA)	—	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	3.0	3.5	—	V
Clock Width (T_J = +25°C)	—	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold	—	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)	—	—	1.0	2.5	—	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)								
Input Offset Voltage	V_{IO}	—	0.5	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	—	1.0	10	μA
Input Offset Current	I_{IO}	—	—	1.0	—	—	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	—	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	3.8	5.6	—	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	—	60	75	—	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	—	50	60	—	dB
PWM COMPARATOR SECTION								
Minimum Duty Cycle	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	—	0.05	1.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A Min	Typ	Max	SG3525A SG3527A Min	Typ	Max	Unit
SOFT-START SECTION								
Soft-Start Current ($V_{shutdown}$ = 0 V)	—	25	50	80	25	50	80	μA
Soft-Start Voltage ($V_{shutdown}$ = 2.0 V)	—	—	0.4	0.6	—	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)	—	—	0.4	1.0	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)								
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 — —	 0.2 1.0	 0.4 2.0	 — —	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 — —	 18 17	 19 18	 — —	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	—	—	200	—	—	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	100	600	—	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	300	—	50	300	ns
Shutdown Delay (V_{SD} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	—	0.2	0.5	—	0.2	0.5	μs
Supply Current, (V_{CC} = +35 V)	I_{CC}	—	14	20	—	14	20	mA

NOTES:

4. T_{low} = −55°C for SG1525A/1527A
−25°C for SG2525A/2527A
0°C for SG3525A/3527A

T_{high} = +150°C for SG1525A/1527A
+150°C for SG2525A/2527A
+125°C for SG3525A/3527A

5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6 Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0 Ω).
7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

Shutdown Options (see block diagram, front page)

1. An external open collector comparator or transistor can be used to pull down the Compensation pin (9). This will set the PWM latch and turn off both outputs. Pulse-by-pulse protection can be accomplished if the shutdown signal is momentary, since the PWM latch will be reset with each clock pulse.

2. Shutdown can also be accomplished by pulling down on the SOFT-START pin (8). When using this approach, shutdown will not affect the amplifier compensation network; however, if a SOFT-START capacitor is used, it must be discharged, possible slowing shutdown response.

3. Applying a positive-going signal to the Shutdown pin (10) will provide the most rapid shutdown of the outputs if a soft-start capacitor is not used at Pin 8. An external soft-start capacitor at Pin 8 will slow shutdown response due to the discharge time of the soft-start capacitor. Dishcarge current is approximately twice the charging current.

4. The Shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Pin 8. Soft-start characteristics may still be accomplished by applying an external capacitor, blocking diode and charging resistor to the Compensation pin (9).

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC

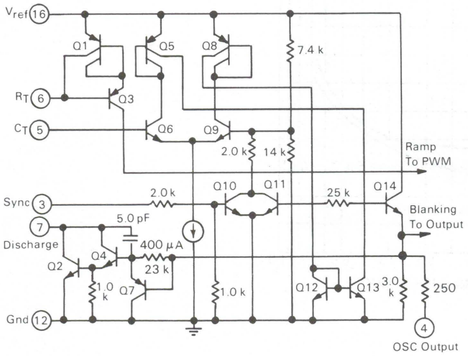

Vref 16
Q1
Q5
Q8
7.4 k
RT 6
Q3
CT 5
Q6
Q9
2.0 k
14 k
Ramp To PWM
Sync 3
2.0 k
Q10
Q11
25 k
Q14
Blanking To Output
7 Discharge
5.0 pF
400 μA
Q2
Q4
23 k
1.0 k
Q7
1.0 k
Q12
Q13
3.0 k
250
Gnd 12
4 OSC Output

FIGURE 2 — OSCILLATOR CHARGE TIME versus R_T

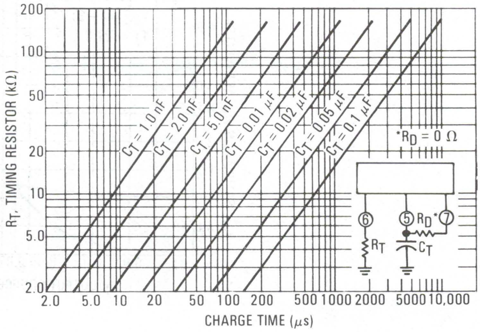


FIGURE 3 — OSCILLATOR DISCHARGE TIME versus R_D

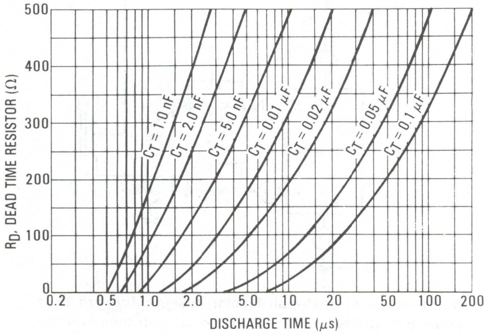


FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC

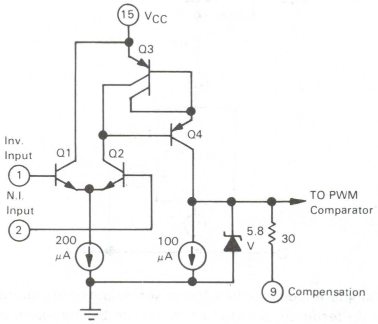

15 VCC
Q3
Q4
Inv. Input
1
Q1
Q2
N.I. Input
2
200 μA
100 μA
5.8 V
30
TO PWM Comparator
9 Compensation

FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

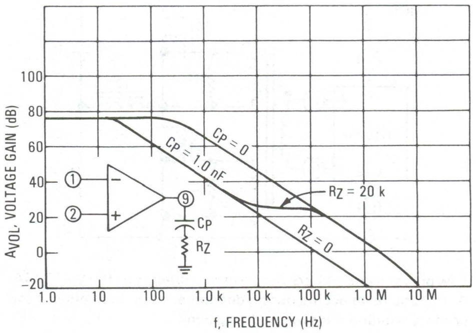


FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

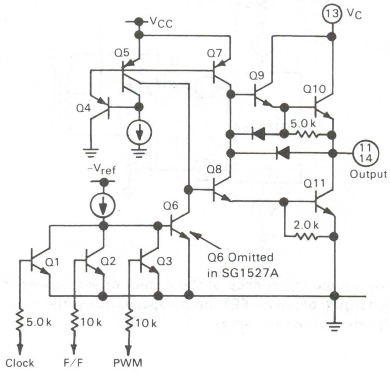

13 VC
VCC
Q5
Q7
Q9
Q10
Q4
5.0 k
11 14 Output
−Vref
Q8
Q6
Q11
2.0 k
Q1
Q2
Q3
Q6 Omitted in SG1527A
5.0 k
10 k
10 k
Clock
F/F
PWM

FIGURE 7 — SG1525A/2525A/3525A OUTPUT SATURATION CHARACTERISTICS

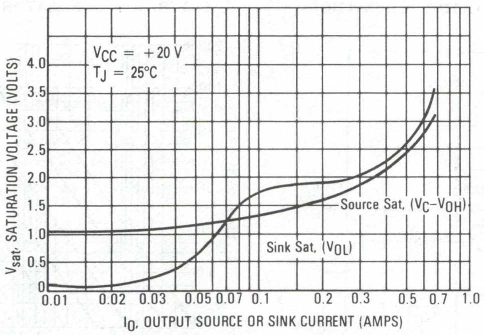
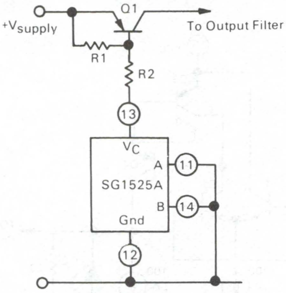


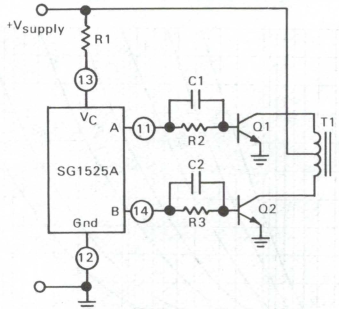
FIGURE 8 — SINGLE ENDED SUPPLY



+V_{supply}
Q1
To Output Filter
R1
R2
13
V_C
A
11
SG1525A
B
14
Gnd
12

For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

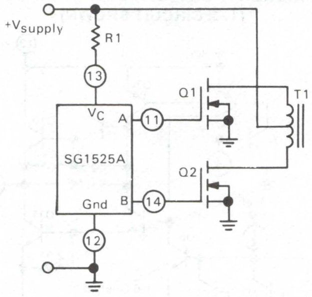
FIGURE 9 — PUSH-PULL CONFIGURATION



+V_{supply}
R1
13
C1
V_C
A
11
R2
Q1
T1
SG1525A
C2
B
14
R3
Q2
Gnd
12

In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

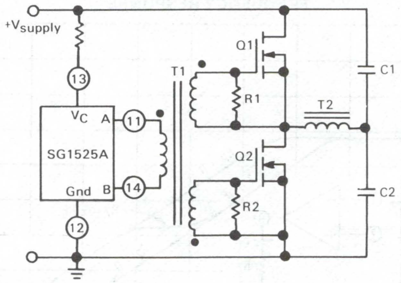
FIGURE 10 — DRIVING POWER FETS



+V_{supply}
R1
13
Q1
T1
V_C
A
11
SG1525A
Q2
Gnd
B
14
12

The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

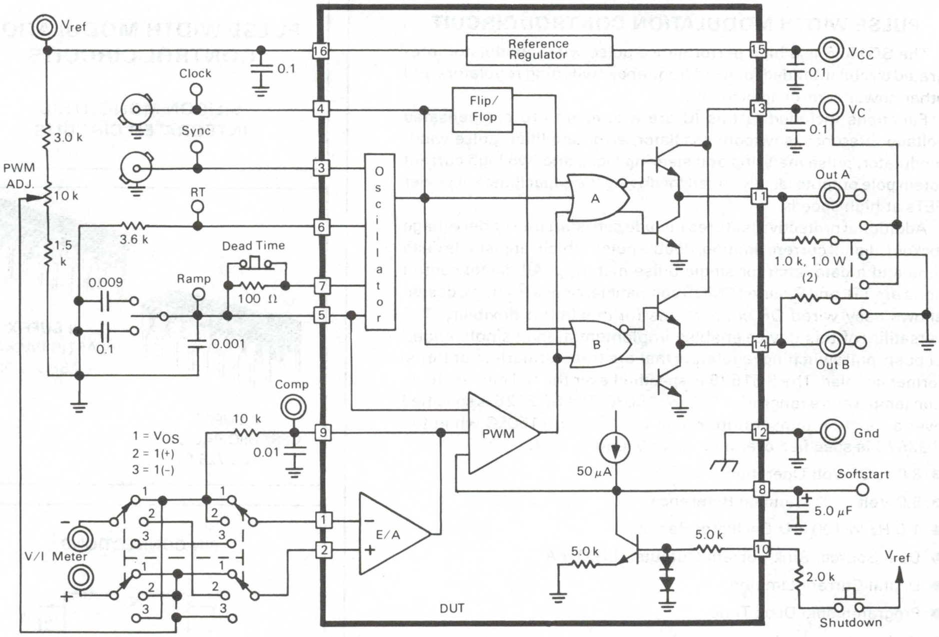
FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION



+V_{supply}
Q1
C1
13
T1
R1
T2
V_C
A
11
SG1525A
Q2
Gnd
B
14
R2
C2
12

Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

FIGURE 12 — LAB TEST FIXTURE


Vref
0.1
Clock
Sync
3.0 k
PWM ADJ.
10 k
RT
3.6 k
1.5 k
Dead Time
0.009
Ramp
100 Ω
0.1
0.001
Comp
10 k
0.01
1 = VOS
2 = I(+)
3 = I(−)
1
2
3
V/I Meter
−
+
16
4
3
6
7
5
9
1
2
Reference Regulator
Flip/Flop
Oscillator
A
B
PWM
E/A
DUT
50 µA
5.0 k
5.0 k
15
VCC
0.1
13
VC
0.1
Out A
11
1.0 k, 1.0 W (2)
14
Out B
12
Gnd
Softstart
8
5.0 µF
10
Vref
2.0 k
Shutdown

SG1526
SG2526
SG3526

MOTOROLA

PULSE WIDTH MODULATION CONTROL CIRCUIT

The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

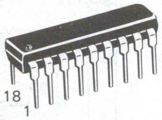
Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft-start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of −55°C to +150°C. The SG2526 is specified over a junction temperature range of −40°C to +150°C while the SG3526 is specified over a range of 0°C to +125°C.

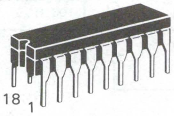
- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

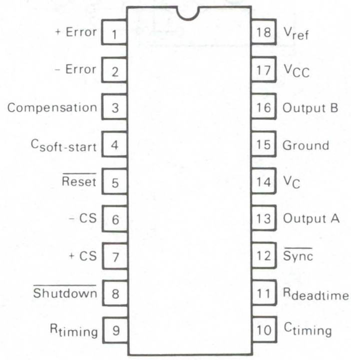


N SUFFIX
PLASTIC PACKAGE
CASE 707-02



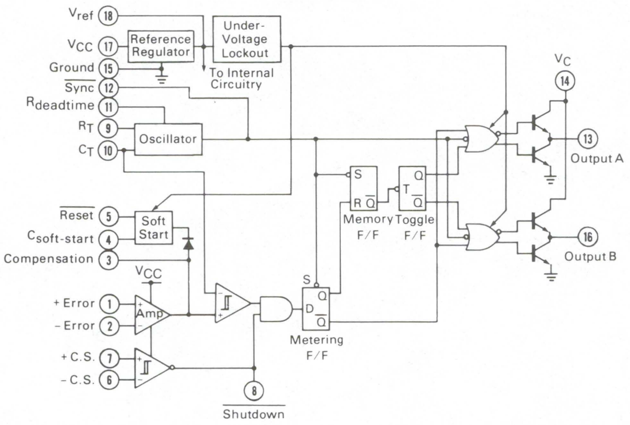
J SUFFIX
CERAMIC PACKAGE
CASE 726-01

PIN CONNECTIONS


+ Error 1
− Error 2
Compensation 3
$C_{soft\text{-}start}$ 4
$\overline{Reset}$ 5
− CS 6
+ CS 7
$\overline{Shutdown}$ 8
R_{timing} 9
18 V_{ref}
17 V_{CC}
16 Output B
15 Ground
14 V_C
13 Output A
12 $\overline{Sync}$
11 $R_{deadtime}$
10 C_{timing}

(Top View)

BLOCK DIAGRAM


V_{ref} 18
V_{CC} 17
Ground 15
$\overline{Sync}$ 12
$R_{deadtime}$ 11
R_T 9
C_T 10
Reference Regulator
Under-Voltage Lockout
To Internal Circuitry
Oscillator
V_C
14
13 Output A
16 Output B
S
R $\overline{Q}$
Memory F/F
Q
T
$\overline{Q}$
Toggle F/F
$\overline{Reset}$ 5
$C_{soft\text{-}start}$ 4
Compensation 3
Soft Start
V_{CC}
+ Error 1
− Error 2
Amp
+ C.S. 7
− C.S. 6
S
Q
D
$\overline{Q}$
Metering F/F
8
$\overline{Shutdown}$

ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1526J	−55 to +150°C	Ceramic DIP
SG2526J SG2526N	−40 to +150°C	Ceramic DIP Plastic DIP
SG3526J SG3526N	0 to +125°C	Ceramic DIP Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	−0.3 to +5.5	V
Analog Inputs	—	−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Output Current	I_{ref}	50	mA
Logic Sink Current	—	15	mA
Power Dissipation (Plastic & Ceramic Package) Note 2, $T_A = +25°C$ Note 3, $T_C = +25°C$	P_D	 1000 3000	mW
Thermal Resistance Junction to Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case (Plastic and Ceramic Package)	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

Notes:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 24 mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	μF
Available Deadtime Range (40 kHz)		3.0	50	%
Operating Junction Temperature Range SG1526 SG2526 SG3526	T_J	 −55 −40 0	 +150 +150 +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, $T_J = T_{low}$ to T_{high} [Note 4] unless otherwise specified)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION (Note 5)								
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	30	mV
Load Regulation, 0 mA ≤ I_L ≤ 20 mA	Reg_{load}	—	10	30	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T_J$	—	15	50	—	15	50	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V)	I_{SC}	25	50	100	25	50	100	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)	—	—	0.2	0.4	—	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)	—	2.4	4.8	—	2.4	4.8	—	V
OSCILLATOR SECTION (Note 6)								
Initial Accuracy (T_J = +25°C)	—	—	±3.0	±8.0	—	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	—	0.5	1.0	%
Frequency Stability over Temperature ($\Delta T_J = T_{low}$ to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	7.0	10	—	3.0	5.0	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	—	—	1.0	—	—	1.0	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	—	—	400	—	—	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc(P)}$	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc(V)}$	0.5	1.0	—	0.5	1.0	—	V
ERROR AMPLIFIER SECTION (Note 7)								
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	−350	−1000	—	−350	−2000	nA
Input Offset Current	I_{IO}	—	35	100	—	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{Vol}	64	72	—	60	72	—	dB
High Output Voltage ($V_{Pin\ 1} - V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	—	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2} - V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	—	70	94	—	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	—	66	80	—	dB
PWM COMPARATOR SECTION (Note 6)								
Minimum Duty Cycle ($V_{compensation}$ = +0.4 V)	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle ($V_{compensation}$ = +3.6 V)	DC_{max}	45	49	—	45	49	—	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
DIGITAL PORTS ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{RESET}}$)								
Output Voltage — High Logic Level (I_{source} = 40 μA)	V_{OH}	2.4	4.0	—	2.4	4.0	—	V
Output Voltage — Low Logic Level (I_{sink} = 3.6 mA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Input Current — High Logic Level (V_{IH} = +2.4 V)	I_{IH}	—	-125	-200	—	-125	-200	μA
Input Current — Low Logic Level (V_{IL} = +0.4 V)	I_{IL}	—	-225	-360	—	-225	-360	μA
CURRENT LIMIT COMPARATOR SECTION (Note 8)								
Sense Voltage ($R_S \leqslant 50\ \Omega$)	V_{sense}	90	100	110	80	100	120	mV
Input Bias Current	I_{IB}	—	-3.0	-10	—	-3.0	-10	μA
SOFT-START SECTION								
Error Clamp Voltage ($\overline{\text{Reset}}$ = +0.4 V)	—	—	0.1	0.4	—	0.1	0.4	V
$C_{Soft\text{-}Start}$ Charging Current ($\overline{\text{Reset}}$ = +2.4 V)	I_{CS}	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc unless otherwise specified)								
Output High Level I_{source} = 20 mA I_{source} = 100 mA	V_{OH}	 12.5 12	 13.5 13	 — —	 12.5 12	 13.5 13	 — —	V
Output Low Level I_{sink} = 20 mA I_{sink} = 100 mA	V_{OL}	 — —	 0.2 1.2	 0.3 2.0	 — —	 0.2 1.2	 0.3 2.0	V
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	—	50	150	—	50	150	μA
Rise Time (C_L = 1000 pF)	t_r	—	0.3	0.6	—	0.3	0.6	μs
Fall Time (C_L = 1000 pF)	t_f	—	0.1	0.2	—	0.1	0.2	μs
Supply Current ($\overline{\text{Shutdown}}$ = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	—	18	30	—	18	30	mA

Notes:

4. T_{low} = −55°C for SG1526
   −40°C for SG2526
   0°C for SG3526
   T_{high} = +150°C for SG1526/2526
   +125°C for SG3526
5. I_L = 0 mA unless otherwise noted.
6. f_{osc} = 40 kHz (R_T = 4.12 kΩ ±1%, C_T = 0.01 μF ±1%, R_D = 0 Ω)
7. $0\ V \leqslant V_{CM} \leqslant +5.2\ V$
8. $0\ V \leqslant V_{CM} \leqslant +12\ V$

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

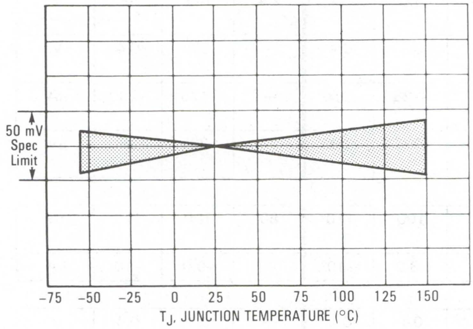


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

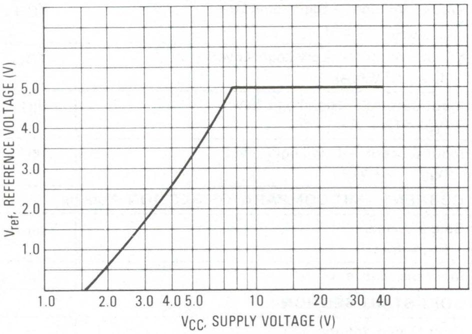


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

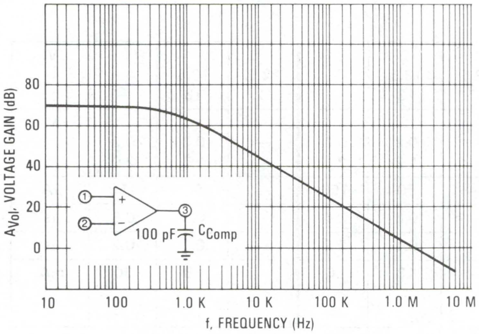


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

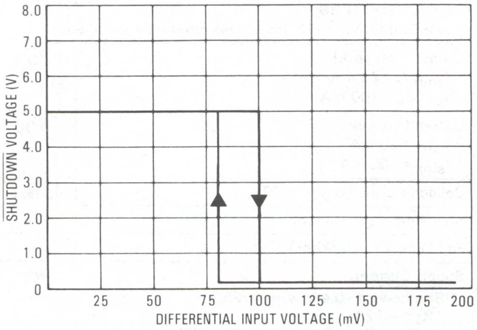


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

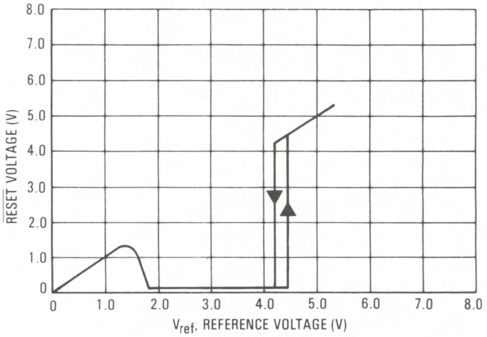
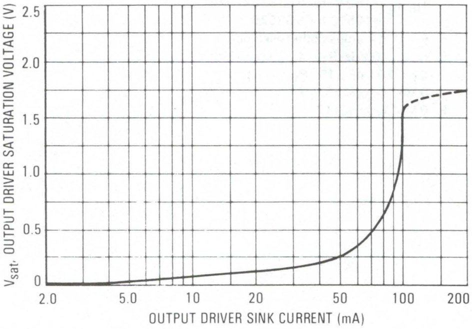


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT



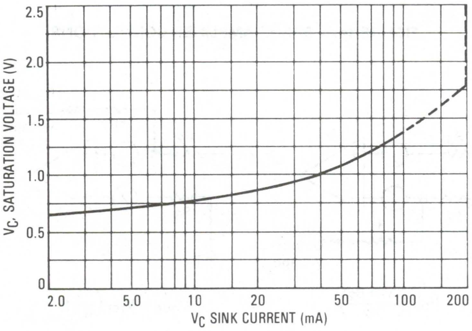


FIGURE 7 — V_C SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

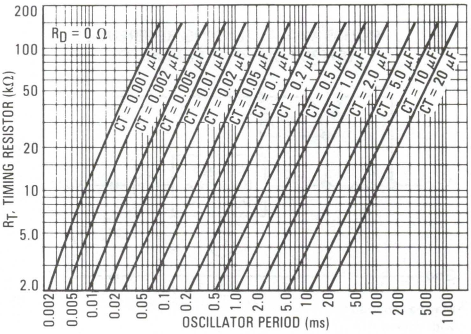


FIGURE 8 — SG1526 OSCILLATOR PERIOD

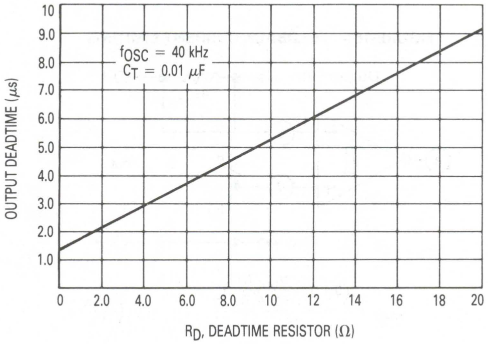


FIGURE 9 — OUTPUT DEADTIME AS A FUNCTION OF DEADTIME RESISTOR VALUE

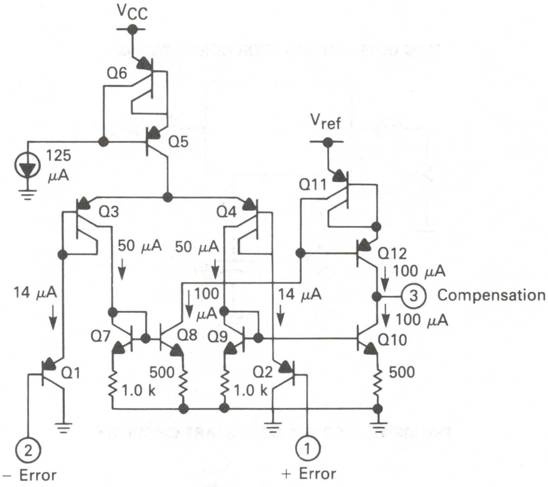

V_{CC}
Q6
Q5
125 μA
V_{ref}
Q11
Q3
Q4
50 μA
50 μA
Q12
100 μA
14 μA
100 μA
14 μA
3 Compensation
100 μA
Q7
Q8
Q9
Q10
Q1
500
1.0 k
Q2
1.0 k
500
2
− Error
1
+ Error

FIGURE 10 — SG1526 ERROR AMPLIFIER

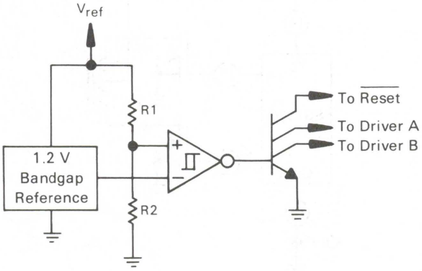

V_{ref}
R1
1.2 V Bandgap Reference
+
−
R2
To $\overline{\text{Reset}}$
To Driver A
To Driver B

FIGURE 11 — SG1526 UNDERVOLTAGE LOCKOUT

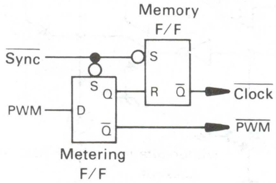

Memory F/F
$\overline{\text{Sync}}$
S
S
Q
R
$\overline{Q}$
$\overline{\text{Clock}}$
PWM
D
$\overline{Q}$
$\overline{\text{PWM}}$
Metering F/F

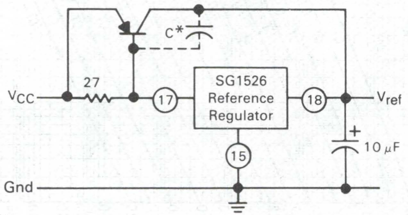
FIGURE 12 — SG1526 PULSE PROCESSING LOGIC

The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

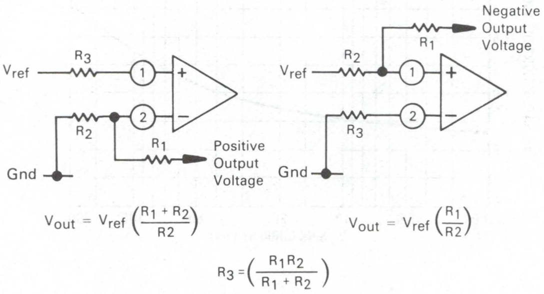
APPLICATIONS INFORMATION

FIGURE 13 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY


C*
27
VCC
17
SG1526
Reference
Regulator
18
Vref
15
+
10 µF
Gnd

*May be required
with some types
of transistors

FIGURE 14 — ERROR AMPLIFIER CONNECTIONS


Vref
R3
1
+
2
−
R2
R1
Gnd
Positive
Output
Voltage
Negative
Output
Voltage
R1
Vref
R2
1
+
2
−
R3
Gnd

$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right)$$

$$V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

FIGURE 15 — OSCILLATOR CONNECTIONS

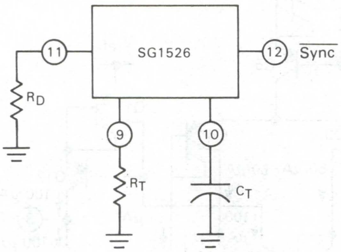
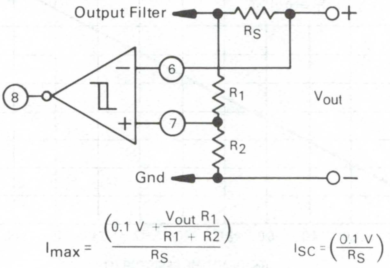

11
SG1526
12
Sync
RD
9
10
RT
CT

FIGURE 16 — FOLDBACK CURRENT LIMITING


Output Filter
RS
+
−
6
8
R1
Vout
+
7
R2
Gnd
−

$$I_{max} = \frac{\left(0.1\ V + \frac{V_{out}\ R_1}{R1\ +\ R2}\right)}{R_S}$$

$$I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$$

FIGURE 17 — SG1526 SOFT-START CIRCUITRY

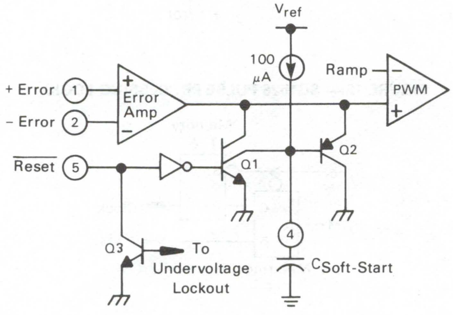
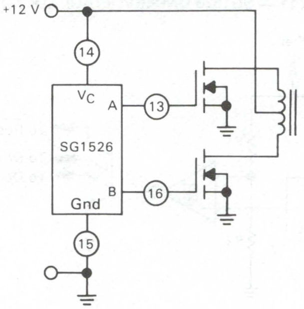

Vref
100 µA
Ramp
PWM
−
+
+ Error
1
− Error
2
+
Error
Amp
−
Reset
5
Q1
Q2
4
Q3
To
Undervoltage
Lockout
CSoft-Start

FIGURE 18 — DRIVING TMOS POWER FETS


+12 V
14
VC
A
13
SG1526
B
16
Gnd
15

The totem-pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 19 — HALF-BRIDGE CONFIGURATION

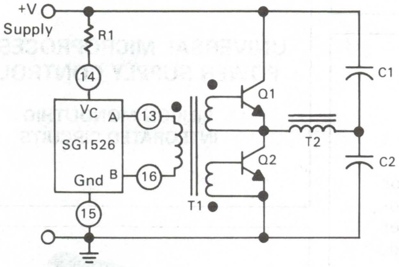
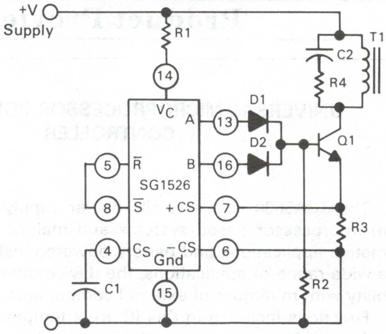

+V
Supply
R1
14
VC
A
13
SG1526
Gnd
B
16
15
T1
Q1
Q2
T2
C1
C2

FIGURE 20 — FLYBACK CONVERTER WITH CURRENT LIMITING


+V
Supply
R1
14
VC
A
13
D1
D2
5
R̄
B
16
SG1526
8
S̄
+CS
7
4
CS
−CS
6
Gnd
15
C1
T1
C2
R4
Q1
R3
R2

In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

FIGURE 21 — SINGLE-ENDED CONFIGURATION

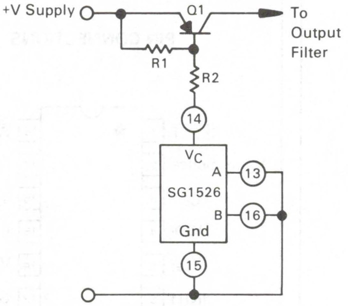
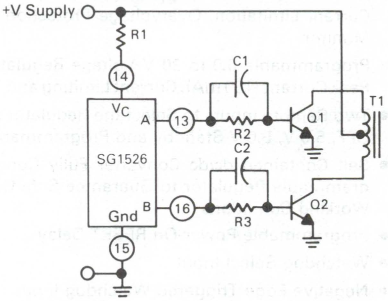

+V Supply
Q1
To
Output
Filter
R1
R2
14
VC
A
13
SG1526
B
16
Gnd
15

FIGURE 22 — PUSH-PULL CONFIGURATION


+V Supply
R1
14
C1
VC
A
13
R2
Q1
T1
C2
SG1526
B
16
R3
Q2
Gnd
15

TCA5600
TCF5600

MOTOROLA

Product Preview

UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

The TCA5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

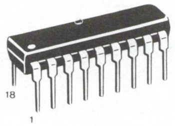
- 6.0 to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor
- Programmable 6.0 to 30 V Voltage Regulator Exhibiting High Peak Current (150 mA), Current Limiting and Thermal Protection
- Two Remote Inputs to Select the Regulator's Operation Mode: OFF, 5.0 V, 5.0 V Standby and Programmable Output Voltage
- Self Contained dc/dc Converter Fully Controlled By the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL- and MOS-Compatible

APPLICATIONS INCLUDE

- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems

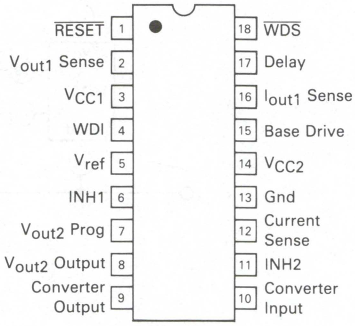
UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 707-02

PIN CONNECTIONS



(Top View)

RECOMMENDED OPERATION CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

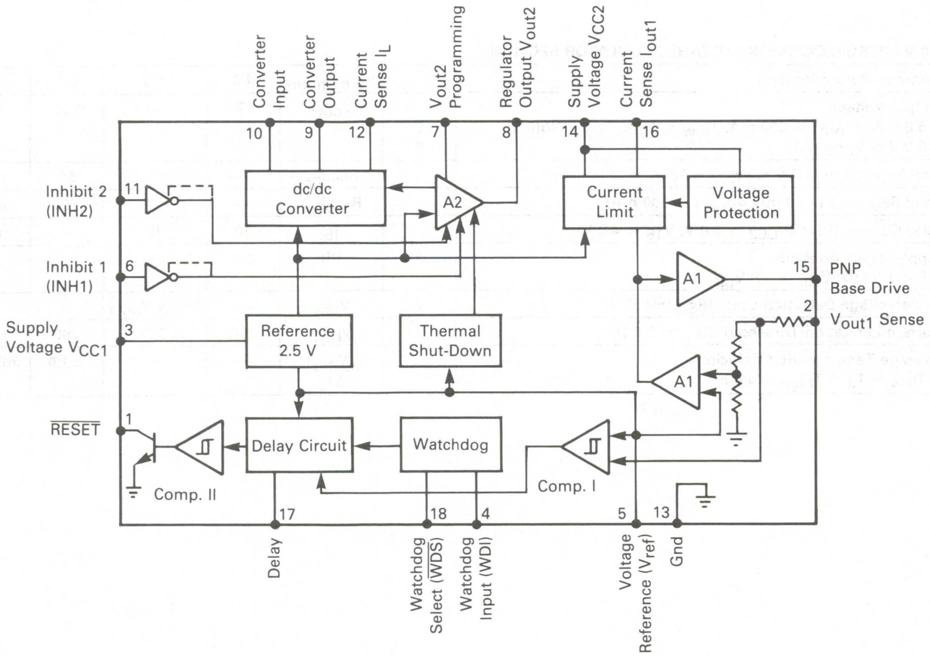
Device	Operating Junction Temperature Range	Package
TCA5600	0 to +125°C	Plastic DIP
TCF5600	−40 to +150°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3, 14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10–Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{\text{WDS}}$ (Pin 6, 11, 18)	V_{INP}	−0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{\text{RESET}}$ (Pin 1)	$I_{\overline{RES}}$	10	mA
Analog Inputs (Pin 2) (Pin 7)	— —	−0.3 to 10 −0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +75°C TCA5600 T_A = +85°C TCF5600	P_D	 500 650	mW
Thermal Resistance (Junction to Air)	$R_{\theta JA}$	100	°C/W
Operating Temperature Range TCA5600 TCF5600	T_A	 0 to +75 −40 to +85	°C
Operating Junction Temperature TCA5600 TCF5600	T_J	 +125 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:
1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
   Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



Converter Input
Converter Output
Current Sense I_L
Vout2 Programming
Regulator Output Vout2
Supply Voltage VCC2
Current Sense Iout1
10
9
12
7
8
14
16
Inhibit 2 (INH2)
11
dc/dc Converter
A2
Current Limit
Voltage Protection
Inhibit 1 (INH1)
6
A1
15
PNP Base Drive
2
Vout1 Sense
Supply Voltage VCC1
3
Reference 2.5 V
Thermal Shut-Down
A1
RESET
1
Delay Circuit
Watchdog
Comp. II
Comp. I
17
18
4
5
13
Delay
Watchdog Select (WDS)
Watchdog Input (WDI)
Voltage Reference (Vref)
Gnd

ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 (Note 3); R_{SC} = 0.5 Ω; INH1 = "High"; INH2 = "High"; $\overline{WDS}$ = "High"; I_{out2} = 0 (Note 4); if not otherwise specified)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage I_{ref} = 0.5 mA, T_{low} ≤ T_J ≤ T_{high} (Note 5), 6.0 V ≤ V_{CC1} ≤ 18 V		V_{ref}	2.4	—	2.6	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	+/−0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	60	70	—	dB
Output Impedance 0 ≤ I_{ref} ≤ 2.0 mA		Z_O	—	1.0	—	Ohm
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA

NOTES:

3. The external PNP power transistor satisfies the following minimum specifications:
   h_{FE} ≥ 60 at I_C = 500 mA and V_{CE} = 5.0 V; $V_{CE(sat)}$ ≤ 300 mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1)
5. T_{low} = 0°C for TCA5600; T_{low} = −40°C for TCF5600.
   T_{high} = 125°C for TCA5600; T_{high} = 150°C for TCF5600.

5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION

Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage 5.0 mA ≤ I_{out1} ≤ 300 mA, T_{low} ≤ T_J ≤ T_{high} (Note 5) 6.0 V ≤ V_{CC2} ≤ 18 V	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	10	50	mV
Load Regulation (5.0 mA ≤ I_{out1} ≤ 300 mA)		Reg_{load}	—	20	100	mV
Base Current Drive (V_{CC2} = 6.0 V, V_{15} = 4.0 V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	50	65	—	dB
Undervoltage Detection Level (R_{SC} = 5.0 Ω)	7	V_{low}	4.5	0.93 x V_{out1}	—	V
Current Limitation Threshold (R_{SC} = 5.0 Ω)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)						
Nominal Output Voltage		$V_{out2(nom)}$	23	24	25	V
Output Voltage 1.0 mA ≤ I_{out2} ≤ 100 mA, T_{low} ≤ T_J ≤ T_{high} (Notes 5, 7)	8	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)		Reg_{load}	—	40	200	mV
DC Output Current		I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)		$I_{out2\ p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}		RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, T_{low} ≤ T_J ≤ T_{high}, INH1 = "High" (Note 5)		$V_{out2(5.0\ V)}$	4.75	—	5.25	V
OFF State Output Impedance (INH2 = "Low")		R_{out1}	—	10	—	kΩ
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)		$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V

NOTES:

6. V_9 = 28 V, INH1 = "Low" for this Electrical Characteristic section unless otherwise specified.
7. Pulse tested t_p ≤ 300 µs

DC/DC CONVERTER SECTION

Collector Current Detection Level "High" R_C = 10 k "Low"	9	$V_{12}(H)$ $V_{12}(L)$	350 —	400 50	450 —	mV
Collector Saturation Voltage I_C = 600 mA (Note 7)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop I_F = 600 mA (Note 7)	11	V_F	—	—	1.4	V

WATCHDOG AND $\overline{\text{RESET}}$ CIRCUIT SECTION

Threshold Voltage "High" (static) "Low"		$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source T_{low} ≤ T_J ≤ T_{high} (Note 5) Power-Up $\overline{\text{RESET}}$ Watchdog Time Out Watchdog $\overline{\text{RESET}}$		I_{C5}	 −1.8 — —	 −2.5 5xI_{C5} −50xI_{C5}	 −3.2 — —	µA
Watchdog Input Voltage Swing		V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance		r_i	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)		t_p	—	—	10	µs
DIGITAL PORTS: $\overline{\text{WDS}}$, INH 1, INH 2, $\overline{\text{RESET}}$ (Note 8)						
Input Voltage Range		V_{INP}	—	—	−0.3 to V_{CC1}	V
Input HIGH Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ V_{IH} ≤ V_{CC1}		I_{IH}	 — —	 — —	 100 150	µA
Input LOW Current −0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, −0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{\text{WDS}}$		I_{IL}	 —	 —	 −100	µA
Leakage Current Immunity (INH2, High "Z" State)	12	I_Z	±20	—	—	µA
Output LOW Voltage $\overline{\text{RESET}}$ (I_{OL} = 6.0 mA)		V_{OL}	—	—	0.4	V
Output HIGH Current $\overline{\text{RESET}}$ (V_{OH} = 5.5 V)		V_{OH}	—	—	20	µA

NOTES:

8. Temperature range T_{low} ≤ T_J ≤ T_{high} applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (−2.5 V ≥ V_4 ≥ −5.5 V).

TYPICAL CHARACTERISTICS

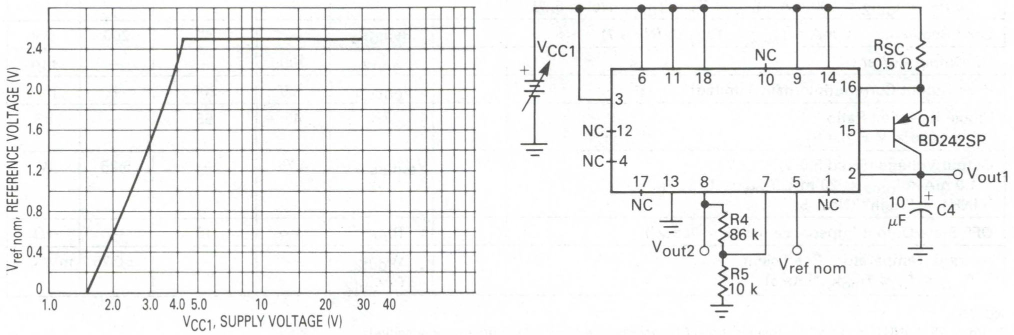


FIGURE 1 — REFERENCE VOLTAGE versus SUPPLY VOLTAGE

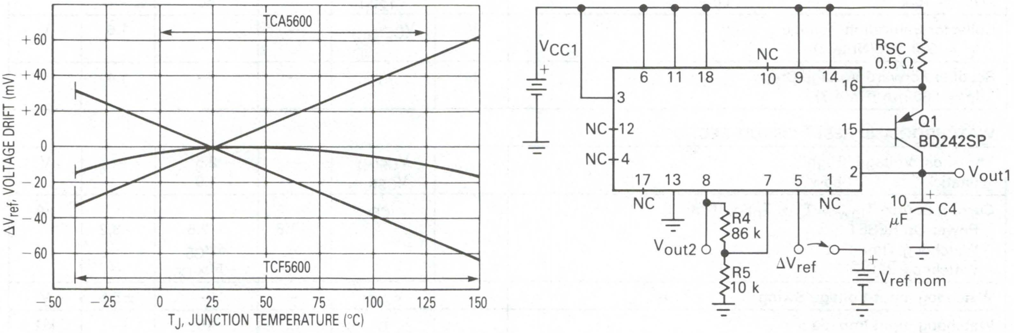


FIGURE 2 — REFERENCE STABILITY versus TEMPERATURE

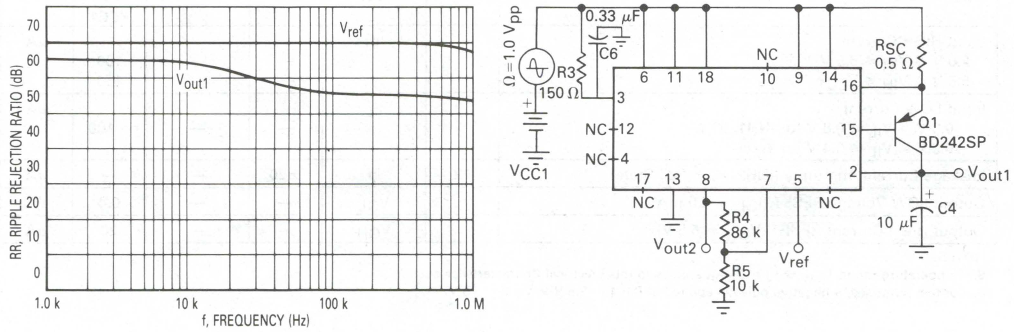


FIGURE 3 — RIPPLE REJECTION versus FREQUENCY

FIGURE 4 — STAND-BY CURRENT versus SUPPLY VOLTAGE

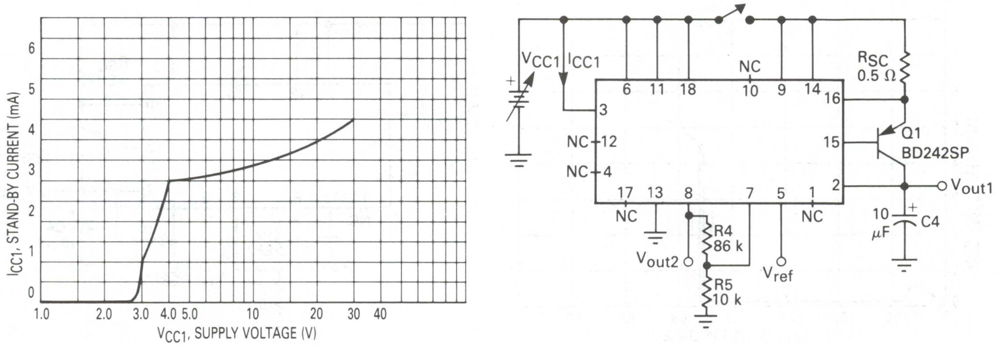


FIGURE 5 — POWER-UP BEHAVIOR OF THE 5.0 V REGULATOR

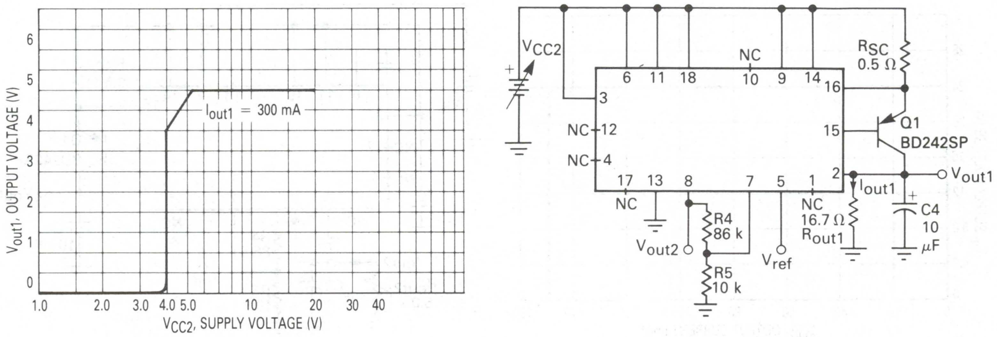


FIGURE 6 — FOLDBACK CHARACTERISTICS OF THE 5.0 V REGULATOR

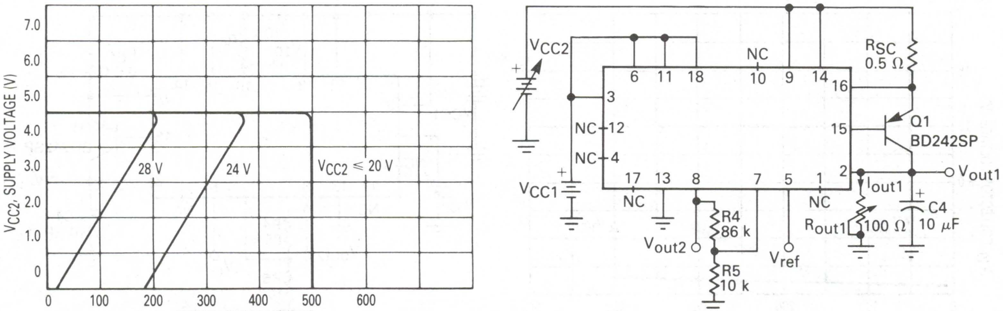


FIGURE 7 — UNDERVOLTAGE LOCKOUT CHARACTERISTICS

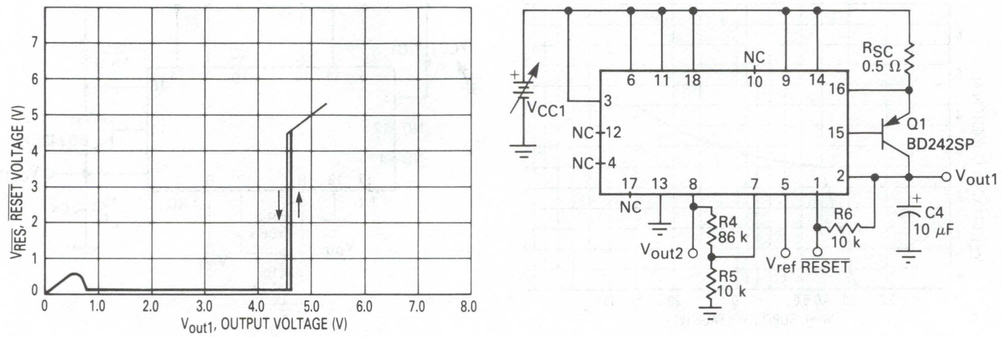


FIGURE 8 — OUTPUT CURRENT CAPABILITY OF THE PROGRAMMING REGULATOR

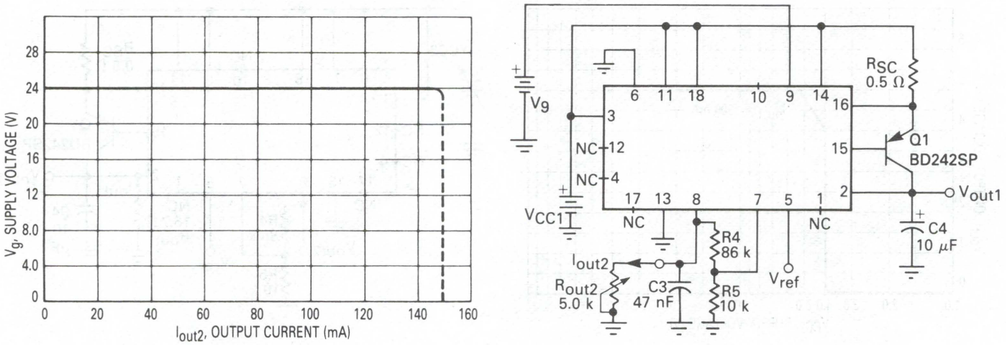


FIGURE 9 — COLLECTOR CURRENT DETECTION LEVEL

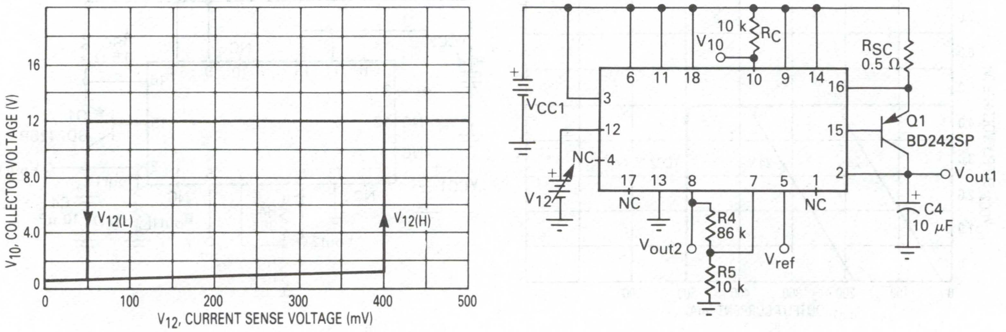


FIGURE 10 — POWER SWITCH CHARACTERISTICS

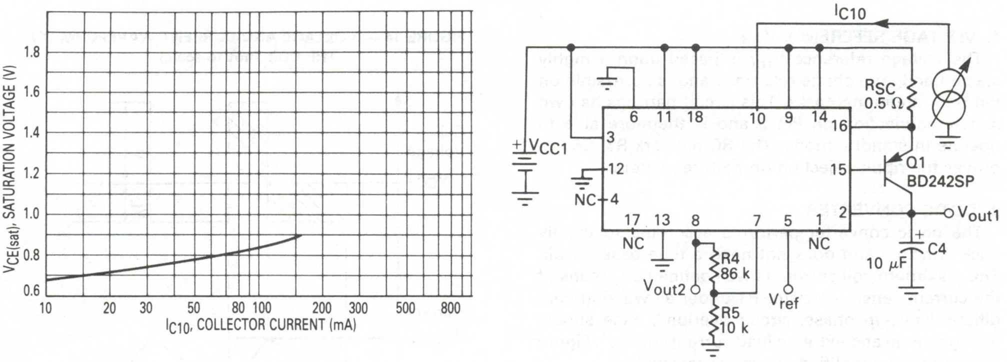


FIGURE 11 — RECTIFIER CHARACTERISTICS

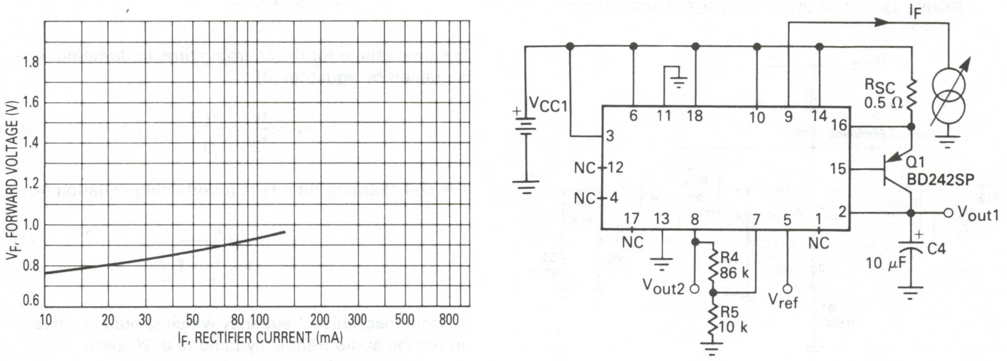
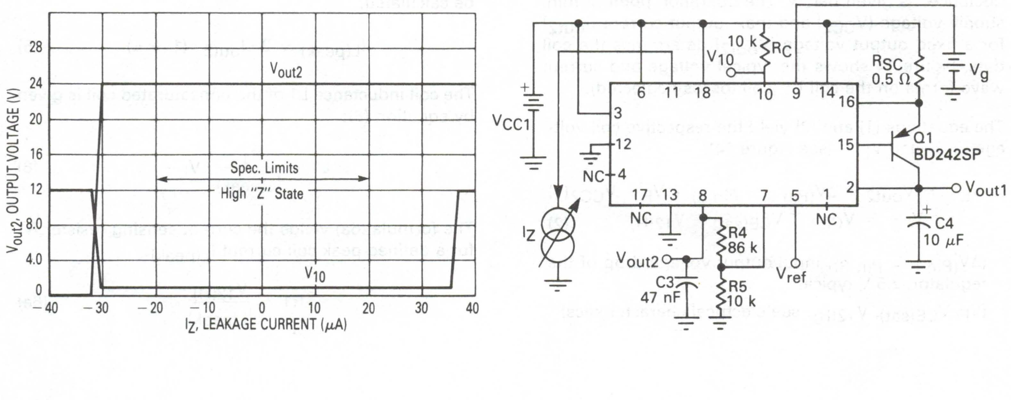


FIGURE 12 — INH 2 LEAKAGE CURRENT IMMUNITY



APPLICATIONS INFORMATION
(See Figure 18)

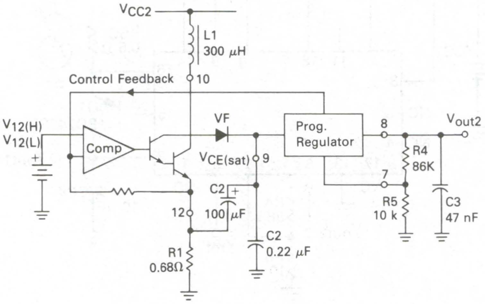
1. VOLTAGE REFERENCE V_{ref}

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is therefore able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

2. DC/DC CONVERTER

The dc/dc converter performs according to the fly back principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the simplified converter schematic:

FIGURE 13 — SIMPLIFIED CONVERTER SCHEMATIC



A simplified method on "how to calculate the coil inductance" is given below. The operation point at min. supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current wave forms on the coil L1 (coil losses neglected).

The equations (1) and (2) yield the respective coil voltage V_L- and V_L+ (see Figure 14):

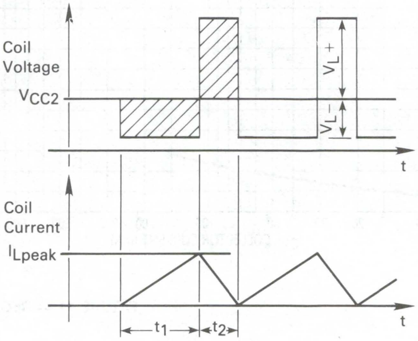
$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

($\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical)

(V_F, $V_{CE(sat)}$, $V_{12(H)}$: see electrical characteristics)

FIGURE 14 — VOLTAGE AND CURRENT WAVEFORM ON THE COIL (not to scale)



The time ratio α for the charging time to dumping time is defined by equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

The coil charging time t_1 is found using equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

(f : min. oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz))

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot I_{out2} \cdot (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} \cdot V_L- \quad (6)$$

The formula (6a) yields the current sensing resister R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

3. PROGRAMMABLE VOLTAGE REGULATOR

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage 6.0 V $\leqslant V_{out2} \leqslant$ 30 V.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \cdot R5}{V_{ref\ nom}} \qquad (7)$$

$$(R5 = 10\ k,\ V_{ref\ nom} = 2.5\ V)$$

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

4. CONTROL INPUTS INH1, INH2

The dc/dc converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a 3-level detector (Logic "0", high impedance "Z", Logic "1"). Both inputs are setup to provide the following truth table:

FIGURE 15 — INH1, INH2 TRUTH TABLE

Mode	INH1	INH2	V_{out2}	dc/dc
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.

ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.

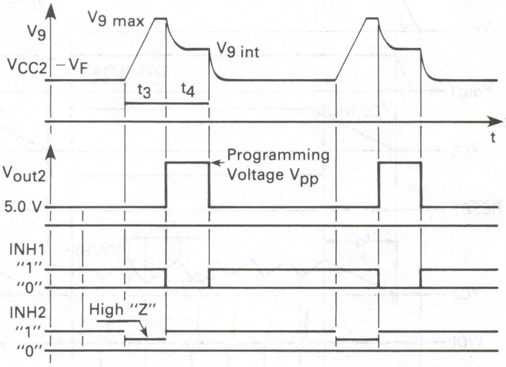
OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The high "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

5. MICROPROCESSOR SUPLY REGULATOR

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxilliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1 amp.

FIGURE 16 — TYPICAL E²PROM PROGRAMMING SEQUENCE (not to scale)



The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor R_{SC}.

$$R_{SC} = \frac{V_{RSC}}{I_E} \qquad (8)$$

(I_E: emitter current of Q1)

(V_{RSC}: threshold voltage (see electrical characteristics))

The voltage protection circuit performs a fold-back characteristic above a nominal operating voltage $V_{CC2} \geqslant$ 18 V.

6. DELAY AND WATCHDOG CIRCUIT

The under voltage monitor supervises the power supply V_{out1} and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating range (e.g. $V_{LOW} \geqslant 0.93 \cdot V_{out1(nom)}$). The $\overline{RESET}$ output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the typical $\overline{RESET}$ timing diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the equations (9) to (11).

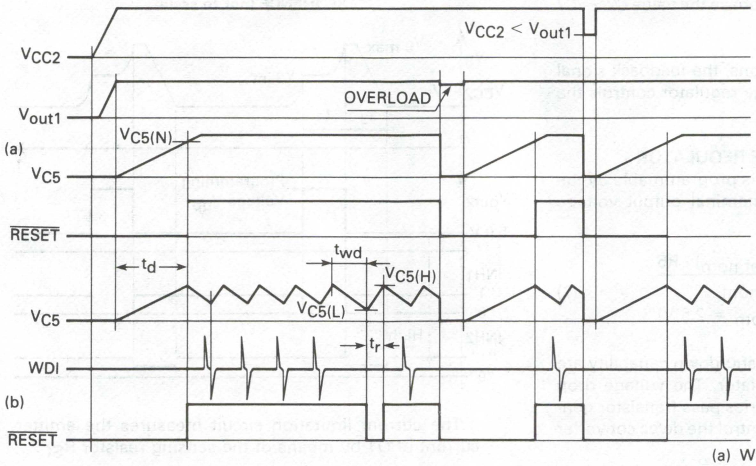
$\overline{RESET}$ delay: $$t_d = \frac{C5 \cdot V_{C5(H)}}{|I_{C5}|} \qquad (9)$$

Watchdog time-out: $$t_{wd} = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{5 \cdot I_{C5}} \qquad (10)$$

Watchdog $\overline{RESET}$: $$t_r = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{50 \cdot |I_{C5}|} \qquad (11)$$

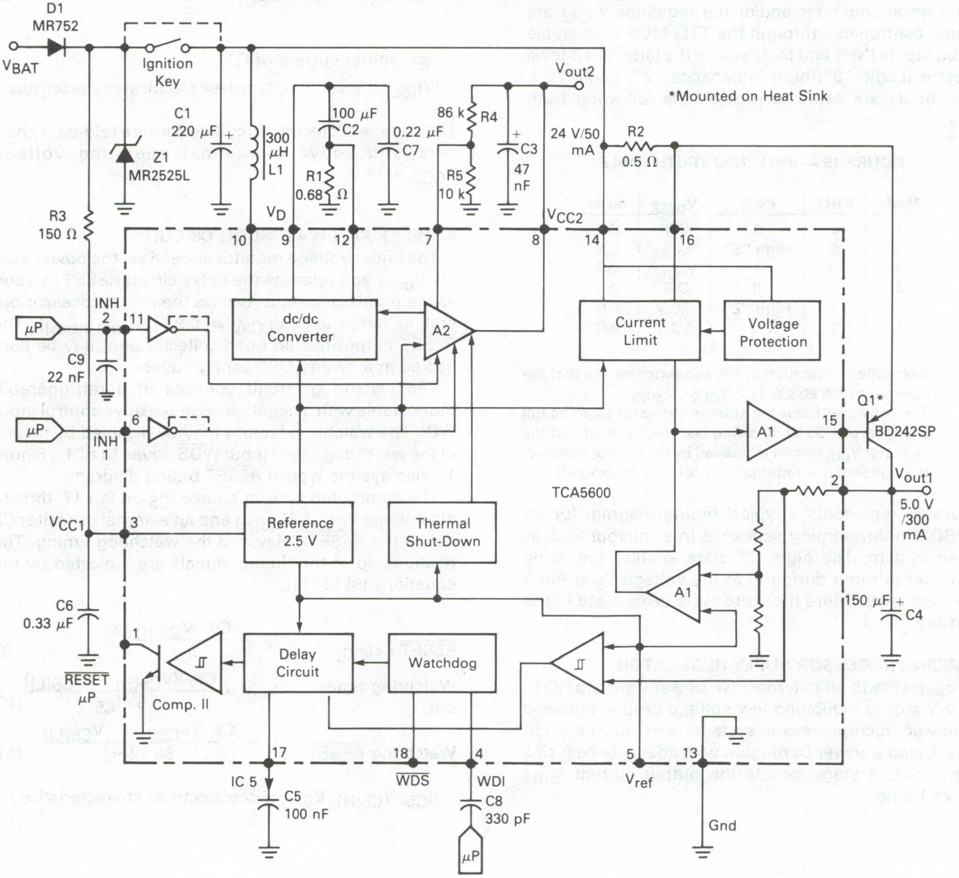
(I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see electrical characteristics.)

FIGURE 17 — TYPICAL $\overline{\text{RESET}}$ TIMING DIAGRAM
(not to scale)


V_{CC2}
$V_{CC2} < V_{out1}$
V_{out1}
OVERLOAD
(a)
$V_{C5(N)}$
V_{C5}
$\overline{\text{RESET}}$
t_d
t_{wd}
$V_{C5(H)}$
V_{C5}
$V_{C5(L)}$
t_r
WDI
(b)
$\overline{\text{RESET}}$

(a) Watchdog inhibited, $\overline{\text{WDS}}$ = "1"
(b) Watchdog operational, $\overline{\text{WDS}}$ = "0"

FIGURE 18 — TYPICAL AUTOMOTIVE APPLICATION


D1
MR752
V_{BAT}
Ignition Key
C1
220 μF
Z1
MR2525L
300 μH
L1
100 μF
C2
R1
0.68 Ω
0.22 μF
C7
86 k
R4
R5
10 k
C3
47 nF
V_{out2}
*Mounted on Heat Sink
24 V/50 mA
R2
0.5 Ω
R3
150 Ω
V_D
10
9
12
7
8
V_{CC2}
14
16
INH
2
11
μP
C9
22 nF
dc/dc Converter
A2
Current Limit
Voltage Protection
μP
6
INH
1
A1
15
Q1*
BD242SP
TCA5600
2
V_{out1}
5.0 V /300 mA
V_{CC1}
3
Reference 2.5 V
Thermal Shut-Down
A1
150 μF
C4
C6
0.33 μF
1
$\overline{\text{RESET}}$
μP
Comp. II
Delay Circuit
Watchdog
17
18
4
5
13
IC 5
$\overline{\text{WDS}}$
WDI
V_{ref}
C5
100 nF
C8
330 pF
μP
Gnd

MOTOROLA

TDA4600

Specifications and Applications Information

CONTROL IC FOR LINE ISOLATED FREELY OSCILLATING FLYBACK CONVERTER

The bipolar integrated circuit TDA4600 drives, regulates and monitors the switching transistor in a power supply based on freely oscillating flyback converters.

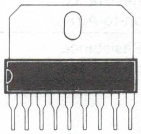
Due to the wide regulating range and the high voltage stability during large load changes, SMPS for Hi-Fi equipment and active loudspeakers can be realized as well as applications in TV receivers and video recorders.

The TDA4600 is available in a 9-pin SIP plastic medium-power package. The ambient temperature during operation can be from −15°C to +85°C.

- Wide Operational Range
- High Voltage Stability Even at High Load Changes
- Direct Control of Switching Transistor
- Low Start-Up Current
- Linear Foldback of the Overload Characteristic
- Base Drive Proportional to the Current Through the Power Switching Transistor

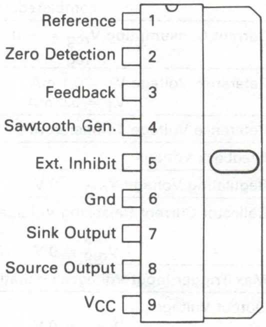
FLYBACK CONVERTER REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



SIP 9
PLASTIC
MEDIUM-POWER PACKAGE
CASE 762-01

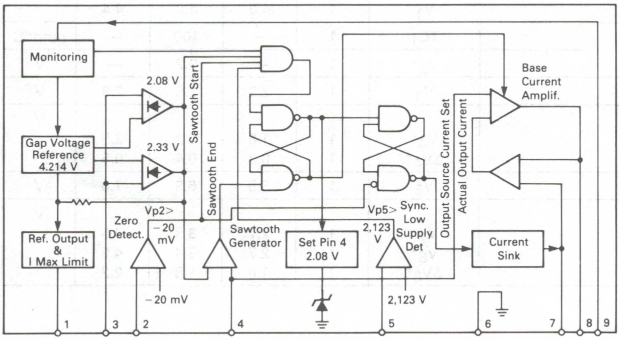
PIN CONNECTIONS


Reference 1
Zero Detection 2
Feedback 3
Sawtooth Gen. 4
Ext. Inhibit 5
Gnd 6
Sink Output 7
Source Output 8
VCC 9

ORDERING INFORMATION

Device	Temperature Range	Package
TDA4600	−15°C to +85°C	Plastic SIP

BLOCK DIAGRAM


Monitoring
2.08 V
2.33 V
Gap Voltage Reference 4.214 V
Ref. Output & I Max Limit
Sawtooth Start
Sawtooth End
Zero Detect.
Vp2>
−20 mV
−20 mV
Sawtooth Generator
Set Pin 4 2.08 V
Vp5>
2,123 V
Sync. Low Supply Det
2,123 V
Output Source Current Set
Actual Output Current
Base Current Amplif.
Current Sink
1
3
2
4
5
6
7
8
9

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_9	20	V
Sink Output Voltage	V_7	0 to V_9	V
Source Output	V_8 V_7-V_8	0 to V_9 ±6.0	V
Reference Output	I_1	−10 to +1.0	mA
Zero Passage	I_2	−3.0 to +3.0	mA
Control Amplifier	I_3	−3.0 to 0	mA
Collector Current Balancing	I_4	−2.0 to +5.0	mA
Trigger Input	I_5	−2.0 to +3.0	mA
Sink Output Current	I_7	−1.5	A
Source Output Current	I_8	1.5	A
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Thermal Resistance (Junction-to-Air)	$R_{\theta JA}$	70	°C/W
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	15	°C/W

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Operating Conditions	Symbol	Fig.	Min	Typ	Max	Unit
Supply Voltage	V_9		—	—	18	V
Ambient Temperature	T_A		−15	—	85	°C

START OPERATION

Current Consumption (V_1 not yet switched)	I_9	1	—	—	0.5	mA
V_9 = 3.0 V	I_9	1	—	1.5	2.0	mA
V_9 = 5.0 V	I_9	1	—	2.4	3.2	mA
V_9 = 10 V	V_9	1	11.3	11.8	12.3	V
Turn-on Point for V_1						

NORMAL OPERATION (V_9 = 10 V; V_{reg} = −10 V; V_{pulse} = ±0.5 V; f = 20 kHz; duty cycle: ½ after the turn-on process is completed.)

Current Consumption V_{reg} = −10 V V_{reg} = 0	I_9 I_9	1 1	110 55	135 85	160 110	mA
Reference Voltage V_1 < 0.1 mA V_1 = 5.0 mA	V_1 V_1	1 1	4.0 4.0	4.2 4.2	4.5 4.4	V
Reference Voltage Temperature Coefficient	TC_1	1	—	100	—	ppm/°C
Feedback Voltage	V_2*	1	—	0.2	—	V
Regulating Voltage V_{reg} = 0 V	V_3	1	2.3	2.6	2.9	V
Collector Current Balancing Voltage V_{reg} = 0 V V_{reg} = 0 V/−10 V	 V_4* ΔV_4*	 1 1	 1.8 0.3	 2.2 0.4	 2.5 0.5	V
Max Trigger Input Voltages Limitation	V_5	1	5.5	6.3	7.0	V
Output Voltages V_{reg} = 0 V V_{reg} = 0 V V_{reg} = 0 V/−10 V	 V_7* V_8* ΔV_8*	 1 1 1	 2.7 2.7 1.4	 3.3 3.4 1.8	 4.0 4.0 2.2	V

*Only dc portion.

PROTECTIVE OPERATION (V_9 = 10 V; V_{reg} = −10 V; V_{pulse} = ±0.5 V; f = 20 kHz; duty cycle: ½)

Current Consumption ($V_5 < 1.8$ V)	I_9	1	14	20	26	mA
Turn-off Voltage ($V_5 < 1.8$ V)	V_7	1	1.3	1.5	1.8	V
	V_4	1	1.8	2.1	2.5	
External Trigger Input						V
Enable Voltage (V_{reg} = 0 V)	V_5	1	—	2.4	2.7	
Disabled Voltage (V_{reg} = 0 V)	V_5	1	1.8	2.2	—	
Supply Voltage Disabling V_8 (V_{reg} = 0 V)	V_9	1	6.7	7.4	7.8	V

RANGE OF OPERATION

Turn-on Time (Secondary Voltages)	+on	2	—	350	450	ms
Voltage Change						mV
When S_3 = Closed (ΔP_3 = 19 W Audio Frequency Output Power)	ΔV_2	2	—	100	500	
When S_2 = Closed (ΔP_2 = 15 W)	ΔV_2	2	—	500	1000	
Standby Operation (Secondary Useable Power = 3.0 W)	ΔV_2	2	—	20	30	V
When S_1 = Open	f	2	70	75	—	kHz
	P_{prim}	2	—	10	12	VA

The heat sink must be optimized, taking the maximum data (T_J, $R_{\theta JC}$, $R_{\theta JA}$, T_A) into consideration.

FIGURE 1 — MEASURING CIRCUIT

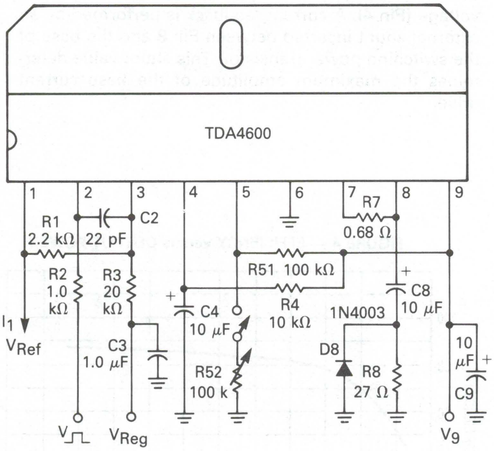
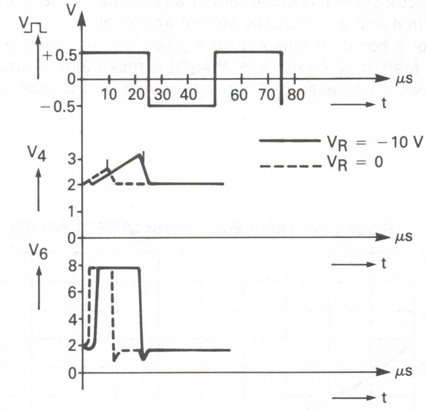


FIGURE 2 — TEST DIAGRAM: NORMAL OPERATION



CIRCUIT DESCRIPTION

The TDA4600 regulates, controls, and protects the switching transistor in flyback converter power supplies at starting, normal and overload operation.

A. Starting Behavior

At the start-up there are three consecutive operation states.

1. An internal reference voltage is created. It supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. For a supply voltage of V_9 = 12 V, the current I_9 is less than 3.2 mA.
2. Release of the internal reference voltage V_1 = 4.0 V. This voltage is available when V_9 = 12 V and

enables all parts of the IC to be supplied from the control logic with thermal and overload protection.

3. Release of control logic — As soon as the reference voltage is available, the control is switched on through an additional stabilization circuit.

This start-up sequence is necessary for driving the switching transistor through the coupling electrolytic capacitor.

B. Normal Operation

Zero crossing detection is sensed on Pin 2 and linked to the control logic.

The signal picked up on the feedback winding is applied, after filtering, to Pin 3 (used for input regulation and for overload protection). The regulating section works with an input voltage of about 2.0 V for normal regulation and a current of about 1.4 mA for foldback operation. Together with the collector current simulation Pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at Pin 4 and an internally set voltage level.

For a constant line and for a given output power on the load (t_{on} fixed) less than the maximum output power, a decrease of C Pin 4 produces an increase of the current sent to the base of the power switching transistor. So the foldback point is reached earlier. The regulation range starts from a 2.0 Vdc level which is the bottom of a sawtooth waveform whose top is limited at 4.0 V (reference voltage).

A secondary load of 19 W produces a switching frequency of about 50 kHz at an almost constant duty cycle. Furthermore, when the switchmode power supply delivers approximately 3.0 W, the switching frequency jumps to about 70 kHz. At the same time, the collector peak current falls below 1.0 A.

The comparison of the output level of the regulating amplifier, the overload detection and the collector current simulation drives the control logic. An additional steering control and blocking possibility is offered thru Pin 5. When the voltage applied on Pin 5 falls below 2.2 V, the source output (Pin 8) is blocked.

The control logic is set according to the start-up circuit, the zero crossing detection and the trigger enable. This logic drives the base current amplifier and the base current shutdown. The base current amplifier drives the source output (Pin 8) proportionally to the sawtooth voltage (Pin 4). A current feedback is performed by an external shunt inserted between Pin 8 and the base of the switching power transistor. This shunt value determines the maximum amplitude of the base current drive.

FIGURE 3 — FREQUENCY versus OUTPUT POWER

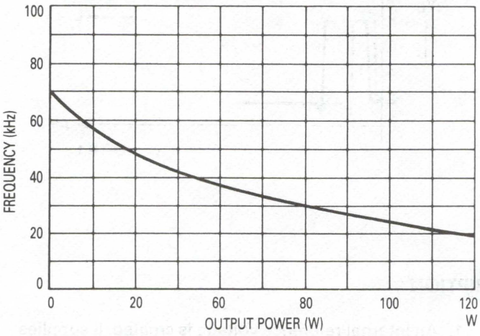
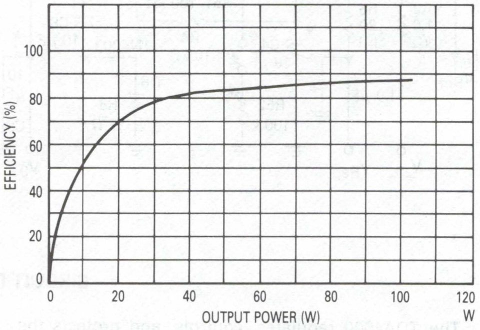


FIGURE 4 — EFFICIENCY versus OUTPUT POWER



C. Protective Features

The base current shutdown, released by the control logic, clamps the sink output (Pin 7) at 1.6 V, turning off the switching transistor. This feature will be released if the voltage on Pin 9 is less than 7.4 V, or if the applied voltage on Pin 5 is less than 2.2 V. In case of a short circuit of the secondary windings, the TDA4600 continuously monitors the fault condition.

In standby operation the circuit is set to a high duty cycle. The total power consumption of the power supply is held below 6.0 to 10 W. Once the output is blocked (due to the supply voltage coming down to 7.4 V), a further voltage reduction to 6.0 V switches off the reference voltage.

FIGURE 5 — LOAD CHARACTERISTICS ($V_2 = f(I_{q2})$)

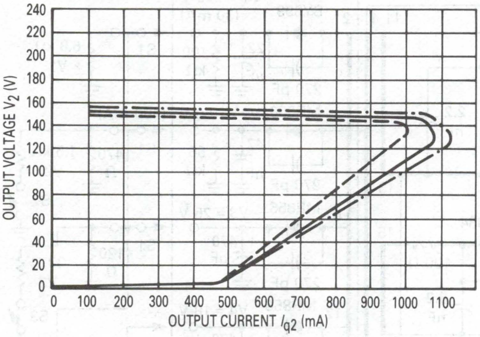
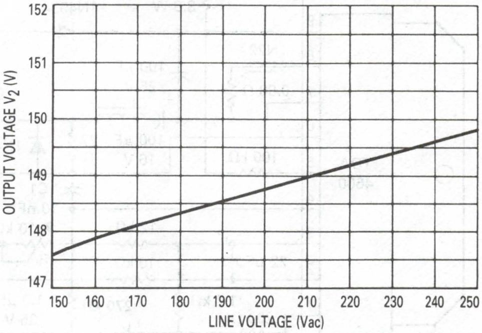


FIGURE 6 — OUTPUT VOLTAGE V_2 (line change)



TEST CIRCUIT AND TYPICAL APPLICATION (see Figure 7 on the next page)

This application circuit shown in Figure 7 represents a blocking converter for color TV sets with 30 W to 120 W of output power and line voltages from 160 V to 270 V.

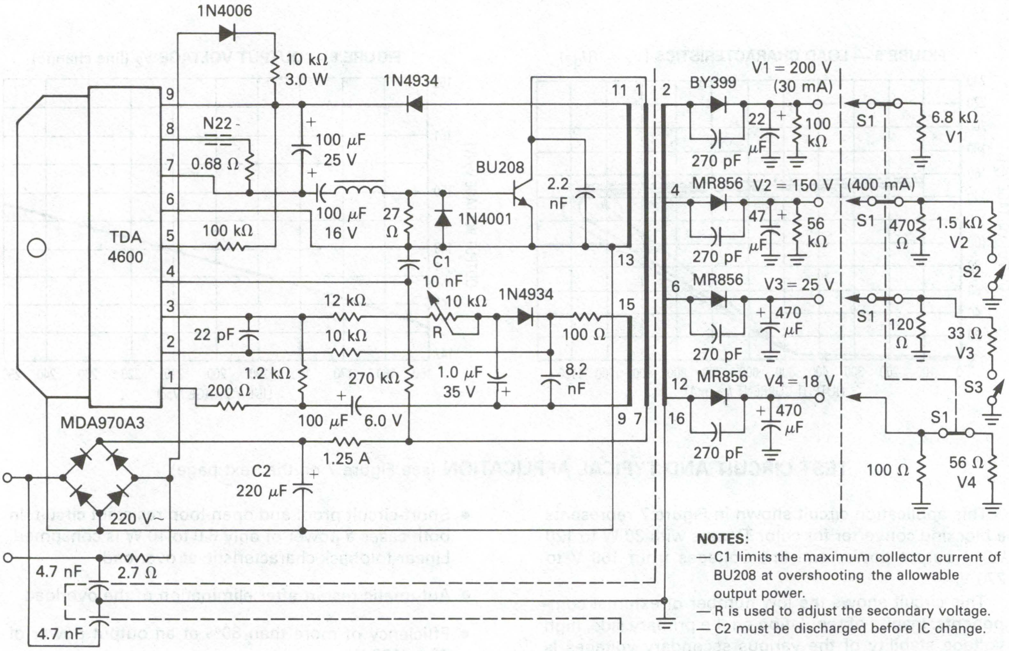
This circuit shows the low number of external components. Inspite of regulation on the primary side, high voltage stability of the various secondary voltages is achieved even with large load changes.

For line isolation and transformation to the desired secondary voltages, a transformer with ferrite core is used.

SPECIAL FEATURES OF THE FLYBACK CONVERTER POWER SUPPLY USING THE TDA4600

- Direct driving of the power switching transistor
- Low starting current, defines starting behavior even at slowly rising line voltage
- Short-circuit proof and open-loop resistant circuit. In both cases a power of only 6.0 to 10 W is consumed. Linear foldback characteristic at overload
- Automatic restart after elimination of the overload
- Efficiency of more than 80% at an output power of 40 to 100 W
- Frequency of ocillation between 20 kHz (100 W) and 70 kHz (without load)
- Simple RF I suppression
- Good regulation of load current and line voltage variations. At a line voltage variation between 170 and 240 Vac the output voltage of 150 V will change only by about 2.0 V

FIGURE 7 — TYPICAL APPLICATION


1N4006
10 kΩ
3.0 W
1N4934
9
8
7
6
5
4
3
2
1
N22
0.68 Ω
TDA
4600
100 kΩ
100 µF
25 V
100 µF
16 V
27
Ω
1N4001
BU208
2.2
nF
C1
10 nF
10 kΩ
R
1N4934
12 kΩ
10 kΩ
22 pF
1.2 kΩ
200 Ω
270 kΩ
1.0 µF
35 V
100 Ω
8.2
nF
100 µF
6.0 V
1.25 A
C2
220 µF
MDA970A3
220 V~
4.7 nF
2.7 Ω
4.7 nF
11
1
2
13
15
9
7
4
6
12
16
BY399
MR856
MR856
MR856
V1 = 200 V
(30 mA)
22
µF
100
kΩ
270 pF
V2 = 150 V
(400 mA)
47
µF
56
kΩ
270 pF
V3 = 25 V
470
µF
270 pF
V4 = 18 V
470
µF
270 pF
S1
6.8 kΩ
V1
S1
470
Ω
1.5 kΩ
V2
S2
S1
120
Ω
33 Ω
V3
S3
S1
100 Ω
56 Ω
V4

NOTES:

— C1 limits the maximum collector current of BU208 at overshooting the allowable output power.

— R is used to adjust the secondary voltage.

— C2 must be discharged before IC change.

MOTOROLA

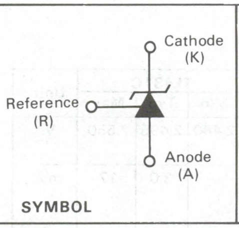
TL431 Series

Specifications and Applications Information

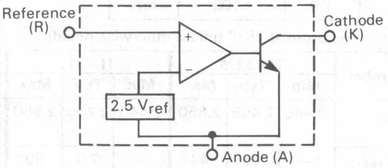
PROGRAMMABLE PRECISION REFERENCES

The TL431 integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

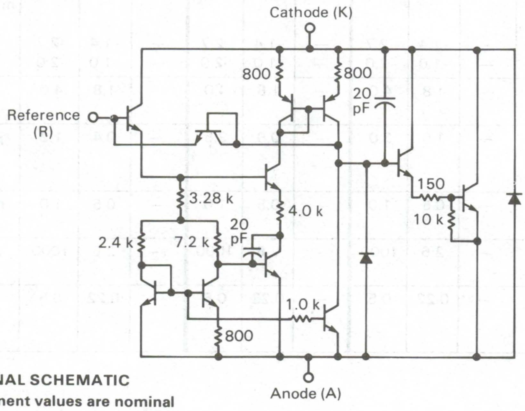
- Programmable Output Voltage to 36 Volts
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage


Cathode
(K)
Reference
(R)
Anode
(A)

SYMBOL


Reference
(R)
Cathode
(K)
+
−
2.5 V_{ref}
Anode (A)

FUNCTIONAL BLOCK DIAGRAM

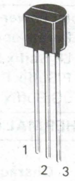

Cathode (K)
800
800
20
pF
Reference
(R)
3.28 k
4.0 k
150
10 k
2.4 k
7.2 k
20
pF
1.0 k
800
Anode (A)

INTERNAL SCHEMATIC
Component values are nominal

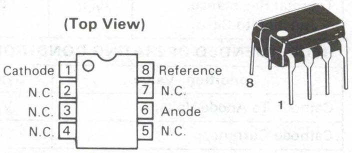
PROGRAMMABLE PRECISION REFERENCES

SILICON MONOLITHIC INTEGRATED CIRCUITS

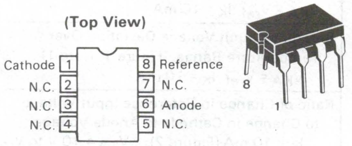
LP SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)



Pin 1. Reference
2. Anode
3. Cathode


(Top View)
Cathode 1
N.C. 2
N.C. 3
N.C. 4
8 Reference
7 N.C.
6 Anode
5 N.C.
8
1

P SUFFIX
PLASTIC DUAL-IN-LINE PACKAGE
CASE 626-04


(Top View)
Cathode 1
N.C. 2
N.C. 3
N.C. 4
8 Reference
7 N.C.
6 Anode
5 N.C.
8
1

JG SUFFIX
CERAMIC DUAL-IN-LINE PACKAGE
CASE 693-02

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP	0 to +70°C	Plastic TO-92
TL431CP	0 to +70°C	Plastic DIP
TL431CJG	0 to +70°C	Ceramic DIP
TL431ILP	−40 to +85°C	Plastic TO-92
TL431IP	−40 to +85°C	Plastic DIP
TL431IJG	−40 to +85°C	Ceramic DIP
TL431MJG	−55 to +125°C	Ceramic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	-100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	-0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I TL431C	T_A	 -55 to +125 -40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C Ambient Temperature LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.775 1.10 1.25	W
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C Case Temperature LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

THERMAL CHARACTERISTICS

Characteristics	Symbol	LP Suffix Package	P Suffix Package	JG Suffix Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, $I_K = 10$ mA	V_{ref}	2.440	2.495	2.550	2.440	2.495	2.550	2.440	2.495	2.550	V
Reference Input Voltage Deviation Over Temperature Range. (Figure 1, Note 1) $V_{KA} = V_{ref}$, $I_K = 10$ mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_K = 10$ mA (Figure 2), $\Delta V_{KA} = 10$ V to V_{ref} $\Delta V_{KA} = 36$ V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 -1.4 -1.0	 -2.7 -2.0	 — —	 -1.4 -1.0	 -2.7 -2.0	 — —	 -1.4 -1.0	 -2.7 -2.0	mV/V
Reference Input Current (Figure 2) $I_K = 10$ mA, R1 = 10 k, R2 = ∞	I_{ref}	—	1.8	4.0	—	1.8	4.0	—	1.8	4.0	μA
Reference Input Current Deviation Over Temperature Range. (Figure 2) $I_K = 10$ mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) $V_{KA} = 36$ V, $V_{ref} = 0$ V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 2) $V_{KA} = V_{ref}$, $\Delta I_K = 1.0$ mA to 100 mA $f \leqslant 1.0$ kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

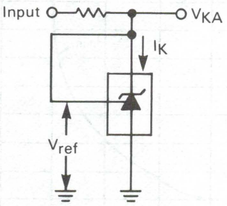
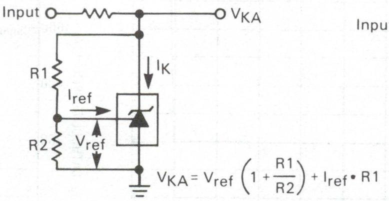
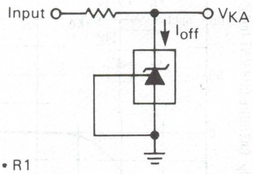


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$



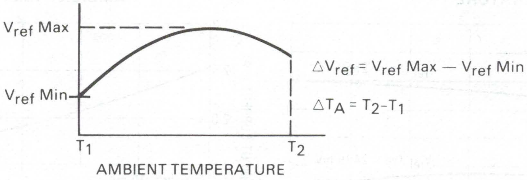
$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \bullet R1$$

FIGURE 3 — TEST CIRCUIT FOR I_{off}



Note 1

The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, $\alpha\ V_{ref}$, is defined as:

$$\alpha\ V_{ref}\ \frac{\text{ppm}}{°\text{C}} = \frac{\left(\dfrac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\,(V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: $\Delta V_{ref} = 8.0$ mV and slope is positive, V_{ref} @ 25°C = 2.495 V, $\Delta T_A = 70°C$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\,(2.495)} = 45.8\ \text{ppm}/°\text{C}$$

Note 2

The dynamic impedance Z_{ka} is defined as:

$$|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}'| \approx |Z_{ka}|\left(1 + \frac{R1}{R2}\right)$$

FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

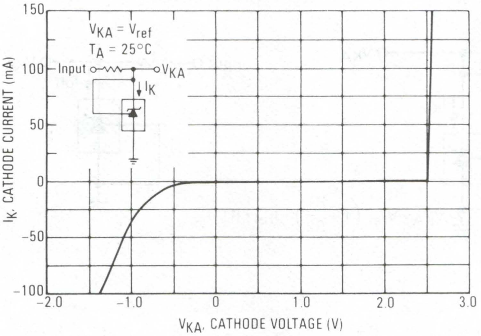


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

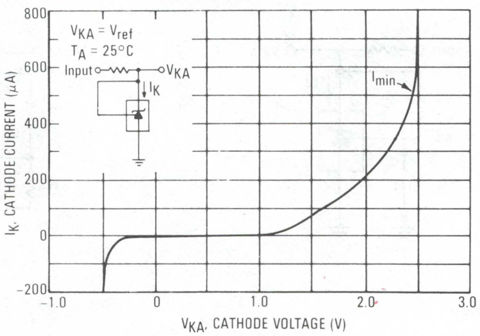


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

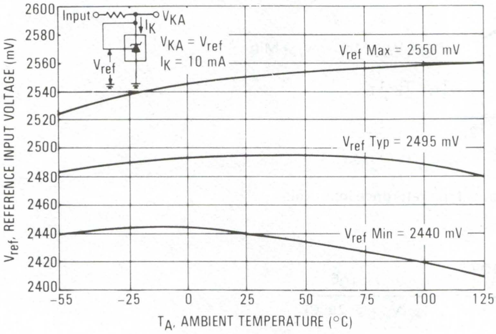


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

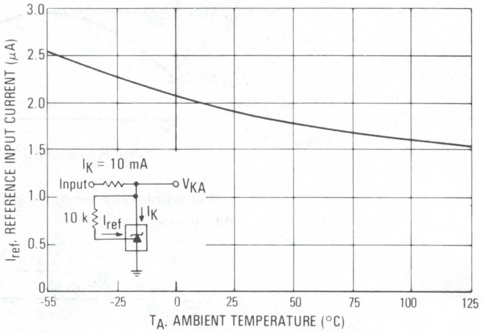


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

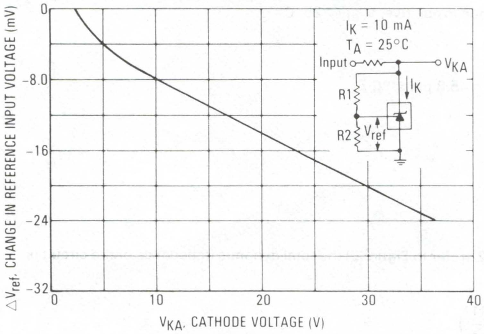


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

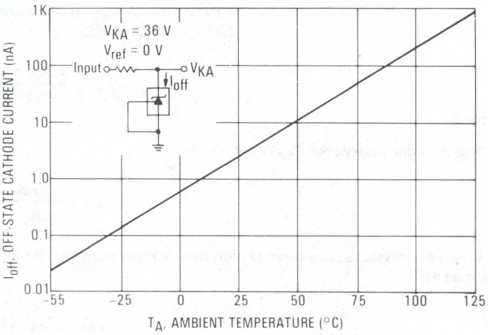


FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY

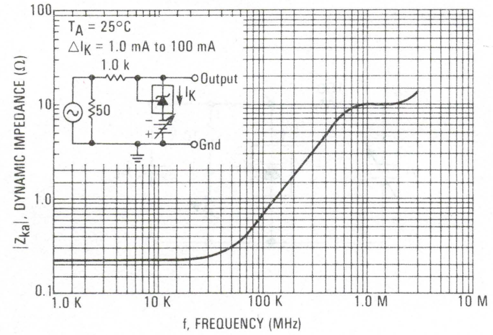


FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE

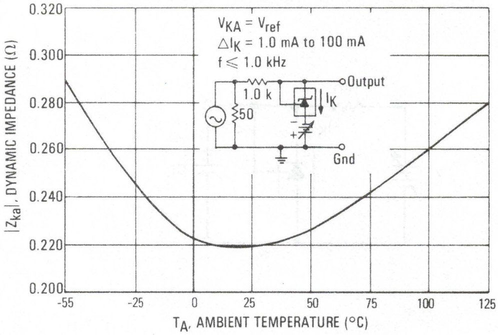


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

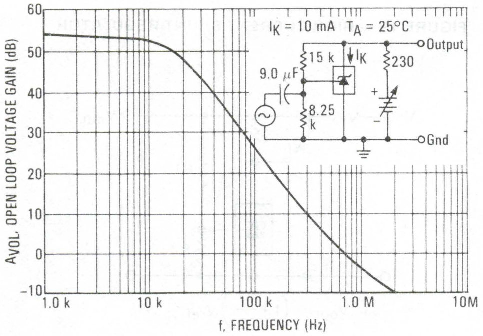


FIGURE 13 — SPECTRAL NOISE DENSITY

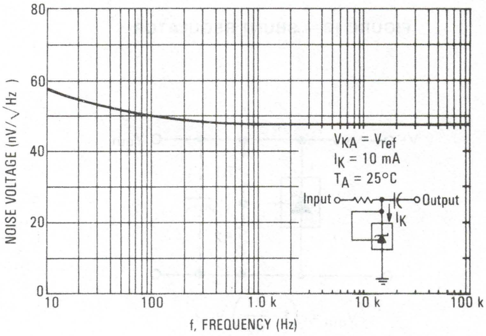


FIGURE 14 — PULSE RESPONSE

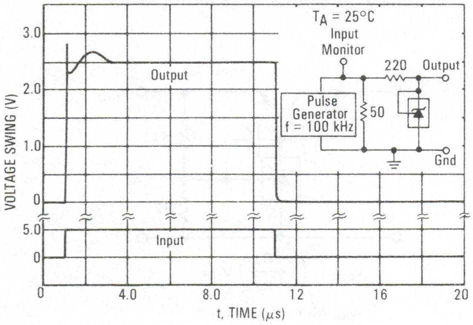


FIGURE 15 — STABILITY BOUNDARY CONDITIONS

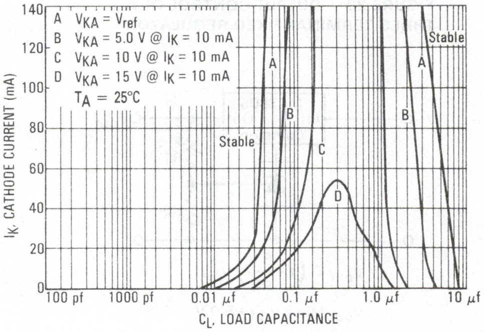


FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

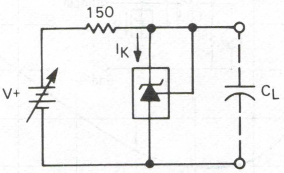
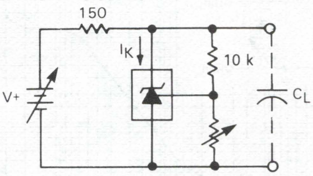
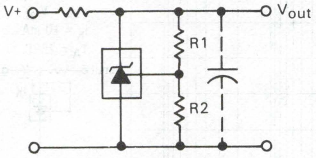


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS


150
I_K
10 k
V+
C_L

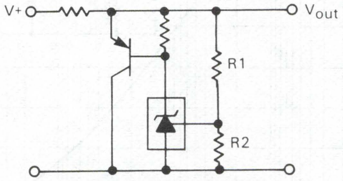
TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR



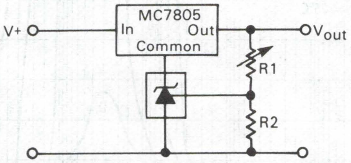
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 19 — HIGH CURRENT SHUNT REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

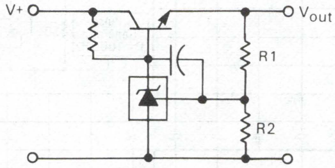
FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR


MC7805
In
Out
Common
V+
V_{out}
R1
R2

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + 5.0 V

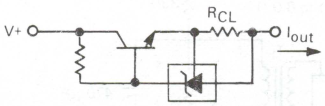
FIGURE 21 — SERIES PASS REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

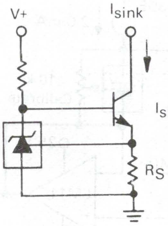
V_{out} Min = V_{ref} + 5.0 V

FIGURE 22 — CONSTANT CURRENT SOURCE



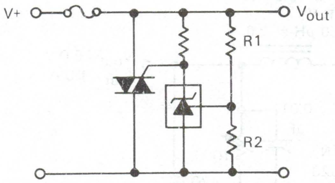
$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

FIGURE 23 — CONSTANT CURRENT SINK



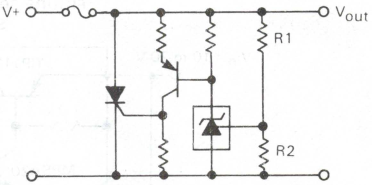
$$I_{sink} = \frac{V_{ref}}{R_S}$$

FIGURE 24 — TRIAC CROWBAR



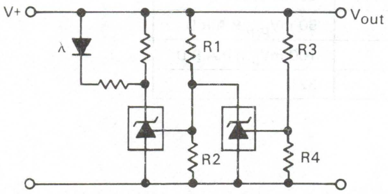
$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 25 — SCR CROWBAR



$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 26 — VOLTAGE MONITOR

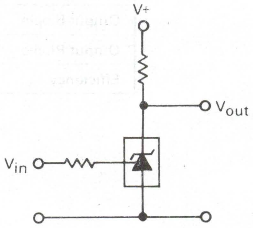

V+
V_{out}
λ
R1
R3
R2
R4

L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



$V_{th} = V_{ref}$

V_{in}	V_{out}
$<V_{ref}$	V+
$>V_{ref}$	≈ 2.0 V

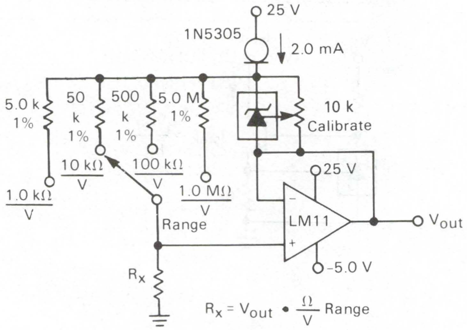

25 V
1N5305
2.0 mA
5.0 k 1%
50 k 1%
500 k 1%
5.0 M 1%
10 k Calibrate
25 V
1.0 kΩ/V
10 kΩ/V
100 kΩ/V
1.0 MΩ/V
Range
LM11
Vout
-5.0 V
Rx
Rx = Vout • Ω/V Range

FIGURE 28 — LINEAR OHMMETER

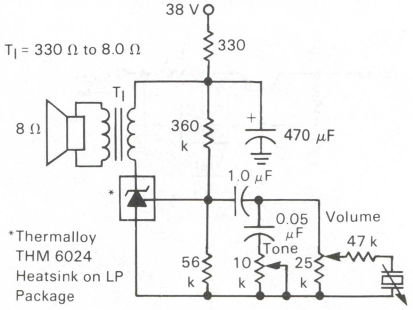

38 V
330
TI = 330 Ω to 8.0 Ω
TI
8 Ω
360 k
470 µF
1.0 µF
*
0.05 µF
Tone
Volume
47 k
56 k
10 k
25 k
*Thermalloy THM 6024 Heatsink on LP Package

FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

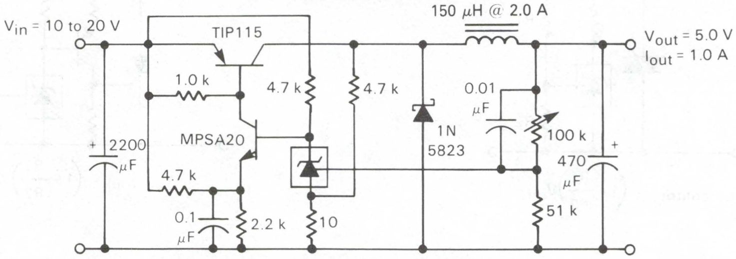

150 µH @ 2.0 A
Vin = 10 to 20 V
TIP115
Vout = 5.0 V
Iout = 1.0 A
1.0 k
4.7 k
4.7 k
0.01 µF
1N 5823
100 k
MPSA20
2200 µF
470 µF
4.7 k
51 k
0.1 µF
2.2 k
10

FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%

MOTOROLA

TL494
TL495

Specifications and Applications Information

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

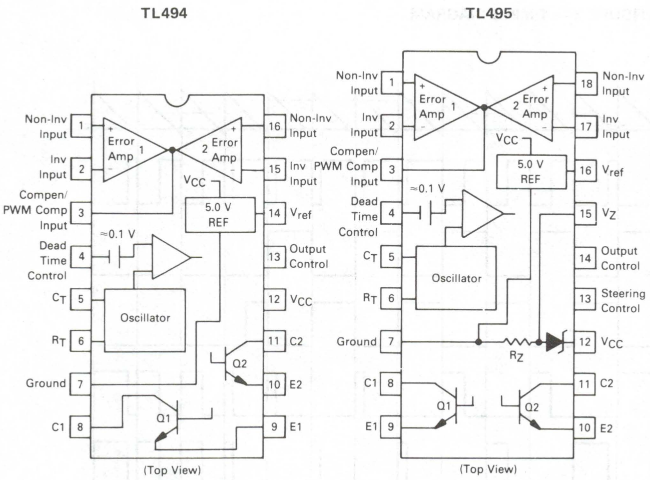
SILICON MONOLITHIC INTEGRATED CIRCUITS

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 and TL495 are fixed frequency, pulse width modulation control circuits designed primarily for Switchmode power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors For 200 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- On-Chip 39 Volt Zener (TL495 Only)
- Output Steering Control (TL495 Only)

PIN CONNECTIONS

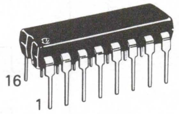

TL494

TL495

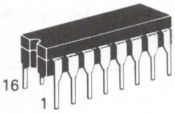
Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead Time Control 4
C_T 5
R_T 6
Ground 7
C1 8
16 Non-Inv Input
15 Inv Input
14 V_{ref}
13 Output Control
12 V_{CC}
11 C2
10 E2
9 E1
Error Amp 1
2 Error Amp
V_{CC}
5.0 V REF
≈0.1 V
Oscillator
Q1
Q2
Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead Time Control 4
C_T 5
R_T 6
Ground 7
C1 8
E1 9
18 Non-Inv Input
17 Inv Input
16 V_{ref}
15 V_Z
14 Output Control
13 Steering Control
12 V_{CC}
11 C2
10 E2
R_Z

(Top View) (Top View)

TL494

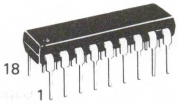


N SUFFIX
PLASTIC PACKAGE
CASE 648-05

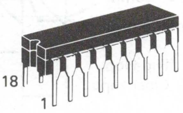


J SUFFIX
CERAMIC PACKAGE
CASE 620-02

TL495



N SUFFIX
PLASTIC PACKAGE
CASE 707-02



J SUFFIX
CERAMIC PACKAGE
CASE 726-01

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0 To 70°C	Plastic DIP
TL494CJ	0 To 70°C	Ceramic DIP
TL494IN	−25 To 85°C	Plastic DIP
TL494IJ	−25 To 85°C	Ceramic DIP
TL494MJ	−55 To 125°C	Ceramic DIP
TL495CN	0 To 70°C	Plastic DIP
TL495CJ	0 To 70°C	Ceramic DIP
TL495IN	−25 To 85°C	Plastic DIP
TL495IJ	−25 To 85°C	Ceramic DIP

The TL494C/495C are specified over the commercial operating range of 0°C to 70°C. The TL494I/495I are specified over the industrial range of −25°C to 85°C. The TL494M is specified over the full military range of −55°C to 125°C.

FIGURE 1 — BLOCK DIAGRAM

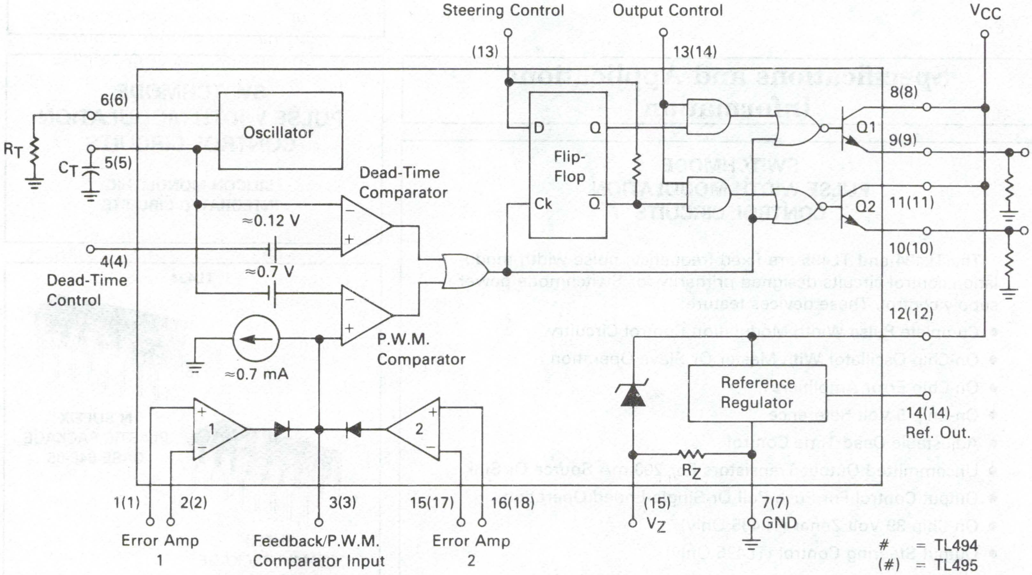
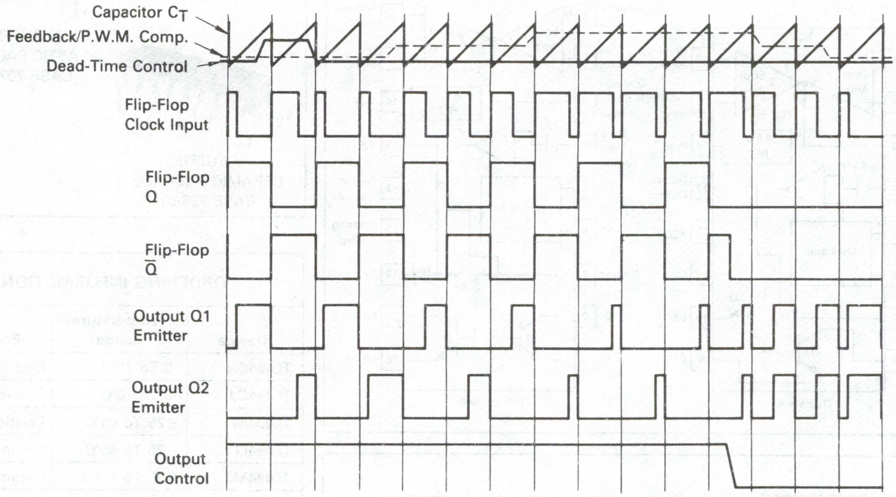

Steering Control
(13)
Output Control
13(14)
V_{CC}
8(8)
9(9)
Q1
Q2
11(11)
10(10)
12(12)
6(6)
Oscillator
R_T
C_T
5(5)
Dead-Time Comparator
≈0.12 V
≈0.7 V
4(4)
Dead-Time Control
D
Q
Flip-Flop
Ck
$\overline{Q}$
P.W.M. Comparator
≈0.7 mA
Reference Regulator
14(14)
Ref. Out.
R_Z
1
2
1(1)
2(2)
3(3)
15(17)
16(18)
(15)
V_Z
7(7)
GND
Error Amp 1
Feedback/P.W.M. Comparator Input
Error Amp 2
# = TL494
(#) = TL495

FIGURE 2 — TIMING DIAGRAM



Description

The TL494/495 are fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494/495 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an accuracy of ±5% with a thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

The TL495 contains an on-chip 39 volt zener diode for high voltage applications where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop. (Refer to the functional table shown in Figure 3.)

FIGURE 3 — FUNCTIONAL TABLE

Inputs		Output Function	$\frac{f_{out}}{f_{osc}}$ =
Output Control	Steering Control		
Grounded	Open	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Open	Push-pull operation	0.5
At V_{ref}	V1 <0.4 V	Single-ended P.W.M. at Q1 only	1
At V_{ref}	V1 >2.4 V	Single-ended P.W.M. at Q2 only	1

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	TL494M	TL494I/TL495I	TL494C/TL495C	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor)	I_{C1}, I_{C1}	250	250	250	mA
Amplifier Input Voltage	V_{in}	V_{CC} + .03	V_{CC} + .03	V_{CC} + .03	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature	T_J	150	150	150	°C
Operating Ambient Temperature Range	T_A	−55 to 125	−25 to 85	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	J Suffix Ceramic Package	N Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	°C/W
Power Derating Factor	$1/R_{\theta JA}$	10.0	12.5	mW/°C
Derating Ambient Temperature	T_A	50	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494/TL495 Min	 Typ	 Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	$I_{f.b.}$	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.47	1.0	10,000	nF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, f_{osc} = 10 kHz unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494M Min	 Typ	 Max	TL494C, I/TL495C,I Min	 Typ	 Max	Unit
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Reference Voltage Change with Temperature (ΔT_A = Min to Max)	ΔV_{ref} (ΔT)	—	0.2	2.0	—	1.3	2.6	%
Input Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Output Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V, T_A = 25°C)	I_{SC}	10	35	50	—	35	—	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, f_{osc} = 10 kHz unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494M			TL494C, I/TL495C, I			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−150	—	—	−100	μA
Collector-Emitter Saturation Voltage Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.5	—	1.1	1.3	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State ($V_{OC} \leqslant$ 0.4 V)	I_{OCL}	—	10	—	—	10	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time (T_A = 25°C) Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time (T_A = 25°C) Common-Emitter (See Figure 13)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL494/TL495			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	0.1	1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 7.0 V to 40 V)	V_{ICR}	−0.3	—	V_{CC} − 2.0	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	$\emptyset m$	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O+	−2.0	−4.0	—	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, f_{osc} = 10 kHz unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494/TL495 Min	 Typ	 Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero duty cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_{I-}	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB\ (DT)}$	—	−2.0	−10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode (V_{in} = 0 V, C_T = 0.1 μF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.1	—	%
Frequency Change with Temperature (ΔT_A = T_{Alow} to T_{Ahigh})	Δf_{osc} (ΔT)	—	±1.0	±2.0	%

Characteristic	Symbol	TL495 Min	 Typ	 Max	Unit
STEERING CONTROL					
Input Current Low ($V_{(Pin\ 13)}$ = 0.4 V)	I_{STL}	—	−25	−200	μA
Input Current High ($V_{(Pin\ 13)}$ = 2.4 V) ($V_{(Pin\ 13)}$ = V_{ref})	I_{STH}	 — —	 25 75	 200 —	μA
ZENER CHARACTERISTICS					
Zener Breakdown Voltage (I_Z = 2.0 mA)	V_Z	—	39	—	V
Sink Current ($V_{(Pin\ 15)}$ = 1.0 V)	I_{RZ}	—	0.3	—	mA
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{(Pin\ 4)}$ = 2.0 V) (See Figure 12.) (C_T = 0.001, R_T = 12 kΩ, V_{CC} = 15 V)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\dfrac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

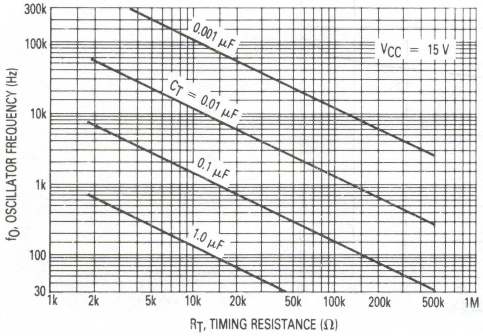


FIGURE 5 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

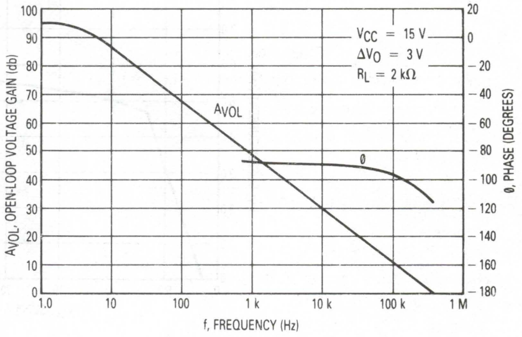


FIGURE 6 — PERCENT DEAD TIME versus OSCILLATOR FREQUENCY

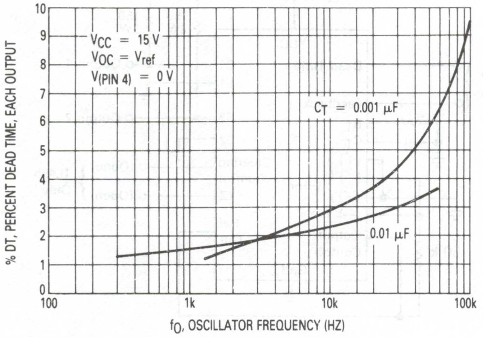


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

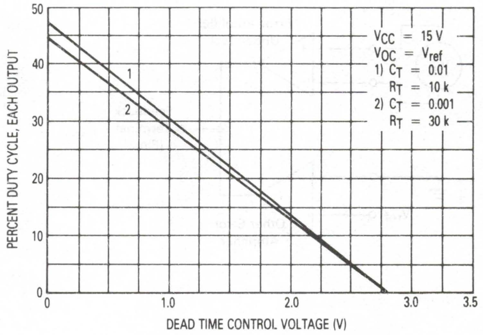


FIGURE 8 — EMITTER-FOLLOWER CONFIGURATION, OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT

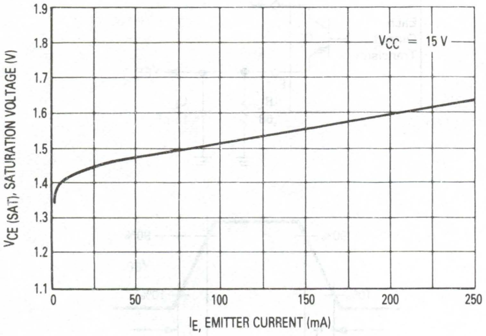


FIGURE 9 — COMMON-EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus COLLECTOR CURRENT

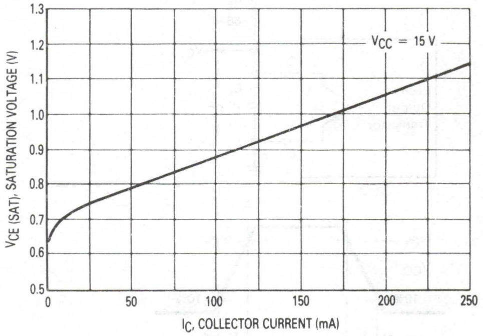


FIGURE 10 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

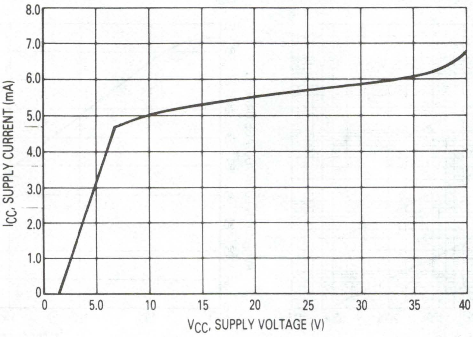


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

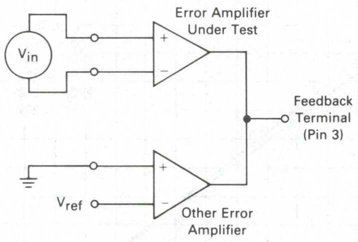

Vin
Error Amplifier
Under Test
+
−
Feedback
Terminal
(Pin 3)
+
−
Vref
Other Error
Amplifier

FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

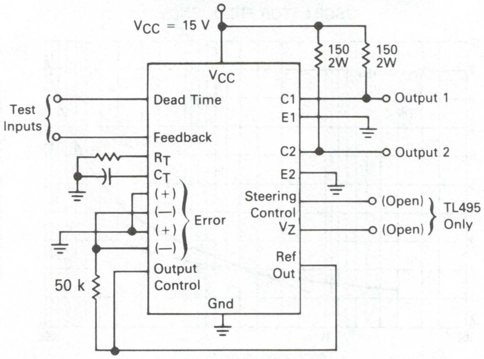

VCC = 15 V
150
2W
150
2W
VCC
Test
Inputs
Dead Time
Feedback
RT
CT
(+)
(—)
(+)
(—)
Error
Output
Control
Gnd
C1
E1
C2
E2
Steering
Control
VZ
Ref
Out
Output 1
Output 2
(Open)
(Open)
TL495
Only
50 k

FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

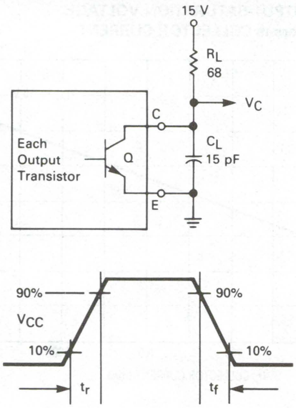

15 V
RL
68
VC
C
CL
15 pF
Each
Output
Transistor
Q
E
90%
90%
VCC
10%
10%
tr
tf

FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

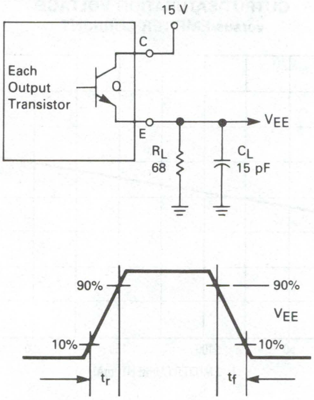

15 V
C
Each
Output
Transistor
Q
E
VEE
RL
68
CL
15 pF
90%
90%
VEE
10%
10%
tr
tf

FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES

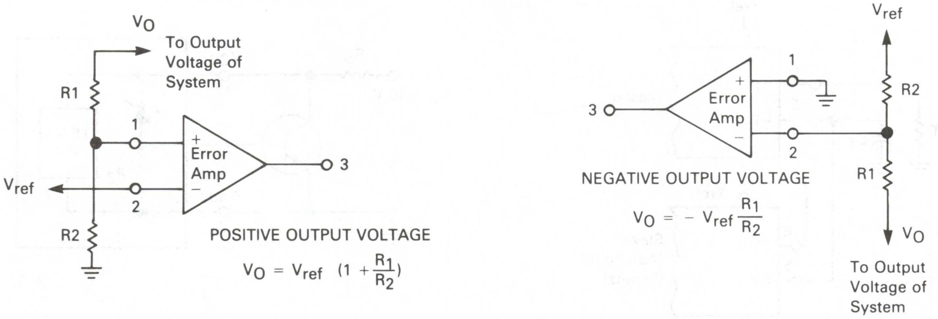

V_O
To Output Voltage of System
R1
1
+
Error Amp
−
3
V_{ref}
2
R2
POSITIVE OUTPUT VOLTAGE
$V_O = V_{ref} \left(1 + \frac{R1}{R2}\right)$
V_{ref}
1
3
2
R2
R1
NEGATIVE OUTPUT VOLTAGE
$V_O = -V_{ref} \frac{R1}{R2}$
V_O
To Output Voltage of System

FIGURE 16 — DEAD-TIME CONTROL CIRCUIT

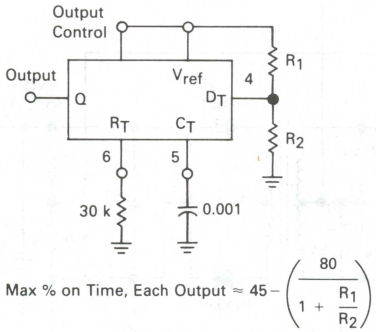

Output Control
Output
Q
V_{ref}
4
D_T
R_1
R_2
R_T
C_T
6
5
30 k
0.001
Max % on Time, Each Output ≈ $45 - \left(\frac{80}{1 + \frac{R_1}{R_2}}\right)$

FIGURE 17 — SOFT-START CIRCUIT

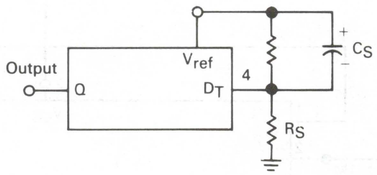
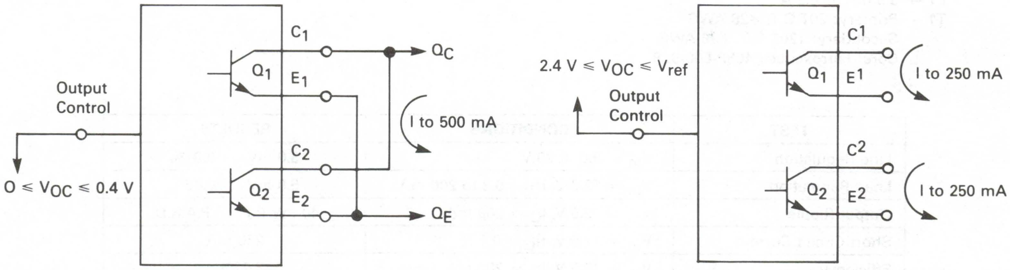

Output
Q
V_{ref}
4
D_T
C_S
+
−
R_S

FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS


Output Control
$0 \le V_{OC} \le 0.4$ V
C_1
Q_1
E_1
C_2
Q_2
E_2
Q_C
Q_E
I to 500 mA
$2.4 \text{ V} \le V_{OC} \le V_{ref}$
Output Control
C1
Q_1
E1
C2
Q_2
E2
I to 250 mA
I to 250 mA

Single Ended Configuration

Push-Pull Configuration

FIGURE 19 — SLAVING TWO OR MORE CONTROL CIRCUITS

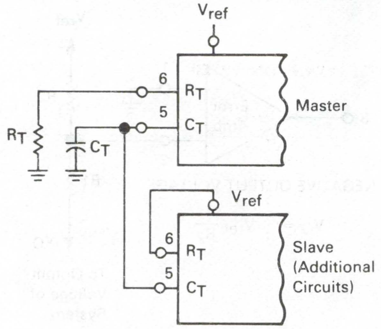

V_{ref}
6
R_T
5
C_T
Master
R_T
C_T
V_{ref}
6
R_T
5
C_T
Slave
(Additional
Circuits)

FIGURE 20 — OPERATION WITH $V_{IN} > 40$ V USING INTERNAL ZENER (TL495 ONLY)

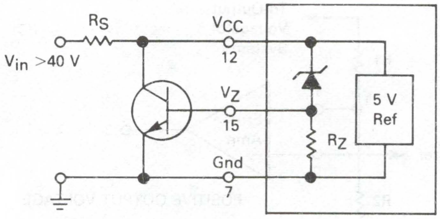
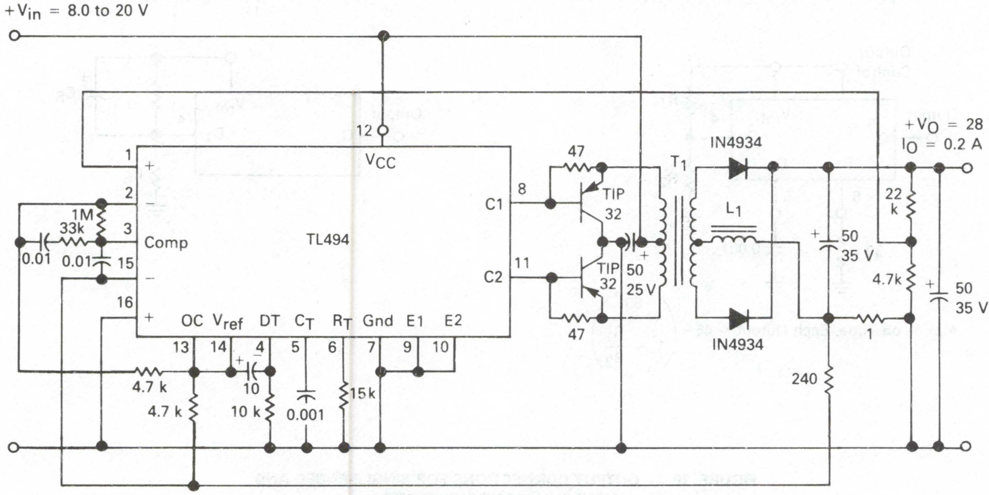

R_S
V_{CC}
12
$V_{in} > 40$ V
V_Z
15
Gnd
7
R_Z
5 V
Ref

FIGURE 21 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER

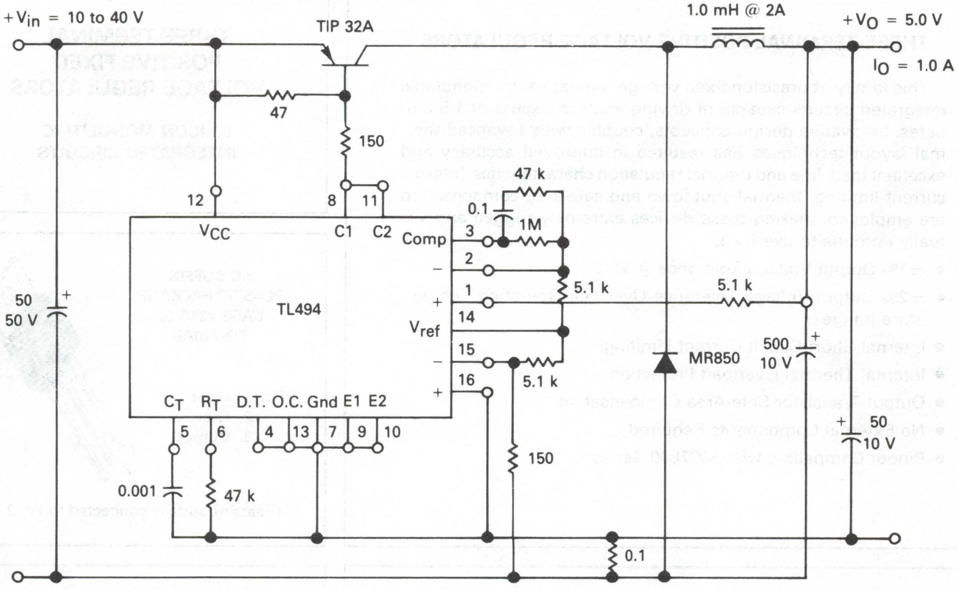

$+V_{in}$ = 8.0 to 20 V
12
V_{CC}
TL494
1
+
2
3
Comp
15
−
16
+
1M
33k
0.01
0.01
C1
8
C2
11
OC
V_{ref}
DT
C_T
R_T
Gnd
E1
E2
13
14
4
5
6
7
9
10
4.7 k
4.7 k
10
10 k
0.001
15k
47
47
TIP
32
TIP
32
50
25 V
T_1
L_1
IN4934
IN4934
50
35 V
22
k
4.7k
1
240
50
35 V
$+V_O$ = 28 V
I_O = 0.2 A

All capacitors in µF

L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 to 20 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

FIGURE 22 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER


+Vin = 10 to 40 V
TIP 32A
1.0 mH @ 2A
+VO = 5.0 V
IO = 1.0 A
47
150
47 k
0.1
1M
12
8
11
VCC
C1
C2
Comp
3
2
1
14
15
16
−
+
−
+
Vref
TL494
5.1 k
5.1 k
5.1 k
50
50 V
500
10 V
MR850
CT
RT
D.T.
O.C.
Gnd
E1
E2
5
6
4
13
7
9
10
0.001
47 k
150
50
10 V
0.1

All capacitors in µF

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 mA	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

TL780 Series

MOTOROLA

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 amperes. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

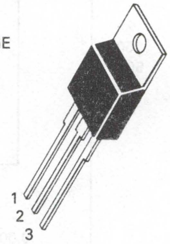
- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

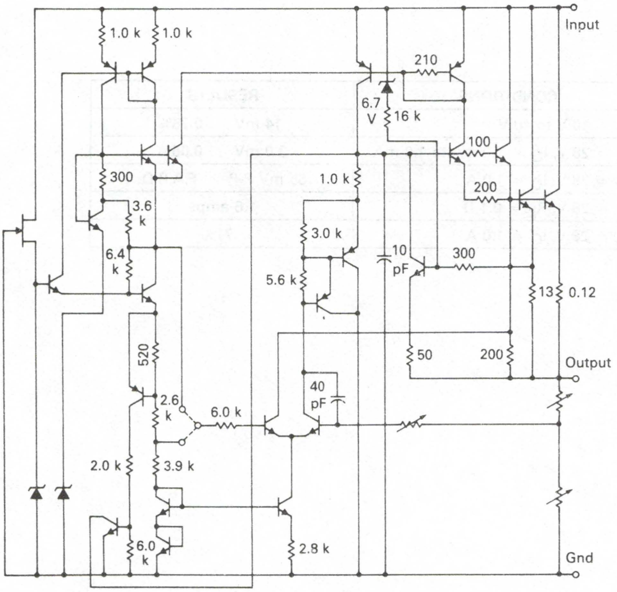
KC SUFFIX
PLASTIC PACKAGE
CASE 221A-02
TO-220AB

Pin 1. Input
2. Ground
3. Output

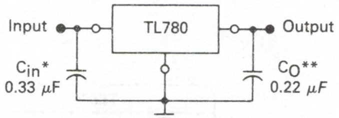


(Heatsink surface connected to Pin 2.)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output Voltage	Device
5.0 V	TL780-05CKC
12 V	TL780-12CKC
15 V	TL780-15CKC

TL780 Series MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics	–		
$T_A = +25°C$	P_D	2.0	Watts
Derate above $T_A = +25°C$	$1/\theta_{JA}$	16	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	62.5	°C/W
$T_C = +25°C$	P_D	15	Watts
Derate above $T_C = +75°C$ (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TL780-05C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-05C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 7.0 V ≤ V_{in} ≤ 20 V	V_O				V
$T_J = +25°C$		4.95	5.0	5.05	
0°C ≤ T_J ≤ +125°C		4.90	—	5.10	
Line Regulation ($T_J = +25°C$)	Reg_{line}				mV
7.0 V ≤ V_{in} ≤ 25 V		—	0.5	5.0	
8.0 V ≤ V_{in} ≤ 12 V		—	0.5	5.0	
Load Regulation ($T_J = +25°C$)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	4.0	25	
250 mA ≤ I_O ≤ 750 mA		—	1.5	15	
Ripple Rejection 8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz	RR	70	80	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.06	—	mV/°C
Output Noise Voltage ($T_J = +25°C$) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	µV
Dropout Voltage ($T_J = +25°C$) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current ($T_J = +25°C$)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA		—	0.7	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		—	0.03	0.5	
Short-Circuit Output Current ($T_J = +25°C$) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current ($T_J = +25°C$)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-12C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 14.5 V ≤ V_{in} ≤ 27 V	V_O				V
$T_J = +25°C$		11.88	12	12.12	
0°C ≤ T_J ≤ +125°C		11.76	—	12.24	
Line Regulation ($T_J = +25°C$)	Reg_{line}				mV
14.5 V ≤ V_{in} ≤ 30		—	1.2	12	
16 V ≤ V_{in} ≤ 22		—	1.2	12	

(continued)

TL780-12C (continued)

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	6.5	60	
250 mA ≤ I_O ≤ 750 mA		—	2.5	36	
Ripple Rejection 15 V ≤ V_{in} ≤ 25 V, f = 120 Hz	RR	65	77	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.15	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	180	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA		—	0.4	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		—	0.03	0.5	
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-15C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-15C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 17.5 V ≤ V_{in} ≤ 30 V					
T_J = +25°C		14.85	15	15.15	
0°C ≤ T_J ≤ +125°C		14.70	—	15.30	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
17.5 V ≤ V_{in} ≤ 30 V		—	1.5	15	
20 V ≤ V_{in} ≤ 26 V		—	1.5	15	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	7.0	75	
250 mA ≤ I_O ≤ 750 mA		—	2.5	45	
Ripple Rejection 18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz	RR	60	75	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.18	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	225	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change	ΔI_B				mA
17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA		—	0.4	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		—	0.02	0.5	
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTICS

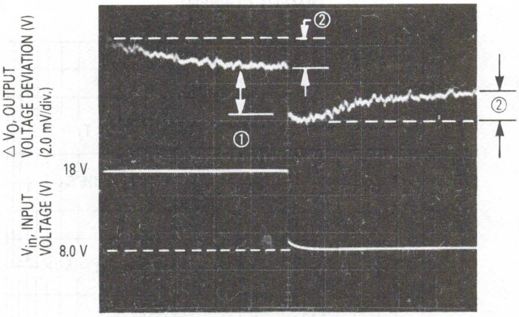
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100\ \mu s$) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



TL780-05C

$V_O = 5.0$ V

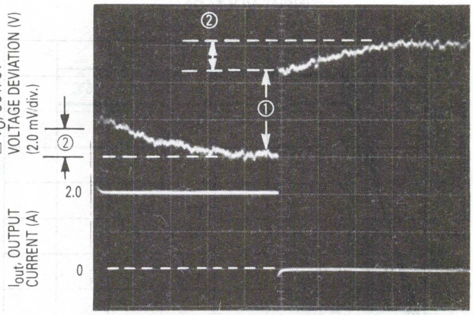
$V_{in} = 8.0\ V \rightarrow 18\ V \rightarrow 8.0$ V

$I_{out} = 1.0$ A

① = $Reg_{line} = 2.4$ mV

② = $Reg_{therm} = 0.0030\%\ V_O/W$

FIGURE 2 — LOAD AND THERMAL REGULATION



TL780-05C

$V_O = 5.0$ V

$V_{in} = 15$

$I_{out} = 0\ A \rightarrow 1.5\ A \rightarrow 0$ A

① = $Reg_{line} = 4.4$ mV

② = $Reg_{therm} = 0.0020\%\ V_O/W$

FIGURE 3 — TEMPERATURE STABILITY

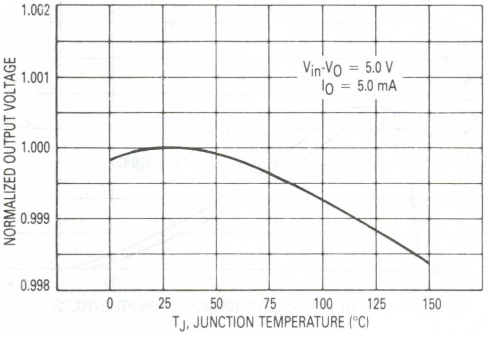


FIGURE 4 — OUTPUT IMPEDANCE

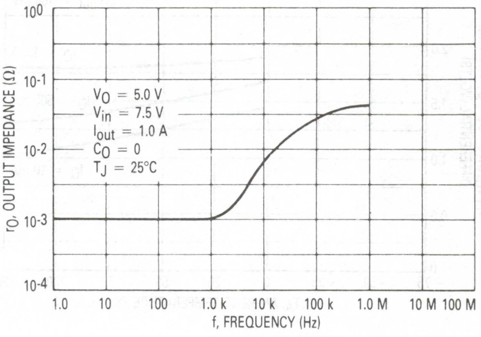


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

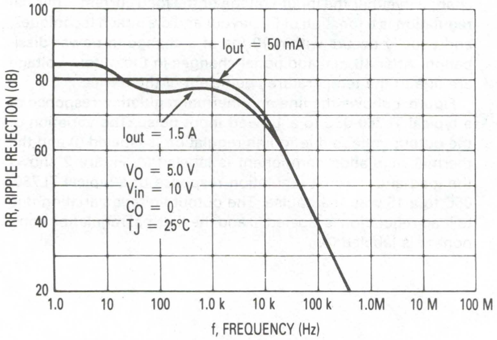


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

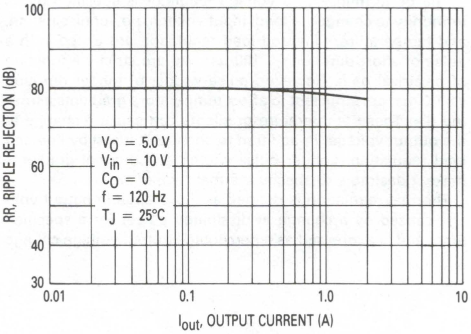


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

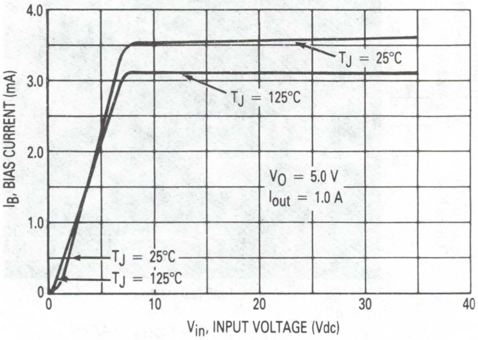


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

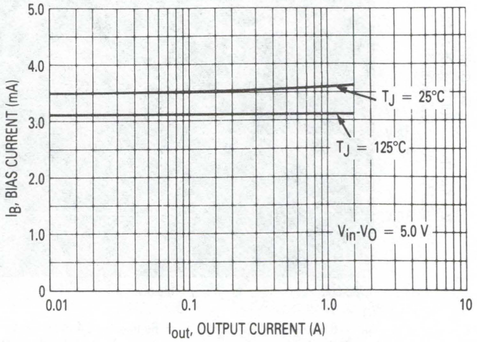


FIGURE 9 — DROPOUT VOLTAGE

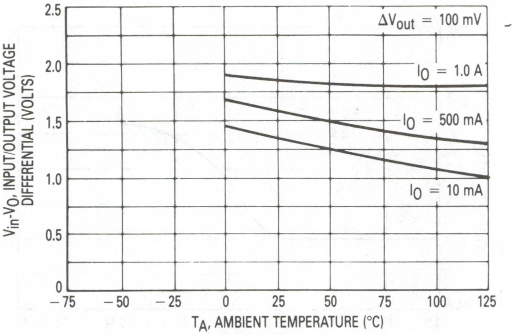


FIGURE 10 — PEAK OUTPUT CURRENT

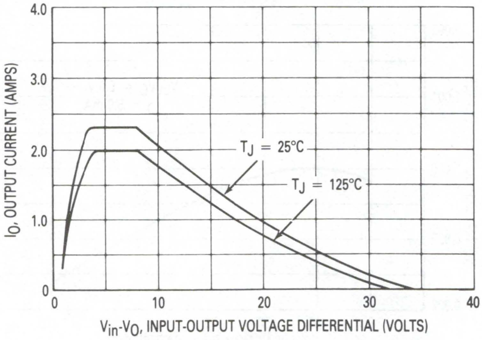


FIGURE 11 — LINE TRANSIENT RESPONSE

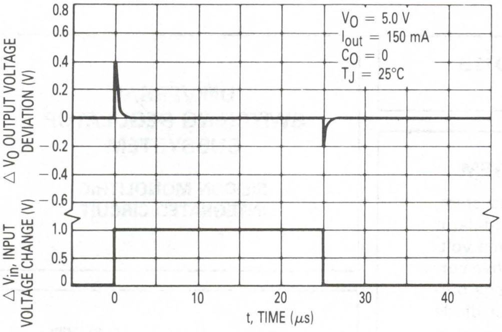


FIGURE 12 — LOAD TRANSIENT RESPONSE

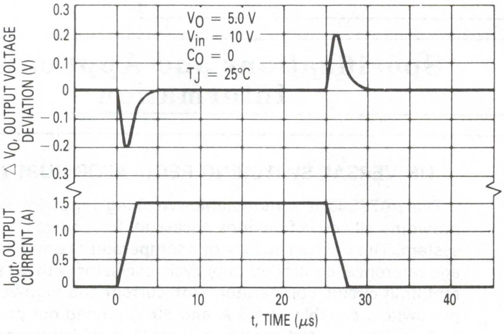
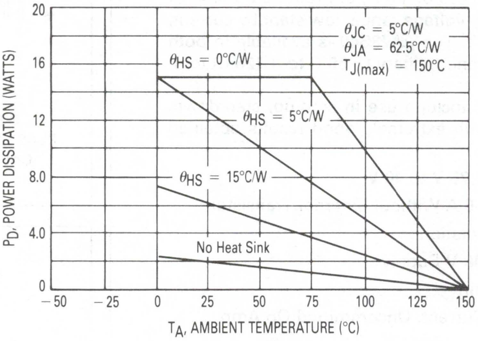


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE



μA78S40

MOTOROLA

Specifications and Applications Information

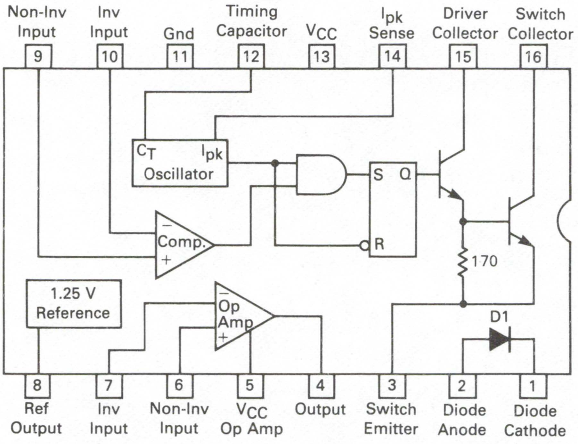
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

The μA78S40 is a monolithic-switching regulator subsystem, providing all active functions necessary for a switching regulator system. The device consists of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater than 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in both commercial (0°C to +70°C) and military (−55°C to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

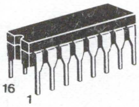
BLOCK DIAGRAM


Non-Inv Input 9
Inv Input 10
Gnd 11
Timing Capacitor 12
V_{CC} 13
I_{pk} Sense 14
Driver Collector 15
Switch Collector 16
C_T I_{pk} Oscillator
S Q
R
Comp.
170
1.25 V Reference
Op Amp
D1
8 Ref Output
7 Inv Input
6 Non-Inv Input
5 V_{CC} Op Amp
4 Output
3 Switch Emitter
2 Diode Anode
1 Diode Cathode

(Bottom View)

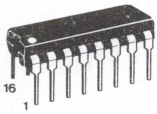
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

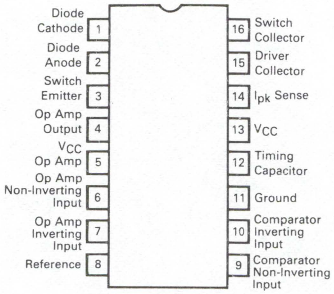


D SUFFIX
CERAMIC PACKAGE
CASE 620-02

P SUFFIX
PLASTIC PACKAGE
CASE 648-05



PIN CONNECTIONS


Diode Cathode 1
Diode Anode 2
Switch Emitter 3
Op Amp Output 4
V_{CC} Op Amp 5
Op Amp Non-Inverting Input 6
Op Amp Inverting Input 7
Reference 8
16 Switch Collector
15 Driver Collector
14 I_{pk} Sense
13 V_{CC}
12 Timing Capacitor
11 Ground
10 Comparator Inverting Input
9 Comparator Non-Inverting Input

(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	0°C to +70°C	Plastic DIP
μA78S40DC	0°C to +70°C	Ceramic DIP
μA78S40DM	−55°C to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	-0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	±30	V
Output Short-Circuit Duration (Op Amp)	—	Continuous	—
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd	—	40	V
Voltage from Switch Emitters to Gnd	—	40	V
Voltage from Switch Collectors to Emitter	—	40	V
Voltage from Power Diode to Gnd	—	40	V
Reverse-Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics			
Plastic Package — $T_A = +25°C$	P_D	1500	mW
Derate above +25°C (Note 1)	$1/R_{\theta JA}$	14	mW/°C
Ceramic Package — $T_A = 25°C$	P_D	1000	mW
Derate above +25°C (Note 1)	$1/R_{\theta JA}$	8.0	mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range	T_A		°C
μA78S40M		−55 to +125	
μA78S40C		0 to +70	

Notes:

1. T_{low} = −55°C for μA78S40DM
   = 0°C for μA78S40DC and μA78S40PC
   T_{high} = +125°C for μA78S40DM
   = +70°C for μA78S40DC and μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{CC}$ (Op Amp) = 5.0 V, $T_A = T_{low}$ to T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	—	40	V
Supply Current (Op Amp V_{CC} Disconnected)	I_{CC}				mA
(V_{CC} = 5.0 V)		—	1.8	3.5	
(V_{CC} = 40 V)		—	2.3	5.0	
Supply Current (Op Amp V_{CC} Connected)	I_{CC}				mA
(V_{CC} = 5.0 V)		—	—	4.0	
(V_{CC} = 40 V)		—	—	5.5	
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	—	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	—	0.2	0.5	mV/mA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C)	I_{chg}				μA
(V_{CC} = 5.0 V)		20	—	50	
(V_{CC} = 40 V)		20	—	70	
Discharge Current (T_A = 25°C)	I_{dis}				μA
(V_{CC} = 5.0 V)		150	—	250	
(V_{CC} = 40 V)		150	—	350	
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	—	0.5	—	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	—	6.0	—	—
CURRENT LIMIT					
Current-Limit Sense Voltage (T_A = 25°C) (V_{CC} − V_{Ipk} Sense)	V_{CLS}	250	—	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	—	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	—	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	—	70	—	—
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	—	10	—	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	—	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	—	10	—	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{Ref})	V_{IO}	—	1.5	15	mV
Input Bias Current (V_{CM} = V_{Ref})	I_{IB}	—	35	200	nA
Input Offset Current (V_{CM} = V_{Ref})	I_{IO}	—	5.0	75	nA
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} − 2.0	V
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 ≤ V_{CC} ≤ 40 V)	PSRR	70	96	—	dB
OUTPUT OPERATIONAL AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	—	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	—	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	—	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL+}	25	250	—	V/mV
Voltage Gain − (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL-}	25	250	—	V/mV
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} − 2.0	V
Common-Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 to 3.0 V)	CMRR	76	100	—	dB
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	—	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	—	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	—	mA
Slew Rate (T_A = 25°C)	SR	—	0.6	—	V/μs
Output Low Voltage (T_A = 25°C, I_L = −5.0 mA)	V_{OL}	—	—	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC} (Op Amp) −3.0	—	—	V

FIGURE 1 — OUTPUT SWITCH ON/OFF TIME versus OSCILLATOR TIMING CAPACITOR

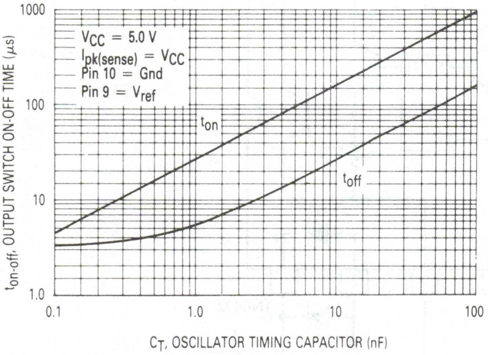


FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

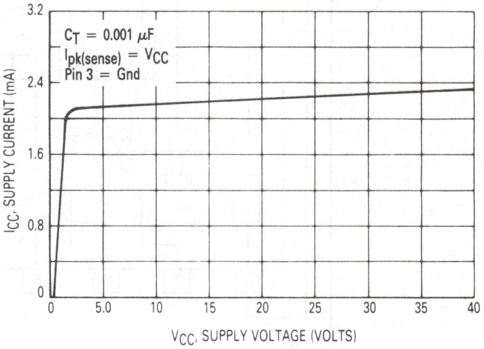


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT

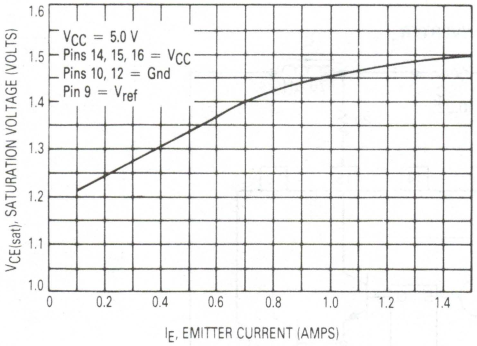


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

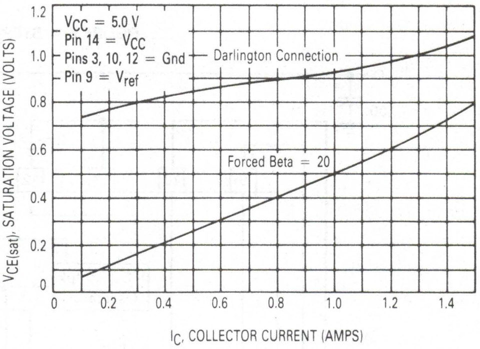
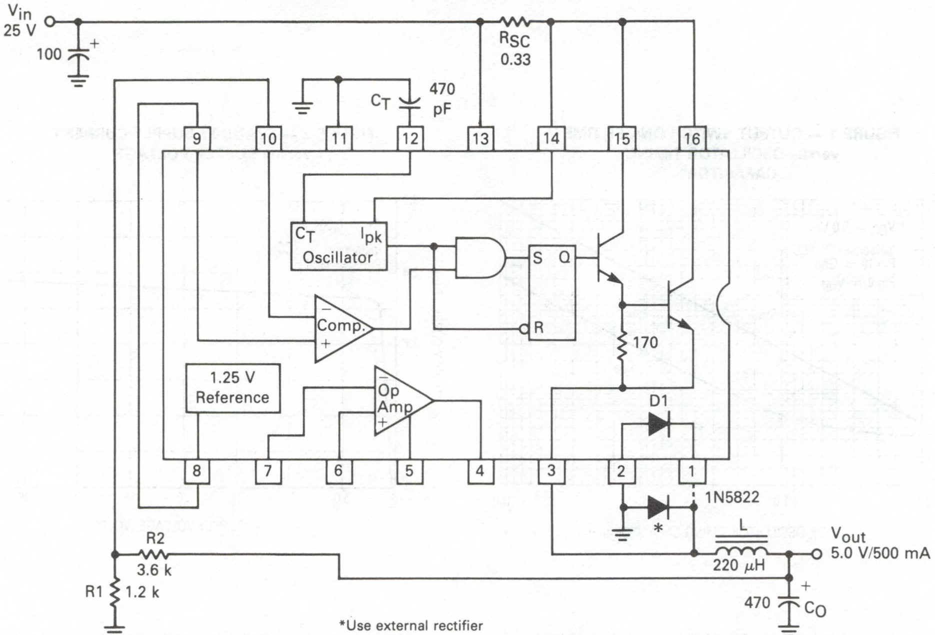
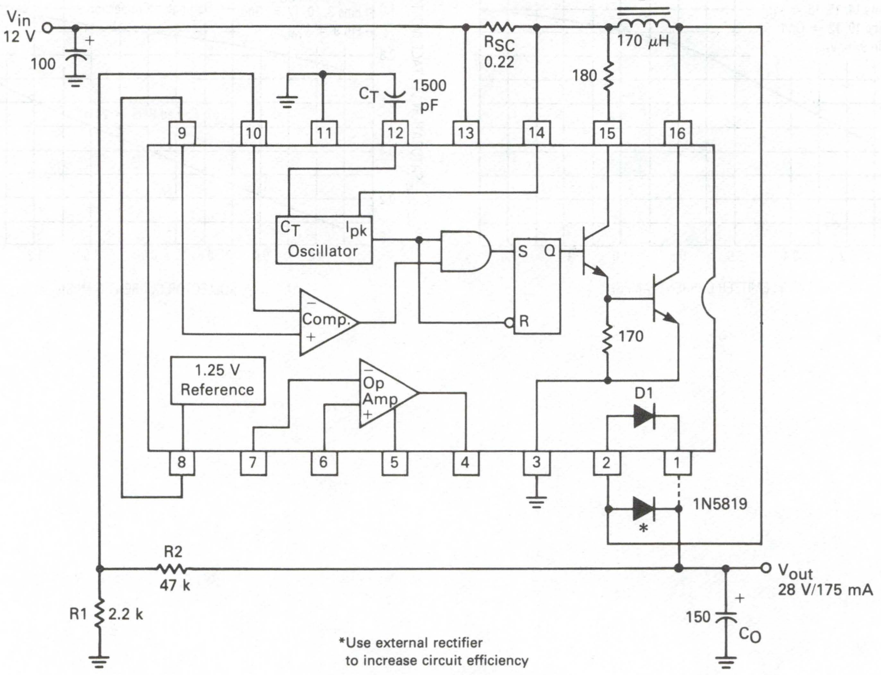


FIGURE 5 — STEP-DOWN CONVERTER


Vin
25 V
100
+
RSC
0.33
CT
470
pF
9
10
11
12
13
14
15
16
CT
Ipk
Oscillator
S
Q
R
Comp.
−
+
1.25 V
Reference
Op
Amp
−
+
170
D1
8
7
6
5
4
3
2
1
1N5822
*
L
220 μH
Vout
5.0 V/500 mA
R2
3.6 k
R1
1.2 k
470
+
CO

*Use external rectifier
to increase circuit efficiency

FIGURE 6 — STEP-UP CONVERTER


L
Vin
12 V
100
+
RSC
0.22
170 μH
180
CT
1500
pF
9
10
11
12
13
14
15
16
CT
Ipk
Oscillator
S
Q
R
Comp.
−
+
1.25 V
Reference
Op
Amp
−
+
170
D1
8
7
6
5
4
3
2
1
1N5819
*
R2
47 k
R1
2.2 k
Vout
28 V/175 mA
150
+
CO

*Use external rectifier
to increase circuit efficiency

FIGURE 7 — INVERTING CONVERTER

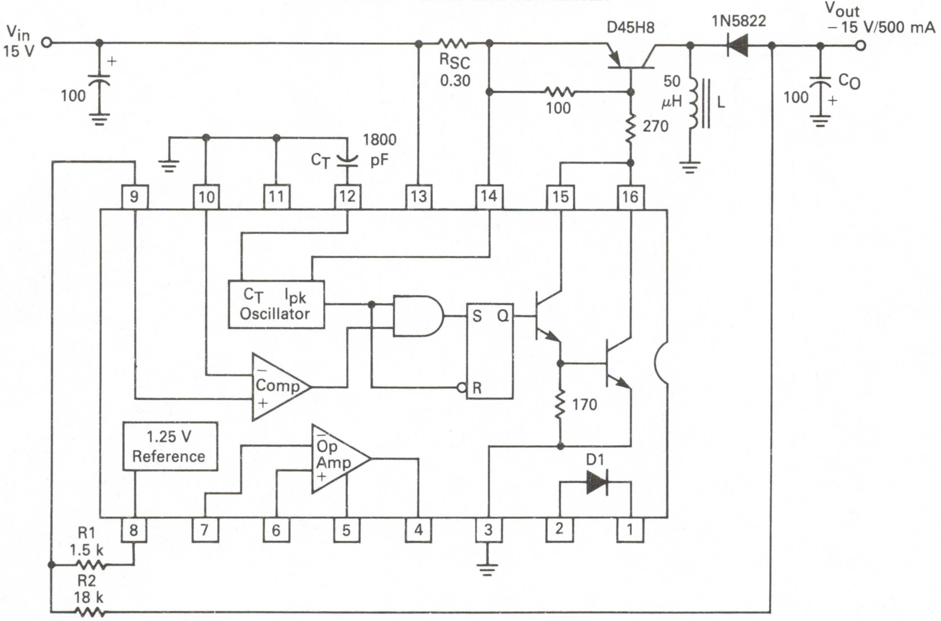


FIGURE 8 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(max)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2\, I_{out(max)}$	$2\, I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$	$2\, I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(max)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8\, V_{ripple(p-p)}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

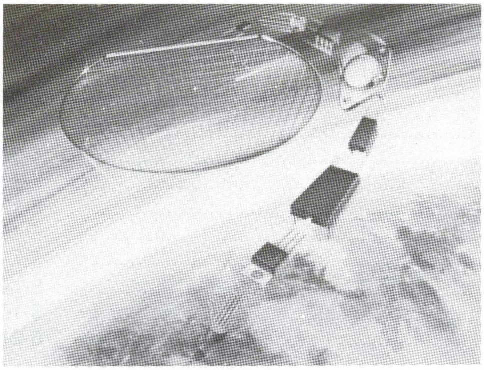
V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting convertor.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step-down and step-up; $V_{out} = \frac{1.25\ R2}{R1}$ for Inverting.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.



Voltage References

VOLTAGE REFERENCES

Device	Function	Page
LM285	Micropower Voltage Reference Diodes	5-3
LM385	Micropower Voltage Reference Diode	5-3
MC1400,A	Precision Voltage References	5-7
MC1403,A	Precision Low-Voltage Reference	5-12
MC1404,A	Precision Low-Drift Voltage Reference	5-16
MC1500,A	Precision Voltage References	5-7
MC1503,A	Precision Low-Voltage Reference	5-12
MC1504,A	Precision Low-Drift Voltage Reference	5-16
TL431	Programmable Precision References	5-21

MOTOROLA

LM285
LM385

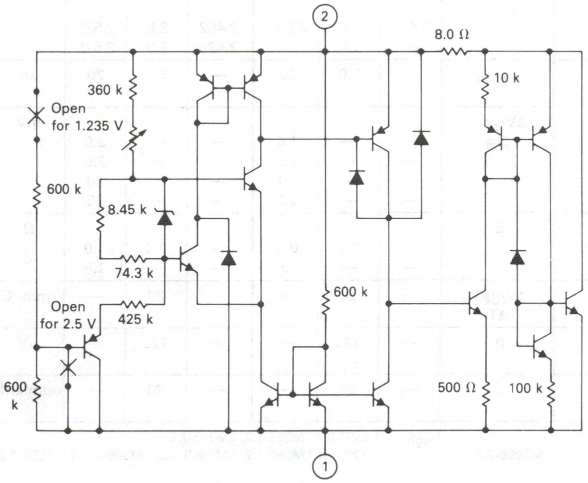
MICROPOWER VOLTAGE REFERENCE DIODES

The LM285/LM385 series are micropower two-terminal band-gap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO-226AA (TO-92) plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Available in 1.235 and 2.500 Volt Versions

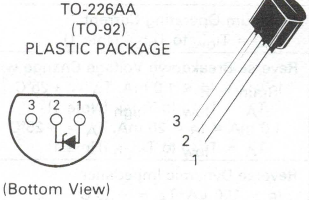
EQUIVALENT CIRCUIT SCHEMATIC



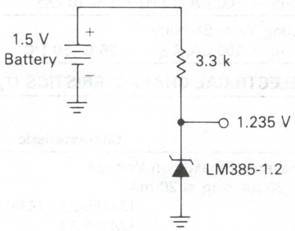
MICROPOWER VOLTAGE REFERENCE DIODES

SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX
CASE 29-02
TO-226AA
(TO-92)
PLASTIC PACKAGE



STANDARD APPLICATION



ORDERING INFORMATION

Device	Temp. Range	Reverse Break-down Voltage	Tolerance
LM285Z-1.2	−40 °C to +85°C	1.235 Volts	±1.0%
LM285Z-2.5		2.500 Volts	±1.5%
LM385BZ-1.2	0°C to +70°C	1.235 Volts	±1.0%
LM385Z-1.2		1.235 Volts	±2.0%
LM385BZ-2.5		2.500 Volts	±1.5%
LM385Z-2.5		2.500 Volts	±3.0%

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range	T_A		°C
LM285		−40 to +85	
LM385		0 to +70	
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise noted)

Characteristic	Symbol	LM285-1.2			LM385-1.2/LM385B-1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$V_{(BR)R}$							V
$I_{Rmin} \le I_R \le 20$ mA								
LM285-1.2/LM385B-1.2		1.223	1.235	1.247	1.223	1.235	1.247	
LM385-1.2		—	—	—	1.205	1.235	1.260	
Minimum Operating Current (T_A = T_{low} to T_{high} Note 1)	I_{Rmin}	—	2.5	10	—	2.5	15	μA
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)}/\Delta I_R$							mV
$I_{Rmin} \le I_R \le 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	1.0	
T_A = T_{low} to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
T_A = T_{low} to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance	Z							Ω
I_R = 100 μA, T_A = +25°C		—	0.2	0.6	—	0.4	1.0	
T_A = T_{low} to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
Average Temperature Coefficient 10 μA $\le I_R \le$ 20 mA, T_A = T_{low} to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	20	—	—	20	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz $\le f \le$ 10 kHz	n	—	60	—	—	60	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ±0.1°C	S	—	20	—	—	20	—	ppm/kHR

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise noted)

Characteristic	Symbol	LM285-2.5			LM385-2.5/LM385B-2.5			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$V_{(BR)R}$							V
20 μA $\le I_R \le$ 20 mA								
LM285-2.5/LM385B-2.5		2.462	2.5	2.538	2.462	2.5	2.538	
LM385-2.5		—	—	—	2.425	2.5	2.575	
Minimum Operating Current T_A = T_{low} to T_{high} (Note 1)	I_{Rmin}	—	5.0	20	—	5.0	20	μA
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)}/\Delta I_R$							mV
20 μA $\le I_R \le$ 1.0 mA, T_A = +25°C		—	—	1.0	—	—	2.0	
T_A = T_{low} to T_{high} (Note 1)		—	—	1.5	—	—	2.5	
1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
T_A = T_{low} to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance	Z							Ω
I_R = 100 μA, T_A = +25°C		—	0.2	0.6	—	0.4	1.0	
T_A = T_{low} to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
Average Temperature Coefficient 20 μA $\le I_R \le$ 20 mA, T_A = T_{low} to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	20	—	—	20	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz $\le f \le$ 10 kHz	n	—	120	—	—	120	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ±0.1°C	S	—	20	—	—	20	—	ppm/kHR

NOTES: 1. T_{low} = −40°C for LM285-1.2, LM285-2.5
= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

T_{high} = +85°C for LM285-1.2, LM285-2.5
= +70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

FIGURE 1 — REVERSE CHARACTERISTICS

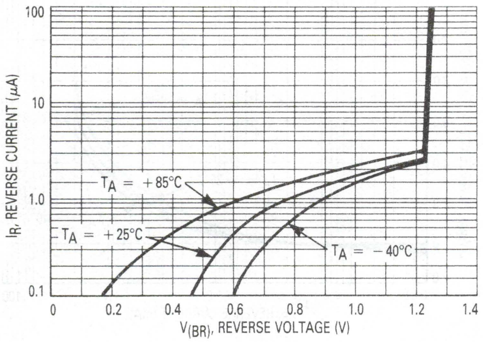


FIGURE 2 — REVERSE CHARACTERISTICS

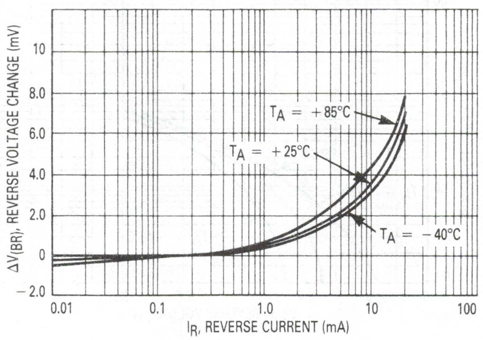


FIGURE 3 — FORWARD CHARACTERISTICS

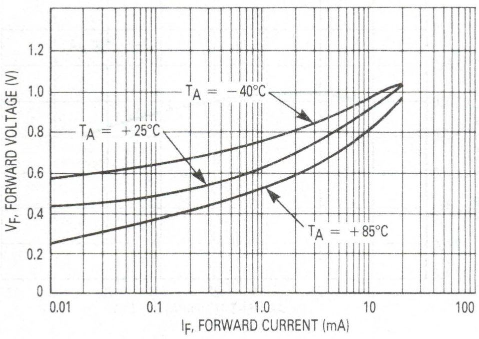


FIGURE 4 — TEMPERATURE DRIFT

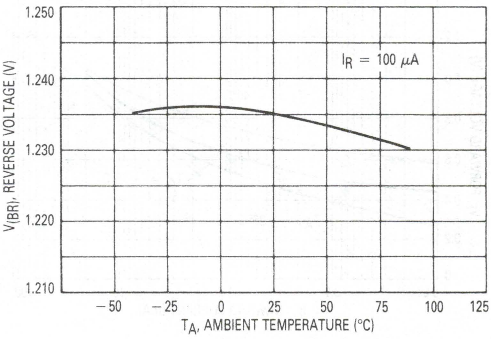


FIGURE 5 — NOISE VOLTAGE

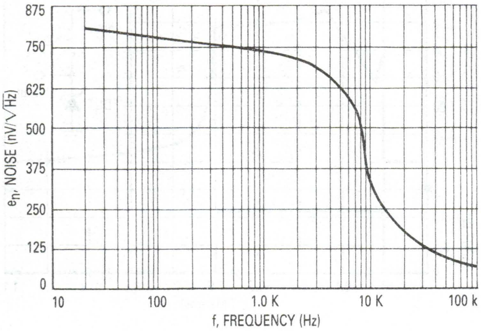
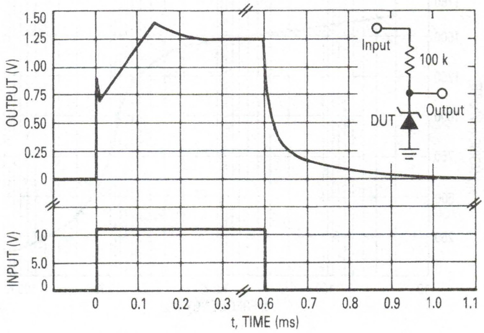


FIGURE 6 — RESPONSE TIME



TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

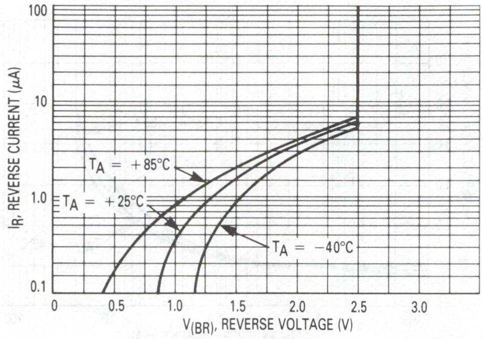


FIGURE 8 — REVERSE CHARACTERISTICS

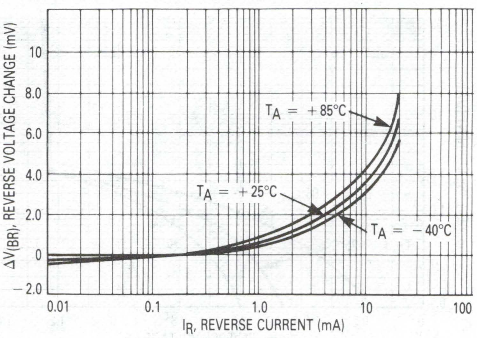


FIGURE 9 — FORWARD CHARACTERISTICS

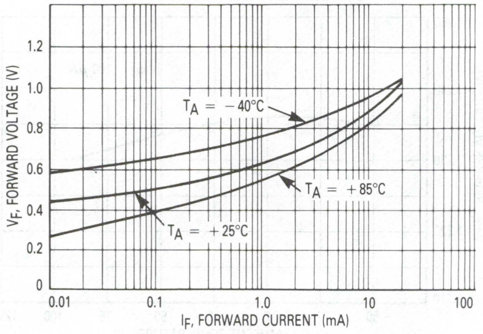


FIGURE 10 — TEMPERATURE DRIFT

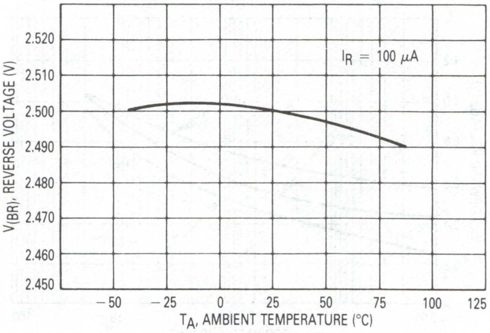


FIGURE 11 — NOISE VOLTAGE

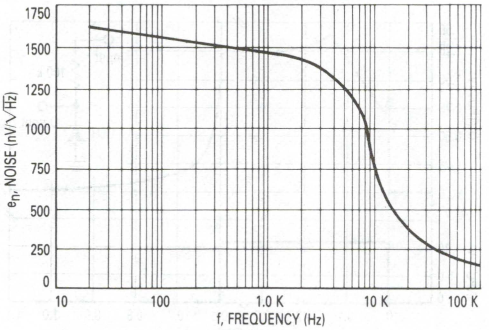
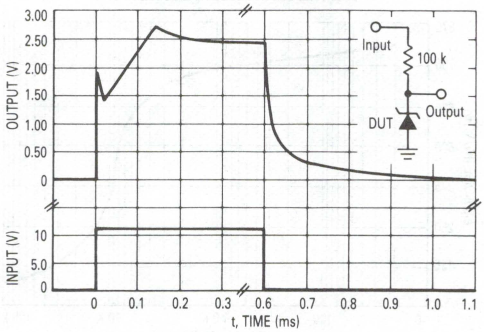


FIGURE 12 — RESPONSE TIME



MOTOROLA

MC1400,A
MC1500,A

Specifications and Applications Information

PRECISION VOLTAGE REFERENCES

2.5, 5.0, 6.25 and 10-VOLT

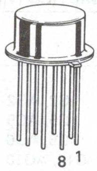
LASER-TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

TIGHT-TOLERANCE, LOW-DRIFT VOLTAGE REFERENCE FAMILY

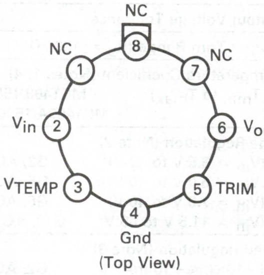
The MC1400 series of ICs is a family of temperature-compensated voltage references for precision data conversion and instrumentation applications. Advances in thin-film resistors, laser-trimming techniques, ion-implanted devices, and monolithic fabrication techniques make this reference both temperature and time stable in applications demanding accuracy to the 12-bit level.

These devices offer simple, no-external-component operation as three-terminal, positive-voltage references, and also simple, one-external-resistor operation as either positive or negative references. Unique circuitry permits these devices to either source or sink greater than 10 mA of load current with excellent regulation. This feature means that the buffer amplifiers and current sources normally required for precision zener references can be eliminated.

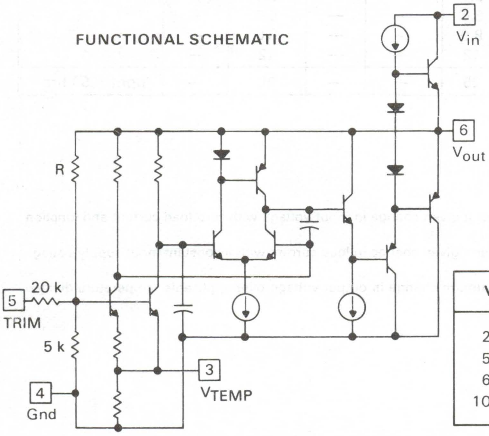
- Four Different Output Voltages: 2.5, 5.0, 6.25, 10 V
- Tight Absolute Accuracy: ±0.2% Maximum Initial Tolerance
- Single-Component Output Trimming Without Degrading Temperature Coefficient
- Wide Input Voltage Range: $(V_{out} + 1.0\ V) \leq V_{in} \leq 40\ V$
- Three-Terminal Operation:
  Positive References That Can Source and Sink Current
- Two-Terminal Operation:
  Positive or Negative References
  Floating References
- Low Current Consumption: 1.0 mA Typical
- Very Low Temperature Coefficient
- Low Output Noise Voltage
- Excellent Ripple Rejection: 87 dB Typical at 120 Hz
- Excellent Long Term Stability: 25 ppm/1000 Hrs Typical



G SUFFIX
METAL PACKAGE
CASE 601-04



FUNCTIONAL SCHEMATIC



V_{out}	R
2.5 V	5 kΩ
5.0 V	15 kΩ
6.25 V	20 kΩ
10.0 V	35 kΩ

ORDERING INFORMATION

Device	Temperature Range
2.5 Volts	
MC1500G2	−55°C to +125°C
MC1500AG2	−55°C to +125°C
MC1400G2	0°C to +70°C
MC1400AG2	0°C to +70°C
5.0 Volts	
MC1500G5	−55°C to +125°C
MC1500AG5	−55°C to +125°C
MC1400G5	0°C to +70°C
MC1400AG5	0°C to +70°C
6.25 Volts	
MC1500G6	−55°C to +125°C
MC1500AG6	−55°C to +125°C
MC1400G6	0°C to +70°C
MC1400AG6	0°C to +70°C
10 Volts	
MC1500G10	−55°C to +125°C
MC1500AG10	−55°C to +125°C
MC1400G10	0°C to +70°C
MC1400AG10	0°C to +70°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Applied Voltages			V
	V_{in}	−0.3 to +40	
	V_{TRIM}	−0.3 to +5.0	
Load Current			
V_{TEMP}, Pin 3	I_{TEMP}	±50	µA
Output, Pin 6	I_{out}	±40	mA
Output Short Circuit Duration	t_{sc}		seconds
To Ground		Continuous	
To V_{in}		10	
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC1500,A		−55 to +125	
MC1400,A		0 to +70	

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic		Symbol	MC1400,A			MC1500,A			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage (I_O = 0 mA)		V_O							Volts
	G2, AG2		2.495	2.500	2.505	2.495	2.500	2.505	
	G5, AG5		4.990	5.000	5.010	4.990	5.000	5.010	
	G6, AG6		6.240	6.250	6.260	6.240	6.250	6.260	
	G10, AG10		9.980	10.000	10.020	9.980	10.000	10.020	
Output Voltage Tolerance		—	—	0.05	0.20	—	0.05	0.20	%
Output Trim Range (R_p = 100 kΩ)		ΔV_{TRIM}	±6.0	—	—	±6.0	—	—	%
Temperature Coefficient (Notes 1, 4) (T_{min} to T_{max})		TCV_O							ppm/°C
	MC1400/1500		—	—	25	—	—	40	
	MC1400A/1500A		—	—	10	—	—	10	
Line Regulation (Note 2)		Reg_{line}							mV
(V_{in} = 3.5 V to 40 V)	G2, AG2		—	1.0	3.0	—	1.0	3.0	
(V_{in} = 6.0 V to 40 V)	G5, AG5		—	1.5	4.0	—	1.5	4.0	
(V_{in} = 7.5 V to 40 V)	G6, AG6		—	1.5	4.0	—	1.5	4.0	
(V_{in} = 11.5 V to 40 V)	G10, AG10		—	2.0	4.0	—	2.0	4.0	
Load Regulation (Note 3)		Reg_{load}							mV
($-10 \leq I_L \leq +10$ mA)	G2, AG2		—	6.0	10	—	6.0	10	
	G5, AG5		—	8.0	20	—	8.0	20	
	G6, AG6		—	8.0	20	—	8.0	20	
	G10, AG10		—	8.0	20	—	8.0	20	
Quiescent Current (I_O = 0 mA)		I_I	—	0.77	1.5	—	0.77	1.5	mA
Zener Mode Regulation (Figure 1)		V_Z							mV
($1.0 \leq I_Z \leq 10$ mA)	G2, AG2		—	3.0	—	—	3.0	—	
	G5, AG5		—	6.0	—	—	6.0	—	
	G6, AG6		—	8.0	—	—	8.0	—	
	G10, AG10		—	12	—	—	12	—	
Long Term Stability		—	—	25	—	—	25	—	ppm/1000 hrs

NOTES:

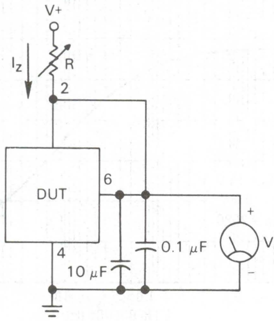
1. T_{min} = −55°C for MC1500,A
   = 0°C for MC1400,A
   T_{max} = +125°C for MC1500,A
   = +70°C for MC1400,A
2. Line Regulation is defined as the maximum excursion in output voltage over a given change in input voltage with zero load current and junction temperature constant.
3. Load Regulation is defined as the maximum excursion in output voltage over a given change in load current with a constant input supply voltage of +15 volts and a constant junction temperature.
4. Temperature Coefficient of the output voltage (TCV_O) is defined as the maximum change in output voltage over applicable temperature divided by the device operating temperature range and expressed as ppm/°C.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1400,A Min	MC1400,A Typ	MC1400,A Max	MC1500,A Min	MC1500,A Typ	MC1500,A Max	Unit
Turn-On Settling Time (Figure 2) (to ±0.01%)	t_S	—	50	—	—	50	—	µs
Output Noise Voltage — P to P (0.1≤f≤10 Hz)	V_n							µV
G2, AG2		—	8.0	—	—	8.0	—	
G5, AG5		—	12	—	—	12	—	
G6, AG6		—	14	—	—	14	—	
G10, AG10		—	16	—	—	16	—	
Small-Signal Output Impedance (f = 120 Hz)	z_o	—	0.3	—	—	0.3	—	Ω
Power Supply Rejection Ratio (f = 120 Hz)	PSRR	60	87	—	60	87	—	dB

TYPICAL CHARACTERISTICS

FIGURE 1 — ZENER MODE REGULATION TEST CIRCUIT



NOTE: I_z is the net current flowing into the device.

FIGURE 2 — TURN-ON SETTLING TIME TEST CIRCUIT

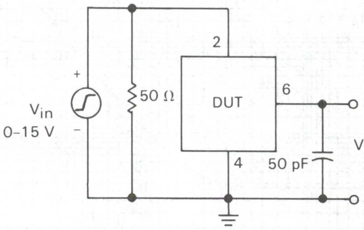


FIGURE 3 — NORMALIZED OUTPUT VOLTAGE versus TEMPERATURE

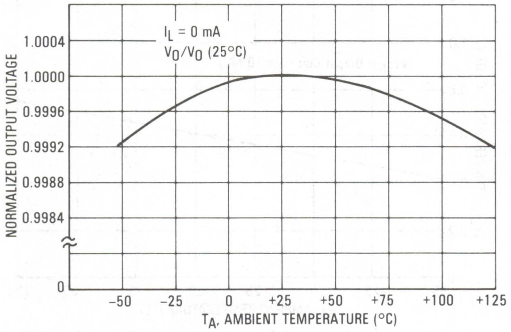


FIGURE 4 — LINE REGULATION versus TEMPERATURE

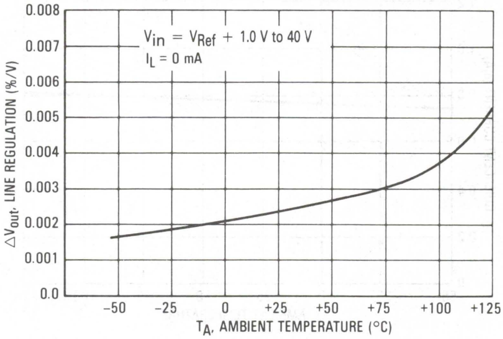


FIGURE 5 — LOAD REGULATION versus TEMPERATURE

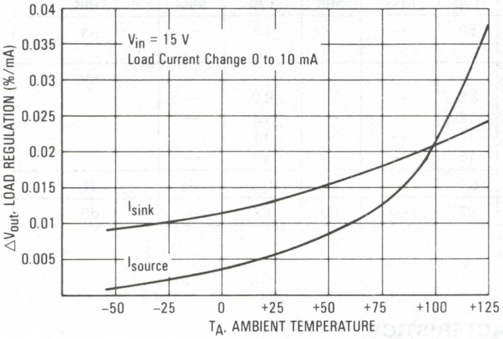


FIGURE 6 — ZENER MODE REGULATION versus TEMPERATURE

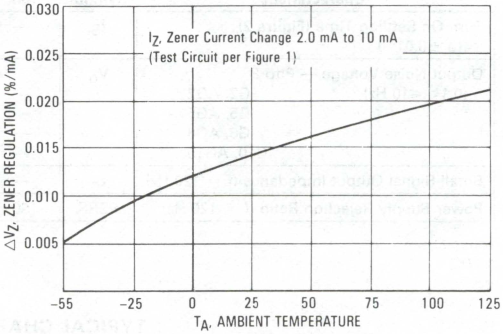


FIGURE 7 — OUTPUT IMPEDANCE versus FREQUENCY

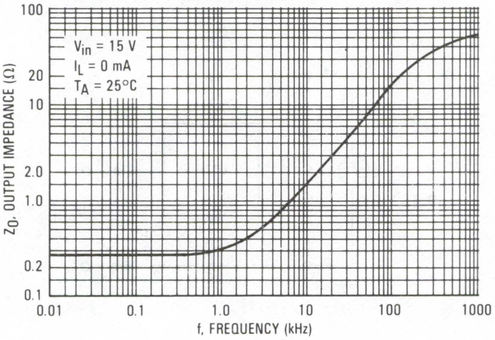


FIGURE 8 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

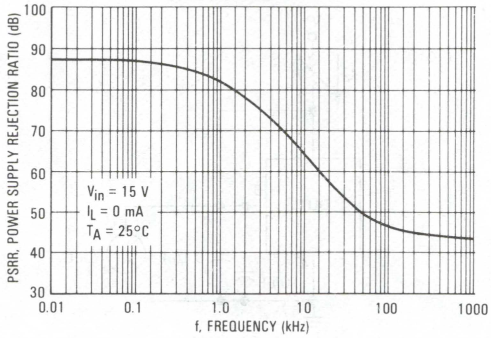


FIGURE 9 — QUIESCENT CURRENT versus TEMPERATURE

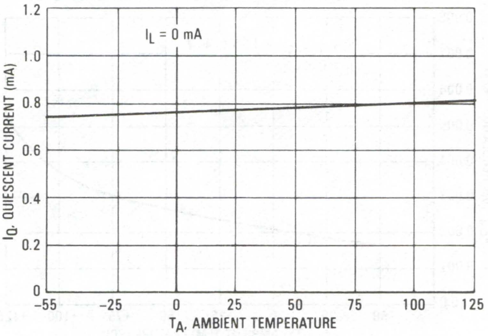


FIGURE 10 — V_{TEMP}, OUTPUT versus TEMPERATURE

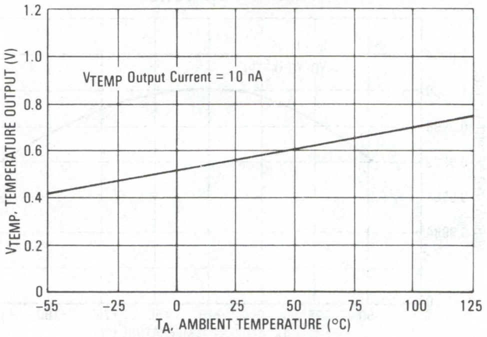
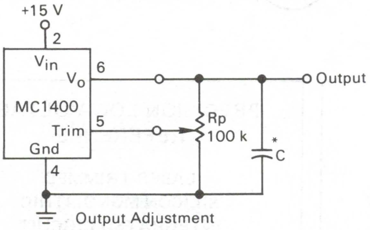


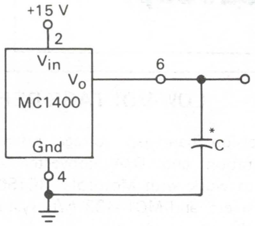
FIGURE 11 — OUTPUT TRIM CONFIGURATION


+15 V
2
Vin
Vo
6
Output
MC1400
5
Trim
Rp
100 k
*
C
Gnd
4
Output Adjustment

The MC1400 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although the circuit of Figure 11 allows a wide trim range, trimming should be kept to ⩽ ±6% in applications requiring low temperature coefficents.

FIGURE 12 — FIXED REFERENCE


+15 V
2
Vin
Vo
6
MC1400
*
C
Gnd
4

*For better stability, transient response, and minimum noise voltage, the device should be bypassed with a 0.1 μF ceramic capacitor from Pins 6 to 4 as shown.

FIGURE 13 — NEGATIVE REFERENCE OPERATION

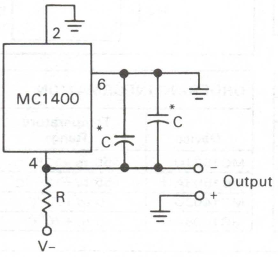
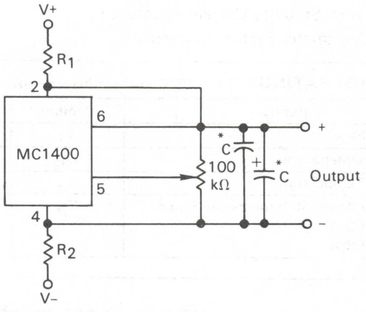

2
MC1400
6
*
C
*
C
4
–
Output
+
R
V–

FIGURE 14 — TRIMMABLE FLOATING REFERENCE OPERATION


V+
R1
2
MC1400
6
+
*
C
100
kΩ
+
*
C
Output
5
4
–
R2
V–

*For better stability, transient response, and minimum noise voltage, the device should be bypassed with a 0.1 μF ceramic and a 10 μF electrolytic capacitor from Pins 6 to 4 as shown.

MC1403,A
MC1503,A

MOTOROLA

LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

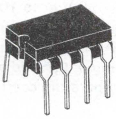
- Output Voltage = 2.5 V ±25 mV
- Input Voltage Range = 4.5 V to 40 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP Package

Typical Applications

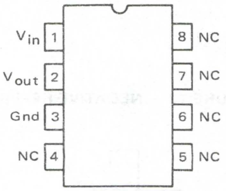
- Voltage Reference for 8-12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

PRECISION LOW-VOLTAGE REFERENCE

LASER TRIMMED
SILICON MONOLITHIC
INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



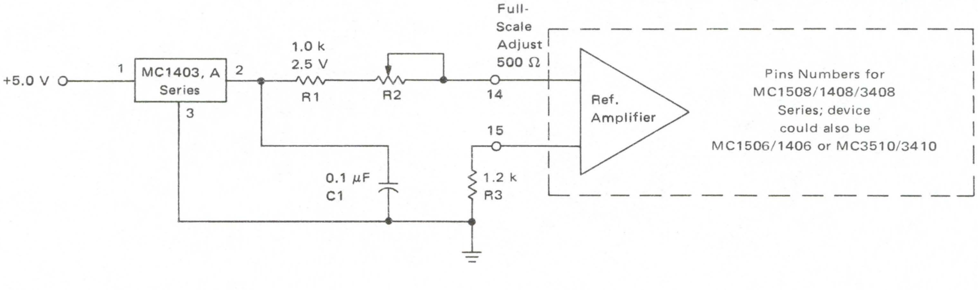
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temeprature Range	T_A		
MC1503,A		-55 to +125	°C
MC1403,A		0 to +70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	-55 to +125°C	Ceramic DIP
MC1503AU	-55 to +125°C	Ceramic DIP
MC1403U	0 to +70°C	Ceramic DIP
MC1403AU	0 to +70°C	Ceramic DIP

FIGURE 1 — A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1406/1506, MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_I = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503 } −55°C to +125°C		–	–	25	
MC1503A		–	–	11	
MC1403 } 0°C to +70°C		–	–	7.0	
MC1403A		–	–	4.4	
Line Regulation	Reg_{line}				mV
($15\ V \leqslant V_I \leqslant 40\ V$)		–	1.2	4.5	
($4.5\ V \leqslant V_I \leqslant 15\ V$)		–	0.6	3.0	
Load Regulation ($0\ mA < I_O < 10\ mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	mA

FIGURE 2 – MC1403/1503 SCHEMATIC

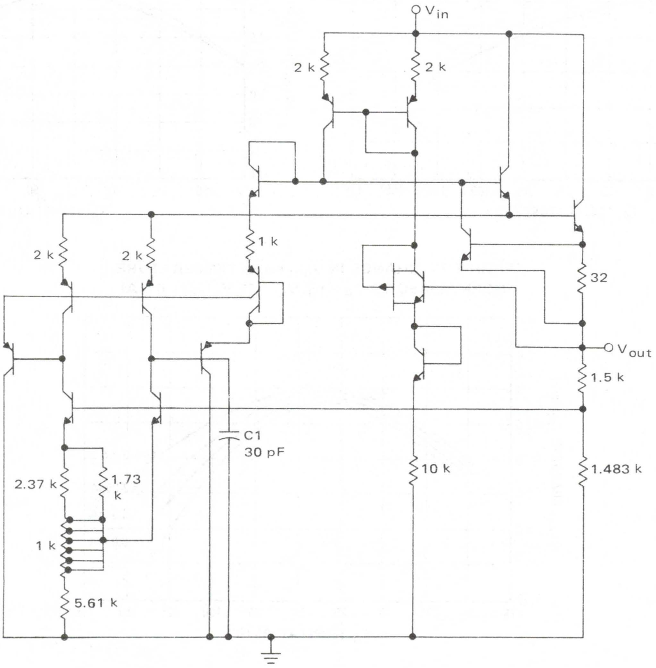


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in} (NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

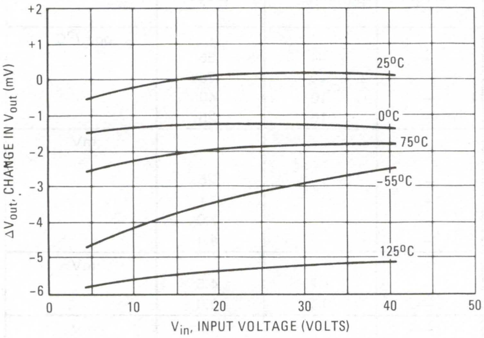


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE versus LOAD CURRENT (NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

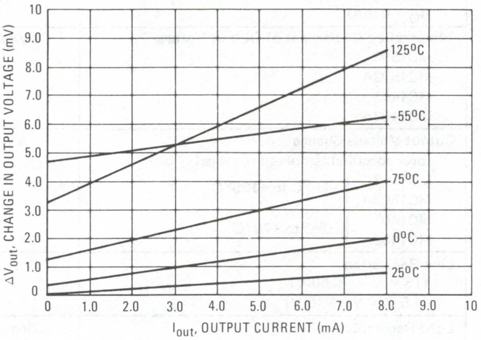


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE (V_{in} = 15 V, I_{out} = 0 mA)

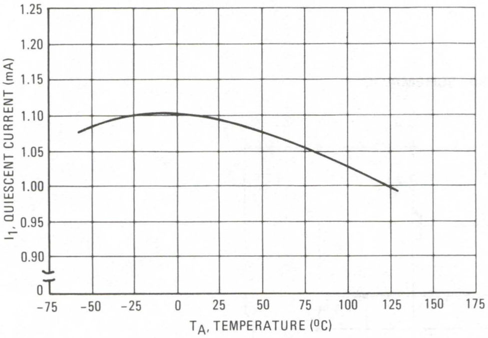


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO V_{out} @ V_{in} = 15 V)

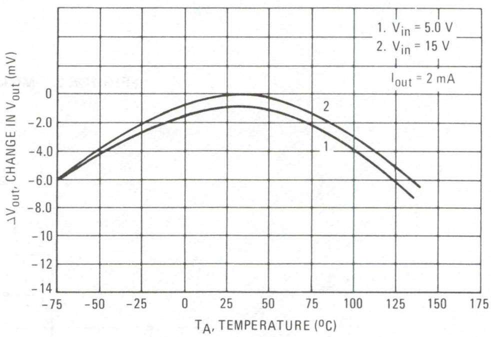
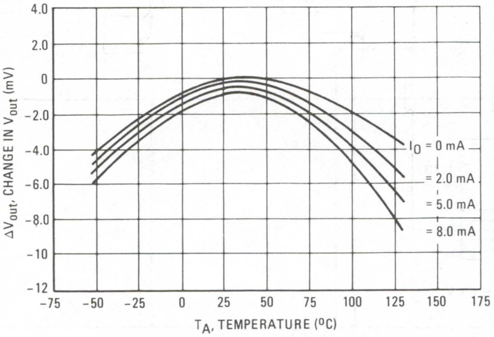


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE (NORMALIZED TO T_A = I_O, V_{in} = 15 V, I_{out} = 0 mA)



3-1/2-DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

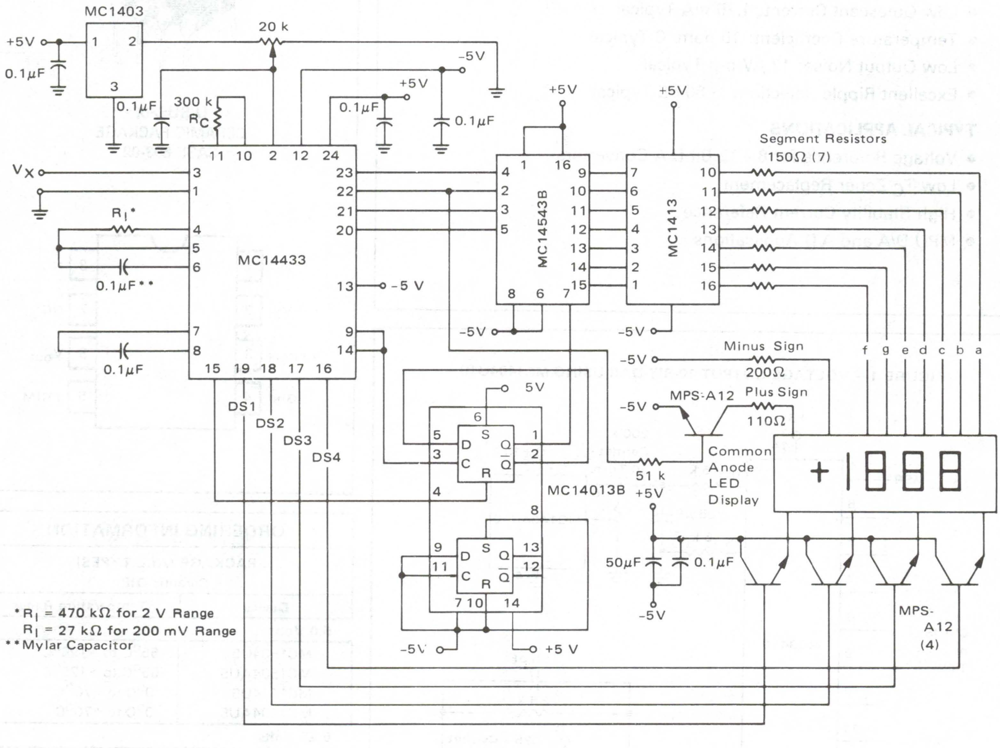
An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 — 3-1/2-DIGIT VOLTMETER


MC1403
+5V
0.1μF
1
2
3
20 k
−5V
+5V
0.1μF
300 k
R_C
0.1μF
0.1μF
11 10 2 12 24
V_X
3
1
23
22
21
20
R_I*
4
5
6
0.1μF**
MC14433
13
−5 V
7
8
9
14
0.1μF
15 19 18 17 16
DS1
DS2
DS3
DS4
+5V
+5V
MC14543B
4 1 16 9 10 11 12 13 14 15
2 3 5 8 6 7
MC1413
7 6 5 4 3 2 1
10 11 12 13 14 15 16
Segment Resistors
150Ω (7)
−5V
−5V
f g e d c b a
Minus Sign
−5V
200Ω
MPS-A12
Plus Sign
−5V
110Ω
Common
Anode
LED
Display
+1888
51 k
+5V
5V
6
5 D S Q 1
3 C R Q̄ 2
4
MC14013B
8
9 D S Q 13
11 C R Q̄ 12
7 10 14
50μF
0.1μF
−5V
−5V
+5 V
MPS-
A12
(4)

*R_I = 470 kΩ for 2 V Range
R_I = 27 kΩ for 200 mV Range
**Mylar Capacitor

MC1404,A
MC1504,A

MOTOROLA

VOLTAGE REFERENCE FAMILY

The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ±6%
- Wide Input Voltage Range: V_{ref} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

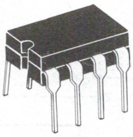
TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

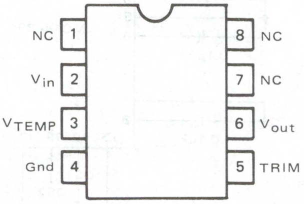
PRECISION LOW-DRIFT VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



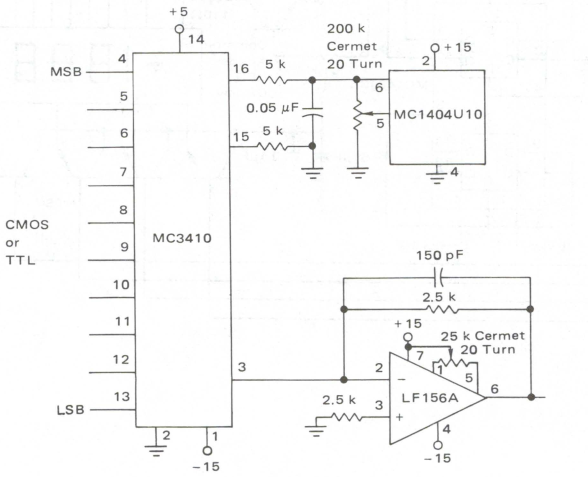
NC 1
Vin 2
VTEMP 3
Gnd 4
8 NC
7 NC
6 Vout
5 TRIM

ORDERING INFORMATION

PACKAGE (ALL TYPES)
Ceramic DIP

Device	Temperature Range
5.0 Volts	
MC1504U5	−55°C to +125°C
MC1504AU5	−55°C to +125°C
MC1404U5	0°C to +70°C
MC1404AU5	0°C to +70°C
6.25 Volts	
MC1504U6	−55°C to +125°C
MC1504AU6	−55°C to +125°C
MC1404U6	0°C to +70°C
MC1404AU6	0°C to +70°C
10 Volts	
MC1504U10	−55°C to +125°C
MC1504AU10	−55°C to +125°C
MC1404U10	0°C to +70°C
MC1404AU10	0°C to +70°C

FIGURE 1 – VOLTAGE OUTPUT 10-BIT DAC USING MC1404U10



+5
14
MSB
4
5
6
7
8
9
10
11
12
13
LSB
CMOS or TTL
MC3410
16
5 k
15
5 k
0.05 μF
200 k Cermet 20 Turn
+15
2
6
5
MC1404U10
4
2
1
−15
3
150 pF
2.5 k
+15
25 k Cermet 20 Turn
7
1
5
2
3
2.5 k
LF156A
6
4
−15

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A		
MC1504,A		-55 to +125	°C
MC1404,A		0 to +70	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504,A			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (I_O = 0 mA)	V_O							Volt
U5, AU5		4.95	5.00	5.05	4.95	5.00	5.05	
U6, AU6		6.19	6.25	6.31	6.19	6.25	6.31	
U10, AU10		9.90	10	10.10	9.90	10	10.10	
Output Voltage Tolerance	—	—	±0.1	±1.0	—	±0.1	±1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)	ΔV_{TRIM}	±6.0	—	—	±6.0	—	—	%
Output Voltage Temperature Coefficient, Over Full Temperature Range	$\Delta V_O/\Delta T$							ppm/°C
MC1404, MC1504		—	10	40	—	—	55	
MC1404A, MC1504A		—	10	25	—	—	25	
Maximum Output Voltage Change Over Temperature Range	ΔV_O							mV
MC1404U5, MC1504U5		—	—	14	—	—	50	
MC1404AU5, MC1504AU5		—	—	9.0	—	—	23	
MC1404U6, MC1504U6		—	—	17.5	—	—	62	
MC1404AU6, MC1504AU6		—	—	11	—	—	28	
MC1404U10, MC1504U10		—	—	28	—	—	99	
MC1404AU10, MC1504AU10		—	—	18	—	—	45	
Line Regulation (1) ($V_{in} = V_{out}$ + 2.5 V to 40 V, I_{out} = 0 mA)	Reg_{line}	—	2.0	6.0	—	2.0	6.0	mV
Load Regulation (1) ($0 \leqslant I_O \leqslant 10$ mA)	Reg_{load}	—	—	10	—	—	10	mV
Quiescent Current (I_O = 0 mA)	I_I	—	1.2	1.5	—	1.2	1.5	mA
Short Circuit Current	I_{SC}	15	20	30	—	—	30	mA
Long Term Stability	—	—	25	—	—	25	—	ppm/1000 hrs

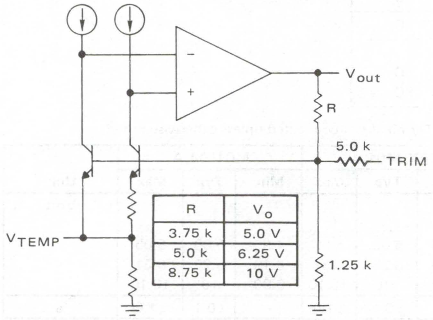
Note 1: Includes thermal effects.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504,A			Unit
		Min	Typ	Max	Min	Typ	Max	
Turn-On Settling Time (to ±0.01%)	t_S	—	50	—	—	50	—	µs
Output Noise Voltage — P to P (Bandwidth 0.1 to 10 Hz)	V_n	—	12	—	—	12	—	µV
Small-Signal Output Impedance	r_o							Ω
120 Hz		—	0.15	—	—	0.15	—	
500 Hz		—	0.2	—	—	0.2	—	
Power Supply Rejection Ratio	PSRR	70	80	—	70	80	—	dB

TYPICAL CHARACTERISTICS

FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM



R	V_o
3.75 k	5.0 V
5.0 k	6.25 V
8.75 k	10 V

FIGURE 3 – LINE REGULATION versus TEMPERATURE

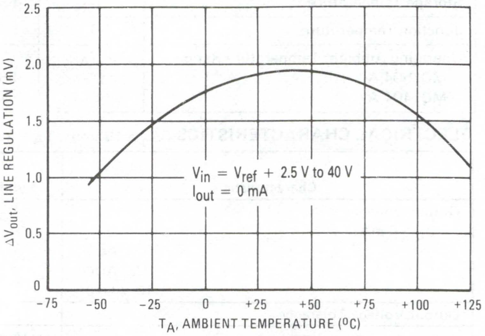


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE MC1404U10

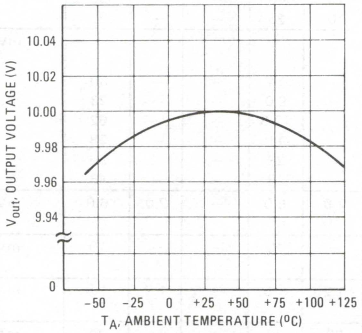


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

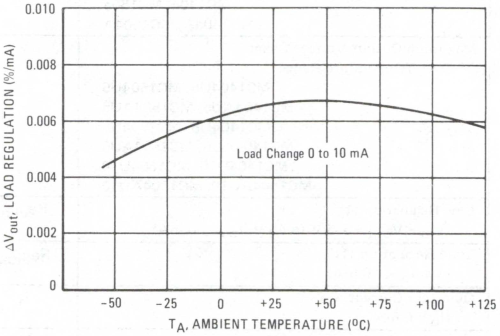


FIGURE 6 – POWER SUPPLY REJECTION RATIO versus FREQUENCY

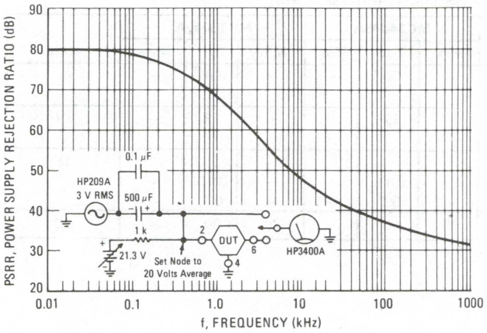


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE

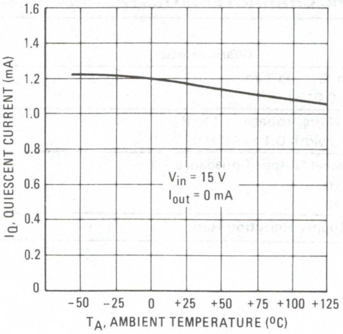


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

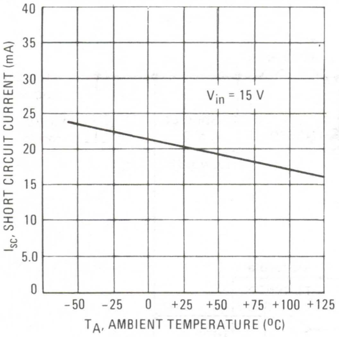


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE

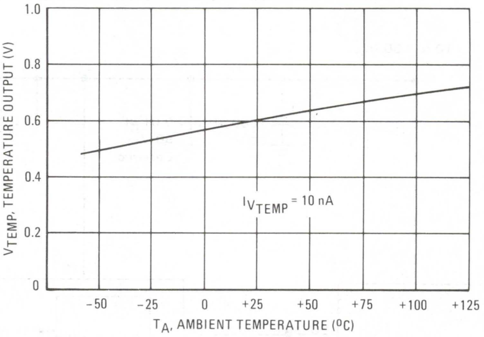
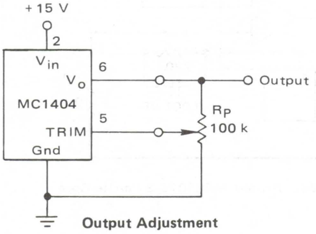


FIGURE 10 – OUTPUT TRIM CONFIGURATION

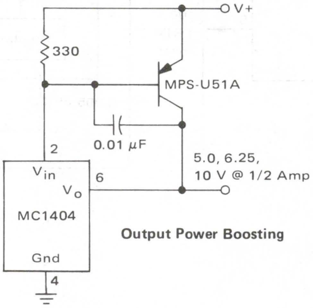

+15 V
2
V_{in}
V_o
6
Output
MC1404
5
TRIM
R_P
100 k
Gnd

Output Adjustment

The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ±6.0%.

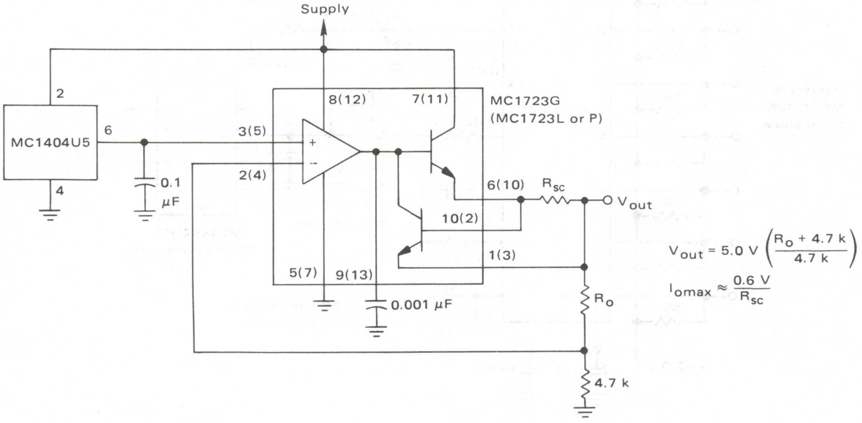
FIGURE 11 – PRECISION SUPPLY USING MC1404


V+
330
MPS-U51A
0.01 µF
2
V_{in}
6
V_o
5.0, 6.25,
10 V @ 1/2 Amp
MC1404
Gnd
4

Output Power Boosting

The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

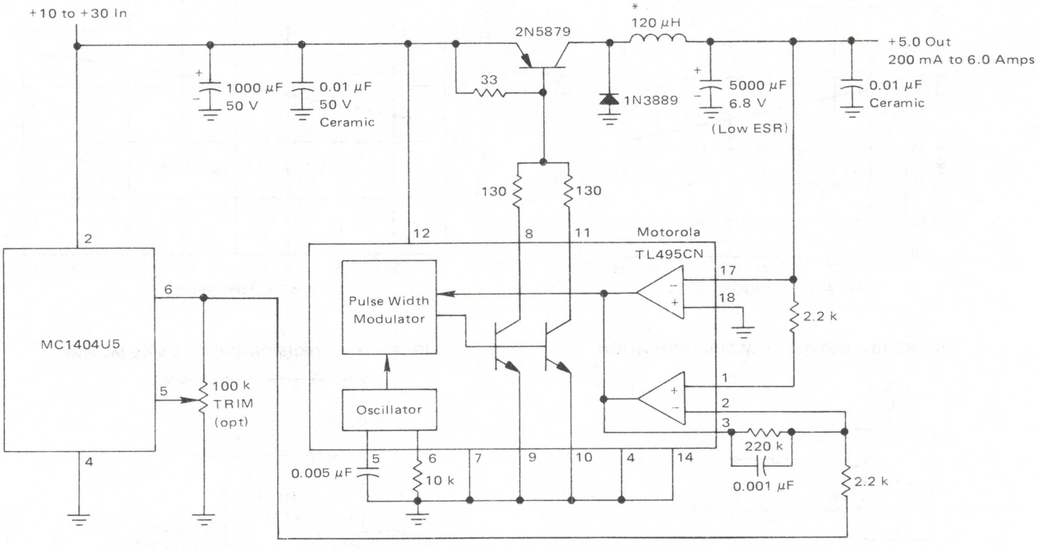
FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR


Supply
2
MC1404U5
6
4
0.1
µF
3(5)
2(4)
+
–
8(12)
7(11)
MC1723G
(MC1723L or P)
6(10)
R_{sc}
V_{out}
10(2)
1(3)
5(7)
9(13)
0.001 µF
R_o
4.7 k

$$V_{out} = 5.0\ V \left(\frac{R_o + 4.7\ k}{4.7\ k}\right)$$

$$I_{omax} \approx \frac{0.6\ V}{R_{sc}}$$

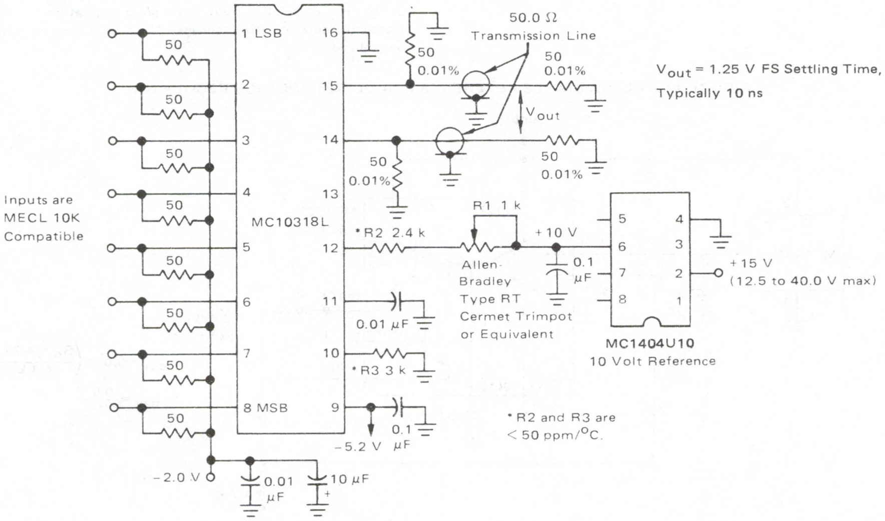
FIGURE 13 – 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE


+10 to +30 In
2N5879
*
120 µH
+5.0 Out
200 mA to 6.0 Amps
1000 µF
50 V
0.01 µF
50 V
Ceramic
33
1N3889
5000 µF
6.8 V
(Low ESR)
0.01 µF
Ceramic
130
130
Motorola
TL495CN
Pulse Width Modulator
Oscillator
MC1404U5
100 k
TRIM
(opt)
2.2 k
220 k
0.001 µF
2.2 k
0.005 µF
10 k
2
6
5
4
12
8
11
17
18
1
2
3
5
6
7
9
10
4
14

*40 Turns #16 Wire, Arnold A-894075-2 Ferrite Core

FIGURE 14 – HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10

I_{FS} is set to 51.000 mA with R1


Inputs are
MECL 10K
Compatible
50
1 LSB
2
3
4
5
6
7
8 MSB
16
15
14
13
12
11
10
9
MC10318L
50.0 Ω
Transmission Line
50
0.01%
50
0.01%
Vout
50
0.01%
50
0.01%
R1 1 k
*R2 2.4 k
Allen-
Bradley
Type RT
Cermet Trimpot
or Equivalent
+10 V
0.1 µF
0.01 µF
*R3 3 k
0.1 µF
-5.2 V
-2.0 V
0.01 µF
10 µF
MC1404U10
10 Volt Reference
+15 V
(12.5 to 40.0 V max)

V_{out} = 1.25 V FS Settling Time, Typically 10 ns

*R2 and R3 are < 50 ppm/°C.

MOTOROLA

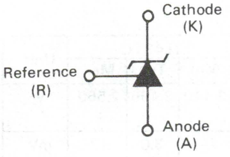
TL431 series

Specifications and Applications Information

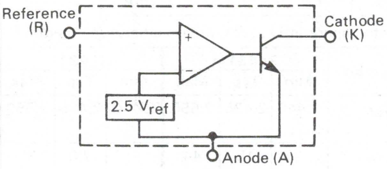
PROGRAMMABLE PRECISION REFERENCES

The TL431 integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

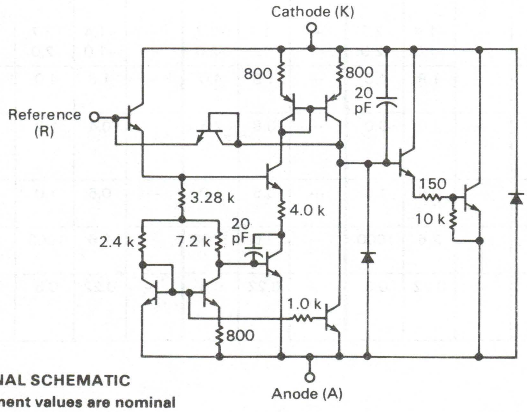
- Programmable Output Voltage to 36 Volts
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage


Cathode (K)
Reference (R)
Anode (A)

SYMBOL


Reference (R)
Cathode (K)
+
−
2.5 Vref
Anode (A)

FUNCTIONAL BLOCK DIAGRAM


Cathode (K)
800
800
20 pF
Reference (R)
3.28 k
4.0 k
150
10 k
2.4 k
7.2 k
20 pF
1.0 k
800
Anode (A)

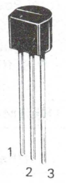
INTERNAL SCHEMATIC
Component values are nominal

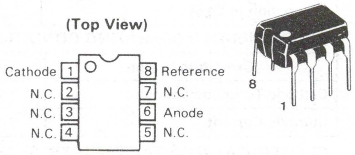
PROGRAMMABLE PRECISION REFERENCES

SILICON MONOLITHIC INTEGRATED CIRCUITS

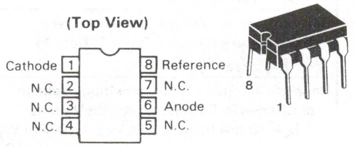
LP SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)

Pin 1. Reference
2. Anode
3. Cathode




(Top View)
Cathode 1
N.C. 2
N.C. 3
N.C. 4
8 Reference
7 N.C.
6 Anode
5 N.C.
8
1

P SUFFIX
PLASTIC DUAL-IN-LINE PACKAGE
CASE 626-04


(Top View)
Cathode 1
N.C. 2
N.C. 3
N.C. 4
8 Reference
7 N.C.
6 Anode
5 N.C.
8
1

JG SUFFIX
CERAMIC DUAL-IN-LINE PACKAGE
CASE 693-02

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP	0 to +70°C	Plastic TO-92
TL431CP	0 to +70°C	Plastic DIP
TL431CJG	0 to +70°C	Ceramic DIP
TL431ILP	−40 to +85°C	Plastic TO-92
TL431IP	−40 to +85°C	Plastic DIP
TL431IJG	−40 to +85°C	Ceramic DIP
TL431MJG	−55 to +125°C	Ceramic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	-100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	-0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I TL431C	T_A	 -55 to +125 -40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C Ambient Temperature LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.775 1.10 1.25	W
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C Case Temperature LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

THERMAL CHARACTERISTICS

Characteristics	Symbol	LP Suffix Package	P Suffix Package	JG Suffix Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, $I_K = 10$ mA	V_{ref}	2.440	2.495	2.550	2.440	2.495	2.550	2.440	2.495	2.550	V
Reference Input Voltage Deviation Over Temperature Range. (Figure 1, Note 1) $V_{KA} = V_{ref}$, $I_K = 10$ mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_K = 10$ mA (Figure 2), $\Delta V_{KA} = 10$ V to V_{ref} $\Delta V_{KA} = 36$ V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 -1.4 -1.0	 -2.7 -2.0	 — —	 -1.4 -1.0	 -2.7 -2.0	 — —	 -1.4 -1.0	 -2.7 -2.0	mV/V
Reference Input Current (Figure 2) $I_K = 10$ mA, R1 = 10 k, R2 = ∞	I_{ref}	—	1.8	4.0	—	1.8	4.0	—	1.8	4.0	µA
Reference Input Current Deviation Over Temperature Range. (Figure 2) $I_K = 10$ mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) $V_{KA} = 36$ V, $V_{ref} = 0$ V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 2) $V_{KA} = V_{ref}$, $\Delta I_K = 1.0$ mA to 100 mA $f \leqslant 1.0$ kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

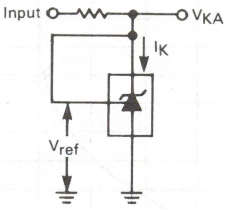
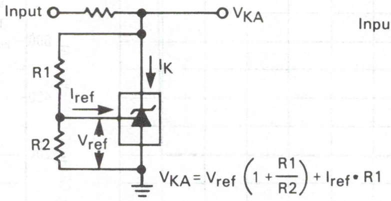
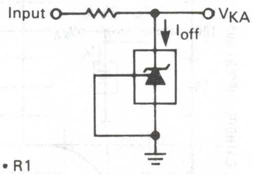


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$



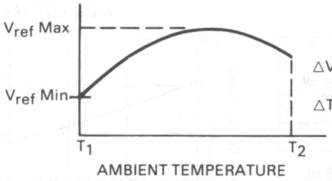
$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \cdot R1$$

FIGURE 3 — TEST CIRCUIT FOR I_{off}



Note 1

The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



$\Delta V_{ref} = V_{ref}$ Max — V_{ref} Min

$\Delta T_A = T_2 - T_1$

The average temperature coefficient of the reference input voltage, $\alpha\ V_{ref}$, is defined as:

$$\alpha\ V_{ref}\ \frac{\text{ppm}}{^\circ\text{C}} = \frac{\left(\dfrac{\Delta V_{ref}}{V_{ref}\ @\ 25^\circ\text{C}}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\ (V_{ref}\ @\ 25^\circ\text{C})}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: $\Delta V_{ref} = 8.0$ mV and slope is positive, V_{ref} @ 25°C = 2.495 V, $\Delta T_A = 70^\circ$C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ \text{ppm}/^\circ\text{C}$$

Note 2

The dynamic impedance Z_{ka} is defined as:

$$|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}'| \approx |Z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

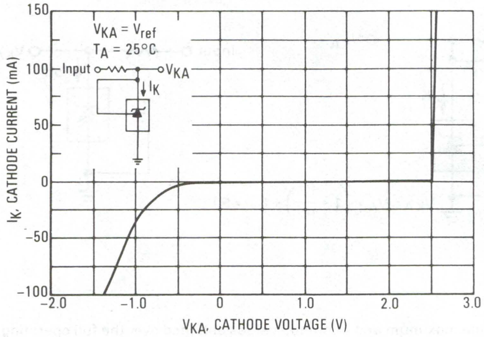


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

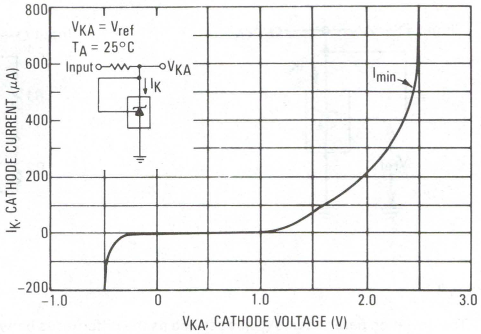


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

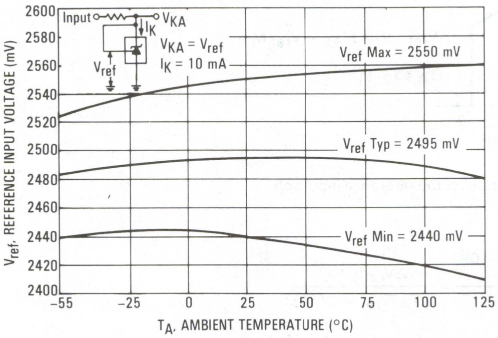


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

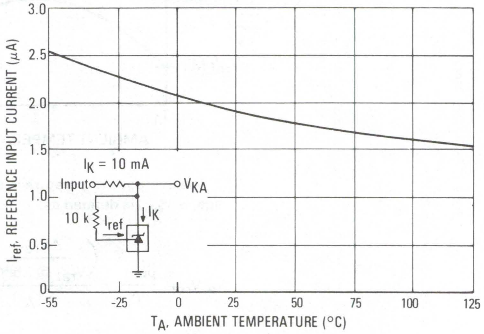


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

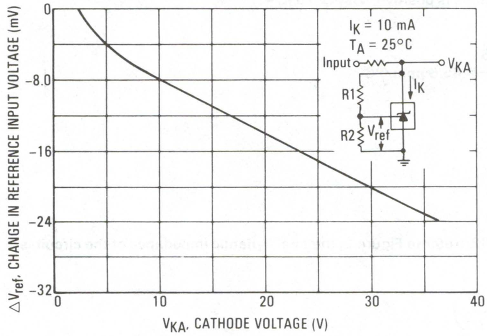


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

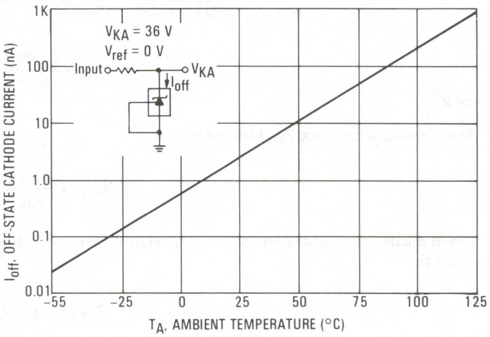


FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY

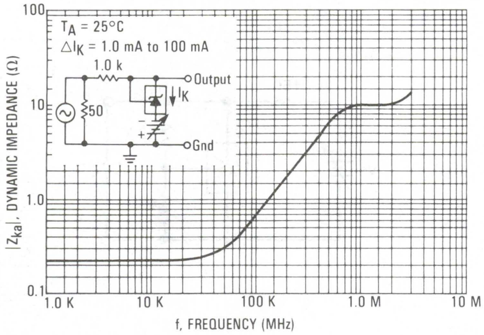


FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE

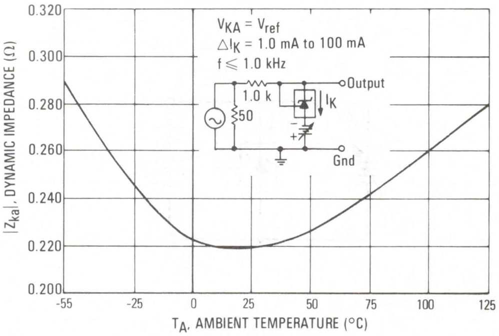


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

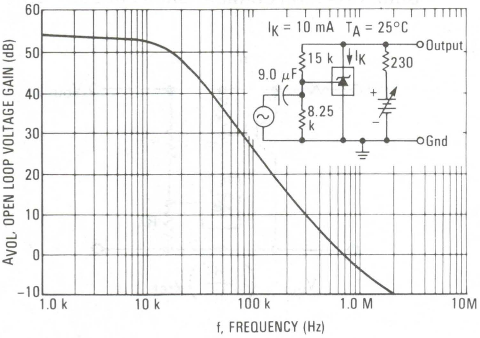


FIGURE 13 — SPECTRAL NOISE DENSITY

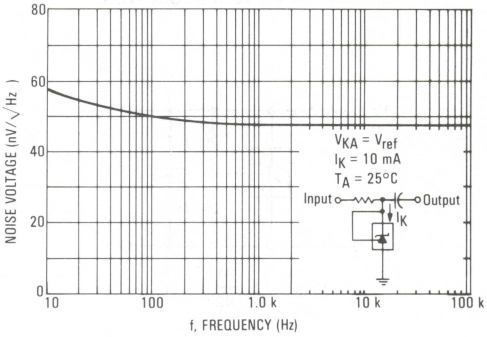


FIGURE 14 — PULSE RESPONSE

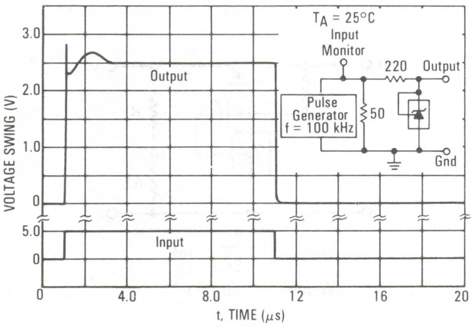


FIGURE 15 — STABILITY BOUNDARY CONDITIONS

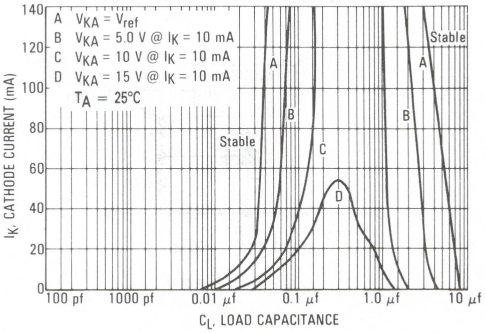


FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

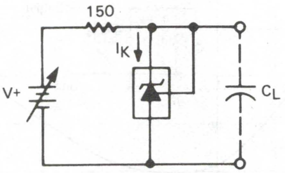
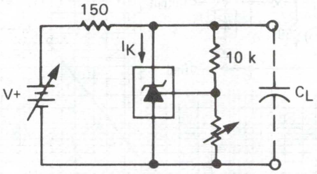
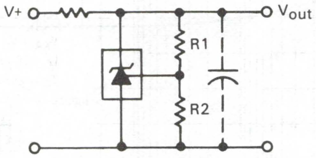


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS


150
I_K
10 k
V+
C_L

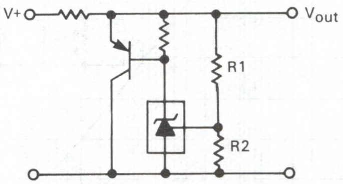
TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR



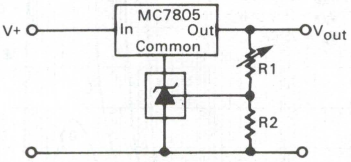
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 19 — HIGH CURRENT SHUNT REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

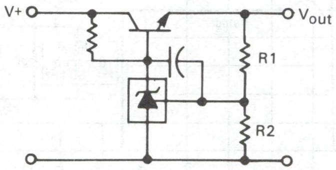
FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR


MC7805
In
Out
Common
V+
V_{out}
R1
R2

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + 5.0 V

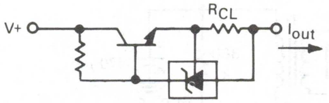
FIGURE 21 — SERIES PASS REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

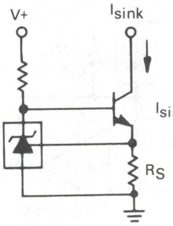
V_{out} Min = V_{ref} + 5.0 V

FIGURE 22 — CONSTANT CURRENT SOURCE



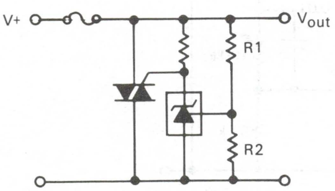
$I_{out} = \frac{V_{ref}}{R_{CL}}$

FIGURE 23 — CONSTANT CURRENT SINK



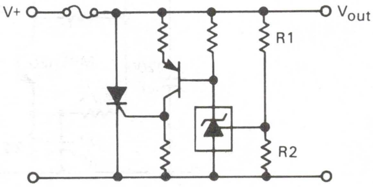
$I_{sink} = \frac{V_{ref}}{R_S}$

FIGURE 24 — TRIAC CROWBAR



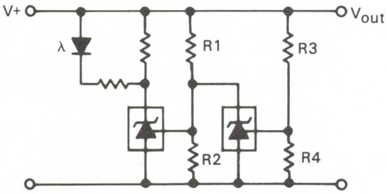
$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$

FIGURE 25 — SCR CROWBAR



$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$

FIGURE 26 — VOLTAGE MONITOR

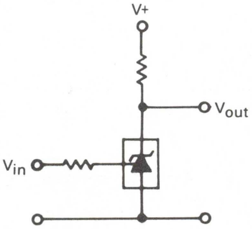

V+
V_{out}
λ
R1
R3
R2
R4

L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

Lower Limit $= \left(1 + \frac{R1}{R2}\right)V_{ref}$

Upper Limit $= \left(1 + \frac{R3}{R4}\right)V_{ref}$

FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



$V_{th} = V_{ref}$

V_{in}	V_{out}
$<V_{ref}$	V+
$>V_{ref}$	≈ 2.0 V

FIGURE 28 — LINEAR OHMMETER

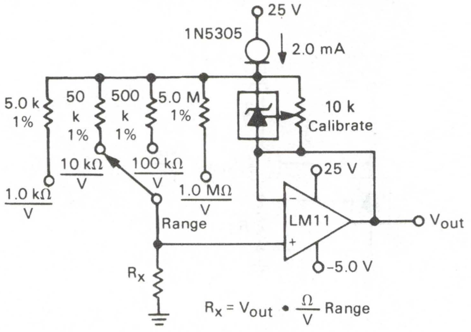

25 V
1N5305
2.0 mA
5.0 k 1%
50 k 1%
500 k 1%
5.0 M 1%
10 k Calibrate
10 kΩ/V
100 kΩ/V
1.0 kΩ/V
1.0 MΩ/V
25 V
Range
LM11
Vout
-5.0 V
Rx
Rx = Vout • Ω/V Range

FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

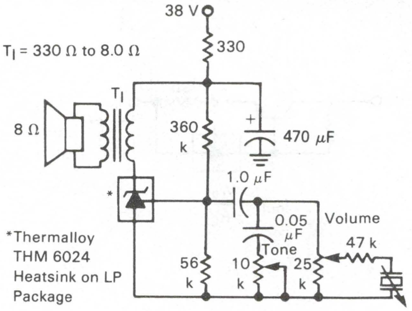
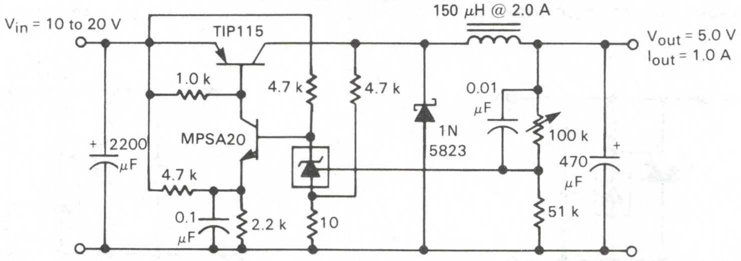
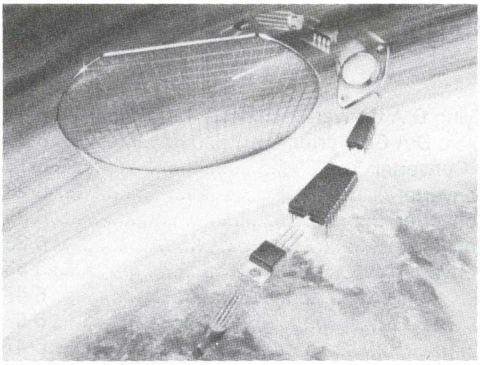

38 V
330
Tl = 330 Ω to 8.0 Ω
Tl
8 Ω
360 k
470 μF
1.0 μF
*
0.05 μF
Volume
Tone
47 k
*Thermalloy THM 6024 Heatsink on LP Package
56 k
10 k
25 k

FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER


150 μH @ 2.0 A
Vin = 10 to 20 V
TIP115
Vout = 5.0 V
Iout = 1.0 A
1.0 k
4.7 k
4.7 k
0.01 μF
MPSA20
100 k
2200 μF
1N 5823
470 μF
4.7 k
51 k
0.1 μF
2.2 k
10

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%



Data Conversion

6

DATA CONVERSION

Device	Function	Page
AD562	Complete High-Speed 12-Bit Multiplying D/A Converter	6-3
AD563	Complete 12-Bit High-Speed Monolithic D/A Converter	6-8
DAC-08	High-Speed 8-Bit Multiplying D-to-A Converter	6-13
MC1406L	6-Bit Multiplying Digital-to-Analog Converter	6-23
MC1408	8-Bit Multiplying Digital-to-Analog Converter	6-35
MC1506L	6-Bit Multiplying Digital-to-Analog Converter	6-23
MC1508	8-Bit Multiplying Digital-to-Analog Converter	6-35
MC3410,C	10-Bit D-to-A Converter	6-47
MC3412	High-Speed 12-Bit D/A Converter	6-58
MC3510	10-Bit D-to-A Converter	6-47
MC3512	High-Speed 12-Bit D/A Converter	6-58
MC6890	8-Bit Bus-Compatible MPU D/A Converter	6-63
MC10315L	Seven-Bit Parallel High-Speed A/D Converter	6-70
MC10317L	Seven-Bit Parallel High-Speed A/D Converter	6-70
MC10318L,L9,CL6,CL7	High-Speed 8-Bit D/A Converter	6-77

MOTOROLA

AD562

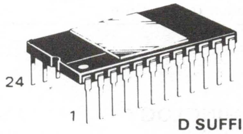
LASER TRIMMED HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

COMPLETE HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

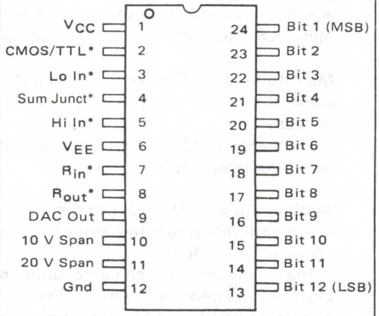
The AD562 is a monolithic 12-bit resolution D/A converter. Active laser trimming of thin-film ladder network, span and bipolar offset resistors at wafer level provide linearity of better than ±1/2 LSB. An innovative bit switching scheme provides fast settling time yet enables selection of CMOS or TTL thresholds which are retained over a wide V_{CC} range from 4.5 to 16.5 volts. Internal precision span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. The AD562 multiplies in two quadrants when varying the reference input voltage. 12-bit accuracy and fast settling time make this converter ideal for applications such as fast A/D converters, CRT display generation waveform synthesis, precision instruments, and data acquisition systems.

- True 12-Bit Linearity: ±1/2 LSB Max
- Fast Settling Time: ±1/2 LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- Low Gain Drift: 3 ppm/°C Max
- True Binary Coded Inputs
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage
- Low Power Consumption: 210 mW



D SUFFIX
CERAMIC PACKAGE
CASE 716-06

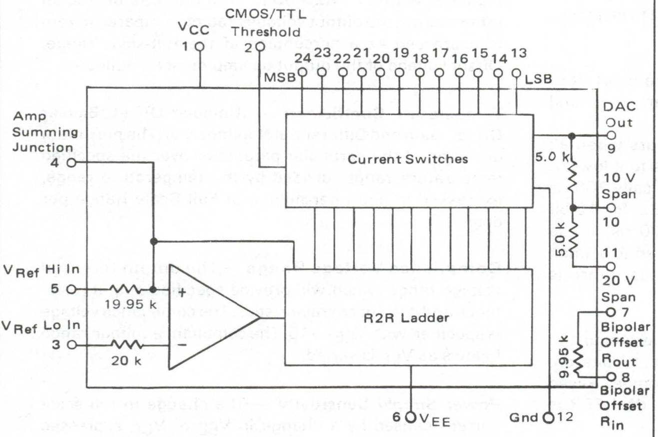
PIN CONNECTIONS



V_{CC} 1
CMOS/TTL* 2
Lo In* 3
Sum Junct* 4
Hi In* 5
V_{EE} 6
R_{in}* 7
R_{out}* 8
DAC Out 9
10 V Span 10
20 V Span 11
Gnd 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

Pin 2 = CMOS/TTL Threshold
Pin 3 = V_{Ref} Lo In
Pin 4 = Amp Summing Junction
Pin 5 = V_{Ref} Hi In
Pin 7 = Bipolar Offset R_{in}
Pin 8 = Bipolar Offset R_{out}

BLOCK DIAGRAM



V_{CC} 1
CMOS/TTL Threshold 2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Amp Summing Junction 4
Current Switches
5.0 k
DAC Out 9
10 V Span 10
5.0 k
11
20 V Span 7
V_{Ref} Hi In 5
19.95 k
+
−
R2R Ladder
V_{Ref} Lo In 3
20 k
9.95 k
Bipolar Offset R_{out} 8
Bipolar Offset R_{in}
6 V_{EE}
Gnd 12

ORDERING INFORMATION

Device	Temperature Range	Accuracy @ 25°C
AD562KD	0°C to +70°C	±1/2 LSB
AD562AD	−25°C to +85°C	±1/2 LSB
AD562SD	−55°C to +125°C	±1/4 LSB

MAXIMUM RATING (T_A = 25°C, Ratings are referred to Ground [Pin 12] unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+18 -18	Vdc
Digital Input Voltage (Pins 13 to 24)		V_I	-5.0 to +18	Vdc
CMOS/TTL Threshold Select (Pin 2)		—	0 to V_{CC}	Vdc
V_{Ref} Hi In (Pin 5)		—	V_{EE} to V_{CC}	Vdc
V_{Ref} Lo In (Pin 3)		—	±1.0	Vdc
Applied Output Voltage (Pin 9)		V_O	-7.0 to V_{CC}	Vdc
Bipolar Offset to Analog Ground (Pin 7 or 8)		—	V_{EE} to V_{CC}	Vdc
Ten Volt Span Resistor to Analog Ground (Pin 10)		—	V_{EE} to V_{CC}	Vdc
Twenty Volt Span Resistor to Analog Ground (Pin 11)		—	V_{EE} to V_{CC}	Vdc
Power Dissipation		P_D	1000	mW
Operating Temperature Range	AD562KD AD562AD AD562SD	T_A	0 to +70 -25 to +85 -55 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Junction Temperature		T_J	+175	°C

TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to nonmonotonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases.

The complete AD562 Series is guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ±1/2 LSB for 12-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

Unipolar Offset Error — Using the configuration shown in Figure 1, with R1 = 50 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Offset Error — Using the configuration shown in Figure 2, with R2 = 50 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Zero Error — Using the configuration shown in Figure 2, with R1 = R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

Temperature Coefficients — (Unipolar Offset, Bipolar Offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

Compliance Voltage Range — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with $V_{EE} = -15$. The compliance voltage range follows as V_{EE} is varied.

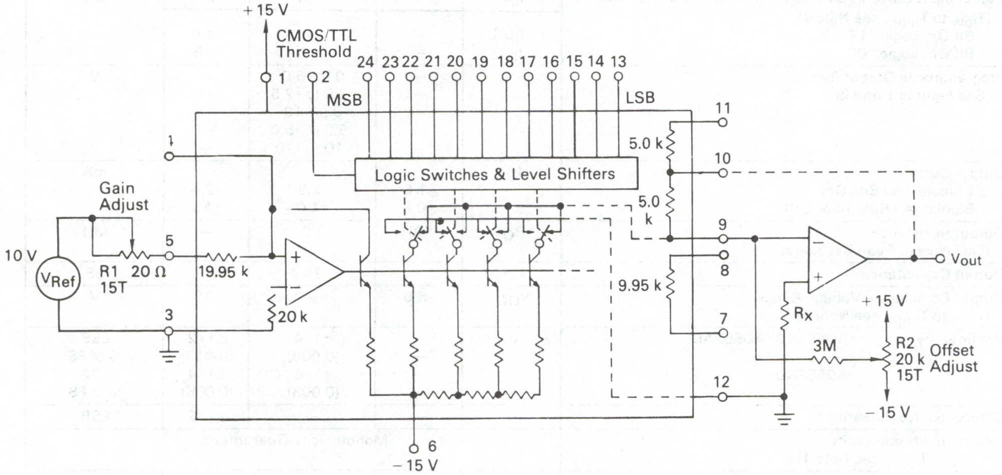
Power Supply Sensitivity — The change in full scale current caused by a change in V_{EE} or V_{CC} expressed in ppm of full scale current per percent change in V_{EE} or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, V_{Ref} = 10 V, Pin 2 open, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TTL Digital Logic Levels (All Bits) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1)					V
Bit On, Logic "1"	V_{IH}	2.0	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	0.8	
CMOS Digital Logic Levels (All Pins) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1, Pin 2 tied to Pin 1)					V
Bit On, Logic "1"	V_{IH}	70% V_{CC}	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	30% V_{CC}	
Digital Input Current, CMOS/TTL Levels — Bit On, Logic "1"	I_{IH}	—	+0.02	+0.1	µA
(T_{low} to T_{high}, see Note 1)					
Bit On, Logic "1"	I_{IH}	—	—	+1.0	
Bit Off, Logic "0"	I_{IL}	—	−2.0	−75	
Programmable Output Range (See Figures 1 and 2)	—	—	0 to +5.0	—	V
		—	−2.5 to +2.5	—	
		—	0 to +10	—	
		—	−5.0 to +5.0	—	
		—	−10 to +10	—	
Output Current	I_O				mA
Unipolar (All Bits On)		−1.6	−2.0	−2.4	
Bipolar (All Bits On or Off)		±0.8	±1.0	±1.2	
Output Resistance (Exclusive of Span Resistors)	R_O	1.0	5.0	—	MΩ
Output Capacitance	C_O	—	25	—	pF
Output Compliance Voltage Range (T_{low} to T_{high}, see Note 1)	V_{OC}	−5.0	—	+10	V
Nonlinearity AD562KD/AD562AD	NL	—	±1/4	±1/2	LSB
		—	(0.006)	(0.012)	% of FS
AD562SD		—	±1/8	±1/4	LSB
		—	(0.003)	(0.006)	% of FS
Differential Nonlinearity	—	—	—	±1/2	LSB
Differential Nonlinearity (T_{low} to T_{high}, see Note 1)	Monotonicity Guaranteed				
Gain Error — Figure 1, R1 = Fixed 50 Ω	—	—	±0.05	±0.15	% of FS
Offset Error	—				% of FS
Unipolar — Figure 1		—	±0.01	±0.05	
Bipolar — Figure 2, R2 = Fixed 50 Ω		—	±0.05	±0.15	
Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 50 Ω	—	—	±0.05	±0.15	% of FS
Gain Adjustment Range — Figure 1	—	±0.20	±0.25	—	% of FS
Bipolar Offset Adjustment Range — Figure 2	—	±0.20	±0.25	—	% of FS
Temperature Coefficients (T_{low} to T_{high}, see Note 1)	—				ppm/°C
Unipolar Zero — AD562KD/AD562AD		—	—	1.0	
AD562SD		—	—	2.0	
Bipolar Zero — All Devices		—	—	4.0	
Gain — All Devices		—	—	3.0	
Differential Nonlinearity — All Devices		—	1.0	—	
Settling Time to 1/2 LSB All Bits On-to-Off or Off-to-On	t_s	—	0.2	1.0	µs
Reference Input Impedance	Z_{in}	15	20	25	kΩ
Power Supply Current					mA
(V_{CC} +4.5 to +16.5 Vdc)	I_{CC}	—	6.0	10	
(V_{EE} −10.8 to −16.5 Vdc)	I_{EE}	—	−8.0	−12	
Power Supply Gain Sensitivity					ppm of FS/%
(V_{CC} +4.5 to 5.5 Vdc)	$PSSI_{FS+}$	—	—	2.0	
(V_{CC} +13.5 to +16.5 Vdc)	$PSSI_{FS+}$	—	—	2.0	
(V_{EE} −10.8 to −16.5 Vdc)	$PSSI_{FS-}$	—	—	6.0	

Note 1:	T_{high}
T_{low} = −55°C for AD562SD	= +125°C for AD562SD
−25°C for AD562AD	+85°C for AD562AD
0°C for AD562KD	+70°C for AD562KD

FIGURE 1 — AD562 IN TYPICAL UNIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
1
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
11
5.0 k
10
Logic Switches & Level Shifters
5.0 k
9
8
9.95 k
7
12
Gain Adjust
10 V
VRef
R1 20 Ω 15T
5
19.95 k
20 k
3
6
−15 V
Vout
+15 V
Rx
3M
R2 20 k 15T
Offset Adjust
−15 V

UNIPOLAR DAC OPERATION

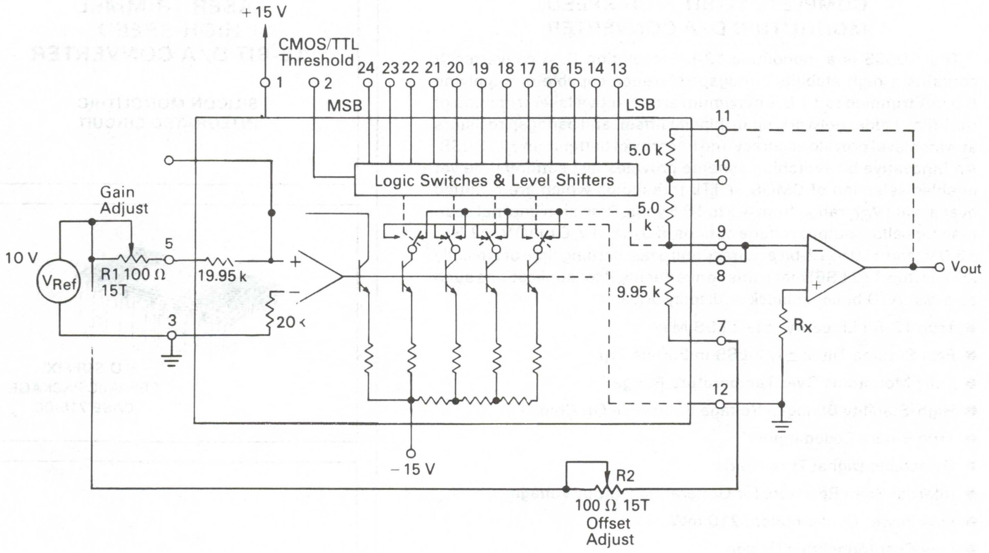
A typical circuit configuration for unipolar operation of AD562 is shown in Figure 1.

Step 1 — Output Range
Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

Step 2 — Zero Adjust
Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

Step 3 — Gain Adjust
Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — AD562 IN TYPICAL BIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
1
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
11
5.0 k
10
Logic Switches & Level Shifters
5.0 k
9
8
9.95 k
Vout
Gain Adjust
10 V
VRef
R1 100 Ω 15T
5
19.95 k
3
20 k
7
Rx
12
−15 V
R2
100 Ω 15T
Offset Adjust

BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of AD562 is shown in Figure 2.

Step 1 — Output Range
Determine which output range is required. For ±2.5 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

Step 2 — Offset Adjust
Turn all bits OFF and adjust R2 until operational amplifier output is:

-2.5000 Volt for ±2.5 Volt range
-5.0000 Volt for ±5.0 Volt range
-10.0000 Volt for ±10 Volt range

Step 3 — Gain Adjust (Bipolar Zero)
Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

NOTES:

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For high voltage CMOS compatibility, short Pin 2 to Pin 1.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, R_X should be made equal to the internal feedback resistor. In bipolar, R_X, equals the feedback resistor in parallel with 10 k.

AD563

MOTOROLA

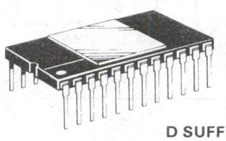
COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

The AD563 is a monolithic 12-bit resolution D/A converter. It contains a high stability bandgap reference capable of supplying 5.0 mA trimmed to ±1.0% maximum error. Active laser trimming of thin-film ladder network, span, bipolar offset, and bandgap resistors at wafer level provide accuracy and linearity of better than ±1/2 LSB. An innovative bit switching scheme provides fast settling time yet enables selection of CMOS or TTL thresholds which are retained over a wide V_{CC} range from 4.5 to 16.5 volts. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±1/2 LSB) make this converter ideal for applications such as a fast A/D building block or display driver.

- True 12-Bit Linearity: ±1/2 LSB Max
- Fast Settling Time: ±1/2 LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- High-Stability Bandgap Voltage Reference On Chip
- True Binary Coded Inputs
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage
- Low Power Consumption: 210 mW
- Low Cost Monolithic Design

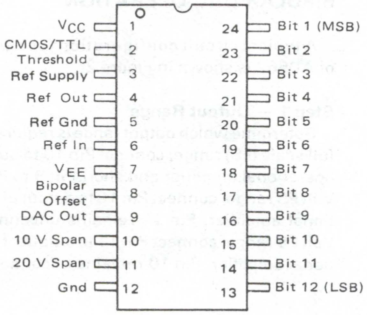
LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



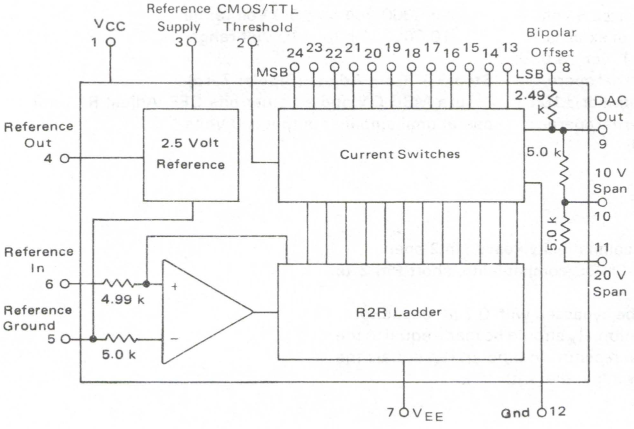
D SUFFIX
CERAMIC PACKAGE
CASE 716-06

PIN CONNECTIONS



V_{CC} 1
CMOS/TTL Threshold 2
Ref Supply 3
Ref Out 4
Ref Gnd 5
Ref In 6
V_{EE} 7
Bipolar Offset 8
DAC Out 9
10 V Span 10
20 V Span 11
Gnd 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

BLOCK DIAGRAM



V_{CC} 1
Reference Supply 3
CMOS/TTL Threshold 2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Bipolar Offset 8
2.49 k
DAC Out 9
5.0 k
10 V Span 10
5.0 k
11
20 V Span
Reference Out 4
2.5 Volt Reference
Current Switches
Reference In 6
4.99 k
Reference Ground 5
5.0 k
+
−
R2R Ladder
7 V_{EE}
Gnd 12

ORDERING INFORMATION

Device	Temperature Range	Accuracy @ 25°C	Gain TC (ppm of FS/°C)
AD563JD	0°C to +70°C	±1/2 LSB	30
AD563KD	0°C to +70°C	±1/4 LSB	20
AD563SD	-55°C to +125°C	±1/4 LSB	30
AD563TD	-55°C to +125°C	±1/4 LSB	10

MAXIMUM RATING (T_A = 25°C, Ratings are referred to Ground [Pin 12] unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+18 −18	Vdc
Reference Ground (Pin 5)		V_{AD}	±1.0	Vdc
Applied Output Voltage (Pin 9)		V_O	−7.0 to +12	Vdc
CMOS/TTL Threshold Select (Pin 2)		—	0 to V_{CC}	Vdc
Digital Input Voltage (Pins 13 to 24)		V_I	−5.0 to +18	Vdc
Reference Input to Reference Ground		V_{RI}	±12	Vdc
Reference Current		I_{REF}	Short circuit to either Gnd; momentary short circuit to V_{CC}	
Bipolar Offset to Reference Ground		—	±12	Vdc
Ten Volt Span Resistor to Reference Ground		—	±12	Vdc
Twenty Volt Span Resistor to Reference Ground		—	±24	Vdc
Power Dissipation		P_D	1000	mW
Operating Temperature Range	AD563JD/AD563KD AD563SD/AD563TD	T_A	0 to +70 −55 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Junction Temperature		T_J	+175	°C

TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to nonmonotonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases.

The AD563 is guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ±1/2 LSB for 12-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

Unipolar Offset Error — Using the configuration shown in Figure 1, with R1 = 10 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Offset Error — Using the configuration shown in Figure 2, with R2 = 10 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Zero Error — Using the configuration shown in Figure 2, with R1 = R2 = 10 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

Temperature Coefficients — (Unipolar Offset, Bipolar Offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

Compliance Voltage Range — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with $V_{EE} = -15$. The compliance voltage range follows as V_{EE} is varied.

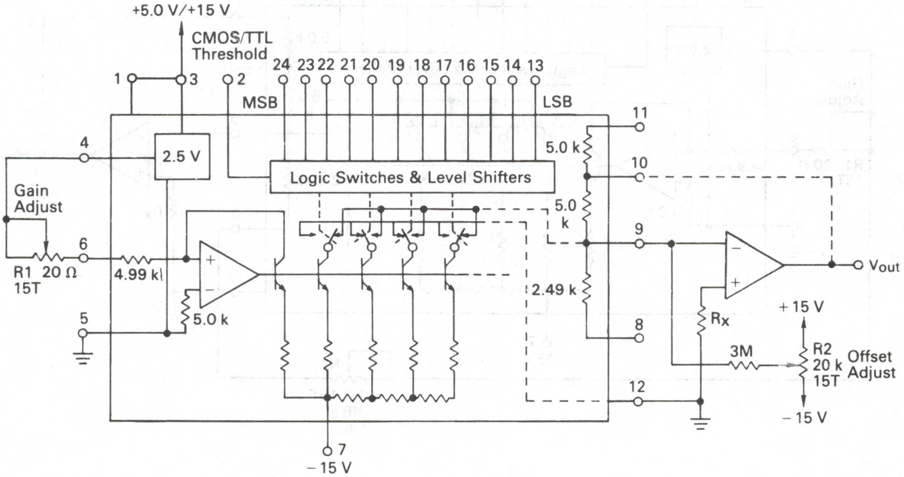
Power Supply Sensitivity — The change in full scale current caused by a change in V_{EE} or V_{CC} expressed in ppm of full scale current per percent change in V_{EE} or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −15 V, Pin 2 open, T_A = 25°C, all tests performed using internal reference, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TTL Digital Logic Levels (All Bits) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1)					V
Bit On, Logic "1"	V_{IH}	2.0	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	0.8	
CMOS Digital Logic Levels (All Pins) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1, Pin 2 tied to Pin 1)					V
Bit On, Logic "1"	V_{IH}	70% V_{CC}	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	30% V_{CC}	
Digital Input Current, CMOS/TTL Levels — Bit On, Logic "1"	I_{IH}	—	+0.02	+0.1	μA
(T_{low} to T_{high}, see Note 1)					
Bit On, Logic "1"	I_{IH}	—	—	+1.0	
Bit Off, Logic "0"	I_{IL}	—	−2.0	−75	
Programmable Output Range (See Figures 1 and 2)	—	—	0 to +5.0	—	V
		—	−2.5 to +2.5	—	
		—	0 to +10	—	
		—	−5.0 to +5.0	—	
		—	−10 to +10	—	
Output Current	I_O				mA
Unipolar (All Bits On)		−1.6	−2.0	−2.4	
Bipolar (All Bits On or Off)		±0.8	±1.0	±1.2	
Output Resistance (Exclusive of Span Resistors)	R_O	1.0	5.0	—	MΩ
Output Capacitance	C_O	—	25	—	pF
Output Compliance Voltage Range (T_{low} to T_{high}, see Note 1)	V_{OC}	−5.0	—	+10	V
Nonlinearity AD563KD/AD563SD/AD563TD	NL	—	—	±1/4	LSB
		—	—	(0.006)	% of FS
AD563JD		—	—	±1/2	LSB
		—	—	(0.012)	% of FS
Differential Nonlinearity	—	—	—	±1/2	LSB
Differential Nonlinearity (T_{low} to T_{high}, see Note 1)	Monotonicity Guaranteed				
Gain Error — Figure 1, R1 = Fixed 10 Ω	—	—	±0.1	—	% of FS
Offset Error	—				% of FS
Unipolar — Figure 1		—	±0.01	±0.05	
Bipolar — Figure 2, R2 = Fixed 10 Ω		—	±0.1	—	
Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 10 Ω	—	—	±0.1	—	% of FS
Gain Adjustment Range — Figure 1	—	—	±0.2	—	% of FS
Bipolar Offset Adjustment Range — Figure 2	—	—	±0.2	—	% of FS
Unipolar Zero Temperature Coefficient (T_{low} to T_{high}, see Note 1)	—	—	1.0	2.0	ppm/°C
Bipolar Zero Temperature Coefficient (T_{low} to T_{high}, see Note 1)	—	—	5.0	10	ppm/°C
Gain Temperature Coefficient, Full Scale (T_{low} to T_{high}, see Note 1)	—				ppm/°C
AD563TD		—	—	10	
AD563KD		—	—	20	
AD563JD/AD563SD		—	—	30	
Differential Nonlinearity Temperature Coefficient (T_{low} to T_{high}, see Note 1)	—	—	1.0	—	ppm/°C
Settling Time to 1/2 LSB All Bits On-to-Off or Off-to-On	t_s	—	0.2	1.2	μs
Reference Input Impedance	Z_{in}	—	5 k	—	kΩ
Reference Output Voltage	V_{RO}	2.475	2.500	2.525	Volts
Reference Output Current	I_{RO}	5.0	—	—	mA
Power Supply Current					mA
(V_{CC} +4.5 to +16.5 Vdc)	I_{CC}	—	6.0	10	
(V_{EE} −10.8 to −16.5 Vdc)	I_{EE}	—	−8.0	−12	
Power Supply Gain Sensitivity					ppm of FS/%
(V_{CC} +4.5 to +5.5 Vdc)	$PSSI_{FS+}$	—	2.0	10	
(V_{CC} +13.5 to +16.5 Vdc)	$PSSI_{FS+}$	—	2.0	10	
(V_{EE} −10.8 to −16.5 Vdc)	$PSSI_{FS-}$	—	10	25	

Note 1: T_{low} = −55°C for AD563SD/AD563TD T_{high} = +125°C for AD563SD/AD563TD
0°C for AD563JD/AD563KD +70°C for AD563JD/AD563KD

FIGURE 1 — AD563 IN TYPICAL UNIPOLAR CONNECTION SCHEME


+5.0 V/+15 V
CMOS/TTL Threshold
1
3
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
11
4
2.5 V
5.0 k
10
Logic Switches & Level Shifters
Gain Adjust
5.0 k
9
6
R1 20 Ω 15T
4.99 k
Vout
2.49 k
+15 V
5
5.0 k
Rx
8
3M
R2 20 k 15T
Offset Adjust
12
−15 V
7
−15 V

UNIPOLAR DAC OPERATION

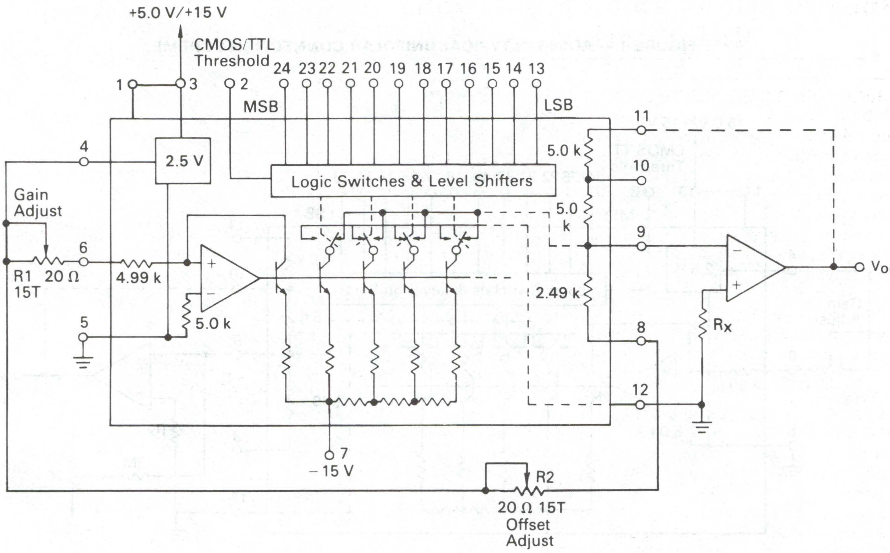
A typical circuit configuration for unipolar operation of AD563 is shown in Figure 1.

Step 1 — Output Range
Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

Step 2 — Zero Adjust
Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

Step 3 — Gain Adjust
Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — AD563 IN TYPICAL BIPOLAR CONNECTION SCHEME


+5.0 V/+15 V
CMOS/TTL Threshold
24 23 22 21 20 19 18 17 16 15 14 13
1
3
2
MSB
LSB
11
10
9
8
12
4
6
5
7
−15 V
2.5 V
Logic Switches & Level Shifters
Gain Adjust
R1 20 Ω 15T
4.99 k
5.0 k
5.0 k
5.0 k
2.49 k
Rx
Vout
R2
20 Ω 15T
Offset Adjust

BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of AD563 is shown in Figure 2.

Step 1 — Output Range

Determine which output range is required. For ±2.5 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

Step 2 — Offset Adjust

Turn all bits OFF and adjust R2 until operational amplifier output is:

-2.5000 Volt for ±2.5 Volt range
-5.0000 Volt for ±5.0 Volt range
-10.0000 Volt for ±10 Volt range

Step 3 — Gain Adjust (Bipolar Zero)

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

NOTES:

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For CMOS compatibility, short Pin 2 to Pin 1.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, R_X should be made equal to the internal feedback resistor. In bipolar, R_X, equals the feedback resistor in parallel with 2.5 k.

DAC-08

Specifications and Applications Information

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

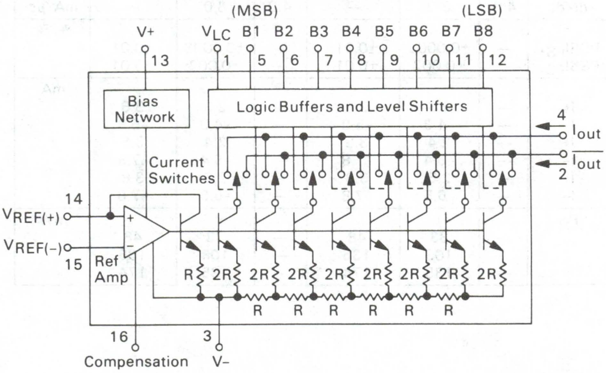
Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC}, (pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (±1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high-speed modems, and high-speed analog-to-digital converters.

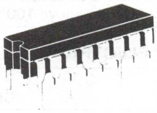
- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs −10 V to +18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost

DAC-08 EQUIVALENT CIRCUIT

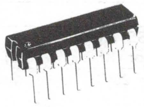

(MSB)
(LSB)
V+
V_{LC}
B1 B2 B3 B4 B5 B6 B7 B8
13
1 5 6 7 8 9 10 11 12
Bias Network
Logic Buffers and Level Shifters
Current Switches
4
I_{out}
$\overline{I_{out}}$
2
14
$V_{REF(+)}$
$V_{REF(-)}$
15
Ref Amp
R 2R 2R 2R 2R 2R 2R 2R 2R
R R R R R R
16
Compensation
3
V−

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

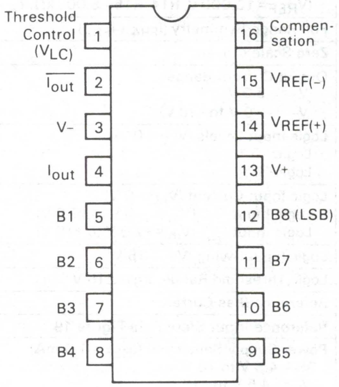


Q SUFFIX
CERAMIC PACKAGE
CASE 620-02



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

PINOUT DIAGRAM


Threshold Control (V_{LC}) 1
$\overline{I_{out}}$ 2
V− 3
I_{out} 4
B1 5
B2 6
B3 7
B4 8
16 Compensation
15 $V_{REF(-)}$
14 $V_{REF(+)}$
13 V+
12 B8 (LSB)
11 B7
10 B6
9 B5

ORDERING INFORMATION

Device	Nonlinearity	Temperature Range	Package
DAC-08AQ	±0.1%	-55°C to +125°C	Ceramic
DAC-08Q	±0.19%	-55°C to +125°C	Ceramic
DAC-08HQ	±0.1%	0°C to +70°C	Ceramic
DAC-08EQ	±0.19%	0°C to +70°C	Ceramic
DAC-08CQ	±0.39%	0°C to +70°C	Ceramic
DAC-08HP	±0.1%	0°C to +70°C	Plastic
DAC-08EP	±0.19%	0°C to +70°C	Plastic
DAC-08CP	±0.39%	0°C to +70°C	Plastic

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V+ Supply to V– Supply	—	36	V
Logic Inputs	—	V– to V– Plus 36	V
Logic Threshold Control	V_{LC}	V– to V+	V
Analog Current Outputs	I_{out}	See Figure 7	mA
Reference Inputs (V14, V15)	V_{REF}	V– to V+	V
Reference Input Differential Voltage (V14 to V15)	$V_{REF(D)}$	±18	V
Reference Input Current (I14)	I_{REF}	5.0	mA
Operating Temperature Range DAC-08AQ, Q DAC-08HQ, EQ, CQ, HP, EP, CP	T_A	 -55 to +125 0 to +70	°C
Storage Temperature	T_A	-65 to +150	°C
Power Dissipation Derate above 100°C	P_D $R_{\theta JA}$	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = -55° C to +125° C, unless otherwise noted.)

Characteristic	Symbol	DAC-08A Min	DAC-08A Typ	DAC-08A Max	DAC-08 Min	DAC-08 Typ	DAC-08 Max	Unit
Resolution	—	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	%FS
Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, T_A = 25°C)	t_s	—	85	135	—	85	150	ns
Propagation Delay, T_A = 25°C								ns
Each Bit	t_{PLH}	—	35	60	—	35	60	
All Bits Switched	t_{PHL}	—	35	60	—	35	60	
Full Scale Tempco	TCI_{FS}	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	-10	—	+18	-10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ, T_A = 25°C)	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	μA
Output Current Range								mA
V– = -5.0 V	I_{OR1}	0	—	2.1	0	—	2.1	
V– = -8.0 V to -18 V	I_{OR2}	0	—	4.2	0	—	4.2	
Logic Input Levels (V_{LC} = 0 V)								V
Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	
Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	
Logic Input Current (V_{LC} = 0 V)								μA
Logic Input "0" (V_{in} = -10 V to +0.8 V)	I_{IL}	—	-2.0	-10	—	-2.0	-10	
Logic Input "1" (V_{in} = +2.0 V to +18 V)	I_{IH}	—	0.002	10	—	0.002	10	
Logic Input Swing, V– = -15 V	V_{IS}	-10	—	+18	-10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I_{15}	—	-1.0	-3.0	—	-1.0	-3.0	μA
Reference Input Slew Rate Figure 19	di/dt	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA)								%/%
V+ = 4.5 V to 18 V	$PSSI_{FS+}$	—	±0.0003	±0.01	—	±0.0003	±0.01	
V– = -4.5 V to -18 V	$PSSI_{FS-}$	—	±0.002	±0.01	—	±0.002	±0.01	
Power Supply Current								mA
V_S = ±5.0 V, I_{REF} = 1.0 mA	I+ I–	— —	2.3 -4.3	3.8 -5.8	— —	2.3 -4.3	3.8 -5.8	
V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA	I+ I–	— —	2.4 -6.4	3.8 -7.8	— —	2.4 -6.4	3.8 -7.8	
V_S = ±15 V, I_{REF} = 2.0 mA	I+ I–	— —	2.5 -6.5	3.8 -7.8	— —	2.5 -6.5	3.8 -7.8	
Power Dissipation	P_D							mW
V_S = ±5.0 V, I_{REF} = 1.0 mA		—	33	48	—	33	48	
V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA		—	103	136	—	108	136	
V_S = ±15 V, I_{REF} = 2.0 mA		—	135	174	—	135	174	

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time to ±1/2 LSB (All Bits Switched On or Off, (T_A = 25°C) Figure 24	t_s	—	85	135	—	85	150	—	85	150	ns
Propagation Delay, T_A = 25°C											ns
Each Bit	t_{PLH}	—	35	60	—	35	60	—	35	60	
All Bits Switched	t_{PHL}	—	35	60	—	35	60	—	35	60	
Full Scale Tempco	TCI_{FS}	—	±10	±50	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	−10	—	+18	−10	—	+18	−10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ) T_A = 25°C	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range											mA
V− = −5.0 V	I_{OR1}	0	—	2.1	0	—	2.1	0	—	2.1	
V− = −8.0 V to −18 V	I_{OR2}	0	—	4.2	0	—	4.2	0	—	4.2	
Logic Input Levels (V_{LC} = 0 V)											V
Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	—	—	0.8	
Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current (V_{LC} = 0 V)											μA
Logic Input "0" (V_{in} = −10 V to +0.8 V)	I_{IL}	—	−2.0	−10	—	−2.0	−10	—	−2.0	−10	
Logic Input "1" (V_{in} = +2.0 V to +18 V)	I_{IH}	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing, V− = −15 V	V_{IS}	−10	—	+18	−10	—	+18	−10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	V
Reference Bias Current	I_{15}	—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	μA
Reference Input Slew Rate Figure 19	dI/dt	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA)											%/%
V+ = 4.5 V to 18 V	$PSSI_{FS+}$	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	
V− = −4.5 V to −18 V	$PSSI_{FS-}$	—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	
Power Supply Current	I+	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
V_S = ±5.0 V, I_{REF} = 1.0 mA	I−	—	−4.3	−5.8	—	−4.3	−25.8	—	−4.3	−5.8	
	I+	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA	I−	—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
V_S = ±15 V, I_{REF} = 2.0 mA	I−	—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_D										mW
V_S = ±5.0 V, I_{REF} = 1.0 mA		—	33	48	—	33	48	—	33	48	
V_S = +5.0 V, −15 V, I_{REF} = 2.0 mA		—	108	136	—	108	136	—	108	136	
V_S = ±15 V, I_{REF} = 2.0 mA		—	135	174	—	135	174	—	135	174	

TYPICAL PERFORMANCE CURVES

FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT

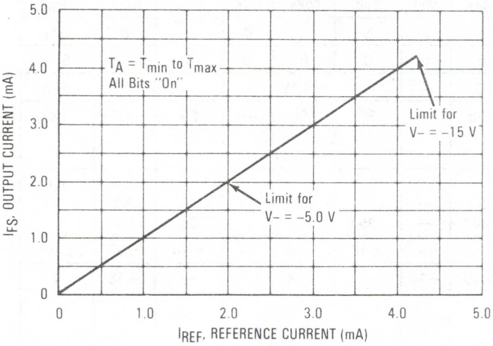
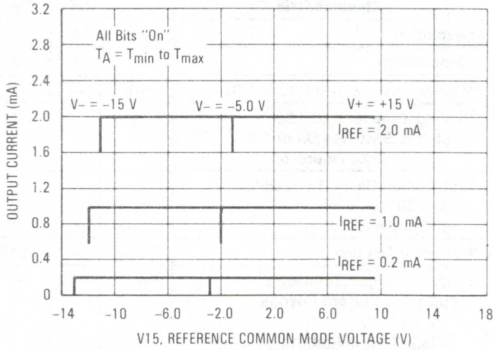
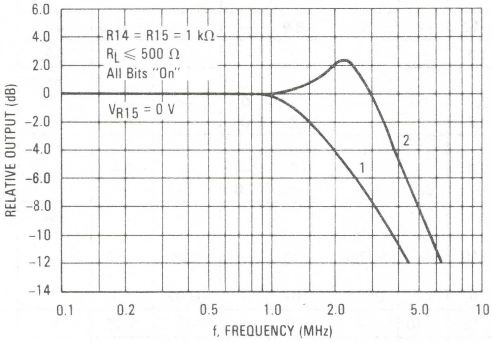


FIGURE 2 — REFERENCE AMP COMMON MODE RANGE



NOTE: Positive Common Mode Range is Always (V+) −1.5 V

FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE



Curve 1 — C_c = 15 pF, V_{in} = 2.0 V p-p Centered at +1.0 V (Large-Signal)
Curve 2 — C_c = 15 pF, V_{in} = 50 mV p-p Centered at +200 mV (Small-Signal)

FIGURE 4 — LSB PROPAGATION DELAY versus I_{FS}

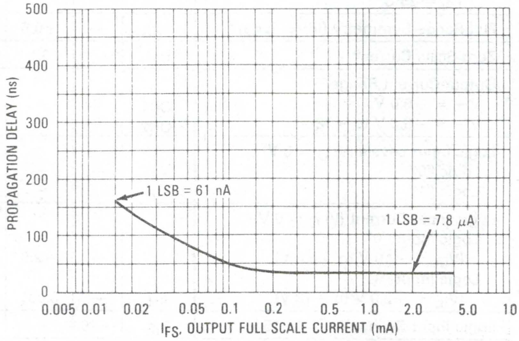


FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

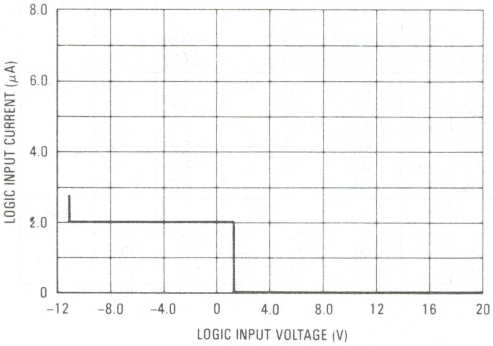
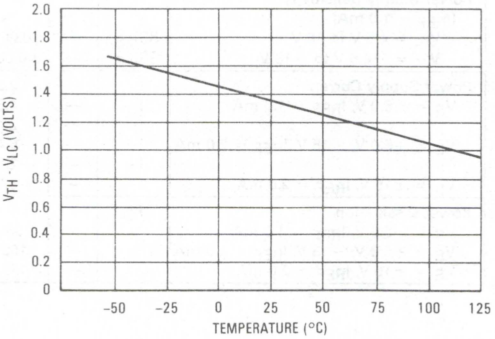


FIGURE 6 — V_{TH} - V_{LC} versus TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Voltage Compliance)

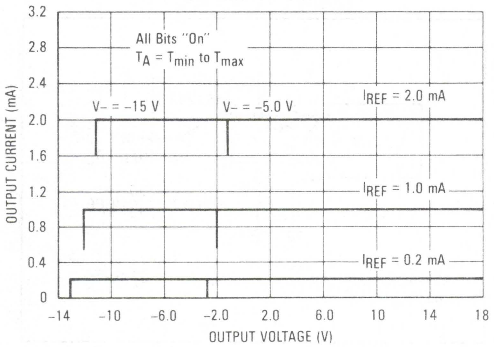


FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE

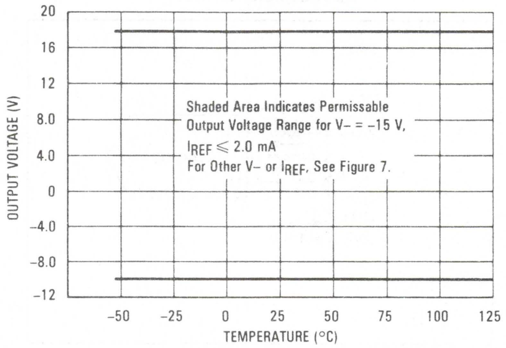
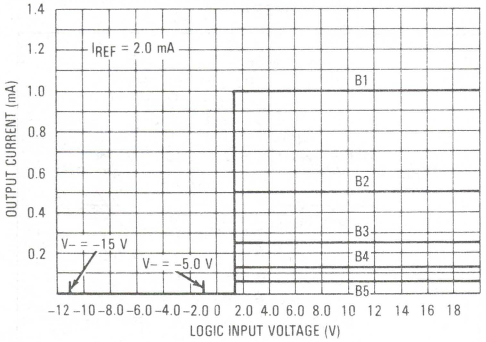


FIGURE 9 — BIT TRANSFER CHARACTERISTICS



NOTE: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range (V_{LC} = 0 V).

FIGURE 10 — POWER SUPPLY CURRENT versus V+

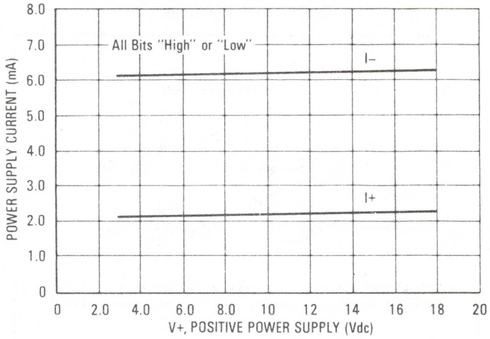


FIGURE 11 — POWER SUPPLY CURRENT versus V–

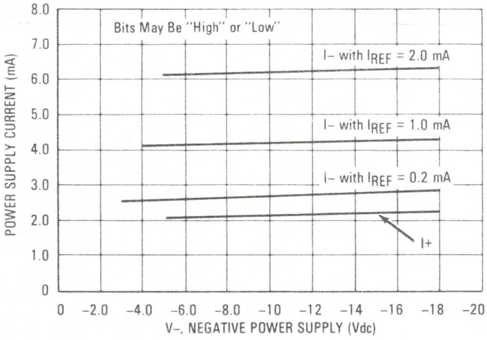
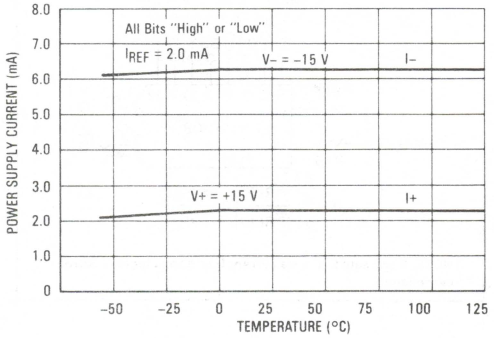


FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE



BASIC CIRCUIT CONFIGURATIONS

FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

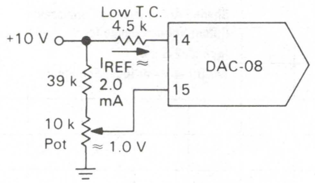
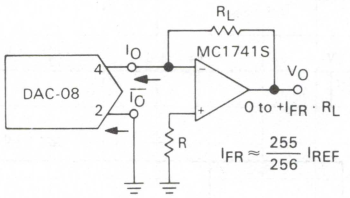

Low T.C.
4.5 k
+10 V
$I_{REF} \approx$ 2.0 mA
39 k
14
DAC-08
15
10 k Pot
≈ 1.0 V

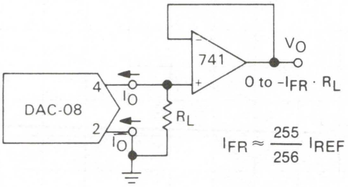
FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION


R_L
I_O
MC1741S
4
DAC-08
2
$\overline{I_O}$
V_O
0 to $+I_{FR} \cdot R_L$
R

$$I_{FR} \approx \frac{255}{256} I_{REF}$$

If complementry output (Negative Logic DAC) operation is desired, connect inverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4).

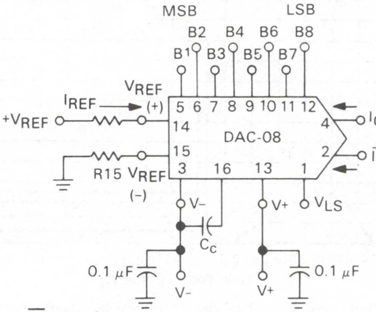
FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


741
V_O
DAC-08
4
I_O
2
$\overline{I_O}$
R_L
0 to $-I_{FR} \cdot R_L$

$$I_{FR} \approx \frac{255}{256} I_{REF}$$

If complementry output (Negative Logic DAC) is desired, connect noninverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4).

FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION

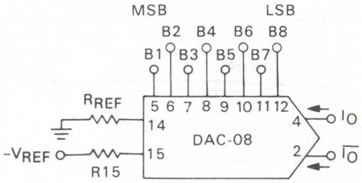

MSB
LSB
B2 B4 B6 B8
B1 B3 B5 B7
V_{REF} (+)
I_{REF}
$+V_{REF}$
5 6 7 8 9 10 11 12
14
DAC-08
15
3 16 13 1
4
2
I_O
$\overline{I_O}$
R15
V_{REF} (−)
V−
V+
V_{LS}
C_C
0.1 μF
V−
V+
0.1 μF

$I_O + \overline{I_O} = I_{FR}$ for all logic states $\quad I_{FR} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$

For fixed reference, TTL operation, typical values are

V_{REF} = +10.000 V
R_{REF} = 5.000 k
R15 ≈ R_{REF}
C_c = 0.01 μF
V_{LC} = 0 V (Ground)

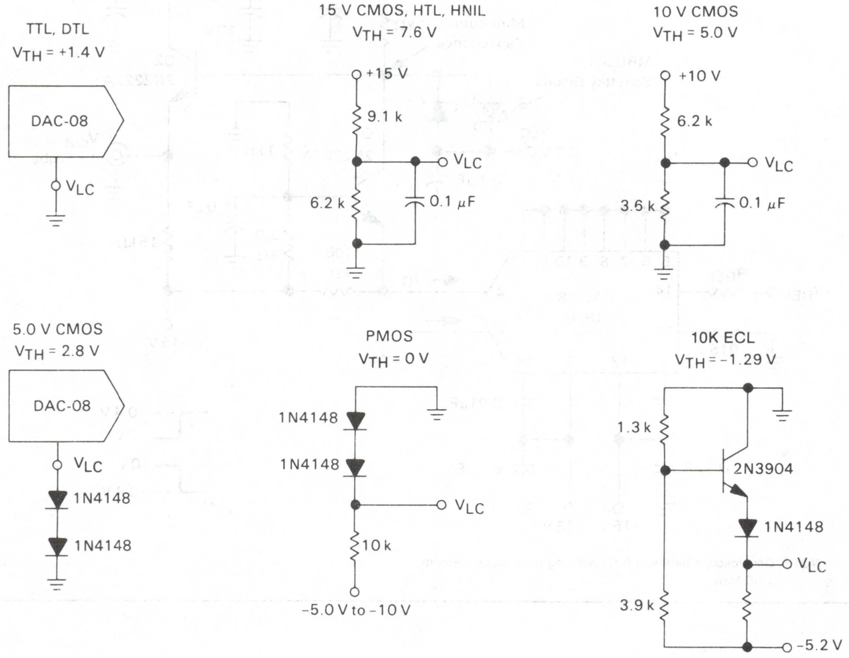
FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION


MSB
LSB
B2 B4 B6 B8
B1 B3 B5 B7
R_{REF}
5 6 7 8 9 10 11 12
14
DAC-08
$-V_{REF}$
15
R15
4
2
I_O
$\overline{I_O}$

$$I_{FR} \approx \left| \frac{-V_{REF}}{R_{REF}} \right| \times \frac{255}{256}$$

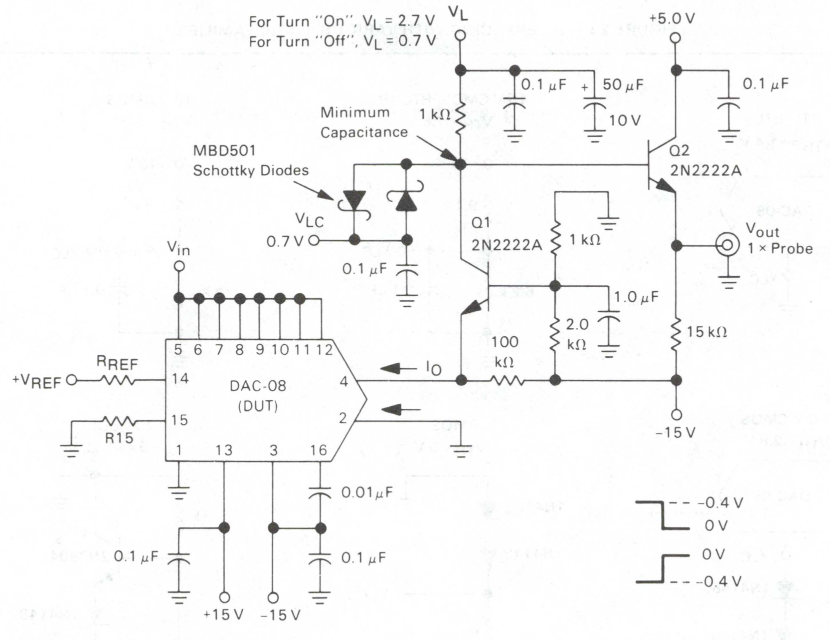
NOTE: R_{REF} sets full scale current I_{FR}; R15 is for bias current cancellation.

FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES


TTL, DTL
V_{TH} = +1.4 V
DAC-08
V_{LC}
15 V CMOS, HTL, HNIL
V_{TH} = 7.6 V
+15 V
9.1 k
V_{LC}
6.2 k
0.1 µF
10 V CMOS
V_{TH} = 5.0 V
+10 V
6.2 k
V_{LC}
3.6 k
0.1 µF
5.0 V CMOS
V_{TH} = 2.8 V
DAC-08
V_{LC}
1N4148
1N4148
PMOS
V_{TH} = 0 V
1N4148
1N4148
V_{LC}
10 k
−5.0 V to −10 V
10K ECL
V_{TH} = −1.29 V
1.3 k
2N3904
1N4148
V_{LC}
3.9 k
−5.2 V

NOTE: Do not exceed negative logic input range of DAC.
$V_{TH} = V_{LC} + 1.4$ V

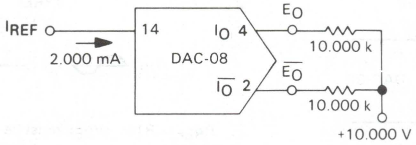
FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT


For Turn "On", VL = 2.7 V
For Turn "Off", VL = 0.7 V
VL
+5.0 V
0.1 μF
50 μF
10 V
0.1 μF
Minimum Capacitance
1 kΩ
MBD501 Schottky Diodes
Q2 2N2222A
VLC
0.7 V
0.1 μF
Q1 2N2222A
1 kΩ
Vout
1 × Probe
Vin
1.0 μF
2.0 kΩ
100 kΩ
15 kΩ
RREF
+VREF
14
DAC-08 (DUT)
5 6 7 8 9 10 11 12
4
IO
15
R15
2
1 13 3 16
−15 V
0.01 μF
0.1 μF
0.1 μF
+15 V −15 V
−0.4 V
0 V
0 V
−0.4 V

NOTE: Oscilloscope bandwidth for settling time measurement ⩾ 50 MHz

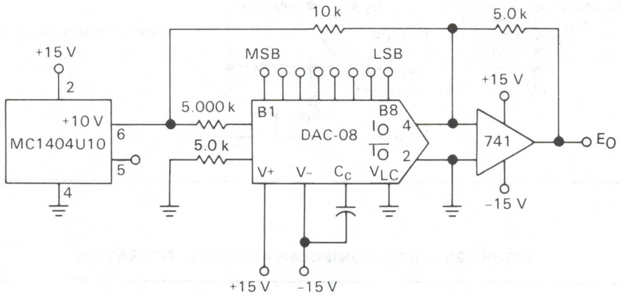
BASIC CIRCUIT CONFIGURATIONS

FIGURE 21 — BASIC BIPOLAR OUTPUT OPERATION


I_REF
2.000 mA
14
DAC-08
I_O 4
Ī_O 2
E_O
Ē_O
10.000 k
10.000 k
+10.000 V

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos Full Range	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos Full Range -LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale +LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale -LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale +LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

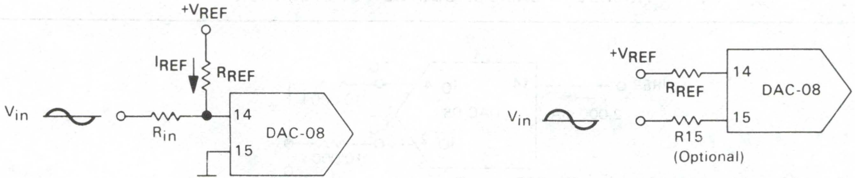
FIGURE 22 — OFFSET BINARY OPERATION


+15 V
2
+10 V
MC1404U10
6
5
4
10 k
5.0 k
MSB
LSB
5.000 k
5.0 k
B1
B8
DAC-08
I_O 4
Ī_O 2
V+
V-
C_C
V_LC
+15 V
741
-15 V
E_O
+15 V
-15 V

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Range	1	1	1	1	1	1	1	1	-4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale +1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

BASIC CIRCUIT CONFIGURATIONS

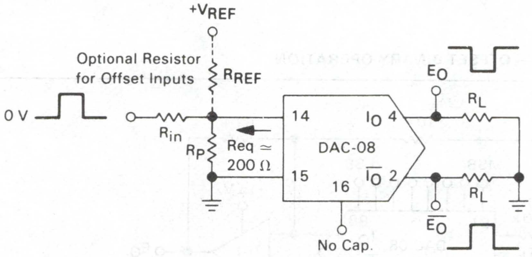
FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES


+V_{REF}
I_{REF}
R_{REF}
V_{in}
R_{in}
14
15
DAC-08
+V_{REF}
R_{REF}
14
DAC-08
V_{in}
15
R15
(Optional)

$R_{REF} \simeq$ R15 +V_{REF} must be above peak positive swing of V_{in}

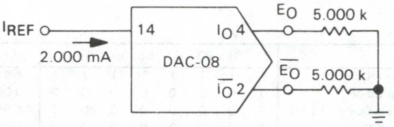
$I_{REF} \geq$ Peak Negative Swing of I_{in}

FIGURE 19 — PULSED REFERENCE OPERATION


+V_{REF}
Optional Resistor for Offset Inputs
R_{REF}
0 V
R_{in}
R_P
Req ≃ 200 Ω
14
15
16
DAC-08
I_O 4
$\overline{I_O}$ 2
No Cap.
E_O
R_L
R_L
$\overline{E_O}$

Typical Values: R_{in} 5.0 k, +V_{in} = 10 V

FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION


I_{REF}
2.000 mA
14
DAC-08
I_O 4
$\overline{I_O}$ 2
E_O 5.000 k
$\overline{E_O}$ 5.000 k

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Range	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

MOTOROLA

MC1406L
MC1506L

Specifications and Applications Information

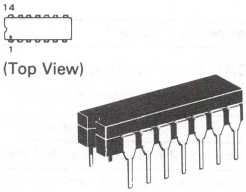
SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy – ±0.78% Error maximum
- Low Power Dissipation – 85 mW typical @ ±5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time – 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V

SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632-02
MO-001AA

FIGURE 1 – OUTPUT CURRENT SETTLING TIME (ALL BITS SWITCHED, $R_L = 50\ \Omega$)

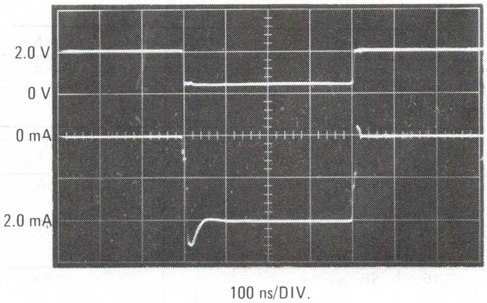
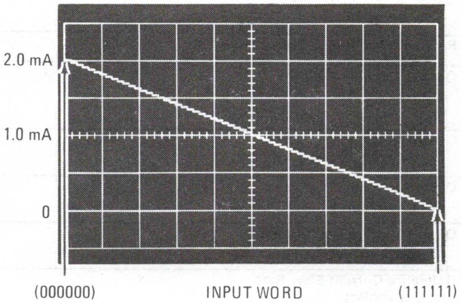


FIGURE 2 – D-to-A TRANSFER CHARACTERISTICS



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Digital-to-Analog Meter Readout
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Digital Varicap Tuning
- Video Systems
- Stepping Motor Drive
- CRT Character Generation
- Digital Addition and Subtraction
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Programmable Power Supplies
- Speech Encoding

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 −16.5	Vdc
Digital Input Voltage	V_5 thru V_{10}	+8.0, V_{EE}	Vdc
Applied Output Voltage	V_O	±5.0	Vdc
Reference Current	I_{12}	5.0	mA
Reference Amplifier Inputs	V_{12}, V_{13}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		1000	mW
Derate above T_A = +25°C		6.7	mW/°C
Operating Temperature Range	T_A		°C
MC1506L		−55 to +125	
MC1406L		0 to +70	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R12}$ = 2.0 mA, all logic inputs in low logic state, T_A = T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	10	E_r	–	–	±0.78	%
Settling Time (within 1/2 LSB [includes t_d] T_A = +25°C)	9	t_S	–	150	–	ns
Propagation Delay Time T_A = +25°C	9	t_{PHL}, t_{PLH}	–	10	50	ns
Output Full Scale Current Drift		$\lvert TCI_O \rvert$	–	80	–	PPM/°C
Digital Input Logic Levels	3,14					Vdc
High Level, Logic "1"		V_{IH}	2.4	–	–	
Low Level, Logic "0"		V_{IL}	–	–	0.8	
Digital Input Current	3,13					mA
High Level, V_{IH} = 5.0 V		I_{IH}	–	0	+0.01	
Low Level, V_{IL} = 0.8 V		I_{IL}	–	−0.7	−1.5	
Reference Input Bias Current (Pin 13)	3	I_{13}	–	−0.002	−0.01	mA
Output Current Range	3	I_{OR}				mA
V_{EE} = −5.0 V			0	2.0	2.1	
V_{EE} = −15 V, T_A = +25°C			0	2.0	4.2	
Output Current V_{ref} = 2.000 V, R_{12} = 1.000 kΩ	3	I_O	1.9	1.97	2.1	mA
Output Current (all bits high)	3	I_O(min)	–	0	10	μA
Output Voltage Compliance ($E_r \leqslant$ ±0.78% at T_A = +25°C)	3,4,5	V_{O+} V_{O-}	– –	+0.25 −0.45	+0.1 −0.3	Vdc
Reference Current Slew Rate (T_A = +25°C)	8,15	SR I_{ref}	–	2.0	–	mA/μs
Output Current Power Supply Sensitivity	10	PSRR (−)	–	0.002	0.010	mA/V
Power Supply Current	3,11,12					mA
A1 thru A6; V_{IL} = 0.8 V		I_{CC}	–	+7.2	+11	
A1 thru A6; V_{IH} = 2.4 V		I_{EE}	–	−9.0	−11	
Power Dissipation (all bits high)		P_D				mW
V_{EE} = −5.0 Vdc			–	85	120	
V_{EE} = −15 Vdc			–	175	240	

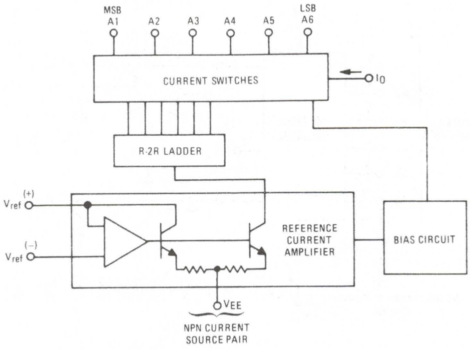
*T_{high} = +70°C for MC1406L T_{low} = 0°C for MC1406L
= +125°C for MC1506L   = −55°C for MC1506L

The MC1506L consists of a reference current amplifier, an R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

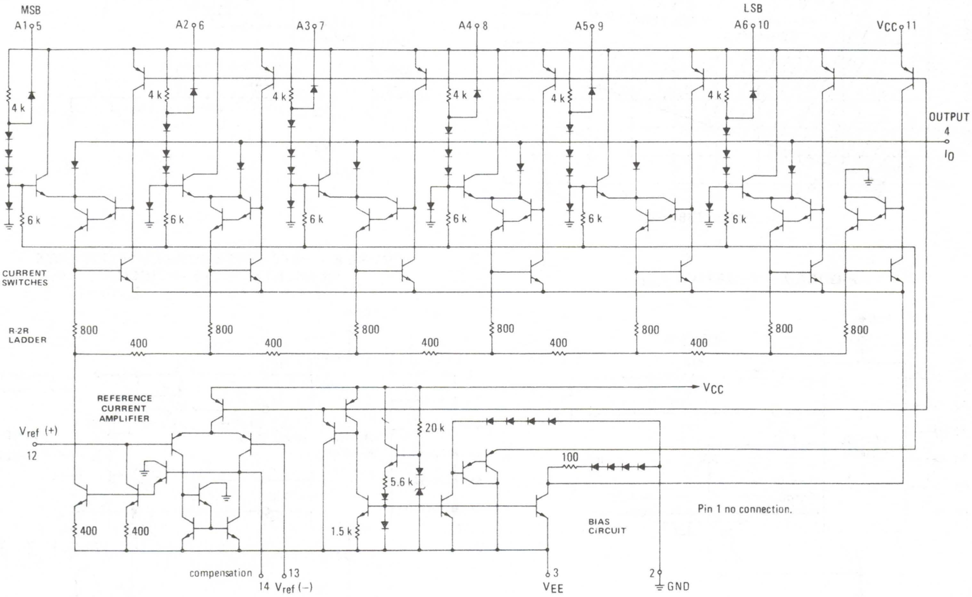
The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

BLOCK DIAGRAM


MSB
A1
A2
A3
A4
A5
LSB
A6
CURRENT SWITCHES
I0
R-2R LADDER
(+)
Vref
(–)
Vref
REFERENCE
CURRENT
AMPLIFIER
BIAS CIRCUIT
VEE
NPN CURRENT
SOURCE PAIR

COMPLETE CIRCUIT SCHEMATIC
(Digital Inputs; pins 5,6,7,8,9,10)


MSB
A1 5
A2 6
A3 7
A4 8
A5 9
LSB
A6 10
VCC 11
4 k
6 k
OUTPUT
4
I0
CURRENT
SWITCHES
R-2R
LADDER
800
400
VCC
REFERENCE
CURRENT
AMPLIFIER
Vref (+)
12
20 k
100
5.6 k
1.5 k
400
BIAS
CIRCUIT
Pin 1 no connection.
compensation
14
13
Vref (–)
3
VEE
2
GND

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT

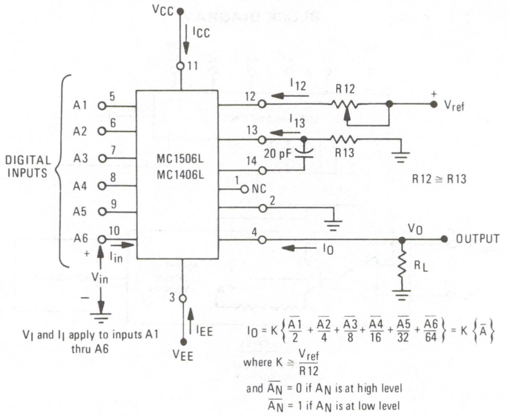

VCC
ICC
11
A1
A2
A3
A4
A5
A6
5
6
7
8
9
10
DIGITAL INPUTS
MC1506L
MC1406L
12
I12
R12
+
Vref
13
I13
14
20 pF
R13
R12 ≅ R13
1
NC
2
4
VO
OUTPUT
IO
RL
+
Iin
Vin
−
3
IEE
VEE
VI and II apply to inputs A1 thru A6
IO = K{A̅1/2 + A̅2/4 + A̅3/8 + A̅4/16 + A̅5/32 + A̅6/64} = K{A̅}
where K ≅ Vref/R12
and A̅N = 0 if AN is at high level
A̅N = 1 if AN is at low level

FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

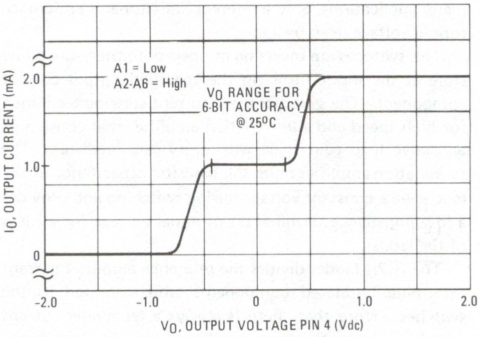


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

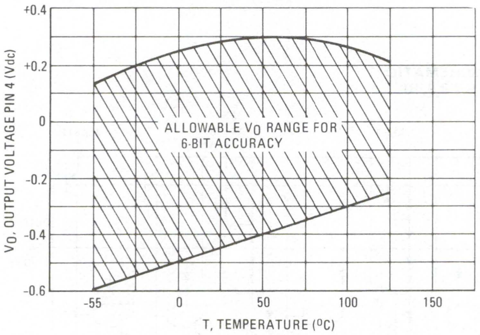


FIGURE 6 – POSITIVE V_{ref}

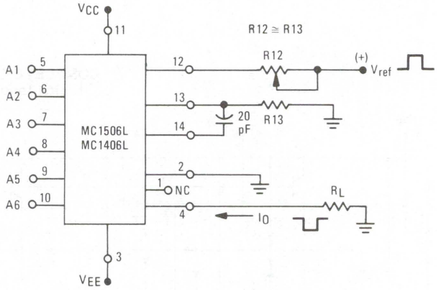

VCC
11
R12 ≅ R13
A1
A2
A3
A4
A5
A6
5
6
7
8
9
10
MC1506L
MC1406L
12
R12
(+)
Vref
13
20 pF
R13
14
2
1
NC
RL
4
IO
3
VEE

FIGURE 7 – NEGATIVE V_{ref}

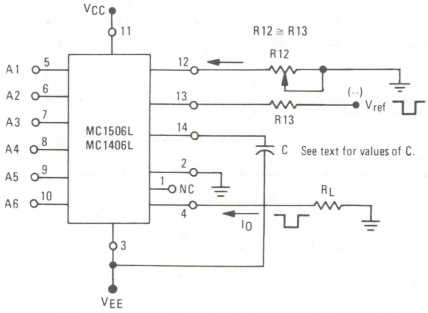
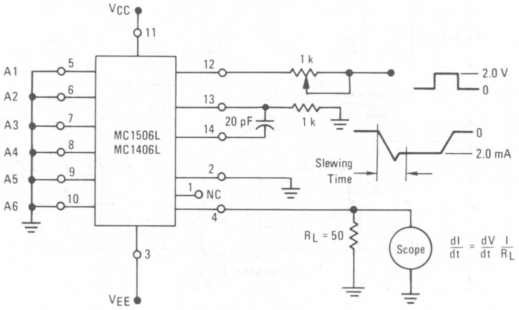

VCC
11
R12 ≅ R13
A1
A2
A3
A4
A5
A6
5
6
7
8
9
10
MC1506L
MC1406L
12
R12
13
(−)
Vref
R13
14
C
See text for values of C.
2
1
NC
RL
4
IO
3
VEE

FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT


VCC
11
A1
A2
A3
A4
A5
A6
5
6
7
8
9
10
MC1506L
MC1406L
12
1 k
2.0 V
0
13
20 pF
1 k
14
0
2.0 mA
Slewing Time
2
1
NC
4
RL = 50
Scope
dI/dt = dV/dt · 1/RL
3
VEE

TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – TRANSIENT RESPONSE

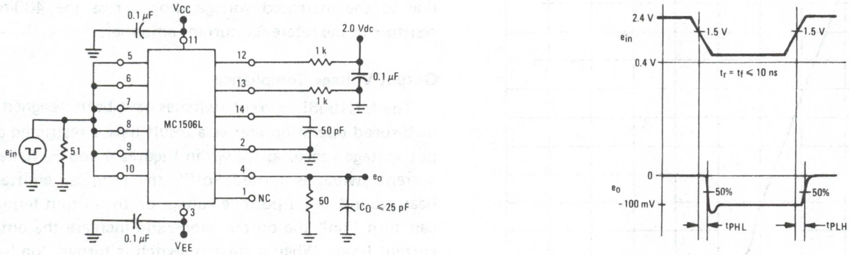

0.1 μF
VCC
11
2.0 Vdc
5
12
1 k
6
13
0.1 μF
7
1 k
14
8
MC1506L
50 pF
9
2
ein
51
10
4
eo
1
NC
50
CO ≤ 25 pF
3
0.1 μF
VEE
2.4 V
1.5 V
1.5 V
ein
0.4 V
tr = tf ≤ 10 ns
0
eo
50%
50%
-100 mV
tPHL
tPLH

FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT

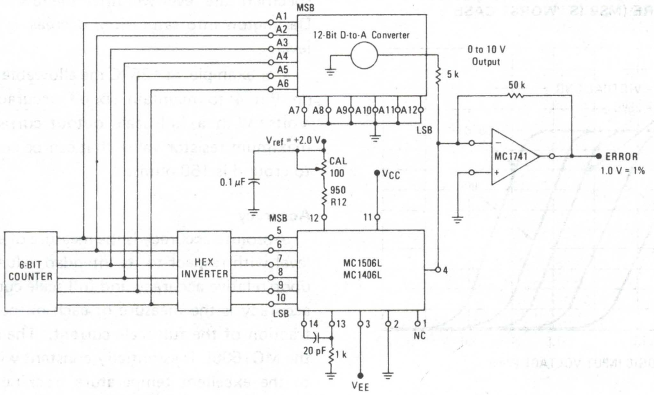

MSB
A1
A2
A3
A4
A5
A6
12-Bit D-to-A Converter
0 to 10 V
Output
5 k
50 k
A7
A8
A9
A10
A11
A12
LSB
Vref = +2.0 V
CAL
100
950
R12
0.1 μF
VCC
MC1741
ERROR
1.0 V = 1%
MSB
12
11
5
6
6-BIT
COUNTER
HEX
INVERTER
7
8
9
10
LSB
MC1506L
MC1406L
4
14
13
3
2
1
NC
20 pF
1 k
VEE

FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

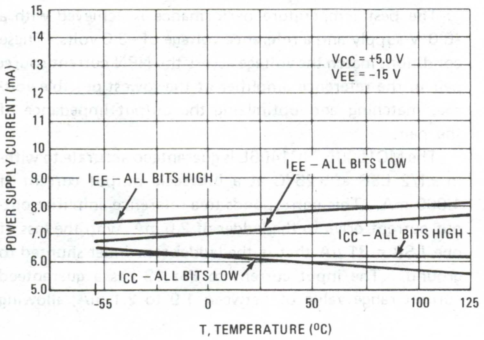
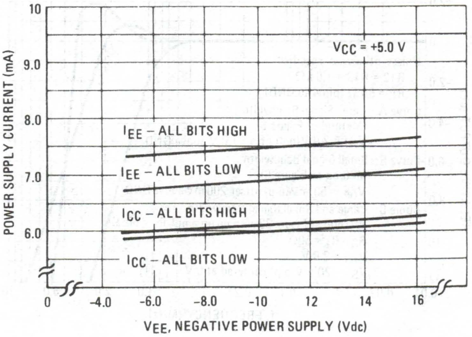


FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus VEE



TYPICAL CHARACTERISTICS (continued)

FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

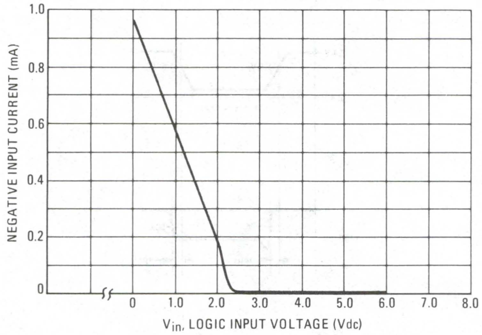


FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")

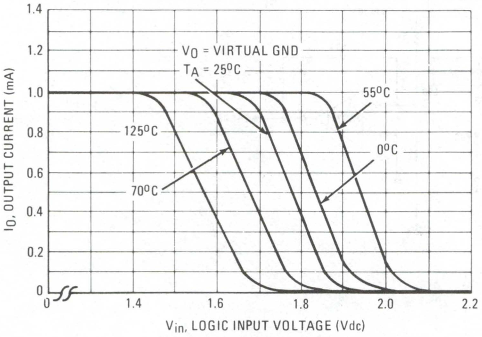
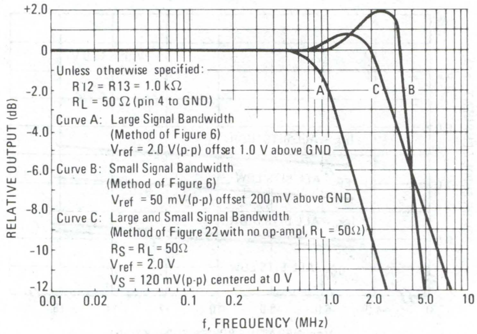


FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE



GENERAL INFORMATION

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

Output Voltage Compliance

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on Pin 4 to maintain six-bit accuracy is +0.1 to -0.3 Volts. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from Pin 4 to ground is 150 ohms.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to Pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

GENERAL INFORMATION (continued)

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of ±1/2 of one part in 4096, or ±0.012%, which is more accurate than the ±0.78% specification provided by the MC1506L.

Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of 6.0 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 60 μA to 4.0 mA, the 6.0 μA contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within ±1/2 LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at Pin 12 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into Pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from Pin 14 to Pin 13. This compensation method yields the best slew rate, typically better than 2.0 mA/μs, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at Pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to V_{EE}. The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

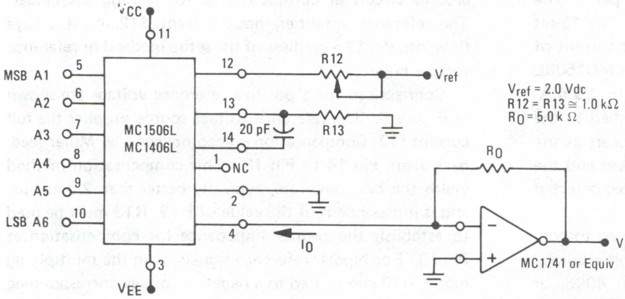
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to V_{EE} on Pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above V_{EE}. Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at Pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 12 and ground.

If Pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION


VCC
11
MSB A1
5
A2
6
A3
7
A4
8
A5
9
LSB A6
10
MC1506L
MC1406L
12
13
14
1
NC
2
4
3
VEE
20 pF
R12
R13
Vref
RO
IO
VO
MC1741 or Equiv

V_{ref} = 2.0 Vdc
$R12 = R13 \cong 1.0\ k\Omega$
$R_O = 5.0\ k\ \Omega$

Theoretical V_O

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) = K\ R_O\left\{\bar{A}\right\}$$

Adjust R_{ref} so that V_O with all digital inputs at low level is equal to 9.844 volts.

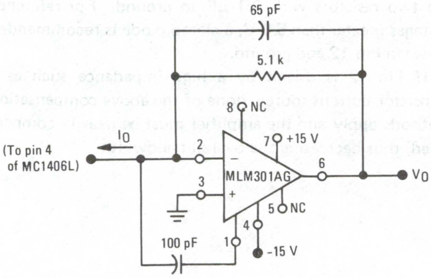
$$V_O = \frac{2\ V}{1\ K}(5\ K)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64}\right) = 10\ V\left(\frac{63}{64}\right) = 9.844\ V$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

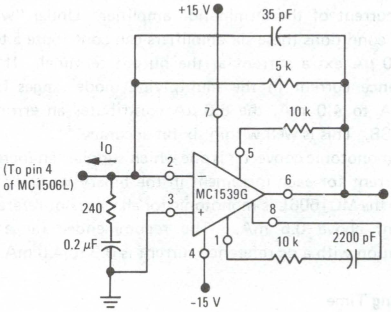
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17

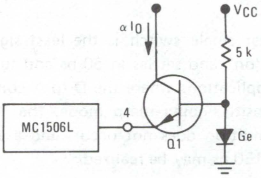

65 pF
5.1 k
8
NC
(To pin 4 of MC1406L)
IO
2
3
7
+15 V
6
VO
MLM301AG
5
NC
4
1
-15 V
100 pF

An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18


+15 V
35 pF
5 k
7
10 k
5
IO
(To pin 4 of MC1506L)
2
3
6
MC1539G
VO
240
8
0.2 µF
1
10 k
2200 pF
4
-15 V

The positive voltage range may be extended by cascoding the output with a high beta common base transistor, Q1, as shown.


VCC
α IO
5 k
MC1506L
4
Q1
Ge

The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

APPLICATIONS INFORMATION (continued)

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

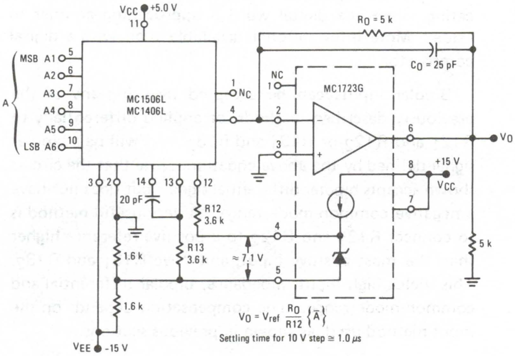
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ±0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ±0.25 volt.

FIGURE 19 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



VCC +5.0 V
11
MSB A1 5
A2 6
A3 7
A4 8
A5 9
LSB A6 10
A
MC1506L
MC1406L
1 NC
4
RO = 5 k
CO = 25 pF
NC
1
MC1723G
2
3
6
VO
8
+15 V
VCC
7
4
5
3 2 14 13 12
20 pF
R12 3.6 k
R13 3.6 k
≈ 7.1 V
1.6 k
1.6 k
5 k
VEE -15 V

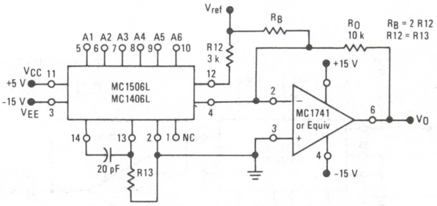
$$V_O = V_{ref}\,\frac{R_O}{R12}\left\{\bar{A}\right\}$$

Settling time for 10 V step ≅ 1.0 µs

Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

FIGURE 20 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



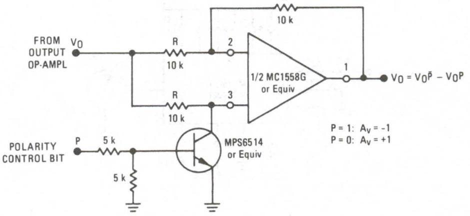
Vref
RB
RO 10 k
RB = 2 R12
R12 = R13
A1 A2 A3 A4 A5 A6
5 6 7 8 9 10
R12 3 k
VCC 11
+5 V
-15 V
VEE 3
MC1506L
MC1406L
12
4
2
3
+15 V
MC1741 or Equiv
6
VO
4
-15 V
14 13 2 1 NC
20 pF
R13

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) - \frac{V_{ref}}{R_B}(R_O)$$

Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 – POLARITY SWITCHING CIRCUIT
(6-Bit Magnitude Plus Sign D-to-A Converter)



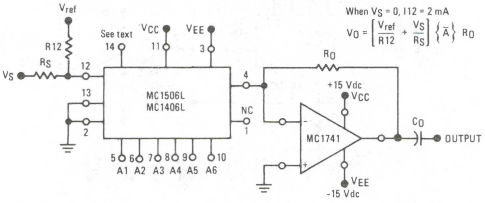
R
10 k
FROM OUTPUT OP-AMPL VO
R
10 k
2
R
10 k
3
1/2 MC1558G or Equiv
1
VO = VOP̄ – VOP
P = 1: Av = -1
P = 0: Av = +1
POLARITY CONTROL BIT P
5 k
5 k
MPS6514 or Equiv

APPLICATIONS INFORMATION (continued)

Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

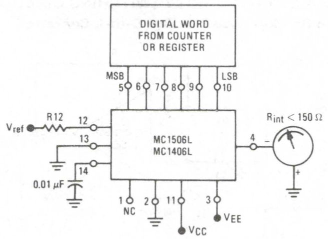
FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT


Vref
R12
RS
VS
See text
14
VCC
11
VEE
3
12
13
2
MC1506L
MC1406L
4
NC
1
5 6 7 8 9 10
A1 A2 A3 A4 A5 A6
When VS = 0, I12 = 2 mA
$V_O = \left[\frac{V_{ref}}{R12} + \frac{V_S}{R_S}\right]\left\{\bar{A}\right\} R_O$
RO
+15 Vdc
VCC
MC1741
VEE
-15 Vdc
CO
OUTPUT

Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or V_{ref}.

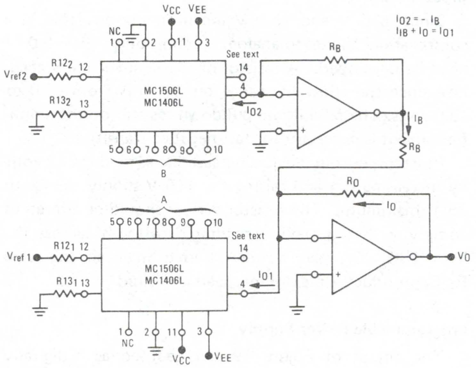
FIGURE 23 – PANEL METER READOUT CIRCUIT


DIGITAL WORD
FROM COUNTER
OR REGISTER
MSB
LSB
5 6 7 8 9 10
Vref
R12
12
13
14
0.01 µF
MC1506L
MC1406L
1
NC
2
11
3
VEE
VCC
4
Rint < 150 Ω

The best frequency response is obtained by not allowing I_{12} to reach zero. R_S can be set for a ±1.0 mA variation in relation to I_{12}. I_{12} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION


VCC VEE
NC
1 2 11 3
See text
14
4
Vref2
R12$_2$ 12
R13$_2$ 13
MC1506L
MC1406L
IO2
5 6 7 8 9 10
B
A
RB
IB
RB
IO2 = - IB
IB + IO = IO1
RO
IO
Vref 1
R12$_1$ 12
R13$_1$ 13
See text
14
4
IO1
MC1506L
MC1406L
1 2 11 3
NC
VCC
VEE
VO

$$I_O = I_{O1} - I_{O2} = \frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\} - \frac{V_{ref2}}{R12_2}\left\{\bar{B}\right\}$$

Digital Subtraction:

$$\text{let } \frac{V_{ref1}}{R12_1} = \frac{V_{ref2}}{R12_2}$$

$$V_O = \frac{V_{ref1}}{R12_1} R_O \left[\left\{\bar{A}\right\} - \left\{\bar{B}\right\}\right]$$

Programmable Amplifier:

Connect digital inputs so A = B

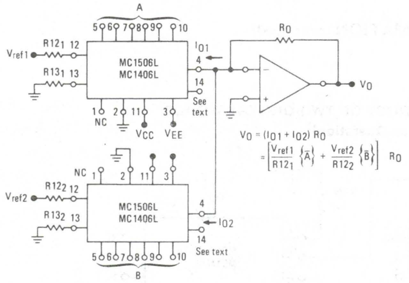
$$V_O = \left\{\bar{A}\right\}\left[\frac{V_{ref1}}{R12_1} - \frac{V_{ref2}}{R12_2}\right]$$

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R12_1$ and $R12_2$ or $R13_1$ and $R13_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R12_1$ and $R12_2$ to a positive reference higher than the most positive input, and drive $R13_1$ and $R13_2$. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

APPLICATIONS INFORMATION (continued)

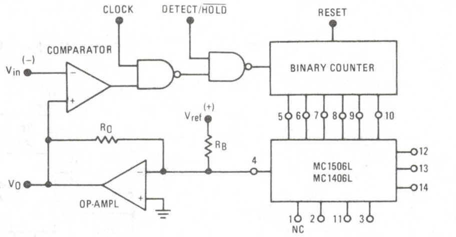
FIGURE 25 – DIGITAL SUMMING and CHARACTER GENERATION


A
5 6 7 8 9 10
Vref1
R12₁ 12
R13₁ 13
MC1506L
MC1406L
IO1
4
14
See text
1 2 11 3
NC
VCC VEE
RO
VO
NC 1 2 11 3
Vref2
R12₂ 12
R13₂ 13
MC1506L
MC1406L
4
IO2
14
See text
5 6 7 8 9 10
B

$$V_O = (I_{O1} + I_{O2})\,R_O = \left[\frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\} + \frac{V_{ref2}}{R12_2}\left\{\bar{B}\right\}\right] R_O$$

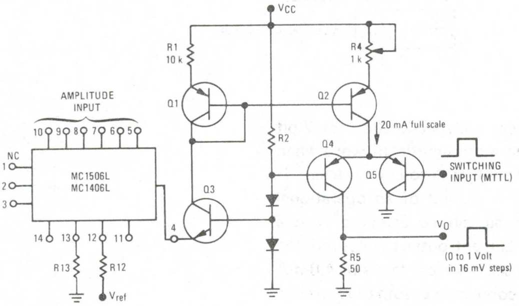
In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

FIGURE 26 – PEAK DETECTING SAMPLE and HOLD
(Features infinite hold time and optional digital output.)


CLOCK
DETECT/HOLD
RESET
COMPARATOR
(–)
Vin
+
BINARY COUNTER
Vref (+)
RB
RO
5 6 7 8 9 10
4
MC1506L
MC1406L
12
13
14
VO
OP-AMPL
1 2 11 3
NC

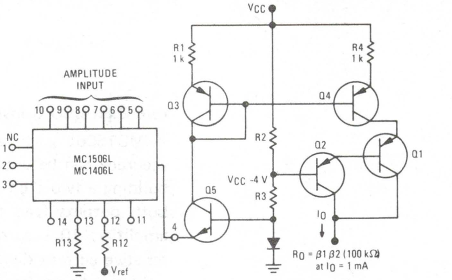
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

FIGURE 27 – PROGRAMMABLE PULSE GENERATOR


VCC
R1
10 k
R4
1 k
AMPLITUDE
INPUT
Q1
Q2
20 mA full scale
10 9 8 7 6 5
NC
1
2
3
MC1506L
MC1406L
R2
Q4
Q5
SWITCHING
INPUT (MTTL)
Q3
4
14 13 12 11
R13
R12
Vref
VO
R5
50
(0 to 1 Volt
in 16 mV steps)

Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

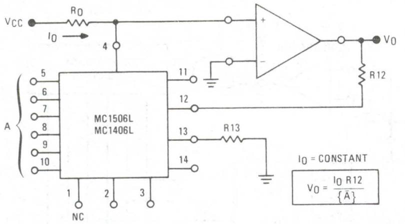
FIGURE 28 – PROGRAMMABLE CONSTANT CURRENT SOURCE


VCC
R1
1 k
R4
1 k
AMPLITUDE
INPUT
10 9 8 7 6 5
Q3
Q4
NC
1
2
3
MC1506L
MC1406L
R2
Q2
Q1
VCC -4 V
R3
Q5
4
14 13 12 11
R13
R12
Vref
IO

$R_O = \beta1\,\beta2$ (100 kΩ) at $I_O = 1$ mA

Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

FIGURE 29 – ANALOG DIVISION BY DIGITAL WORD


VCC
RO
IO
4
VO
5
6
7
8
9
10
A
MC1506L
MC1406L
11
12
R12
13
R13
14
1 2 3
NC

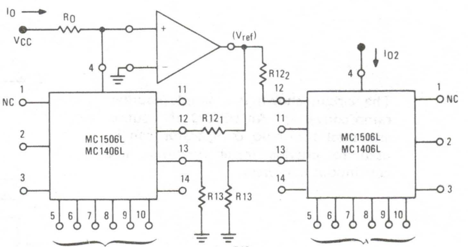
I_O = CONSTANT

$$\boxed{V_O = \frac{I_O\,R12}{\{\bar{A}\}}}$$

This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 62 μA so that I_{12} will have a maximum value of 3.938 mA for a digital bit input configuration of 111110.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 30 – ANALOG QUOTIENT OF TWO DIGITAL WORDS


IO
RO
VCC
(Vref)
IO2
4
R12₂
12
1
NC
2
3
MC1506L
MC1406L
11
12
R12₁
13
14
R13
R13
5 6 7 8 9 10
A
B
NC

$$V_{ref} = \frac{I_{O1}\,R12_1}{\{\bar{A}\}}$$

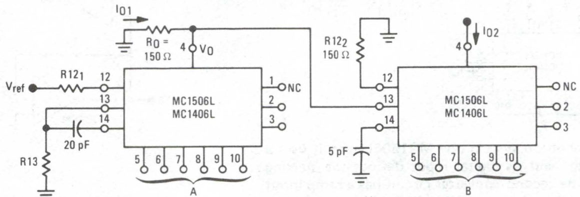
$$I_{O2} = \frac{V_{ref}}{R12_2}\{\bar{B}\}$$

if $R12_1 = R12_2$

$$\boxed{I_{O2} = I_{O1}\frac{\{\bar{B}\}}{\{\bar{A}\}}}$$

APPLICATIONS INFORMATION (continued)

FIGURE 31 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)


I01
R0 = 150 Ω
4
V0
Vref
R12₁
12
13
14
20 pF
R13
MC1506L
MC1406L
1
NC
2
3
5 6 7 8 9 10
A
R12₂
150 Ω
I02
4
12
13
14
5 pF
MC1506L
MC1406L
NC
2
3
5 6 7 8 9 10
B

$$V_O = I_{O1}R_O = \frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\}R_O$$

$$I_{O2} = -\frac{\left\{\bar{B}\right\}|V_O|}{R12_2}$$

$$= \frac{\left\{\bar{B}\right\}}{R12_2}\left[R_O\left(\frac{V_{ref1}}{R12_1}\right)\left\{\bar{A}\right\}\right]$$

since $R_O = R12_2$ and $K = V_{ref}/R12_1$

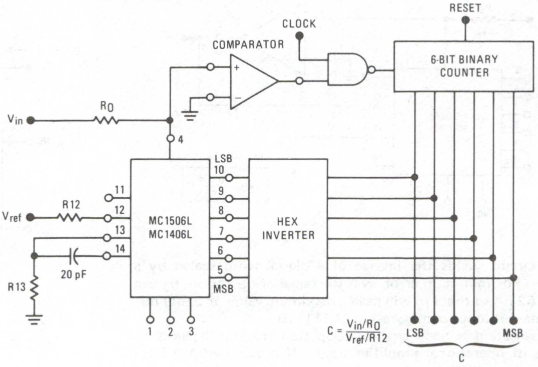
$$\boxed{I_{O2} = K\left\{\bar{A}\right\}\left\{\bar{B}\right\}}$$

K can be an analog variable.

Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

FIGURE 32 – DIGITAL QUOTIENT of TWO ANALOG VARIABLES
or ANALOG-TO-DIGITAL CONVERSION


RESET
CLOCK
COMPARATOR
+
–
6-BIT BINARY COUNTER
Vin
R0
4
LSB
10
9
8
7
6
5
MSB
11
12
13
14
Vref
R12
20 pF
R13
MC1506L
MC1406L
HEX INVERTER
1 2 3
C = Vin/R0 / Vref/R12
LSB
MSB
C

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA

MC1408
MC1508

Specifications and Applications Information

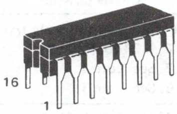
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

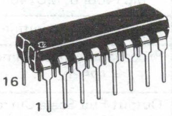
- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620-02



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

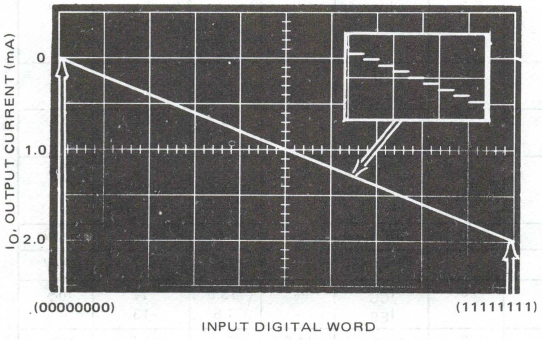
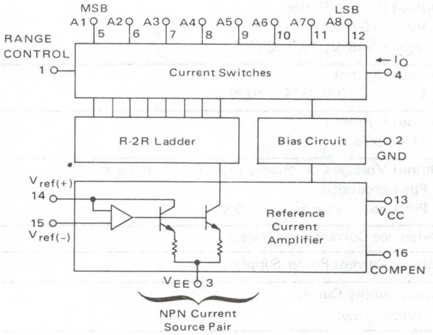


FIGURE 2 – BLOCK DIAGRAM



MSB
LSB
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
RANGE CONTROL
1
Current Switches
I_O
4
R-2R Ladder
Bias Circuit
2
GND
$V_{ref(+)}$
14
15
$V_{ref(-)}$
Reference Current Amplifier
13
V_{CC}
16
COMPEN
V_{EE} 3
NPN Current Source Pair

TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Operating Temperature Range	T_A		°C
MC1508		-55 to +125	
MC1408 Series		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

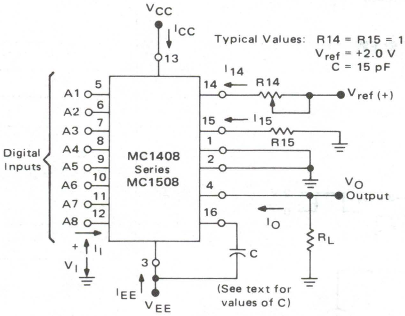
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	4	E_r				%
MC1508L8, MC1408L8, MC1408P8			–	–	±0.19	
MC1408P7, MC1408L7, See Note 1			–	–	±0.39	
MC1408P6, MC1408L6, See Note 1			–	–	±0.78	
Settling Time to within ±1/2 LSB [includes t_{PLH}](T_A=+25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH}, t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	-20		PPM/°C
Digital Input Logic Levels (MSB)	3					Vdc
High Level, Logic "1"		V_{IH}	2.0	–	–	
Low Level, Logic "0"		V_{IL}	–	–	0.8	
Digital Input Current (MSB)	3					mA
High Level, V_{IH} = 5.0 V		I_{IH}	–	0	0.04	
Low Level, V_{IL} = 0.8 V		I_{IL}	–	-0.4	-0.8	
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	µA
Output Current Range	3	I_{OR}				mA
V_{EE} = -5.0 V			0	2.0	2.1	
V_{EE} = -15 V, T_A = 25°C			0	2.0	4.2	
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	1.9	1.99	2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	µA
Output Voltage Compliance ($E_r \leq$ 0.19% at T_A = +25°C)	3	V_O				Vdc
Pin 1 grounded			–	–	-0.55, +0.4	
Pin 1 open, V_{EE} below -10 V			–	–	-5.0, +0.4	
Reference Current Slew Rate	6	$SR\ I_{ref}$	–	4.0	–	mA/µs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	µA/V
Power Supply Current (All bits low)	3	I_{CC}	–	+13.5	+22	mA
		I_{EE}	–	-7.5	-13	
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR}	+4.5	+5.0	+5.5	Vdc
		V_{EER}	-4.5	-15	-16.5	
Power Dissipation	3	P_D				mW
All bits low						
V_{EE} = -5.0 Vdc			–	105	170	
V_{EE} = -15 Vdc			–	190	305	
All bits high						
V_{EE} = -5.0 Vdc			–	90	–	
V_{EE} = -15 Vdc			–	160	–	

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_{CC}
I_{CC}
13
Typical Values: R14 = R15 = 1 k
V_{ref} = +2.0 V
C = 15 pF
I_{14}
14
R14
V_{ref} (+)
15
I_{15}
R15
1
2
4
16
V_O Output
I_O
R_L
C
(See text for values of C)
Digital Inputs
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1408 Series MC1508
I_I
V_I
3
I_{EE}
V_{EE}

V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

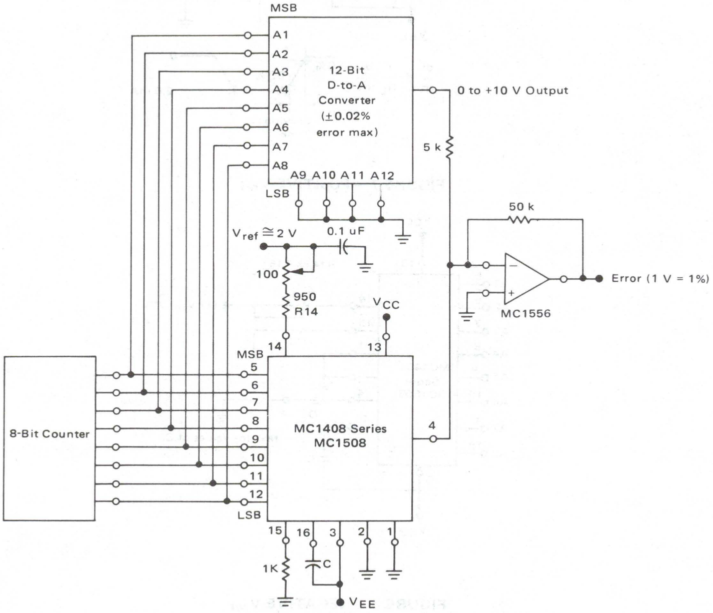
$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level

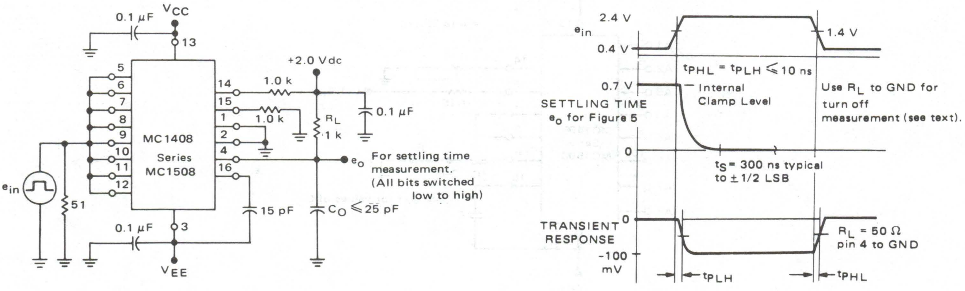
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT



MSB
A1
A2
A3
A4
A5
A6
A7
A8
12-Bit D-to-A Converter (±0.02% error max)
A9 A10 A11 A12
LSB
0 to +10 V Output
5 k
50 k
V_{ref} ≅ 2 V
0.1 uF
100
950
R14
Error (1 V = 1%)
MC1556
V_{CC}
14
13
MSB
5
6
7
8
9
10
11
12
LSB
8-Bit Counter
MC1408 Series MC1508
4
15
16
3
2
1
1K
C
V_{EE}

FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



0.1 µF
V_{CC}
13
5
6
7
8
9
10
11
12
MC1408 Series MC1508
14
15
1
2
4
16
+2.0 Vdc
1.0 k
1.0 k
R_L 1 k
0.1 µF
e_o
For settling time measurement. (All bits switched low to high)
15 pF
C_O ≤ 25 pF
e_{in}
51
0.1 µF
3
V_{EE}
e_{in}
2.4 V
0.4 V
1.4 V
t_{PHL} = t_{PLH} ≤ 10 ns
0.7 V
Internal Clamp Level
SETTLING TIME
e_o for Figure 5
0
Use R_L to GND for turn off measurement (see text).
t_S = 300 ns typical to ± 1/2 LSB
TRANSIENT RESPONSE
0
-100 mV
R_L = 50 Ω pin 4 to GND
t_{PLH}
t_{PHL}

TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

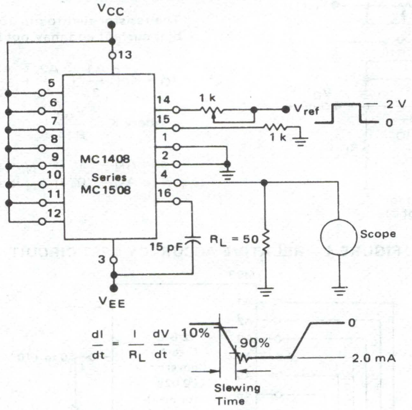

VCC
13
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
1 k
Vref
2 V
0
1 k
15 pF
RL = 50
Scope
3
VEE
dI/dt = 1/RL dV/dt
10%
90%
0
2.0 mA
Slewing Time

FIGURE 7 – POSITIVE V_{ref}

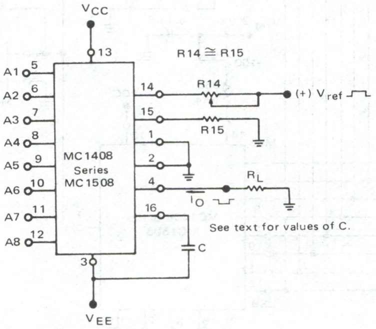

VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
R14
R15
(+) Vref
RL
IO
See text for values of C.
C
3
VEE

FIGURE 8 – NEGATIVE V_{ref}

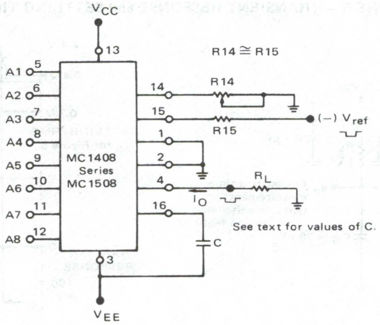
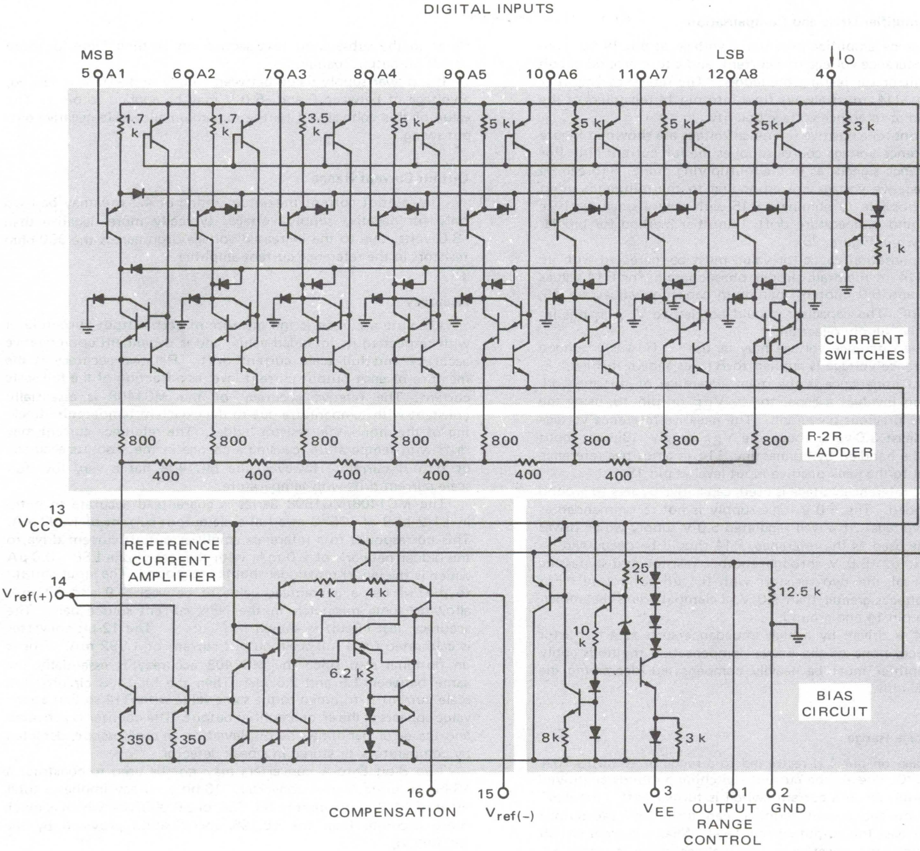

VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
R14
R15
(–) Vref
RL
IO
See text for values of C.
C
3
VEE

FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC


DIGITAL INPUTS
MSB
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
LSB
4
I_O
1.7 k
1.7 k
3.5 k
5 k
5 k
5 k
5 k
5k
3 k
1 k
CURRENT SWITCHES
800
800
800
800
800
800
800
800
R-2R LADDER
400
400
400
400
400
400
13
V_{CC}
REFERENCE CURRENT AMPLIFIER
14
$V_{ref(+)}$
4 k
4 k
6.2 k
350
350
25 k
12.5 k
10 k
8 k
3 k
BIAS CIRCUIT
16
COMPENSATION
15
$V_{ref(-)}$
3
V_{EE}
1
OUTPUT RANGE CONTROL
2
GND

CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

]

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on).

Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

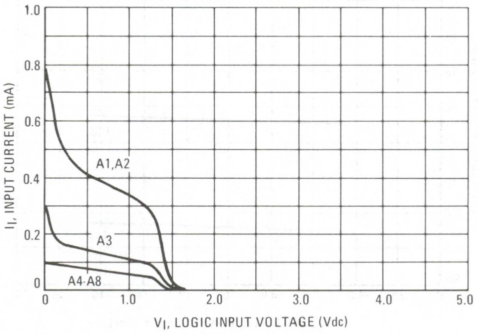


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

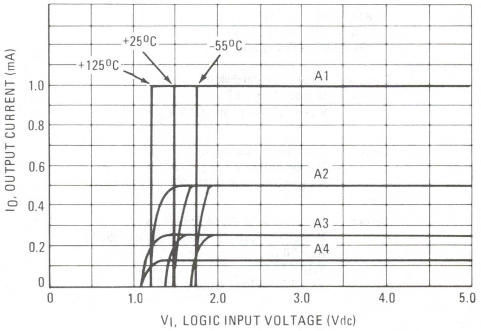


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

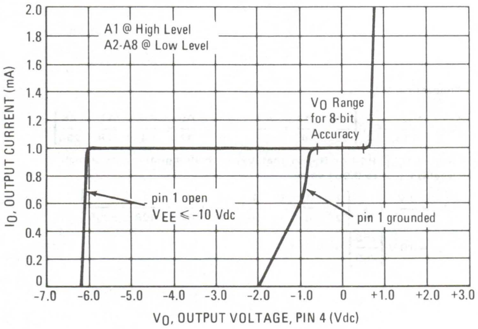
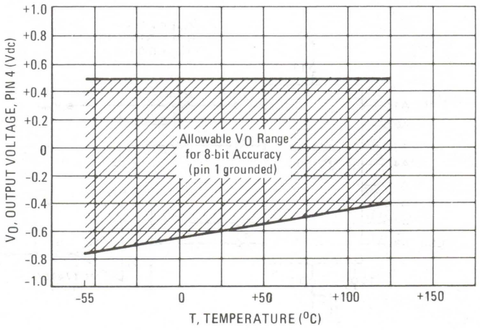


FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is −5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE

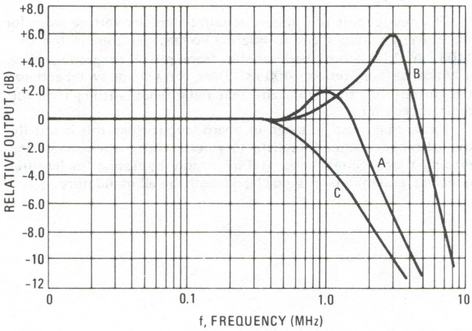
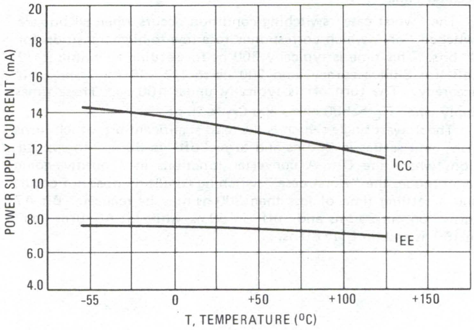


FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)



Unless otherwise specified:

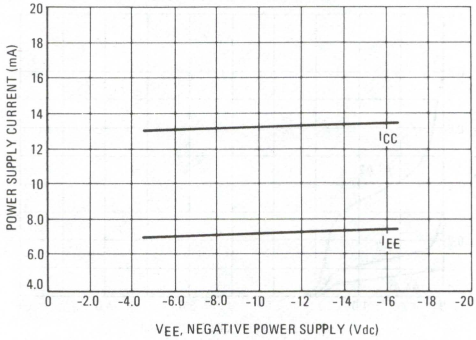
R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

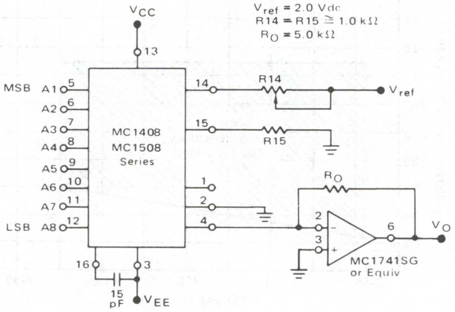
Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION


VCC
13
Vref = 2.0 Vdc
R14 = R15 ≅ 1.0 kΩ
RO = 5.0 kΩ
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1408
MC1508
Series
14
R14
Vref
15
R15
1
2
4
RO
2
3
6
VO
MC1741SG
or Equiv
16
3
15 pF
VEE

Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

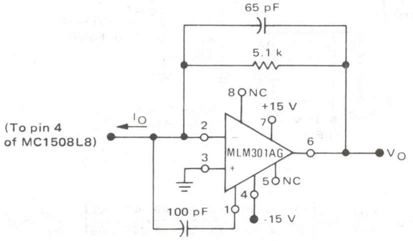
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

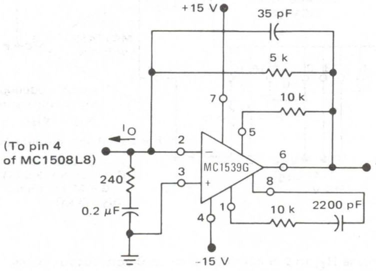
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



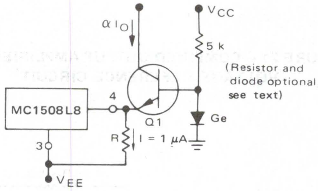
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

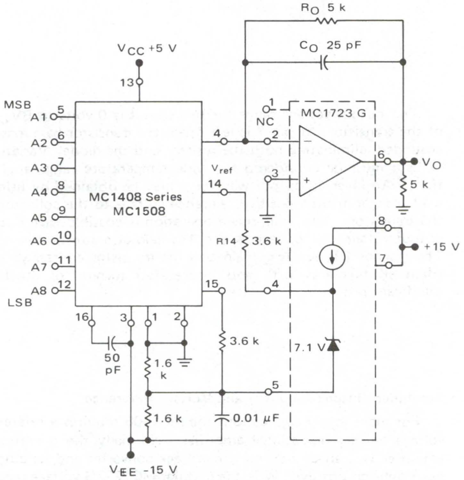
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



R_O 5 k
C_O 25 pF
V_{CC} +5 V
13
MSB
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
LSB
MC1408 Series
MC1508
4
V_{ref}
14
R14 3.6 k
15
16
3
1
2
50 pF
1.6 k
1.6 k
3.6 k
0.01 µF
V_{EE} -15 V
1
NC
2
3
MC1723 G
6
V_O
5 k
8
+15 V
7
4
7.1 V
5

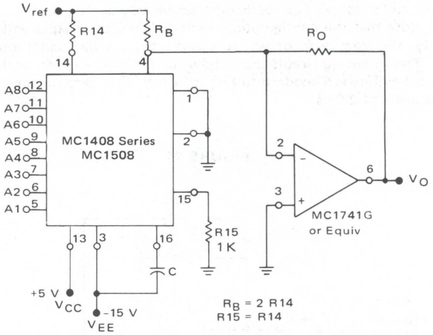
$$V_O = V_{ref} \cdot \frac{R_O}{R14}\{A\}$$

Settling time for a 10-volt step ≅ 1.0 µs

Bipolar or Negative Output Voltage

The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT

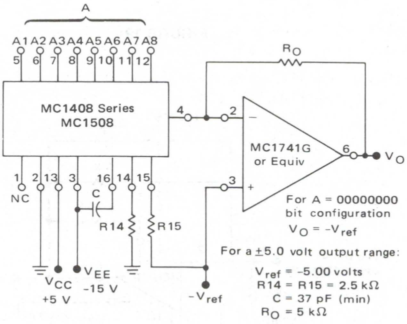


V_{ref}
R14
R_B
R_O
14
4
A8 12
A7 11
A6 10
A5 9
A4 8
A3 7
A2 6
A1 5
MC1408 Series
MC1508
1
2
15
13
3
16
R15
1 K
C
+5 V
V_{CC}
-15 V
V_{EE}
2
3
6
V_O
MC1741G
or Equiv

R_B = 2 R14
R15 = R14

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



A
A1 A2 A3 A4 A5 A6 A7 A8
5 6 7 8 9 10 11 12
R_O
MC1408 Series
MC1508
4
2
3
6
V_O
MC1741G
or Equiv
1 2 13 3 16 14 15
NC
C
R14
R15
V_{CC}
+5 V
V_{EE}
-15 V
$-V_{ref}$

For A = 00000000 bit configuration
$V_O = -V_{ref}$

For a ±5.0 volt output range:
V_{ref} = -5.00 volts
R14 = R15 = 2.5 kΩ
C = 37 pF (min)
R_O = 5 kΩ

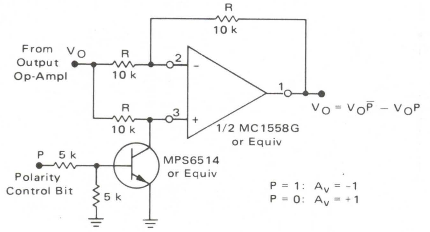
Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 — POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)


R
10 k
From Output Op-Ampl
V_O
R
10 k
R
10 k
2
3
1
$V_O = V_{O\bar{P}} - V_{OP}$
1/2 MC1558G or Equiv
P 5 k
Polarity Control Bit
5 k
MPS6514 or Equiv
P = 1: $A_V = -1$
P = 0: $A_V = +1$

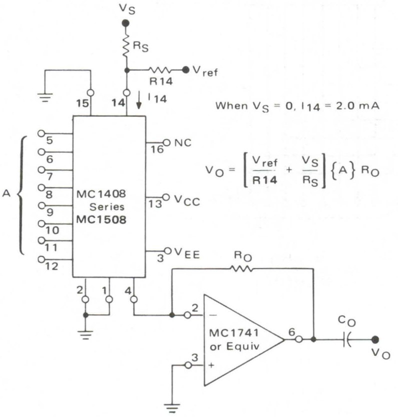
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 — PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT


V_S
R_S
V_{ref}
R14
15
14
I_{14}
When V_S = 0, I_{14} = 2.0 mA
A
5
6
7
8
9
10
11
12
MC1408 Series MC1508
16 NC
13 V_{CC}
3 V_{EE}
$V_O = \left[\frac{V_{ref}}{R14} + \frac{V_S}{R_S}\right]\{A\} R_O$
R_O
2
1
4
2
3
MC1741 or Equiv
6
C_O
V_O

Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 — PANEL METER READOUT CIRCUIT

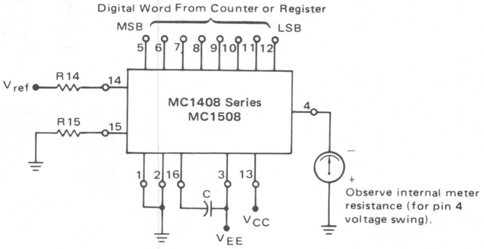
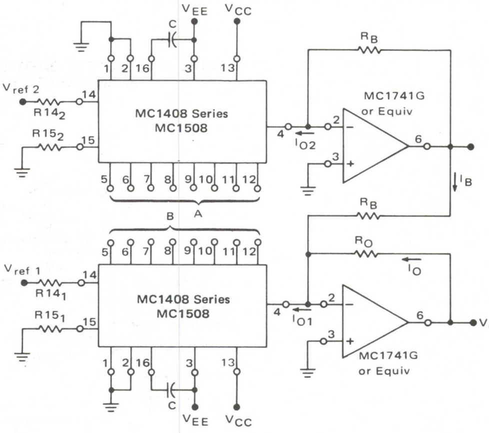

Digital Word From Counter or Register
MSB
LSB
5 6 7 8 9 10 11 12
V_{ref}
R14
14
R15
15
MC1408 Series MC1508
4
−
+
1 2 16 3 13
C
V_{CC}
V_{EE}
Observe internal meter resistance (for pin 4 voltage swing).

FIGURE 27 — DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION


V_{EE}
V_{CC}
C
1 2 16 3 13
$V_{ref\,2}$
$R14_2$
$R15_2$
14
15
MC1408 Series MC1508
4
I_{O2}
5 6 7 8 9 10 11 12
B
A
R_B
MC1741G or Equiv
2
3
6
I_B
R_B
R_O
I_O
5 6 7 8 9 10 11 12
$V_{ref\,1}$
$R14_1$
$R15_1$
14
15
MC1408 Series MC1508
4
I_{O1}
2
3
6
V_O
MC1741G or Equiv
1 2 16 3 13
C
V_{EE}
V_{CC}

$I_O = I_{O\,1} - I_{O\,2} = \frac{V_{ref\,1}}{R14_1}\{A\} - \frac{V_{ref\,2}}{R14_2}\{B\}$

$I_{O\,2} = -I_B$

$I_B + I_O = I_{O\,1}$

Digital Subtraction:

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier:

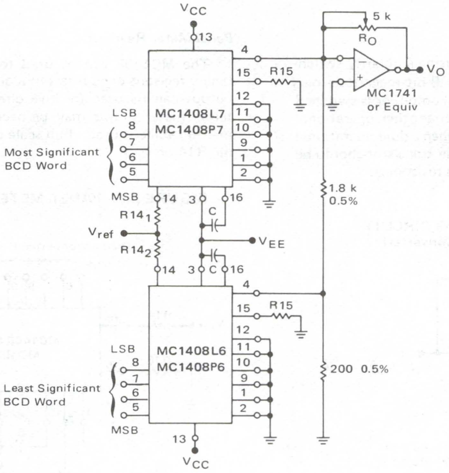
Connect Digital Inputs so A = B

$\boxed{V_O = \frac{V_{ref\,1}}{R14_1} R_O\left[\{A\} - \{B\}\right]}$

$\boxed{V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]}$

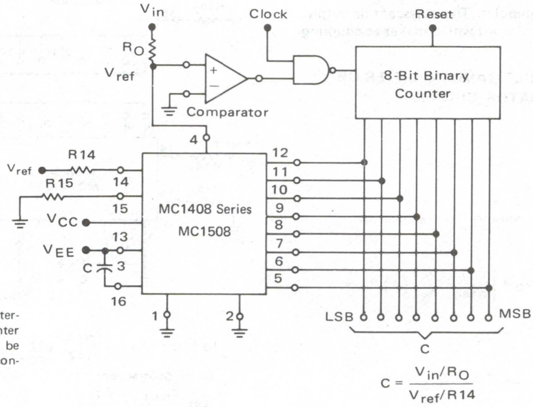
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO-DIGIT BCD CONVERSION


V_{CC}
13
4
15
R15
12
11
10
9
1
2
LSB
MC1408L7
MC1408P7
8
7
6
5
Most Significant BCD Word
MSB
14
3
16
C
$R14_1$
V_{ref}
$R14_2$
V_{EE}
5 k
R_O
V_O
MC1741 or Equiv
1.8 k 0.5%
200 0.5%
MC1408L6
MC1408P6
Least Significant BCD Word
V_{CC}

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION


V_{in}
Clock
Reset
R_O
V_{ref}
Comparator
8-Bit Binary Counter
4
R14
V_{ref}
R15
14
15
V_{CC}
13
V_{EE}
C
3
16
MC1408 Series
MC1508
12
11
10
9
8
7
6
5
1
2
LSB
MSB
C

$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA

MC3410
MC3510 MC3410C

Specifications and Applications Information

LASER TRIMMED

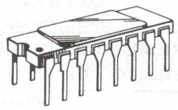
TEN BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

TEN BIT D TO A CONVERTER

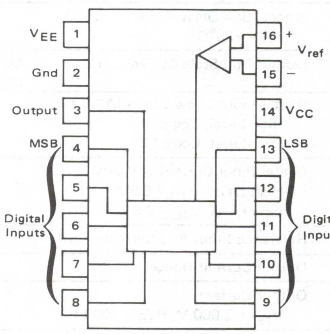
The MC3410 series devices are low-cost, high-accuracy monolithic D/A converter subsystems. Like their MC1408 series predecessors, they provide the logic controlled current switches, the R-2R resistor ladder network and output termination networks. The output buffer amplifier and reference voltage have been omitted from the circuit to allow greatest system speed, flexibility and lowest cost. This device is useful in industrial control and microprocessor based systems.

- Relative Accuracy – ±0.05% Error Maximum (MC3510 and MC3410)
- Fast Settling Time – 250 ns Typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible (from 5 to 15 V CMOS)
- Output Voltage Swing – +0.2 V to −2.5 V
- High Speed Multiplying Input Slew Rate – 20 mA/μs
- Standard Supply Voltages – +5 V and – 15 V
- All Categories Guaranteed Monotonic Across Temperature
- Reference Amplifier Internally Compensated



L SUFFIX
CASE 690-13
(CERAMIC PACKAGE)

PIN CONNECTIONS


VEE 1
Gnd 2
Output 3
MSB 4
5
6
7
8
Digital Inputs
16 +
Vref
15 −
14 VCC
13 LSB
12
11
10
9
Digital Inputs

TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 3-Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Speech Compression and Expansion
- Sample Data Systems

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

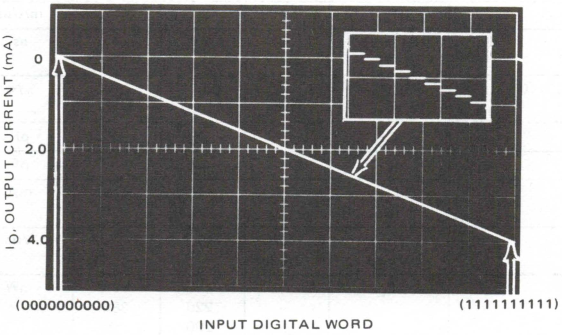
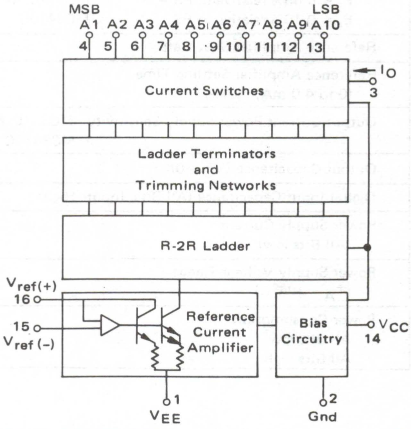


FIGURE 2 – TEN-BIT D/A CONVERTER BLOCK DIAGRAM


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
IO
3
Current Switches
Ladder Terminators and Trimming Networks
R-2R Ladder
Vref(+) 16
15
Vref(−)
Reference Current Amplifier
Bias Circuitry
VCC 14
1 VEE
2 Gnd

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −18	Vdc
Digital Input Voltage	V_I	+15	Vdc
Applied Output Voltage	V_O	+0.5, -5.0	Vdc
Reference Current	$I_{REF(16)}$	2.5	mA
Reference Amplifier Inputs	V_{REF}	V_{CC}, V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{REF(D)}$	0.7	Vdc
Operating Temperature Range MC3510 MC3410,C	T_A	 −55 to +125 0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R16}$ = 2.0 mA, MC3510 T_A = −55°C to +125°C. MC3410 Series: T_A = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) T_A = 25°C MC3510, MC3410 MC3410C	E_r	 – –	 – –	 ±0.05 ±0.1	%
Relative Accuracy Temperature Drift (Relative to Full Scale I_O)	TCE_r	–	2.5	–	PPM/°C
Monotonicity (Full Temperature Range)	–	Monotonic to 10 Bits			–
Settling Time to within ±1/2 LSB (T_A = 25°C) (All Bits Low to High)	t_S	–	250	–	ns
Propagation Delay Time T_A = +25°C	t_{PLH} t_{PHL}	– –	35 20	– –	ns
Output Full Scale Current Drift MC3410, MC3410C MC3510	TCI_O	– –	– –	60 70	PPM/°C
Digital Input Logic Levels (All Bits) High Level, Logic "1" Low Level, Logic "0"	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (All Bits) High Level, V_{IH} = 5.5V Low Level, V_{IL} = 0.8V	 I_{IH} I_{IL}	 – –	 – 0.05	 0.04 0.4	mA
Reference Input Bias Current (Pin 15)	$I_{REF(15)}$	–	−1.0	−5.0	µA
Output Current Range	I_{OR}	0	4.0	5.0	mA
Output Current V_{ref} = 2.000 V, R_{16} = 1000 Ω	I_O	 3.8	 3.996	 4.2	mA
Output Current MC3510, MC3410 (All bits low) (T_A = 25°C) MC3410C	$I_{O(min)}$	– –	0 0	2.0 4.0	µA
Output Voltage Compliance (T_A 25°C) $E_r \leqslant 0.05\%$ relative to FS – MC3510, MC3410 $E_r \leqslant 0.10\%$ relative to FS – MC3410C	V_O	 –	 –	 -2.5,+0.2 -2.5,+0.2	Vdc
Reference Amplifier Slew Rate	SR I_{ref}	–	20	–	mA/µs
Reference Amplifier Settling Time (0 to 4.0 mA, ±0.1%)	STI_{REF}	–	2.0	–	µs
Output Current Power Supply Sensitivity MC3510, MC3410 MC3410C	PSRR(−)	– –	0.003 0.003	0.01 0.02	%/%
Output Capacitance (V_O = 0)	C_O	–	25	–	pF
Digital Input Capacitance (All Bits, Inputs High)	C_I	–	4.0	–	pF
Power Supply Current (All Bits low)	I_{CC} I_{EE}	– –	+10 −11.4	+18 −20	mA
Power Supply Voltage Range (T_A = +25°C)	V_{CCR} V_{EER}	+4.75 -14.25	+5.0 −15	+5.25 −15.75	Vdc
Power Consumption All Bits low All Bits high	P_C	 – –	 220 200	 380 –	mW

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUITS

V_I and I_I apply to inputs A1 thru A10

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \; \frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}+\frac{A9}{512}+\frac{A10}{1024}$$

where $K \cong \frac{2\,V_{ref}}{R16}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Typical Values:
R15 = R16 = 1 k
V_{ref} (+) = +2.0 V
V_{ref} (–) = Gnd
I_O = 4.0 mA

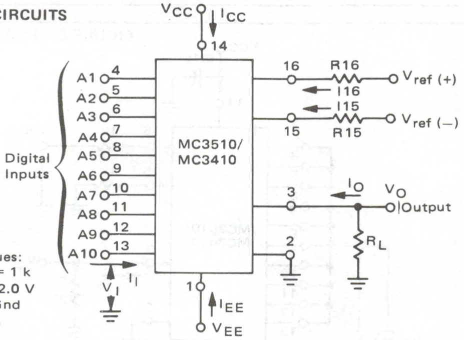

V_{CC}
I_{CC}
14
Digital Inputs
A1 4
A2 5
A3 6
A4 7
A5 8
A6 9
A7 10
A8 11
A9 12
A10 13
V_I
I_I
MC3510/
MC3410
16
R16
V_{ref} (+)
I_{16}
I_{15}
V_{ref} (–)
15
R15
3
I_O
V_O
Output
2
R_L
1
I_{EE}
V_{EE}

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

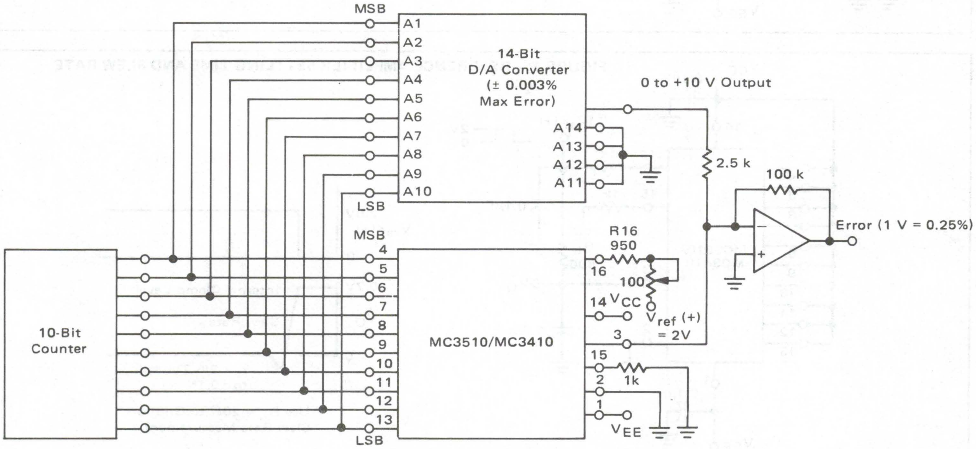
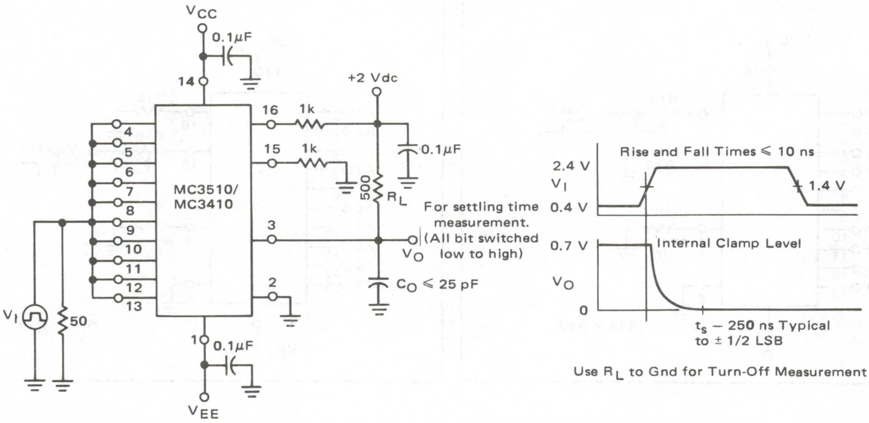

MSB
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
LSB
14-Bit
D/A Converter
(± 0.003%
Max Error)
A14
A13
A12
A11
0 to +10 V Output
2.5 k
100 k
Error (1 V = 0.25%)
10-Bit
Counter
MSB
4
5
6
7
8
9
10
11
12
13
LSB
MC3510/MC3410
R16
950
16
100
14 V_{CC}
V_{ref} (+)
= 2V
3
15
2 1k
1
V_{EE}

FIGURE 5 – SETTLING TIME


V_{CC}
0.1μF
14
+2 Vdc
16 1k
15 1k
0.1μF
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
500
R_L
3
2
V_O
C_O ≤ 25 pF
V_I
50
1
0.1μF
V_{EE}
Rise and Fall Times ≤ 10 ns
2.4 V
V_I
0.4 V
1.4 V
0.7 V
Internal Clamp Level
V_O
0
t_s – 250 ns Typical
to ± 1/2 LSB

For settling time measurement. (All bit switched low to high)

Use R_L to Gnd for Turn-Off Measurement

TEST CIRCUITS (Continued)

FIGURE 6 – PROPAGATION DELAY TIME

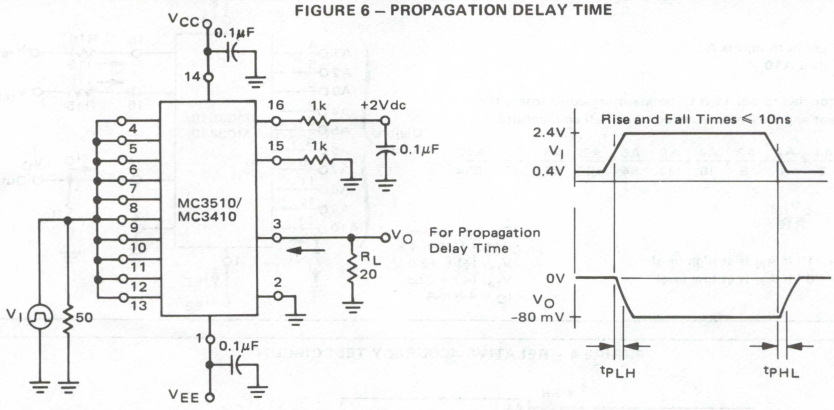

VCC
0.1µF
14
16
1k
+2Vdc
15
1k
0.1µF
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
3
VO
For Propagation
Delay Time
RL
20
2
VI
50
1
0.1µF
VEE
Rise and Fall Times ≤ 10ns
2.4V
VI
0.4V
0V
VO
–80 mV
tPLH
tPHL

FIGURE 7 – REFERENCE AMPLIFIER SETTLING TIME AND SLEW RATE

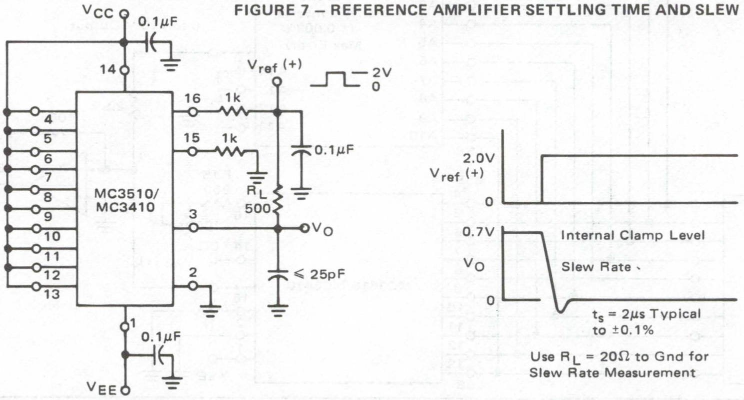

VCC
0.1µF
14
Vref (+)
2V
0
16
1k
15
1k
0.1µF
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
RL
500
3
VO
≤ 25pF
2
1
0.1µF
VEE
2.0V
Vref (+)
0
0.7V
Internal Clamp Level
VO
Slew Rate
0
ts = 2µs Typical
to ±0.1%
Use RL = 20Ω to Gnd for
Slew Rate Measurement

FIGURE 8 – POSITIVE V_{ref}

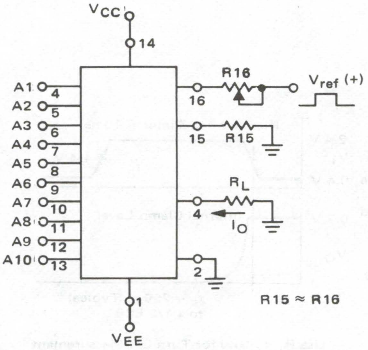

VCC
14
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
4
5
6
7
8
9
10
11
12
13
R16
16
Vref (+)
15
R15
RL
4
IO
2
1
VEE
R15 ≈ R16

FIGURE 9 – NEGATIVE V_{ref}

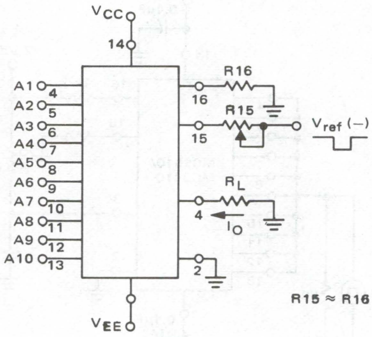
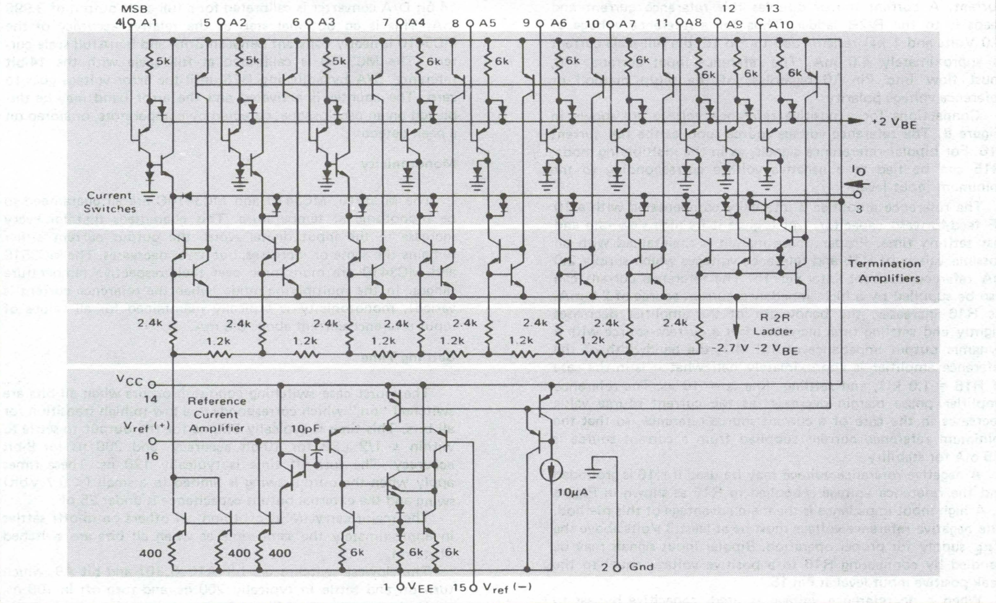

VCC
14
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
4
5
6
7
8
9
10
11
12
13
R16
16
R15
15
Vref (–)
RL
4
IO
2
VEE
R15 ≈ R16

FIGURE 10 — MC3410 10-BIT D/A CONVERTER EQUIVALENT CIRCUIT



CIRCUIT DESCRIPTION

The MC3410 consists of a reference current amplifier, a diffused R-2R ladder, a laser trimming network, and ten high-speed current switches. The trimming method employed makes it possible to improve the linearity attainable with modern diffusion technology by as much as a factor of ten so that a highly linear part results. The trim is performed by cutting aluminum links arranged to give incremental variations in voltage at the ladder termination amplifiers (See Figure 10). This yields a highly stable trim with no increase in fabrication complexity.

The switches are non-inverting in operation, so that a high state on an input turns on the specific component of output current. The switches use current steering for speed, and interface the R-2R ladder through unity gain feedback termination amplifiers, which provide low impedance terminations of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the current switches. The three least-significant bit switches derive their current through emitter scaling from the last leg of the ladder. The remaining current, equal to one LSB, is shunted to V_{CC} at the LSB switch. Therefore, the maximum output current is 1023/1024 of the reference amplifier current, or nominally 3.996 mA for a 2.000 mA reference input current.

Reference Voltage

To generate the precision voltage reference input for the MC3410, either the MC1403 or the MC1404 may be used. The MC1403 produces a 2.5 V ±1% output voltage while the MC1404 produces a 10 V ±1% output. Both have excellent temperature and long term stability. In order to reduce the effect of reference amplifier offset voltage on overall accuracy, the highest possible stability reference voltage should be used. Therefore, in systems with a +15 V supply, the MC1404 (10 V) is recommended. Where the most positive supply is only +5 V, the MC1403 provides a 2.5 V reference. To set the reference current exactly, a low temperature coefficient potentiometer in series with R1 should be used.

GENERAL INFORMATION

Reference Amplifier

The reference amplifier allows the user to provide a voltage and a resistor to Pin 16 to convert the reference voltage to a current. A current mirror doubles this reference current and feeds it to the R-2R ladder. Thus for a reference voltage of 2.0 Volts and 1 kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0 mA. The reference input current, I16, must flow into Pin 16 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 8. The reference voltage source supplies the full current I16. For bipolar refererence signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level.

The reference amplifier is internally compensated with a 10 pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0 mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0 mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0 MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0 kΩ, and settling time is ≈ 10 µs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5 mA for stability.

A negative reference voltage may be used if R16 is grounded and the reference voltage is applied to R15 as shown in Figure 9. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3 Volts above the V_{EE} supply for proper operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0 V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1 µF capacitor to ground.

Output Voltage Range

The voltage on Pin 3 is restricted to a range of −2.5 V to +0.2 V due to the current switching methods employed in the MC3410. When a current switch is turned off, the positive voltage at the output terminal can turn on the output diode and increase the output current. When a current switch is on, the negative output voltage range is restricted to the point at which the low current device of the termination amplifier Darlington begins to saturate, resulting in a decrease in output current.

The output voltage compliance is guaranteed at 25°C. Note from Figure 14 that the output compliance of the MC3410 is nearly constant over temperature.

Accuracy

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the diffused resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full scale current drift with temperature.

The MC3510 and MC3410 are guaranteed accurate to within ±1/2 LSB at 25°C and at a full scale current of 3.996 mA. Input reference current to Pin 16 is guaranteed to be between 1.9 and 2.1 mA to produce a full scale output current of 3.996 mA. The relative accuracy test circuit is shown in Figure 4. The 14 bit D/A converter is calibrated for a full scale output of 3.996 mA. This is an optional step as the relative accuracy of the MC3410 is nearly constant between 3 mA and 5 mA full scale current. The MC3410 is calibrated at full scale with the 14-bit reference D/A by adjusting R16 until the error voltage goes to zero. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored on a peak detector.

Monotonicity

The MC3510, MC3410 and MC3410C are all guaranteed to be monotonic at temperature. This guarantees that for every increase in the input digital word, the output current either remains the same or increases, but never decreases. The MC3510 and MC3410 are monotonic over their respective temperature ranges. In the multiplying mode (when the reference current is varied), monotonicity is typically maintained for all values of input reference current above 0.5 mA.

Settling Time

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200 ns for 8-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (< 0.7 Volt) swing and the external output capacitance is under 25 pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

The slowest switches are bit A10 (LSB) and bit A9, which turn on and settle in typically 200 ns, and turn off in 100 ns.

In the test circuit of Figure 5, the output voltage is internally clamped in the MC3410 at about 0.7 Volts above ground. The output is thus limited to a 0.7 Volt swing. If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5 µs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100µF supply bypassing, and minimum scope lead length are all necessary.

MC3510 TERMINOLOGY

RELATIVE ACCURACY – Maximum output deviation from the straight line connecting zero and full scale, expressed as a percentage of full scale.

RELATIVE ACCURACY DRIFT – The average change in linearity error that will occur with a change in ambient temperature, expressed in parts per million of full scale per degree C.

MONOTONICITY – For every increase in the input digital word, the output current either remains the same or increases.

SETTLING TIME – The elapsed time from the input transition until the output has settled within an error band about its final value.

OUTPUT FULL SCALE CURRENT DRIFT – The average change in full scale current between 25°C and either temperature extreme, expressed in parts per million of full scale per degree C.

REFERENCE AMPLIFIER SLEW RATE – The maximum rate of change of the full scale output current expressed in milliamperes per microsecond.

OUTPUT VOLTAGE COMPLIANCE – The maximum voltage that can be applied to the output pin so that the specified change in output current is not exceeded.

POWER SUPPLY SENSITIVITY – The change in full scale current caused by a change in V_{EE}, expressed as a percent of full scale current per percent change in V_{EE}.

TYPICAL CHARACTERISTICS

FIGURE 11 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

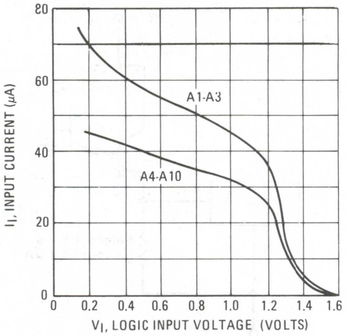


FIGURE 12 – TRANSFER CHARACTERISTIC versus TEMPERATURE

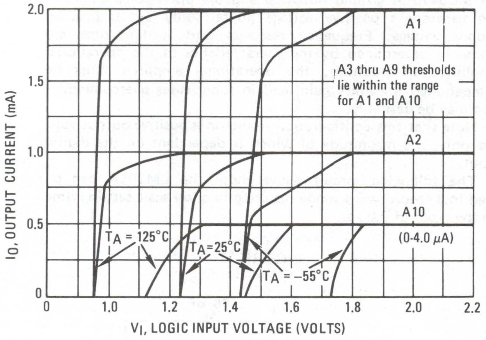


FIGURE 13 – OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Compliance)

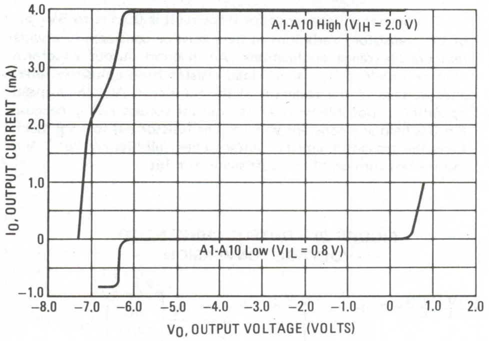


FIGURE 14 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

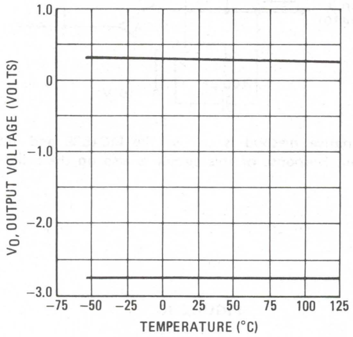


FIGURE 15 – REFERENCE AMPLIFIER FREQUENCY RESPONSE

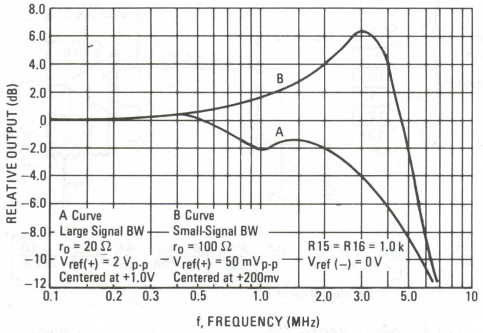
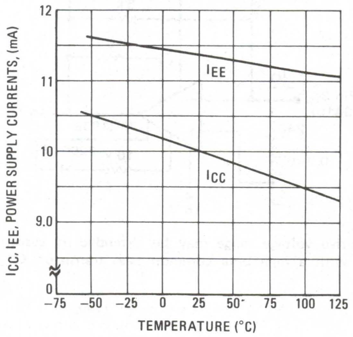


FIGURE 16 – TYPICAL POWER SUPPLY CURRENTS versus TEMPERATURE



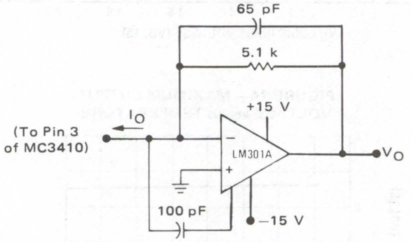
APPLICATIONS INFORMATION

Voltage outputs are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC3410 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

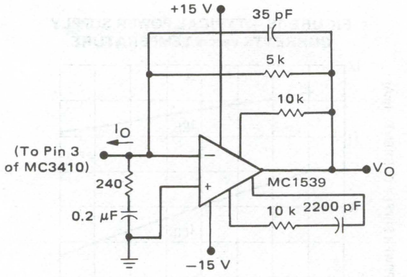
The following circuit shows how the LM301A can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17


65 pF
5.1 k
+15 V
I_O
(To Pin 3 of MC3410)
LM301A
−
+
V_O
100 pF
−15 V

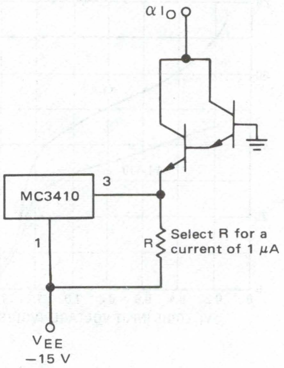
An alternative method is to use the MC1539 and input compensation. Response of this circuit is also on the order of 2.0 μs.

FIGURE 18


+15 V
35 pF
5 k
10 k
I_O
(To Pin 3 of MC3410)
240
0.2 μF
−
+
MC1539
V_O
10 k
2200 pF
−15 V

The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

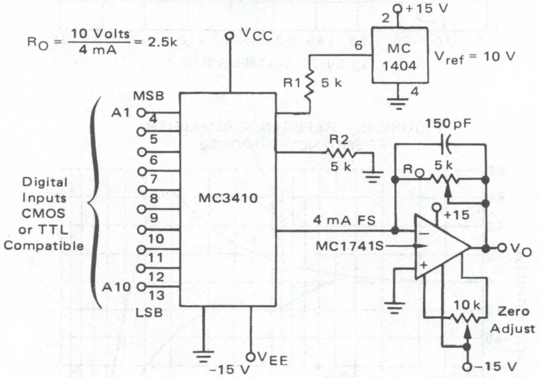
FIGURE 19 – EXTENDING POSITIVE VOLTAGE RANGE


αI_O
MC3410
3
1
R
Select R for a current of 1 μA
V_{EE}
−15 V

The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because Pin 3 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

FIGURE 20 – OUTPUT CURRENT TO VOLTAGE CONVERSION

$R_O = \frac{10\ \text{Volts}}{4\ \text{mA}} = 2.5\text{k}$


V_{CC}
+15 V
2
6
MC 1404
V_{ref} = 10 V
4
R1
5 k
MSB
A1
4
5
6
7
8
9
10
11
12
13
A10
LSB
Digital Inputs CMOS or TTL Compatible
MC3410
150 pF
R2
5 k
R_O
5 k
+15
4 mA FS
MC1741S
−
+
V_O
10 k
Zero Adjust
−15 V
V_{EE}
−15 V

$$V_O = \frac{2R_O}{R_1} V_{ref} \left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024} \right]$$

for 10 volt fullscale calibration

$$V_O = \frac{2(2.5\ \text{k})}{5.0\ \text{k}} 10\ \text{Volts} \left[\frac{1023}{1024}\right] \qquad V_O = 10\ \text{Volts}\ [0.9990]$$

R_O = Full Scale Adjust

APPLICATIONS INFORMATION (Continued)

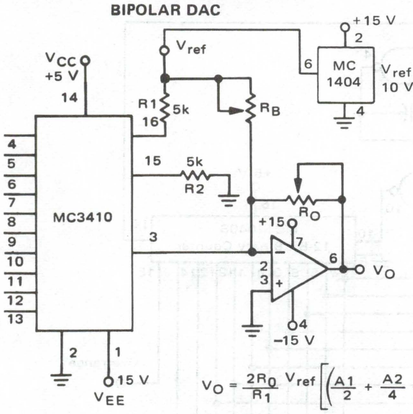
Bipolar or Negative Output Voltage

The circuit in Figure 21 is a variation of the standard output voltage circuit in Figure 20. A negative or offset binary output may be obtained by sourcing current from the reference into the output through R_B. If R_B allows 2 mA (R_B = 5 kΩ from 10 Volts) then 1000000000 input will generate zero output voltage.

Successive Approximation A to D

The fastest and most efficient means of A to D conversion using D to A convertors is successive approximation (SA). Similar in appearance to staircase devices, the SA converter is capable of 100 times faster conversions for a 10-bit result. A complete 10-bit SA coverter using MC3410 and MC14559B/49B successive approximation registers is shown in Figure 22. The complexity which results in higher conversion speeds is contained in the MC14559B/49B registers. Quite simply, the register compares the DAC output resulting from activating each bit with the input voltage. This is done starting with most significant bit and after 10 comparisons generates the 10-bit binary output representing that input. The accuracy of the conversion is fixed by the accuracy of the MC3410 and is not dependent on tolerances of the other components. An EOC outout is available and can be used to latch the parallel output or to synchronize the serial output which is also available. For more details on SA converters, see AN-716.

FIGURE 21 – OFFSET BINARY OR BIPOLAR DAC


+15 V
2
6
MC
1404
4
Vref = 10 V
Vref
VCC
+5 V
14
R1
5k
16
RB
4
5
6
7
8
9
10
11
12
13
MC3410
15
5k
R2
3
RO
+15
7
2
3
6
VO
4
-15 V
2
1
15 V
VEE

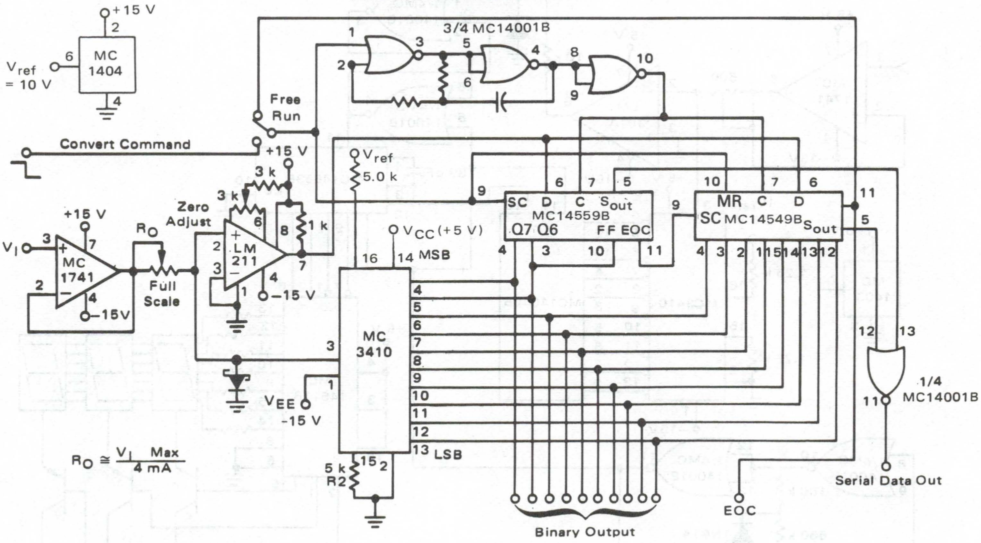
For Offset Binary Output From +5 V to −5 V

$R_O \cong 2.5\ k\Omega$

$R_B \cong 5\ k\Omega$

$$V_O = \frac{2R_O}{R_1} V_{ref}\left[\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}+\frac{A9}{512}+\frac{A10}{1024}\right)-\frac{2R_1}{R_B}\right]$$

FIGURE 22 – SUCCESSIVE APPROXIMATION CONVERTER USING MC3410 AND MC1404


+15 V
2
Vref = 10 V
6
MC
1404
4
3/4 MC14001B
1
2
3
5
6
4
8
9
10
Free Run
Convert Command
+15 V
3 k
3 k
Zero Adjust
6
8
1 k
+
LM
211
2
3
7
4
1
-15 V
Vref
5.0 k
+15 V
VI
3
7
MC
1741
2
4
-15V
RO
Full Scale
VCC (+5 V)
16
14 MSB
MC
3410
3
1
VEE
-15 V
4
5
6
7
8
9
10
11
12
13 LSB
5 k
R2
15
2
9
6
7
5
SC
D
C
Sout
MC14559B
Q7 Q6
FF EOC
4
3
10
11
9
10
7
6
MR
C
D
SC MC14549B Sout
4
3
2
11
15
14
13
12
11
5
12
13
1/4 MC14001B
11
Serial Data Out
EOC
Binary Output
RO ≅ VI Max / 4 mA

APPLICATIONS INFORMATION (Continued)

Staircase A to D

If high conversion speed is not required, a staircase A to D convertor can be built for somewhat lower cost. A complete staircase A/D convertor is shown in Figure 23. Here the complicated SA registers are replaced with simple binary counters. With an input voltage applied, the binary counter is reset by the convert command pulse and the begin accumulating counts. The DAC output steps upward until the comparator detects that the input is equal to the DAC output. The counters are disabled and the conversion result is held at the output until the circuit is reset by the convert command input.

One advantage of staircase convertors is the ease with which BCD outputs may be obtained. Figure 24 shows a 3-digit panel meter using the staircase technique and an MC14553B 3-decade counter. The circuit function is similar to Figure 23 but Multiplexed BCD output is available from the MC14553B counters. Parallel BCD may be obtained with equal ease using the MC14518B 2-decade CMOS counters.

In both these staircase designs the system accuracy is determined by the specified accuracy of the MC3410.

FIGURE 23 – 10-BIT STAIRCASE A to D USING MC3410 AND MC1403

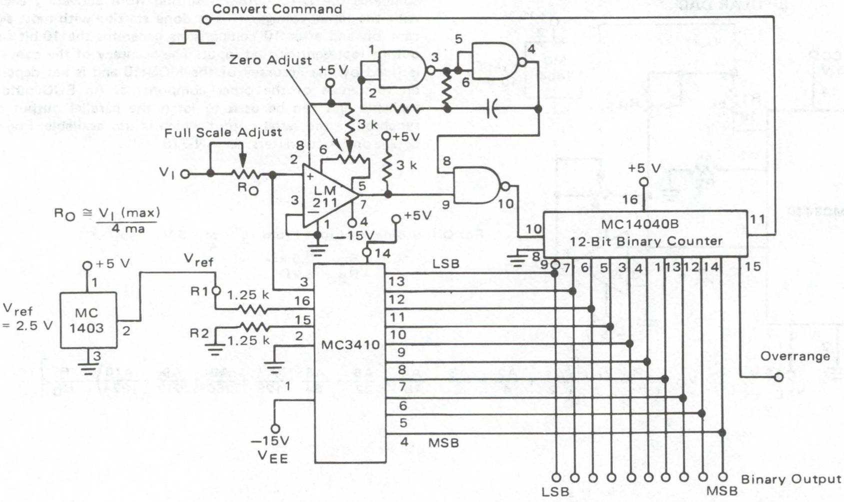
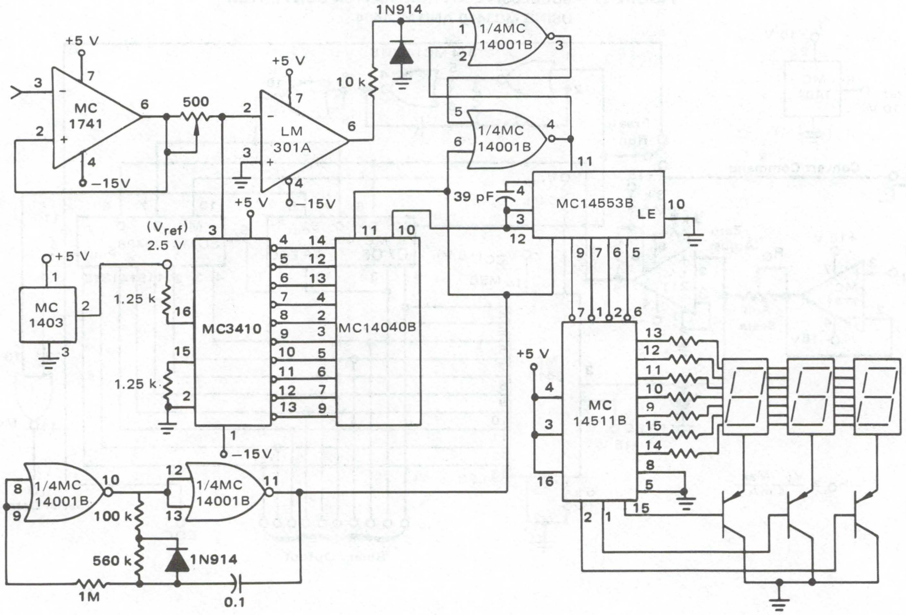
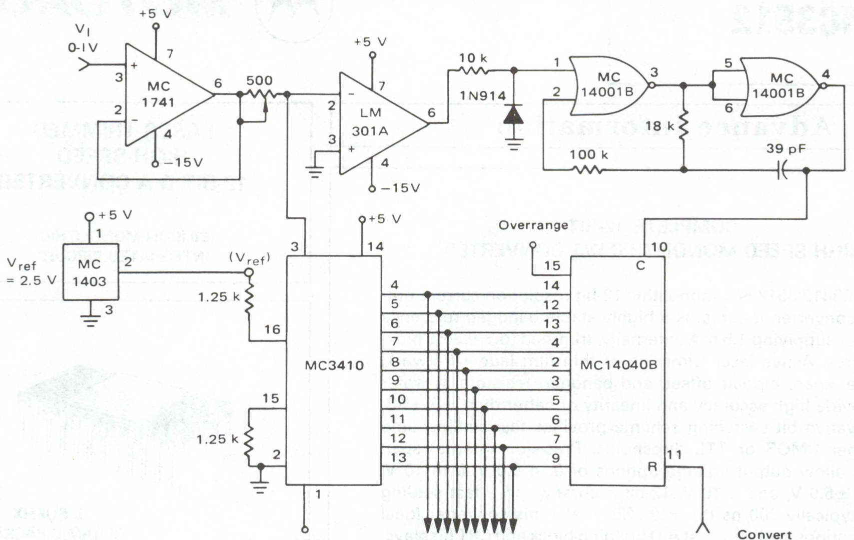

Convert Command
Zero Adjust
+5 V
3 k
Full Scale Adjust
V_I
R_O
LM 211
−15V
$R_O \cong \frac{V_I\,(max)}{4\,ma}$
V_{ref} = 2.5 V
MC 1403
V_{ref}
R1 1.25 k
R2 1.25 k
MC3410
−15V
V_{EE}
LSB
MSB
MC14040B
12-Bit Binary Counter
Overrange
LSB
MSB
Binary Output

FIGURE 24 – 3-DIGIT DVM USING MC3410 AND MC1403


+5 V
MC 1741
−15V
500
LM 301A
10 k
1N914
1/4MC 14001B
39 pF
MC14553B
LE
(V_{ref}) 2.5 V
MC 1403
1.25 k
MC3410
MC14040B
MC 14511B
100 k
560 k
1M
0.1

APPLICATIONS INFORMATION (Continued)

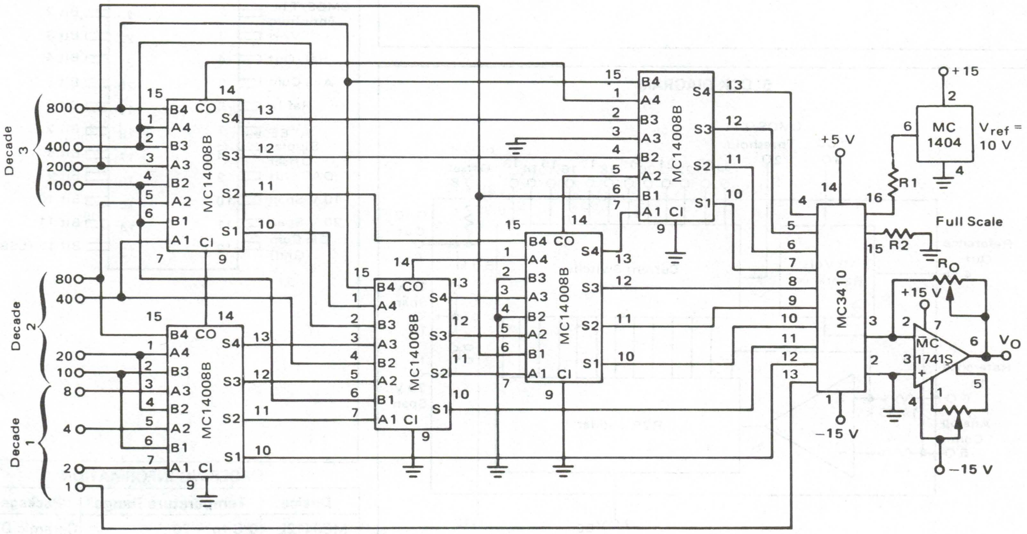
FIGURE 25 – ALTERNATE APPROACH STAIRCASE A TO D


V_I 0-1V
+5 V
MC 1741
−15 V
500
+5 V
LM 301A
−15 V
10 k
1N914
MC 14001B
MC 14001B
18 k
100 k
39 pF
+5 V
MC 1403
V_ref = 2.5 V
(V_ref)
1.25 k
1.25 k
+5 V
MC3410
−15 V
Overrange
MC14040B
C
R
MSB
LSB
Convert Command

BCD D to A Converter

BCD output A to D conversions are most easily accomplished by accumulating the digital results in two different counters, but that concept does not extend to BCD Dto A techniques. Using the circuit in Figure 26 a three-digit BCD number can be converted to a 10-bit accurate voltage.|The MC14008B's perform the combinational BCD-to-Binary conversion. The accuracy of this circuit is also solely dependent on the accuracy of the MC3410.

FIGURE 26 – 3-DECADE BCD DAC


Decade 3
800
400
200
100
Decade 2
800
400
200
100
Decade 1
8
4
2
1
MC14008B
MC14008B
MC14008B
MC14008B
MC14008B
B4 CO
A4
B3
A3
B2
A2
B1
A1 CI
S4
S3
S2
S1
+5 V
MC3410
−15 V
+15
MC 1404
V_ref = 10 V
R1
Full Scale
R2
R_O
+15 V
MC 1741S
V_O
−15 V

MC3412
MC3512

MOTOROLA

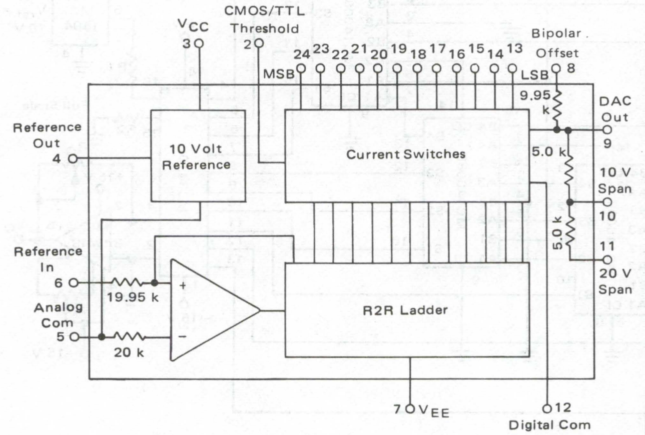
Advance Information

COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

The MC3412/3512 is a monolithic 12-bit resolution current output D/A converter. It contains a highly stable bandgap reference capable of supplying 1.5 mA externally, trimmed to ±0.25% maximum error. Active laser trimming of thin film ladder network, reference, span, bipolar offset, and bandgap resistors at wafer level provide high accuracy and linearity of better than ±½ LSB. An innovative bit switching scheme provides fast settling time with either CMOS or TTL thresholds. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±½ LSB) make this converter ideal for applications such as a fast A/D building block and CRT displays.

- True 12-Bit Linearity: ±½ LSB Max
- Fast Settling Time: ±½ LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- Highly Stable Bandgap Voltage Reference On Chip
- Linearity Guaranteed Over Temperature
- Low Power Consumption: 210 mW
- Pinout Compatible with AD563 and AD565
- Selectable Digital Thresholds
- Internal Application Resistors for Generating Calibrated Output Voltages

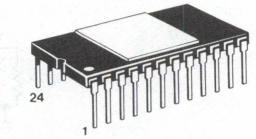
BLOCK DIAGRAM



CMOS/TTL Threshold
2
VCC
3
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Bipolar Offset
8
9.95 k
DAC Out
9
5.0 k
10 V Span
10
5.0 k
11
20 V Span
Reference Out
4
10 Volt Reference
Current Switches
Reference In
6
19.95 k
Analog Com
5
20 k
R2R Ladder
7 VEE
12
Digital Com

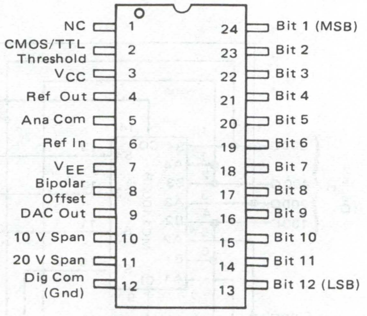
LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 716-06

PIN CONNECTIONS



NC 1
CMOS/TTL Threshold 2
VCC 3
Ref Out 4
Ana Com 5
Ref In 6
VEE 7
Bipolar Offset 8
DAC Out 9
10 V Span 10
20 V Span 11
Dig Com (Gnd) 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3412L	0°C to +70°C	Ceramic DIP
MC3512L	−55°C to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATING (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Analog Ground to Digital Ground	V_{AD}	±1.0	Vdc
Applied Output Voltage (Pin 9)	V_O	−7.0 to +12	Vdc
Digital Input Voltage (Pins 13 to 24)	V_I	−5.0 to +18	Vdc
Reference Input to Analog Ground	V_{RI}	±12	Vdc
Reference Current	I_{REF}	Short circuit to either Com (Ground) or V_{CC}	
Bipolar Offset to Analog Ground		±12	Vdc
Ten Volt Span Resistor to Analog Ground		±12	Vdc
Twenty Volt Span Resistor to Analog Ground		±24	Vdc
Power Dissipation	P_D	1000	mW
Operating Temperature Range MC3412 MC3512	T_A	0 to 70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Junction Temperature Ceramic	T_J	+175	°C

TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to non-monitonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases.

The MC3512 and MC3412 are all guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ± ½ LSB for 12 bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

Unipolar Offset Error — Using the configuration shown in Figure 1, with R1 = 50 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Offset Error — Using the configuration shown in Figure 2, with R2 = 50 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Zero Error — Using the configuration shown in Figure 2, with R1 = R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

Temperature Coefficients — (Unipolar offset, Bipolar offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

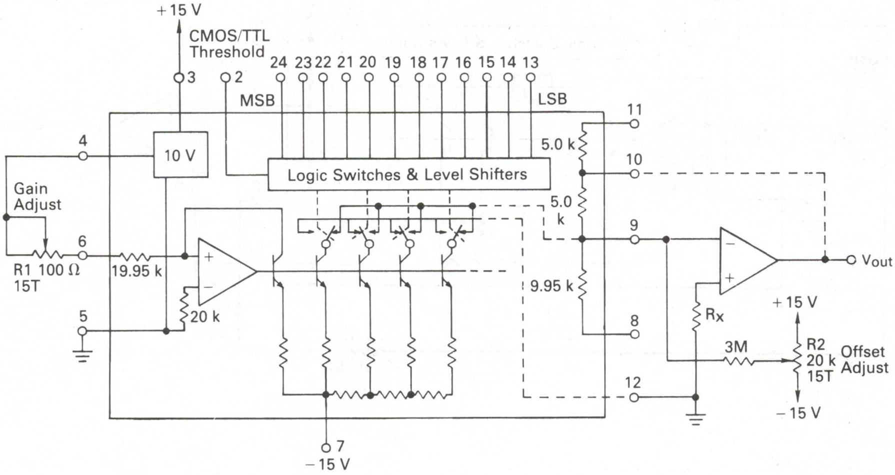
Compliance Voltage Range — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with V_{EE} = − 15. The compliance voltage range follows as V_{EE} is varied.

Power Supply Sensitivity — The change in full scale current caused by a change in V_{EE} or V_{CC} expressed in ppm of full scale current per percent change in V_{EE} or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, MC3512: T_A = −55 to 125°C, MC3412: T_A = 0 to +70°C All tests performed using internal reference, unless otherwise noted.)

Characteristic	Symbol	MC3512			MC3412			Unit
		Min	Typ	Max	Min	Typ	Max	
TTL Digital Logic Levels (All Bits) (Pin 2 open circuit) $13.5 \le V_{CC} \le 16.5$ V								V
Bit On, Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	
CMOS Digital Logic Levels (All Pins) (Pin 2 tied to Pin 3) $13.5 \le V_{CC} \le 16.5$ V								V
Bit On, Logic "1"	V_{IH}	70% V_{CC}	—	—	70% V_{CC}	—	—	
Bit Off, Logic "0"	V_{IL}	—	—	30% V_{CC}	—	—	30% V_{CC}	
Digital Input Current (CMOS/TTL Levels)								µA
Bit On, Logic "1"	I_{IH}	—	+0.02	+1.0	—	+0.02	+1.0	
Bit Off, Logic "0"	I_{IL}	—	−2.0	−75	—	−2.0	−75	
Programmable Output Range See Figures 1 and 2		—	0 to +5.0	—	—	0 to +5.0	—	V
		—	−2.5 to +2.5	—	—	−2.5 to +2.5	—	
		—	0 to +10	—	—	0 to +10	—	
		—	−5.0 to +5.0	—	—	−5.0 to +5.0	—	
		—	−10 to +10	—	—	−10 to +10	—	
Output Current (T_A = 25°C)	I_O							mA
Unipolar (All Bits On)		−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	
Bipolar (All Bits On or Off)		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Output Resistance (T_A = 25°C) (Exclusive of Span Resistors)	R_O	1.0	5.0	—	1.0	5.0	—	MΩ
Output Capacitance (T_A = 25°C)	C_O	—	25	—	—	25	—	pF
Output Compliance Voltage Range	V_{OC}	−5.0	—	+10	−5.0	—	+10	V
Nonlinearity (T_A = 25 °C)	NL	— —	±¼ (0.006)	±½ (0.012)	— —	±¼ (0.006)	±½ (0.012)	LSB % of FS
Nonlinearity	NL	— —	±½ (0.012)	±¾ (0.018)	— —	±½ (.012)	±¾ (0.018)	LSB % of FS
Differential Nonlinearity (T_A = 25°C)		—	±½	±¾	—	±½	±¾	LSB
Differential Nonlinearity		Monotonicity Guaranteed						
Gain Error — Figure 1, R1 = Fixed 50 Ω (T_A = 25°C)		—	±0.1	±0.25	—	±0.1	±0.25	% of FS
Offset Error								
Unipolar — Figure 1		—	±0.01	±0.05	—	±0.01	±0.05	% of FS
Bipolar — Figure 2, R2 = Fixed 50 Ω (T_A = 25°C)		—	±0.05	±0.15	—	±0.05	±0.15	
Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 50 Ω (T_A = 25°C)		—	±0.05	±0.15	—	±0.05	±0.15	$ of FS
Gain Adjustment Range — Figure 1 (T_A = 25°C)		±0.25	—	—	±0.25	—	—	% of FS
Bipolar Offset Adjustment Range — Figure 2 (T_A = 25°C)		±0.15	—	—	±0.15	—	—	% of FS
Unipolar Zero Temperature Coefficient		—	1.0	2.0	—	1.0	2.0	ppm/°C
Bipolar Zero Temperature Coefficient		—	5.0	10	—	5.0	10	ppm/°C
Gain Temperature Coefficient, Full Scale		—	15	30	—	15	30	ppm/°C
Differential Nonlinearity Temperature Coefficient		—	2.0	—	—	2.0	—	ppm/°C
Settling Time to ½ LSB (T_A = 25°C) All Bits On-to-Off or Off-to-On	t_s	—	200	400	—	200	400	ns
Reference Input Impedance (T_A = 25°C)	Z_{in}	15	20	25	15	20	25	kΩ
Reference Output Voltage (T_A = 25°C)	V_{RO}	9.950	10.00	10.050	9.950	10.00	10.050	Volts
Reference Output Current — Available to External Loads (T_A = 25°C)	I_{RO}	1.5	2.5	—	1.5	2.5	—	mA
Power Supply Current								mA
V_{CC} +13.5 to +16.5 Vdc	I_{CC}	—	6.0	10	—	6.0	10	
V_{EE} −10.8 to −16.5 Vdc (T_A = 25°C)	I_{EE}	—	−8.0	−12	—	−8.0	−12	
Power Supply Gain Sensitivity								ppm of FS/%
V_{CC} +13.5 to +16.5 Vdc	$PSSI_{FS+}$	—	0.5	10	—	2.0	10	
V_{EE} −10.8 to −16.5 Vdc (T_A = 25°C)	$PSSI_{FS-}$	—	2.0	25	—	3.0	25	

FIGURE 1 — MC3412 IN TYPICAL UNIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
3
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
10 V
4
Gain Adjust
6
R1 100 Ω 15T
19.95 k
20 k
5
Logic Switches & Level Shifters
11
5.0 k
10
5.0 k
9
9.95 k
8
12
7
−15 V
Vout
Rx
3M
+15 V
R2 20 k 15T
Offset Adjust
−15 V

UNIPOLAR DAC OPERATION

A typical circuit configuration for unipolar operation of MC3412 is shown in Figure 1.

Step 1 — Output Range

Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

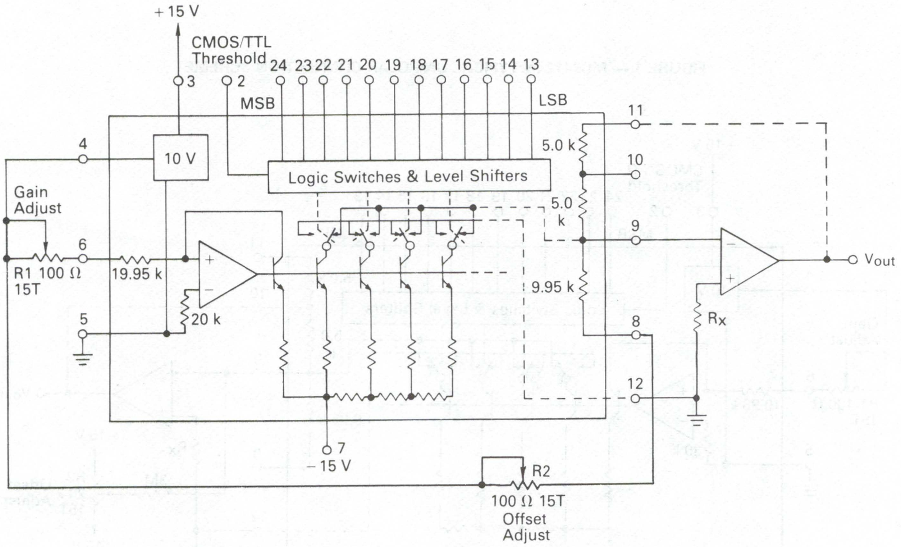
Step 2 — Zero Adjust

Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

Step 3 — Gain Adjust

Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — MC3412 IN TYPICAL BIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
3
2
24
23
22
21
20
19
18
17
16
15
14
13
MSB
LSB
11
4
10 V
5.0 k
10
Logic Switches & Level Shifters
Gain Adjust
5.0 k
9
6
R1 100 Ω 15T
19.95 k
Vout
9.95 k
5
20 k
Rx
8
12
7
−15 V
R2
100 Ω 15T
Offset Adjust

BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of MC3412 is shown in Figure 2.

Step 1 — Output Range

Determine which output range is required. For ±2.5 Volts full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

Step 2 — Offset Adjust

Turn all bits OFF. Adjust R2 until operational amplifier output is:

−2.5000 Volt for ±2.5 Volt range
−5.0000 Volt for ±5.0 Volt range
−10.0000 Volt for ±10 Volt range

Step 3 — Gain Adjust (Bipolar Zero)

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

NOTES:

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For high voltage CMOS compatibility, short Pin 2 to Pin 3.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, R_X should be made equal to the internal feedback resistor. In bipolar, R_X equals the feedback resistor in parallel with 10 k.

MOTOROLA

MC6890

Advance Information

MPU-BUS-COMPATIBLE 8-BIT D-TO-A CONVERTER

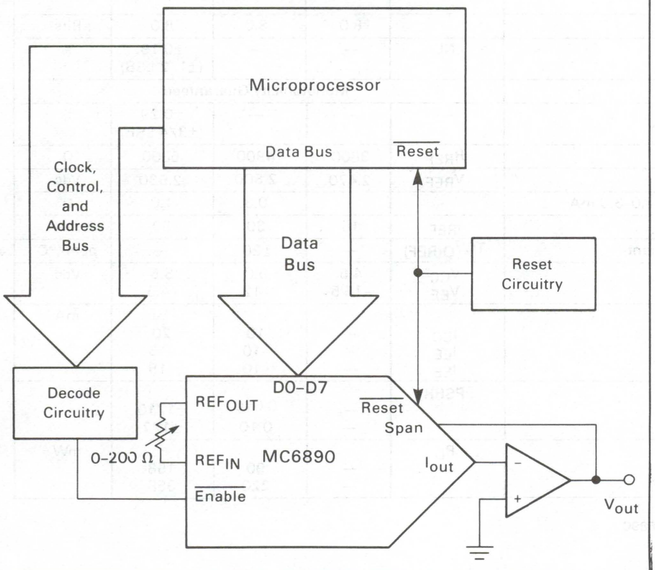
The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

A reset pin provides for overriding stored data and forcing I_{out} to zero.

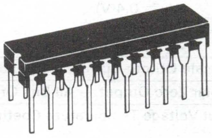
- Direct Data Bus Link with All Popular TTL Level MPU's
- ±1/2 LSB Nonlinearity Over Temperature
- Fast Settling Time: 200 ns Typ
- Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Minimum $\overline{\text{Enable}}$ Pulse Width: 70 ns
- Fast Enable: 10 ns Maximum Data Hold Time
- $\overline{\text{Reset}}$ Pin to Override Data
- Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts
- Low Power: 90 mW Typ
- +5 V and −5 V to −15 V Supplies

OPERATION WITH AN MPU


Microprocessor
Data Bus
$\overline{\text{Reset}}$
Clock, Control, and Address Bus
Data Bus
Reset Circuitry
Decode Circuitry
D0–D7
REF_{OUT}
0–200 Ω
REF_{IN}
MC6890
$\overline{\text{Enable}}$
$\overline{\text{Reset}}$
Span
I_{out}
−
+
V_{out}

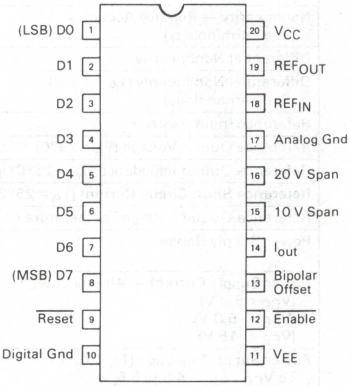
8-BIT MPU-BUS-COMPATIBLE DAC

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CASE 732-03

PIN CONNECTIONS


(LSB) D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
(MSB) D7 8
$\overline{\text{Reset}}$ 9
Digital Gnd 10
20 V_{CC}
19 REF_{OUT}
18 REF_{IN}
17 Analog Gnd
16 20 V Span
15 10 V Span
14 I_{out}
13 Bipolar Offset
12 $\overline{\text{Enable}}$
11 V_{EE}

ORDERING INFORMATION

Device	Temperature Range	Package
MC6890L	0° to +70°C	Ceramic DIP
MC6890AL	−55° to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −18	Vdc
Digital Input Voltage, Pins 1-8, 12 Pin 9	V_{in}	−3.0 to +7.0 0 to +7.0	Vdc
Applied Output Voltage	V_{14}	V_{EE} +2.0 to V_{EE} +24	Vdc
Reference Amplifier Input	V_{18}	±7.5	Vdc
Operating Temperature Range MC6890L, MC6890AL	T_A	 0 to +70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −12 V, Pin 18 loaded only by Pin 19 through 100 Ω. Reset high, $T_A = T_{low}$ to T_{high}[(1)], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Logic Levels High Level, Logic 1 Low Level, Logic 0	 V_{IH} V_{IL}	 2.0 —	 — —	 — 0.8	Vdc
Digital Input Current Data (V_{IH} = 3.0 V) (V_{IL} = 0.4 V) Enable (V_{IH} = 3.0 V) (V_{IL} = 0.4 V) $\overline{\text{Reset}}$ (V_{IH} = 5.0 V) (V_{IL} = 0.4 V)	 I_{IH} I_{IL} I_{IH} I_{IL} I_{IH} I_{IL}	 — — — — — —	 0.001 0.5 0.001 −6.5 0.001 −1.0	 1.0 −10 1.0 −100 1.0 −15	 μA μA μA μA μA μA
Full Scale Output Current — Unipolar	I_O	−1.50	−1.992	−2.50	mA
Unipolar Zero Output — All Bits Off (T_A = 25°C)	—	—	0.010	0.20	μA
Output Voltage Temperature Coefficient Unipolar Zero Bipolar Zero Full Scale Range	TCV_O	 — — —	 ±1.0 ±5.0 ±20	 ±2.0 ±15 ±50	ppm of FSR/°C
Output Voltage, Full Scale Range (See Figure 3) (T_A = 25°C) (10 V Span) (20 V Span) (5.0 V Span)	V_O	 9.861 19.722 4.930	 9.961 19.922 4.980	 10.061 20.122 5.030	Vdc
Output Voltage, Bipolar Zero (MSB on) (See Figure 4) (T_A = 25°C) (10 V Span) (20 V Span) (5.0 V Span)	V_O	 — — —	 0 0 0	 ±20 ±40 ±10	mV
DAC Output Resistance — Exclusive of Span Resistors (T_A = 25°C) (See Figure 5)	r_O	1.0	5.0	—	MΩ
Resolution	—	8.0	8.0	8.0	Bits
Nonlinearity — Relative Accuracy (See Terminology)	NL	—	—	±0.19 (±1/2 LSB)	%
Differential Nonlinearity			Monotonicity Guaranteed		
Differential Nonlinearity (T_A = 25°C) (See Terminology)	—	—	—	±0.29 (±3/4 LSB)	%
Reference Input Resistor	R_{REF}	3800	4900	6800	Ω
Reference Output Voltage (T_A = 25°C)	V_{REF}	2.470	2.500	2.530	Vdc
Reference Output Impedance (T_A = 25°C) I_{load} = 0–3.0 mA	—	—	0.3	1.0	Ω
Reference Short Circuit Current (T_A = 25°C)	I_{REF}	15	30	50	mA
Reference Output Voltage Temperature Coefficient	$TCV_{O(REF)}$	—	±20	—	ppm/°C
Power Supply Range	V_{CC} V_{EE}	4.5 −16.5	5.0 −12	5.5 −4.5	Vdc
Power Supply Current — All Bits Low (V_{CC} = 5.0 V) (V_{EE} = −5.0 V) (V_{EE} = −15 V)	 I_{CC} I_{EE} I_{EE}	 — — —	 10 −10 −10	 20 −15 −15	mA
Power Supply Rejection (T_A = 25°C) To V_{CC} (V_{CC} = 4.5 to 5.5 V) To V_{EE} (V_{EE} = −4.5 V to −16.5 V)	PSRR	 — —	 0.010 0.10	 ±1/10 ±1/2	LSB
Power Dissipation — All Bits Low For V_{CC} = 4.5 V, V_{EE} = −4.5 V For V_{CC} = 5.5 V, V_{EE} = −16.5 V	P_D	 — —	 90 220	 158 358	mW

NOTE 1: T_{low} = −55°C for MC6890A, 0° for MC6890
T_{high} = +125°C for MC6890A, +70°C for MC6890

AC SPECIFICATIONS (V_{CC} = 5.0 V, V_{EE} = −12 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Settling Time (Enable Positive Edge to ±1/2 LSB Output)	t_s	—	200	300*	ns
Data Setup Time	$t_{su(D)}$	70	40	—	ns
Data Hold Time	$t_{h(D)}$	10	0	—	ns
Pulse Widths					ns
$\overline{\text{Enable}}$	$t_{W(\overline{E})}$	70	20	—	
$\overline{\text{Reset}}$	$t_{W(\overline{R})}$	100*	—	—	
Propagation Delays					ns
$\overline{\text{Enable}}$, Low to High	$t_{PLH(\overline{E})}$	—	100	—	
Reset, High to Low (I_O < 1.0 μA)	$t_{PHL(\overline{R})}$	—	250	—	

*Not 100% tested, guaranteed by design

FIGURE 1 — TIMING DIAGRAM

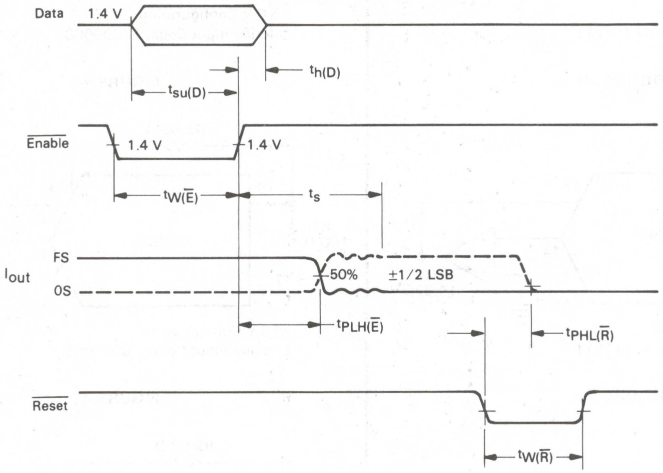
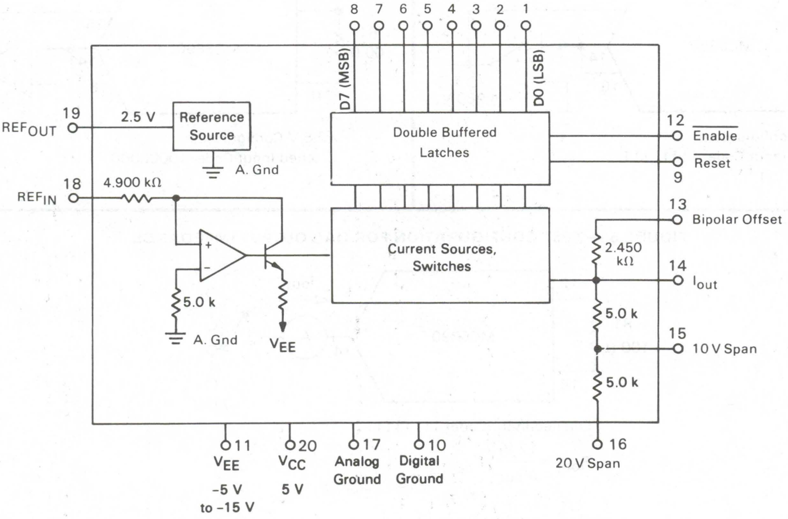

Data
1.4 V
$t_{h(D)}$
$t_{su(D)}$
$\overline{\text{Enable}}$
1.4 V
1.4 V
$t_{W(\overline{E})}$
t_s
FS
I_{out}
OS
50%
±1/2 LSB
$t_{PLH(\overline{E})}$
$t_{PHL(\overline{R})}$
$\overline{\text{Reset}}$
$t_{W(\overline{R})}$

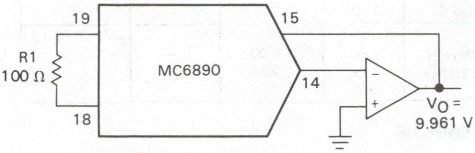
FIGURE 2 — BLOCK DIAGRAM


8 7 6 5 4 3 2 1
D7 (MSB)
D0 (LSB)
19
REF_{OUT}
2.5 V
Reference Source
A. Gnd
18
REF_{IN}
4.900 kΩ
Double Buffered Latches
12
$\overline{\text{Enable}}$
$\overline{\text{Reset}}$
9
13
Bipolar Offset
Current Sources, Switches
2.450 kΩ
14
I_{out}
5.0 k
15
10 V Span
5.0 k
5.0 k
A. Gnd
V_{EE}
11
V_{EE}
−5 V to −15 V
20
V_{CC}
5 V
17
Analog Ground
10
Digital Ground
16
20 V Span

TEST FIGURES

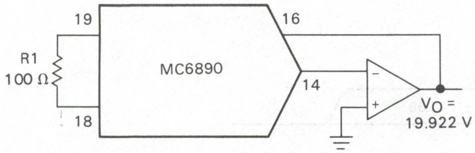
UNIPOLAR CONFIGURATIONS

FIGURE 3A


19
15
R1
100 Ω
MC6890
14
18
V_O =
9.961 V

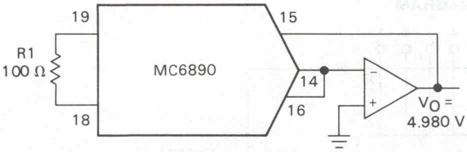
+10 V Configuration
Latched Input Code: 11111111

FIGURE 3B


19
16
R1
100 Ω
MC6890
14
18
V_O =
19.922 V

+20 V Configuration
Latched Input Code: 11111111

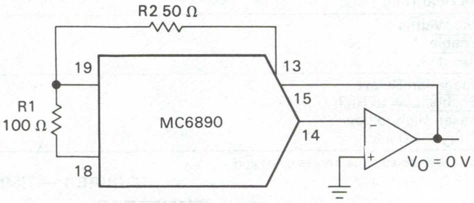
FIGURE 3C


19
15
R1
100 Ω
MC6890
14
16
18
V_O =
4.980 V

+5.0 V Configuration
Latched Input Code: 11111111

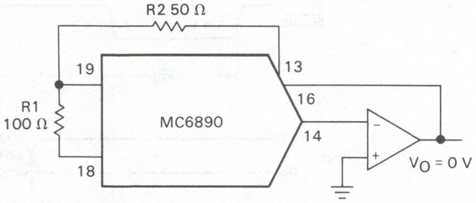
BIPOLAR CONFIGURATIONS

FIGURE 4A


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
18
V_O = 0 V

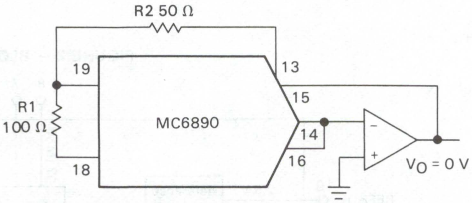
±5.0 V Configuration
Latched Input Code: 10000000

FIGURE 4B


R2 50 Ω
19
13
16
R1
100 Ω
MC6890
14
18
V_O = 0 V

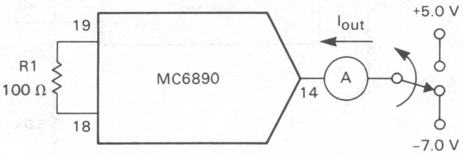
±10 V Configuration
Latched Input Code: 10000000

FIGURE 4C


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
16
18
V_O = 0 V

±2.5 V Configuration
Latched Input Code: 10000000

FIGURE 5 — TEST CONFIGURATION FOR DAC OUTPUT IMPEDANCE


19
R1
100 Ω
MC6890
18
14
I_{out}
A
+5.0 V
−7.0 V

Latched Input Code: 11111111

$$R_{out} = \frac{12\ V}{\Delta I_{out}}$$

TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to non-monotonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases. The MC6890 is guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the $\overline{\text{Enable}}$ positive transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are latched "on," which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the current output to settle to within ±1/2 LSB for 8 bit accuracy. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{255}{256} \times 10\text{ V} =$ 9.961 V.

Gain error is laser trimmed to less than ±1.0% with R1 = 100 Ω (Figure 3) and can be user trimmed to zero error with R1 = 200 Ω pot.

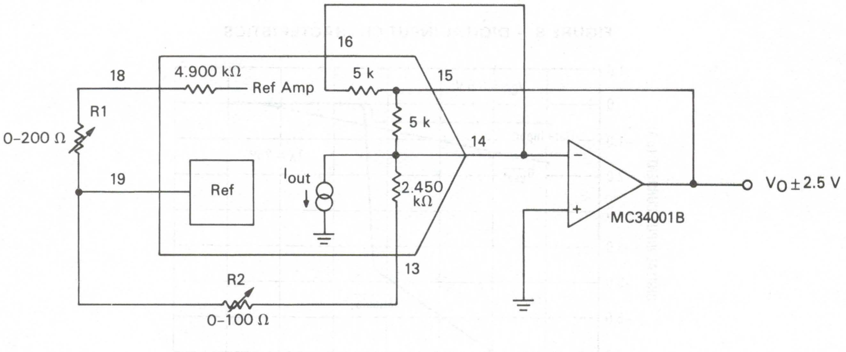
Bipolar Zero — Using the configuration shown in Figure 6 with R1 = 100 Ω, R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to analog ground is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled. Bipolar Zero error is laser trimmed to less than 0.20% and can be user trimmed to zero with R2 = 100 Ω pot.

Temperature Coefficients — (Unipolar zero, Bipolar zero, Gain and Reference Output). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

Power Supply Rejection — The change in full scale current caused by the specified change in V_{EE} or V_{CC} is expressed in LSB's.

$\overline{\text{Reset}}$ Function — The MC6890 has a $\overline{\text{Reset}}$ pin (9) that will force the DAC's registers, and therefore the DAC output current, to zero. This input is active low and should not occur simultaneously with an active $\overline{\text{Enable}}$ signal although no harm would result to the converter. The power dissipation increases slightly during $\overline{\text{Reset}}$ low. $\overline{\text{Reset}}$ should not be allowed to become more negative than ground.

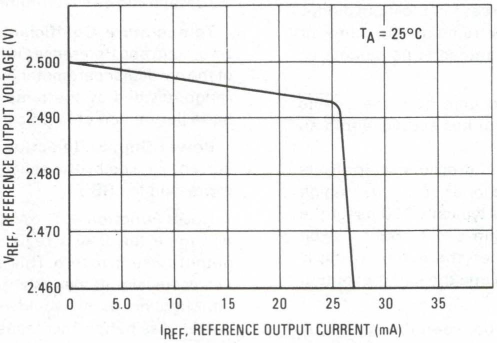
FIGURE 6 — MC6890 IN TYPICAL BIPOLAR ±2.5 V OPERATION



D7	D6	D5	D4	D3	D2	D1	D0	V_O (Volts)	
								R2 ≅ 60 Ω	R2 ≅ 50 Ω
1	1	1	1	1	1	1	1	+2.490	+2.480
1	1	1	1	1	1	1	0	+2.470	+2.460
1	0	0	0	0	0	0	0	+0.010	+0.000
0	1	1	1	1	1	1	1	−0.010	−0.020
0	0	0	0	0	0	0	1	−2.470	−2.480
0	0	0	0	0	0	0	0	−2.490	−2.500

TYPICAL PERFORMANCE CURVES

FIGURE 7 — REFERENCE VOLTAGE versus EXTERNAL LOAD CURRENT*



*External load current is in addition to Reference Input Current (Pin 18) of D/A converter.

FIGURE 8 — DIGITAL INPUT CHARACTERISTICS

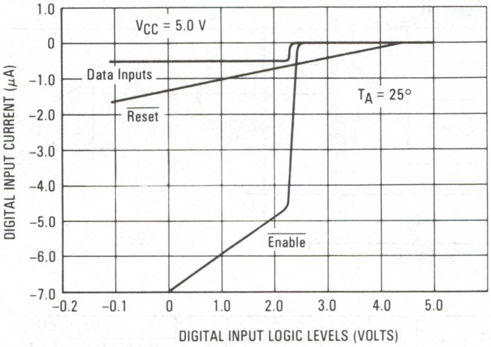
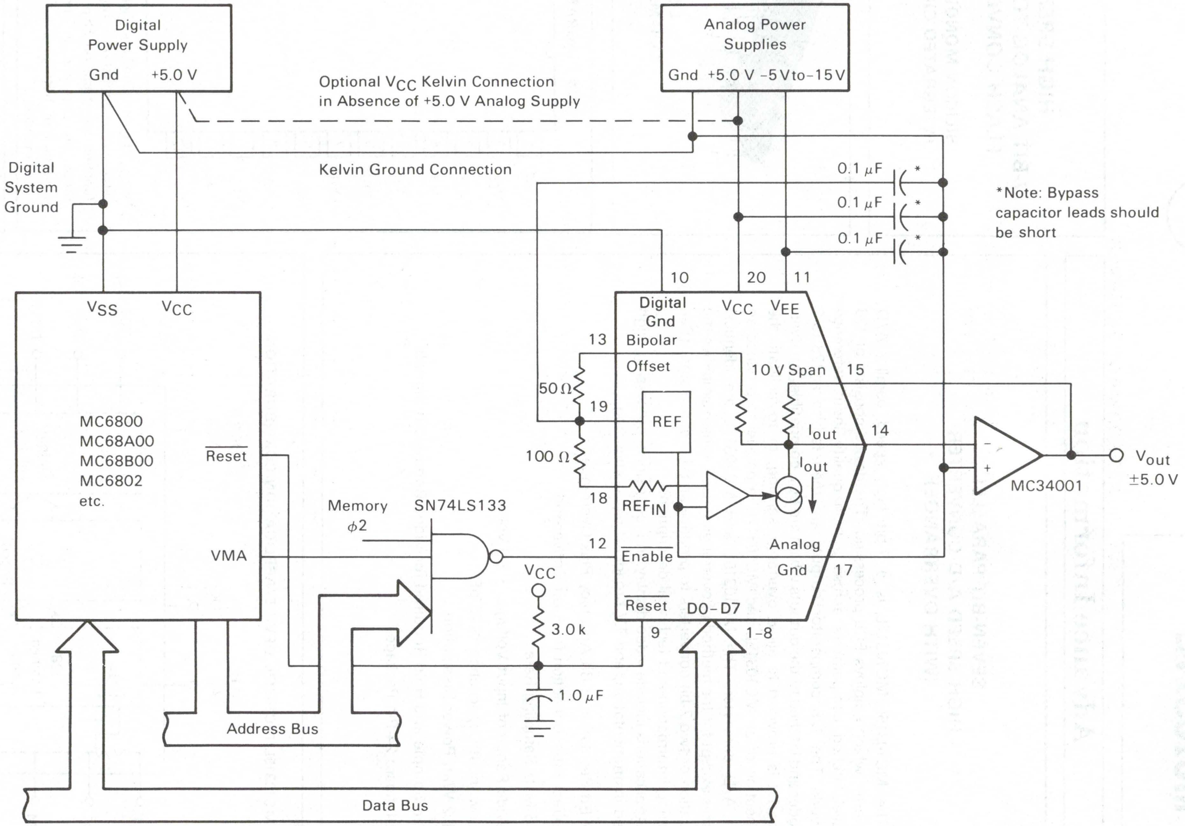


FIGURE 9 — TYPICAL APPLICATION OF THE MC6890 IN A MC6800 SERIES MPU SYSTEM


Digital Power Supply
Gnd
+5.0 V
Analog Power Supplies
Gnd
+5.0 V
-5 V to -15 V
Optional V_{CC} Kelvin Connection in Absence of +5.0 V Analog Supply
Kelvin Ground Connection
Digital System Ground
0.1 μF *
0.1 μF *
0.1 μF *
*Note: Bypass capacitor leads should be short
10
20
11
V_{SS}
V_{CC}
Digital Gnd
V_{CC}
V_{EE}
13
Bipolar Offset
10 V Span
15
50 Ω
19
REF
I_{out}
14
100 Ω
I_{out}
18
REF_{IN}
MC6800
MC68A00
MC68B00
MC6802
etc.
$\overline{Reset}$
MC34001
V_{out}
±5.0 V
Memory
ϕ2
SN74LS133
12
$\overline{Enable}$
Analog Gnd
17
VMA
V_{CC}
3.0 k
$\overline{Reset}$
D0–D7
9
1–8
1.0 μF
Address Bus
Data Bus

MC10315L
MC10317L

MOTOROLA

Advance Information

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

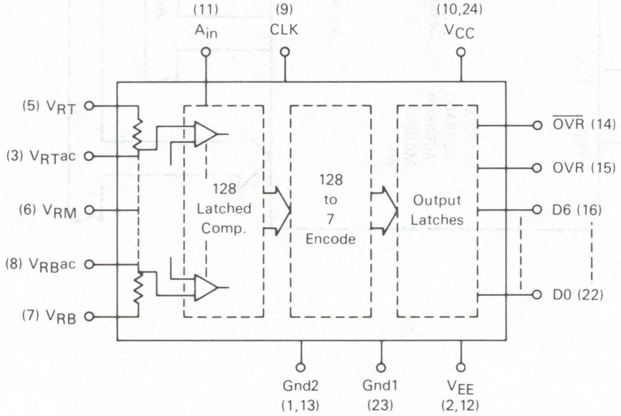
SEVEN-BIT PARALLEL HIGH SPEED A/D CONVERTER (WITH OVERRANGE)

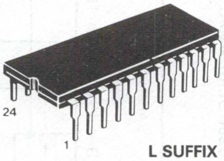
The MC10315L/MC10317L is a 7-bit high speed parallel A/D converter which employs ECL processing. The device consists of 128 parallel latched comparators across a high quality input reference network. The 128 comparator outputs are then fed to a 128-to-7 encoder and latched to the outputs which are ECL compatible. An overrange bit is provided to allow overrange sensing, or to facilitate the connection of an MC10315L and MC10317L in parallel to produce an 8-bit A/D converter. The MC10315L and MC10317L are identical devices except for the method of overranging used, which simplifies the utilization of two 7-bit converters to produce an 8-bit conversion. (See ordering information and technical description.)

Applications include video display and radar signal processing, high speed instrumentation, and TV broadcast video encoding.

- 7-Bit Resolution/8-Bit Accuracy Plus Overrange
- Direct Interconnection for 8-Bit Conversion
- 15 MHz Sampling Rate
- Wide Range of Input Voltage: ±2.0 Volts
- Low Input Capacitance: ≤ 70 pF
- 1.2 Watt Power Dissipation
- No Sample and Hold Required for Video Bandwidth Signals
- Standard 24-Pin Package

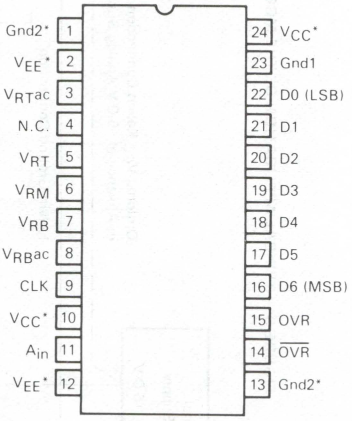
MC10315L/MC10317L DEVICE/APPLICATION CONFIGURATION


(11)
Ain
(9)
CLK
(10,24)
VCC
(5) VRT
(3) VRTac
(6) VRM
(8) VRBac
(7) VRB
128
Latched
Comp.
128
to
7
Encode
Output
Latches
OVR (14)
OVR (15)
D6 (16)
D0 (22)
Gnd2
(1,13)
Gnd1
(23)
VEE
(2,12)



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

PIN DIAGRAM


Gnd2* 1
VEE* 2
VRTac 3
N.C. 4
VRT 5
VRM 6
VRB 7
VRBac 8
CLK 9
VCC* 10
Ain 11
VEE* 12
24 VCC*
23 Gnd1
22 D0 (LSB)
21 D1
20 D2
19 D3
18 D4
17 D5
16 D6 (MSB)
15 OVR
14 OVR
13 Gnd2*

*V_{CC}, V_{EE} and Gnd2 are each available on two pins. Interconnections for the respective function are made on chip. To minimize I•R drops on chip and in the bonding wires, utilization of both pins for each function is recommended.

ORDERING INFORMATION**

Device	Overrange Function		
	Analog Input Condition	Logic Levels	
		OVR Bit	D0-D6 Bits
MC10315L	Overranged	High	High
MC10317L	Overranged	High	Low

**For information regarding an evaluation board, contact Linear Marketing.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted (Note 1))

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+7.0 −8.0	Vdc Vdc
Ground 1	Gnd1	−0.8, +3.0	Volts
Clock Input Voltage	V_{CLK}	0 to V_{EE}	Volts
Analog Inputs: A_{in}, V_{RT}, V_{RB} $\lvert V_{RT} - V_{RB} \rvert$		 +2.5 2.5	Volts
Digital Output Source Current (per Output)	I_{source}	30	mA
Power Dissipation Free Air Convection Air Flow ≥ 500 Lfpm	$P_{D(max)}$	 2.8 4.0	W
Operating Temperature	T_A	0 to +70	°C
Junction Temperature	T_J	165	°C
Storage Temperature Range	T_{stg}	65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Air Free Air Convection Air Flow ≥ 500 Lfpm	$R_{\theta JA}$	 50 35	°C/W

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $V_{EE} = -5.2$ Vdc, $T_A = 25°C$ unless otherwise noted (Note 1))

Characteristic	Symbol	MC10315L/MC10317L			Unit
		Min	Typ	Max	
Resolution $0°C \leq T_A \leq 70°C$		—	—	7	Bits
Non-Linearity fs ≤ 15 MHz, V_{RT}-V_{RB} = 2.0 V	NL	—	±0.16	—	%
Differential Non-Linearity fs ≤ 15 MHz, V_{RT}-V_{RB} = 2.0 V	DNL	—	±0.10	—	%
Offset Error V_{RT}-V_{RB} = 2.0 V Top Bottom	 V_{OSRT} V_{OSRB}	 — —	 ±7.0 ±7.0	 — —	mV
Maximum Sampling Frequency $0°C \leq T_A \leq 70°C$ V_{RT}-V_{RB} = 2.0 V, No Missing Codes	fs	—	15	—	MHz
Aperture Delay Time	t_{ad}	—	3.0	—	ns
Aperture Uncertainty		—	80	—	ps
Data Valid Delay Time $0°C \leq T_A \leq +70°C$	t_{vd}	—	43	—	ns
Comparator Track Delay Time $0°C \leq T_A \leq +70°C$	t_{cd}	—	25	—	ns
Differential Phase Differential Gain fs = 14.3 MHz Unlocked NTSC or PAL Ramp Modulated with 40 IRE Color Subcarrier		— —	1.0 1.5	— —	Deg. %
Maximum Analog Input Slew Rate	SR	—	35	—	V/μs
Analog Input Bias Current $V_{in} \geq V_{RT}$, $0°C \leq T_A \leq +70°C$	I_{IB}	—	300	400	μA
Equivalent Analog Input Resistance V_{RT}-V_{RB} = 2.0 V, $0°C \leq T_A \leq +70°C$	R_{in}	5.0	—	—	KΩ
Analog Input Capacitance $V_{in} \geq V_{RT}$	C_{in}	—	70	—	pF
Reference Ladder Current V_{RT}-V_{RB} = 2.0 V	I_{ref}	24	31	47	mA
Reference Ladder Resistance (Total Resistance)	R_{ref}	—	64	—	Ω

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −5.2 Vdc, T_A = 25°C unless otherwise noted [Note 1]) continued

Characteristic	Symbol	MC10315L/MC10317L Min	Typ	Max	Unit
Reference Ladder Resistance Temperature Coefficient $0°C \leq T_A \leq +70°C$	T_{CR}	—	0.37	—	%/°C
Clock Input Logic Levels, $0°C \leq T_A \leq +70°C$					V
High Logic State	V_{IH}	-1.145	—	—	
Low Logic State Note 2	V_{IL}		—	-1.455	
Clock Input Current					μA
High Logic State	I_{IH}	—	150	—	
Low Logic State	I_{IL}	—	100	—	
Digital Output Logic Levels					V
High Logic State	V_{OH}	1.020	—	—	
Low Logic State $0°C \leq T_A \leq +70°C$ Note 2	V_{OL}	—	—	− 1.605	
Power Supply Current, $0°C \leq T_A \leq +70°C$					mA
$4.75\ V \leq V_{CC} \leq 5.25\ V$	I_{CC}	—	118	150	
$-4.94\ V \geq V_{EE} \geq -5.46\ V$	I_{EE}		-110	-140	

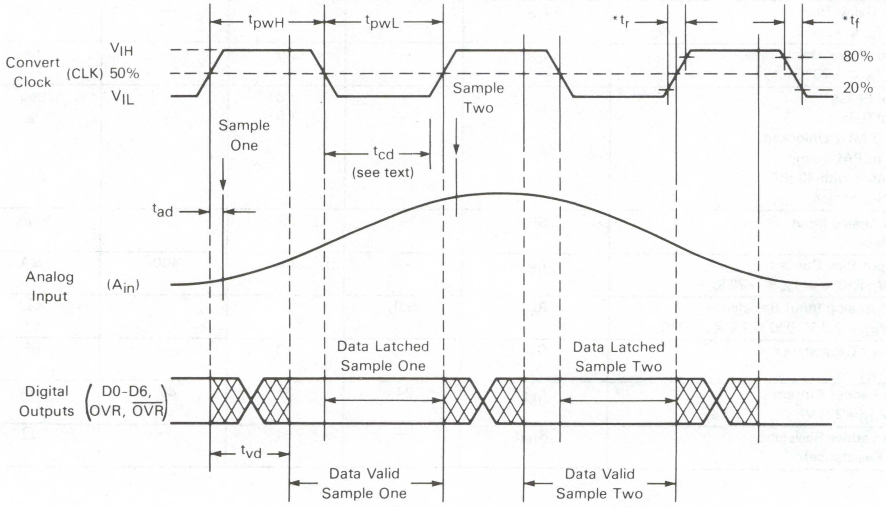
RECOMMENDED OPERATING CONDITIONS (Note 1)

Characteristic	Symbol	MC10315L/MC10317L Min	NOMINAL	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	4.75 5.46	5.0 5.2	5.25 4.94	Vdc
Ground 1	Gnd1	0.3	0	+ 1.0	V
Reference Input, Top	V_{RT}	1.0	0	+ 2.0	V
Reference Input, Bottom	V_{RB}	2.0	0	+ 1.0	V
Reference Input Voltage Range (V_{RT}-V_{RB})	V_{RR}	1.0		2.0	V
Convert Clock Pulse Width, High Convert Clock Pulse Width, Low	t_{pwH} t_{pwL}	44 25			ns
Digital Output Current	I_{OH}		10		mA
Operating Temperature Range	T_A	0		70	°C

Notes:

1. All voltage levels referenced to Ground 2 (Gnd2) unless otherwise noted.
2. MECL 10K logic levels are designed to meet the dc specifications after thermal equilibrium has been established with a transverse airflow greater than 500 Linear fpm and $V_{EE} = -5.2\ V \pm 0.010\ V$. All outputs are specified driving 50Ω to −2.0 V.

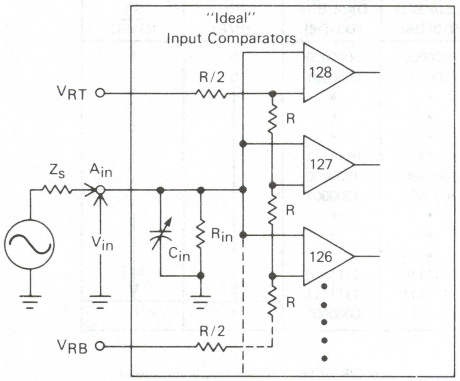
FIGURE 1 — TIMING DIAGRAM



tpwH
tpwL
*tr
*tf
VIH
Convert Clock
(CLK) 50%
VIL
80%
20%
Sample Two
Sample One
tcd
(see text)
tad
Analog Input
(Ain)
Data Latched Sample One
Data Latched Sample Two
Digital Outputs
D0-D6, OVR, $\overline{OVR}$
tvd
Data Valid Sample One
Data Valid Sample Two

*Recommended range of rise (t_r) and fall (t_f) times are 2.0 to 7.0 ns.

FIGURE 2 — EQUIVALENT R_{in} AND C_{in} OF THE ANALOG INPUT


"Ideal"
Input Comparators
128
127
126
R/2
R
R
R
R/2
V_{RT}
V_{RB}
Z_s
A_{in}
V_{in}
C_{in}
R_{in}

$$R_{in} \simeq \frac{|V_{RT}-V_{RB}|}{400\ \mu A}$$

$$^{*}C_{in} \simeq \frac{30\text{pF}}{|V_{RT}-V_{RB}|}\ |V_{in}-V_{RB}| + 40\text{ pF}$$

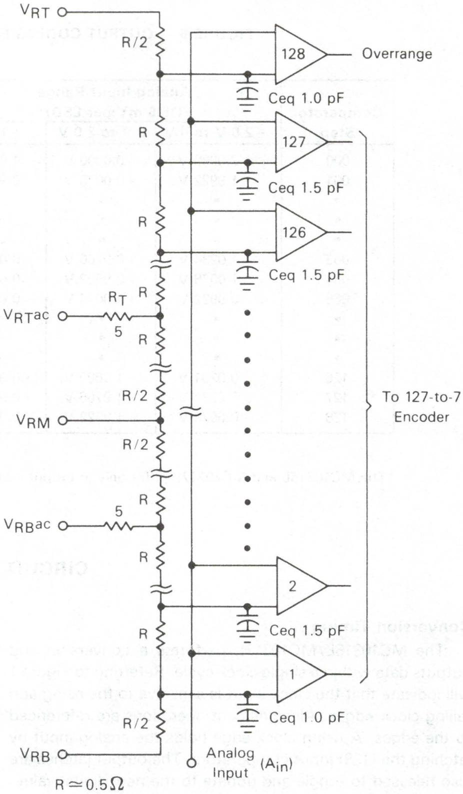
*Valid for $V_{RT} \geqslant V_{in} \geqslant V_{RB}$

$R \simeq 0.5\,\Omega$

R_{in} — Effective input resistance representing the cumulative bias currents of the 128 input comparators.

C_{in} — Equivalent input capacitance variable as a function of V_{in}.

FIGURE 3 — EQUIVALENT CIRCUIT OF REFERENCE RESISTOR LADDER NETWORK


V_{RT}
R/2
128
Overrange
Ceq 1.0 pF
R
127
Ceq 1.5 pF
R
126
Ceq 1.5 pF
R
R_T
V_{RTac}
5
R
R/2
V_{RM}
R/2
R
5
V_{RBac}
R
2
R
Ceq 1.5 pF
1
Ceq 1.0 pF
R/2
V_{RB}
Analog Input (A_{in})
To 127-to-7 Encoder

$R \simeq 0.5\,\Omega$

Ceq — The lumped equivalent value of capacitance representing the distributed capacitance for each resistor (R) and the input capacitance for each comparator.

FIGURE 4 — CLOCK INPUT IS STANDARD MECL INPUT WITH EMITTER FOLLOWER

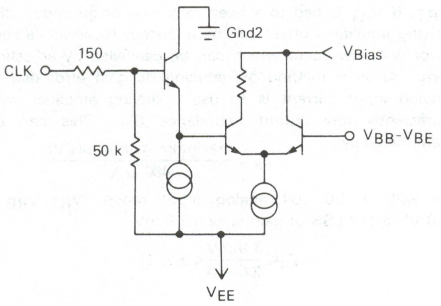
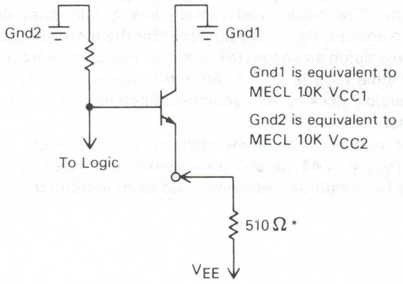

Gnd2
V_{Bias}
150
CLK
50 k
$V_{BB}-V_{BE}$
V_{EE}

FIGURE 5 — DIGITAL OUTPUTS ARE STANDARD MECL 10K WITH EMITTER FOLLOWERS CAPABLE OF SOURCING 25 mA. EXTERNAL PULL-DOWN RESISTORS ARE REQUIRED ON ALL OUTPUTS.


Gnd2
Gnd1
Gnd1 is equivalent to MECL 10K V_{CC1}
Gnd2 is equivalent to MECL 10K V_{CC2}
To Logic
510 Ω *
V_{EE}

*Recommended value of external pull-down resistors for all outputs.

FIGURE 6 — OUTPUT CODING FOR THE MC10315L/MC10317L DEVICES*

Comparator Step	Analog Input Range (15.6 mV per LSB)			MC10315L	MC10317L	Overrange	$\overline{\text{Overrange}}$
	−2.0 V to 0 V	0 V to 2.0 V	±1.0 V	Data Bits (D0-D6)	Data Bits (D0-D6)	Bit (OVR)	Bit $(\overline{\text{OVR}})$
000	- 2.0000 V	+ 0.0000 V	- 1.0000 V	0000000	0000000	0	1
001	- 1.9922 V	+ 0.0078 V	- 0.9922 V	0000001	0000001	0	1
•	•	•	•	•	•	↓	↓
•	•	•	•	•	•	↓	↓
•	•	•	•	•	•	↓	↓
063	- 1.0234 V	+ 0.9766 V	0.0234 V	0111111	0111111	↓	↓
064	- 1.0078 V	+ 0.9922 V	0.0078 V	1000000	1000000	↓	↓
065	- 0.9922 V	+ 1.0078 V	+ 0.0078 V	1000001	1000001	↓	↓
•	•	•	•	•	•	↓	↓
•	•	•	•	•	•	↓	↓
•	•	•	•	•	•	↓	↓
126	- 0.0391 V	+ 1.9609 V	+ 0.9609 V	1111110	1111110	↓	↓
127	- 0.0234 V	+ 1.9766 V	+ 0.9766 V	1111111	1111111	↓	↓
128	- 0.0078 V	+ 1.9922 V	+ 0.9922 V	1111111	0000000	1	0

*The MC10315L and MC10317L differ only in output coding at comparator step 128 where the device is overranged.

CIRCUIT DESCRIPTION

Conversion Timing

The MC10315L/MC10317L performs a conversion and outputs data within a single clock cycle. Referring to Figure 1 will indicate that the clock input is sensitive to the rising and falling clock edges. All significant operations are referenced to the edges. A rising clock edge holds the analog input by latching the (128) input comparators. The output latches are also released to toggle and update to the new digital value. The falling edge of the clock will latch the data outputs. Clock timing must be considered to ensure a valid conversion. With the rising edge of the clock, there will be an aperture delay (t_{ad}) which is the time from the threshold of the (50%) edge to the actual time the input comparators latch in the analog value of A_{in}. The data valid delay time (t_{vd}) is the time interval for valid data to appear at the outputs. t_{vd} is 43 ns from the rising clock edge. After this time, the clock can go low to latch the valid data at the outputs. The clock must remain low a minimum time before another rising edge in order for the input comparators to unlatch and begin to track. This comparator tracking delay time (t_{cd}) is 25 ns. After this minimum time, the conversion clock cycle is repeated, latching in a new analog input value.

The minimum recommended clock pulse width high time (t_{pwH}) is 44 ns and pulse width low time (t_{pwL}) is 25 ns for maximum recommended sample frequency (fs). Rise (t_r) and fall (t_f) time of the clock edges should be in the range from 2.0 to 7.0 ns to minimize the chance of clocking errors or uncertainty.

Analog Input (A_{in})

The dc current drive required by the analog input (A_{in}) is a function of the input voltage (V_{in}) and is directly attributable to the accumulation of input bias currents for each of the 128 comparators. When $V_{in} \leqslant V_{RB}$, the dc current is zero and when $V_{in} \geqslant V_{RT}$ the current is a maximum of 400 µA. Looking at this current as a function of V_{in} on a large signal basis, it will appear as a straight line approximation.

This input current loading on a driving source impedance can produce a dc gain error. Cancellation of this error is accomplished by utilizing an adjustable voltage reference at V_{RT}. If V_{RT} is tied to a fixed reference or grounded, the driving amplifiers offset can be adjusted. However, a zero error will now occur which can be cancelled by adjusting V_{RB}. Another method of reducing dc gain error due to analog input current is to use a driving amplifier with sufficiently low output impedance (Z_s). This can be determined by:

$$Z_s \leqslant \frac{\text{maximum gain error (V)}}{400\ \mu\text{A}}$$

i.e.,with a 1.0 volt analog input range (V_{RT}-V_{RB} = 1.0 V), a 1/2 LSB of gain error = 3.9 mV

$$Z_s \leqslant \frac{3.9\ \text{mV}}{400\ \mu\text{A}} \leqslant 9.76\ \Omega$$

Analog Input (A_{in}) (Continued)

The input capacitance (C_{in}) is also a function of input voltage (V_{in}). For $V_{in} \leqslant V_{RB}$, $C_{in} \simeq 40$ pF; $V_{in} \geqslant V_{RT}$, $C_{in} \simeq 70$ pF. The input capacitance on a large signal basis over the analog input range is a linear function. C_{in} can limit the analog input bandwidth if the driving source impedance is too great. This can introduce an ac gain error if the corner frequency f_c is not sufficiently extended from maximum input frequency (f_{in}).

For example, to keep the ac gain error to within 1/2 LSB of 7-bits, the corner frequency (f_c) of the effective single pole, low-pass filter created by the driving source impedance (Z_S) and the input capacitance (C_{in}) should be: $f_c \geqslant 11.3\ f_{in}$

C_{in} - analog input capacitance.
f_{in} - maximum input frequency of A_{in}
f_c - corner frequency determined by C_{in} and Z_S
n - number of bits
Z_S - driving source impedance of the analog input

For single Pole Filter:
$$\frac{f_c}{f_{in}} \geqslant \frac{1}{\sqrt{\dfrac{1}{\left(\dfrac{2^{n+1}-1}{2^{n+1}}\right)^2} - 1}}$$

If measures have already been taken to keep dc gain error to within 3.9 mV (1/2 LSB for 1.0 V full scale) by providing a low Z_S as described earlier, the calculated $Z_S \leqslant 9.76\ \Omega$ will sufficiently extend the corner frequency of the input pole to $\simeq 233$ MHz.

Figure 2 illustrates the equivalent analog input in terms of an effective variable C_{in} and R_{in}.

Reference Inputs

As shown in Figure 3, a resistive (divider) ladder comprised of 128 matched resistors with a nominal value of 0.5 Ω each, provides a reference voltage to each of the 128 comparator inputs. Recommended range of reference voltage applied across the resistive ladder (V_{RT} to V_{RB}) is 1.0 volt to 2.0 volts. V_{RT} must be kept more positive than V_{RB}. V_{RT} must not exceed +2.5 volts above Gnd2 and V_{RB} must not become more negative than −2.5 volts below Gnd2. With 2.0 volts across the reference ladder (V_{RT}-V_{RB} = 2.0 V), the ladder network has a common-mode range capability about Gnd2, permitting analog input (A_{in}) ranging options such as ± 1.0 volt, 0 to - 2.0 volts and 0 to 2.0 volts. A minimum of 1.0 volt should be maintained across the ladder network to ensure linearity to 7-bits. Less than 1.0 volt will degrade linearity due to comparator offsets becoming a significant factor.

Additional taps on the reference ladder are pinned out, providing access to the middle (V_{RM}), 1/4 (V_{RB}ac) and 3/4 (V_{RT}ac) scale points. V_{RM} can be left open, but if ladder linearity adjustment is required, an appropriate reference voltage can be applied. The V_{RB}ac and V_{RT}ac pins are intended for ac bypassing if ladder noise presents a problem. Reference voltages can be applied to these pins if tighter ladder linearity is desired. If the reference ladder voltage is to be varied dynamically such as in an AGC application, ac bypassing of any of the reference taps would likely yield undesirable results.

Calibration is accomplished by adjusting V_{RB} and V_{RT} to set the first and 127th comparator thresholds to the desired voltages. If a 0 to −1.0 V input (A_{in}) range is desired, continuously strobe the convertor with −0.9961 V on the analog input, adjust V_{RB} for output toggling between codes 0000000 and 0000001. Then apply $A_{in} = -0.0117$ V and adjust V_{RT} for toggling between 1111110 and 1111111 (thresholds 126th and 127th). Rather than adjusting V_{RT}, it may be more convenient to connect V_{RT} to Gnd2 and adjust the driving amplifier offset control. V_{RB} can again be used as a gain adjust point to cancel the effects of using the offset control technique.

Application Information

8-bits of resolution and accuracy can be obtained by stacking two 7-bit converters and wire ORing the data outputs. Shown in Figure 7 is an MC10315L and MC10317L in an 8-bit A/D configuration. The circuit is quite straightforward with the analog input (A_{in}) for each converter tied together, forming a common input. The analog input range is negative unipolar with V_{RT} of the MC10315L grounded (Gnd2) or referenced very near ground. V_{RB} of the MC10315L is connected to V_{RT} of the MC10317L and referenced to $V_{REF}/2$ to ensure this node is midscale. Unit to unit variations in Reference Ladder Resistance of each device can shift this point if a reference is not used, causing linearity errors. Care should be taken when interconnecting V_{RB} and V_{RT} of the MC10315L and MC10317L respectively. Reference ladder current flowing through resistance of printed circuit board runs, sockets and even device pins and bonding wires can establish significant IR drops of several millivolts causing differential non-linearity errors at midscale. A negative reference of -2.000 V is applied to V_{RB} of the MC10317L. The remaining pins V_{RT}ac, V_{RB}ac and V_{RM} for both devices can be left open or be connected to additional external references if linearity improvements are required. V_{RT}ac and V_{RB}ac can also be used as ac decoupling points for the resistor ladders to reduce any transients which may exist due to current noise.

The clock (CLK) inputs are driven by a common clock. Depending on the input frequency to be encoded, it may be necessary to skew the rising clock edges to one of the devices to compensate for a slight difference in aperture delay time (t_{ad}) which may occur between the two devices.

Application Information (Continued)

The digital outputs, D0 through D6 are wire ORed. The overrange (OVR) bit of the MC10317L becomes the MSB for the 8-bit word in Binary coding.

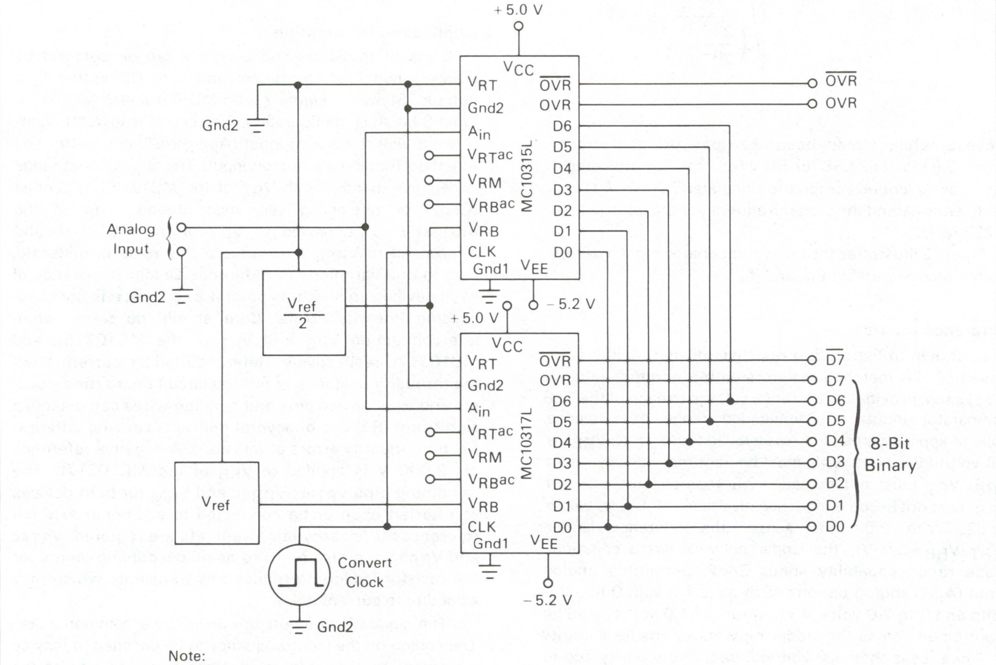
The MC10315L and MC10317L differ only in the method of overranging (see Figure 6, output coding truth table). When the MC10317L input (A_{in}) is overranged, the overrange (OVR) bit goes high, all other bits (D0-D6) go low. This enables direct wire ORing of additional A/D outputs to expand to ≥8-bits. When the MC10315L is overranged, OVR goes high and the data bits (D0-D6) remain high. This device provides a true termination of a digital word when the system becomes overranged. Generally the MC10315L will be used in a 7-bit, stand-alone converter scheme, or as the upper scale A/D when stacking two or more devices to expand to ≥7-bits.

Pull-down resistors are required at the digital outputs. A recommended value of 510 Ω will provide proper output fall times in most applications and also hold down device power dissipation. The outputs are capable of sustaining MECL levels when terminated with a 50 Ω (to −2.0 V) characteristic load impedance to minimize reflections. Design rules for MECL 10K should be followed when using these devices.

Care must be taken in PC board ground layout to prevent digital ground currents from flowing through the analog ground. Separate grounds are provided on the MC10315L/MC10317L to help isolate the digital noise from the analog section of a system. Gnd1 is internally connected to only the collectors of the output emitter followers as shown in Figure 5. This provides a separate path for current transients of the switched output loads. All other internal circuitry is referenced to Gnd2.

Low and high frequency power supply bypassing should be provided physically close to the device, with V_{CC} and V_{EE} bypassed to Gnd2.

FIGURE 7 — CIRCUIT CONFIGURATION UTILIZING A MC10315L AND MC10317L A/D TO PERFORM A HIGH SPEED, 8-BIT CONVERSION



Note:
Required pull-down resistors at the digital outputs are not shown. All digital outputs should be treated according to MECL 10K design rules.

MOTOROLA

MC10318L9
MC10318L
MC10318CL7
MC10318CL6

Specifications and Applications Information

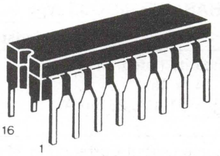
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

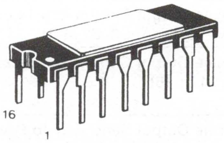
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

The MC10318 (Series) is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 Series is available in 4 accuracy grades (over temperature) to meet the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilliscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

- FAST Settling Time — 10 ns (Typ to ±0.19%)
- Four Accuracy Grades
  - 9-Bit Linearity (±0.10%) — MC10318L9
  - 8-Bit Linearity (±0.19%) — MC10318L
  - 7-Bit Linearity (±0.39%) — MC10318CL7
  - 6-Bit Linearity (±0.78%) — MC10318CL6
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: −1.3 V to +2.5 V
- Single MECL Supply: −5.2 V
- Standard 16-Pin Dual-In-Line Package

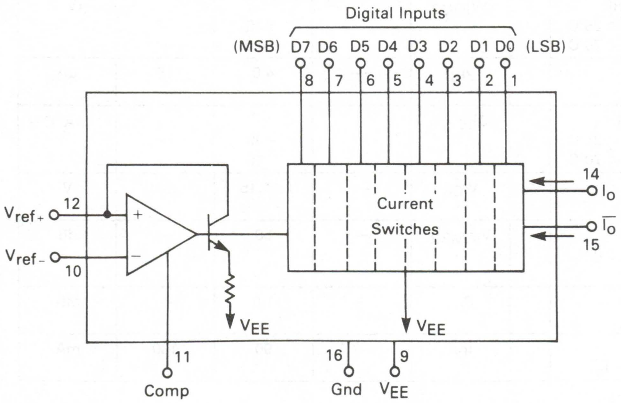


CL SUFFIX
CERAMIC PACKAGE
CASE 620-02



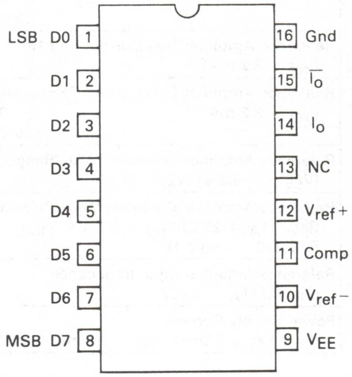
L SUFFIX
CERAMIC PACKAGE
CASE 690-13

BLOCK DIAGRAM


Digital Inputs
(MSB) D7 D6 D5 D4 D3 D2 D1 D0 (LSB)
8 7 6 5 4 3 2 1
V_{ref+} 12
V_{ref-} 10
+
−
Current Switches
14 I_o
$\overline{I_o}$ 15
V_{EE}
V_{EE}
11 Comp
16 Gnd
9 V_{EE}

PIN CONNECTIONS

(TOP VIEW)


LSB D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
MSB D7 8
16 Gnd
15 $\overline{I_o}$
14 I_o
13 NC
12 V_{ref+}
11 Comp
10 V_{ref-}
9 V_{EE}

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	−6.0 to +0.5	Vdc
Digital Input Voltage	V_I	0 to V_{EE}	Vdc
Applied Output Voltage	V_O	+5.0 to V_{EE}	Vdc
Reference Current	$I_{ref}(12)$	5.0	mA
Output Current	I_{FS}	−75	mA
Reference Amplifier Input Range	V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{ref(D)}$	±5.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Ceramic Package	T_J	+175	°C
Thermal Resistance, Junction to Ambient Still Air With 500 LFPM	$R\theta_{JA}$	80 50	°C/W

DC CHARACTERISTICS (V_{EE} = −5.2 V, ±5% T_A = 0°C to +70°C after thermal equilibrium is reached.)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Nonlinearity (Integral) (Pin 14 or 15) (@ I_{FS} = 51 mA, 25.5 mA) MC10318L9 MC10318L MC10318CL7 MC10318CL6		— — — —	— — — —	— — — —	±0.10 ±0.19 ±0.39 ±0.78	% FS
Zero Scale Output Current (Pin 14 or 15) (T_A = 25°C)	10	I_{ZS}	—	5.0	50	μA
Zero Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$I_{ZS}/\Delta T$	— —	±17 ±2.0	— —	nA/°C
Full Scale Output Current (Pin 14 or 15) (I_{ref} = 3.2 mA, D0–D7 = 1)	10	I_{FS}	−46.00	−51.00	−56.00	mA
Full Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{FS}/°C$	— —	±50 ±10	— —	ppm/°C
Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) (−4.94 V < V_{EE} < −5.46 V) MC10318L,9 MC10318CL6,7		I_{FSPSS}	— —	±0.005 ±0.005	±0.02 ±0.04	%/%
Full Scale Symmetry ($I_{FS} — \overline{I_{FS}}$)	10	I_{FSS}	—	±21	±100	μA
Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ ½ LSB (Specified Nonlinearity) (T_A = 25°C)		V_{OC}	−1.3	—	+2.5	V
Output Resistance (Pin 14 or 15) (T_A = 25°C)	12	R_O	—	69	—	kΩ
Reference Amplifier Offset Voltage (T_A = 25°C)		V_{IO}	—	±3.2	—	mV
Reference Amplifier Offset Voltage Temperature Drift 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta V_{IO}/\Delta T$	— —	±10 ±4.0	— —	μV/°C
Reference Amplifier Bias Current (Pin 10) (I_{ref} = 3.2 mA)		I_{IB}	—	4.0	15	μA
Reference Amplifier Bias Current Temperature Drift (I_{ref} = 3.2 mA) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{IB}/\Delta T$	— —	−40 −10	— —	nA/°C
Reference Amplifier Common Mode Range (V_{EE} = −5.2 V) (T_A = 25°C)		V_{ICR}	—	±1.15	—	V
Reference Amplifier Common Mode Rejection Ratio (T_A = 25°C) (I_{ref} = 3.2 mA, V_{ICR} = 0 to −2.0 V, Pins 1–8 = Logic 1)		V_{ICMRR}	—	58	—	dB
Reference Amplifier Input Impedance (Pin 10) (T_A = 25°C)		R_{IN}	—	1.0	—	MΩ
Power Supply Current (Pins 1 thru 8 Open, I_{ref} = 3.2 mA, Includes $I_o + \overline{I_o}$)		I_{EE}	—	90	130	mA

AC CHARACTERISTICS (T_A = 25°C, V_{EE} = −5.2 V, ±5%)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Feedthrough Current — All Bits Off	9	I_{FC}				μA p-p
f = 10 kHz			—	2.0	—	
f = 100 kHz			—	18	—	
Distortion — (@ I_O) (Sinewave applied to reference amplifier Input, D0–D7 = Logic 1)						%
C = 0.01 μF, f = 20 kHz		THD	—	1.0	—	
C = 0.01 μF, f = 65 kHz		THD	—	5.0	—	
C = 0.001 μF, f = 340 kHz		THD	—	1.0	—	
C = 0.001 μF, f = 600 kHz		THD	—	2.0	—	
C = 240 pF, f = 600 kHz		THD	—	0.8	—	
Reference Amplifier Slew Rate (Step change at Pin 10, all bits on)	13					mA/μs
C = 0.01 μF			—	0.5	—	
C = 0.001 μF			—	5.0	—	
C = 240 pF			—	20	—	
Settling Time (to ±0.19% of Full Scale)	1,22	t_s				ns
1 LSB Change			—	7.0	—	
All Bits Switched			—	10	—	
Propagation Delay	2	t_p	—	5.0	—	ns
Output Glitch Energy (with De-Skewing Capacitors) (Input Change: 01111111 ⟷ 10000000)			—	50	—	LSB·ns
Glitch Duration			—	5.0	—	ns

DIGITAL INPUT VOLTAGE LEVELS				
Volts (See Note)				
T_A	V_{IH}max	V_{IHA}min	V_{ILA}max	V_{IL}min
0°C	−0.845	−1.151	−1.516	−1.868
25°C	−0.810	−1.105	−1.505	−1.850
70°C	−0.727	−1.052	−1.480	−1.830

FUNCTIONAL PIN DESCRIPTION

D0–D7 (Pins 1-8) The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally −1.8 V, and Logic "1" is nominally −0.9 V.

V_{ref-} (Pin 10) The high impendance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to V_{EE} +2.9 V (nominally −2.3 V).

V_{ref+} (Pin 12) The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

Comp. (Pin 11) A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

I_O, $\overline{I_O}$ (Pins 14,15) The complementary current outputs. Current flow is into the DAC and varies linearily with I_{ref} and the digital input code. I_{out} increases as the digital input increases. Output compliance range is −1.3 V to +2.5 V.

V_{EE} (Pin 9) The power supply pin. V_{EE} is nominal −5.2 V, ±5%.

Gnd (Pin 16) The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: V_{EE} = −5.2 V, ±5% Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig. 19 in this data sheet.

FIGURE 1 — SETTLING TIME

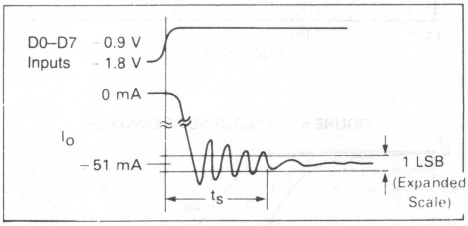
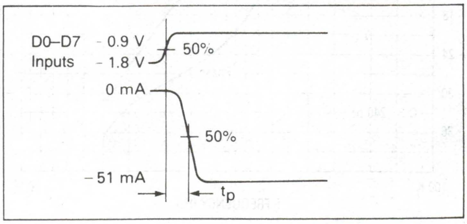


FIGURE 2 — PROPAGATION DELAY



REFERENCE AMPLIFIER RESPONSE

Inverting Input (V_{ref-})
Test Circuit of Fig. 14

Noninverting Input (V_{ref+})
Test Circuit of Fig. 11

FIGURE 3 — FREQUENCY RESPONSE

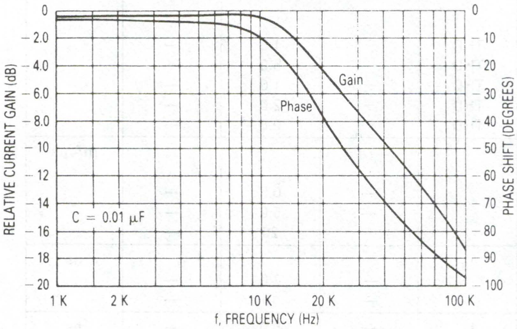


FIGURE 6 — FREQUENCY RESPONSE

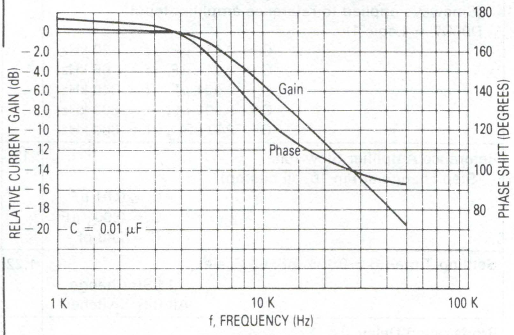


FIGURE 4 — FREQUENCY RESPONSE

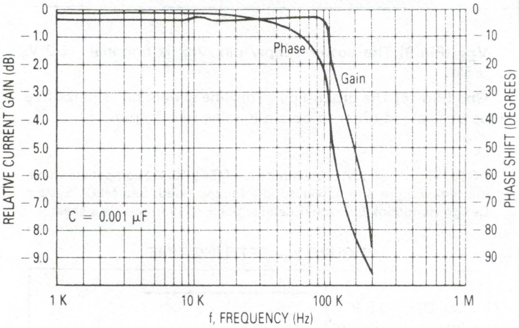


FIGURE 7 — FREQUENCY RESPONSE

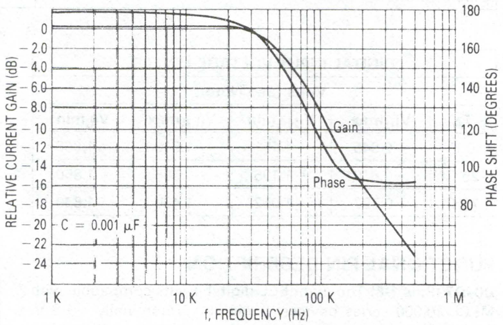


FIGURE 5 — FREQUENCY RESPONSE

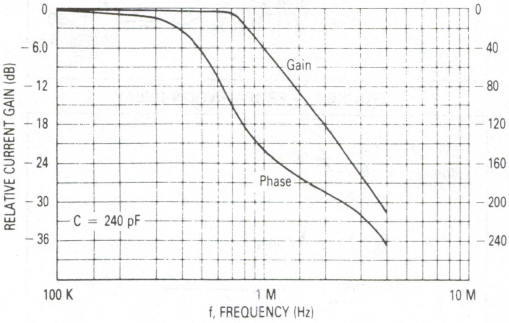
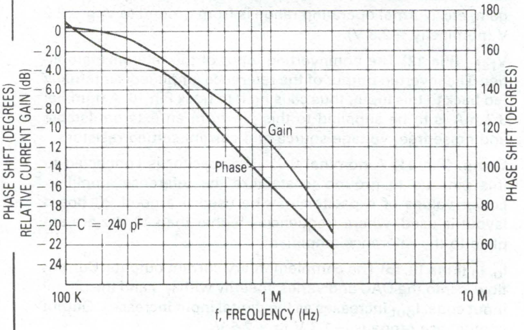
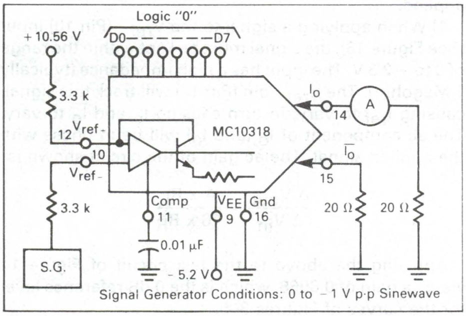


FIGURE 8 — FREQUENCY RESPONSE



TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT


Logic "0"
+10.56 V
D0———————D7
3.3 k
Vref+
12
10
Vref-
MC10318
Io
14
A
Io
15
3.3 k
Comp
11
VEE
9
Gnd
16
20 Ω
20 Ω
0.01 µF
S.G.
-5.2 V

Signal Generator Conditions: 0 to −1 V p-p Sinewave

FIGURE 10 — ZERO/FULL SCALE CURRENT

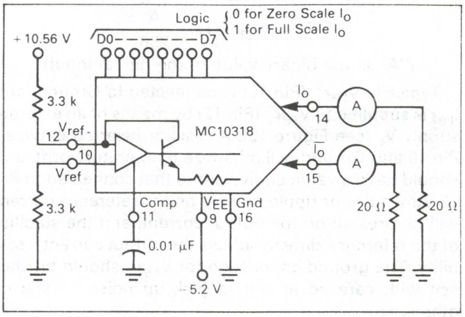
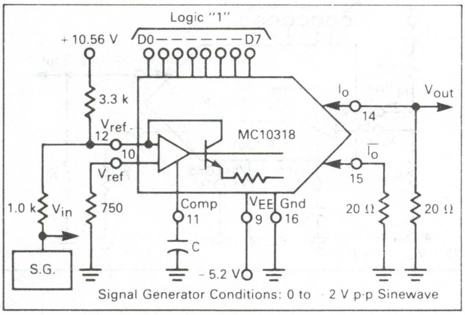

Logic
0 for Zero Scale Io
1 for Full Scale Io
+10.56 V
D0———————D7
3.3 k
Vref+
12
10
Vref-
MC10318
Io
14
A
Io
15
A
3.3 k
Comp
11
VEE
9
Gnd
16
20 Ω
20 Ω
0.01 µF
-5.2 V

FIGURE 11 — GAIN/PHASE MEASUREMENT

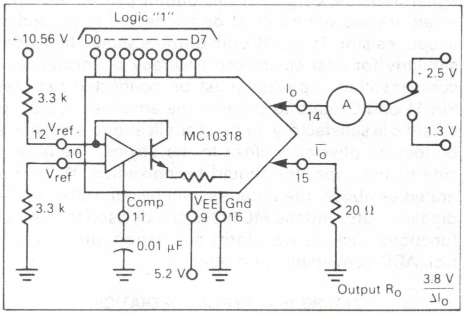

Logic "1"
+10.56 V
D0———————D7
3.3 k
Vref+
12
10
Vref-
MC10318
Io
14
Vout
Io
15
1.0 k
Vin
750
Comp
11
VEE
9
Gnd
16
20 Ω
20 Ω
C
S.G.
-5.2 V

Signal Generator Conditions: 0 to −2 V p-p Sinewave

Reference dB Level: See Text

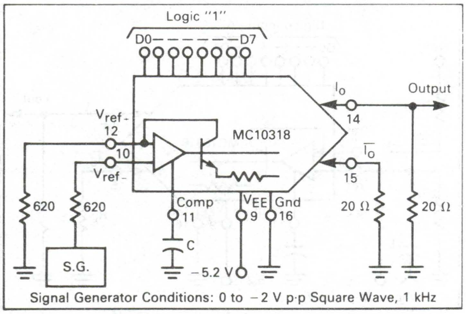
See Figures 6–8

FIGURE 12 — OUTPUT RESISTANCE


Logic "1"
+10.56 V
D0———————D7
3.3 k
Vref+
12
10
Vref-
MC10318
Io
14
A
-2.5 V
1.3 V
Io
15
3.3 k
Comp
11
VEE
9
Gnd
16
20 Ω
0.01 µF
-5.2 V

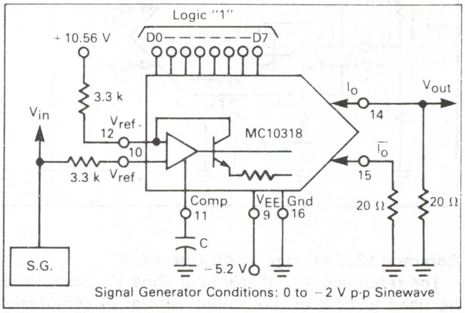
$\text{Output } R_O = \frac{3.8 \text{ V}}{\Delta I_O}$

FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE


Logic "1"
D0———————D7
Vref+
12
10
Vref-
MC10318
Io
14
Output
Io
15
620
620
Comp
11
VEE
9
Gnd
16
20 Ω
20 Ω
C
S.G.
-5.2 V

Signal Generator Conditions: 0 to −2 V p-p Square Wave, 1 kHz

FIGURE 14 — GAIN/PHASE MEASUREMENT


Logic "1"
+10.56 V
D0———————D7
3.3 k
Vin
Vref+
12
10
3.3 k
Vref-
MC10318
Io
14
Vout
Io
15
Comp
11
VEE
9
Gnd
16
20 Ω
20 Ω
C
S.G.
-5.2 V

Signal Generator Conditions: 0 to −2 V p-p Sinewave

Reference dB Level: See Text.

See Figures 3–5

OPERATIONAL INFORMATION

Typical DAC Operation

The MC10318 is designed to be operated with an I_{ref} (Pin 12) of 3.2 mA, resulting in a full scale output current (I_O) of 51 mA when D0 through D7 are at a Logical "1" (−0.9 V). The transfer equation for I_O is therefore:

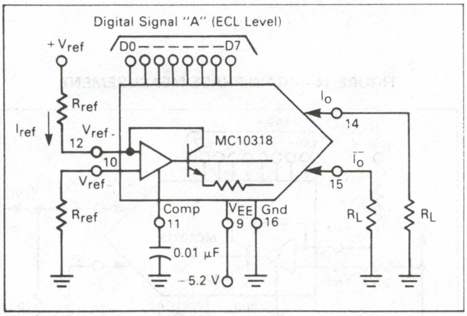
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically V_{ref-} (Pin 10) is connected to Ground, and I_{ref} is supplied to V_{ref+} (Pin 12) by means of an external supply V_r (see Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for V_{ref-} should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs (I_O and $\overline{I_O}$) are high impedance current sources having a compliance range of 3.8 V (−1.3 to +2.5 V). I_O increases with increasing digital input, while $\overline{I_O}$ decreases. Their sum is a constant equal to 15.94 x I_{ref}. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A 0.01 μF ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION


Digital Signal "A" (ECL Level)
+Vref
D0 — — — — — — D7
Rref
Iref
Vref+
12
10
Vref-
MC10318
Io
14
Īo
15
Rref
Comp
11
0.01 μF
VEE
9
Gnd
16
−5.2 V
RL
RL

Common Mode Range — AC Operation

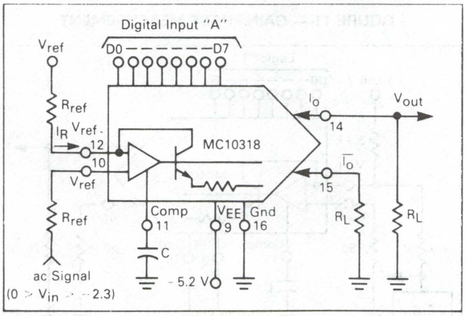
The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the V_{ref-} (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to −2.3 V. The input has a high impedance (typically 1 Megohm). The V_{ref+} pin (Pin 12) will track this signal, causing I_{ref} to vary, in turn causing I_O and $\overline{I_O}$ to vary. The ac component of I_O (and $\overline{I_O}$) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

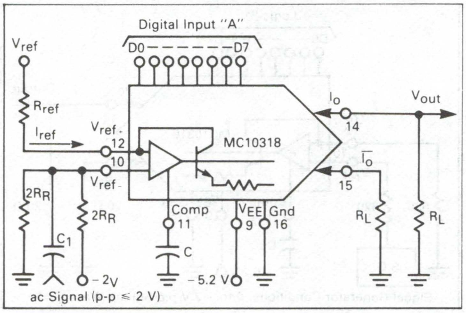
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3–5.

FIGURE 16 — AC OPERATION, NONINVERTING


Digital Input "A"
Vref
D0 — — — — — — D7
Rref
IR
Vref+
12
10
Vref-
MC10318
Io
14
Vout
Īo
15
Rref
Comp
11
C
VEE
9
Gnd
16
−5.2 V
RL
RL
ac Signal
(0 ≥ Vin ≥ −2.3)

If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)


Digital Input "A"
Vref
D0 — — — — — — D7
Rref
Iref
Vref+
12
10
Vref-
MC10318
Io
14
Vout
Īo
15
2RR
2RR
C1
−2V
Comp
11
C
VEE
9
Gnd
16
−5.2 V
RL
RL
ac Signal (p-p ≤ 2 V)

The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3–5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the V_{ref+} (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by V_{ref}. Pin 12 is a virtual ground, and therefore the current I_{ref} is equal to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} + \frac{V_i}{R_i}$$

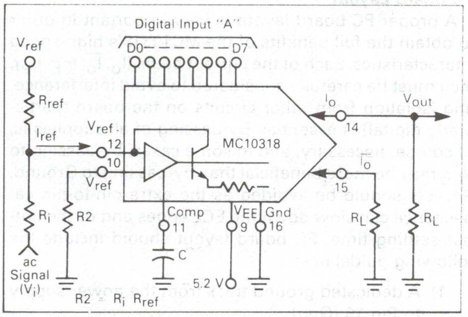
I_o and $\overline{I_o}$ will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of −0.3188, which is the 0 dB reference level for the curves of Figures 6–8.

The reference current I_{ref} must always flow **into** Pin 12, requiring that the values of V_{ref}, R_{ref}, R_i, and V_i be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING

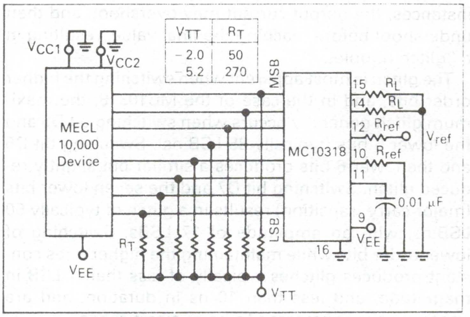

Digital Input "A"
V_ref
D0 — — — — — — D7
R_ref
I_ref
V_ref
12
10
MC10318
I_o
V_out
14
$\overline{I_o}$
15
V_ref
R_i
R2
Comp
11
C
V_EE
9
Gnd
16
R_L
R_L
ac Signal (V_i)
−5.2 V
R2 = R_i R_ref

The compensation capacitor (Pin 11) of Figure 18 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6–8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

DIGITAL INTERFACE

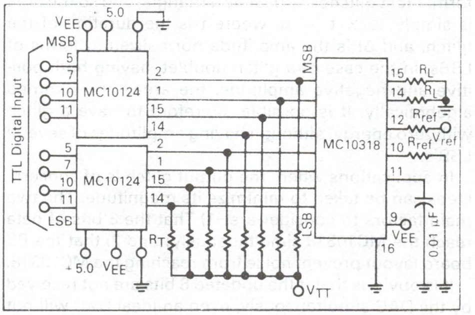
The digital inputs (Pins 1–8) are compatible with MECL 10,000 series devices over the temperature and V_{EE} range listed on page 3. Standard MECL 10,000 design guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of R_T and V_{TT} may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (−1.8 V), or a Logic 1 (−0.9 V). Resistors R_T should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE


V_TT
R_T
−2.0
50
−5.2
270
V_CC1
V_CC2
MECL 10,000 Device
MSB
LSB
MC10318
15
R_L
14
R_L
12
R_ref
V_ref
10
R_ref
11
0.01 μF
9
V_EE
16
R_T
V_EE
V_TT

Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (Figure 20).

FIGURE 20 — TTL INTERFACE


+5.0
V_EE
MSB
5
7
10
11
MC10124
2
1
15
14
5
7
10
11
MC10124
2
1
15
14
TTL Digital Input
LSB
R_T
+5.0
V_EE
V_TT
MSB
LSB
MC10318
15
R_L
14
R_L
12
R_ref
V_ref
10
R_ref
11
9
V_EE
16
0.01 μF

OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high-speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB·ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB·ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

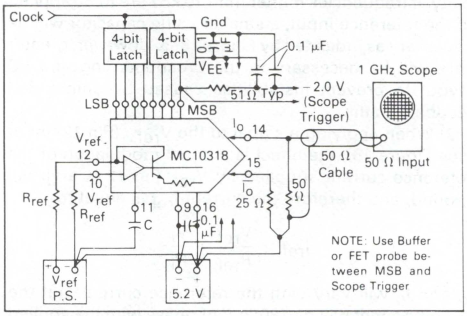
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits. See Fig. 31.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply $\frac{1}{2} \times t \times \Delta I$, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS



NOTE: Use Buffer or FET probe between MSB and Scope Trigger

Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 series will not differ from the **ideal** value by more than the specified nonlinearity.

PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths (I_o, $\overline{I_o}$, I_{EE}, I_{ref}, etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. By-passing of all supplies is, of course, necessary, and in some cases, by-passing to V_{EE} may be more beneficial than by-passing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

1) A dedicated ground track from the power supply to Pin 16 (Gnd);
2) A single dedicated ground track from the power supply to the **two** load resistors associated with I_o and $\overline{I_o}$ — this results in a constant dc current in this track;
3) A separate ground for the circuitry associated with V_{ref+}, V_{ref-}, and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
4) The compensation capacitor must be physically adjacent to Pin 11;
5) Bypass V_{EE} (Pin 9) with a 0.1 µF to the ground line feeding the load resistors;
6) Provide proper terminations at the inputs — the suggested values for R_T and V_{TT} will provide best speed response;

7) Bypass V_{TT} to V_{EE} **and** to Ground with 0.1 μF capacitors;
8) If the power supplies are not on the same PC board with the MC10318, bypass V_{EE} and V_{TT} to Ground with (minimum) 10 μF and 0.1 μF where the supply voltages enter the PC board;
9) Use of a ground plane is mandatory in all high speed applications;
10) Keep all TTL circuitry tracks separate from the MC10318 by means of ground tracks and/or ground planes.

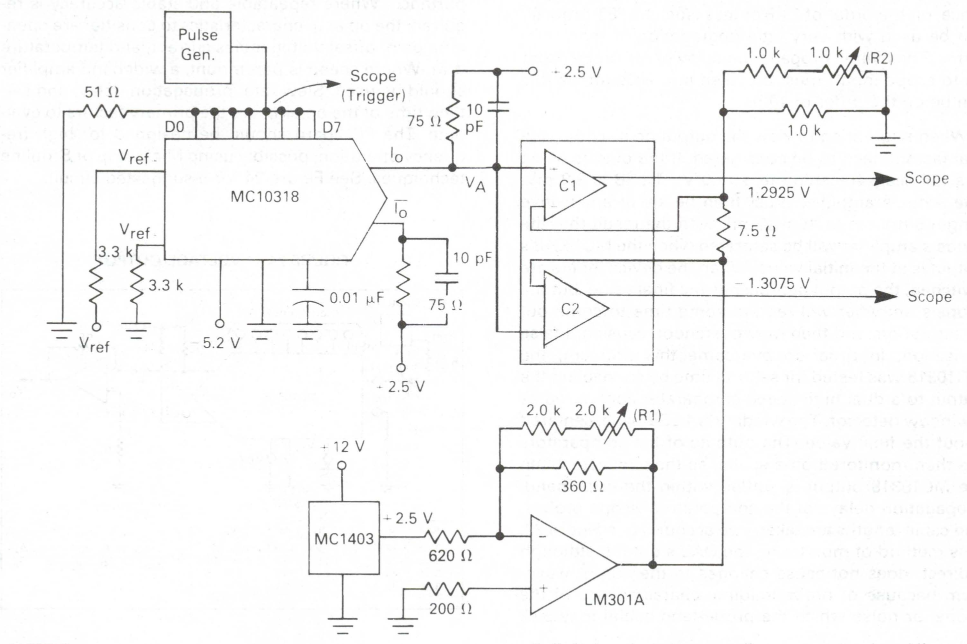
Many of the above points have to do with isolating the device from all other circuitry, since most applications involve using the MC10318 (which is 50% analog) in a (noisy) digital circuit. If the output voltage swing is typically 1 volt, then 1 LSB is approximately 4 mV. Since TTL circuitry can easily generate 50 mV noise on the ground line, the need for isolation is apparent.

The above points are not the only ones to be considered by the designer, as each application will have its own individual additional requirements.

Propagation Delay

The propagation delay is measured from the 50% point of the input transition to the 50% point of the output transition. Since the typical propagation delay is on the order of 5 ns, see Figure 21 and the information in Settling Time if this parameter is to be measured. Switching 1 LSB or all of the bits simultaneously produces no significant difference in propagation delay.

FIGURE 22 — SETTLING TIME MEASUREMENT



NOTES:
1) Pulse generator outputs −0.9 V to −1.8 V, t_r and t_f ≈ 2 ns.
2) Adjust v_{ref} for full scale output at $V_A = -1.3000$ V.
3) Adjust R1 for −1.3075 V at input of lower comparator.
4) Adjust R2 for −1.2925 V at input of upper comparator.
5) R1, R2 are 20 turn trimpots.
6) Keep all wiring as short, tidy as possible — isolate all digital and analog supplies, grounds, signal lines, etc.
7) Heavily bypass all supplies at each device, and reference (−) inputs to the comparators.
8) Comparators are high-speed devices, such as AM687ADL.
9) Account for comparator offset when setting reference values.

Settling Time

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into **and** stays within ±½LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate, and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

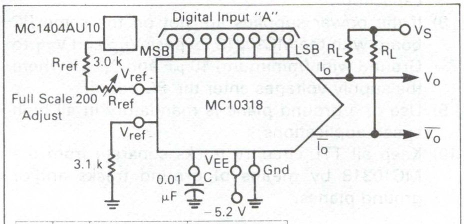
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

APPLICATIONS

Voltage Output

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

FIGURE 23 — VOLTAGE OUTPUT

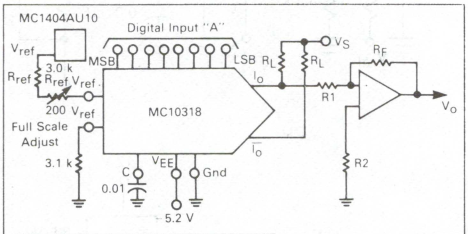


V_S	R_L	V_O	$\overline{V_O}$
0 V	25.5	0 to −1.3 V	−1.3 V to 0 V
+2.5	49	+2.5 to 0 V	0 to +2.5 V
+2.5	74.5	+2.5 to −1.3 V	−1.3 to +2.5 V
+1.0	39	+1.0 to −1.0 V	−1.0 to +1.0 V

$$V_O = \frac{V_{ref} \cdot A \times R_L}{R_{ref} \times 16} + V_S$$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

FIGURE 24 — VOLTAGE OUTPUT



R_{ref}	R_L	V_S	R1	R_F	V_O
3125	20	0	1.0 k	5.0 k	0 to −5
3125	20	0	1.0 k	10 k	0 to −10
3125	40	+1.02	2.0 k	10 k	5 to −5
3125	40	+1.02	2.0 k	20 k	10 to −10

$$V_O = \frac{V_{ref} \cdot A \cdot R_L \cdot R_F}{R_{ref} \cdot 16 \cdot (R1 + R_L)} - \frac{V_S \cdot R_F}{(R1 + R_L)}$$

Connecting I_O and $\overline{I_O}$ as shown in the above figures places a constant dc load (51 mA) on the V_S supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

WAVEFORM GENERATION

FIGURE 25 — SAWTOOTH GENERATOR

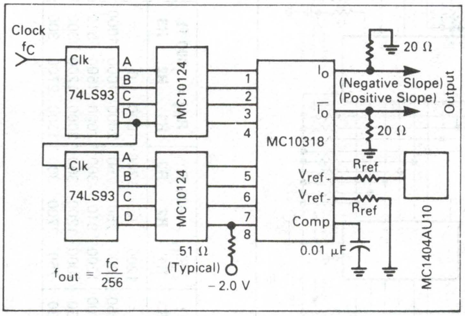

Clock
f_C
Clk
74LS93
A
B
C
D
MC10124
1
2
3
4
5
6
7
8
MC10318
I_o
$\overline{I_o}$
20 Ω
(Negative Slope)
(Positive Slope)
Output
20 Ω
V_{ref} -
V_{ref} -
R_{ref}
R_{ref}
Comp
0.01 µF
51 Ω
(Typical)
- 2.0 V
MC1404AU10
$f_{out} = \frac{f_C}{256}$

FIGURE 26 — TRIANGLE GENERATOR

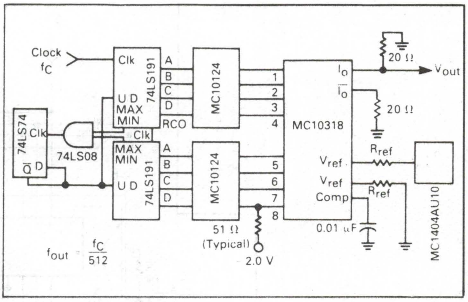
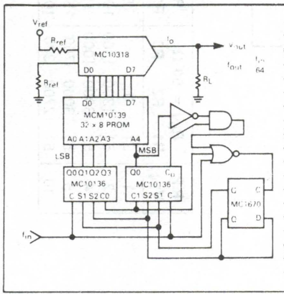

Clock
f_C
Clk
U D
MAX
MIN
74LS191
A
B
C
D
RCO
Clk
74LS74
$\overline{Q}$ D
74LS08
MC10124
1
2
3
4
5
6
7
8
MC10318
I_o
$\overline{I_o}$
20 Ω
20 Ω
V_{out}
R_{ref}
V_{ref} -
V_{ref}
Comp
R_{ref}
0.01 µF
51 Ω
(Typical)
- 2.0 V
MC1404AU10
$f_{out} = \frac{f_C}{512}$

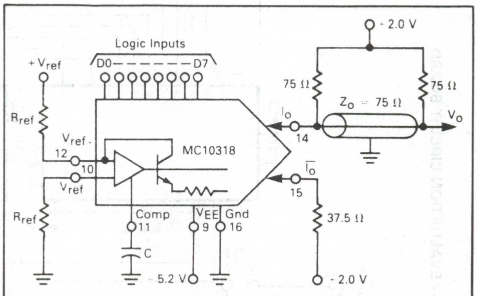
FIGURE 27 — SINEWAVE GENERATOR


V_{ref}
R_{ref}
MC10318
D0
D7
I_o
V_{out}
$f_{out} = \frac{f_{in}}{64}$
R_L
R_{ref}
MCM10139
32 × 8 PROM
A0 A1 A2 A3
A4
LSB
MSB
Q0 Q1 Q2 Q3
MC10136
C S1 S2 C0
Q0
MC10136
C1 S2 S1
MC1670
f_{in}

PROM CONTENTS

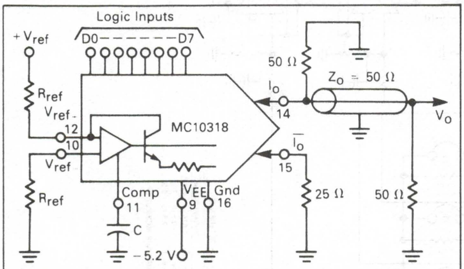
Address	Output	Address	Output
00	00	10	80
01	01	11	8C
02	03	12	98
03	06	13	A4
04	0A	14	B0
05	0F	15	BC
06	15	16	C6
07	1D	17	D0
08	25	18	DA
09	2F	19	E2
0A	39	1A	E9
0B	44	1B	F1
0C	4F	1C	F6
0D	5B	1D	FA
0E	67	1E	FD
0F	73	1F	FF

FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE


- 2.0 V
Logic Inputs
D0 — — — — — — D7
+ V_{ref}
R_{ref}
75 Ω
75 Ω
Z_O = 75 Ω
I_o
14
V_o
V_{ref} -
12
10
V_{ref}
MC10318
$\overline{I_o}$
15
Comp
11
V_{EE}
9
Gnd
16
C
- 5.2 V
R_{ref}
37.5 Ω
- 2.0 V

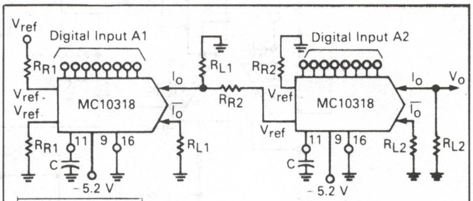
NOTE: Terminating Resistors and Z_O must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE


Logic Inputs
D0 — — — — — — D7
+ V_{ref}
R_{ref}
V_{ref} -
12
10
V_{ref}
MC10318
50 Ω
Z_O = 50 Ω
I_o
14
V_o
$\overline{I_o}$
15
25 Ω
50 Ω
R_{ref}
Comp
11
V_{EE}
9
Gnd
16
C
- 5.2 V

NOTE: Terminating Resistors and Z_O must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 30 — DIGITAL MULTIPLICATION


V_{ref}
Digital Input A1
R_{R1}
V_{ref} -
V_{ref}
MC10318
I_o
$\overline{I_o}$
R_{L1}
R_{R2}
R_{R2}
Digital Input A2
V_{ref}
V_{ref}
MC10318
I_o
$\overline{I_o}$
V_o
R_{R1}
11
9
16
C
- 5.2 V
R_{L1}
R_{L2}
R_{L2}

Suggested Values	
V_{ref}	+ 10 V
R_{R1}	3079*
R_{L1}	20
R_{R2}	330
R_{L2}	20

$$V_O = \frac{A1 \cdot A2 \cdot V_{ref} \cdot R_{L1} \cdot R_{L2}}{R_{R1} \cdot R_{R2} \cdot 256} = K \cdot A1 \cdot A2$$

(With suggested values, V_O range is 0 to - 1.0 V)

* 3.0 k Resistor + 100 Ω Trimpot

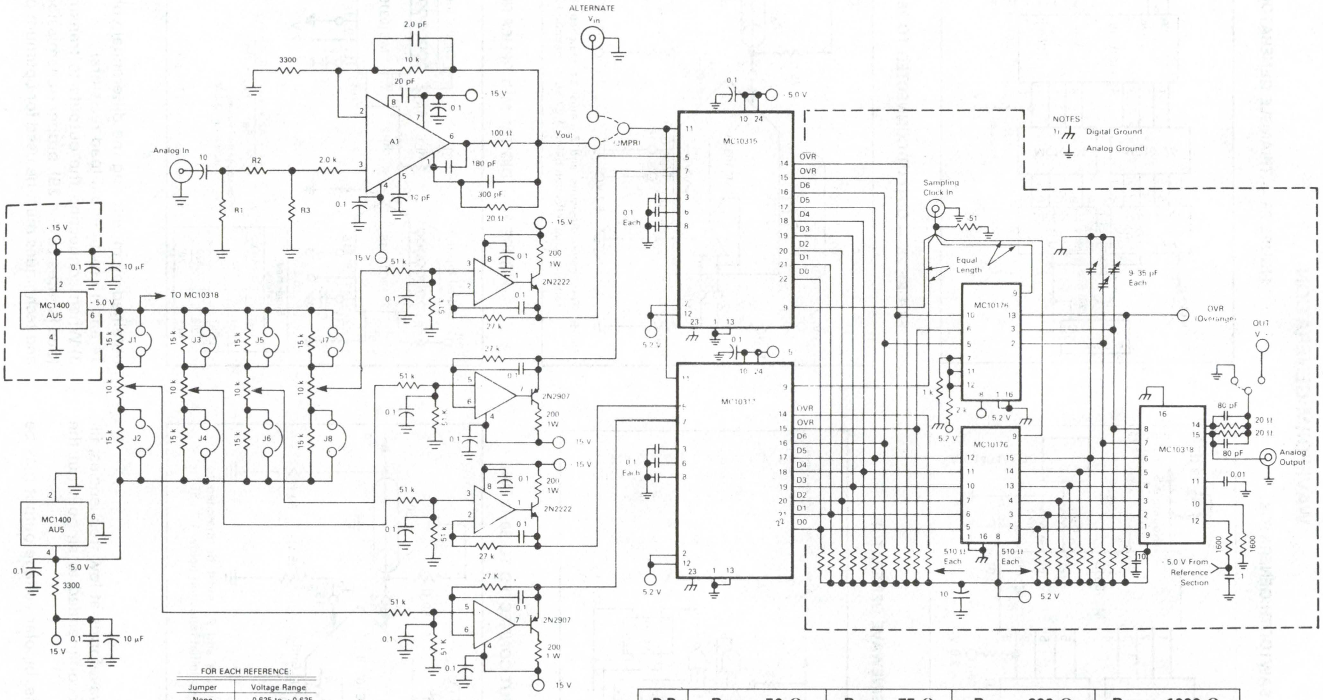
NOTES:

1) When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.

2) In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).

3) When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

FIGURE 31 — EVALUATION CIRCUIT BOARD


ALTERNATE V_in
Analog In
R1
R2
R3
A1
2.0 pF
3300
10 k
20 pF
−15 V
100 Ω
V_out
JUMPR
180 pF
300 pF
20 Ω
10 pF
MC1400 AU5
TO MC10318
−5.0 V
J1
J2
J3
J4
J5
J6
J7
J8
15 k
10 k
51 k
27 k
200 1W
2N2222
2N2907
15 V
MC10315
OVR
D6
D5
D4
D3
D2
D1
D0
0.1 Each
5.2 V
−5.0 V
Sampling Clock In
51
Equal Length
MC10176
9-35 pF Each
OVR (Overange)
OUT V−
NOTES
Digital Ground
Analog Ground
MC10318
80 pF
20 Ω
Analog Output
0.01
1600
−5.0 V From Reference Section
510 Ω Each
1 k
2 k

FOR EACH REFERENCE:

Jumper	Voltage Range
None	−0.625 to +0.625
Odd # Only	+0.5 to +2.5
Even # Only	−2.5 to −0.5

— OP AMPS ARE MC34002 BP

P.P	R_{IN} = 50 Ω			R_{IN} = 75 Ω			R_{IN} = 600 Ω			R_{IN} = 1000 Ω		
V_{IN}	R1	R2	R3	R1	R2	R3	R1	R2	R3	R1	R2	R3
1	51	0	∞	75	0	∞	1200	0	1200	1000	0	∞
2	51	1300	1300	100	150	150	1000	750	750	2000	1000	1000
4	51	3000	1000	91	300	100	1200	910	300	2000	1500	510
5	51	3000	750	150	120	30	1000	1200	300	3000	1200	300
10	51	2700	300	100	270	30	750	2700	300	1500	2700	300

EVALUATION BOARD FOR HIGH SPEED TESTING

Introduction

In order to facilitate evaluation of the MC10318 DAC, a PC board layout has been developed providing the appropriate signal levels and timing requirements. The board is designed to simultaneously evaluate the MC10315 and the MC10317 flash ADC's in conjunction with the MC10318 DAC, and the system is capable of passing video speed signals at sampling rates of up to 15 MHz. However, the MC10318 may be evaluated alone by installing only the appropriate components. The board may be purchased from Motorola (blank), or the user may make his own from the artwork shown on Figures 33 and 34.

Board Specifications

Power supply requirements: +15 V @ 100 mA.
−15 V @ 120 mA.
−5.2 V @ 550 mA.
+5.0 V @ 300 mA.

Sampling clock: $V_{IH} = -0.9$ V, $V_{IL} = -1.8$ V (ECL levels) terminated with 50 ohms, 15 MHz max.
Analog Input level: Selectable, see chart.
Analog Input Impedance: Selectable, see chart.
Output level: 0 to −1.0 V, user alterable.
Digital Input levels: (When ADC converters are not included) $V_{IH} = -0.9$ V, $V_{IL} = -1.8$ V (ECL levels).

Operation

The power supplies should be connected as shown in Figure 32. The leads should be short and direct.

The CLK Input (necessary if the ADC converters and or the latches are used) uses a BNC connector, and is terminated with 50 ohms to ground.

The Analog Input level (if the ADC converters are installed) depends on the input resistors selected (see chart). The output of the buffer amplifier should produce a maximum 4 V p-p signal, or an amplitude equal to the references (user adjustable).

The Analog Output is 0 to −1.0 V, corresponding to a digital input (to the MC10318) of FF and 00 respectively. Output impedance is normally 20 ohms, but may be varied by the user (see previous text).

Options

Input Signal — The p-p voltage level of the analog input signal (when using the ADC converters) is accommodated by selection of the input resistors from the chart (see schematic).

ALT IN — The analog signal may be applied directly to the ADC converters (by-passing the on-board amplifier) by applying the input signal to this connector, and relocating the jumper adjacent to the ALT IN connector. The signal source must be capable of driving 2.5 k ohms in parallel with approx. 140 pF.

V+ OUT — A pullup voltage (max. +2.5 V) may be applied to this connector in order to increase the output voltage swing. See the APPLICATIONS section of this data sheet. The 20 ohm load resistors may then be changed to other values. The jumper adjacent to the A OUT connector must be relocated.

Evaluating the MC10318 only — Only those components within the dotted line on the schematic are required. The digital inputs (ECL level) are to be applied to a connector strip located in pins 15–22 of the MC10317 position. +15 V and −5.2 V supplies are required. The latches transfer the information on the rising edge of the clock.

Video Testing

The above described printed circuit board has been tested, with a standard video test signal, for differential phase and differential gain (40 IRE sub-carrier on a 100 IRE ramp, sampled at 14.3 MHz) with results of 1% gain error and 2° phase error. The signal was obtained from a Tektronix 147A video test generator, applied to the ALT IN connector. The output (of the MC10318) was configured into a 75 ohm output impedance, and applied to a vector scope.

Tests conducted with the Evaluation Board in a video system (video camera and a TV monitor) showed no visible degradation of picture quality (at 8 bits resolution). The board provides an easy means of testing picture quality at reduced number of bits, or for conducting any test on a digitized video signal.

FIGURE 32 — COMPONENT LOCATION AND EXTERNAL CONNECTIONS

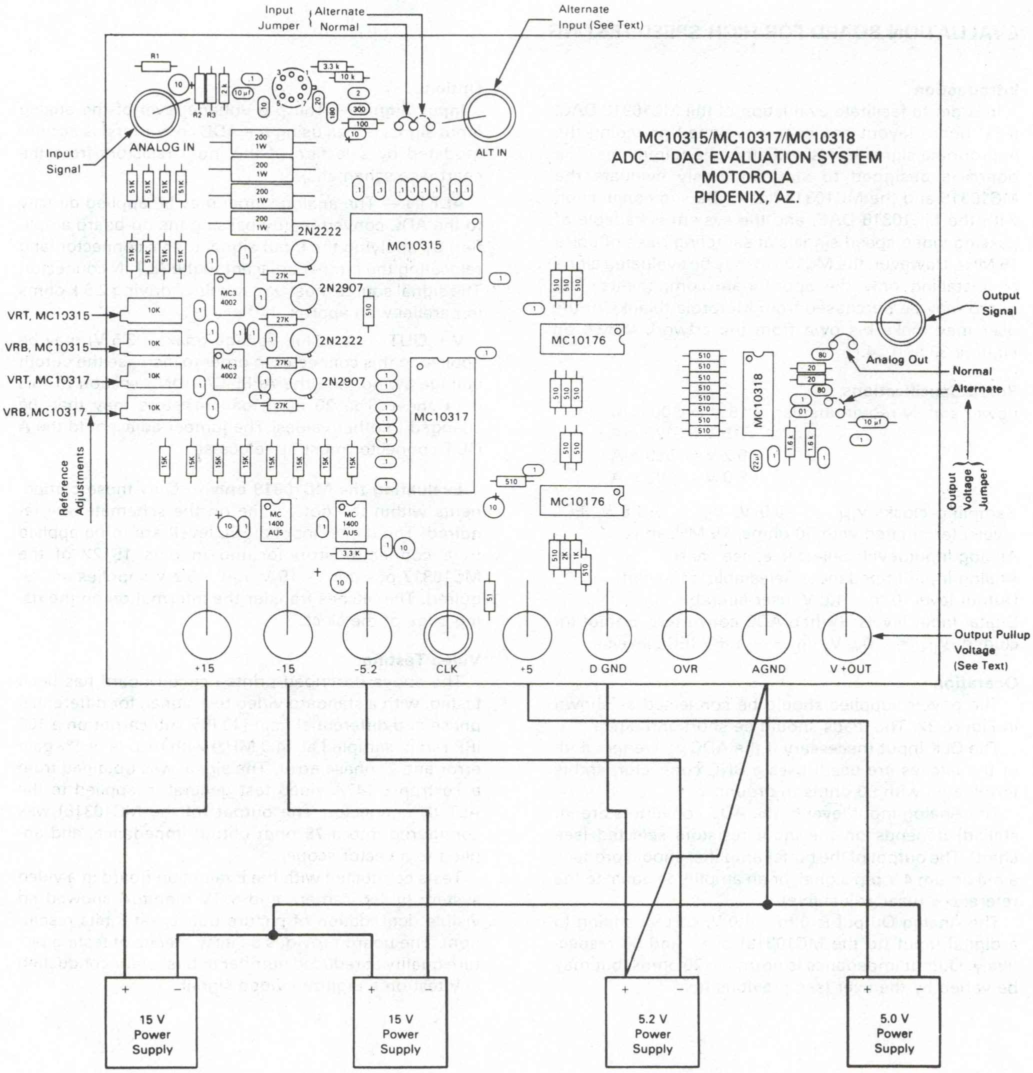

Input Jumper
Alternate
Normal
Alternate Input (See Text)
Input Signal
ANALOG IN
ALT IN
MC10315/MC10317/MC10318
ADC — DAC EVALUATION SYSTEM
MOTOROLA
PHOENIX, AZ.
R1
R2 R3
3.3 k
10 k
200 1W
51K
2N2222
2N2907
MC10315
MC10317
MC3 4002
27K
10K
15K
510
MC10176
MC10318
MC 1400 AU5
3.3K
1.6 k
VRT, MC10315
VRB, MC10315
VRT, MC10317
VRB, MC10317
Reference Adjustments
Output Signal
Analog Out
Normal
Alternate
Output Voltage Jumper
Output Pullup Voltage (See Text)
+15
-15
-5.2
CLK
+5
D GND
OVR
AGND
V +OUT
15 V Power Supply
15 V Power Supply
5.2 V Power Supply
5.0 V Power Supply

FIGURE 33 — COMPONENT SIDE ARTWORK (TOP)
(OVERALL SIZE = 6.00″ × 8.00″)

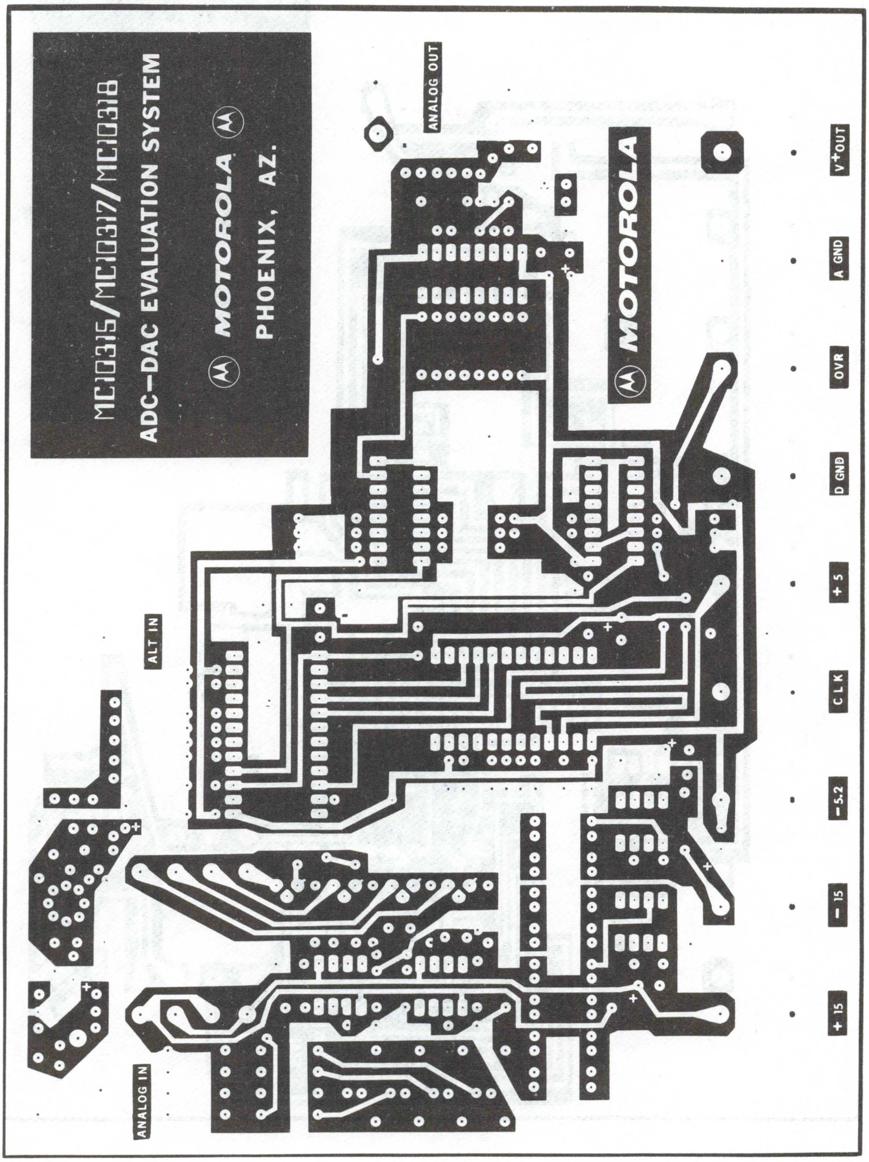

MC10315/MC10317/MC10318
ADC–DAC EVALUATION SYSTEM
MOTOROLA
PHOENIX, AZ.
ANALOG OUT
MOTOROLA
V+OUT
A GND
OVR
D GND
+5
CLK
−5.2
−15
+15
ALT IN
ANALOG IN

FIGURE 34 — SOLDER SIDE ARTWORK (BOTTOM)

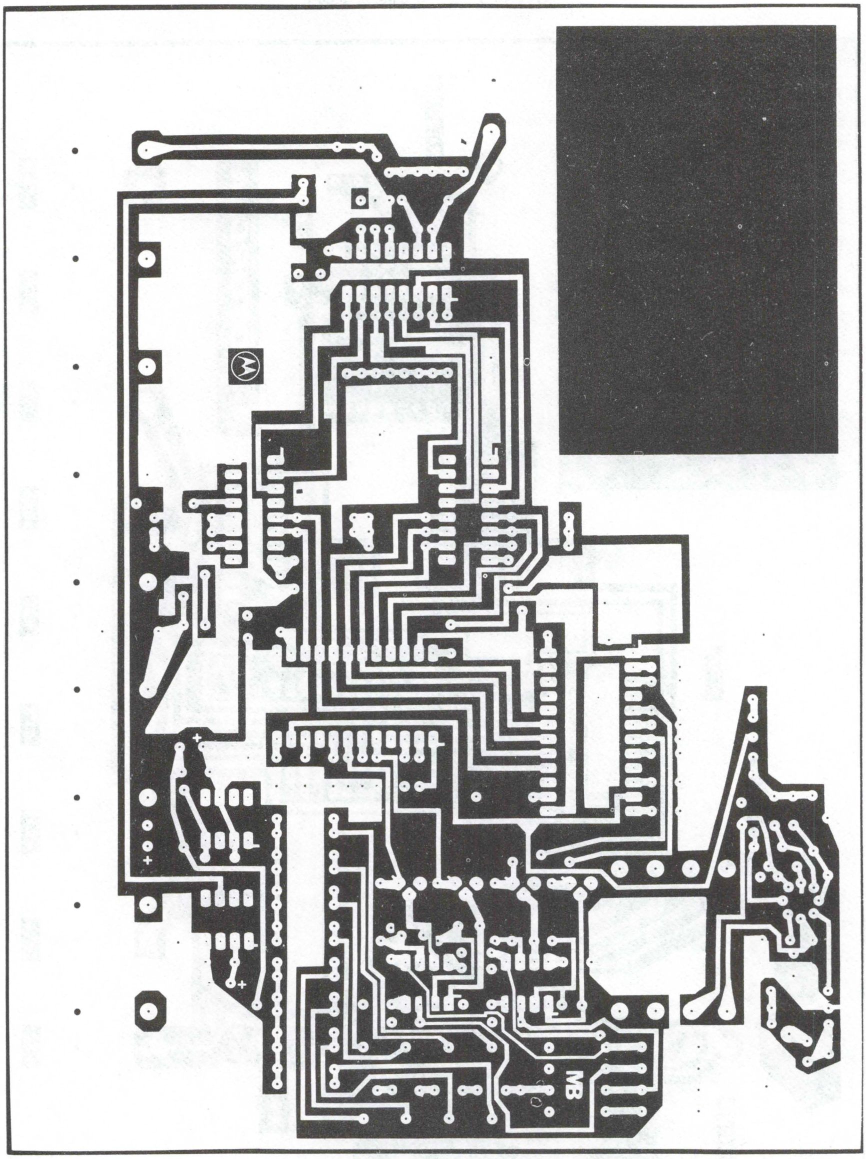
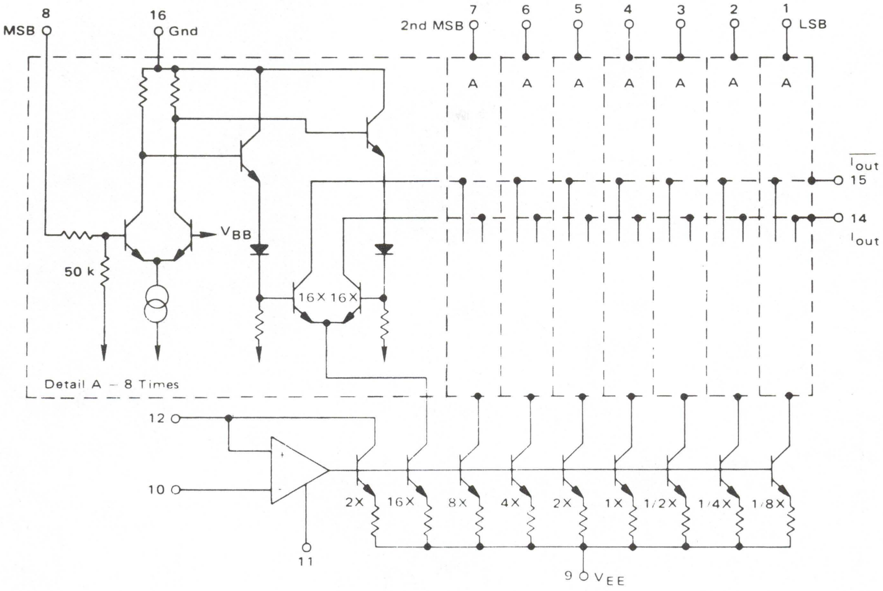
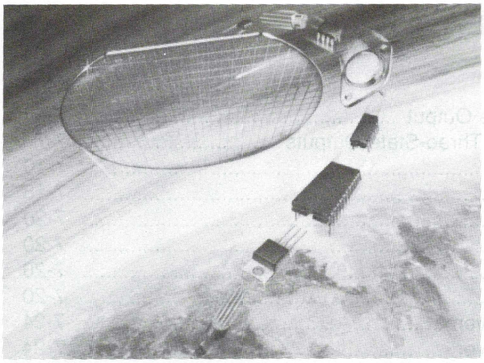


FIGURE 35 — MC10318 EQUIVALENT CIRCUIT


8
MSB
16
Gnd
7
2nd MSB
6
5
4
3
2
1
LSB
A
$\overline{I_{out}}$
15
14
I_{out}
V_{BB}
50 k
16X 16X
Detail A – 8 Times
12
10
11
2X
16X
8X
4X
2X
1X
1/2X
1/4X
1/8X
9
V_{EE}



Interface

7

INTERFACE

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MC8T95	Hex Three-State Buffer/Inverter	7-20
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MC26S10	Quad Open-Collector Bus Transceiver	7-24
MC26S11	Quad Open-Collector Bus Transceiver	7-24
MC75S110	Dual Line Driver	7-27
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AM26LS31

MOTOROLA

QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA Standard RS-422 and Federal Standard 1020.

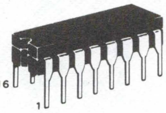
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 RS-422 driver.

The high impedance output state is assured during power down.

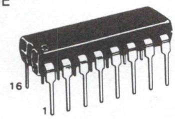
- Full RS-422 Standard Compliance
- Single +5 V Supply
- Meets Full $V_O = 6.0$ V, $V_{CC} = 0$ V, $I_O < 100\ \mu$A Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

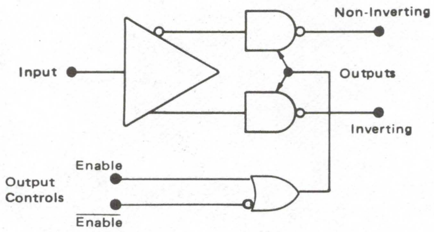


D SUFFIX
CERAMIC PACKAGE
CASE 620-02

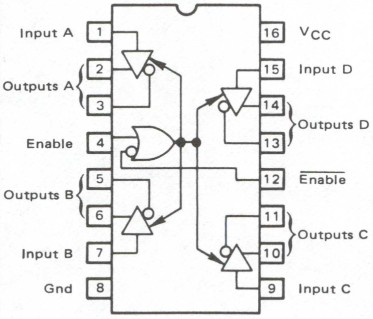


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

DRIVER BLOCK DIAGRAM


Non-Inverting
Input
Outputs
Inverting
Enable
Output Controls
$\overline{\text{Enable}}$

PIN CONNECTIONS


Input A 1
Outputs A 2
3
Enable 4
Outputs B 5
6
Input B 7
Gnd 8
16 VCC
15 Input D
14 Outputs D
13
12 $\overline{\text{Enable}}$
11 Outputs C
10
9 Input C

ORDERING INFORMATION

Device	Temperature Range	Package
AM26LS31DC	0 to 70°C	Ceramic DIP
AM26LS31PC	0 to 70°C	Plastic DIP

TRUTH TABLE

Input	Control Inputs (E/$\overline{\text{E}}$)	Non-Inverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply 4.75 V $\leq V_{CC} \leq$ 5.25 V and 0°C $\leq T_A \leq$ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–	-360	µA
Input Current – High Logic State	I_{IH}				µA
(V_{IH} = 2.7 V)		–	–	+20	
(V_{IH} = 7.0 V)		–	–	+100	
Input Clamp Voltage (I_{IK} = -18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 20 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = -20 mA)	V_{OH}	2.5	–	–	V
Output Short-Circuit Current (V_{IH} = 2.0 V)[2]	I_{OS}	-30	–	-150	mA
Output Leakage Current – Hi-Z State	$I_{O(Z)}$				µA
(V_{OL} = 0.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V)		–	–	-20	
(V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V)		–	–	+20	
Output Leakage Current – Power OFF	$I_{O(off)}$				µA
(V_{OH} = 6.0 V, V_{CC} = 0 V)		–	–	+100	
(V_{OL} = -0.25 V, V_{CC} = 0 V)		–	–	-100	
Output Offset Voltage Difference[1]	$V_{OS}-\overline{V}_{OS}$	–	–	±0.4	V
Output Differential Voltage 1	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference 1	$\lvert\Delta V_{OD}\rvert$	–	–	±0.4	V
Power Supply Current (Output Disabled)[3]	I_{CCX}	–	60	80	mA

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	–	–	20	
Low to High Output	t_{PLH}	–	–	20	
Output Skew		–	–	6.0	ns
Propagation Delay – Control to Output					ns
(C_L = 10 pF, R_L = 75 Ω to Gnd)	$t_{PHZ(E)}$	–	–	30	
(C_L = 10 pF, R_L = 180 Ω to V_{CC})	$t_{PLZ(E)}$	–	–	35	
(C_L = 30 pF, R_L = 75 Ω to Gnd)	$t_{PZH(E)}$	–	–	40	
(C_L = 30 pF, R_L = 180 Ω to V_{CC})	$t_{PZL(E)}$	–	–	45	

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

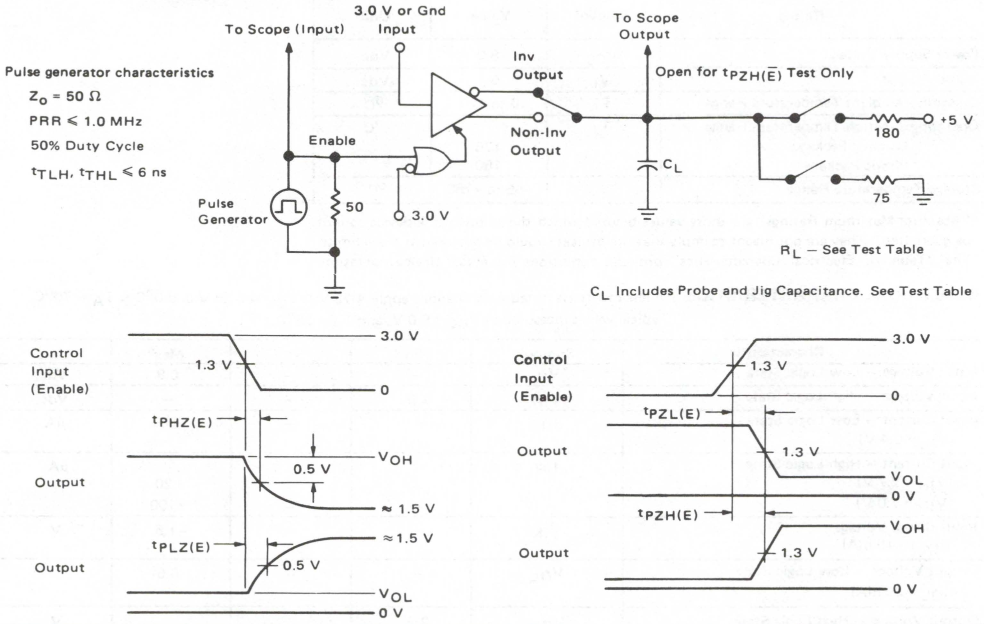
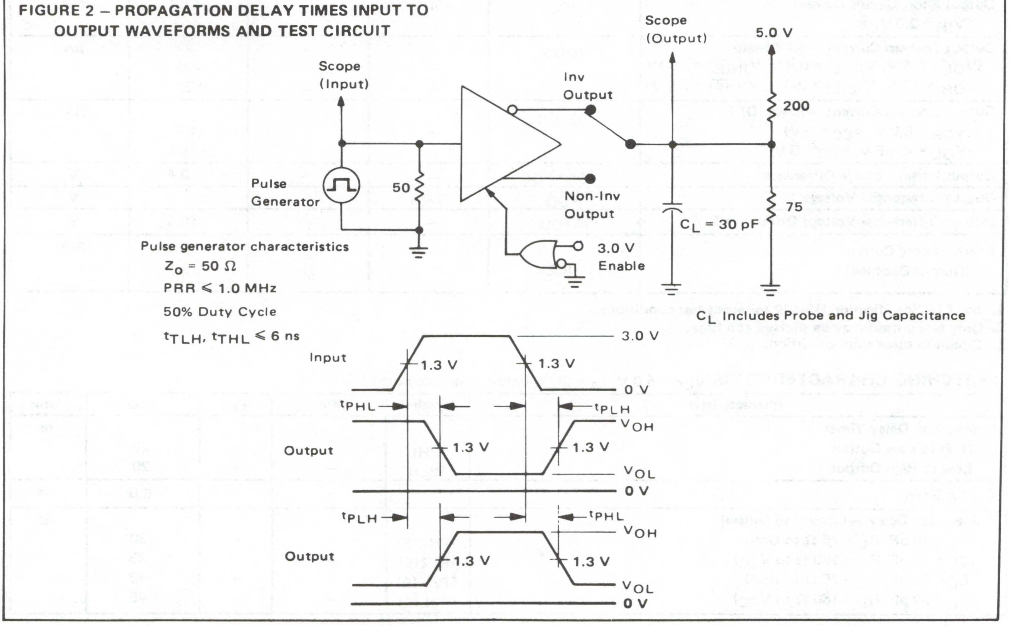

3.0 V or Gnd
Input
To Scope (Input)
To Scope
Output
Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR ≤ 1.0 MHz
50% Duty Cycle
$t_{TLH}, t_{THL} \leq 6$ ns
Inv
Output
Open for $t_{PZH(\overline{E})}$ Test Only
+5 V
180
Enable
Non-Inv
Output
C_L
75
Pulse
Generator
50
3.0 V
R_L – See Test Table
C_L Includes Probe and Jig Capacitance. See Test Table
Control
Input
(Enable)
3.0 V
1.3 V
0
$t_{PHZ(E)}$
V_{OH}
0.5 V
Output
≈ 1.5 V
≈1.5 V
$t_{PLZ(E)}$
0.5 V
Output
V_{OL}
0 V
Control
Input
(Enable)
3.0 V
1.3 V
0
$t_{PZL(E)}$
Output
1.3 V
V_{OL}
0 V
$t_{PZH(E)}$
V_{OH}
Output
1.3 V
0 V

FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT


Scope
(Output)
5.0 V
Scope
(Input)
Inv
Output
200
Pulse
Generator
50
Non-Inv
Output
75
$C_L = 30$ pF
3.0 V
Enable
Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR ≤ 1.0 MHz
50% Duty Cycle
$t_{TLH}, t_{THL} \leq 6$ ns
C_L Includes Probe and Jig Capacitance
3.0 V
Input
1.3 V
1.3 V
0 V
t_{PHL}
t_{PLH}
V_{OH}
Output
1.3 V
1.3 V
V_{OL}
0 V
t_{PLH}
t_{PHL}
V_{OH}
Output
1.3 V
1.3 V
V_{OL}
0 V

MOTOROLA

AM26LS32

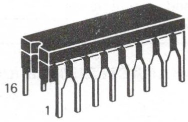
QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

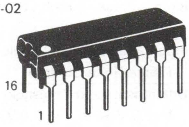
QUAD RS-422/423 LINE RECEIVER

Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1". A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times — 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6K Minimum Input Impedance

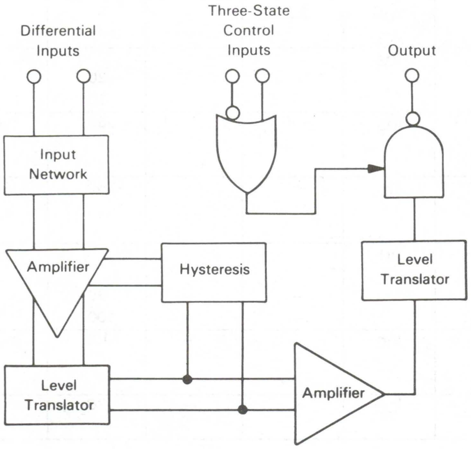


D SUFFIX
CERAMIC PACKAGE
CASE 620-02

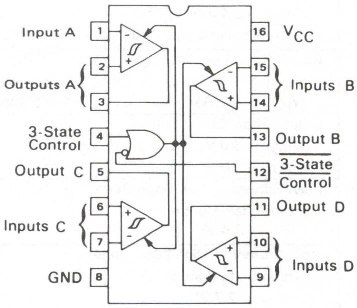


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

RECEIVER CHAIN BLOCK DIAGRAM


Differential Inputs
Three-State Control Inputs
Output
Input Network
Amplifier
Hysteresis
Level Translator
Level Translator
Amplifier

PIN CONNECTIONS


Input A
1
Outputs A
2
3
3-State Control
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control
11
Output D
10
Inputs D
9

ORDERING INFORMATION		
Device	**Temperature**	**Package**
AM26LS32D	0 to +70°C	Ceramic DIP
AM26LS32P	0 to +70°C	Plastic DIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	−7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IC} = 0.V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage (Note 4) ($-7.0\ V \leqslant V_{IC} \leqslant 7.0\ V$, $V_{IH} = 2.0\ V$)	$V_{TH(D)}$				V
($I_O = -0.4$ mA, $V_{OH} \geqslant 2.7$ V)		—	—	0.2	
($I_O = 8.0$ mA, $V_{OL} \leqslant 0.45$ V)		—	—	-0.2	
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at $-15\ V \leqslant V_{in} \leqslant +15\ V$)	$I_{IB(D)}$				mA
$V_{in} = +15$ V		—	—	2.3	
$V_{in} = -15$ V		—	—	-2.8	
Input Resistance ($-15\ V \leqslant V_{in} \leqslant +15\ V$)	R_{in}	6.0 K	—	—	Ohms
Input Balance and Output Level ($-7.0\ V \leqslant V_{IC} \leqslant 7.0\ V$, $V_{IH} = 2.0\ V$, See Note 3)					V
($I_O = -0.4$ mA, $V_{ID} = 0.4$ V)	V_{OH}	2.7	—	—	
($I_O = 8.0$ mA, $V_{ID} = -0.4$ V)	V_{OL}	—	—	0.45	
Output Third State Leakage Current	I_{OZ}				µA
($V_{I(D)} = +3.0$ V, $V_{IL} = 0.8$ V, $V_O = 0.4$ V)		—	—	-20	
($V_{I(D)} = -3.0$ V, $V_{IL} = 0.8$ V, $V_O = 2.4$ V)		—	—	20	
Output Short-Circuit Current ($V_{I(D)} = 3.0$ V, $V_{IH} = 2.0$ V, $V_O = 0$ V) See Note 2)	I_{OS}	−15	—	-85	mA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.4$ V)	I_{IL}	—	—	-360	µA
Input Current — High Logic State (Three-State Control)	I_{IH}				µA
($V_{IH} = 2.7$ V)		—	—	20	
($V_{IH} = 5.5$ V)		—	—	100	
Input Clamp Diode Voltage (Three-State Control) ($I_{IC} = -18$ mA)	V_{IC}	—	—	-1.5	V
Power Supply Current ($V_{IL} = 0$ V) (All Inputs Grounded)	I_{CC}	—	—	70	mA

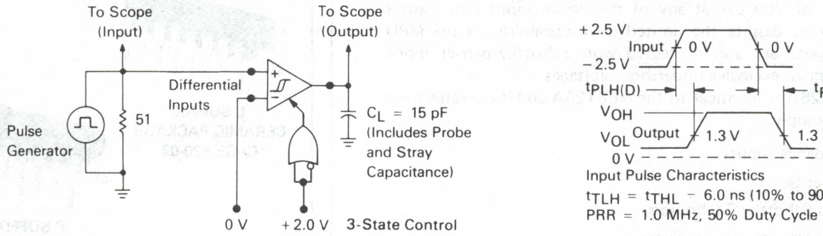
SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential					ns
Inputs to Output					
(Output High to Low)	$t_{PHL(D)}$	—	—	30	
(Output Low to High)	$t_{PLH(D)}$	—	—	30	
Propagation Delay Time — Three-State					ns
Control to Output					
(Output Low to Third State)	t_{PLZ}	—	—	35	
(Output High to Third State)	t_{PHZ}	—	—	35	
(Output Third State to High)	t_{PZH}	—	—	30	
(Output Third State to Low)	t_{PZL}	—	—	30	

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

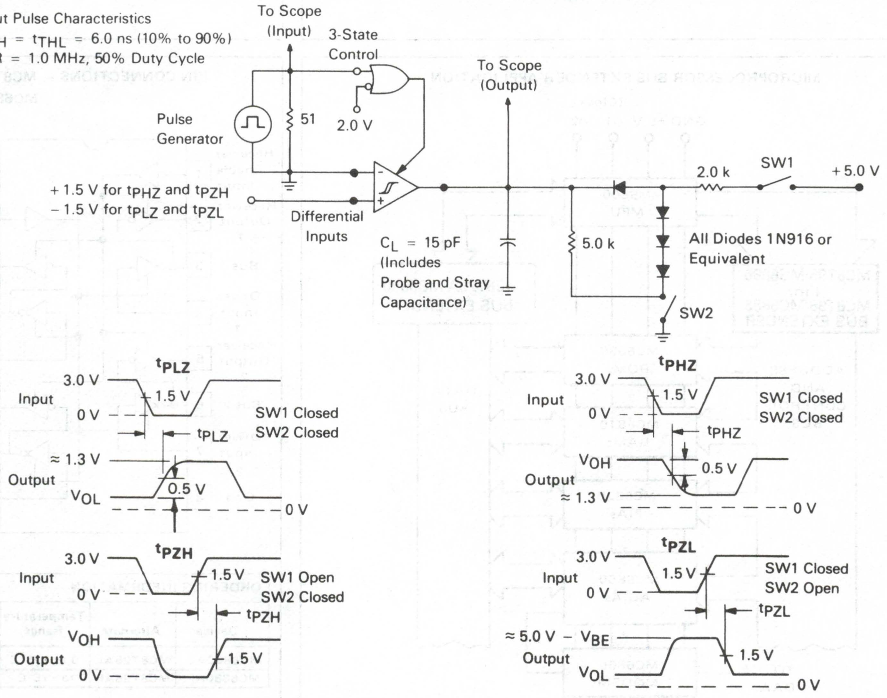
SWITCHING TEST CIRCUIT AND WAVE FOR
FIGURE 1 - PROPAGATION DELAY DIFFERENTIAL INPUT TO OUTPUT


To Scope (Input)
To Scope (Output)
Differential Inputs
Pulse Generator
51
C_L = 15 pF (Includes Probe and Stray Capacitance)
0 V
+2.0 V
3-State Control
+2.5 V
Input
0 V
0 V
−2.5 V
$t_{PLH(D)}$
$t_{PHL(D)}$
V_{OH}
V_{OL}
Output
1.3 V
1.3 V
0 V

Input Pulse Characteristics
t_{TLH} = t_{THL} = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT

Input Pulse Characteristics
t_{TLH} = t_{THL} = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle


To Scope (Input)
3-State Control
To Scope (Output)
Pulse Generator
51
2.0 V
+1.5 V for t_{PHZ} and t_{PZH}
−1.5 V for t_{PLZ} and t_{PZL}
Differential Inputs
C_L = 15 pF (Includes Probe and Stray Capacitance)
5.0 k
2.0 k
SW1
+5.0 V
All Diodes 1N916 or Equivalent
SW2
t_{PLZ}
3.0 V
Input
0 V
1.5 V
SW1 Closed
SW2 Closed
t_{PLZ}
≈ 1.3 V
Output
V_{OL}
0.5 V
0 V
t_{PZH}
3.0 V
Input
0 V
1.5 V
SW1 Open
SW2 Closed
t_{PZH}
V_{OH}
Output
0 V
1.5 V
t_{PHZ}
3.0 V
Input
0 V
1.5 V
SW1 Closed
SW2 Closed
t_{PHZ}
V_{OH}
0.5 V
Output
≈ 1.3 V
0 V
t_{PZL}
3.0 V
Input
0 V
1.5 V
SW1 Closed
SW2 Open
t_{PZL}
≈ 5.0 V − V_{BE}
Output
V_{OL}
1.5 V
0 V

MC8T26A
MC6880A

MOTOROLA

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

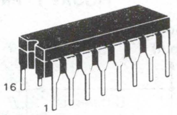
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

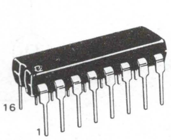
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

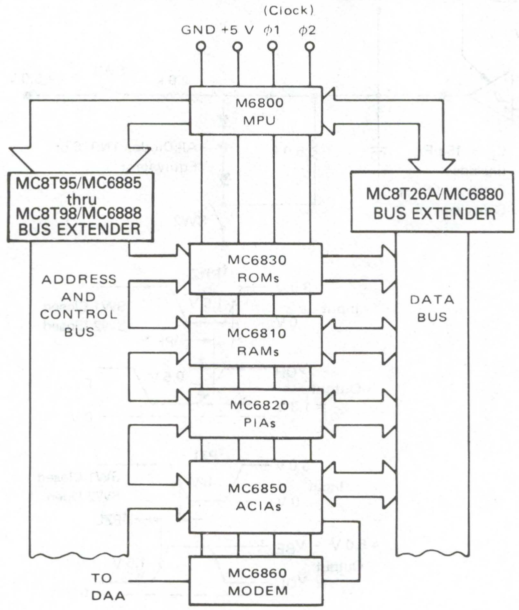


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

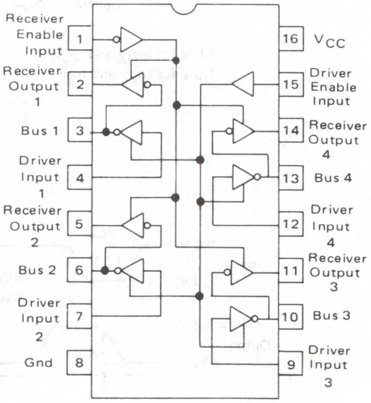


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
GND +5 V φ1 φ2
M6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T26A/MC6880 BUS EXTENDER
ADDRESS AND CONTROL BUS
DATA BUS
MC6830 ROMs
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 MODEM
TO DAA

PIN CONNECTIONS – MC8T26A MC6880A


Receiver Enable Input 1
Receiver Output 1 2
Bus 1 3
Driver Input 1 4
Receiver Output 2 5
Bus 2 6
Driver Input 2 7
Gnd 8
16 VCC
15 Driver Enable Input
14 Receiver Output 4
13 Bus 4
12 Driver Input 4
11 Receiver Output 3
10 Bus 3
9 Driver Input 3

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC6880AL	MC8T26AL	0 to +75°C	Ceramic DIP
MC6880AP	MC8T26AP	0 to +75°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ⩽ V_{CC} ⩽ 5.25 V and 0°C ⩽ T_A ⩽ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State					
($\overline{\text{Receiver Enable}}$ Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	µA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current – Low Logic State	$I_{IL(D)\ DIS}$				
(Driver Input, $V_{IL(D)}$ = 0.4 V)		–	–	-25	µA
Input Current-High Logic State					
($\overline{\text{Receiver Enable}}$ Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	µA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
(Receiver Input, $V_{IH(B)}$ = 5.25 V)	$I_{IH(B)}$	–	–	100	
Input Voltage – Low Logic State					
($\overline{\text{Receiver Enable}}$ Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage – High Logic State					
($\overline{\text{Receiver Enable}}$ Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage – Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage – High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = –10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = –2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = –100 µA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current – High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	µA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current – Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	–100	µA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	–100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = –12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = –12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

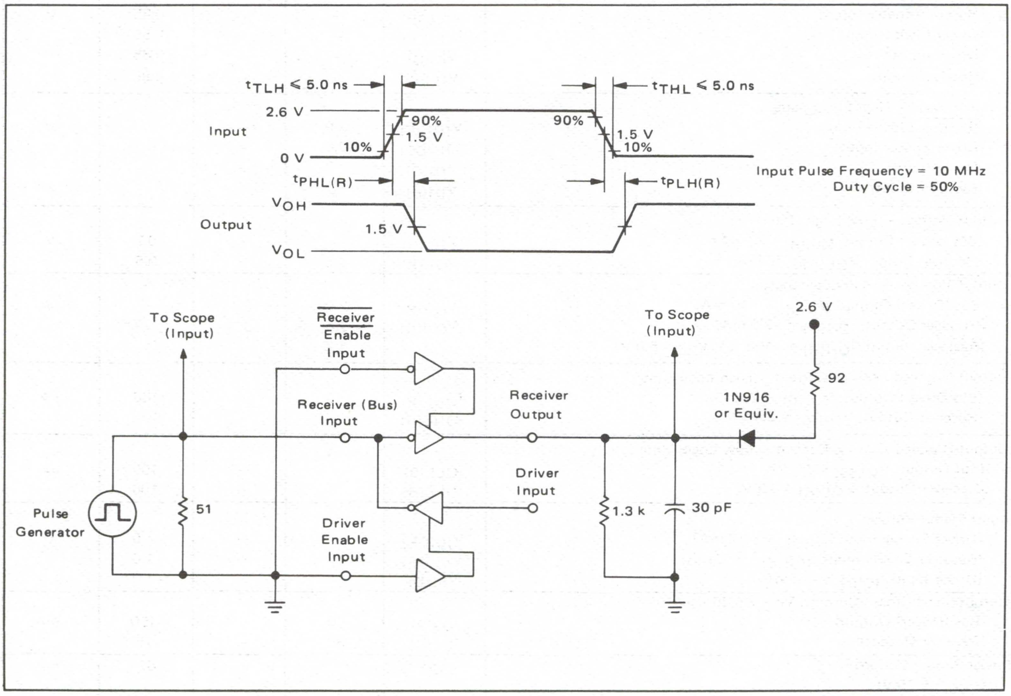

$t_{TLH} \leq 5.0$ ns
$t_{THL} \leq 5.0$ ns
2.6 V
Input
90%
1.5 V
10%
0 V
$t_{PHL(R)}$
$t_{PLH(R)}$
V_{OH}
Output
1.5 V
V_{OL}
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
To Scope (Input)
$\overline{\text{Receiver}}$ Enable Input
Receiver (Bus) Input
Receiver Output
To Scope (Input)
2.6 V
92
1N916 or Equiv.
Driver Input
Pulse Generator
51
Driver Enable Input
1.3 k
30 pF

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

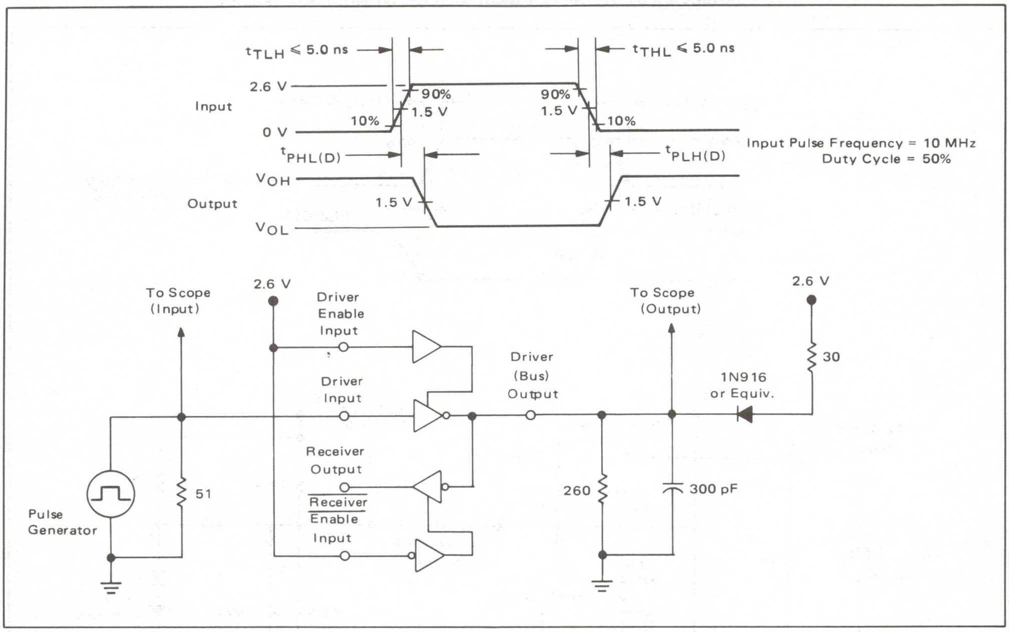

t_{TLH} ≤ 5.0 ns
t_{THL} ≤ 5.0 ns
2.6 V
Input
90%
1.5 V
10%
0 V
$t_{PHL(D)}$
$t_{PLH(D)}$
V_{OH}
Output
1.5 V
V_{OL}
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
To Scope (Input)
2.6 V
Driver Enable Input
Driver Input
Receiver Output
Receiver Enable Input
Pulse Generator
51
Driver (Bus) Output
To Scope (Output)
2.6 V
30
1N916 or Equiv.
260
300 pF

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

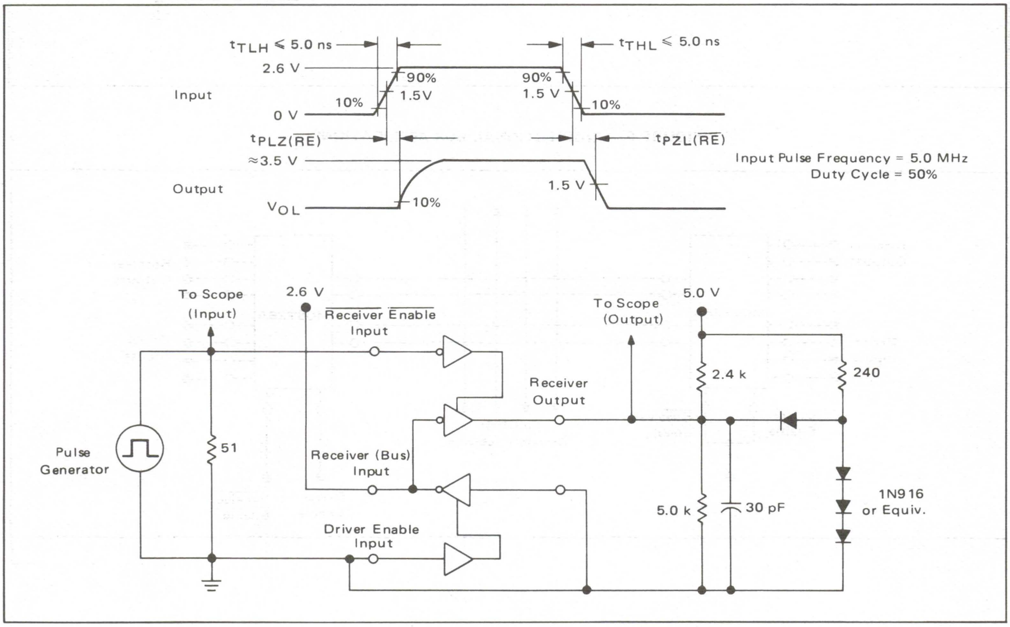
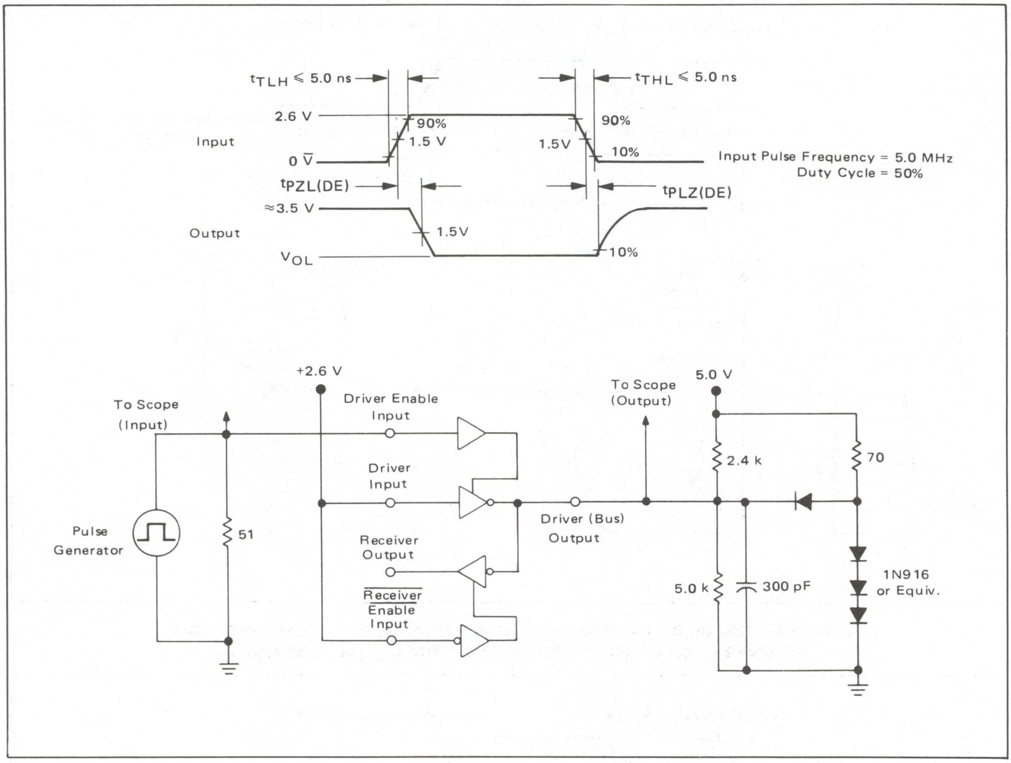
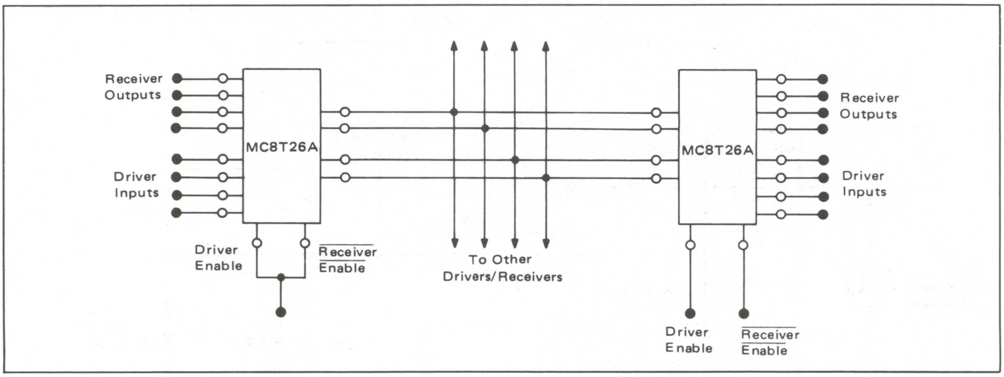

t_{TLH} ≤ 5.0 ns
t_{THL} ≤ 5.0 ns
2.6 V
Input
90%
1.5V
10%
0 V
$t_{PLZ(\overline{RE})}$
$t_{PZL(\overline{RE})}$
≈3.5 V
Output
1.5 V
V_{OL}
10%
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
To Scope (Input)
2.6 V
Receiver Enable Input
To Scope (Output)
5.0 V
2.4 k
240
Receiver Output
Pulse Generator
51
Receiver (Bus) Input
Driver Enable Input
5.0 k
30 pF
1N916 or Equiv.

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$



tTLH ≤ 5.0 ns
tTHL ≤ 5.0 ns
2.6 V
90%
1.5 V
1.5V
90%
10%
Input
0 V
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
tPZL(DE)
tPLZ(DE)
≈3.5 V
Output
1.5V
VOL
10%
+2.6 V
To Scope (Input)
Driver Enable Input
To Scope (Output)
5.0 V
2.4 k
70
Driver Input
Pulse Generator
51
Driver (Bus) Output
Receiver Output
Receiver Enable Input
5.0 k
300 pF
1N916 or Equiv.

FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



Receiver Outputs
Driver Inputs
MC8T26A
Driver Enable
Receiver Enable
To Other Drivers/Receivers
MC8T26A
Receiver Outputs
Driver Inputs
Driver Enable
Receiver Enable

MOTOROLA

MC8T28
MC6889

NONINVERTING QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

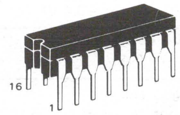
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

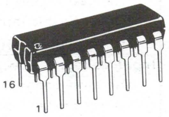
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

NONINVERTING BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

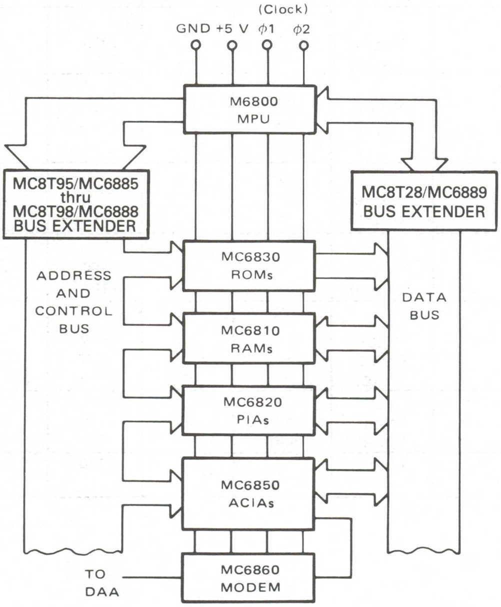


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

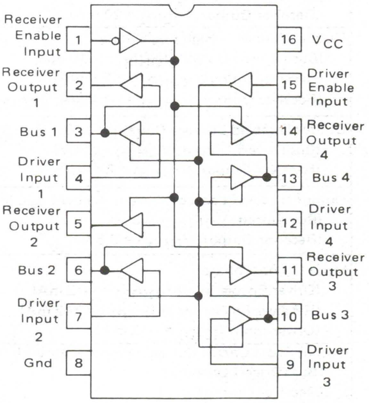


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
GND
+5 V
φ1
φ2
M6800
MPU
MC8T95/MC6885
thru
MC8T98/MC6888
BUS EXTENDER
MC8T28/MC6889
BUS EXTENDER
ADDRESS
AND
CONTROL
BUS
DATA
BUS
MC6830
ROMs
MC6810
RAMs
MC6820
PIAs
MC6850
ACIAs
MC6860
MODEM
TO
DAA

PIN CONNECTIONS — MC8T28 MC6889


Receiver Enable Input
1
Receiver Output 1
2
Bus 1
3
Driver Input 1
4
Receiver Output 2
5
Bus 2
6
Driver Input 2
7
Gnd
8
16
V_CC
15
Driver Enable Input
14
Receiver Output 4
13
Bus 4
12
Driver Input 4
11
Receiver Output 3
10
Bus 3
9
Driver Input 3

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T28L	MC6889L	0 to +75°C	Ceramic DIP
MC8T28P	MC6889P	0 to +75°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

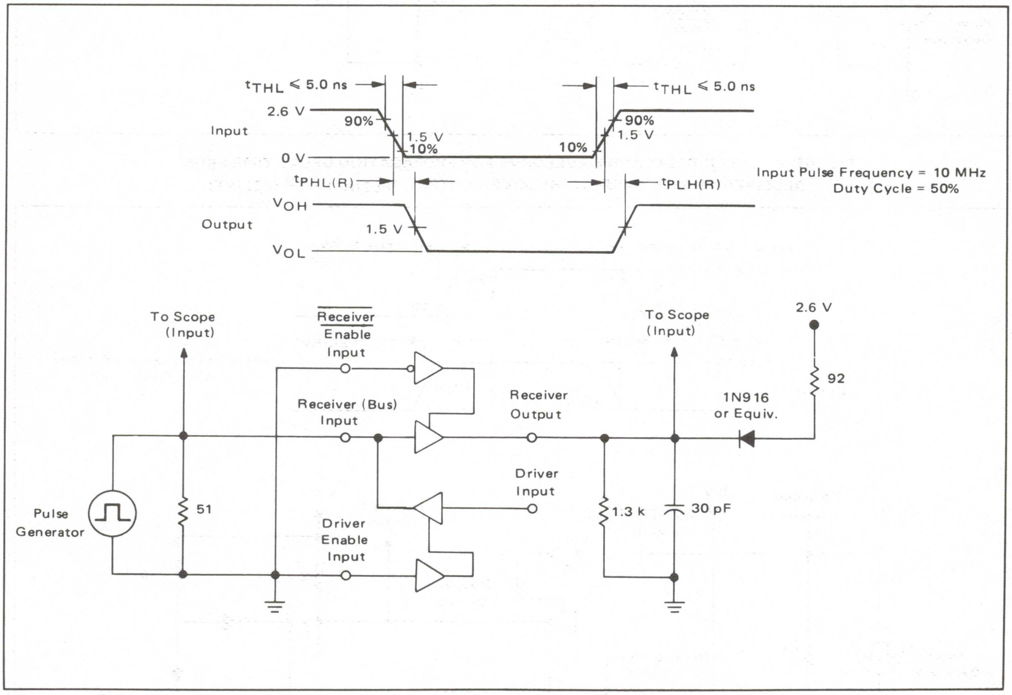
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State					
(Receiver Enable Input, $V_{IL(\overline{RE})}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	µA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current – Low Logic State	$I_{IL(D)\ DIS}$				
(Driver Input, $V_{IL(D)}$ = 0.4 V)		–	–	-25	µA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(\overline{RE})}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	µA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
Input Voltage – Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage – High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage – Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage – High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = –10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = –2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = –100/µA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current – High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	µA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current – Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	-100	µA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	-100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = –12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = –12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current	I_{CC}	–	–	110	mA
(V_{CC} = 5.25 V)					

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver (C_L = 30 pF)	$t_{PLH(R)}$ $t_{PHL(R)}$	—	17 17	ns
Propagation Delay Time—Driver (C_L = 300 pF)	$t_{PLH(D)}$ $t_{PHL(D)}$	—	17 17	ns
Propagation Delay Time—Enable (C_L = 30 pF) — Receiver	$t_{PZL(R)}$ $t_{PLZ(R)}$	— —	23 18	ns
— Driver Enable (C_L 300 pF)	$t_{PZL(D)}$ $t_{PLZ(D)}$	— —	28 23	

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$



t_{THL} ≤ 5.0 ns
2.6 V
90%
Input
1.5 V
10%
0 V
10%
t_{THL} ≤ 5.0 ns
90%
1.5 V
$t_{PHL(R)}$
$t_{PLH(R)}$
V_{OH}
Output
1.5 V
V_{OL}
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
To Scope (Input)
Receiver Enable Input
Receiver (Bus) Input
Receiver Output
To Scope (Input)
2.6 V
92
1N916 or Equiv.
Driver Input
Pulse Generator
51
Driver Enable Input
1.3 k
30 pF

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

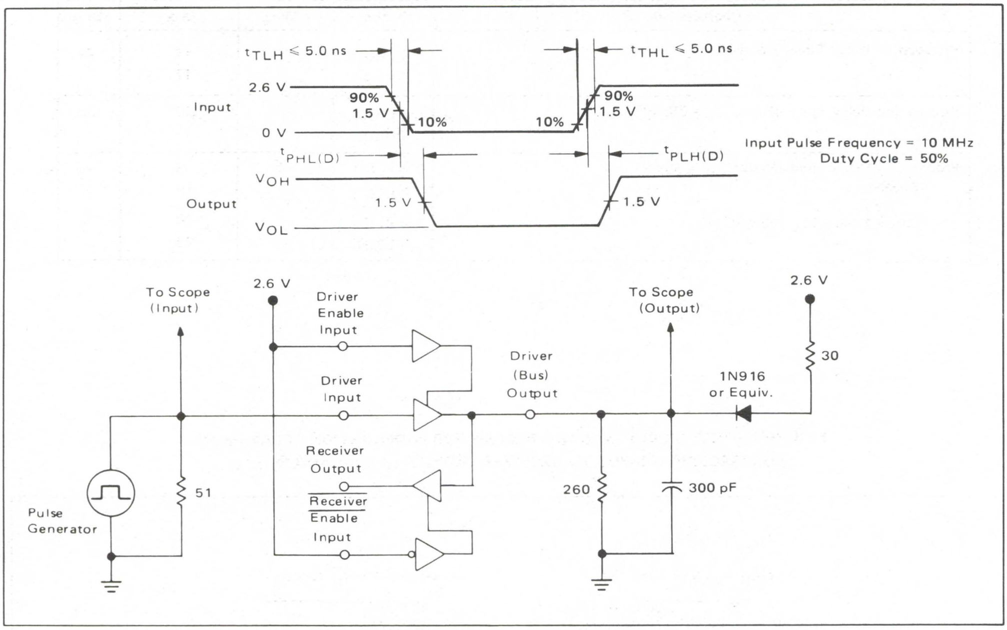

tTLH ≤ 5.0 ns
tTHL ≤ 5.0 ns
2.6 V
Input
90%
1.5 V
10%
0 V
tPHL(D)
tPLH(D)
VOH
Output
VOL
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
To Scope (Input)
2.6 V
Driver Enable Input
Driver Input
Receiver Output
Receiver Enable Input
Driver (Bus) Output
To Scope (Output)
1N916 or Equiv.
30
260
300 pF
51
Pulse Generator

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

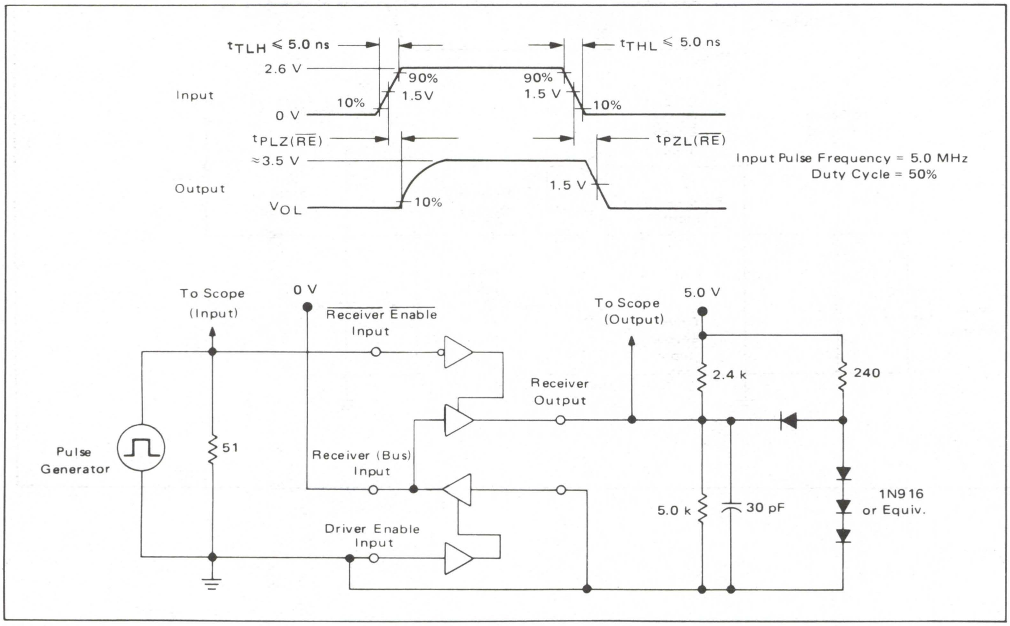

tTLH ≤ 5.0 ns
tTHL ≤ 5.0 ns
2.6 V
Input
90%
1.5V
10%
0 V
tPLZ(RE)
tPZL(RE)
≈3.5 V
Output
VOL
1.5 V
10%
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
To Scope (Input)
0 V
Receiver Enable Input
Receiver (Bus) Input
Driver Enable Input
Pulse Generator
51
To Scope (Output)
5.0 V
Receiver Output
2.4 k
240
5.0 k
30 pF
1N916 or Equiv.

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

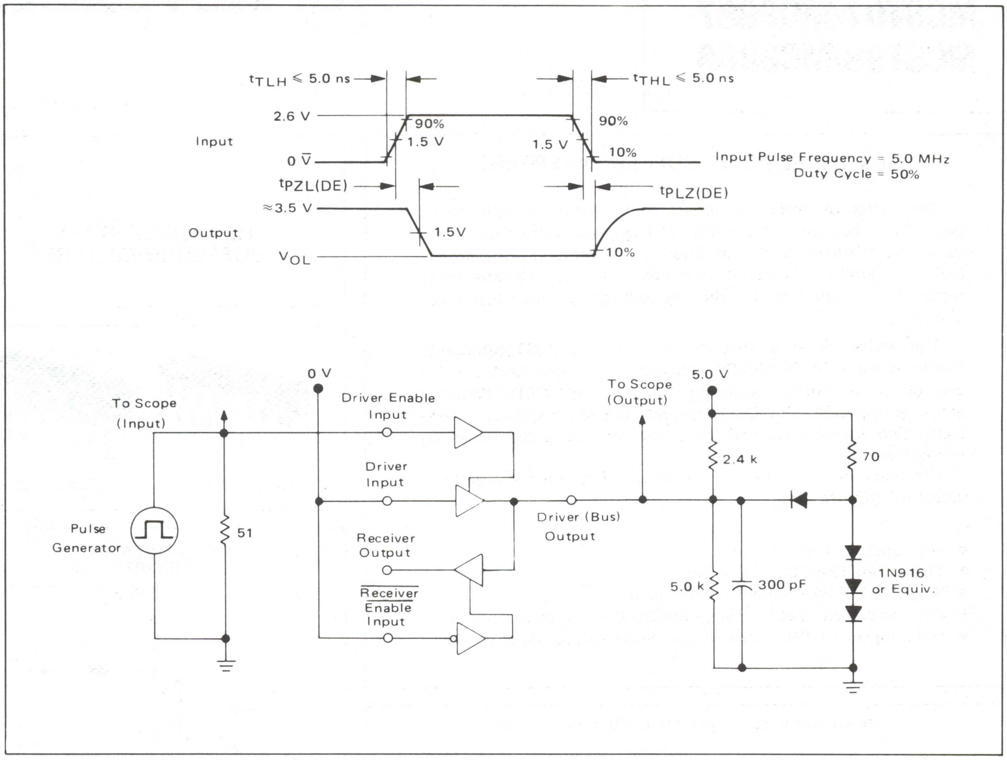
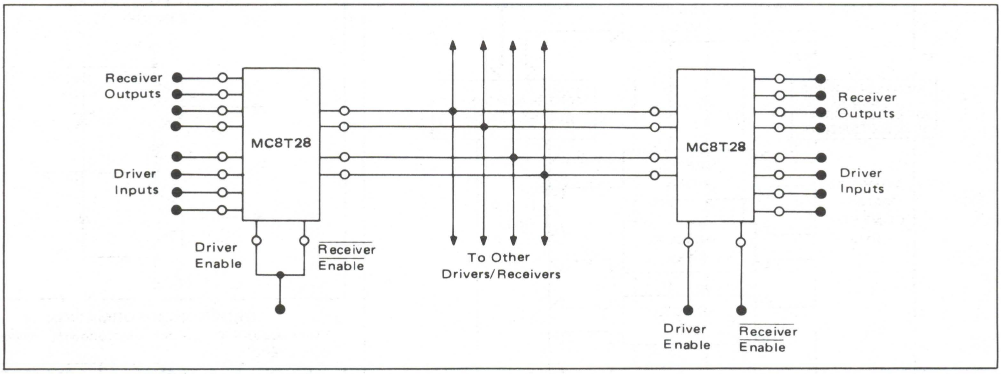

$t_{TLH} \leq 5.0$ ns
$t_{THL} \leq 5.0$ ns
2.6 V
Input
0 V
90%
1.5 V
1.5 V
90%
10%
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
$t_{PZL(DE)}$
$t_{PLZ(DE)}$
≈3.5 V
Output
1.5V
V_{OL}
10%
0 V
To Scope (Input)
Driver Enable Input
Driver Input
Receiver Output
Receiver Enable Input
Pulse Generator
51
To Scope (Output)
5.0 V
2.4 k
70
Driver (Bus) Output
5.0 k
300 pF
1N916 or Equiv.

FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS


Receiver Outputs
Driver Inputs
MC8T28
Driver Enable
Receiver Enable
To Other Drivers/Receivers
MC8T28
Receiver Outputs
Driver Inputs
Driver Enable
Receiver Enable

MC8T95/MC6885
MC8T96/MC6886
MC8T97/MC6887
MC8T98/MC6888

MOTOROLA

HEX THREE-STATE BUFFER INVERTERS

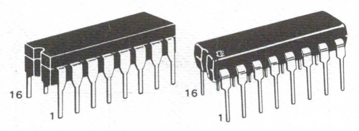
This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs – one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

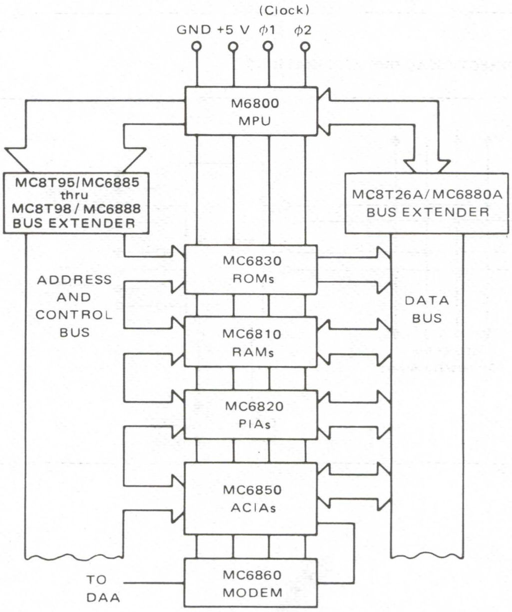
- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

HEX THREE-STATE BUFFER/INVERTERS

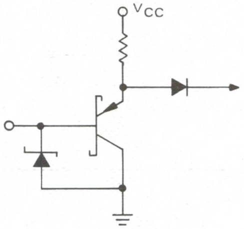


CASE 620-02 CASE 648-05

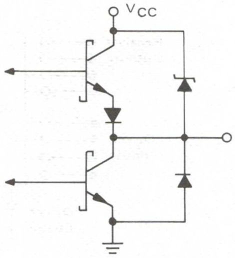
MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
GND
+5 V
ϕ1
ϕ2
M6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T26A/MC6880A BUS EXTENDER
ADDRESS AND CONTROL BUS
DATA BUS
MC6830 ROMs
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 MODEM
TO DAA

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



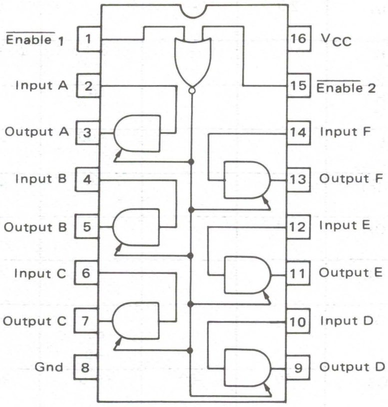
ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

DEVICE	ALTERNATE	PACKAGE
MC8T95L	MC6885L	Ceramic DIP
MC8T96L	MC6886L	Ceramic DIP
MC8T97L	MC6887L	Ceramic DIP
MC8T98L	MC6888L	Ceramic DIP
MC8T95P	MC6885P	Plastic DIP
MC8T96P	MC6886P	Plastic DIP
MC8T97P	MC6887P	Plastic DIP
MC8T98P	MC6888P	Plastic DIP

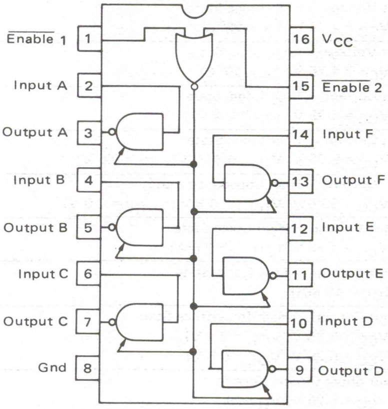
PIN CONNECTIONS AND TRUTH TABLES

MC8T95/MC6885


$\overline{\text{Enable}}$ 1
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
V_{CC}
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

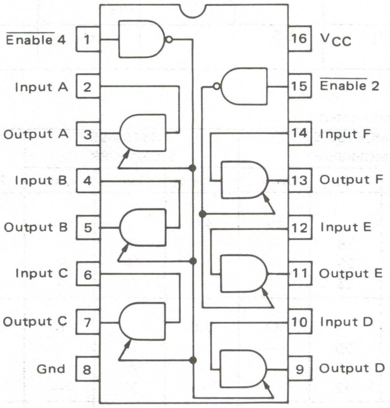
$\overline{\text{Enable}}$ 2	$\overline{\text{Enable}}$ 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

MC8T96/MC6886


$\overline{\text{Enable}}$ 1
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
V_{CC}
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

$\overline{\text{Enable}}$ 2	$\overline{\text{Enable}}$ 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

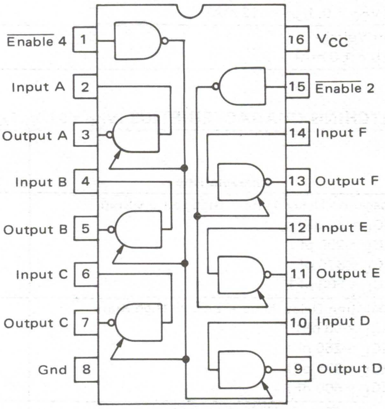
MC8T97/MC6887


$\overline{\text{Enable}}$ 4
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
V_{CC}
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

$\overline{\text{Enable}}$	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC8T98/MC6888


$\overline{\text{Enable}}$ 4
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
V_{CC}
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

$\overline{\text{Enable}}$	Input	Output
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 150 175	°C

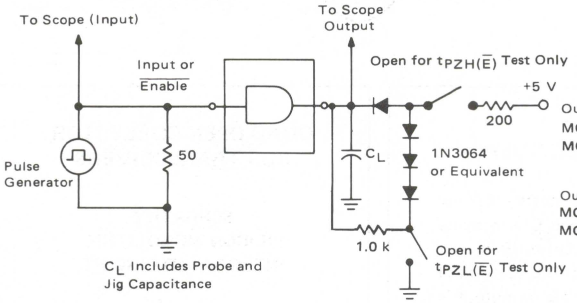
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^\circ C \leqslant T_A \leqslant 75^\circ C$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current – High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	µA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V)	I_{IL}	–	–	-400	µA
Input Current – High Impedance State (V_{CC} = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$= 2.0 V)	$I_{IH(\overline{E})}$	–	–	-40	µA
Output Voltage – High Logic State (V_{CC} = 4.75 V, I_{OH} = -5.2 mA)	V_{OH}	2.4	–	–	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current – High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	I_{OZ}	 – –	 – –	 40 -40	µA
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current (V_{CC} = 5.25 V) MC8T95, MC8T97, MC6885, MC6887 MC8T96, MC8T98, MC6886, MC6888	I_{CC}	 – –	 65 59	 98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	–	–	1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = -12 mA)	V_{OC}	–	–	-1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	5.5	–	–	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

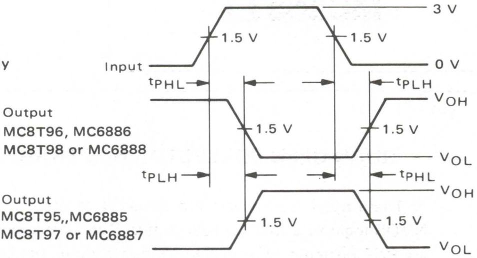
		MC8T95/97 MC6885/87			MC8T96/98 MC6886/88			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Propagation Delay Time – High to Low State	t_{PHL}							ns
(C_L = 50 pF)		3.0	–	12	4.0	–	11	
(C_L = 250 pF)		–	16	–	–	15	–	
(C_L = 375 pF)		–	20	–	–	18	–	
(C_L = 500 pF)		–	23	–	–	22	–	
Propagation Delay Time – Low to High State	t_{PLH}							ns
(C_L = 50 pF)		3.0	–	13	3.0	–	10	
(C_L = 250 pF)		–	25	–	–	22	–	
(C_L = 375 pF)		–	33	–	–	28	–	
(C_L = 500 pF)		–	42	–	–	35	–	
Transition Time – High to Low State	t_{THL}							ns
(C_L = 250 pF)		–	10	–	–	10	–	
(C_L = 375 pF)		–	11	–	–	13	–	
(C_L = 500 pF)		–	14	–	–	15	–	
Transition Time – Low to High State	t_{TLH}							ns
(C_L = 250 pF)		–	32	–	–	28	–	
(C_L = 375 pF)		–	42	–	–	38	–	
(C_L = 500 pF)		–	60	–	–	53	–	
Propagation Delay Time – High State to Third State (C_L = 5.0 pF)	$t_{PHZ(\overline{E})}$	–	–	10	–	–	10	ns
Propagation Delay Time – Low State to Third State (C_L = 5.0 pF)	$t_{PLZ(\overline{E})}$	–	–	12	–	–	16	ns
Propagation Delay Time – Third State to High State (C_L = 50 pF)	$t_{PZH(\overline{E})}$	–	–	25	–	–	22	ns
Propagation Delay Time – Third State to Low State (C_L = 50 pF)	$t_{PZL(\overline{E})}$	–	–	25	–	–	24	ns

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS


To Scope (Input)
To Scope Output
Input or $\overline{\text{Enable}}$
Open for $t_{PZH(\overline{E})}$ Test Only
+5 V
200
50
Pulse Generator
C_L
1N3064 or Equivalent
1.0 k
Open for $t_{PZL(\overline{E})}$ Test Only

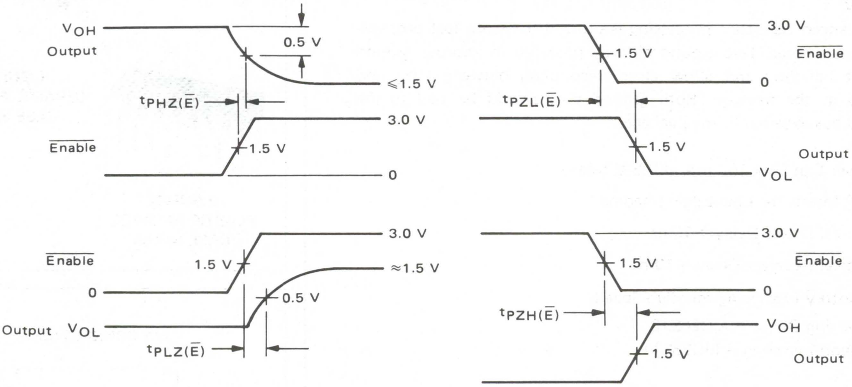
C_L Includes Probe and Jig Capacitance

FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT


3 V
1.5 V
1.5 V
Input
0 V
t_{PHL}
t_{PLH}
V_{OH}
Output
MC8T96, MC6886
MC8T98 or MC6888
1.5 V
1.5 V
V_{OL}
t_{PLH}
t_{PHL}
V_{OH}
Output
MC8T95,,MC6885
MC8T97 or MC6887
1.5 V
1.5 V
V_{OL}

Input Pulse Conditions
$t_{THL} = t_{TLH} \leqslant 10$ ns
f = 1.0 MHz

FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT


V_{OH}
Output
0.5 V
$\leqslant$1.5 V
$t_{PHZ(\overline{E})}$
3.0 V
$\overline{\text{Enable}}$
1.5 V
0
3.0 V
1.5 V
$\overline{\text{Enable}}$
0
$t_{PZL(\overline{E})}$
1.5 V
Output
V_{OL}
3.0 V
$\overline{\text{Enable}}$
1.5 V
$\approx$1.5 V
0
0.5 V
Output V_{OL}
$t_{PLZ(\overline{E})}$
3.0 V
1.5 V
$\overline{\text{Enable}}$
0
$t_{PZH(\overline{E})}$
V_{OH}
1.5 V
Output

H = High-Logic State, L = Low-Logic State, Z = High Impedance State

MC26S10
MC26S11

MOTOROLA

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

These quad transceivers are designed to mate Schottky TTL or NMOS logic to a low impedance bus. The $\overline{\text{Enable}}$ and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

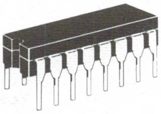
An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

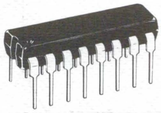
- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver – MC26S10
  Non-Inverting – MC26S11

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT

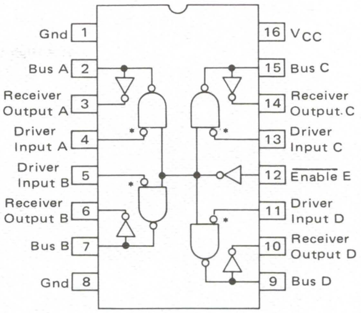


L SUFFIX
CERAMIC PACKAGE
CASE 620-02



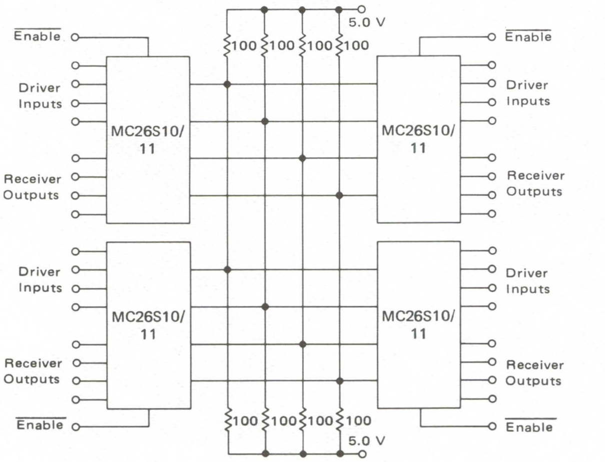
P SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS


Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D
*
*
*
*

*Inverter on MC26S11 only.

TYPICAL APPLICATION


5.0 V
100
100
100
100
Enable
Driver Inputs
Receiver Outputs
MC26S10/11
MC26S10/11
MC26S10/11
MC26S10/11
Enable
Driver Inputs
Receiver Outputs
Driver Inputs
Receiver Outputs
Enable
Driver Inputs
Receiver Outputs
Enable
100
100
100
100
5.0 V

TRUTH TABLE

$\overline{\text{Enable}}$	Bus	Drivers Input 26S10	Drivers Input 26S11	Receiver Output
L	H	L	H	L
L	L	H	L	H
H	Y	X	X	$\overline{Y}$

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by oter elements on the bus

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_I	-0.5 to +5.5	Vdc
Input Current	I_I	-3.0 to +5.0	mA
Output Voltage — High Impedance State	$V_{o\ (Hi\text{-}z)}$	-0.5 to V_{CC}	V
Output Current—Bus	$I_{o(B)}$	200	mA
Output Current—Receiver	$I_{o(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	—	—	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = −18 mA)	V_{IK}	—	—	-1.2	V
Input Current — Low Logic State (V_{IL} = 0.4 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IL}	 — —	 — —	 -0.36 -0.54	mA
Input Current — High Logic State (V_{IH} = 2.7 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IH}	 — —	 — —	 20 30	µA
Input Current — Maximum Voltage (V_{IH1} = 5.5 V) ($\overline{\text{Enable}}$ or Driver Inputs)	I_{IH1}	—	—	100	µA
Driver Output Voltage — Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 — — —	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 — —	 — —	 100 -50	µA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	—	—	100	µA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	—	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	—	2.0	1.75	V
Receiver Output Voltage — Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	—	—	0.5	V
Receiver Output Voltage — High Logic State (I_{OH} = −1.0 mA)	$V_{OH(R)}$	2.7	3.4	—	V
Receiver Output Short-Circuit Current (Note 1)	$I_{OS(R)}$	-18	—	-60	mA
Power Supply Current — Output Low State ($V_{IL(\overline{E})}$ = 0 V) MC26S10 MC26S11	I_{CC}	 — —	 45 —	 70 80	mA

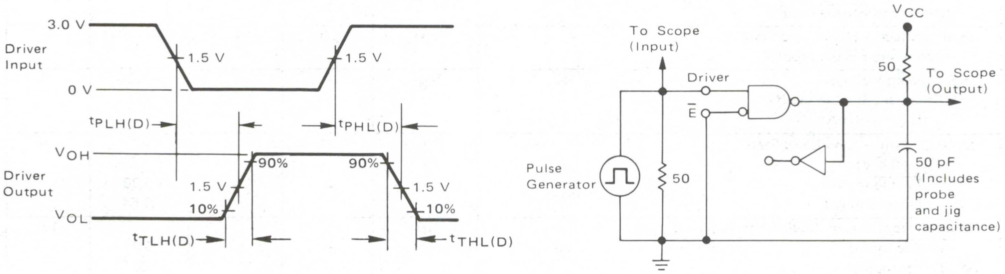
NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC26S10 Min	MC26S10 Typ	MC26S10 Max	MC26S11 Min	MC26S11 Typ	MC26S11 Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$	–	10	15	–	12	19	ns
	$t_{PHL(D)}$	–	10	15	–	12	19	
Propagation Delay Time Enable Input to Output	$t_{PLH(\overline{E})}$	–	14	18	–	15	20	ns
	$t_{PHL(\overline{E})}$	–	13	18	–	14	20	
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$	–	10	15	–	10	15	ns
	$t_{PHL(R)}$	–	10	15	–	10	15	
Rise and Fall Time of Driver Output	$t_{TLH(D)}$	4.0	10	–	4.0	10	–	ns
	$t_{THL(D)}$	2.0	4.0	–	2.0	4.0	–	

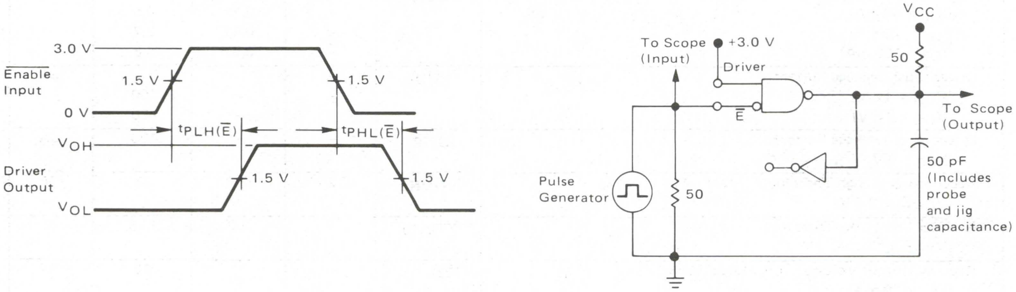
SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 – DATA INPUT TO BUS OUTPUT (DRIVER)



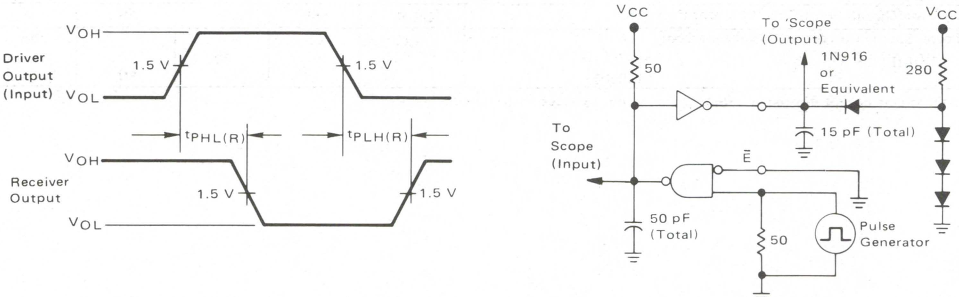
3.0 V
Driver Input
0 V
1.5 V
1.5 V
tPLH(D)
tPHL(D)
VOH
Driver Output
VOL
90%
90%
1.5 V
1.5 V
10%
10%
tTLH(D)
tTHL(D)
VCC
To Scope (Input)
Driver
Ē
50
To Scope (Output)
Pulse Generator
50
50 pF (Includes probe and jig capacitance)

FIGURE 2 – ENABLE INPUT TO BUS OUTPUT (DRIVER)



3.0 V
Enable Input
0 V
1.5 V
1.5 V
tPLH(Ē)
tPHL(Ē)
VOH
Driver Output
VOL
1.5 V
1.5 V
VCC
To Scope (Input)
+3.0 V
Driver
Ē
50
To Scope (Output)
Pulse Generator
50
50 pF (Includes probe and jig capacitance)

FIGURE 3 – BUS INPUT TO RECEIVER OUTPUT



VOH
Driver Output (Input)
VOL
1.5 V
1.5 V
tPHL(R)
tPLH(R)
VOH
Receiver Output
VOL
1.5 V
1.5 V
VCC
50
To Scope (Output)
1N916 or Equivalent
VCC
280
15 pF (Total)
To Scope (Input)
Ē
50 pF (Total)
50
Pulse Generator

MOTOROLA

MC75S110

MONOLITHIC DUAL LINE DRIVER

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes.

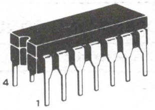
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of −3.0 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

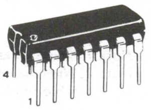
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- High Common-Mode Output Voltage Range (−3.0 V to +10 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVERS

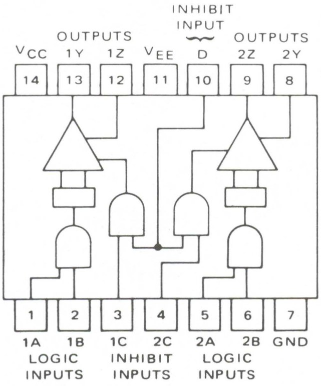
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



P SUFFIX
PLASTIC PACKAGE
CASE 646-05



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
High output represents the "off" state.

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Ceramic Dual In-Line Package Plastic Dual In-Line Package	T_{stg}	 -65 to +150 -65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range	V_{OCR}	−3.0	—	−10	Volts

Note 1. These voltage values are in respect to the ground terminal.
Note 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, V_{EE} = −4.75 to −5.25 V, T_A = 0 to +70°C unless otherwise noted.)

Characteristic # #	Symbol	Min	Typ #	Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)# (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 — —	 — —	 40 1.0	 μA mA
Low-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	 —	 —	 −3.0	mA
High-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 — —	 — —	 40 1.0	 μA mA
Low-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	 —	 —	 −3.0	mA
High-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 — —	 — —	 80 2.0	 μA mA
Low-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	 —	 —	 −6.0	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 — 6.5	 12 —	 15 —	mA
Output Current ("off" state)	$I_{O(off)}$	—		100	μA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	 —	 28	 35	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	 —	 −41	 −50	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_L} = 0.4 V)	$I_{CC(off)}$	 —	 21	 35	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	 —	 −17	 −50	mA

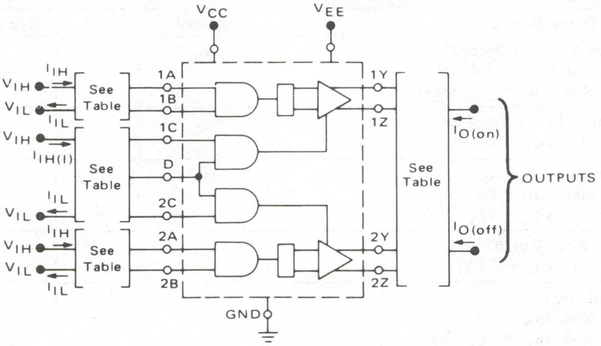
#Values are at V_{CC} = +5.0 V, V_{EE} = −5.0 V.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	– –	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	– –	16 13	25 25	ns

TEST CIRCUITS

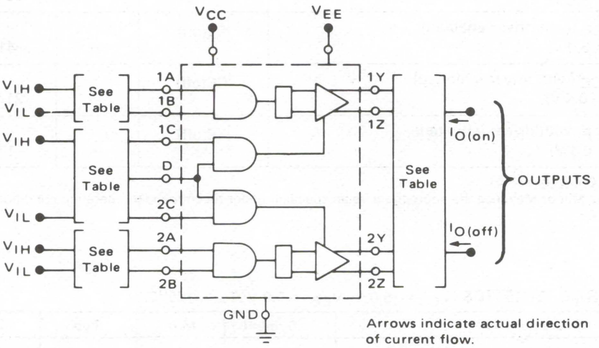
FIGURE 1 — I_{IH}, I_{IL}


VCC
VEE
IIH
VIH
VIL
IIL
VIH
IIH(I)
IIL
VIL
IIH
VIH
VIL
IIL
See Table
See Table
See Table
1A
1B
1C
D
2C
2A
2B
1Y
1Z
2Y
2Z
See Table
IO(on)
IO(off)
OUTPUTS
GND

TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
I_{IH_I}	Gnd	Gnd	Gnd	Gnd
I_{IL_I}	Gnd	4.5 V	Gnd	Gnd

FIGURE 2 — $I_{O(on)}$ and $I_{O(off)}$


VCC
VEE
VIH
VIL
VIH
VIL
VIH
VIL
See Table
See Table
See Table
1A
1B
1C
D
2C
2A
2B
1Y
1Z
2Y
2Z
See Table
IO(on)
IO(off)
OUTPUTS
GND

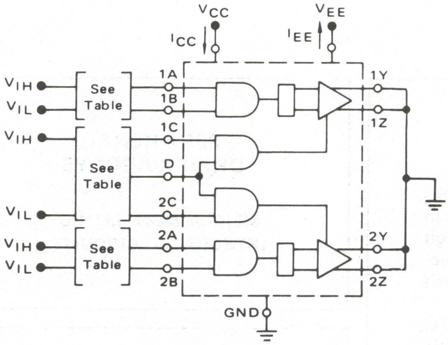
Arrows indicate actual direction of current flow.

TEST TABLE

TEST Ground all output pins not under test.		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

TEST CIRCUITS

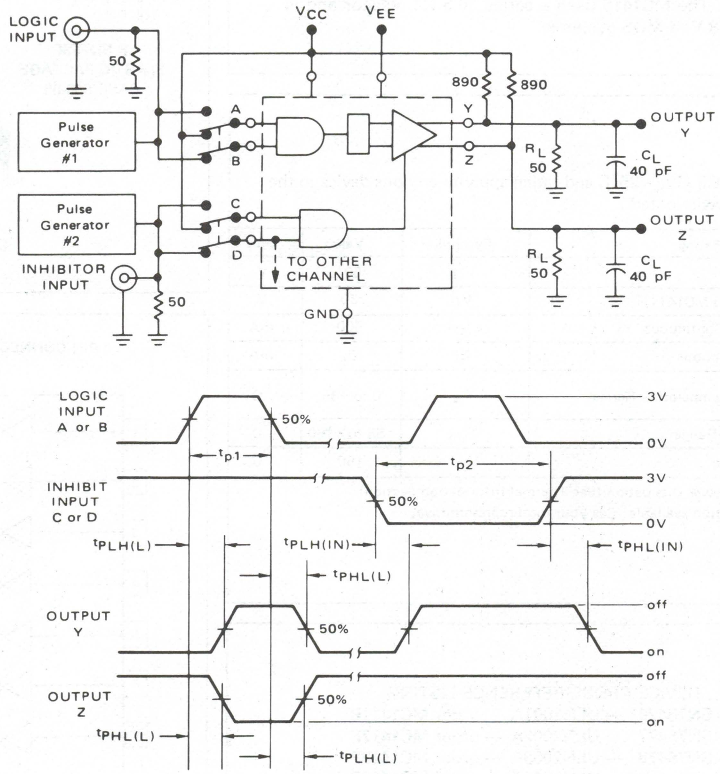
FIGURE 3 — I_{CC} and I_{EE}


VCC
VEE
ICC
IEE
VIH
VIL
See Table
VIH
See Table
VIL
VIH
VIL
See Table
1A
1B
1C
D
2C
2A
2B
1Y
1Z
2Y
2Z
GND

TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
I_{CC}(on)	Driver enabled	V_{IL}	V_{IH}
I_{EE}(on)	Driver enabled	V_{IL}	V_{IH}
I_{CC}(off)	Driver inhibited	V_{IL}	V_{IL}
I_{EE}(off)	Driver inhibited	V_{IL}	V_{IL}

FIGURE 4 — PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS


LOGIC INPUT
50
VCC
VEE
890
890
Pulse Generator #1
Pulse Generator #2
A
B
C
D
Y
Z
OUTPUT Y
OUTPUT Z
RL 50
CL 40 pF
RL 50
CL 40 pF
TO OTHER CHANNEL
INHIBITOR INPUT
50
GND
LOGIC INPUT A or B
50%
tp1
tp2
3V
0V
INHIBIT INPUT C or D
50%
3V
0V
tPLH(L)
tPLH(IN)
tPHL(IN)
tPHL(L)
OUTPUT Y
50%
off
on
OUTPUT Z
50%
off
on
tPHL(L)
tPLH(L)

NOTES:
1. The pulse generators have the following characteristics: z_o = 50 Ω, t_r = t_f = 10 ±5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

MC1411 (ULN2001A)
MC1412 (ULN2002A)
MC1413 (ULN2003A)
MC1416 (ULN2004A)

MOTOROLA

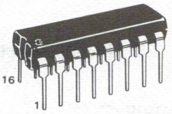
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington-connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

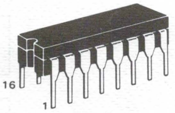
The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412 contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 kΩ series input resistor is well suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 kΩ resistor and is useful in 8–18 Volt MOS systems.

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 648-05



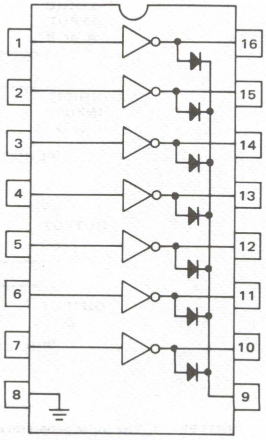
L SUFFIX
CERAMIC PACKAGE
CASE 620-02

MAXIMUM RATINGS ($T_A = 25°C$ and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Maximum Package Power Dissipation (See Thermal Information Section)
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



DEVICE CROSS-REFERENCE LISTING

9665 — SN75476* — ULN2001A — order MC1411P
9666 — SN75477 — ULN2002A — order MC1412P
9667 — SN75478 — ULN2003A — order MC1413P
9668 — ULN2004A — order MC1416P

*Similar

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Leakage Current (*V_O = 50 V, T_A = +70°C) All Types (*V_O = 50 V, T_A = +25°C) All Types (*V_O = 50 V, T_A = +70°C, V_I = 6.0 V) MC1412 (*V_O = 50 V, T_A = +70°C, V_I = 1.0 V) MC1416	I_{CEX}	 — — — —	 — — — —	 100 50 500 500	μA
Collector-Emitter Saturation Voltage (I_C = 350 mA, I_B = 500 μA) All Types (I_C = 200 mA, I_B = 350 μA) All Types (I_C = 100 mA, I_B = 250 μA) All Types	$V_{CE(sat)}$	 — — —	 1.1 0.95 0.85	 1.6 1.3 1.1	V
Input Current — On Condition (V_I = 17 V) MC1412 (V_I = 3.85 V) MC1413 (V_I = 5.0 V) MC1416 (V_I = 12 V) MC1416	$I_{I(on)}$	 — — — —	 0.85 0.93 0.35 1.0	 1.3 1.35 0.5 1.45	mA
Input Voltage — On Condition V_{CE} = 2.0 V, I_C = 300 mA) MC1412 V_{CE} = 2.0 V, I_C = 200 mA) MC1413 V_{CE} = 2.0 V, I_C = 250 mA) MC1413 V_{CE} = 2.0 V, I_C = 300 mA) MC1413 V_{CE} = 2.0 V, I_C = 125 mA) MC1416 V_{CE} = 2.0 V, I_C = 200 mA) MC1416 V_{CE} = 2.0 V, I_C = 275 mA) MC1416 V_{CE} = 2.0 V, I_C = 350 mA) MC1416	$V_{I(on)}$	 — — — — — — — —	 — — — — — — — —	 13 2.4 2.7 3.0 5.0 6.0 7.0 8.0	V
Input Current — Off Condition All Types (I_C = 500 μA, T_A = +70°C)	$I_{I(off)}$	50	100	—	μA
DC Current Gain MC1411 (V_{CE} = 2.0 V, I_C = 350 mA)	h_{FE}	1000	—	—	—
Input Capacitance	C_I	—	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)	t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current T_A = +25°C (V_R = 50 V) T_A = +70°C	I_R	—	—	50 100	μA
Clamp Diode Forward Voltage (I_F 350 mA)	V_F	—	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES – T_A = 25°C

FIGURE 1 – OUTPUT CURRENT versus INPUT VOLTAGE

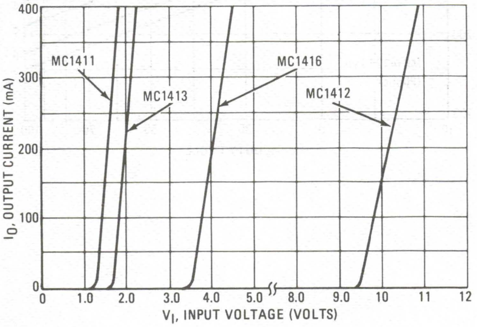
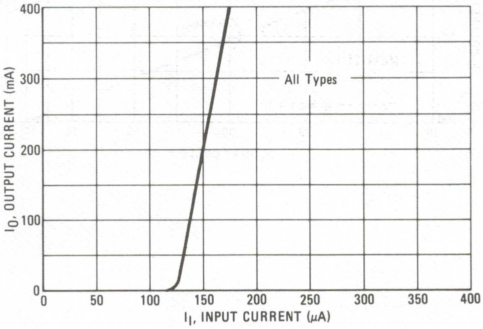


FIGURE 2 – OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES — $T_A = 25^{o}C$ (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

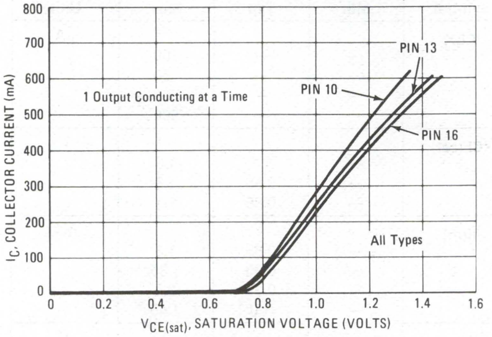


FIGURE 4 — INPUT CHARACTERISTICS — MC1412

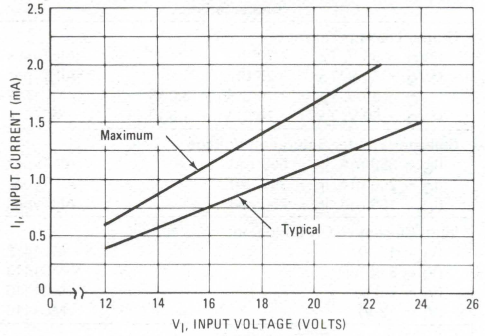


FIGURE 5 — INPUT CHARACTERISTICS — MC1413

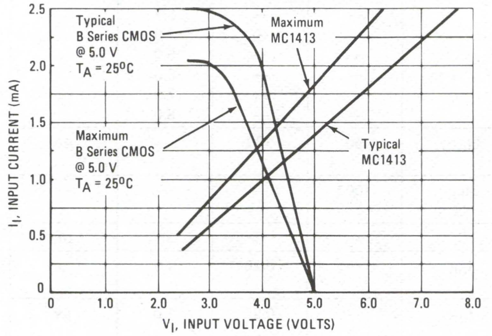


FIGURE 6 — INPUT CHARACTERISTICS — MC1416

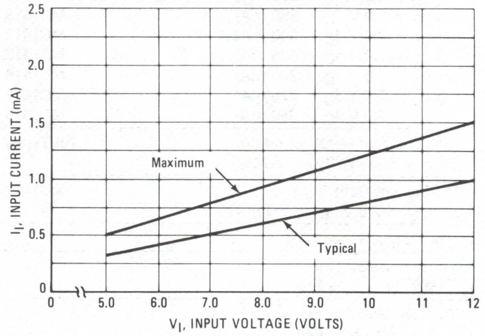


FIGURE 7 — MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) — CERAMIC

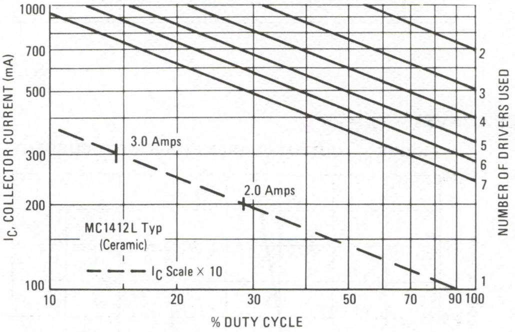
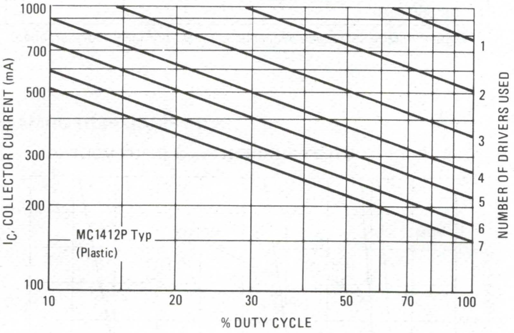
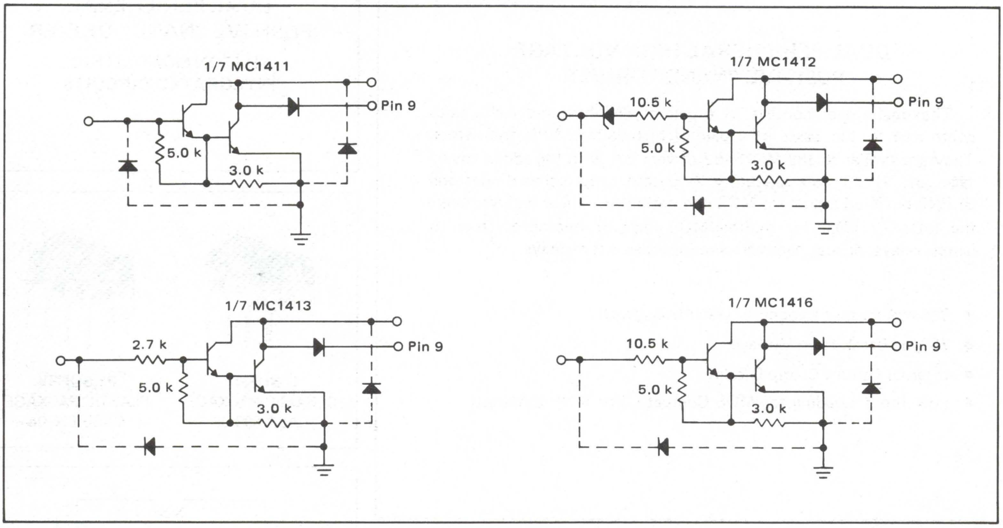


FIGURE 8 — MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) — PLASTIC



REPRESENTATIVE CIRCUIT SCHEMATICS


1/7 MC1411
Pin 9
5.0 k
3.0 k
1/7 MC1412
10.5 k
Pin 9
5.0 k
3.0 k
1/7 MC1413
2.7 k
Pin 9
5.0 k
3.0 k
1/7 MC1416
10.5 k
Pin 9
5.0 k
3.0 k

MC1472

MOTOROLA

DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER

The dual driver consists of a pair of PNP-buffered AND gates connected to the bases of a pair of high-voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)

CROSS REFERENCE

UDN-5712 – SN75475 – MC1472

MAXIMUM RATINGS (T_A = 25°C, Note 1).

Rating	Value	Unit
Supply Voltage	7.0	Volts
Input Voltage	5.5	Volts
Output Voltage	80	Volts
Clamp Voltage	80	Volts
Output Current (Continuous)	300	mA
Operating Junction Temperature Ceramic Package Plastic Package	 +175 +150	°C
Storage Temperature Range	-65 to +150	°C

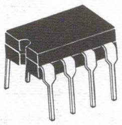
Note 1: "Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

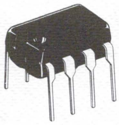
Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	°C
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

DUAL PERIPHERAL POSITIVE "NAND" DRIVER

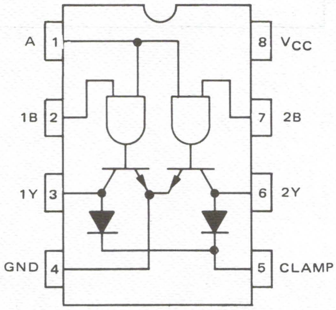
SILICON MONOLITHIC INTEGRATED CIRCUITS



U SUFFIX
CERAMIC PACKAGE
CASE 693-02



P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04



Positive Logic: $Y=AB^*$

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	H ("OFF" STATE)
H	L	H ("OFF" STATE)
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1472U	–	0 to +70°C	Ceramic DIP
MC1472P1	–	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (Unless otherwise noted min/max limits apply across the 0°C to 70°C temperature range with $4.5\ V \leq V_{CC} \leq 5.5\ V$. All typical values are for $T_A = 25°C$, $V_{CC} = 5.0$ Volts.)

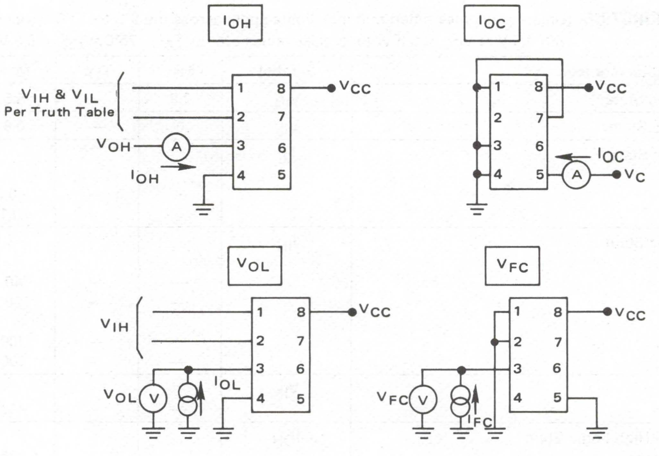
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	—	5.5	Vdc
Input Voltage — Low Logic State	V_{IL}	0	—	0.8	Vdc
Input Current — Low Logic State	I_{IL}				mA
(V_{IL} = 0.4 V)					
A Input		—	—	−0.3	
B Input				−0.15	
Input Current — High Logic State	I_{IH}				μA
(V_{IH} = 2.4 V)					
A Input		—	—	40	
B Input		—	—	20	
(V_{IH} = 5.5 V)					
A Input		—	—	200	
B Input		—	—	100	
Input Clamp Voltage	V_{IK}				V
(I_{CC} = −12 mA)		—	—	−1.5	
Output Leakage Current — High Logic State	I_{OH}				μA
(V_O = 70 V, See Test Figure)			—	100	
Output Voltage — Low Logic State	V_{OL}				V
(I_{OL} = 100 mA)		—	—	0.4	
(I_{OL} = 300 mA)		—	—	0.7	
Output Clamp Diode Leakage Current	I_{OC}				V
(V_C = 70 V, See Test Figure)		—	—	100	
Output Clamp Forward Voltage	V_{FC}				V
(I_{FC} = 300 mA, See Test Figure)		—	—	1.7	
Power Supply Current	I_{CC}				mA
(All Inputs at V_{IH})		—	—	70	
(All Inputs at V_{IL})		—	—	15	

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

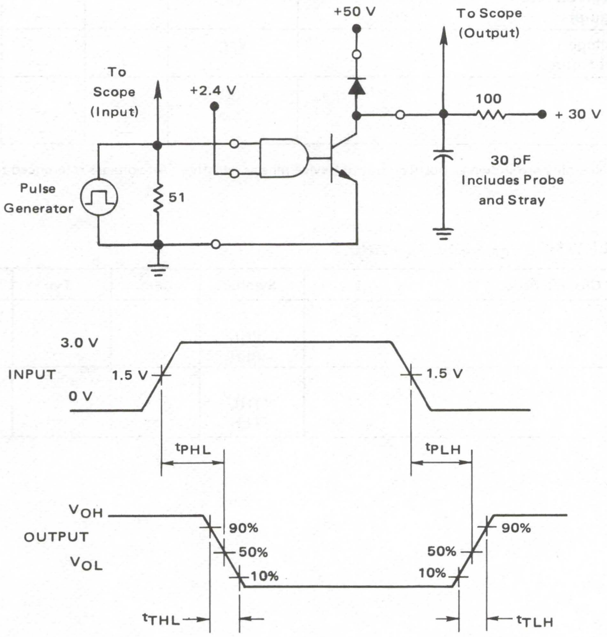
SWITCHING CHARACTERISTICS $V_{CC} = 5.0V$, $T_A = 25^oC$

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					
Output High to Low	t_{PHL}	–	–	1.0	μs
Output Low to High	t_{PLH}	–	–	0.75	
Output Transition Time					
Output High to Low	t_{THL}	–	–	0.1	μs
Output Low to High	t_{TLH}	–	–	0.1	

TEST CIRCUITS


IOH
VIH & VIL
Per Truth Table
VOH
A
IOH
VCC
IOC
VCC
IOC
A
VC
VOL
VIH
VOL
V
IOL
VCC
VFC
VFC
V
IFC
VCC
1
2
3
4
5
6
7
8

SWITCHING TEST CIRCUIT AND WAVEFORM


+50 V
To Scope
(Output)
To
Scope
(Input)
+2.4 V
100
+ 30 V
30 pF
Includes Probe
and Stray
Pulse
Generator
51
3.0 V
INPUT
1.5 V
0 V
1.5 V
tPHL
tPLH
VOH
OUTPUT
VOL
90%
50%
10%
50%
10%
90%
tTHL
tTLH

MOTOROLA

MC1488

QUAD MDTL LINE DRIVER
RS-232C

SILICON MONOLITHIC
INTEGRATED CIRCUIT

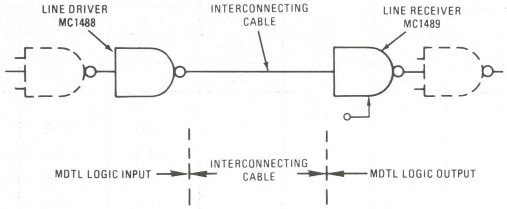
QUAD LINE DRIVER

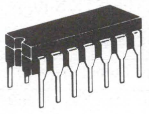
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

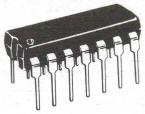
- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

TYPICAL APPLICATION


LINE DRIVER
MC1488
INTERCONNECTING
CABLE
LINE RECEIVER
MC1489
MDTL LOGIC INPUT
INTERCONNECTING
CABLE
MDTL LOGIC OUTPUT

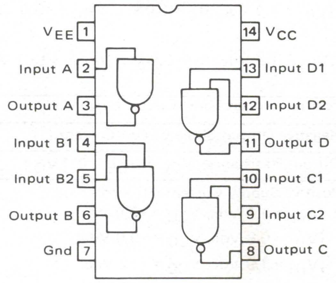


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA



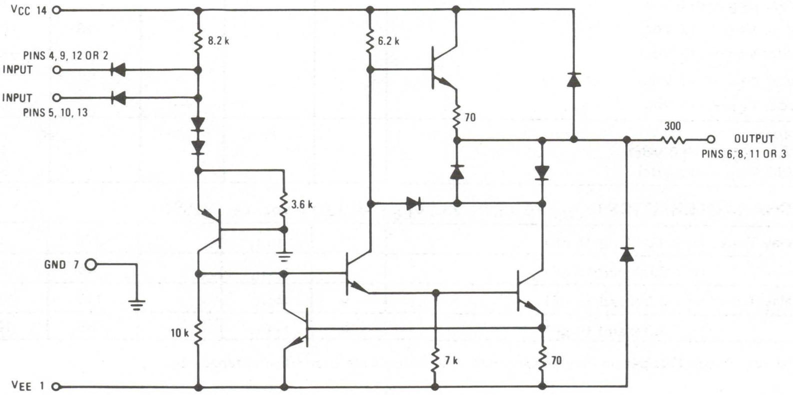
P SUFFIX
PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS


VEE 1
Input A 2
Output A 3
Input B1 4
Input B2 5
Output B 6
Gnd 7
14 VCC
13 Input D1
12 Input D2
11 Output D
10 Input C1
9 Input C2
8 Output C

CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)


VCC 14
PINS 4, 9, 12 OR 2
INPUT
INPUT
PINS 5, 10, 13
8.2 k
6.2 k
70
300
OUTPUT
PINS 6, 8, 11 OR 3
3.6 k
GND 7
10 k
7 k
70
VEE 1

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±10% Vdc, V_{EE} = −9.0 ±10% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (V_{IL} = 0)	1	I_{IL}	–	1.0	1.6	mA
Input Current – High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	–	–	10	µA
Output Voltage – High Logic State	2	V_{OH}				Vdc
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			+6.0	+7.0	–	
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			+9.0	+10.5	–	
Output Voltage – Low Logic State	2	V_{OL}				Vdc
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			-6.0	-7.0	–	
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			-9.0	-10.5	–	
Positive Output Short-Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current (1)	3	I_{OS-}	-6.0	-10	-12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\mid V_O \mid$ = ±2.0 V)	4	r_o	300	–	–	Ohms
Positive Supply Current ($R_I = \infty$)	5	I_{CC}				mA
(V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc)			–	+15	+20	
(V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc)			–	+4.5	+6.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc)			–	+19	+25	
(V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc)			–	+5.5	+7.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc)			–	–	+34	
(V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)			–	–	+12	
Negative Supply Current ($R_L = \infty$)	5	I_{EE}				
(V_{IH} = 1.9 Vdc, V_{EE} = -9.0 Vdc)			–	-13	-17	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -9.0 Vdc)			–	–	-500	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -12 Vdc)			–	-18	-23	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -12 Vdc)			–	–	-500	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -15 Vdc)			–	–	-34	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -15 Vdc)			–	–	-2.5	mA
Power Consumption		P_C				mW
(V_{CC} = 9.0 Vdc, V_{EE} = -9.0 Vdc)			–	–	333	
(V_{CC} = 12 Vdc, V_{EE} = -12 Vdc)			–	–	576	

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PLH}	–	275	350	ns
Fall Time	(z_l = 3.0 k and 15 pF)	6	t_{THL}	–	45	75	ns
Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PHL}	–	110	175	ns
Rise Time	(z_l = 3.0 k and 15 pF)	6	t_{TLH}	–	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

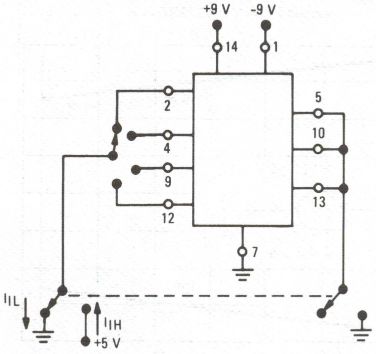

+9 V
-9 V
14
1
2
4
9
12
5
10
13
7
I_{IL}
I_{IH}
+5 V

FIGURE 2 – OUTPUT VOLTAGE

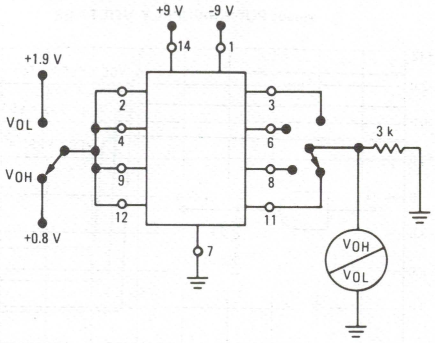

+9 V
-9 V
14
1
+1.9 V
V_{OL}
V_{OH}
+0.8 V
2
4
9
12
3
6
8
11
7
3 k
V_{OH}
V_{OL}

FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

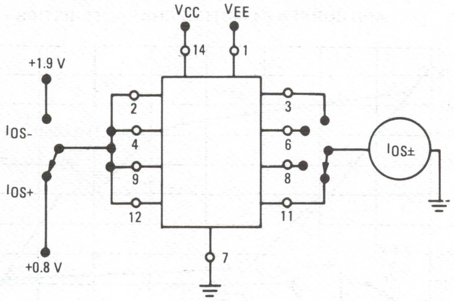

V_{CC}
V_{EE}
14
1
+1.9 V
I_{OS-}
I_{OS+}
+0.8 V
2
4
9
12
3
6
8
11
7
$I_{OS\pm}$

FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

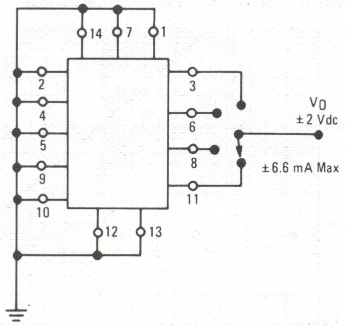

14
7
1
2
4
5
9
10
12
13
3
6
8
11
V_O
± 2 Vdc
± 6.6 mA Max

FIGURE 5 – POWER-SUPPLY CURRENTS

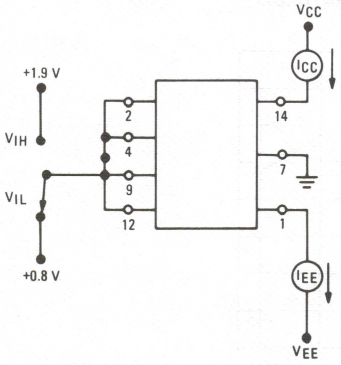
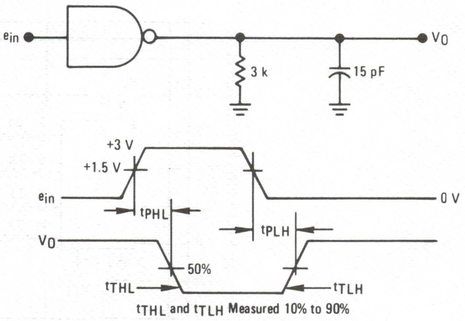

V_{CC}
I_{CC}
+1.9 V
V_{IH}
V_{IL}
+0.8 V
2
4
9
12
14
7
1
I_{EE}
V_{EE}

FIGURE 6 – SWITCHING RESPONSE


e_{in}
V_O
3 k
15 pF
+3 V
+1.5 V
e_{in}
0 V
t_{PHL}
t_{PLH}
V_O
50%
t_{THL}
t_{TLH}
t_{THL} and t_{TLH} Measured 10% to 90%

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

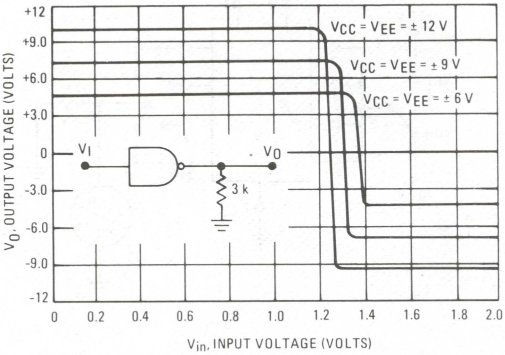


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

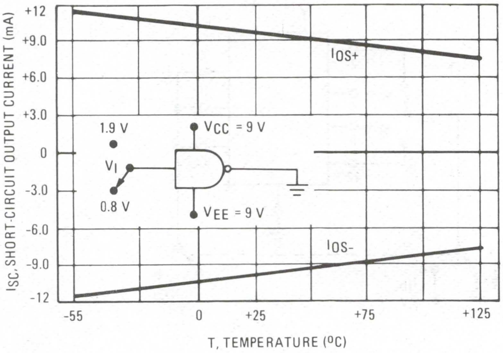


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

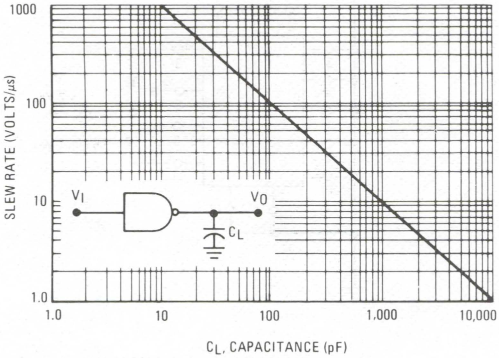


FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

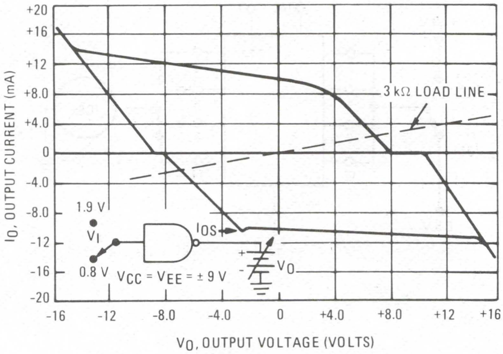
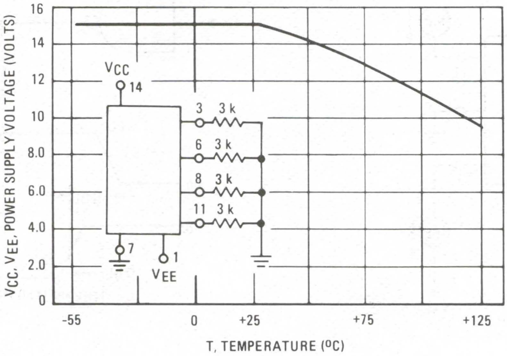


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



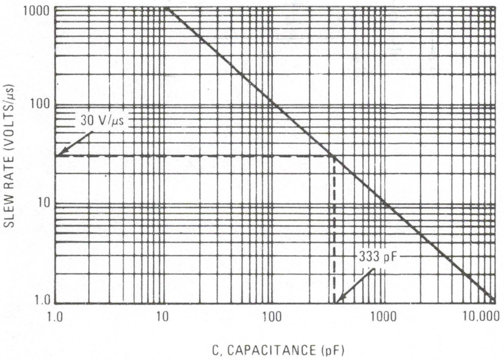
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

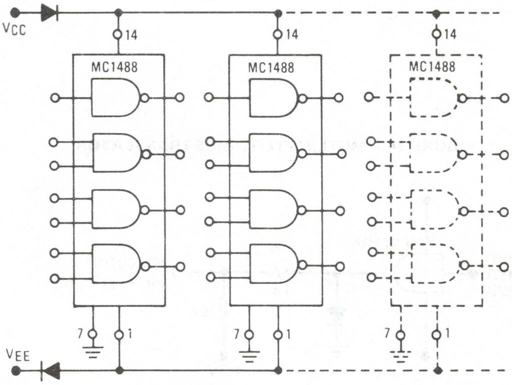
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

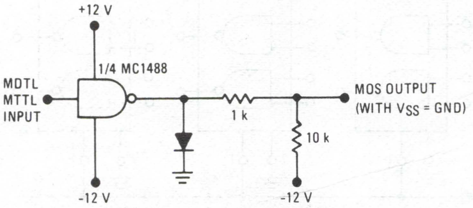
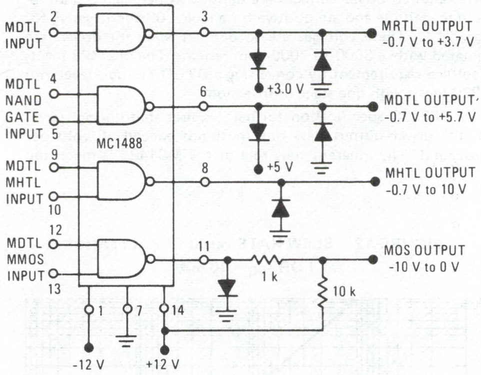

+12 V
1/4 MC1488
MDTL
MTTL
INPUT
1 k
10 k
MOS OUTPUT
(WITH V_{SS} = GND)
-12 V
-12 V

FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS


MDTL INPUT
2
3
MRTL OUTPUT -0.7 V to +3.7 V
+3.0 V
MDTL NAND GATE INPUT
4
5
6
MDTL OUTPUT -0.7 V to +5.7 V
MC1488
+5 V
MDTL MHTL INPUT
9
10
8
MHTL OUTPUT -0.7 V to 10 V
MDTL MMOS INPUT
12
13
11
1 k
10 k
MOS OUTPUT -10 V to 0 V
1
7
14
-12 V
+12 V

MOTOROLA

MC1489
MC1489A

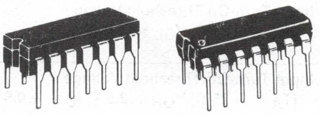
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

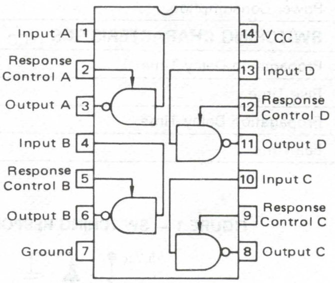
QUAD MDTL LINE RECEIVERS RS-232C

SILICON MONOLITHIC INTEGRATED CIRCUIT

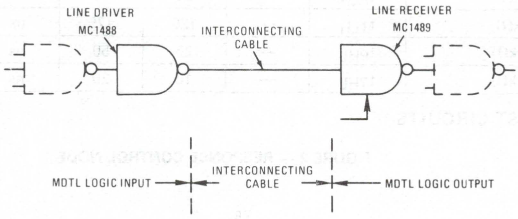


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

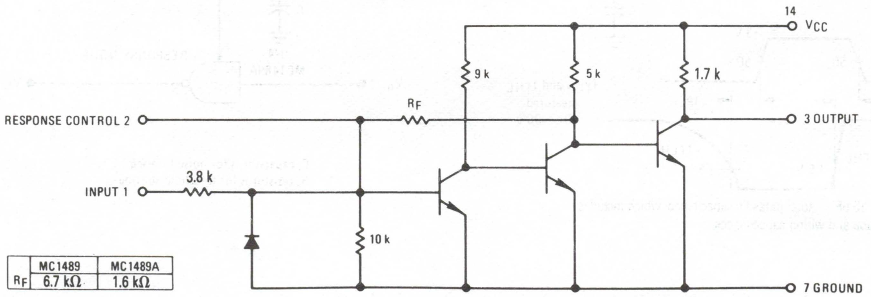
P SUFFIX
PLASTIC PACKAGE
CASE 646-05


Input A 1
Response Control A 2
Output A 3
Input B 4
Response Control B 5
Output B 6
Ground 7
14 VCC
13 Input D
12 Response Control D
11 Output D
10 Input C
9 Response Control C
8 Output C

TYPICAL APPLICATION


LINE DRIVER
MC1488
INTERCONNECTING CABLE
LINE RECEIVER
MC1489
MDTL LOGIC INPUT
INTERCONNECTING CABLE
MDTL LOGIC OUTPUT

EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)


14
VCC
9 k
5 k
1.7 k
RF
RESPONSE CONTROL 2
3 OUTPUT
3.8 k
INPUT 1
10 k
7 GROUND

	MC1489	MC1489A
RF	6.7 kΩ	1.6 kΩ

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±10%, T_A = 0 to +75°C unless otherwise noted)

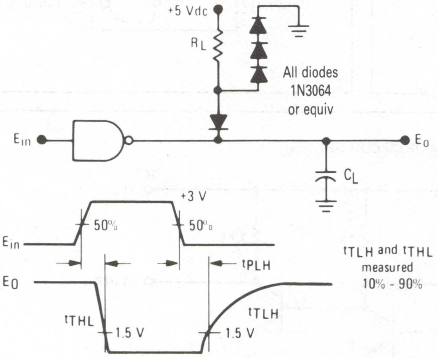
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = −25 Vdc) (V_{IL} = −3.0 Vdc)	I_{IL}	−3.6 −0.43	— —	−8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, $V_{OL} \leq 0.45$ V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, $V_{OH} \geq 2.5$ V, I_L = −0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = −0.5 mA) (Input Open Circuit, I_L = −0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	−3.0	−4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	—	10	20	ns

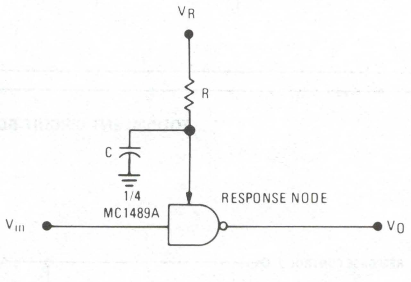
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

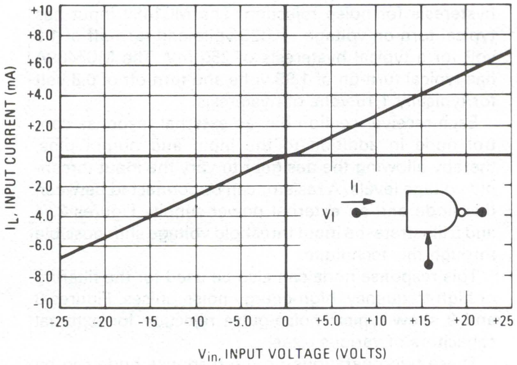


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

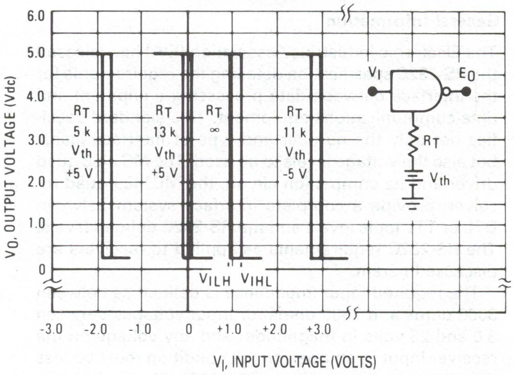


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

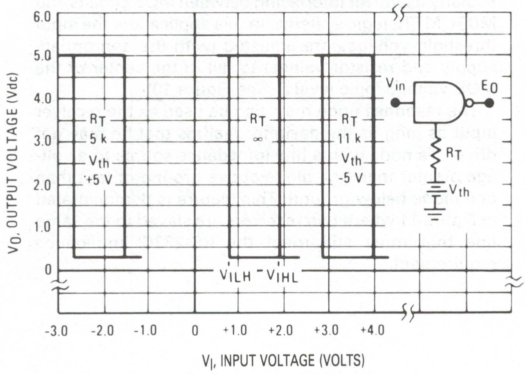


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

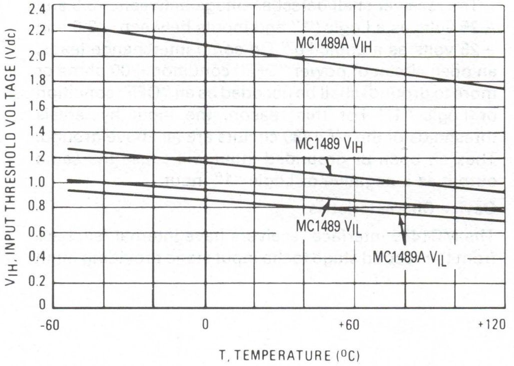
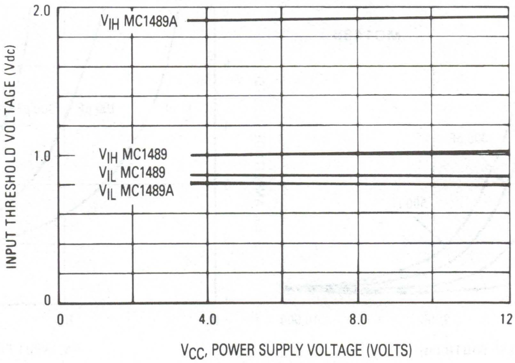


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

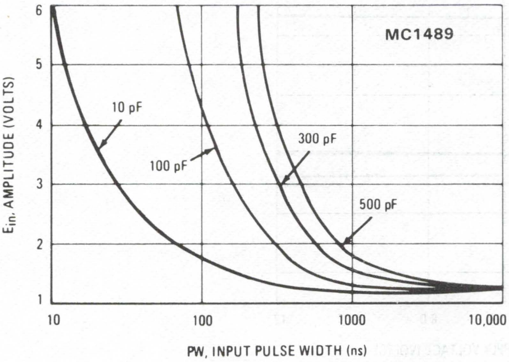
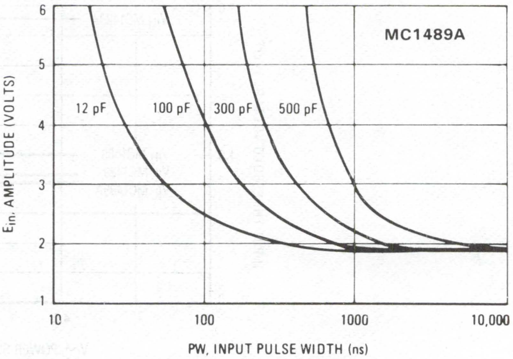


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

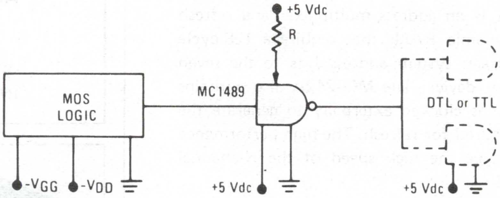
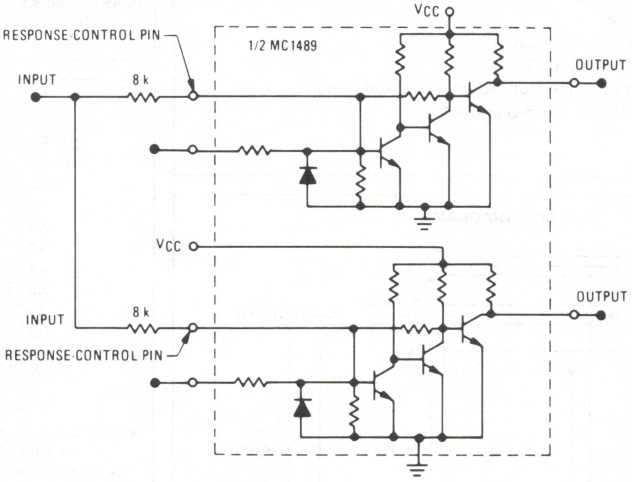

+5 Vdc
R
MOS LOGIC
MC1489
DTL or TTL
-VGG
-VDD
+5 Vdc
+5 Vdc

FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C


VCC
RESPONSE-CONTROL PIN
1/2 MC1489
INPUT
8 k
OUTPUT
VCC
OUTPUT
INPUT
8 k
RESPONSE-CONTROL PIN

MC3242A

MOTOROLA

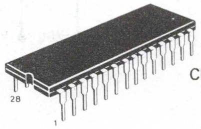
MEMORY ADDRESS MULTIPLEXER FOR 16K RAMs

The Motorola MC3242A is an address multiplexer and refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh. It multiplexes fourteen system address bits to the seven address pins of the memory device. The MC3242A also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

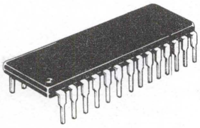
- Simplifies 16-Pin 16K Dynamic Memory Design
- Reduces Package Count
- 7-Bit Binary Counter for 128 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address Input to Output Delay —
  t_{AO} = 25 ns @ C_L = 250 pF
- Second Source to Intel 3242
  (Detect Zero Function Not Included and Additional Chip Enable Feature Added at Pin 15)

MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

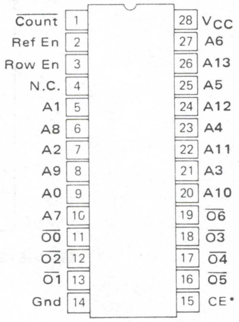
SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 733-03



P SUFFIX
PLASTIC PACKAGE
CASE 710-02


$\overline{\text{Count}}$ 1
Ref En 2
Row En 3
N.C. 4
A1 5
A8 6
A2 7
A9 8
A0 9
A7 10
$\overline{\text{O0}}$ 11
$\overline{\text{O2}}$ 12
$\overline{\text{O1}}$ 13
Gnd 14
28 V_{CC}
27 A6
26 A13
25 A5
24 A12
23 A4
22 A11
21 A3
20 A10
19 $\overline{\text{O6}}$
18 $\overline{\text{O3}}$
17 $\overline{\text{O4}}$
16 $\overline{\text{O5}}$
15 CE*

Note: A0 Through A6 Are Row Addresses
A7 Through A13 Are Column Addresses

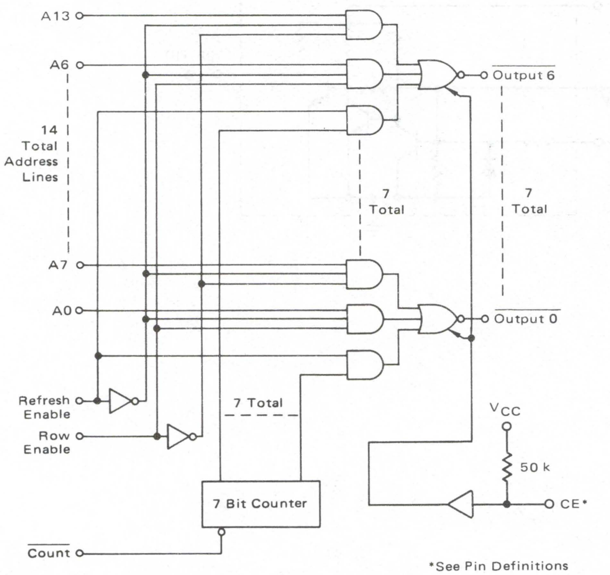
*See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A6)
L	L	Column Address (A7 through A13)

$\overline{\text{Count}}$ — Advances Internal Refresh Counter

LOGIC DIAGRAM


A13
A6
14 Total Address Lines
A7
A0
Refresh Enable
Row Enable
$\overline{\text{Output 6}}$
$\overline{\text{Output 0}}$
7 Total
7 Total
7 Total
7 Bit Counter
$\overline{\text{Count}}$
V_{CC}
50 k
CE*

*See Pin Definitions

ORDERING INFORMATION

Device	Temperature Range	Package
MC3242AL	0 to 75°C	Ceramic DIP
MC3242AP	0 to 75°C	Plastic DIP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +7.0	V
Output Voltage	V_O	−0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	—	−0.25	−0.40	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	—	—	10	μA
Input Voltage, Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	—	—	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	—	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = −1.0 mA)	V_{OH}	3.0	4.0	—	V
Input Clamp Voltage (I_{IK} = −12 mA)	V_{IK}	—	−0.8	−1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	—	80	125	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output	t_{AO}				ns
(Load = 1 TTL, C_L = 250 pF)		—	12	25	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		—	6.0	9.0	
Row Enable to Output	t_{OO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	27	41	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	12	27	
Refresh Enable to Output	t_{EO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	30	45	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7	14	27	
$\overline{\text{Count}}$ Pulse Width	$t_{W\overline{C}}$	30	—	—	ns
Counting Frequency	$f_{\overline{C}}$	5.0	10	—	MHz

FIGURE 1 – AC WAVEFORMS WITH MCM4116 NORMAL CYCLE

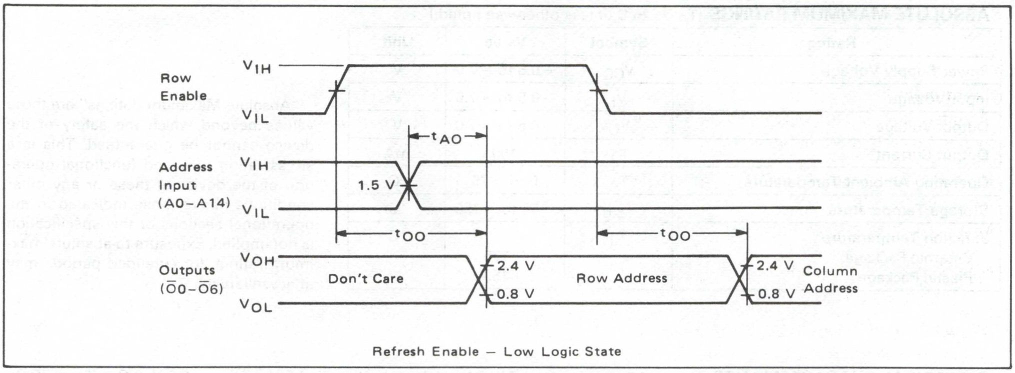
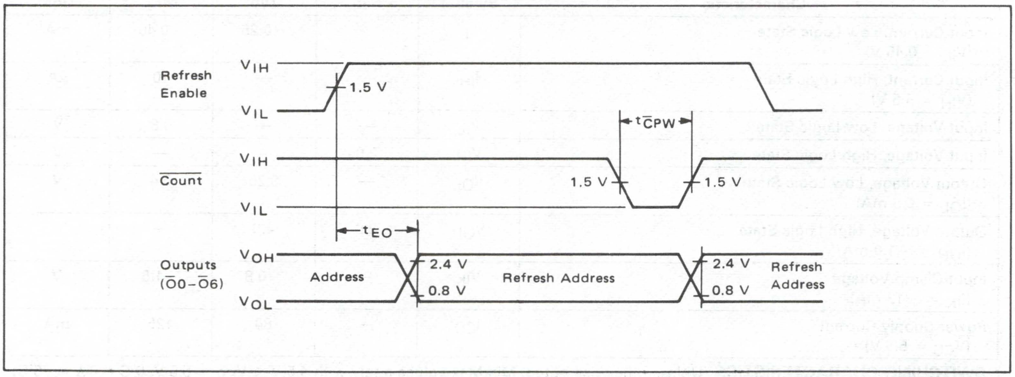

Row Enable
V_IH
V_IL
t_AO
Address Input (A0–A14)
V_IH
1.5 V
V_IL
t_OO
t_OO
Outputs (Ō0–Ō6)
V_OH
V_OL
Don't Care
2.4 V
0.8 V
Row Address
2.4 V
0.8 V
Column Address
Refresh Enable – Low Logic State

FIGURE 2 – REFRESH CYCLE


Refresh Enable
V_IH
V_IL
1.5 V
t_CPW
Count
V_IH
V_IL
1.5 V
1.5 V
t_EO
Outputs (Ō0–Ō6)
V_OH
V_OL
Address
2.4 V
0.8 V
Refresh Address
2.4 V
0.8 V
Refresh Address

TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

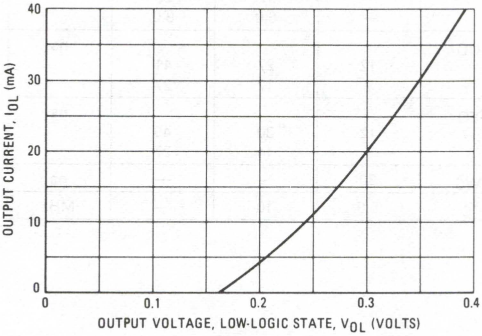
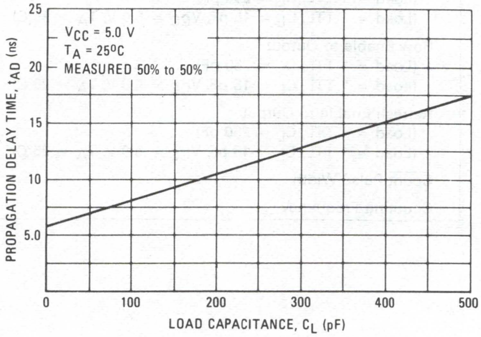


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



PIN DEFINITIONS

$\overline{\text{Count}}$ Input – Pin 1

Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2

Active high input which determines whether the MC3242A is in refresh mode (H) or address enable (L).

A0–A6 Inputs – Pins 9, 5, 7, 21, 23, 27

Row address inputs.

A7–A13 Inputs – Pins 10, 6, 8, 20, 22, 24, 26

Column address inputs.

$\overline{\text{O}}$0–$\overline{\text{O}}$6 Outputs – Pins 11, 12, 13, 18, 17, 16, 19

Address outputs to memories. Inverted with respect to address inputs.

Gnd – Pin 14

Power supply ground.

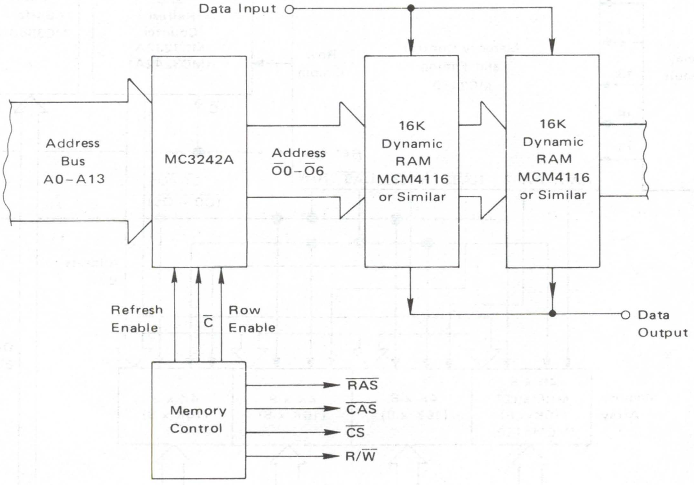
CE Input – Pin 15

Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state.

V_{CC} – Pin 28

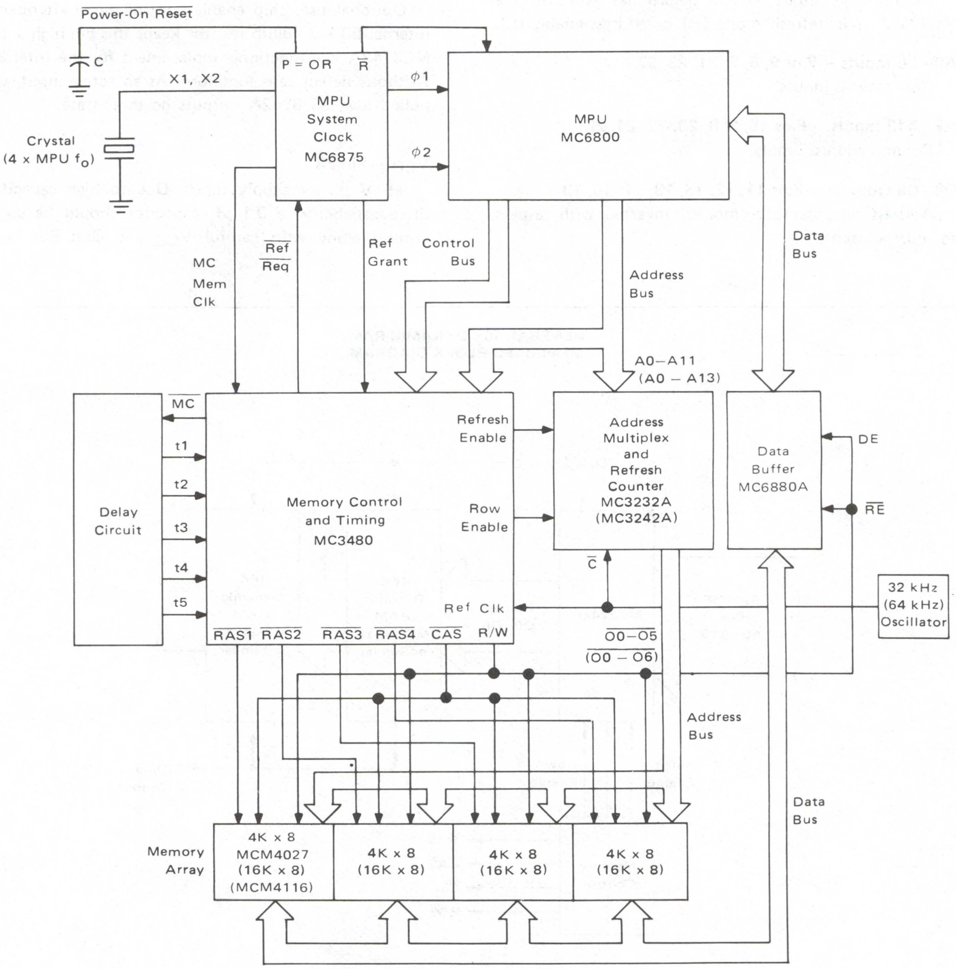
+5 V power supply input. Due to high capacitance drive capability, a 0.1 μF capacitor should be used to ground along with careful V_{CC} and Gnd Bus layout.

GENERAL 16K DYNAMIC RAM
SIMPLIFIED BLOCK DIAGRAM


Data Input
Address Bus A0–A13
MC3242A
Address $\overline{\text{O}}$0–$\overline{\text{O}}$6
16K Dynamic RAM MCM4116 or Similar
16K Dynamic RAM MCM4116 or Similar
Refresh Enable
$\overline{\text{C}}$
Row Enable
Data Output
Memory Control
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{CS}}$
R/$\overline{\text{W}}$

TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



Power-On Reset
C
X1, X2
Crystal (4 x MPU f$_o$)
P = OR
R
MPU System Clock MC6875
ϕ1
ϕ2
MPU MC6800
Data Bus
Address Bus
MC Mem Clk
Ref Req
Ref Grant
Control Bus
A0–A11 (A0 – A13)
Delay Circuit
MC
t1
t2
t3
t4
t5
Memory Control and Timing MC3480
Refresh Enable
Row Enable
Ref Clk
RAS1 RAS2 RAS3 RAS4 CAS R/W
Address Multiplex and Refresh Counter MC3232A (MC3242A)
Data Buffer MC6880A
DE
RE
C
32 kHz (64 kHz) Oscillator
O0–O5 (O0 – O6)
Address Bus
Data Bus
Memory Array
4K x 8 MCM4027 (16K x 8) (MCM4116)
4K x 8 (16K x 8)
4K x 8 (16K x 8)
4K x 8 (16K x 8)

MOTOROLA

MC3437

HEX BUS RECEIVER WITH INPUT HYSTERESIS

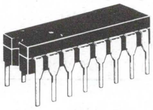
These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time – 20 ns (Typ)
- Direct Replacement for DM8837

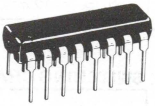
HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

16
(Top View)
1

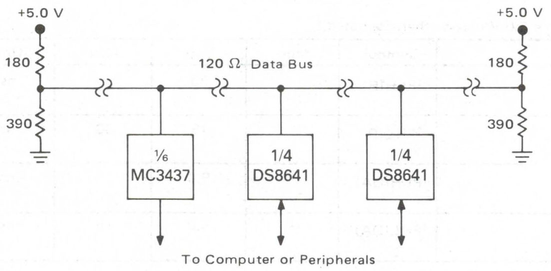


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

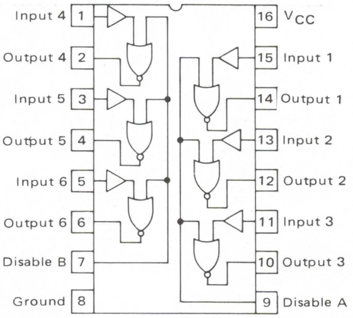


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 – TYPICAL APPLICATION


+5.0 V
+5.0 V
180
120 Ω Data Bus
180
390
390
1/6 MC3437
1/4 DS8641
1/4 DS8641
To Computer or Peripherals

PIN CONNECTIONS


Input 4 1
Output 4 2
Input 5 3
Output 5 4
Input 6 5
Output 6 6
Disable B 7
Ground 8
16 VCC
15 Input 1
14 Output 1
13 Input 2
12 Output 2
11 Input 3
10 Output 3
9 Disable A

TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leqslant T_A \leqslant 70^{\circ}C$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage – High Logic State ($V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$, $V_{OL} \leqslant 0.4\ V$)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$, $V_{OH} \geqslant 2.4\ V$)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Receiver Input Current	$I_{I(R)}$				µA
($V_{I(R)} = 4.0\ V$, $V_{CC} = 5.25\ V$)		–	15	50	
($V_{I(R)} = 4.0\ V$, $V_{CC} = 0\ V$)		–	1.0	50	
Disable Input Voltage – High Logic State ($V_{I(R)} = 0.5\ V$, $V_{OL} \leqslant 0.4\ V$, $I_{OL} = 16\ mA$)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage – Low Logic State ($V_{I(R)} = 0.5\ V$, $V_{OH} \geqslant 2.4\ V$, $I_{OH} = -400\ \mu A$)	$V_{IL(DA)}$	–	–	0.8	V
Output Voltage – High Logic State ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$)	V_{OH}	2.4	–	–	V
Output Voltage – Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$)	V_{OL}	–	0.25	0.4	V
Disable Input Current – High Logic State	$I_{IH(DA)}$				
($V_{IH(DA)} = 2.4\ V$)		–	–	80	µA
($V_{IH(DA)} = 5.5\ V$)		–	–	2.0	mA
Disable Input Current – Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.4\ V$)	$I_{IL(DA)}$	–	–	-3.2	mA
Output Short Circuit Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$, $V_{CC} = 5.25\ V$)	I_{OS}	-18	–	-55	mA
Power Supply Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$)	I_{CC}	–	45	65	mA
Input Clamp Diode Voltage ($I_{I(R)} = -12\ mA$, $I_{I(DA)} = -12\ mA$,	V_I	–	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0\ V$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH(DA)}$	–	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL(DA)}$	–	4.0	15	ns

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

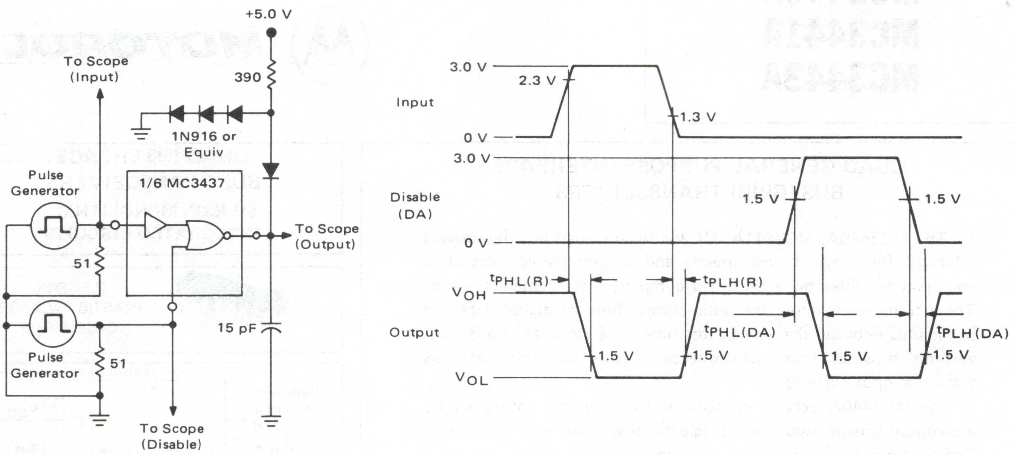
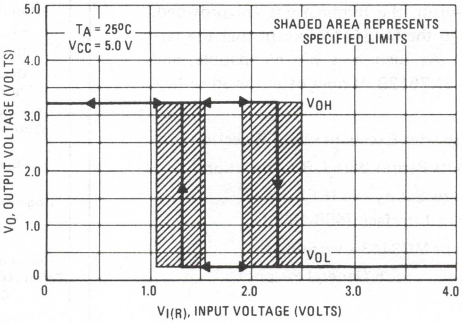
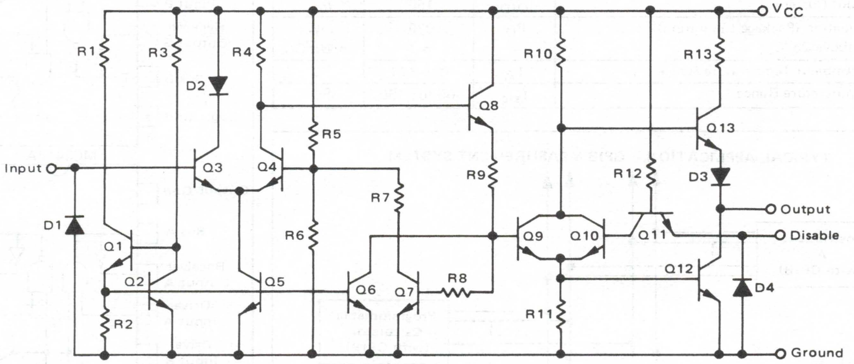

+5.0 V
To Scope (Input)
390
1N916 or Equiv
Pulse Generator
1/6 MC3437
To Scope (Output)
51
15 pF
Pulse Generator
51
To Scope (Disable)
3.0 V
2.3 V
Input
1.3 V
0 V
3.0 V
Disable (DA)
1.5 V
1.5 V
0 V
$t_{PHL(R)}$
$t_{PLH(R)}$
V_{OH}
Output
$t_{PHL(DA)}$
$t_{PLH(DA)}$
1.5 V
1.5 V
1.5 V
1.5 V
V_{OL}

FIGURE 3 – TYPICAL HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC

(1/6 Shown)


V_{CC}
R1
R3
R4
D2
R10
R13
Q8
Q13
R5
Input
Q3
Q4
R9
R12
D3
R7
Output
D1
R6
Q9
Q10
Q11
Disable
Q1
Q12
Q2
Q5
Q6
Q7
R8
D4
R11
R2
Ground

MC3440A
MC3441A
MC3443A

MOTOROLA

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A, MC3443A are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

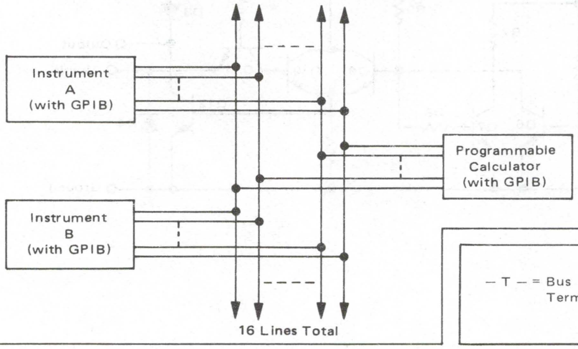
The MC3443A is identical to the MC3441A except that the terminations have been omitted. As such it is pin compatible, and functionally equivalent to the SN75138. It does offer the advantage of receiver input hysteresis.

- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations provided (except MC3443A version)
- Provides Electrical Compatibility with General-Purpose Interface Bus

MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

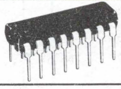
TYPICAL APPLICATION – GPIB MEASUREMENT SYSTEM


Instrument A (with GPIB)
Programmable Calculator (with GPIB)
Instrument B (with GPIB)

16 Lines Total

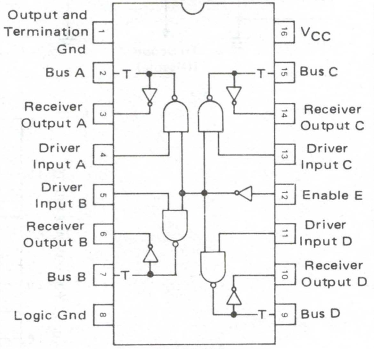
QUAD INTERFACE BUS TRANSCEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

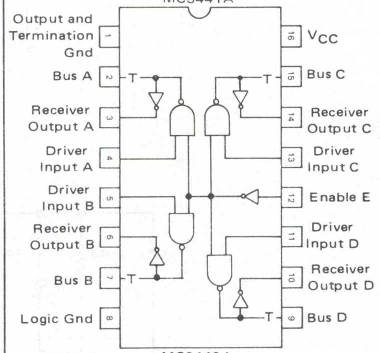


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

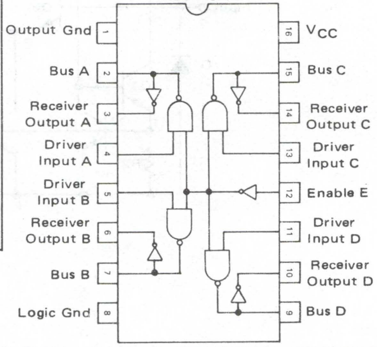
MC3440A


Output and Termination Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D
T

MC3441A


Output and Termination Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D
T

MC3443A


Output Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D

— T — = Bus Termination

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.5 V $\leqslant V_{CC} \leqslant$ 5.5 V and 0 $\leqslant T_A \leqslant$ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

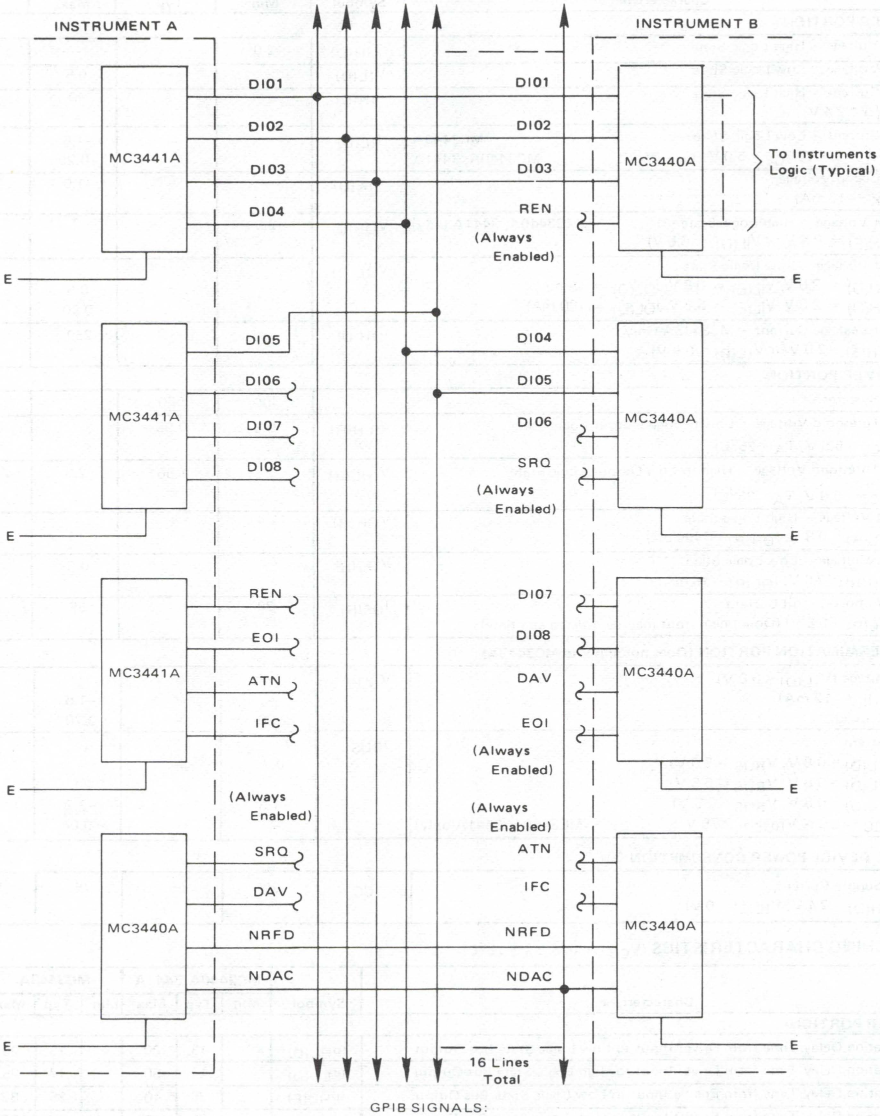
Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	–	–	40	µA
Input Current – Low Logic State MC3443A (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C) MC3440A, 3441A	$I_{IL(D)}$	–	–	–1.6 –0.25	mA
Input Clamp Voltage (I_{IK} = -12 mA)	$V_{IK(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) (MC3440A, 3441A only) ($V_{IH(E)}$ = 2.4 V or $V_{IL(D)}$ = 0.8 V)	$V_{OH(D)}$	2.5	–	–	V
Output Voltage – Low Logic State ($V_{IH(D)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) ($V_{IH(D)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 100 mA)	$V_{OL(D)}$	 – –	 – –	 0.5 0.80	V
Output Leakage Current – MC3443A Only ($V_{IH(E)}$ = 2.0 V or $V_{IL(D)}$ = 0.8 V)	$I_{OH(D)}$	–	–	250	µA
RECEIVER PORTION					
Input Hysteresis	–	400	580	–	mV
Input Threshold Voltage – Low to High Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{ILH(R)}$	0.8	0.98	–	V
Input Threshold Voltage – High to Low Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{IHL(R)}$	–	1.56	2.0	V
Output Voltage – High Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OH(R)}$ = -400 µA)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	–	0.5	V
Output Short-Circuit Current ($V_{IL(R)}$ = 0.8 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	-20	–	-55	mA
BUS TERMINATION PORTION (Does not apply to MC3443A)					
Bus Voltage ($V_{IL(D)}$ = 0.8 V) (I_{BUS} = –12 mA) (No Load)	V_{BUS}	 – 2.50	 – –	 –1.5 3.70	V
Bus Current ($V_{IL(D)}$ = 0.8 V, $V_{BUS} \geqslant$ 5.0 V) ($V_{IL(D)}$ = 0.8 V, $V_{BUS} \leqslant$ 5.5 V) ($V_{IL(D)}$ = 0.8 V, V_{BUS} = 0.5 V) (V_{CC} = 0, 0 $\leqslant V_{BUS} \leqslant$ 2.75 V) (MC3440A, 3441A only)	I_{BUS}	 0.7 – -1.3 –	 – – – –	 – 2.5 –3.2 +0.04	mA
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current ($V_{IH(D)}$ = 2.4 V, $V_{IL(E)}$ = 0 V)	I_{CC}	30	56	75	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	MC3440A,3441A			MC3443A			Unit
		Min	Typ	Max	Min	Typ	Max	
DRIVER PORTION								
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	13	30	–	13	25	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	17	30	–	17	25	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	25	40	–	25	32	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	25	40	–	25	32	ns
RECEIVER PORTION								
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	15	30	–	15	22	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	15	30	–	15	22	ns

(1) 12 k resistor from the bus terminal to V_{CC} required on the MC3443A version.

GENERAL PURPOSE INTERFACE BUS APPLICATION


INSTRUMENT A
INSTRUMENT B
MC3441A
MC3441A
MC3441A
MC3440A
MC3440A
MC3440A
MC3440A
MC3440A
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
REN
EOI
ATN
IFC
SRQ
DAV
NRFD
NDAC
(Always Enabled)
To Instruments Logic (Typical)
E
16 Lines Total

GPIB SIGNALS:

8 Line Data Bus: DIO1 – DIO8

5 General Interrupt Transfer Control Bus:
- REN – Remote Enable
- SRQ – Service Request
- EOI – End or Identify
- ATN – Attention
- IFC – Interface Clear

3 Data Byte Transfer Control Bus
- DAV – Data Valid
- NRFD – Not Ready for Data
- NDAC – Not Data Accepted

16 Total Signal Lines

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

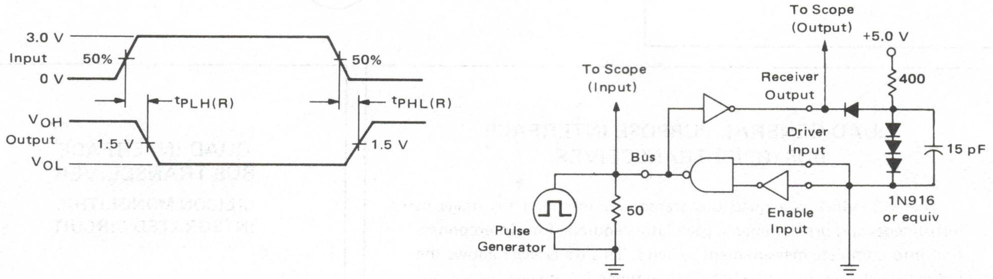

3.0 V
Input
50%
0 V
50%
$t_{PLH(R)}$
$t_{PHL(R)}$
V_{OH}
Output
1.5 V
1.5 V
V_{OL}
To Scope (Output)
+5.0 V
To Scope (Input)
Receiver Output
400
Driver Input
Bus
15 pF
50
Pulse Generator
Enable Input
1N916 or equiv

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

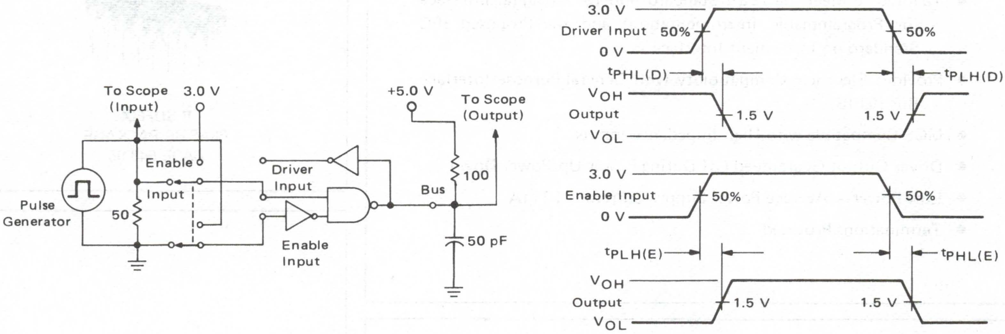
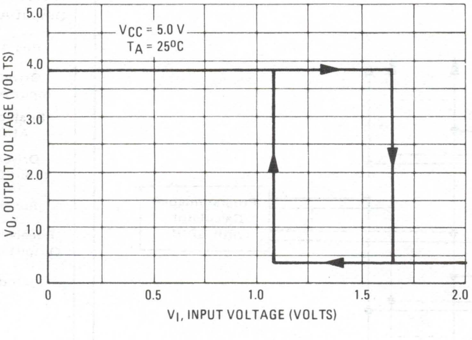

3.0 V
Driver Input
50%
50%
0 V
$t_{PHL(D)}$
$t_{PLH(D)}$
V_{OH}
Output
1.5 V
1.5 V
V_{OL}
3.0 V
Enable Input
50%
50%
0 V
$t_{PLH(E)}$
$t_{PHL(E)}$
V_{OH}
Output
1.5 V
1.5 V
V_{OL}
To Scope (Input)
3.0 V
Enable
Input
Pulse Generator
50
+5.0 V
To Scope (Output)
Driver Input
100
Bus
Enable Input
50 pF

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



MC3446A

MOTOROLA

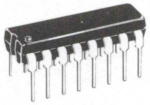
QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVER

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided

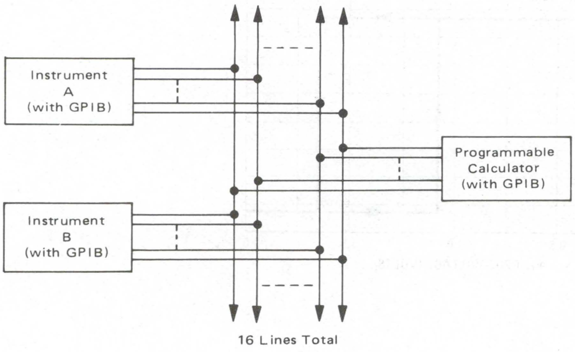
QUAD INTERFACE BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

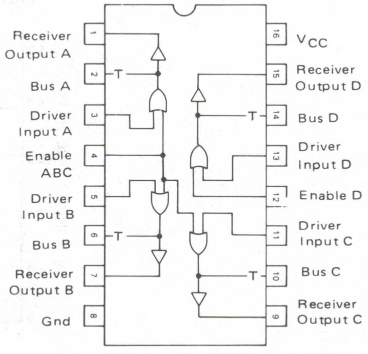


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

TYPICAL MEASUREMENT SYSTEM APPLICATION


Instrument A (with GPIB)
Instrument B (with GPIB)
Programmable Calculator (with GPIB)
16 Lines Total

PIN CONNECTIONS


Receiver Output A
Bus A
Driver Input A
Enable ABC
Driver Input B
Bus B
Receiver Output B
Gnd
VCC
Receiver Output D
Bus D
Driver Input D
Enable D
Driver Input C
Bus C
Receiver Output C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
T
T
T
T

— T — = Bus Termination

MAXIMUM RATINGS ($T_A = 25^oC$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	^oC
Operating Ambient Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $4.5\ V \leqslant V_{CC} \leqslant 5.5\ V$ and $0 \leqslant T_A \leqslant 70^oC$, typical values are at $T_A = 25^oC$, $V_{CC} = 5.0\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State ($V_{IH} = 2.4\ V$)	$I_{IH(D)}$	–	5.0	40	µA
Input Current – Low Logic State ($V_{IL} = 0.4\ V$, $V_{CC} = 5.0\ V$, $T_A = 25^oC$)	$I_{IL(D)}$	–	-0.2	-0.25	mA
Input Clamp Voltage ($I_{IK} = -12\ mA$)	$V_{IK(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) ($V_{IH(S)} = 2.4\ V$ or $V_{IH(D)} = 2.0\ V$)	$V_{OH(D)}$	2.5	3.3	3.7	V
Output Voltage – Low Logic State ($V_{IL(S)} = 0.8\ V$, $V_{IL(D)} = 0.8\ V$, $I_{OL(D)} = 48\ mA$)	$V_{OL(D)}$	–	–	0.5	
Input Breakdown Current ($V_{I(D)} = 5.5\ V$)	$I_{IB(D)}$	–	–	1.0	mA
RECEIVER PORTION					
Input Hysteresis	–	400	625	–	mV
Input Threshold Voltage – Low to High Output Logic State	$V_{ILH(R)}$	–	1.66	2.0	V
Input Threshold Voltage – High to Low Output Logic State	$V_{IHL(R)}$	0.8	1.03	–	V
Output Voltage – High Logic State ($V_{IH(R)} = 2.0\ V$, $I_{OH(R)} = -400\ \mu A$)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IL(R)} = 0.8\ V$, $I_{OL(R)} = 8.0\ mA$)	$V_{OL(R)}$	–	–	0.5	V
Output Short-Circuit Current ($V_{IH(R)} = 2.0\ V$) (Only one output may be shorted at a time)	$I_{OS(R)}$	4.0	–	14	mA
BUS LOAD CHARACTERISTICS					
Bus Voltage ($V_{IH(E)} = 2.4\ V$)	$V_{(BUS)}$	2.5	3.3	3.7	V
($I_{BUS} = -12\ mA$)		–	–	-1.5	
Bus Current ($V_{IH(O)} = 2.4\ V$, $V_{BUS} \geqslant 5.0\ V$)	$I_{(BUS)}$	0.7	–	–	mA
($V_{IH(D)} = 2.4\ V$, $V_{BUS} = 0.5\ V$)		-1.3	–	-3.2	
($V_{BUS} \leqslant 5.5\ V$)		–	–	2.5	
($V_{CC} = 0$, $0\ V \leqslant V_{BUS} \leqslant 2.75\ V$)		–	–	0.04	
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current	I_{CC}				mA
(All Drivers OFF)		–	12	19	
(All Drivers ON)		–	32	40	

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\ V$, $T_A = 25^oC$)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	–	50	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	–	40	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	–	50	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	–	50	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	–	50	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	–	40	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

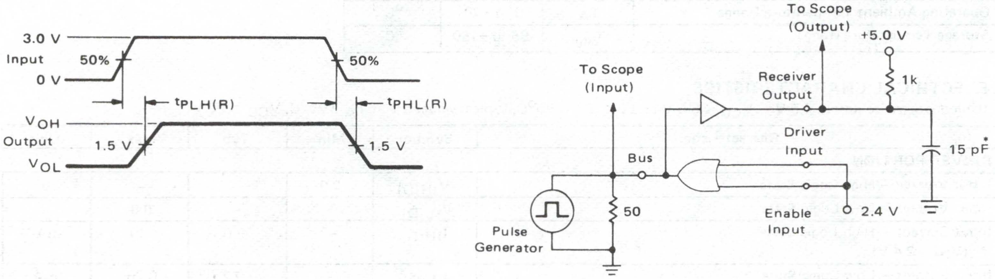
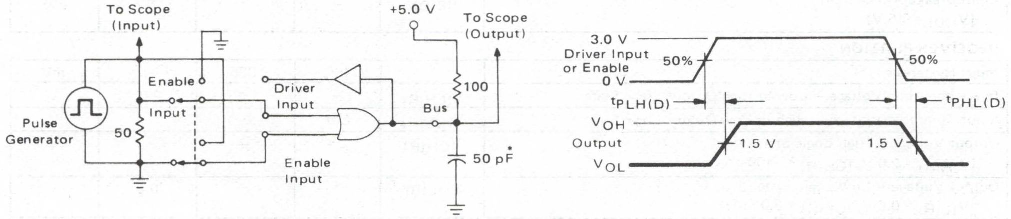

3.0 V
Input
0 V
50%
50%
tPLH(R)
tPHL(R)
VOH
Output
VOL
1.5 V
1.5 V
To Scope
(Output)
+5.0 V
1k
To Scope
(Input)
Receiver
Output
Driver
Input
15 pF*
Bus
50
Pulse
Generator
Enable
Input
2.4 V

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)


To Scope
(Input)
+5.0 V
To Scope
(Output)
Enable
Driver
Input
Input
100
Bus
Pulse
Generator
50
Enable
Input
50 pF*
3.0 V
Driver Input
or Enable
0 V
50%
50%
tPLH(D)
tPHL(D)
VOH
Output
VOL
1.5 V
1.5 V

* Includes Probe and Jig Capacitance

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

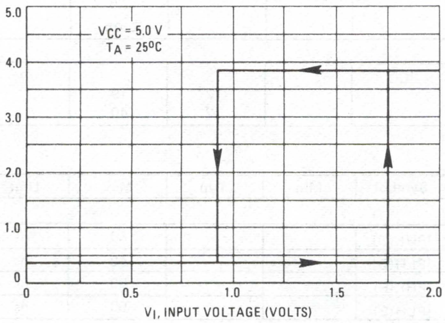
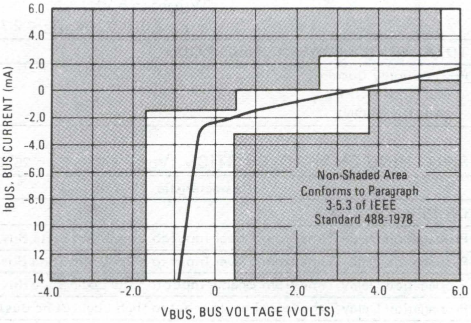


FIGURE 4 – TYPICAL BUS LOAD LINE



MOTOROLA

MC3447

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

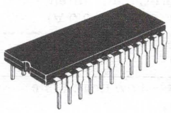
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

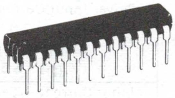
- Low Power — Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided

OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

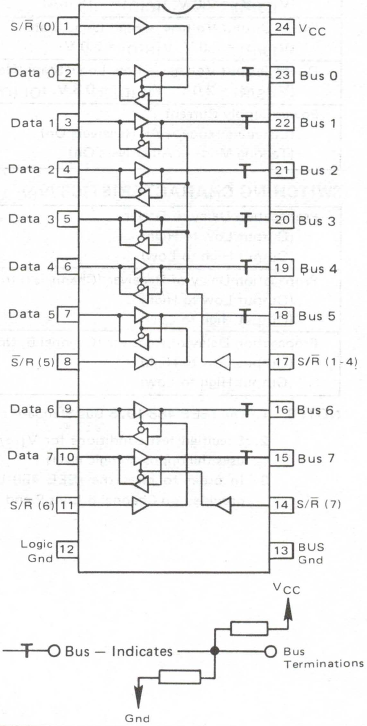


L SUFFIX
CERAMIC PACKAGE
CASE 623-05



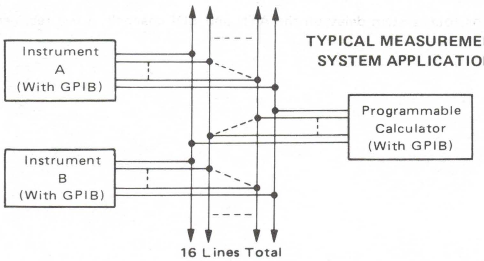
P3 SUFFIX
PLASTIC PACKAGE
CASE 724-02

PIN ASSIGNMENTS


S/R̄ (0) 1
24 VCC
Data 0 2
23 Bus 0
Data 1 3
22 Bus 1
Data 2 4
21 Bus 2
Data 3 5
20 Bus 3
Data 4 6
19 Bus 4
Data 5 7
18 Bus 5
S̄/R (5) 8
17 S/R̄ (1-4)
Data 6 9
16 Bus 6
Data 7 10
15 Bus 7
S/R̄ (6) 11
14 S/R̄ (7)
Logic Gnd 12
13 BUS Gnd
VCC
Bus — Indicates
Bus Terminations
Gnd

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C


Instrument A (With GPIB)
Instrument B (With GPIB)
Programmable Calculator (With GPIB)
16 Lines Total

TYPICAL MEASUREMENT SYSTEM APPLICATION

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V ≤ V_{CC} ≤ 5.50 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic — Note 2	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/\overline{R})}$ = 0.8 V)	$V_{(Bus)}$	2.5	—	3.7	
($I_{(Bus)}$ = −12 mA)	$V_{IC(Bus)}$	—	—	−1.5	
Bus Current	$I_{(Bus)}$				mA
(5.0 V ≤ $V_{(Bus)}$ ≤ 5.5 V)		0.7	—	2.5	
($V_{(Bus)}$ = 0.5 V)		−1.3	—	−3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(Bus)}$ ≤ 2.75 V)		—	—	+0.04	
Receiver Input Hysteresis ($V_{I(S/\overline{R})}$ = 0.8 V)	—	400	600	—	mV
Receiver Input Threshold					V
($V_{I(S/\overline{R})}$ = 0.8 V) Low to High	$V_{ILH(R)}$	—	1.6	2.0	
High to Low	$V_{IHL(R)}$	0.8	1.0	—	
Receiver Output Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = −200 μA, $V_{(Bus)}$ = 2.0 V)	$V_{OH(R)}$	2.4	—	—	V
Receiver Output Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, ($V_{(Bus)}$ = 0.8 V	$V_{OL(R)}$	—	—	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)	$I_{OS(R)}$	−4.0	—	−20	mA
Driver Input Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IH(D)}$	2.0	—	—	V
Driver Input Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IL(D)}$	—	—	0.8	V
Driver Input Current — Data Pins ($V_{I(S/\overline{R})}$ = 2.0 V)					μA
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)	$I_{I(D)}$	−100	—	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	—	—	200	
Input Current — Send/Receive					μA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)	$I_{I(S/\overline{R})}$	−250	—	20	
($V_{I(S/\overline{R})}$ = 5.5 V)	$I_{IB(S/\overline{R})}$	—	—	100	
Driver Input Clamp Voltage ($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)	$V_{IC(D)}$	—	—	−1.5	V
Driver Output Voltage — High Logic State ($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	—	—	V
Driver Output Voltage — Low Logic State (Note 1) ($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	—	—	0.5	V
Power Supply Current					mA
(Listening Mode — All Receivers On)	I_{CCL}	—	30	45	
(Talking Mode — All Drivers On)	I_{CCH}	—	75	95	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	—	7.0	15	
(Output High to Low)	$t_{PHL(D)}$	—	16	30	
Propagation Delay of Receiver (Channels 0 to 5, 7)					ns
(Output Low to High)	$t_{PLH(R)}$	—	28	50	
(Output High to Low)	$t_{PHL(R)}$	—	15	30	
Propagation Delay of Receiver (Channel 6, Note 3)					ns
(Output Low to High)	$t_{PLH(R)}$	—	17	30	
(Output High to Low)	$t_{PHL(R)}$	—	12	22	

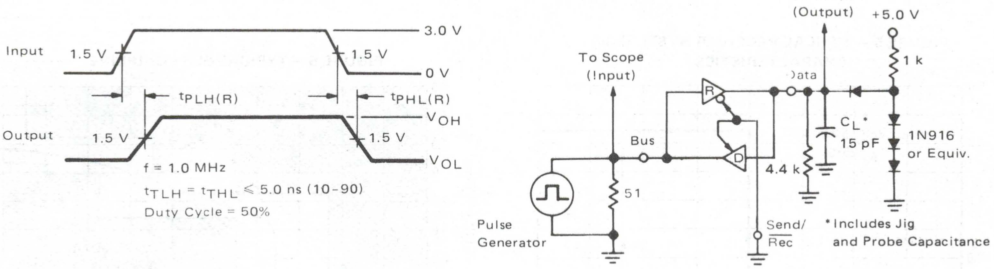
NOTES:
1. The IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
2. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(\overline{S}/R)}$ uses the opposite logic levels.
3. In order to meet the IEEE 488-1978 standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (pins 9 and 16).

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	15	30	
Third State to Logic High	$t_{PZH(R)}$	–	15	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	15	25	
Third State to Logic Low	$t_{PZL(R)}$	–	10	25	
Propagation Delay Time – Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ(D)}$	–	13	25	
Third State to Logic Low	$t_{PZL(D)}$	–	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

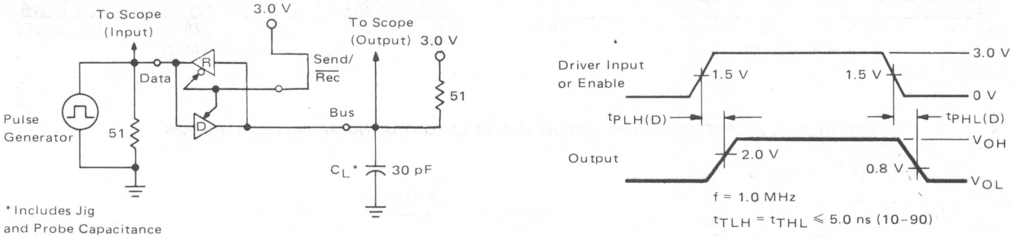
FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)


Input
1.5 V
1.5 V
3.0 V
0 V
tPLH(R)
tPHL(R)
Output
1.5 V
1.5 V
VOH
VOL
To Scope (Output)
+5.0 V
1 k
To Scope (Input)
Data
R
D
Bus
CL*
15 pF
4.4 k
1N916 or Equiv.
51
Pulse Generator
Send/Rec

f = 1.0 MHz
$t_{TLH} = t_{THL} \leq$ 5.0 ns (10–90)
Duty Cycle = 50%

*Includes Jig and Probe Capacitance

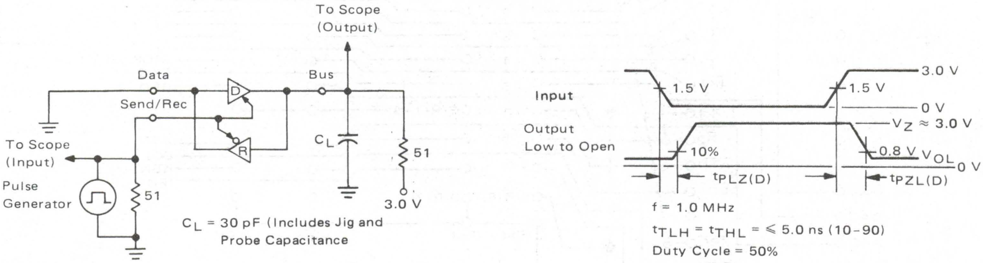
FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)


To Scope (Input)
3.0 V
To Scope (Output)
3.0 V
Send/Rec
Data
R
D
Bus
51
Pulse Generator
51
CL*
30 pF
Driver Input or Enable
1.5 V
1.5 V
3.0 V
0 V
tPLH(D)
tPHL(D)
VOH
Output
2.0 V
0.8 V
VOL

*Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} \leq$ 5.0 ns (10–90)
Duty Cycle = 50%

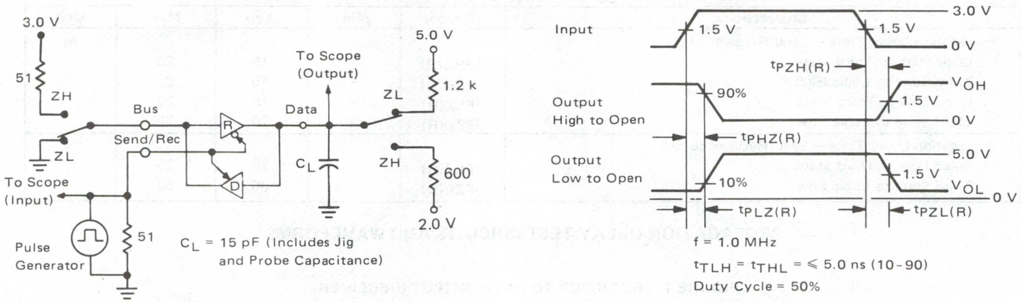
FIGURE 3 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO BUS OUTPUT (DRIVER)


To Scope (Output)
Data
Bus
Send/Rec
D
R
CL
51
3.0 V
To Scope (Input)
Pulse Generator
51
Input
1.5 V
1.5 V
3.0 V
0 V
Output Low to Open
VZ ≈ 3.0 V
10%
0.8 V
VOL
0 V
tPLZ(D)
tPZL(D)

C_L = 30 pF (Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} = \leq$ 5.0 ns (10–90)
Duty Cycle = 50%

FIGURE 4 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO DATA OUTPUT (RECEIVER)


3.0 V
51
ZH
Bus
Send/Rec
ZL
To Scope (Input)
Pulse Generator
51
R
D
Data
To Scope (Output)
5.0 V
1.2 k
ZL
ZH
600
2.0 V
CL
Input
1.5 V
1.5 V
3.0 V
0 V
tPZH(R)
VOH
1.5 V
0 V
Output High to Open
90%
tPHZ(R)
Output Low to Open
5.0 V
1.5 V
VOL
0 V
10%
tPLZ(R)
tPZL(R)

C_L = 15 pF (Includes Jig and Probe Capacitance)

f = 1.0 MHz

$t_{TLH} = t_{THL} = \leqslant 5.0$ ns (10-90)

Duty Cycle = 50%

FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

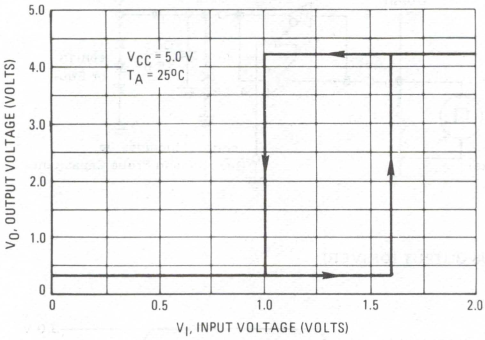


FIGURE 6 – TYPICAL BUS LOAD LINE

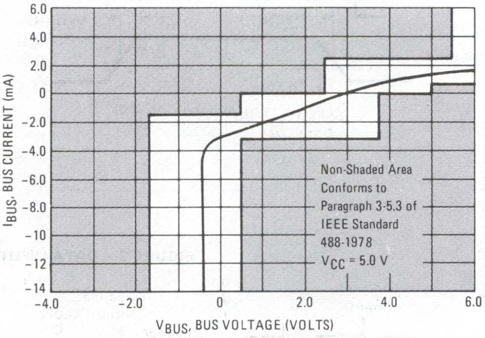


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

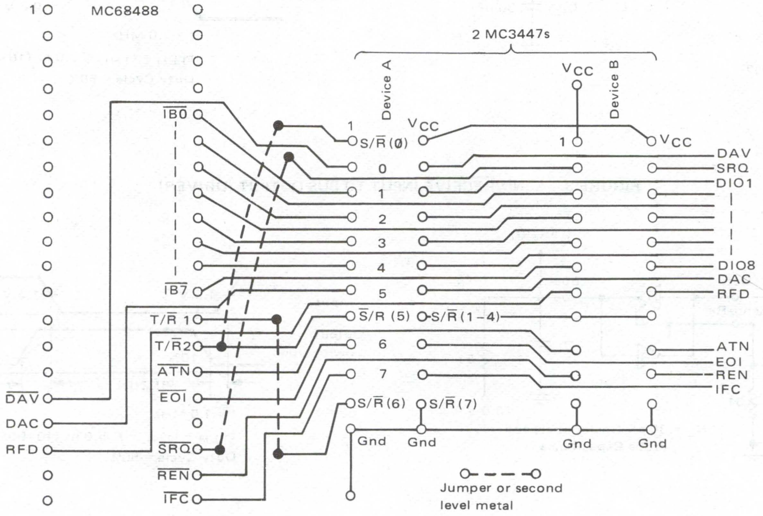
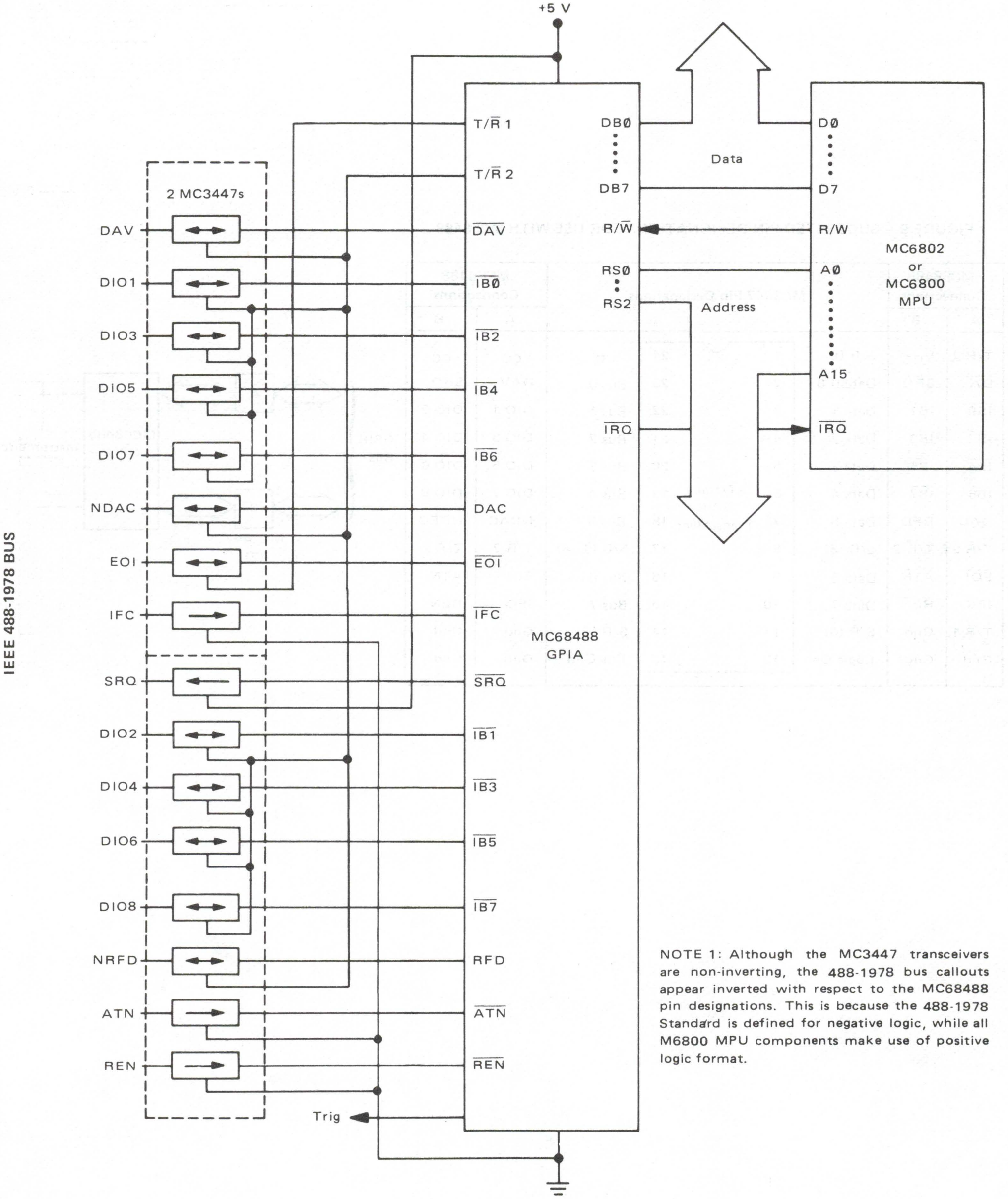

1
MC68488
2 MC3447s
Device A
Device B
VCC
VCC
VCC
$\overline{IB0}$
$\overline{IB7}$
T/R 1
T/R2
$\overline{ATN}$
$\overline{EOI}$
$\overline{DAV}$
DAC
RFD
$\overline{SRQ}$
$\overline{REN}$
$\overline{IFC}$
1
S/$\overline{R}$ (Ø)
0
1
2
3
4
5
S/$\overline{R}$ (5)
S/$\overline{R}$ (1-4)
6
7
S/$\overline{R}$ (6)
S/$\overline{R}$ (7)
1
Gnd
Gnd
Gnd
Gnd
DAV
SRQ
DIO1
DIO8
DAC
RFD
ATN
EOI
REN
IFC
Jumper or second level metal

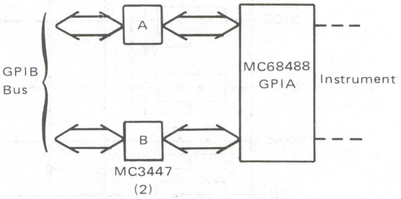
FIGURE 8 — SIMPLE SYSTEM CONFIGURATION


+5 V
2 MC3447s
IEEE 488-1978 BUS
DAV
DIO1
DIO3
DIO5
DIO7
NDAC
EOI
IFC
SRQ
DIO2
DIO4
DIO6
DIO8
NRFD
ATN
REN
Trig
T/R̄ 1
T/R̄ 2
DAV
IB0
IB2
IB4
IB6
DAC
EOI
IFC
SRQ
IB1
IB3
IB5
IB7
RFD
ATN
REN
MC68488
GPIA
DB0
DB7
R/W̄
RS0
RS2
IRQ
Data
Address
D0
D7
R/W
A0
A15
IRQ
MC6802
or
MC6800
MPU

NOTE 1: Although the MC3447 transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

FIGURE 9 — SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations					MC68488 Connections	
A	B						A	B
$T/\overline{R}$ 2	V_{CC}	$S/\overline{R}$ (0)	1		24	V_{CC}	V_{CC}	V_{CC}
$\overline{\text{DAV}}$	$\overline{\text{SRQ}}$	Data 0 0	2		23	Bus 0	DAV	SRQ
$\overline{\text{IB0}}$	$\overline{\text{IB1}}$	Data 1	3		22	Bus 1	DIO 1	DIO 2
$\overline{\text{IB2}}$	$\overline{\text{IB3}}$	Data 2	4		21	Bus 2	DIO 3	DIO 4
$\overline{\text{IB4}}$	$\overline{\text{IB5}}$	Data 3	5		20	Bus 3	DIO 5	DIO 6
$\overline{\text{IB6}}$	$\overline{\text{IB7}}$	Data 4	6	Octal GPIB Transceiver	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7		18	Bus 5	NDAC	NRFD
$T/\overline{R}$ 2	$T/\overline{R}$ 2	$S/\overline{R}$ (5)	8		17	$S/\overline{R}$ (1–4)	$T/\overline{R}$ 2	$T/\overline{R}$ 2
$\overline{\text{EOI}}$	$\overline{\text{ATN}}$	Data 6	9		16	Bus 6	EOI	ATN
$\overline{\text{IFC}}$	$\overline{\text{REN}}$	Data 7	10		15	Bus 7	IFC	REN
$T/\overline{R}$ 1	Gnd	$S/\overline{R}$ (6)	11		14	$S/\overline{R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12		13	Bus Gnd	Gnd	Gnd



MOTOROLA

MC3448A

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

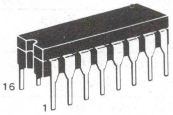
Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector[1] or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option[1]
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

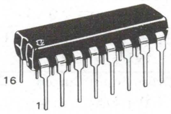
[1] Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT



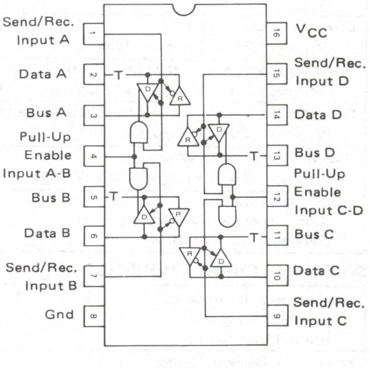
L SUFFIX
CERAMIC PACKAGE
CASE 620-02



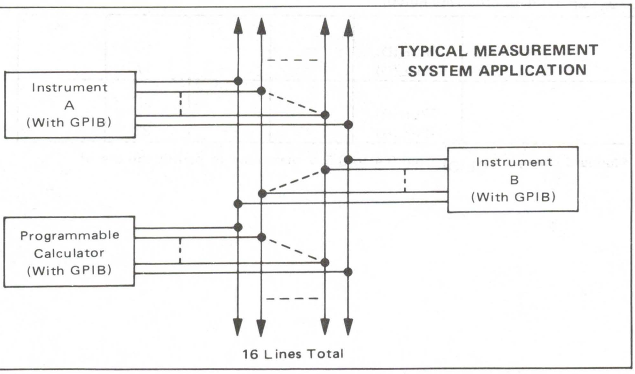
P SUFFIX
PLASTIC PACKAGE
CASE 648-05

MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C


Send/Rec. Input A
Data A
Bus A
Pull-Up Enable Input A-B
Bus B
Data B
Send/Rec. Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Send/Rec. Input D
Data D
Bus D
Pull-Up Enable Input C-D
Bus C
Data C
Send/Rec. Input C
T
D
R

-T- = Bus Termination


Instrument A (With GPIB)
Instrument B (With GPIB)
Programmable Calculator (With GPIB)
16 Lines Total

TYPICAL MEASUREMENT SYSTEM APPLICATION

TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	–
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X = Don't Care

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V and 0 $\leqslant T_A \leqslant 70^{\circ}$C; typical values are at $T_A = 25^{\circ}$C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/R)}$ = 0.8 V)	$V_{(BUS)}$	2.75	–	3.7	
($I_{(BUS)}$ = −12 mA)	$V_{IC(BUS)}$	–	–	−1.5	
Bus Current	$I_{(BUS)}$				mA
(5.0 V $\leqslant V_{(BUS)} \leqslant$ 5.5 V)		0.7	–	2.5	
($V_{(BUS)}$ = 0.5 V)		−1.3	–	−3.2	
(V_{CC} = 0 V, 0 V $\leqslant V_{(BUS)} \leqslant$ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.8 V, Low to High)	$V_{ILH(R)}$	–	1.6	1.8	
($V_{I(S/R)}$ = 0.8 V, High to Low)	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage – High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = −800 μA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	−15		−75	mA
Driver Input Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current – Data Pins					μA
($V_{I(S/R)} = V_{I(E)}$ = 2.0 V)					
(0.5 $\leqslant V_{I(D)} \leqslant$ 2.7 V)	$I_{I(D)}$	−200	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current – Send/Receive					μA
(0.5 $\leqslant V_{I(S/R)} \leqslant$ 2.7 V)	$I_{I(S/R)}$	−100	–	20	
($V_{I(S/R)}$ = 5.5 V)	$I_{IB(S/R)}$	–	–	100	
Input Current – Enable					μA
(0.5 $\leqslant V_{I(E)} \leqslant$ 2.7 V)	$I_{I(E)}$	−200	–	20	
($V_{I(E)}$ = 5.5 V)	$I_{IB(E)}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)	$V_{IC(D)}$	–	–	−1.5	V
Driver Output Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = −5.2 mA)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage – Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	−30	–	−120	mA
Power Supply Current					mA
(Listening Mode – All Receivers On)	I_{CCL}	–	63	85	
(Talking Mode – All Drivers On)	I_{CCH}	–	106	125	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, $T_A = 25^{\circ}$C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	–	15	
(Output High to Low)	$t_{PHL(D)}$	–	–	17	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	–	–	25	
(Output High to Low)	$t_{PHL(R)}$	–	–	23	

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	–	30	
Third State to Logic High	$t_{PZH(R)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	–	30	
Third State to Logic Low	$t_{PZL(R)}$	–	–	30	
Propagation Delay Time – Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	–	30	
Third State to Logic High	$t_{PZH(D)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(D)}$	–	–	30	
Third State to Logic Low	$t_{PZL(D)}$	–	–	30	
Turn-On Time – Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	–	–	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	–	–	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

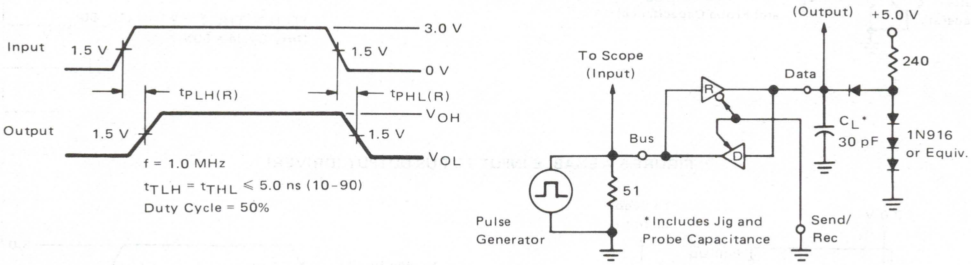

Input
1.5 V
3.0 V
1.5 V
0 V
tPLH(R)
tPHL(R)
VOH
Output
1.5 V
1.5 V
VOL
f = 1.0 MHz
tTLH = tTHL ≤ 5.0 ns (10–90)
Duty Cycle = 50%
To Scope (Output)
+5.0 V
240
To Scope (Input)
Data
R
CL* 30 pF
1N916 or Equiv.
Bus
D
51
Pulse Generator
*Includes Jig and Probe Capacitance
Send/ Rec

FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

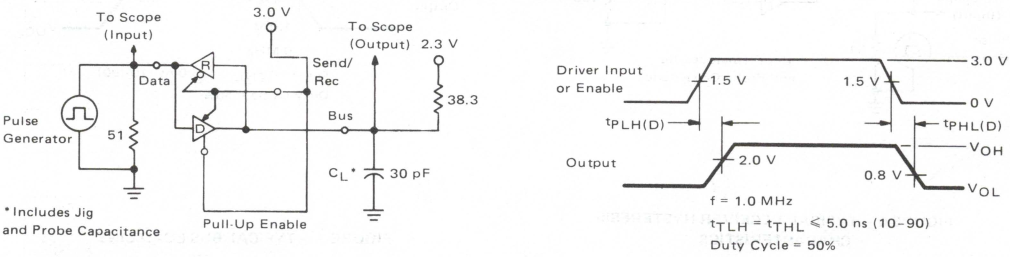

To Scope (Input)
3.0 V
To Scope (Output)
2.3 V
Send/ Rec
Data
R
38.3
Pulse Generator
51
D
Bus
CL* 30 pF
*Includes Jig and Probe Capacitance
Pull-Up Enable
Driver Input or Enable
1.5 V
1.5 V
3.0 V
0 V
tPLH(D)
tPHL(D)
VOH
Output
2.0 V
0.8 V
VOL
f = 1.0 MHz
tTLH = tTHL ≤ 5.0 ns (10–90)
Duty Cycle = 50%

FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

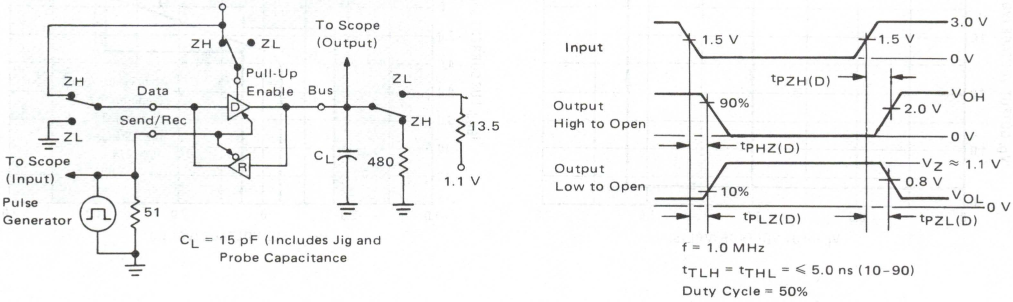
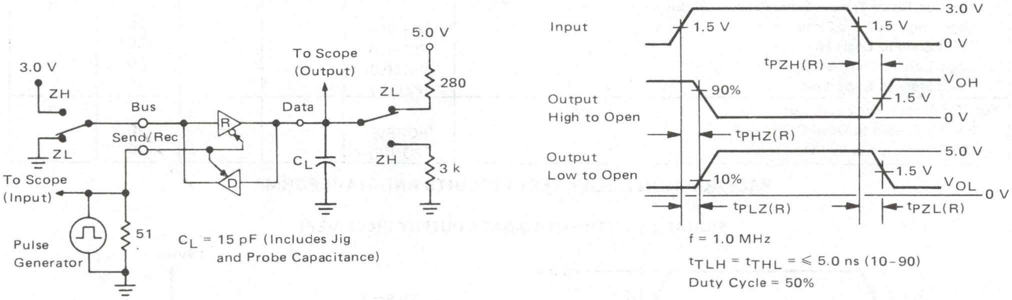

3.0 V
ZH
ZL
To Scope (Output)
Pull-Up Enable
ZH
Data
Bus
ZL
D
ZH
13.5
Send/Rec
ZL
To Scope (Input)
R
CL
480
1.1 V
Pulse Generator
51
CL = 15 pF (Includes Jig and Probe Capacitance
Input
1.5 V
1.5 V
3.0 V
0 V
tPZH(D)
VOH
Output High to Open
90%
2.0 V
0 V
tPHZ(D)
VZ ≈ 1.1 V
Output Low to Open
0.8 V
10%
VOL
0 V
tPLZ(D)
tPZL(D)
f = 1.0 MHz
tTLH = tTHL = ≤ 5.0 ns (10–90)
Duty Cycle = 50%

FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)



3.0 V
ZH
ZL
Bus
Send/Rec
To Scope (Input)
Pulse Generator
51
R
D
To Scope (Output)
Data
5.0 V
280
ZL
ZH
3 k
CL
Input
1.5 V
1.5 V
3.0 V
0 V
tPZH(R)
Output High to Open
90%
VOH
1.5 V
0 V
tPHZ(R)
Output Low to Open
5.0 V
10%
1.5 V
VOL
0 V
tPLZ(R)
tPZL(R)

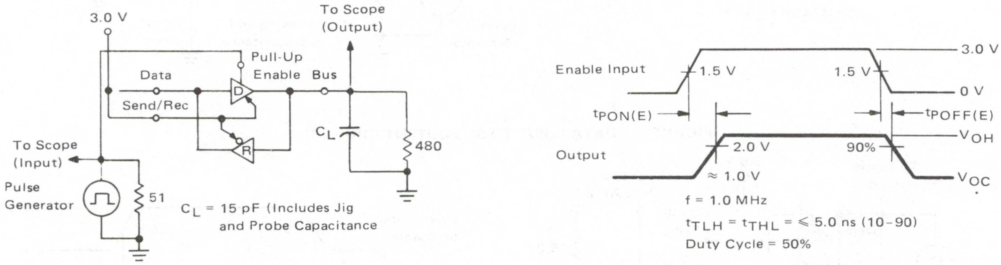
C_L = 15 pF (Includes Jig and Probe Capacitance)

f = 1.0 MHz

$t_{TLH} = t_{THL} = \leqslant 5.0$ ns (10–90)

Duty Cycle = 50%

FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)



3.0 V
Data
Send/Rec
Pull-Up
Enable
Bus
D
R
To Scope (Output)
To Scope (Input)
Pulse Generator
51
CL
480
Enable Input
1.5 V
1.5 V
3.0 V
0 V
tPON(E)
tPOFF(E)
Output
2.0 V
90%
VOH
≈ 1.0 V
VOC

C_L = 15 pF (Includes Jig and Probe Capacitance

f = 1.0 MHz

$t_{TLH} = t_{THL} = \leqslant 5.0$ ns (10–90)

Duty Cycle = 50%

FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

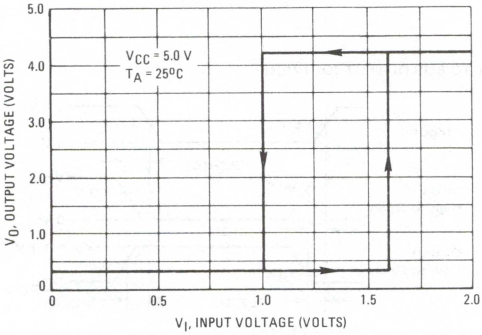


FIGURE 7 – TYPICAL BUS LOAD LINE

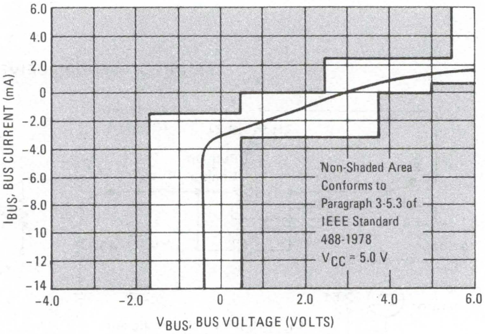
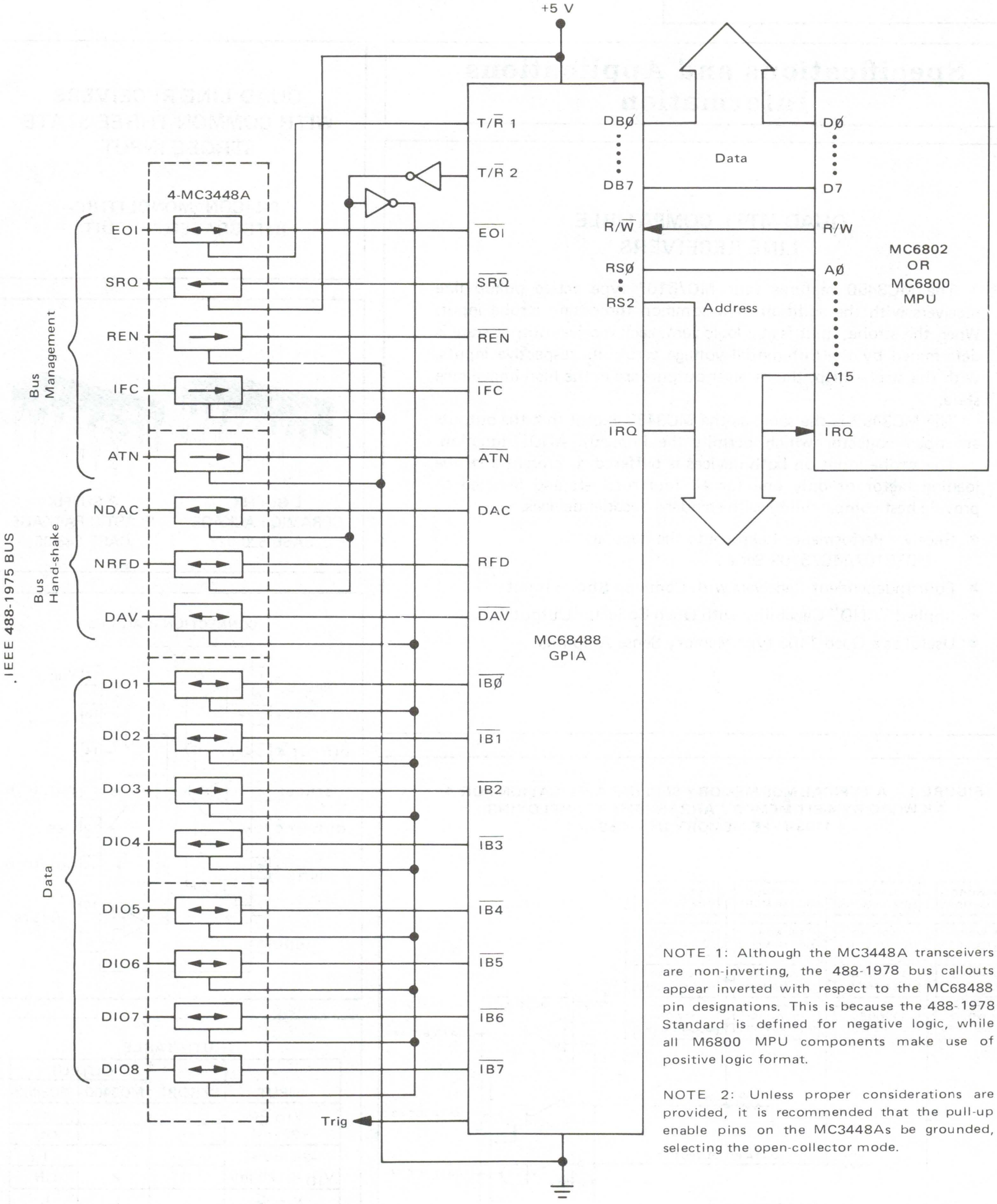


FIGURE 8 — SIMPLE SYSTEM CONFIGURATION


+5 V
4-MC3448A
IEEE 488-1975 BUS
Bus Management
Bus Hand-shake
Data
EOI
SRQ
REN
IFC
ATN
NDAC
NRFD
DAV
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
T/R̄ 1
T/R̄ 2
EOI
SRQ
REN
IFC
ATN
DAC
RFD
DAV
IB0
IB1
IB2
IB3
IB4
IB5
IB6
IB7
MC68488
GPIA
DB0
DB7
R/W̄
RS0
RS2
IRQ
Data
Address
D0
D7
R/W
A0
A15
IRQ
MC6802
OR
MC6800
MPU
Trig

NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

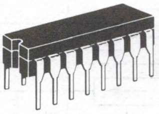
MC3450
MC3452

MOTOROLA

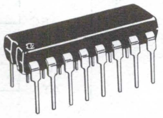
Specifications and Applications Information

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620-02



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

QUAD MTTL COMPATIBLE LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

CONNECTION DIAGRAM

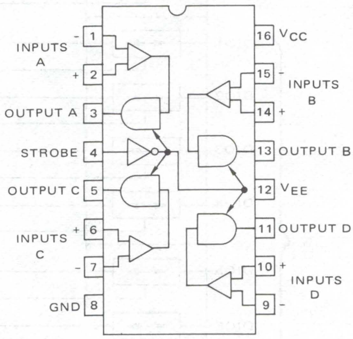
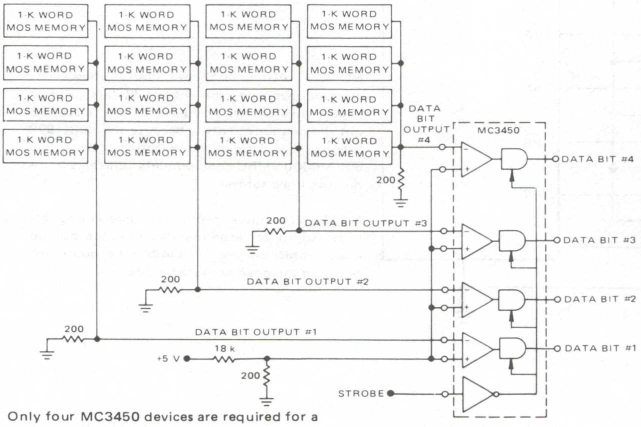

INPUTS A
-
1
+
2
OUTPUT A
3
STROBE
4
OUTPUT C
5
INPUTS C
+
6
-
7
GND
8
16
VCC
15
-
INPUTS B
14
+
13
OUTPUT B
12
VEE
11
OUTPUT D
10
+
INPUTS D
9
-

FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES


1-K WORD MOS MEMORY
DATA BIT OUTPUT #4
MC3450
DATA BIT #4
200
DATA BIT OUTPUT #3
DATA BIT #3
DATA BIT OUTPUT #2
DATA BIT #2
DATA BIT OUTPUT #1
DATA BIT #1
18 k
+5 V
STROBE

Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geqslant$ +25 mV	L	H	Off
	H	Z	Off
-25 mV $\leqslant V_{ID} \leqslant$ +25 mV	L	I	I
	H	Z	Off
$V_{ID} \leqslant$ -25 mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

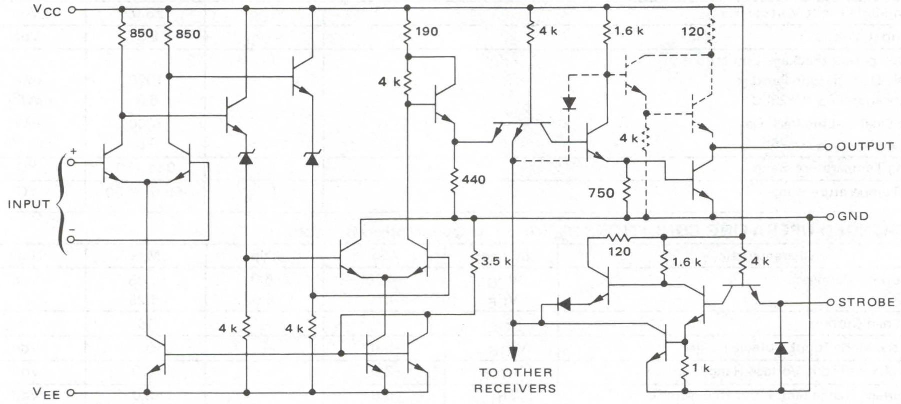
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

			MC3450			MC3452			
Characteristic	Symbol	Fig.	Min	Typ	Max	Min	Typ	Max	Unit
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	µA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	µA
High Level Input Current to Strobe Input	$I_{IH(S)}$	5							
$V_{IH(S)}$ = +2.4 V			–	–	40	–	–	40	µA
$V_{IH(S)}$ = +5.25 V			–	–	1.0	–	–	1.0	mA
Low Level Input Current to Strobe Input $V_{IH(S)}$ = +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	µA
Low Level Output Voltage	V_{OL}	3	–	–	0.5	–	–	0.5	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	µA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

			MC3450			MC3452			
Characteristic	Symbol	Fig.	Min	Typ	Max	Min	Typ	Max	Unit
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

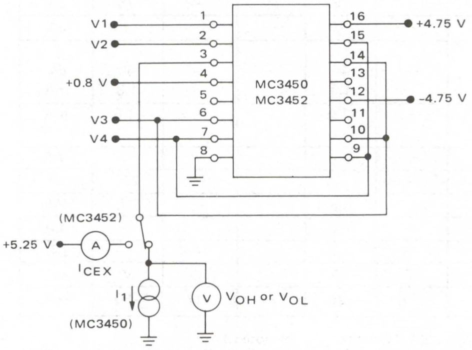
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)


V_{CC}
850
850
190
4 k
1.6 k
120
4 k
440
4 k
750
OUTPUT
INPUT
+
–
GND
120
1.6 k
4 k
3.5 k
STROBE
4 k
4 k
1 k
TO OTHER RECEIVERS
V_{EE}

Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}


V1
V2
+0.8 V
V3
V4
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
+4.75 V
–4.75 V
(MC3452)
+5.25 V
A
I_{CEX}
I_1
(MC3450)
V
V_{OH} or V_{OL}

TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–	+0.4 mA
	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–	
I_{CEX}	–	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–
	–	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	-16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

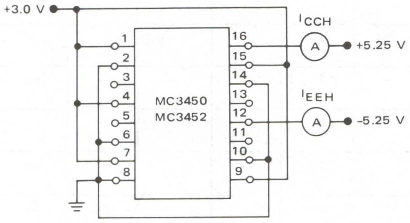
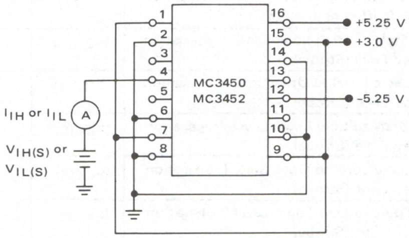
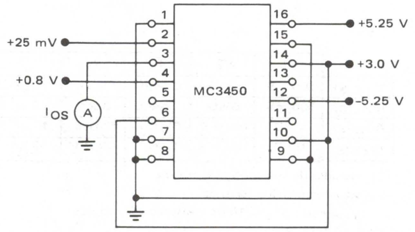

+3.0 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
I_{CCH}
A
+5.25 V
I_{EEH}
A
–5.25 V

FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
+5.25 V
+3.0 V
–5.25 V
I_{IH} or I_{IL}
A
$V_{IH(S)}$ or
$V_{IL(S)}$

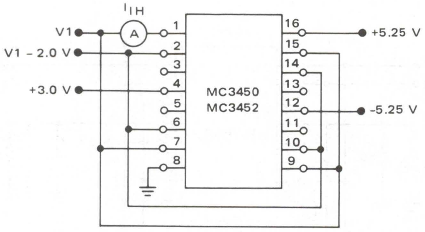
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}


+25 mV
+0.8 V
I_{OS}
A
MC3450
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+5.25 V
+3.0 V
-5.25 V

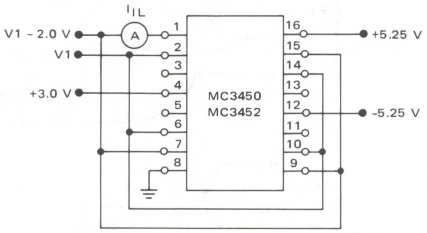
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – I_{IH}


I_{IH}
A
V1
V1 - 2.0 V
+3.0 V
MC3450
MC3452
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+5.25 V
-5.25 V

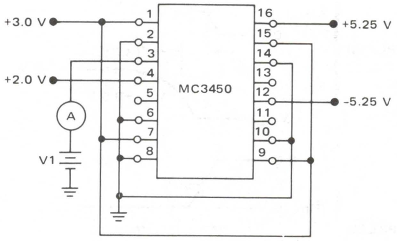
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 8 – I_{IL}


I_{IL}
A
V1 - 2.0 V
V1
+3.0 V
MC3450
MC3452
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+5.25 V
-5.25 V

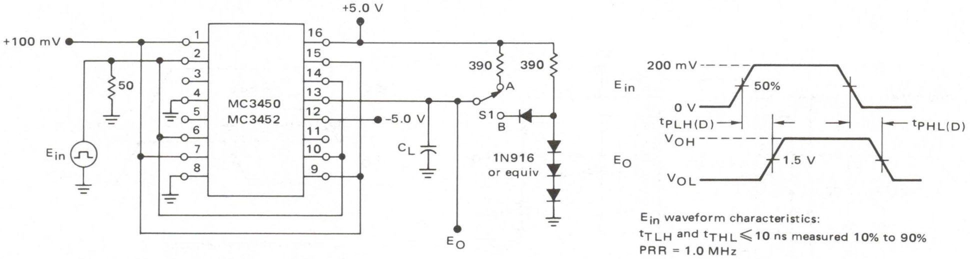
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 9 – I_{off}


+3.0 V
+2.0 V
A
V1
MC3450
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+5.25 V
-5.25 V

Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$


+5.0 V
+100 mV
50
E_{in}
MC3450
MC3452
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
-5.0 V
C_L
390
390
A
S1
B
1N916
or equiv
E_O
200 mV
50%
0 V
E_{in}
$t_{PLH(D)}$
$t_{PHL(D)}$
V_{OH}
1.5 V
E_O
V_{OL}

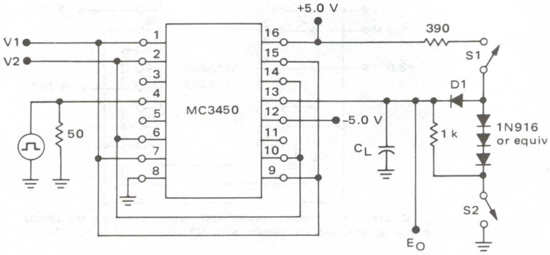
Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$ and $t_{PZH(S)}$


V1
V2
+5.0 V
390
S1
D1
1N916
or equiv
1 k
S2
MC3450
-5.0 V
C_L
50
E_O
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{in} waveform characteristics:

t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

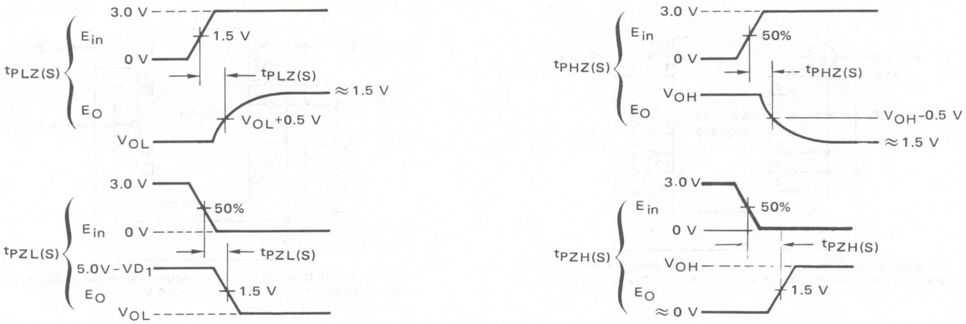
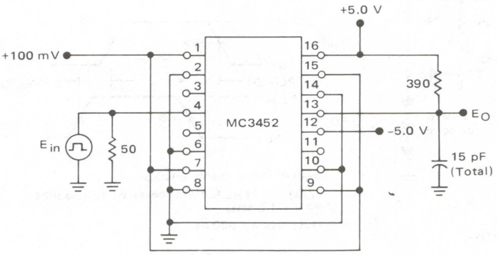
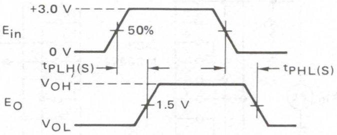

3.0 V
E_{in}
1.5 V
0 V
$t_{PLZ(S)}$
$t_{PLZ(S)}$
≈1.5 V
E_O
$V_{OL}+0.5$ V
V_{OL}
3.0 V
50%
E_{in}
0 V
$t_{PZL(S)}$
$t_{PZL(S)}$
5.0V-VD1
1.5 V
E_O
V_{OL}
3.0 V
E_{in}
50%
0 V
$t_{PHZ(S)}$
$t_{PHZ(S)}$
V_{OH}
E_O
$V_{OH}-0.5$ V
≈1.5 V
3.0 V
E_{in}
50%
0 V
$t_{PZH(S)}$
$t_{PZH(S)}$
V_{OH}
E_O
1.5 V
≈0 V

FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$


+5.0 V
+100 mV
390
E_O
MC3452
-5.0 V
15 pF
(Total)
E_{in}
50
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

Output of Channel B shown under test, other channels are tested similarly.


+3.0 V
E_{in}
50%
0 V
$t_{PLH(S)}$
$t_{PHL(S)}$
V_{OH}
E_O
1.5 V
V_{OL}

E_{in} waveform characteristics:

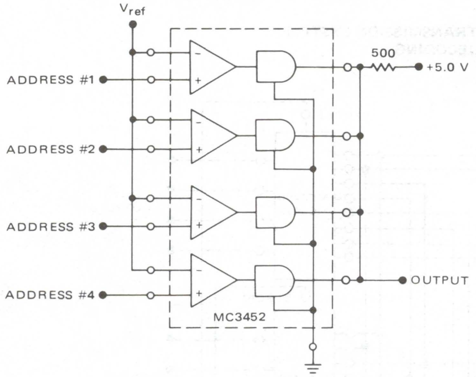
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%

PRR = 1.0 MHz

Duty Cycle = 500 ns

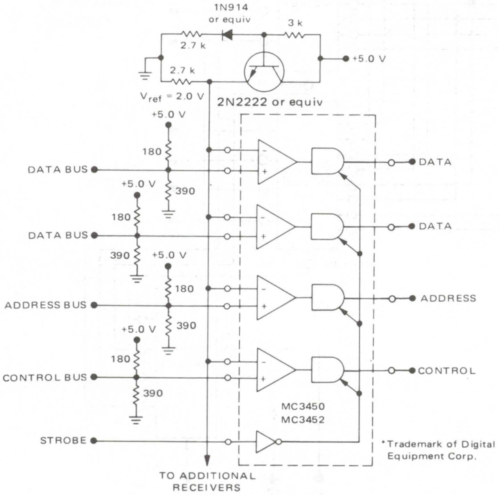
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING


V_ref
ADDRESS #1
ADDRESS #2
ADDRESS #3
ADDRESS #4
500
+5.0 V
OUTPUT
MC3452

The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

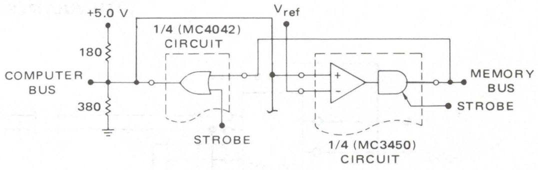
FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS


1N914
or equiv
3 k
2.7 k
2.7 k
+5.0 V
V_ref = 2.0 V
2N2222 or equiv
+5.0 V
180
390
DATA BUS
DATA
+5.0 V
180
DATA BUS
390
DATA
+5.0 V
180
ADDRESS BUS
390
ADDRESS
+5.0 V
180
CONTROL BUS
390
CONTROL
MC3450
MC3452
STROBE
TO ADDITIONAL RECEIVERS

*Trademark of Digital Equipment Corp.

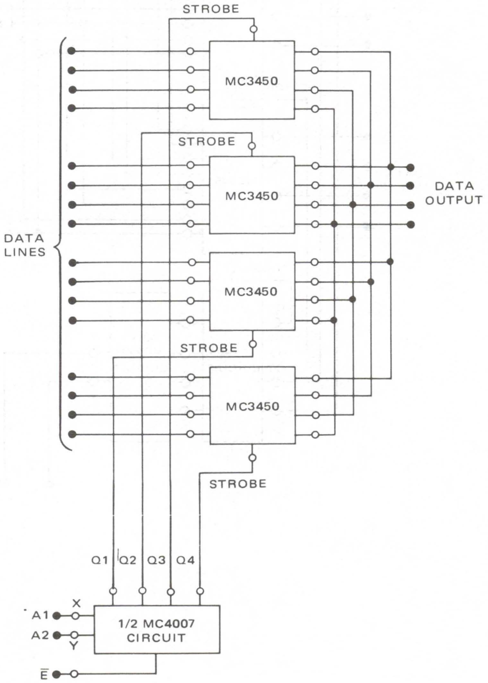
The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION


+5.0 V
V_ref
1/4 (MC4042) CIRCUIT
180
COMPUTER BUS
380
STROBE
MEMORY BUS
STROBE
1/4 (MC3450) CIRCUIT

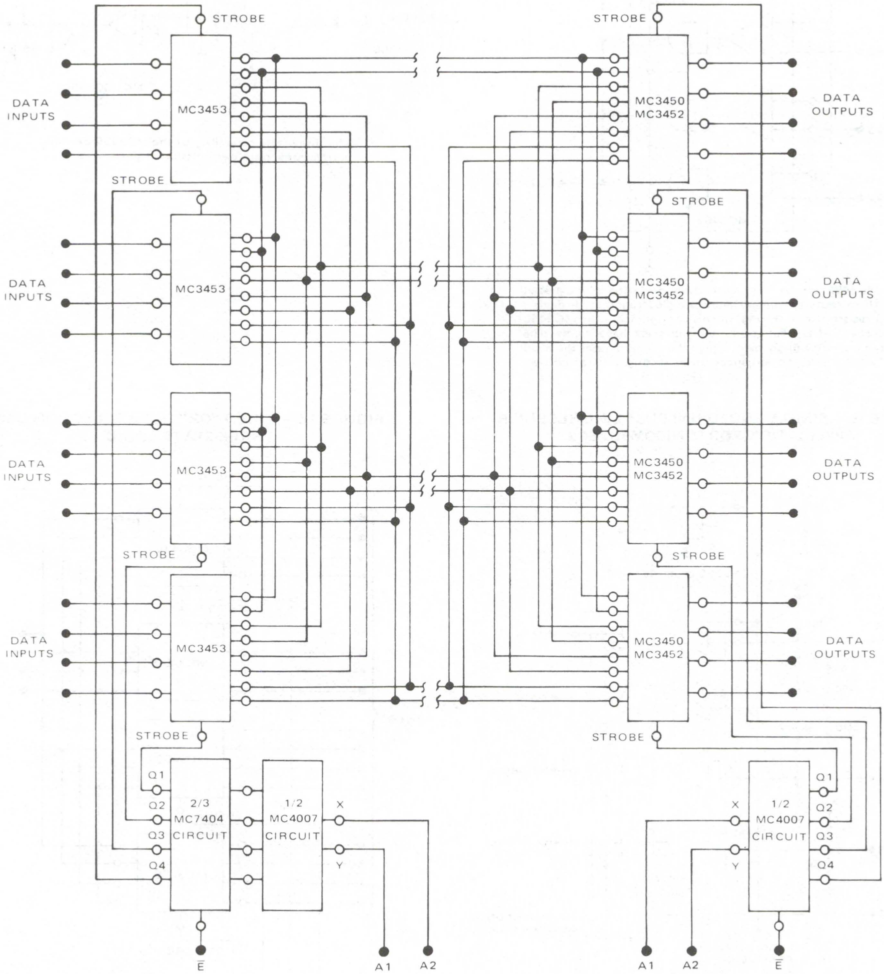
The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC


STROBE
MC3450
STROBE
MC3450
DATA OUTPUT
DATA LINES
MC3450
STROBE
MC3450
STROBE
Q1
Q2
Q3
Q4
X
A1
A2
Y
1/2 MC4007 CIRCUIT
E̅

APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING


STROBE
DATA INPUTS
MC3453
MC3450
MC3452
DATA OUTPUTS
Q1
Q2
Q3
Q4
2/3
MC7404
CIRCUIT
1/2
MC4007
CIRCUIT
X
Y
Ē
A1
A2

MOTOROLA

MC3453

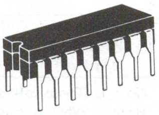
MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

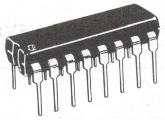
- Four Independent Drivers with Common Inhibit Input
- −3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT

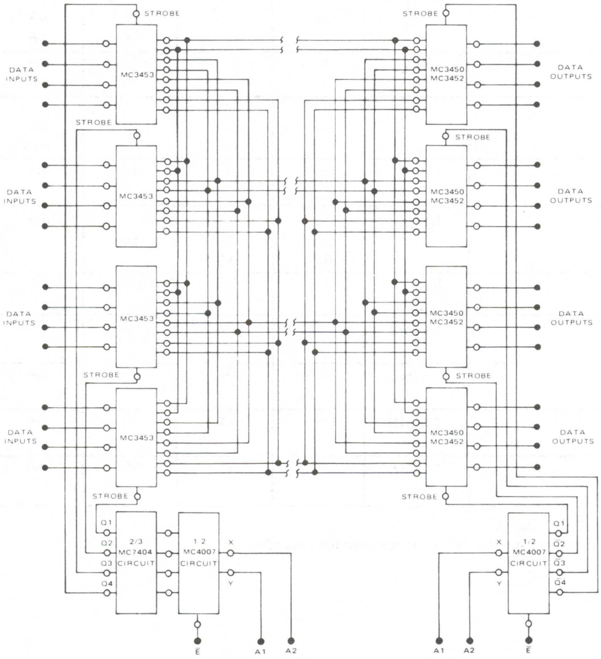


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

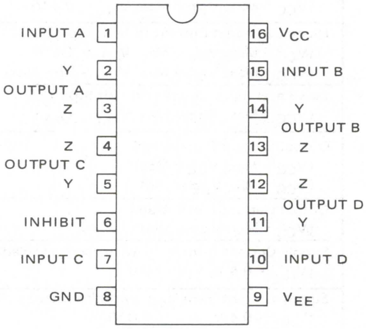


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 — PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING


STROBE
DATA INPUTS
MC3453
MC3450
MC3452
DATA OUTPUTS
Q1
Q2
Q3
Q4
2/3 MC7404 CIRCUIT
1/2 MC4007 CIRCUIT
X
Y
Ē
A1
A2

CONNECTION DIAGRAM


INPUT A 1
Y OUTPUT A 2
Z 3
Z OUTPUT C 4
Y 5
INHIBIT 6
INPUT C 7
GND 8
16 V_CC
15 INPUT B
14 Y OUTPUT B
13 Z
12 Z OUTPUT D
11 Y
10 INPUT D
9 V_EE

TRUTH TABLE
(positive logic)

LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual In-Line Packages		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range	V_{OCR}				Volts
Positive		0	–	+10	
Negative		0	–	-3.0	

Note 1. These voltage values are in respect to the ground terminal.

Note 2. When not using all four channels, unused outputs must be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs)	I_{IH_L}				
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)		–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)		–	–	1.0	mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input)	I_{IH_I}				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)		–	–	40	µA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)		–	–	1.0	mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state)	$I_{O(on)}$				mA
(V_{CC} = Max, V_{EE} = Max)		–	11	15	
(V_{CC} = Min, V_{EE} = Min)		6.5	11	–	
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.

##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	– –	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	– –	16 20	25 25	ns

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

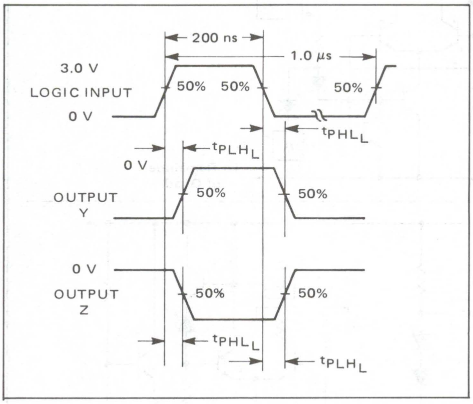
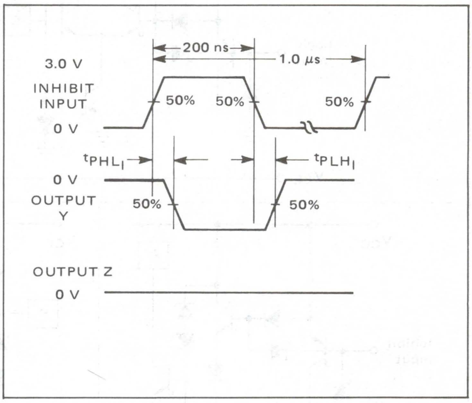
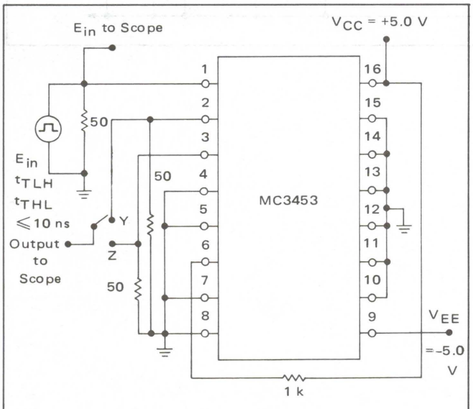

200 ns
1.0 µs
3.0 V
LOGIC INPUT
0 V
50%
50%
50%
t_{PHL_L}
t_{PLH_L}
0 V
OUTPUT Y
50%
50%
0 V
OUTPUT Z
50%
50%
t_{PHL_L}
t_{PLH_L}

FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS


200 ns
1.0 µs
3.0 V
INHIBIT INPUT
0 V
50%
50%
50%
t_{PHL_I}
t_{PLH_I}
0 V
OUTPUT Y
50%
50%
OUTPUT Z
0 V

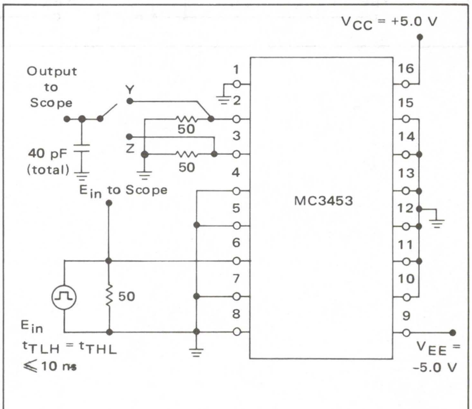
TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT


E_{in} to Scope
V_{CC} = +5.0 V
50
E_{in}
t_{TLH}
t_{THL}
⩽10 ns
Output to Scope
Y
Z
50
50
MC3453
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{EE} = −5.0 V
1 k

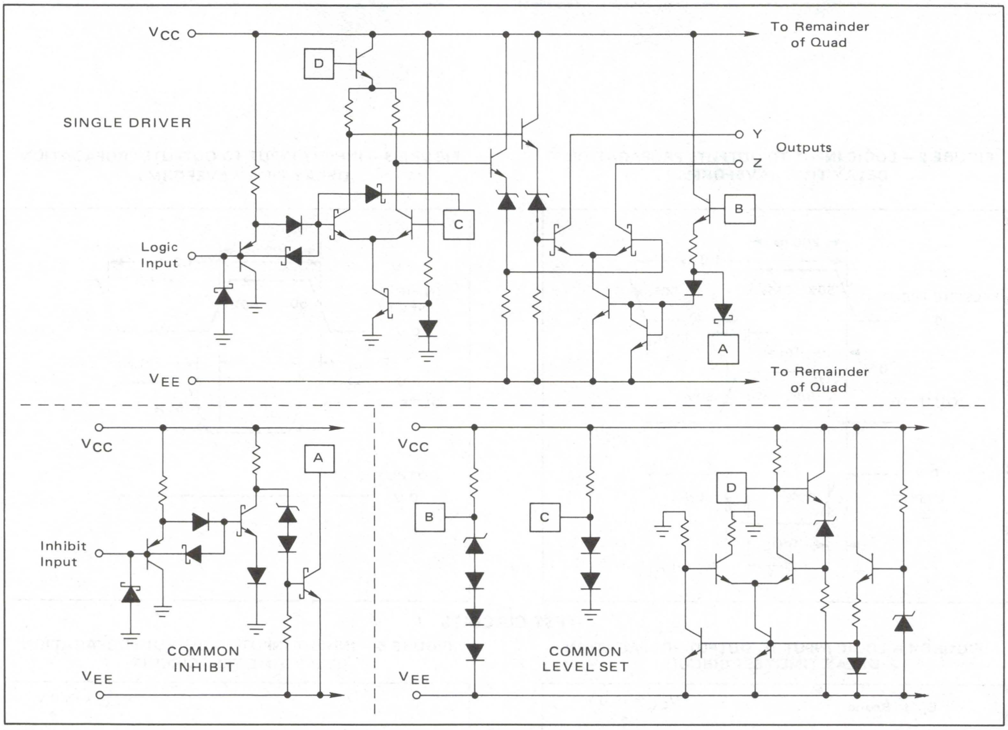
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT


V_{CC} = +5.0 V
Output to Scope
Y
Z
50
50
40 pF (total)
E_{in} to Scope
50
E_{in}
t_{TLH} = t_{THL}
⩽10 ns
MC3453
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{EE} = −5.0 V

Channel A shown under test, the other channels are tested similarly.

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)


VCC
To Remainder of Quad
D
SINGLE DRIVER
Y
Outputs
Z
C
B
Logic Input
A
VEE
To Remainder of Quad
VCC
A
Inhibit Input
COMMON INHIBIT
VEE
VCC
B
C
D
COMMON LEVEL SET
VEE

MOTOROLA

MC3467

TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

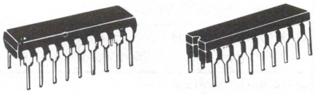
The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

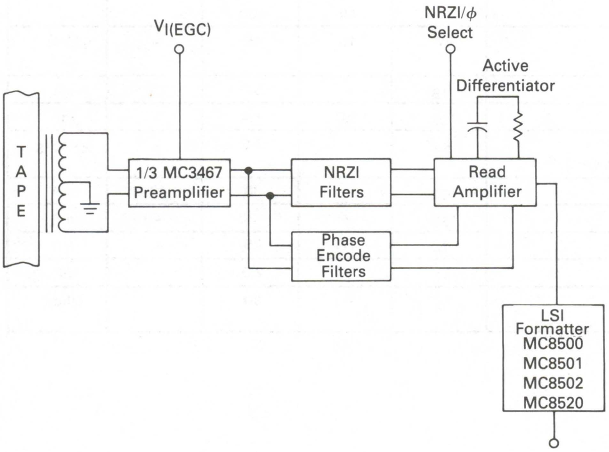
- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

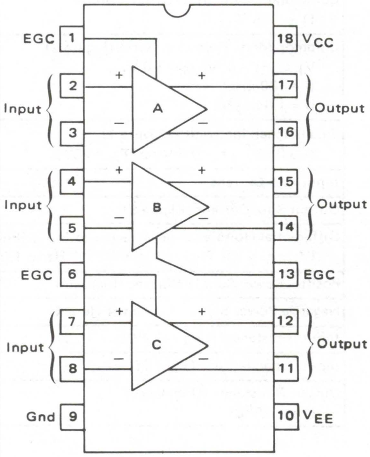
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

L SUFFIX
CERAMIC PACKAGE
CASE 726-01



TYPICAL APPLICATION
HIGH PERFORMANCE 9-TRACK OPEN REEL
TAPE SYSTEM


VI(EGC)
NRZI/ϕ Select
Active Differentiator
T A P E
1/3 MC3467 Preamplifier
NRZI Filters
Read Amplifier
Phase Encode Filters
LSI Formatter MC8500 MC8501 MC8502 MC8520


EGC 1
Input 2
3
Input 4
5
EGC 6
Input 7
8
Gnd 9
18 VCC
17 Output
16
15 Output
14
13 EGC
12 Output
11
10 VEE
A
B
C
+
−

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			V
Positive Supply Voltage	V_{CC}	6.0	
Negative Supply Voltage	V_{EE}	−9.0	
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	−5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	±5.0	V
Input Common-Mode Voltage	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_s	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, f = 100 kHz, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range					
Positive Supply Voltage	V_{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EER}	−5.5	−6.0	−7.0	V
Operating EGC Voltage	$V_{I(EGC)}$	0	–	V_{CC}	V
Differential Voltage Gain (Balanced) ($V_{I(EGC)} = 0$, e_i = 25 mVp-p) (See Figure 1)	A_{VD}	85	100	120	V/V
Differential Voltage Gain ($V_{I(EGC)} = V_{CC}$)	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVp-p)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common-Mode Range	V_{ICR}	±1.5	±2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common-Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common Mode Rejection Ratio (Figure 2) $V_{I(EGC)} = 0$, $V_{CM} = 1.0\ V_{pp}$	CMRR				dB
(f = 100 kHz)		60	100	–	
(f = 1.0 MHz)		40	100	–	
Small-Signal Bandwidth (Figure 1) (−3.0 dB, e_i = 1.0 mVp-p, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	µA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)} = 0$, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	−30	−40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT

(Channel A under test, other channels tested similarly)

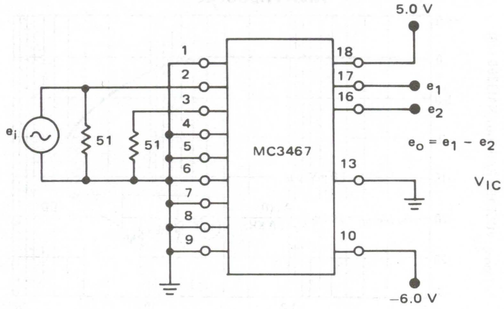

5.0 V
MC3467
1
2
3
4
5
6
7
8
9
18
17
16
13
10
e_1
e_2
$e_o = e_1 - e_2$
e_i
51
51
−6.0 V

FIGURE 2 – COMMON-MODE REJECTION RATIO

(Channel A under test, other amplifiers tested similarly)

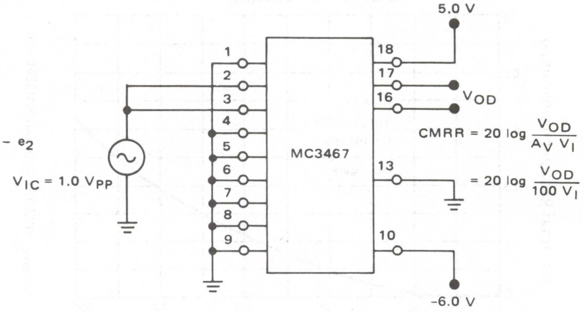
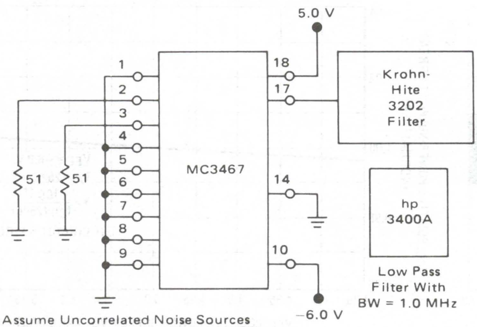

5.0 V
MC3467
1
2
3
4
5
6
7
8
9
18
17
16
13
10
V_{OD}
$V_{IC} = 1.0\ V_{PP}$
$\mathrm{CMRR} = 20 \log \frac{V_{OD}}{A_V V_I}$
$= 20 \log \frac{V_{OD}}{100\ V_I}$
−6.0 V

FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT


5.0 V
MC3467
1
2
3
4
5
6
7
8
9
18
17
14
10
51
51
Krohn-Hite 3202 Filter
hp 3400A
Low Pass Filter With BW = 1.0 MHz
−6.0 V

Assume Uncorrelated Noise Sources

e_n (Differential Noise at Input) = $e_o \sqrt{2}/100$

FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

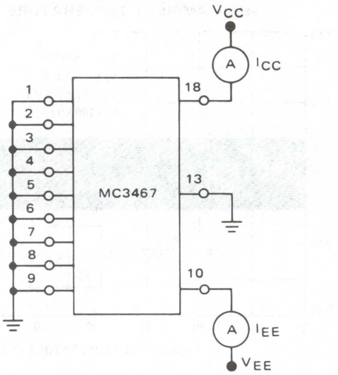

V_{CC}
A
I_{CC}
MC3467
1
2
3
4
5
6
7
8
9
18
13
10
A
I_{EE}
V_{EE}

FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT

(Channel A under test, other channels tested similarly)

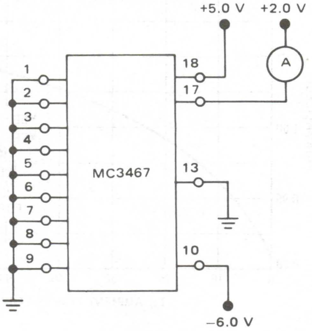
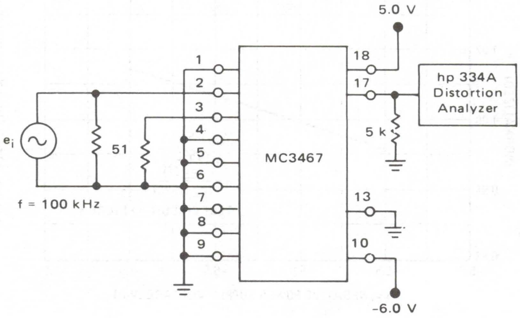

+5.0 V
+2.0 V
A
MC3467
1
2
3
4
5
6
7
8
9
18
17
13
10
−6.0 V

FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT

(Channel A under test, other channels tested similarly)


5.0 V
MC3467
1
2
3
4
5
6
7
8
9
18
17
13
10
hp 334A Distortion Analyzer
5 k
e_i
51
f = 100 kHz
−6.0 V

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = 25° unless otherwise noted)

FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE

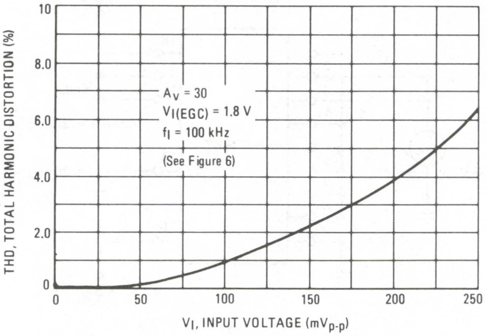


FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY

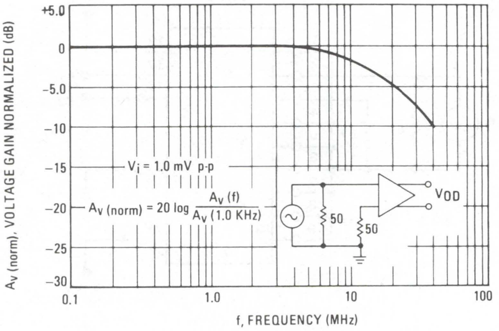


FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE

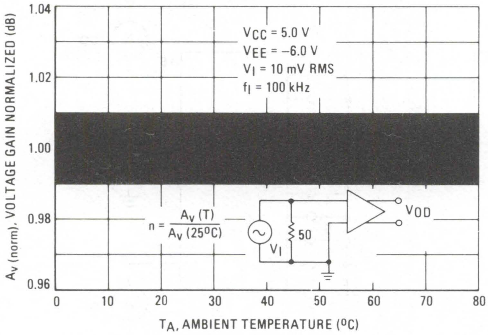


FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE

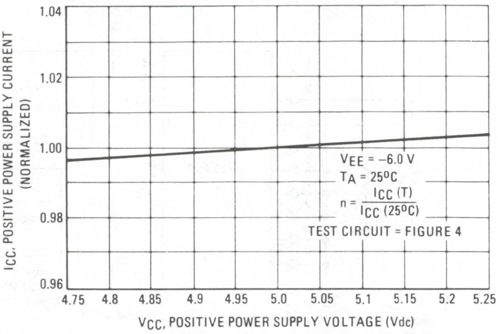


FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

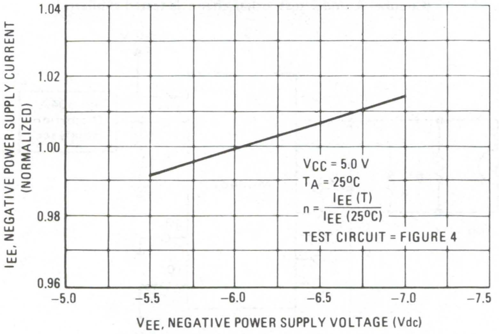


FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE

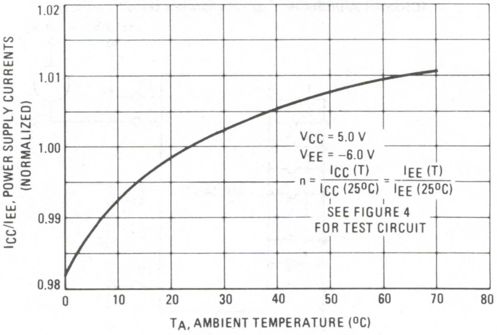


FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

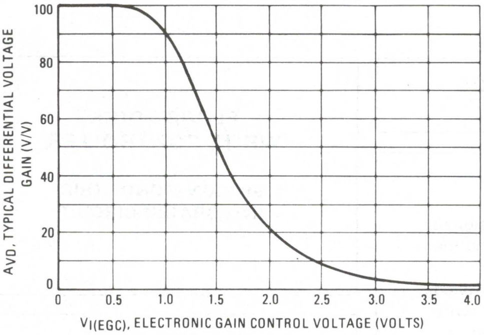


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

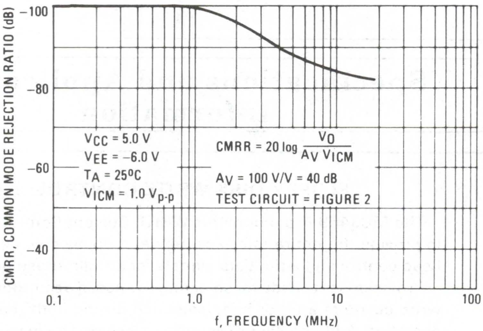


FIGURE 15 – PHASE SHIFT versus FREQUENCY

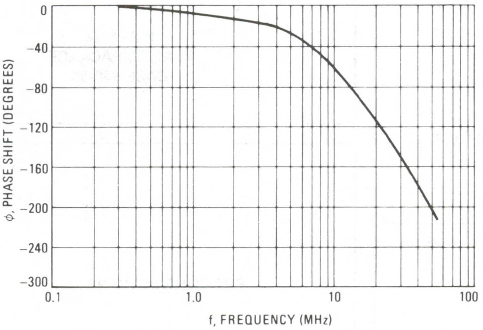
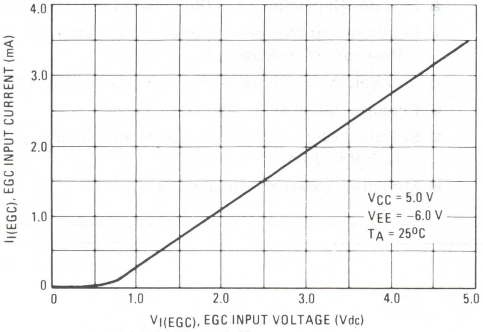
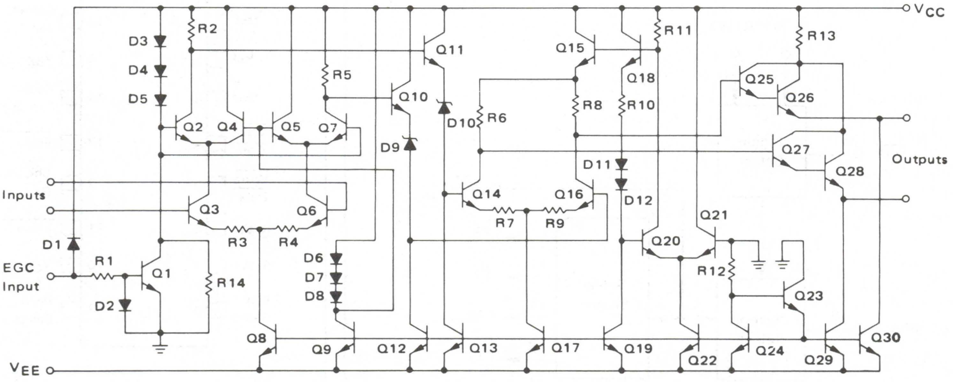


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467


VCC
R2
D3
D4
D5
R5
Q11
Q15
R11
R13
Q10
Q18
Q25
Q26
Q2
Q4
Q5
Q7
D10
R6
R8
R10
D9
Q27
Outputs
D11
Q28
Inputs
Q3
Q6
Q14
Q16
D12
R3
R4
R7
R9
Q21
D1
Q20
EGC Input
R1
Q1
R14
D6
D7
D8
R12
Q23
D2
Q8
Q9
Q12
Q13
Q17
Q19
Q22
Q24
Q29
Q30
VEE

MC3469P

MOTOROLA

Specifications and Applications Information

FLOPPY DISK WRITE CONTROLLER

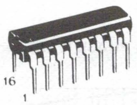
The MC3469 is a monolithic WRITE Current Controller designed to provide the entire interface between floppy disk heads and the head control and write data signals for stradle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With ±10% Logic Supply and Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components

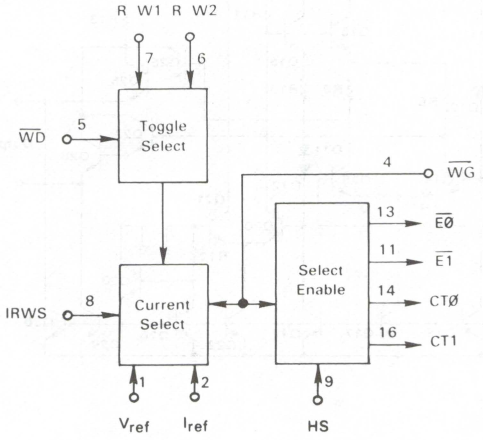
FLOPPY DISK WRITE CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

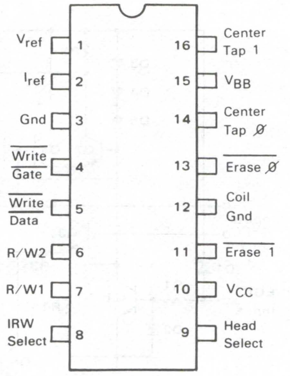


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

BLOCK DIAGRAM


R W1
R W2
7
6
$\overline{WD}$
5
Toggle Select
4
$\overline{WG}$
13
$\overline{E0}$
11
$\overline{E1}$
Select Enable
14
CT0
16
CT1
IRWS
8
Current Select
1
2
9
V_{ref}
I_{ref}
HS

PIN CONNECTIONS


V_{ref} 1
I_{ref} 2
Gnd 3
$\overline{\text{Write Gate}}$ 4
$\overline{\text{Write}}$ Data 5
R/W2 6
R/W1 7
IRW Select 8
16 Center Tap 1
15 V_{BB}
14 Center Tap 0
13 $\overline{\text{Erase 0}}$
12 Coil Gnd
11 $\overline{\text{Erase 1}}$
10 V_{CC}
9 Head Select

ABSOLUTE MAXIMUM RATINGS (Note 1) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 9)	V_I	5.75	Vdc
Storage Temperature	T_{stg}	−55 to +150	°C
Operating Junction Temperature	T_J	150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	+4.5 to +5.5	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	50 30	mA
High Level Input Voltage (V_{CC} = 4.5 V)	4, 8, 9	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.5 V)	4, 8, 9	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = −12 mA)	4, 5, 8, 9	V_{IK}	—	−0.87	−1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$)		V_{HTS}				V
T_A = 0°C to +70°C			0.2	—	—	
T_A = 25°C			0.4	0.76	—	
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 9	I_{IH}	—	0.1	40	µA
Low Level Input Current	4, 5, 8, 9	I_{IL}				mA
(V_{CC} = 5.5 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)			—	—	−1.6	
V_{BB} = 12 V	4		—	0.36	—	
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 9		—	0.39	—	

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 9)	14, 16	V_{OH}				V
(I_{OH} = −100 mA, V_{CC} = 4.5 V)						
V_{BB} = 10.8 to 26.4 V			V_{BB}-1.5	V_{BB}-1.0	—	
Output Low Voltage (See Figure 9)	14, 16	V_{OL}				mV
(I_{OL} = 1.0 mA)						
V_{BB} = 12 V			—	70	150	
V_{BB} = 24 V			—	70	150	
Output High Leakage (V_{OH} = 24 V, V_{CC} = 4.5 V, V_{BB} = 24 V)	11, 13	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 10)	11, 13	V_{OL}				V
(I_{OL} = 90 mA, V_{CC} = 4.5 V)						
V_{BB} = 12 V			—	0.27	0.60	
V_{BB} = 24 V			—	0.27	0.60	
CURRENT SOURCE						
Reference Voltage	1	V_{ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 − Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 35 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,\,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	ΔI/RW2, 1	—	15	40	μA
Average Value Write Current	6, 7					
$\left(\frac{I_{Pin\,6} + I_{Pin\,7}}{2}\right.$ for V_{BB} = 10.8 to 26.4 V)						
@ $I_{R/W}$ = I_{LOW}, R = 10 k		$\overline{I_{R/W(L)}}$				mA
T_A = 25°C			2.91	3.0	3.09	
T_A = 0 to +70°C			2.84	—	3.16	
@ $I_{R/W}$ = I_{LOW}, R = 5.0 k						
T_A = 25°C			5.64	5.89	6.14	
T_A = 0 to +70°C			5.51	—	6.28	
@ $I_{R/W}$ = I_{HI}, R = 10 k (I_{HI} = I_{LOW} + % I_{LOW})		$\overline{\Delta I_{R/W(H)}}$				%
T_A = 25°C			31.3	33.3	35.5	
T_A = 0 to +70°C			30.3	33.3	36.6	
Difference in Write Current	6, 7					
(|$I_{Pin\,6} - I_{Pin\,7}$|						
@ $I_{R/W}$ = I_{LOW}, V_{BB} = 10.8 V to 26.4 V)		$I_{R/W\Delta}$				mA
R = 10 k						
T_A = 25°C			—	0.003	0.015	
T_A = 0 to +70°C			—	—	0.023	
R = 5.0 k						
T_A = 25°C			—	—	0.030	
T_A = 0 to +70°C			—	—	0.046	

AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted — refer to Figure 2 and Figure 11.)

Characteristics (Note 2)	f_{in} (Note 3)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 9	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 9	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS, Pin 9	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS, Pin 9	—	1.4	4.0	μs
5. Delay from $\overline{\text{WG}}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	—	1.3	4.0	μs
6. Delay from $\overline{\text{WG}}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{\text{WG}}$, Pin 4	—	0.8	4.0	μs
7. Delay from $\overline{\text{WG}}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{\text{WG}}$, Pin 4	—	0.75	4.0	μs
8. Delay from $\overline{\text{WG}}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	—	1.2	4.0	μs
9. After $\overline{\text{WG}}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	$\overline{\text{WG}}$, Pin 4	20	750	—	ns
10. After $\overline{\text{WG}}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	20	1200	—	ns
11. After $\overline{\text{WG}}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	20	1200	—	ns
12. After $\overline{\text{WG}}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{\text{WG}}$, Pin 4	20	600	—	ns
13. Delay from $\overline{\text{WG}}$ going low through 0.8 V to $\overline{\text{E0}}$ going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	—	0.085	4.0	μs
14. Delay from $\overline{\text{WG}}$ going low through 0.8 V to $\overline{\text{E1}}$ going low through 1.0 V.	$\overline{\text{WG}}$, Pin 4	—	0.085	4.0	μs
15. Delay from $\overline{\text{WG}}$ going high through 2.0 V to $\overline{\text{E0}}$ going high through 23 V.	$\overline{\text{WG}}$, Pin 4	—	0.7	4.0	μs
16. Delay from $\overline{\text{WG}}$ going high through 2.0 V to $\overline{\text{E1}}$ going high through 23 V.	$\overline{\text{WG}}$, Pin 4	—	0.7	4.0	μs
17. After $\overline{\text{WG}}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	$\overline{\text{WG}}$, Pin 4	20	750	—	ns
18. After $\overline{\text{WG}}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{\text{WG}}$, Pin 4	20	750	—	ns
19. After $\overline{\text{WG}}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{\text{WG}}$, Pin 4	—	5.0	200	ns
20. After $\overline{\text{WG}}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{\text{WG}}$, Pin 4	—	5.0	200	ns
21. Setup time, Head Select going low before $\overline{\text{WG}}$ going low.	$\overline{\text{WG}}$, Pin 4	4.0	—	—	μs
22. $\overline{\text{Write Data}}$ low Hold Time	$\overline{\text{WD}}$, Pin 5	200	—	—	ns
23. $\overline{\text{Write Data}}$ high Hold Time	$\overline{\text{WD}}$, Pin 5	500	—	—	ns
24. Delay from $\overline{\text{WG}}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{\text{WG}}$, Pin 4	—	3.9	—	μs

Note 2: Test numbers refer to encircled numbers in Figure 2.
Note 3: AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 9	50 KHz	0.4 to 2.4 V	50%
$\overline{\text{WG}}$, Pin 4	50 KHz	0.4 to 2.4 V	50%
$\overline{\text{WD}}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

AC SWITCHING CHARACTERISTICS (continued)

(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted — refer to Figure 3 and Figure 11.)

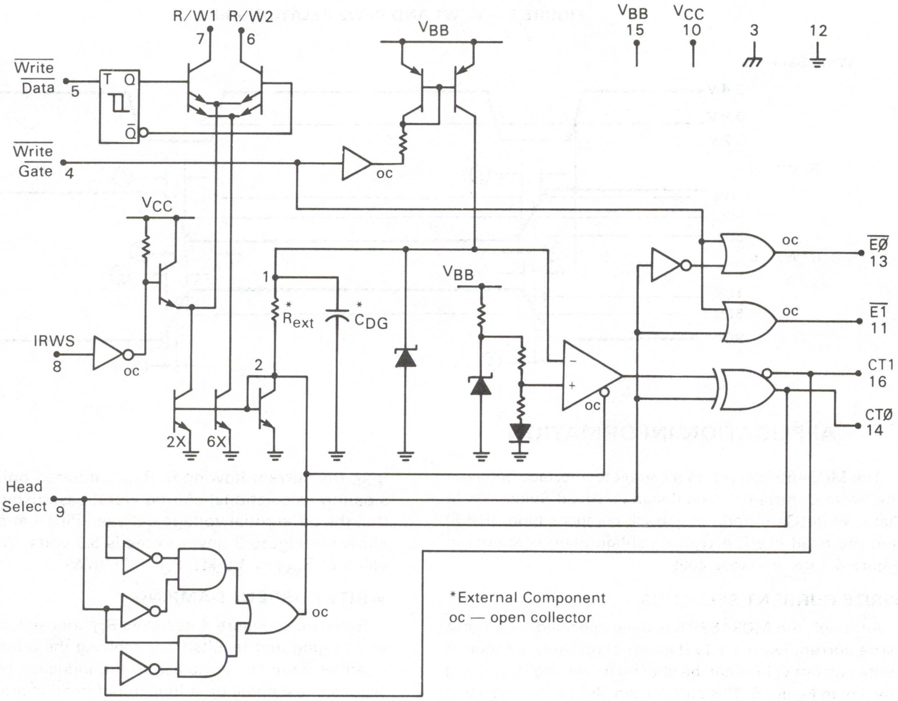
Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Rise time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Rise time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Fall time, 90% to 10%, of R/W1	—	12	200	ns
8. Fall time, 90% to 10%, of R/W2	—	12	200	ns

Note 4: Test numbers refer to encircled numbers in Figure 4.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	9	Head Select input selects between the head I/O pins: center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{\text{WG}}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{\text{WD}}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. Laser trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from V_{ref} to Gnd will adjust the Degauss period.
Center-tap 0	CT0	14	Center-tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{\text{E0}}$	13	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	16	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{\text{E1}}$	11	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	10	+5 V Power
	V_{BB}	15	+12 V or + 24 V Power
	Gnd	12	Coil grounds
	Gnd	3	Reference and logic ground

FIGURE 1 — LOGIC DIAGRAM


R/W1
R/W2
7
6
VBB
VBB
15
VCC
10
3
12
Write
Data
5
T
Q
Q̄
Write
Gate
4
oc
VCC
IRWS
8
oc
1
*
Rext
*
CDG
2
2X
6X
VBB
oc
oc
EØ
13
oc
E1
11
CT1
16
CTØ
14
Head
Select
9
oc

*External Component
oc — open collector

FIGURE 2 — AC TIMING DIAGRAM

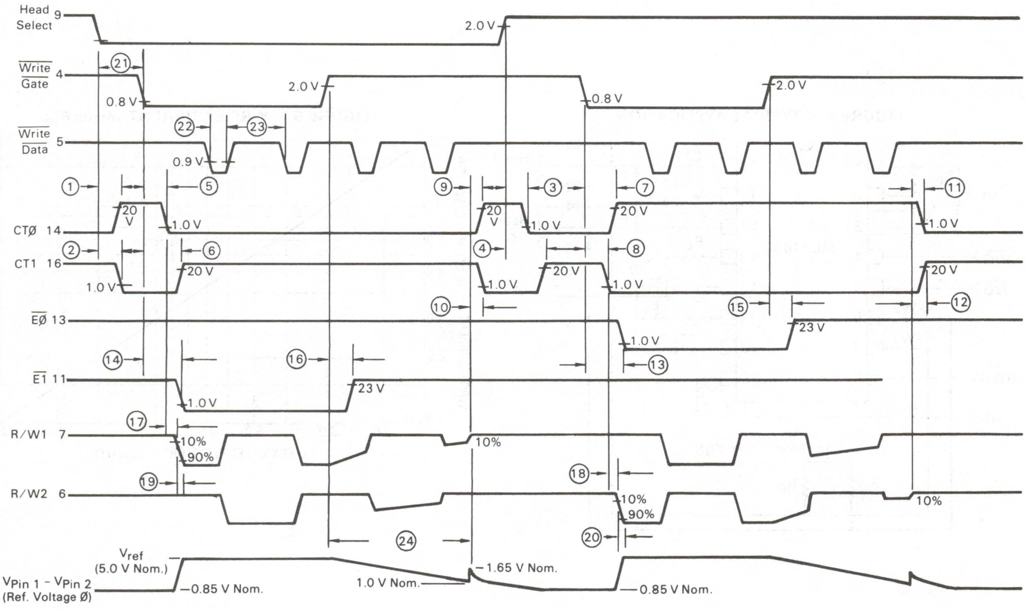
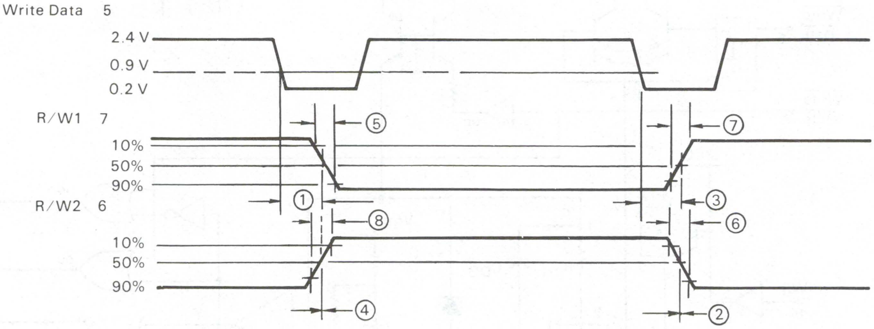

Head Select 9
2.0 V
Write Gate 4
0.8 V
2.0 V
0.8 V
2.0 V
Write Data 5
0.9 V
(21)
(22)
(23)
①
⑤
⑨
③
⑦
⑪
CTØ 14
20 V
1.0 V
20 V
1.0 V
20 V
1.0 V
②
⑥
④
⑧
CT1 16
1.0 V
20 V
1.0 V
20 V
1.0 V
20 V
⑩
⑮
⑫
EØ 13
23 V
1.0 V
⑬
⑭
⑯
E1 11
1.0 V
23 V
⑰
R/W1 7
10%
90%
10%
⑱
⑲
R/W2 6
10%
90%
10%
⑳
(24)
Vref
(5.0 V Nom.)
VPin 1 - VPin 2
(Ref. Voltage Ø)
0.85 V Nom.
1.0 V Nom.
1.65 V Nom.
0.85 V Nom.

FIGURE 3 — R/W1 AND R/W2 RELATIONSHIP


Write Data 5
2.4 V
0.9 V
0.2 V
R/W1 7
10%
50%
90%
R/W2 6
10%
50%
90%
①
②
③
④
⑤
⑥
⑦
⑧

APPLICATION INFORMATION

The MC3469P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3469P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(\text{mA}) = \dfrac{30}{R_{ext}(\text{k}\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

FIGURE 4 — TYPICAL APPLICATION

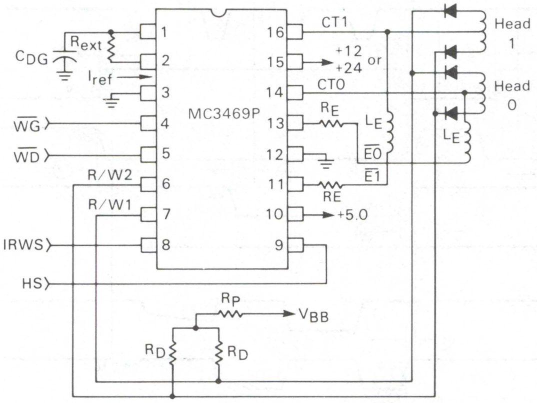
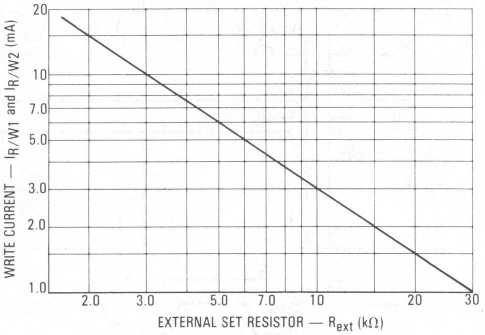

MC3469P
R_{ext}
C_{DG}
I_{ref}
$\overline{WG}$
$\overline{WD}$
R/W2
R/W1
IRWS
HS
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CT1
+12 or +24
CTO
R_E
L_E
$\overline{E0}$
$\overline{E1}$
RE
+5.0
Head 1
Head 0
L_E
R_P
V_{BB}
R_D
R_D

FIGURE 5 — WRITE CURRENT versus R_{ext}



DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from pin 1 to ground. The timing relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into pin 6 or pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus some internal delay times.

POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 µs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

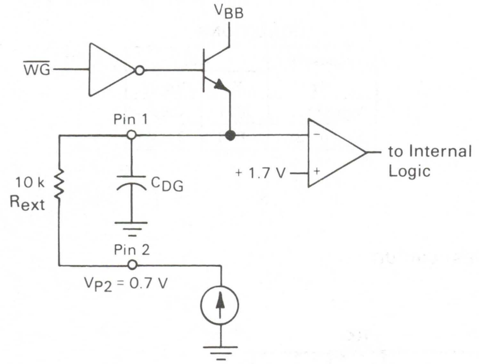


FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})

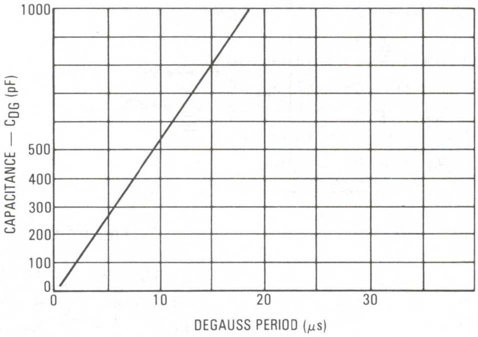
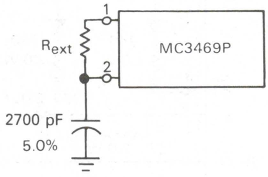
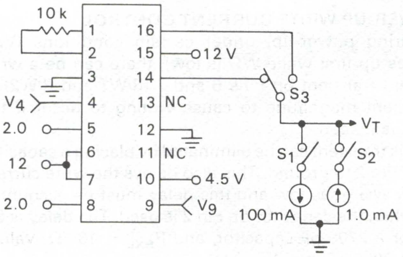


FIGURE 8 — TURN-ON WRITE PROTECTION



TEST FIGURES

FIGURE 9 — CENTER TAP OUTPUT VOLTAGE (PINS 14 AND 16)



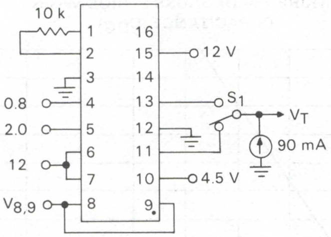
10 k
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12 V
S3
NC
NC
V_T
S_1
S_2
V_4
2.0
12
2.0
4.5 V
V_9
100 mA
1.0 mA

CONDITIONS

Measure	Set				
V_T	S_1	S_2	S_3	V_4*	V_9*
V_{OH} (P14)	On	Off	P14	0.8	2.0
				2.0	0.8
V_{OH} (P16)	On	Off	P16	2.0	2.0
				0.8	0.8
V_{OL} (P14)	Off	On	P14	0.8	0.8
				2.0	2.0
V_{OL} (P16)	Off	On	P16	2.0	0.8
				0.8	2.0

*Volts

FIGURE 10 — ERASE OUTPUT LOW VOLTAGE (PINS 11 AND 13)

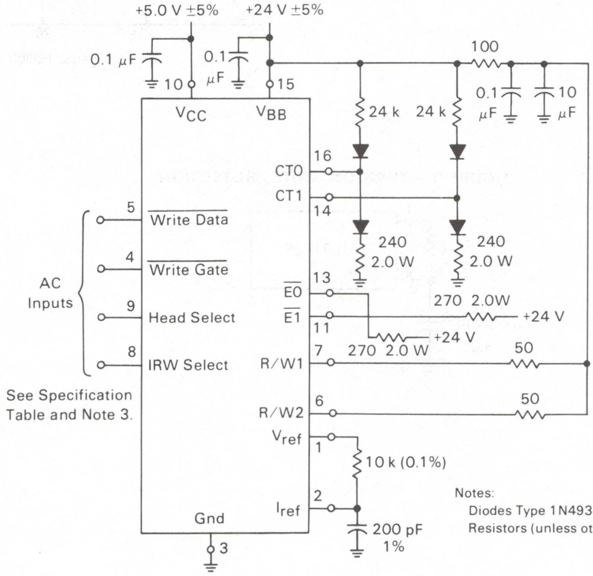


10 k
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12 V
0.8
2.0
12
$V_{8,9}$
S_1
V_T
90 mA
4.5 V

CONDITIONS

Measure	Set	
V_T	S_1	$V_{8,9}$
V_{OL} (P11)	P11	0.8V
V_{OL} (P13)	P13	2.0 V

FIGURE 11 — TIMING TEST CIRCUIT



+5.0 V ±5%
+24 V ±5%
0.1 μF
0.1 μF
10
15
V_{CC}
V_{BB}
100
24 k
24 k
0.1 μF
10 μF
16
CT0
CT1
14
240 2.0 W
240 2.0 W
5
Write Data
4
Write Gate
AC Inputs
9
Head Select
8
IRW Select
13
E0
E1
11
270 2.0W
+24 V
270 2.0 W
+24 V
7
R/W1
50
6
R/W2
50
V_{ref}
1
10 k (0.1%)
2
I_{ref}
200 pF 1%
Gnd
3
See Specification Table and Note 3.

Notes:
Diodes Type 1N4934.
Resistors (unless otherwise noted) are 1/4 W, 5%.

ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)} = 21$ V) and E0 will be low ($V_{OL(max)} = 0.6$ V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired, then:

$$(R_E + 10\ \Omega) \times 40\ \text{mA} = (21 - 0.6)\ \text{V}$$

or

$$R_E = \frac{20.4\ \text{V}}{0.04\ \text{A}} - 10\ \Omega = 500\ \Omega$$

$$P_D = (0.04)\,(20.4) = 0.816\ \text{W or } 1.0\ \text{W}$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as required for inductive back emf suppression.

Erase timing is provided internally and is active during Write Gate low for the selected head.

FIGURE 12 — ERASE CURRENT
(R_E Selection)

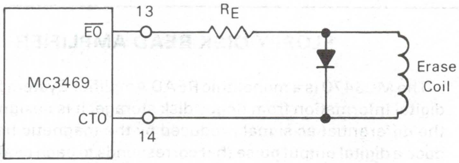
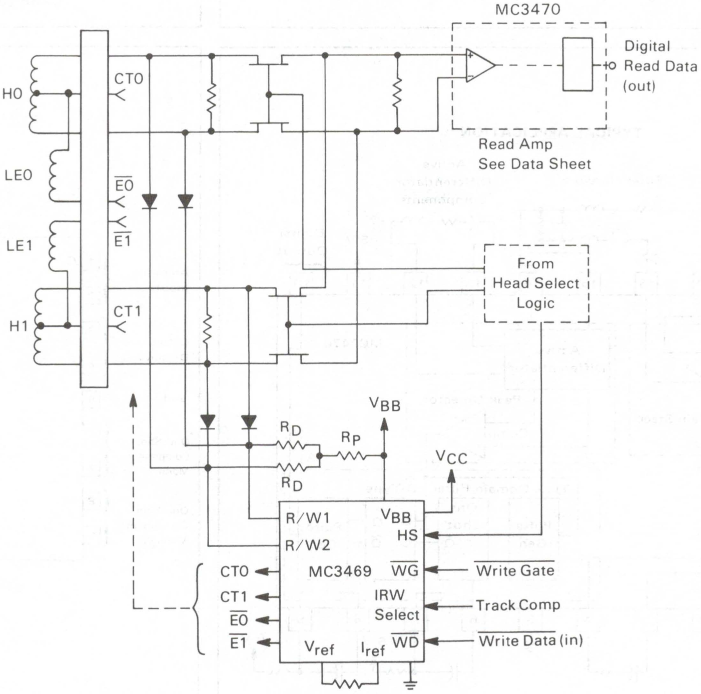

$\overline{\text{E0}}$
13
R_E
MC3469
CT0
14
Erase
Coil

FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3469/MC3470


MC3470
Digital
Read Data
(out)
Read Amp
See Data Sheet
H0
CT0
LE0
$\overline{\text{E0}}$
LE1
$\overline{\text{E1}}$
CT1
H1
From
Head Select
Logic
V_{BB}
R_D
R_P
R_D
V_{CC}
R/W1
R/W2
V_{BB}
HS
MC3469
$\overline{\text{WG}}$
$\overline{\text{Write Gate}}$
IRW
Select
Track Comp
CT0
CT1
$\overline{\text{E0}}$
$\overline{\text{E1}}$
V_{ref}
I_{ref}
$\overline{\text{WD}}$
Write Data (in)

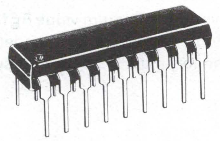
MC3470P
MC3470AP

MOTOROLA

Specifications and Applications Information

FLOPPY DISK READ AMPLIFIER SYSTEM

SILICON MONOLITHIC
INTEGRATED CIRCUIT



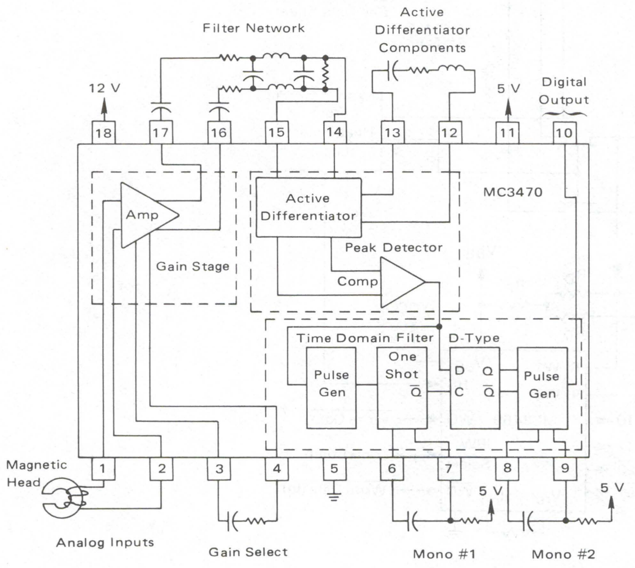
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

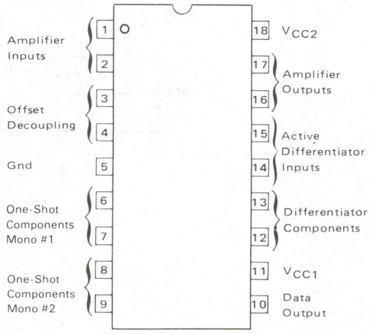
FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode

TYPICAL APPLICATION


Filter Network
Active Differentiator Components
12 V
5 V
Digital Output
18
17
16
15
14
13
12
11
10
MC3470
Amp
Gain Stage
Active Differentiator
Peak Detector
Comp
Time Domain Filter
D-Type
Pulse Gen
One Shot
$\overline{Q}$
D
Q
C
$\overline{Q}$
Pulse Gen
Magnetic Head
1
2
3
4
5
6
7
8
9
5 V
5 V
Analog Inputs
Gain Select
Mono #1
Mono #2


Amplifier Inputs
Offset Decoupling
Gnd
One-Shot Components Mono #1
One-Shot Components Mono #2
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC2}
Amplifier Outputs
Active Differentiator Inputs
Differentiator Components
V_{CC1}
Data Output

ABSOLUTE MAXIMUM RATINGS (Note 1) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V_{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V_I	-0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V_O	-0.2 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package	T_J	150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	V_{CC1} + 4.75 to +5.25 V_{CC2} +10 to +14	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

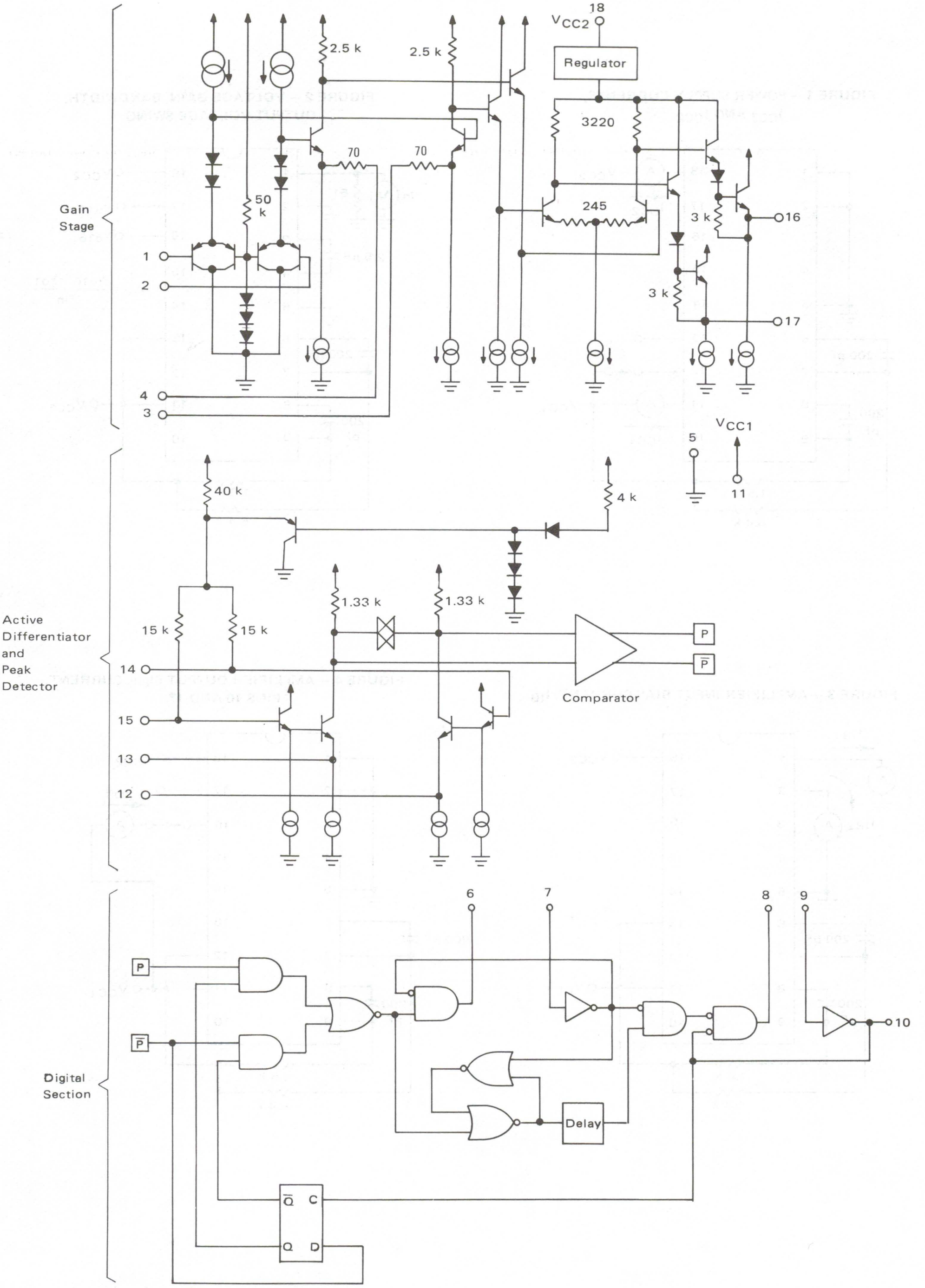
ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain (f = 200 kHz, V_{iD} = 5.0 mV(RMS) MC3470 MC3470A	2	A_{VD}	80 100	100 110	130 130	V/V
Input Bias Current	3	I_{IB}	—	-10	-25	μA
Input Common Mode Range Linear Operation (5% max THD)		v_{iCM}	-0.1	—	1.5	V
Differential Input Voltage Linear Operation (5% max THD)		v_{iD}	—	—	25	mVp-p
Output Voltage Swing Differential	2	v_{oD}	3.0	4.0	—	Vp-p
Output Source Current, Toggled		I_O	—	8.0	—	mA
Output Sink Current, Pins 16 and 17	4	I_{OS}	2.8	4.0	—	mA
Small Signal Input Resistance (T_A = 25°C)		r_i	100	250	—	kΩ
Small Signal Output Resistance, Single-Ended (T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V)		r_o	—	15	—	Ω
Bandwidth, -3.0 dB (v_{iD} = 2.0 mV(RMS), T_A = 25°C V_{CC1} = 5.0 V, V_{CC2} = 12 V)	2, 17	BW	10	—	—	MHz
Common Mode Rejection Ratio (T_A = 25°C, f = 100 kHz, A_{VD} = 40 dB, v_{in} = 200 mVp-p, V_{CC1} = 5.0 V, V_{CC2} = 12 V)	5	CMRR	50	—	—	dB
V_{CC1} Supply Rejection Ratio (T_A = 25°C, V_{CC2} = 12 V, $4.75 \leqslant V_{CC1} \leqslant 5.25$ V, A_{VD} = 40 dB)		—	50	—	—	dB
V_{CC2} Supply Rejection Ratio (T_A = 25°C, V_{CC1} = 5.0 V, $10\ V \leqslant V_{CC2} \leqslant 14$ V, A_{VD} = 40 dB)		—	60	—	—	dB
Differential Output Offset (T_A = 25°C, v_{iD} = v_{in} = 0 V)		V_{DO}	—	—	0.4	V
Common Mode Output Offset (v_{iD} = V_{in} = 0 V, Differential and Common Mode)		V_{CO}	—	3.0	—	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T_A = 25°C)	22	e_n	—	15	—	μV(RMS)
Supply Currents (V_{CC1} = 5.25 V, S_1 to Pin 12 or Pin 13) (V_{CC2} = 14 V)	1	I_{CC1} I_{CC2}	— —	40 4.8	— —	mA

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 (V_{OD} = V_{CC1})	6	I_{OD}	1.0	1.4		mA
Peak Shift (f = 250 kHz, v_{iD} = 1.0 Vp-p, i_{cap} = 500 μA, where $PS = 1/2 \frac{t_{PS1}-t_{PS2}}{t_{PS1}+t_{PS2}} \times 100\%$, MC3470	7, 8	PS	—	—	5.0	%
V_{CC1} = 5.0 V, V_{CC2} = 12 V) MC3470A			—	—	2.0	
Differentiator Input Resistance, Differential		r_{iD}	—	30	—	kΩ
Differentiator Output Resistance, Differential (T_A = 25°C)		r_{oD}	—	40	—	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = −0.4 mA)	9	V_{OH}	2.7	—	—	V
Output Voltage Low Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8.0 mA)	10	V_{OL}	—	—	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	—	—	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	—	—	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A, B}$	500	—	4000	ns
Timing Accuracy Mono #1 (t1 = 1.0 μs = 0.625 R1C1 + 200 ns) (R1 = 6.4 kΩ, C1 = 200 pF) Accuracy guaranteed for R1 in the range 1.5 kΩ ≤ R1 ≤ 10 kΩ and C1 in the range 150 pF ≤ C1 ≤ 680 pF. Note: To minimize current transients, C1 should be kept as small as is convenient.	12, 13	E_{t1}	85	—	115	%
Timing Range Mono #2	11, 12	t2	150	—	1000	ns
Timing Accuracy Mono #2 (t2 = 200 ns = 0.625 R2C2) (R2 = 1.6 kΩ, C2 = 200 pF) Accuracy guaranteed for 1.5 kΩ ≤ R2 ≤ 10 kΩ, 100 pF ≤ C2 ≤ 800 pF	12, 13	E_{t2}	85	—	115	%

MC3470 CIRCUIT SCHEMATIC



Vcc2
18
Regulator
2.5 k
2.5 k
70
70
3220
245
50 k
3 k
3 k
16
17
Gain Stage
1
2
4
3
5
Vcc1
11
40 k
4 k
1.33 k
1.33 k
15 k
15 k
P
P̄
Comparator
Active Differentiator and Peak Detector
14
15
13
12
6
7
8
9
10
Delay
Q̄
C
Q
D
Digital Section

FIGURE 1 — POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

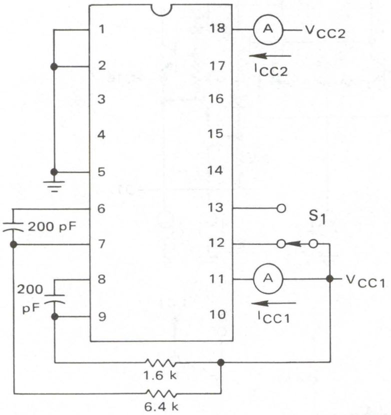

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
A
V_{CC2}
I_{CC2}
S_1
A
V_{CC1}
I_{CC1}
200 pF
200 pF
1.6 k
6.4 k

FIGURE 2 — VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

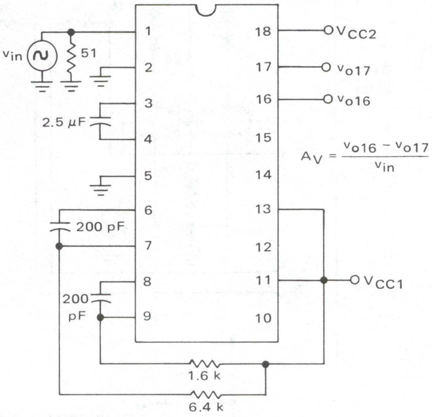

v_{in}
51
2.5 μF
200 pF
200 pF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
V_{CC2}
v_{o17}
v_{o16}
$A_V = \frac{v_{o16} - v_{o17}}{v_{in}}$
V_{CC1}
1.6 k
6.4 k

FIGURE 3 — AMPLIFIER INPUT BIAS CURRENT, I_{IB}

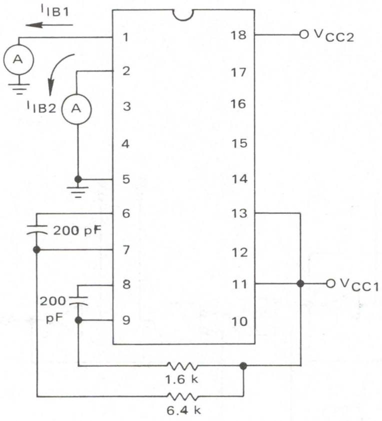

I_{IB1}
A
I_{IB2}
A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
V_{CC2}
V_{CC1}
200 pF
200 pF
1.6 k
6.4 k

FIGURE 4 — AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17

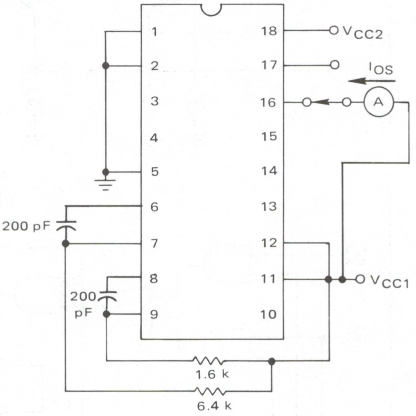
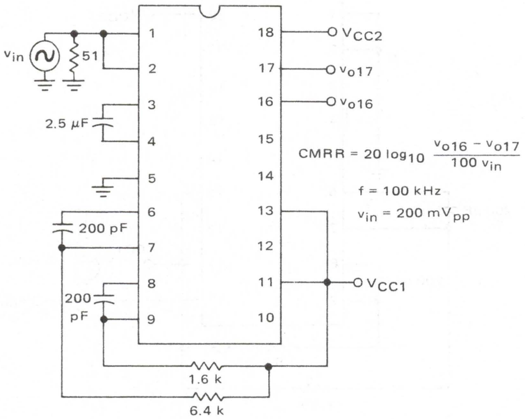

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
V_{CC2}
I_{OS}
A
V_{CC1}
200 pF
200 pF
1.6 k
6.4 k

FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR


vin
51
2.5 µF
200 pF
200 pF
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
VCC2
vo17
vo16
CMRR = 20 log10 (vo16 − vo17)/(100 vin)
f = 100 kHz
vin = 200 mVpp
VCC1
1.6 k
6.4 k

NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

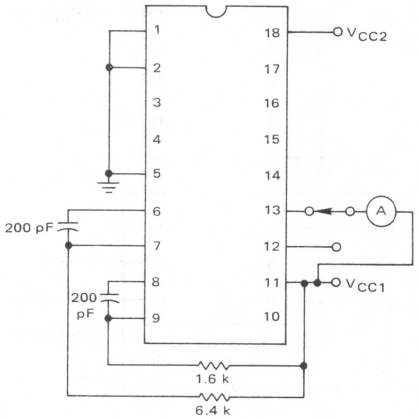

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
VCC2
A
VCC1
200 pF
200 pF
1.6 k
6.4 k

FIGURE 7 – PEAK SHIFT, PS

See Figure 8 for Output Waveform

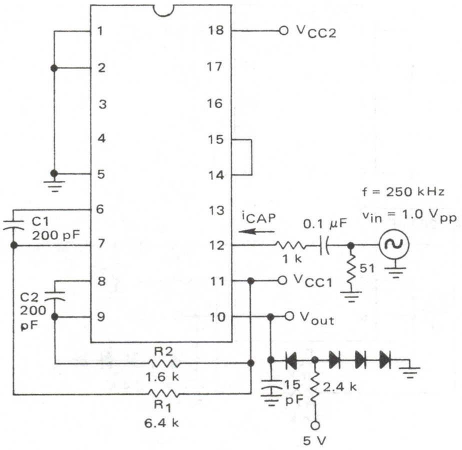
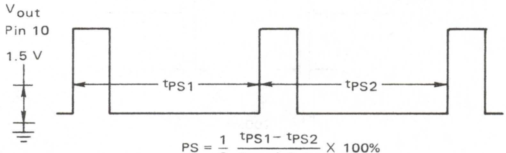

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
VCC2
C1 200 pF
C2 200 pF
iCAP
0.1 µF
f = 250 kHz
vin = 1.0 Vpp
1 k
51
VCC1
Vout
R2 1.6 k
R1 6.4 k
15 pF
2.4 k
5 V

FIGURE 8 – PEAK SHIFT, PS

$V_{in} = 1.0\ V_{pp}$ $f = 250\text{ kHz}$

Test schematic on Figure 7


Vout
Pin 10
1.5 V
tPS1
tPS2

$$PS = \frac{1}{2}\ \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$$

FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

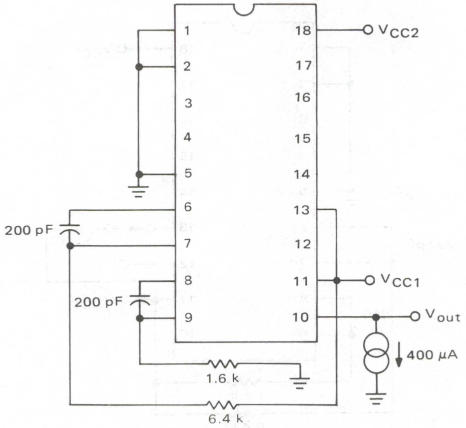

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC2}
V_{CC1}
V_{out}
200 pF
200 pF
400 μA
1.6 k
6.4 k

FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

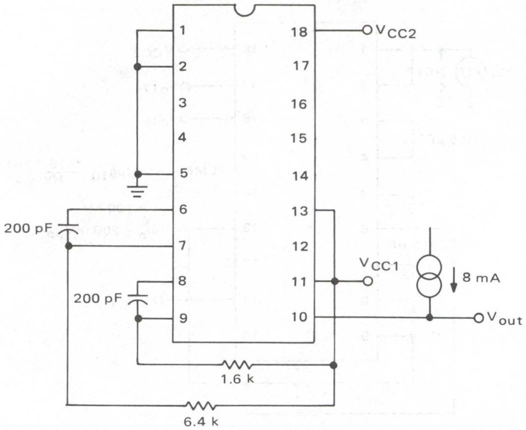
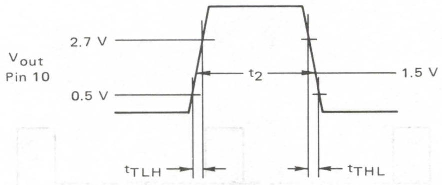

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC2}
V_{CC1}
V_{out}
8 mA
200 pF
200 pF
1.6 k
6.4 k

FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{t2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12


V_{out}
Pin 10
2.7 V
0.5 V
1.5 V
t_2
t_{TLH}
t_{THL}

$$E_{t2} = \frac{t_2}{200\ \text{ns}} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

V_{in} shown on Figure 13

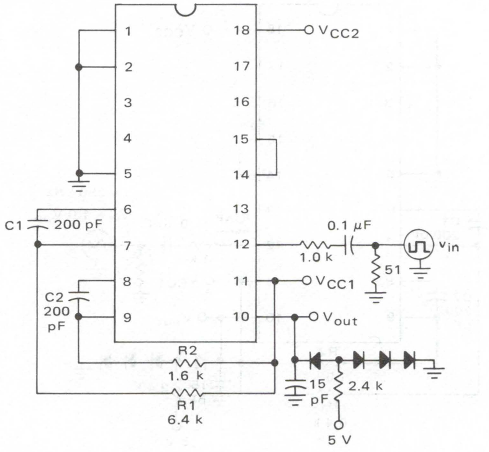
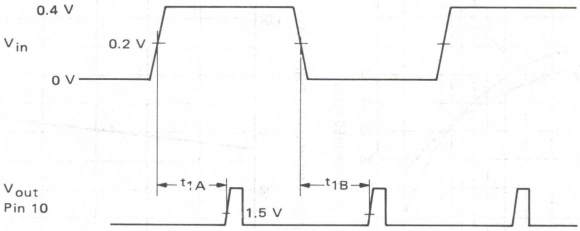

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC2}
V_{CC1}
V_{out}
v_{in}
C1
200 pF
C2
200
pF
0.1 μF
1.0 k
51
R2
1.6 k
R1
6.4 k
15
pF
2.4 k
5 V

FIGURE 13 – TIMING ACCURACY MONO #1, E_{t1}

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

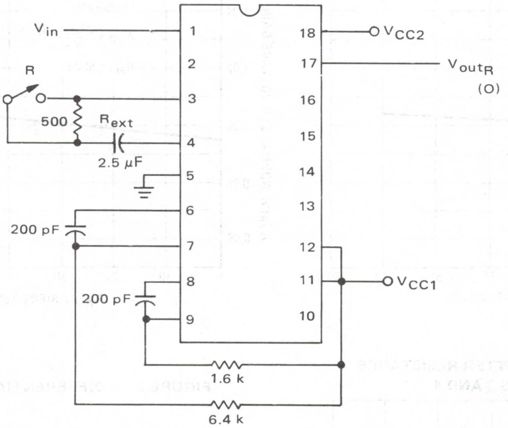

0.4 V
V_{in}
0.2 V
0 V
V_{out}
Pin 10
t_{1A}
t_{1B}
1.5 V

$$E_{t1A} = \frac{t_{1A}}{1000\ \text{ns}} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\ \text{ns}} \times 100\%$$

FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500\ \Omega$


V_{in}
R
500
R_{ext}
2.5 μF
200 pF
200 pF
1.6 k
6.4 k
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC2}
V_{outR}
(O)
V_{CC1}

f = 250 kHz

V_{in} = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{V_O}}{A_{V_R}} - 1\right)}$$

$$= \frac{500\ \Omega}{2\left(\frac{V_{out_O}}{V_{out_R}} - 1\right)}$$

FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT (I_{CC}/I_{CC} 25°C) versus TEMPERATURE

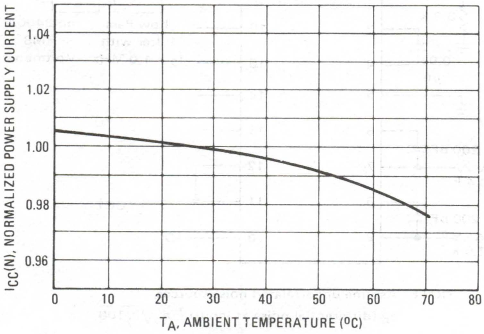


FIGURE 16 – NORMALIZED VOLTAGE GAIN (A_V/A_V 25°C) versus TEMPERATURE

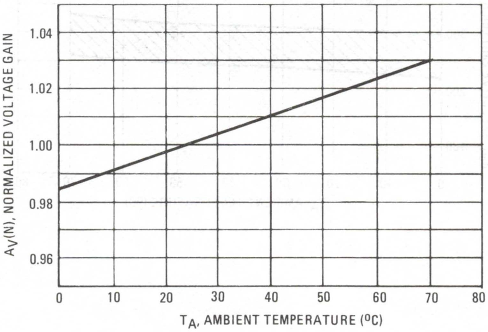


FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

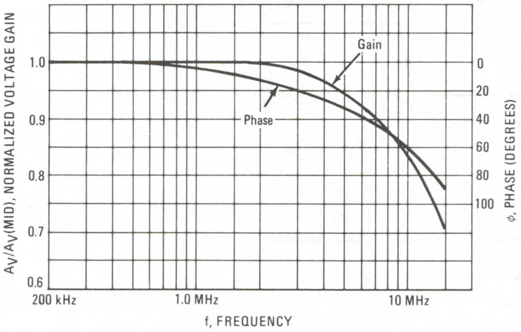


FIGURE 18 – NORMALIZED TIME DELAY t_1 versus TEMPERATURE

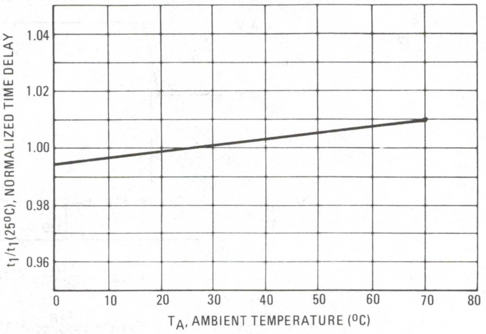


FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, t_2/t_2 25°C

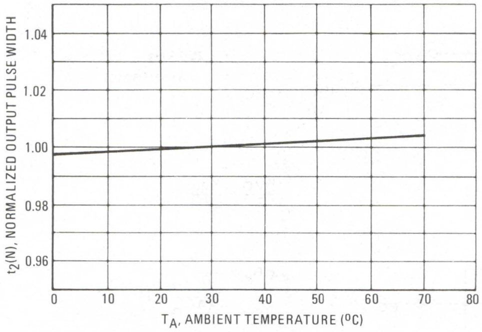


FIGURE 20 – NORMALIZED VOLTAGE GAIN, A_{VR}/A_{VR} 25°C

See Figure 14, Switch Position R

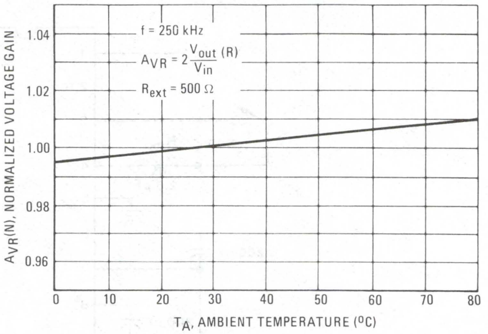


FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

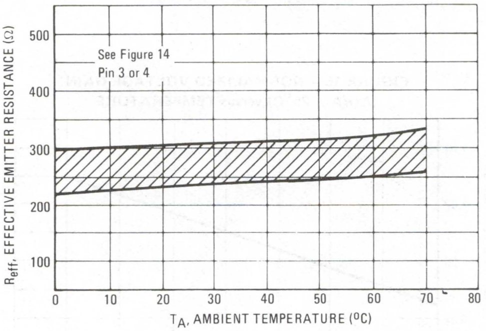
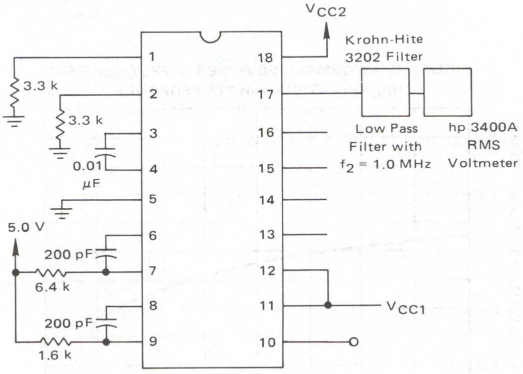


FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE



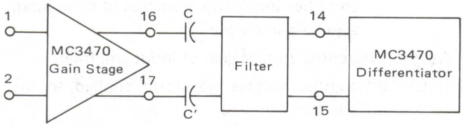
V_{CC2}
Krohn-Hite 3202 Filter
Low Pass Filter with f_2 = 1.0 MHz
hp 3400A RMS Voltmeter
3.3 k
3.3 k
0.01 µF
5.0 V
200 pF
6.4 k
200 pF
1.6 k
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC1}

NOTE: Assume uncorrelated noise sources
e_n (differential noise at input) = $e_o\sqrt{2/100}$

APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a), enabling the active differentiator and time domain filter to produce the desired output.

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C′ are placed before the filter as shown in Figure 23a. The charging and discharging of C and C′ is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic — Pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_p A_{VD})\ max}{2.8\ mA}$$

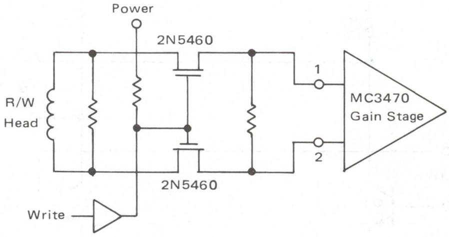
where E_p is the peak differential input voltage to the MC3470.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between Pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$A_{VR} = A_{VO} \cdot \frac{2\,(r_e + R_e)}{2\,(r_e + R_e) + R_{ext}}$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,
$A_{VR} \triangleq$ voltage gain with the external resistor in,
$R_{ext} \triangleq$ the external resistor, and
$r_e + R_e \triangleq$ the resistance looking into Pin 3 or Pin 4.

Thus,

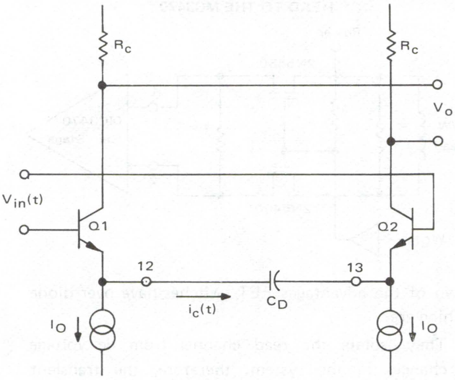
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

FIGURE 24 – ACTIVE DIFFERENTIATOR NETWORK



$$I = C\,dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

V_o is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_p \triangleq$ peak differential voltage applied to MC3470 amplifier input.

$E_p \sin \omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

$A_{VD} \triangleq$ differential voltage gain of input amplifier.

$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.

$= E_p A_{VD} \sin \omega t$ (Note: The filter is assumed to be lossless.)

$i_c(t) \triangleq$ current through capacitor C_D.

$R_O \triangleq$ output resistance of Q1 (Q2) at Pin 12 (13).

If $v_{in}(t) = E_p A_{VD} \sin \omega t$, then the current through the capacitor C_D is given by

$$i_c(t) = C_D A_{VD} E_p \omega \cos \omega t$$

$$\text{and } V_O(t) = 2R_C C_D A_{VD} E_p \omega \cos \omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω, the maximum slew rate occurs for the maximum value of i_c or $\cos \omega t = 1$. Therefore,

$$i_c = C_D A_{VD} E_p \omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_c; therefore, C_D must be chosen such that the maximum i_c occurs at the maximum $A_{VD} E_p \omega$ product.

$$C_D = \frac{i_c\text{max}}{(A_{VD} E_p \omega)_{max}} = \frac{1\text{ mA}}{(120)(E_p \omega)_{max}}$$

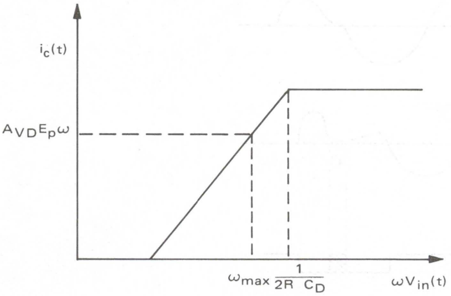
If the peak value specified for i_c is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at Pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2\,R_O C_D$. If this pole is ten times greater than the maximum operating frequency (ω_{max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 ω_{max} needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\, 10\, \omega_{max}}.$$

If R_O is not large enough to satisfy this condition, a series

FIGURE 25 – RESPONSE OF DIFFERENTIATOR USING ONLY C_D

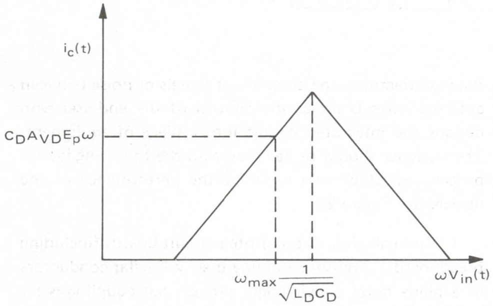


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\, 10\, \omega_{max}}$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_o) and the damping ratio (δ) to meet the systems requirements where

FIGURE 26 – COMPLETE RESPONSE OF DIFFERENTIATOR



$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\, \omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100\, C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

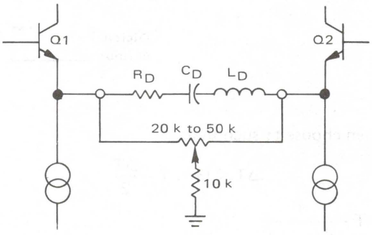
$$R = \frac{\delta}{5\, C_D\, \omega_{max}}$$

The total resistance (R) is the effective output resistance (R_O) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 – PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at Pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on Pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

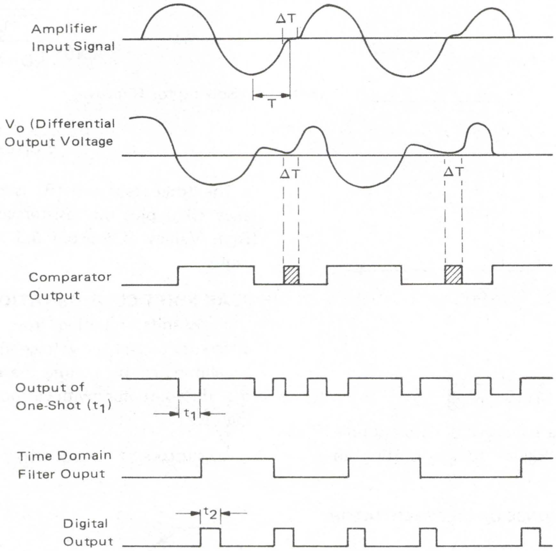
$$t_1 = R_1C_1K_1 + T_o$$

where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 < T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse t_2 (Pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1, R_2, C_1, and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For $t_1 = 1\ \mu s$ and $t_2 = 200$ ns, suggested good values for the capacitors are

$$C_1 = 250\text{ pF}$$

$$C_2 = 160\text{ pF}$$

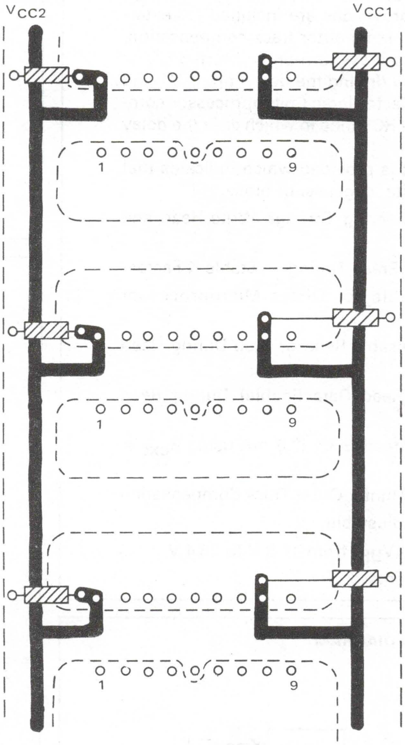
BOARD LAYOUT AND TESTING CONSIDERATIONS

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.

MC3471P

MOTOROLA

Specifications and Applications Information

FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

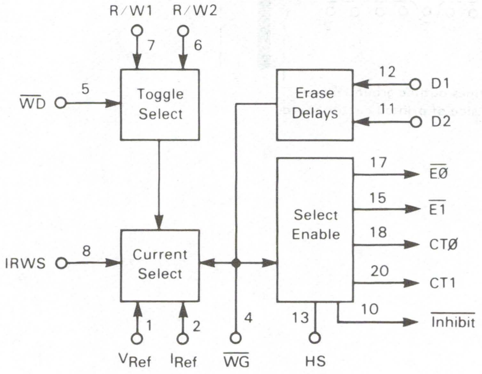
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

In addition, an Inhibit output is provided which indicates that the heads are active during write, degauss, or erase.

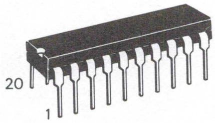
- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- Inhibit Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed ±3% (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Innter/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components

BLOCK DIAGRAM


R/W1
R/W2
7
6
WD
5
Toggle Select
Erase Delays
12
D1
11
D2
17
E0
15
E1
Select Enable
18
CT0
20
CT1
IRWS
8
Current Select
10
Inhibit
1
2
4
13
VRef
IRef
WG
HS

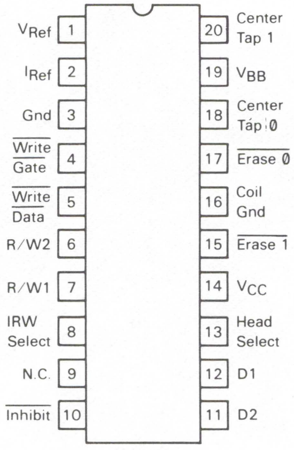
FLOPPY DISK
WRITE CONTROLLER
(WITH ERASE DELAY)

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN CONNECTIONS


VRef 1
IRef 2
Gnd 3
Write Gate 4
Write Data 5
R/W2 6
R/W1 7
IRW Select 8
N.C. 9
Inhibit 10
20 Center Tap 1
19 VBB
18 Center Tap 0
17 Erase 0
16 Coil Gnd
15 Erase 1
14 VCC
13 Head Select
12 D1
11 D2

(Top View)

ABSOLUTE MAXIMUM RATINGS (Note 1) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 13)	V_I	5.75	Vdc
Output Applied Voltage (Pin 10)	V_O	7.0	Vdc
Open-Collector Sink Current (Pin 10)	I_O	25	mA
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Junction Temperature	T_J	150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	+4.75 to +5.25	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	60 30	mA
High Level Input Voltage (V_{CC} = 4.75 V)	4, 8, 13	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.25 V)	4, 8, 13	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = -12 mA)	4, 5, 8, 13	V_{IK}	—	-0.87	-1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$)		V_{HTS}				V
T_A = 0°C to +70°C	5		0.2	—	—	
T_A = 25°C			0.4	0.76	—	
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 13	I_{IH}	—	0.1	40	µA
Low Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)	4, 5, 8, 13	I_{IL}	—	—	-1.6	mA
V_{BB} = 12 V	4		—	0.36	—	
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 13		—	0.39	—	

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 14) (I_{OH} = −100 mA, V_{CC} = 4.75 V) V_{BB} = 10.8 to 26.4 V	18, 20	V_{OH}	V_{BB}-1.5	V_{BB}-1.0	—	V
Output Low Voltage (See Figure 14) (I_{OL} = 1.0 mA)	18, 20	V_{OL}				mV
V_{BB} = 12 V			—	70	150	
V_{BB} = 24 V			—	70	150	
Output High Leakage Current (V_{OH} = 24 V, V_{CC} = 4.75 V, V_{BB} = 24 V)	15, 17	I_{OH}	—	0.01	100	µA
Output Low Voltage (See Figure 15) (I_{OL} = 90 mA, V_{CC} = 4.75 V)	15, 17	V_{OL}				V
V_{BB} = 12 V			—	0.27	0.60	
V_{BB} = 24 V			—	0.27	0.60	
DIGITAL OUTPUT LEVEL $(\overline{\text{Inhibit}})$						
High Level Output Current (V_{OH} = 7.0 V, V_{CC} = 4.75 V)	10	I_{OH}	—	—	100	µA
Low Level Output Voltage (I_{OL} = 4.0 mA, V_{CC} = 4.75 V)	10	V_{OL}	—	—	0.5	V
CURRENT SOURCE						
Reference Voltage	1	V_{Ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 – Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 30 V)	6, 7	I_{OH}	—	0.03	15	µA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,\,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	ΔI/RW2, 1	—	15	40	µA
Average Value Write Current $\left(\frac{(I_{Pin\,6} + I_{Pin\,7})}{2}\right.$ for V_{BB} = 10.8 to 26.4 V)	6, 7					
@ $I_{R/W}$ = I_{LOW}, R = 10 k		$\overline{I_{R/W(L)}}$				mA
T_A = 25°C			2.91	3.0	3.09	
T_A = 0 to +70°C			2.84	—	3.16	
@ $I_{R/W}$ = I_{LOW}, R = 5.0 k						
T_A = 25°C			5.64	5.89	6.14	
T_A = 0 to +70°C			5.51	—	6.28	
@ $I_{R/W}$ = I_{HI}, R = 10 k (I_{HI} = I_{LOW} + % I_{LOW})		$\overline{\Delta I_{R/W(H)}}$				%
T_A = 25°C			31.3	33.3	35.5	
T_A = 0 to +70°C			30.3	33.3	36.6	
Difference in Write Current ($\lvert I_{Pin\,6} - I_{Pin\,7}\rvert$ @ $I_{R/W}$ = I_{LOW}, V_{BB} = 10.8 V to 26.4 V) R = 10 k	6, 7	$I_{R/W\Delta}$				mA
T_A = 25°C			—	0.003	0.015	
T_A = 0 to +70°C			—	—	0.023	
R = 5.0 k						
T_A = 25°C			—	—	0.030	
T_A = 0 to +70°C			—	—	0.046	

ERASE DELAY ACCURACY (V_{CC} = 4.75 to 5.25 V, T_A = 0 to +70°C, V_{BB} = 10.8 to 26.4 V, — refer to Figure 9.)

Characteristics	Test	Min	Typ	Max	Unit
Delay Error, Pin 11, 12 D1, D2 = RC $\pm E_{D1,2}$, 30 kΩ ≤ R ≤ 300 kΩ	$E_{D1,2}$	—	—	15	%

AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted.)

Characteristics (Note 2)	f_{in} (Note 3)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 13	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.0 V to CT0 going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	μs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	μs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	μs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	μs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	μs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. After $\overline{WG}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
14. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
15. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
16. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
17. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	μs
18. Write Data low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
19. Write Data high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
20. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	μs
21. Delay from $\overline{WG}$ going low thru 0.8 V to $\overline{Inhibit}$ going low thru 0.5 V (Note 5)	$\overline{WG}$, Pin 4	—	0.08	4.0	μs
22. After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{Inhibit}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 5)	$\overline{WG}$, Pin 4	20	750	—	ns
23. After $\overline{WG}$ goes high, delay from $\overline{E1}$ going high thru 23 V to $\overline{Inhibit}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 5)	$\overline{WG}$	20	750	—	ns

Note 2: Test numbers refer to encircled numbers in Figures 3 & 16.

Note 3: AC test waveforms applied to the designated pins as follows:

Note 4: 22. or 23., whichever produces the longer delay, will control $\overline{Inhibit}$.

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

AC SWITCHING CHARACTERISTICS (continued)

(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{\text{WG}}$ = 0.4 unless otherwise noted)

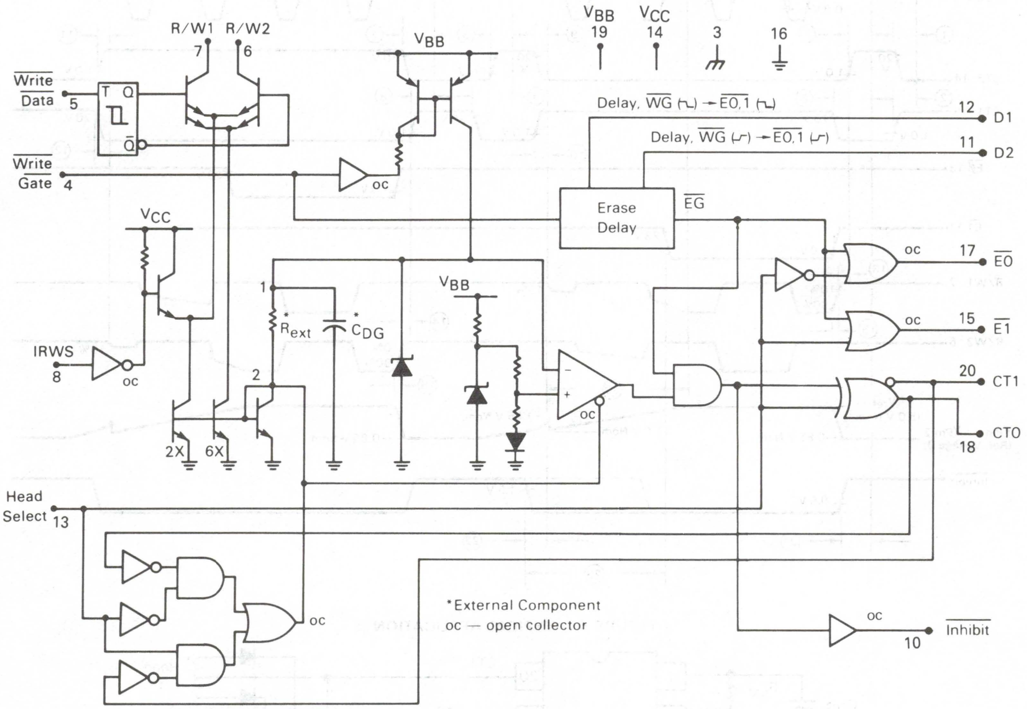
Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after Write Data going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after Write Data going low through 0.9 V.	—	1.0	±40	ns
5. Fall time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Fall time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Rise time, 90% to 10%, of R/W1	—	12	200	ns
8. Rise time, 90% to 10%, of R/W2	—	12	200	ns

Note 5: Test numbers refer to encircled numbers in Figures 2 & 15.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	13	Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{\text{WG}}$	4	Write Gate input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{\text{WD}}$	5	Write Data input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{Ref} I_{Ref}	V_{Ref} I_{Ref}	1 2	A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from V_{Ref} to Gnd will adjust the Degauss period.
Center-Tap 0	CT0	18	Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{\text{E0}}$	17	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-Tap 1	CT1	20	Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{\text{E1}}$	15	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	14	+5.0 V Power
	V_{BB}	19	+12 V or + 24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground
Delay 1	D1	12	Erase Turn-On Delay adjust (RC or Logic)
Delay 2	D2	11	Erase Turn-Off Delay adjust (RC or Logic)
Inhibit	$\overline{\text{Inhibit}}$	10	Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.)

FIGURE 1 — LOGIC DIAGRAM


R/W1
R/W2
7
6
VBB
VBB 19
VCC 14
3
16
Write Data 5
T Q
Q̄
Write Gate 4
oc
Delay, WG (⌐_) → E0,1 (⌐_)
12
D1
Delay, WG (_⌐) → E0,1 (_⌐)
11
D2
Erase Delay
EG
VCC
1
* Rext
* CDG
VBB
oc
17
E0
oc
15
E1
IRWS 8
oc
2
oc
20
CT1
CT0
18
2X
6X
Head Select 13
oc
oc
Inhibit
10

*External Component
oc — open collector

FIGURE 2 — R/W1 AND R/W2 RELATIONSHIP

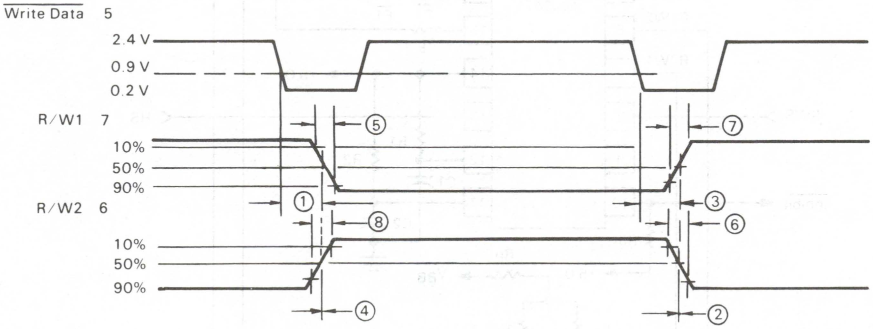
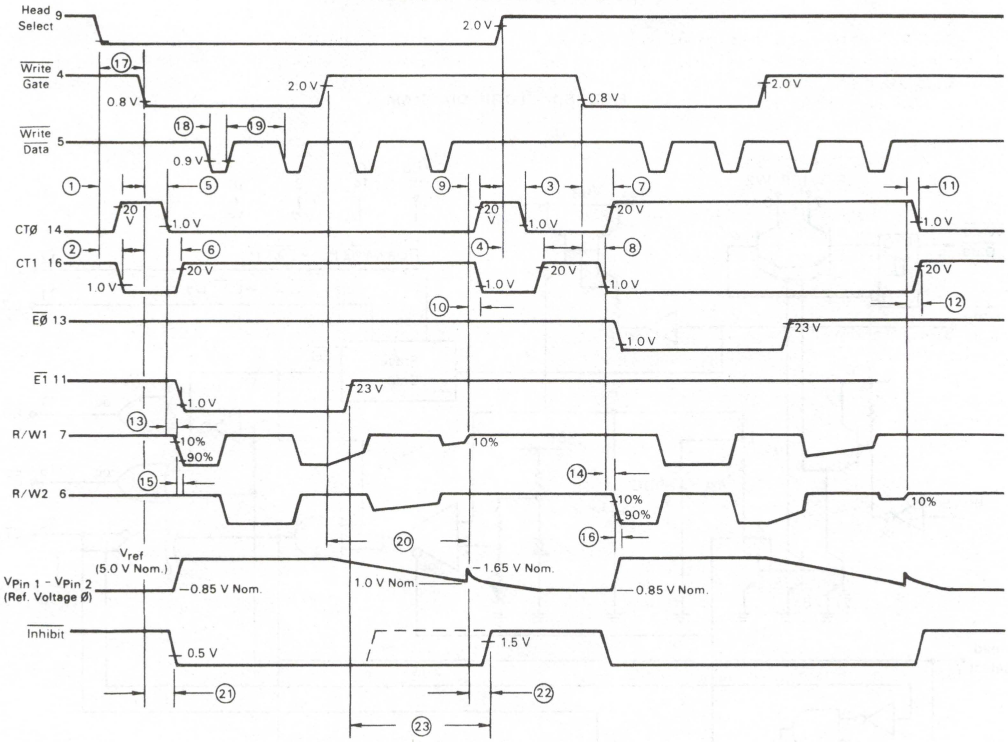

Write Data 5
2.4 V
0.9 V
0.2 V
R/W1 7
10%
50%
90%
R/W2 6
10%
50%
90%
①
②
③
④
⑤
⑥
⑦
⑧

FIGURE 3 — AC TIMING DIAGRAM


Head Select 9
Write Gate 4
Write Data 5
CTØ 14
CT1 16
EØ 13
E1 11
R/W1 7
R/W2 6
Vref (5.0 V Nom.)
VPin 1 - VPin 2 (Ref. Voltage Ø)
Inhibit
2.0 V
0.8 V
0.9 V
20 V
1.0 V
23 V
10%
90%
−0.85 V Nom.
1.0 V Nom.
−1.65 V Nom.
0.5 V
1.5 V
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
⑫
⑬
⑭
⑮
⑯
⑰
⑱
⑲
⑳
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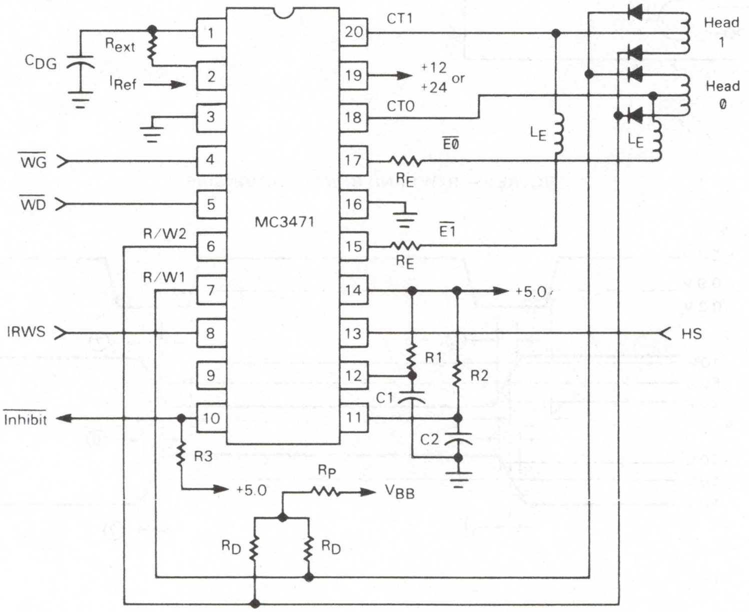
㉓

FIGURE 4 — TYPICAL APPLICATION


MC3471
CDG
Rext
IRef
WG
WD
R/W2
R/W1
IRWS
Inhibit
R3
+5.0
RP
VBB
RD
RD
CT1
+12 or +24
CTO
EØ
RE
E1
RE
+5.0
HS
R1
R2
C1
C2
LE
LE
Head 1
Head Ø
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

APPLICATION INFORMATION

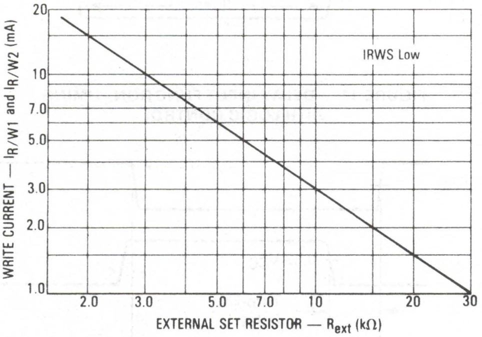
The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(\text{mA}) = \dfrac{30}{R_{ext}(\text{k}\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

FIGURE 5 — WRITE CURRENT versus R_{ext}



WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

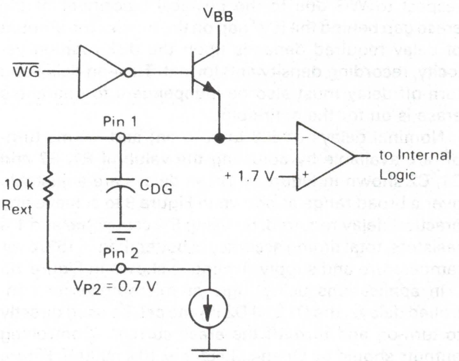
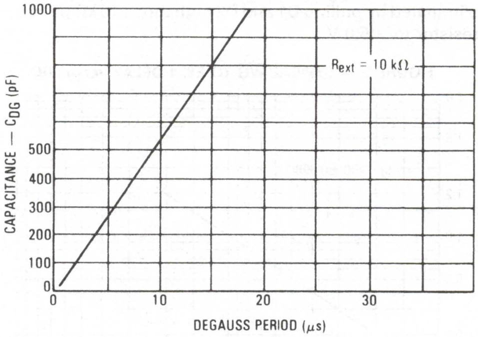


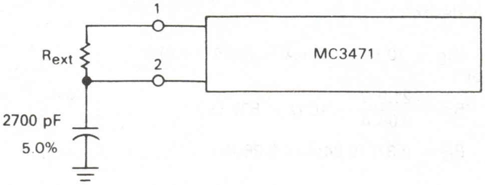
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})



POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.



ERASE DELAY

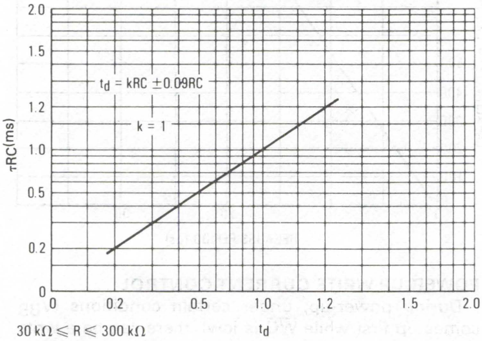
The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to $\overline{WG}$ due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μs turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than ±15% over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 kΩ pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL $\overline{WG}$ TO E0, 1 DELAY versus RC



ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)}$ = 22.5 V) and E0 will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10\ \Omega) \times 40\ \text{mA} = (22.5 - 0.6)\ \text{V}$$

or

$$R_E = \frac{21.9\ \text{V}}{0.04\ \text{A}} - 10\ \Omega = 537\ \Omega$$

$$P_D = (537)\,(0.04)^2 = 0.86\ \text{W}$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

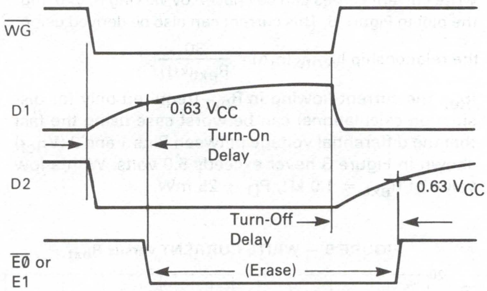


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

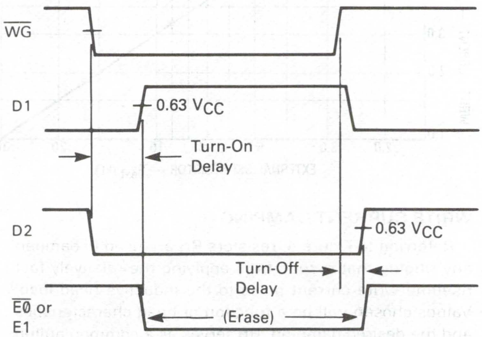


FIGURE 12 — ERASE CURRENT (R_E Selection)

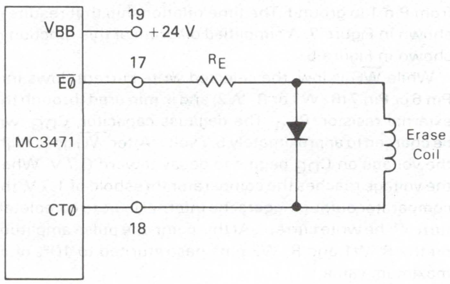
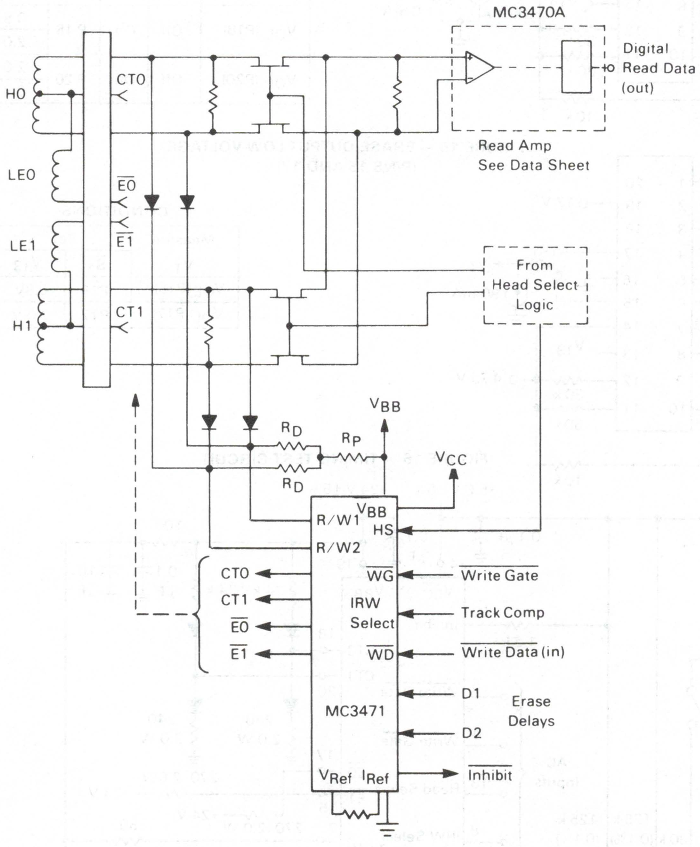


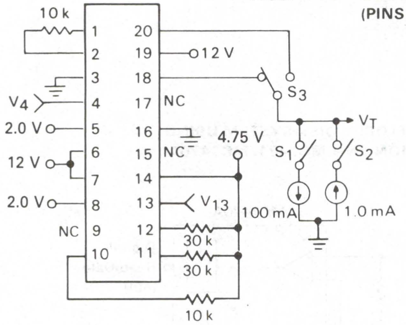
FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A


MC3470A
Digital
Read Data
(out)
Read Amp
See Data Sheet
H0
CT0
LE0
$\overline{E0}$
LE1
$\overline{E1}$
From
Head Select
Logic
CT1
H1
V_{BB}
R_D
R_P
V_{CC}
R_D
R/W1
V_{BB}
HS
R/W2
CT0
CT1
$\overline{E0}$
$\overline{E1}$
$\overline{WG}$
$\overline{\text{Write Gate}}$
IRW
Select
Track Comp
$\overline{WD}$
$\overline{\text{Write Data}}$ (in)
D1
Erase
Delays
MC3471
D2
V_{Ref}
I_{Ref}
$\overline{\text{Inhibit}}$

Function	CT0	CT1	E0	E1
Write 0	V_{BB}	0 V	On	Off
Write 1	0 V	V_{BB}	Off	On
Read 0	0 V	V_{BB}	Off	Off
Read 1	V_{BB}	0 V	Off	Off

TEST FIGURES

FIGURE 14 — CENTER TAP OUTPUT VOLTAGE (PINS 18 AND 20)



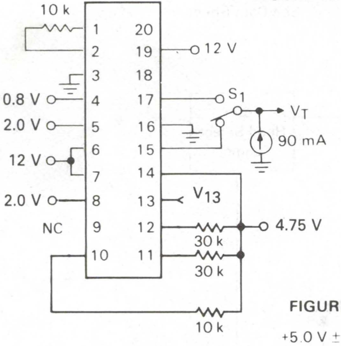
10 k
1
2
3
V4
4
2.0 V
5
12 V
6
7
2.0 V
8
NC
9
10
20
19
12 V
18
17
NC
16
4.75 V
15
NC
14
13
V13
12
30 k
11
30 k
10 k
S3
VT
S1
S2
100 mA
1.0 mA

CONDITIONS

Measure V_T	Set S_1	S_2	S_3	V_4*	V_{13}*
V_{OH} (P18)	On	Off	P 18	0.8	2.0
				2.0	0.8
V_{OH} (P20)	On	Off	P 20	2.0	2.0
				0.8	0.8
V_{OL} (P18)	Off	On	P 18	0.8	0.8
				2.0	2.0
V_{OL} (P20)	Off	On	P 20	2.0	0.8
				0.8	2.0

*Volts

FIGURE 15 — ERASE OUTPUT LOW VOLTAGE (PINS 15 AND 17)

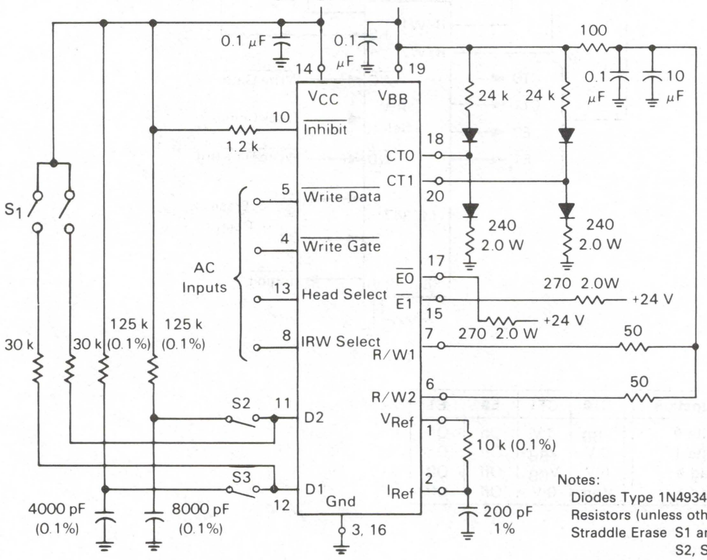


10 k
1
2
3
0.8 V
4
2.0 V
5
12 V
6
7
2.0 V
8
NC
9
10
20
19
12 V
18
17
S1
VT
16
90 mA
15
14
13
V13
12
4.75 V
30 k
11
30 k
10 k

CONDITIONS

Measure V_T	Set S_1	V_{13}
V_{OL} (P15)	P15	0.8V
V_{OL} (P17)	P17	2.0 V

FIGURE 16 — TIMING TEST CIRCUIT



+5.0 V ±5%
+24 V ±5%
0.1 μF
0.1 μF
14
19
100
0.1 μF
10 μF
VCC
VBB
24 k
24 k
10
Inhibit
1.2 k
18
CT0
CT1
20
5
Write Data
240 2.0 W
240 2.0 W
4
Write Gate
S1
AC Inputs
13
Head Select
17
E0
E1
270 2.0W
+24 V
15
+24 V
270 2.0 W
8
IRW Select
R/W1
7
50
30 k
30 k
125 k (0.1%)
125 k (0.1%)
6
R/W2
50
S2
11
D2
VRef
1
10 k (0.1%)
S3
2
D1
Gnd
IRef
12
4000 pF (0.1%)
8000 pF (0.1%)
3, 16
200 pF 1%

Notes:
Diodes Type 1N4934
Resistors (unless otherwise noted) are 1/4 W 5%
Straddle Erase S1 and S_4 Closed
S2, S3 Open
Tunnel Erase S1 and S_4 Open
S2, S3 Closed

MC3480

Specifications and Applications Information

DYNAMIC MEMORY CONTROLLER

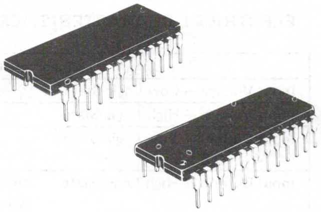
SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

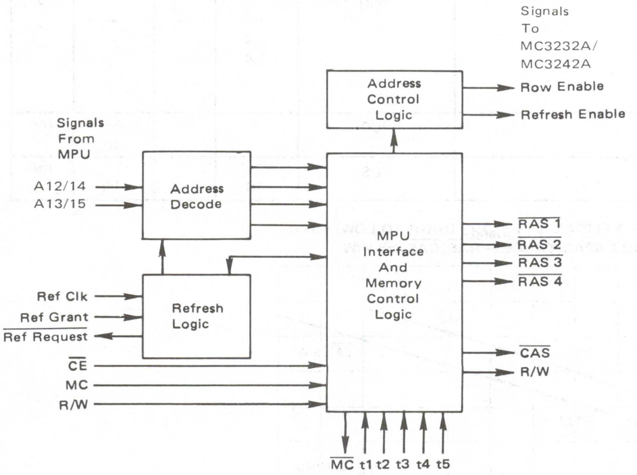
- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 $\overline{\text{RAS}}$ Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

L SUFFIX
CERAMIC PACKAGE
CASE 623-05



P SUFFIX
PLASTIC PACKAGE
CASE 649-03

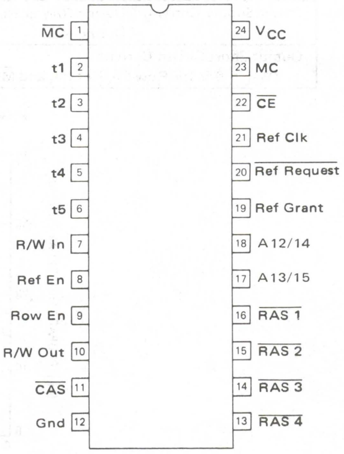
BLOCK DIAGRAM


Signals To MC3232A/ MC3242A
Address Control Logic
Row Enable
Refresh Enable
Signals From MPU
A12/14
A13/15
Address Decode
MPU Interface And Memory Control Logic
$\overline{\text{RAS 1}}$
$\overline{\text{RAS 2}}$
$\overline{\text{RAS 3}}$
$\overline{\text{RAS 4}}$
Ref Clk
Ref Grant
$\overline{\text{Ref Request}}$
Refresh Logic
$\overline{\text{CE}}$
MC
R/W
$\overline{\text{CAS}}$
R/W
$\overline{\text{MC}}$ t1 t2 t3 t4 t5

Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

PIN CONNECTIONS


$\overline{\text{MC}}$ 1
t1 2
t2 3
t3 4
t4 5
t5 6
R/W In 7
Ref En 8
Row En 9
R/W Out 10
$\overline{\text{CAS}}$ 11
Gnd 12
24 V_{CC}
23 MC
22 $\overline{\text{CE}}$
21 Ref Clk
20 $\overline{\text{Ref Request}}$
19 Ref Grant
18 A12/14
17 A13/15
16 $\overline{\text{RAS 1}}$
15 $\overline{\text{RAS 2}}$
14 $\overline{\text{RAS 3}}$
13 $\overline{\text{RAS 4}}$

See Pin Descriptions

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	−0.5 to +7.0	Vdc
Output Voltage	V_O	−0.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

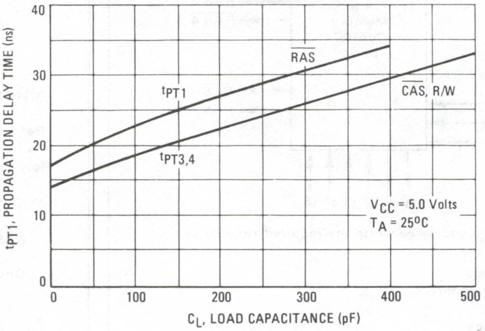
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.50 to +5.50	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-250	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	–	–	40 100	µA
Input Clamp Voltages (I_{IK} = 18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 24 mA for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and R/W) (I_{OL} = 8.0 mA for Row En, Ref En, $\overline{\text{MC}}$, $\overline{\text{Ref Req}}$)	V_{OL}	 – –	 – –	 0.5 0.5	V
Output Voltage – High Logic State (I_{OH} = -1.0 mA for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and R/W) (I_{OH} = -0.4 mA for Row En, Ref En, and $\overline{\text{MC}}$) I_{OH} = -0.2 mA for $\overline{\text{Ref Req}}$ (Note: $\overline{\text{Ref Req}}$ output has internal 5.0 k resistive pullup to V_{CC}.)	V_{OH}	 3.0 2.4 2.4	 – – –	 – – –	V
Power Supply Current – During R/W or Refresh – During Idle	I_{CC}	–	–	65 40	mA
Output Short-Circuit Current (V_{OL} = 0 V for Row En, Ref En, and $\overline{\text{MC}}$)	I_{OS}	-10	–	-55	mA

FIGURE 1 – TYPICAL $t_{PT1,3,\text{and}\,4}$ (HIGH TO LOW) versus LOAD CAPACITANCE – $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and R/W



SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times (Full AC Load – All Outputs)					ns
MC to $\overline{MC}$ – Low to High	$t_{PLH(\overline{MC})}$	–	7.0	14	
MC to $\overline{MC}$ – High to Low	$t_{PHL(\overline{MC})}$	–	9.0	17	
t1 to $\overline{RAS}$	t_{PT1}	18	26	40	
t2 to Row En	t_{PT2}	16	21	35	
t3 to $\overline{CAS}$	t_{PT3}	17	26	45	
t4 to R/$\overline{W}$	t_{PT4}	16	22	45	
t5 to $\overline{CAS}$	t_{PT5C}	22	30	42	
to $\overline{RAS}$	t_{PT5R}	19	26	40	
to R/$\overline{W}$	t_{PT5W}	30	42	58	
to Row En (Refresh)	t_{PT5ER}	30	50	65	
to Row En (R/$\overline{W}$)	t_{PT5E}	25	32	48	
to Refresh En	t_{PT5F}	22	46	55	
Ref Clk to $\overline{Ref\ Req}$	t_{PCQ}	10	17	27	
Ref Grant to Row En to Ref En	t_{PGS}	20	30	43	
t1 to $\overline{Ref\ Req}$ (Ref only) Note 2	t_{PTQ}	22	60	75	
Setup Times (Full AC Load – All Pins)					ns
Ref Clk before Ref Grant	$t_{su(RC)}$	35	–	–	
A12, A13 before t1	$t_{su(A)}$	10	–	–	
R/$\overline{W}$ Input before t4	$t_{su(R/\overline{W})}$	33	–	–	
$\overline{CE}$ before t1	$t_{su(\overline{CE})}$	20	–	–	
Ref Grant before t1	$t_{su(RG)}$	50	–	–	
Hold Times (Full AC Load – All Pins)					ns
A12, A13 after t5	$t_{h(A)}$	15	–	–	
$\overline{CE}$ after t1	$t_{h(\overline{CE})}$	0	–	–	
R/$\overline{W}$ after t4	$t_{h(R/\overline{W})}$	0	–	–	
MC Rising after t1 Rising	$t_{h(MC)}$	30	–	–	
Minimum Delay Times (Note 2 – Full AC Load – All Pins)					ns
t1 Low to High to t2 Low to High	$t_{d(1-2)}$	30	–	–	
t1 Low to High to t4 Low to High	$t_{d(1-4)}$	33	–	–	
t2 Low to High to t3 Low to High	$t_{d(2-3)}$	30	–	–	
t3 Low to High to t5 Low to High	$t_{d(3-5)}$	30	–	–	
Minimum Pulse Widths					ns
t1 through t5 Low	$t_{WL(t)}$	30	–	–	
High	$t_{WH(t)}$	30	–	–	
MC	$t_{W(MC)}$	30	–	–	
Ref Grant	$t_{W(RG)}$	25	–	–	

Note 2: $\overline{\text{Ref. Req.}}$ has an internal 5.0 kΩ pullup to V_{CC}. If faster propagation delay is required (t_{PTQ}), then an external registor can be added in parallel to the internal one to decrease the propagation delay. The value of resistance needed is a function of the capacitive loaded connection to $\overline{\text{Ref. Req.}}$ The minimum value of R that can be used is 5.0 V/8.0 mA = 625 Ω, assuming there are no other dc loads connected to that pin.

Note 3: If delays between t1–t5 are less than the minimum specified, the succeeding outputs may not switch.

AC LOADS (Note 4)

R/$\overline{W}$ and $\overline{CAS}$ Outputs	450 pF to Gnd*
$\overline{RAS}$ Outputs	150 pF to Gnd*
$\overline{MC}$, Row En, Ref En, and $\overline{Ref\ Req}$ Outputs	15 pF to Gnd*

*Includes probe and jig capacitance.

Note 4: All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.

PIN DESCRIPTION TABLE

Name	No.	Function
$\overline{\text{RAS1}}$ * $\overline{\text{RAS2}}$ $\overline{\text{RAS3}}$ $\overline{\text{RAS4}}$	16 15 14 13	Row Address Strobe pins which connect to each of the dynamic RAMs to latch in row address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle.
$\overline{\text{CAS}}$ *	11	Column Address Strobe pin which connects to each dynamic RAM to latch in column address.
R/W Out *	10	This pin signals the dynamic RAM whether the RAM is to be read from or written into.
Row En	9	Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses.
Ref En	8	Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done.
$\overline{\text{CE}}$	22	Chip Enable Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the $\overline{\text{MC}}$ output. $\overline{\text{CE}}$ must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of $\overline{\text{CE}}$.
R/W In	7	The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle.
A13 (A15) A12 (A14)	17 18	Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four $\overline{\text{RAS}}$ outputs. A14 and A15 apply to 16K RAMs.
MC	23	Memory Clock input from MC6875 clock or other signal source. The rising edge of MC must occur after the rising edge of t1 to avoid aborting the refresh cycle. When MC rises, it resets an internal flag that will terminate refresh at the end of the current cycle. Failure to reset the flag forces the 3480 to refresh every cycle thereafter. MC can be connected to t2 or t3 in noncritical applications.
$\overline{\text{MC}}$	1	The buffered complement output of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t1 through t5.
t1 t2 t3 t4 t5	2 3 4 5 6	These pins use external timing inputs to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four $\overline{\text{RAS}}$ outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the $\overline{\text{CAS}}$ output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of $\overline{\text{MC}}$, Ref En, and $\overline{\text{Ref Req}}$). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1.
Ref Clk	21	The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the $\overline{\text{Ref Req}}$ pin goes to a Logic 0.
$\overline{\text{Ref Req}}$	20	The Refresh Request output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 kΩ pullup resistor to the V_{CC} supply to allow wire-ORing if desired.
Ref Grant	19	Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the $\overline{\text{Ref Req}}$ pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes $\overline{\text{Ref Req}}$ to go high and all the $\overline{\text{RAS}}$ outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t3 and t4 go high because no $\overline{\text{CAS}}$ or R/W signal is needed during refresh. A positive edge on t5 resets the $\overline{\text{RAS}}$ and Row En to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle.
V_{CC}	24	+5.0 V supply. A 0.1 μF capacitor is recommended to bypass pin 24 to ground.
Gnd	12	System Ground.

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMs/(150 pF for $\overline{\text{RAS}}$ outputs, and 450 pF for $\overline{\text{CAS}}$ and R/W outputs). Consequently, these outputs have no short-circuit limit and must be handled accordingly. Good high capacitance load driving techniques usually include a 10 Ω or greater series damping resistor. It is highly recommended that this be done on $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and R/W outputs of the MC3480. The effect of these series damping resistors on rise and fall times must be included in timing considerations.

NOTE: All other outputs are LS/TTL totem-pole configuration unless otherwise noted.

TIME DELAY INFORMATION

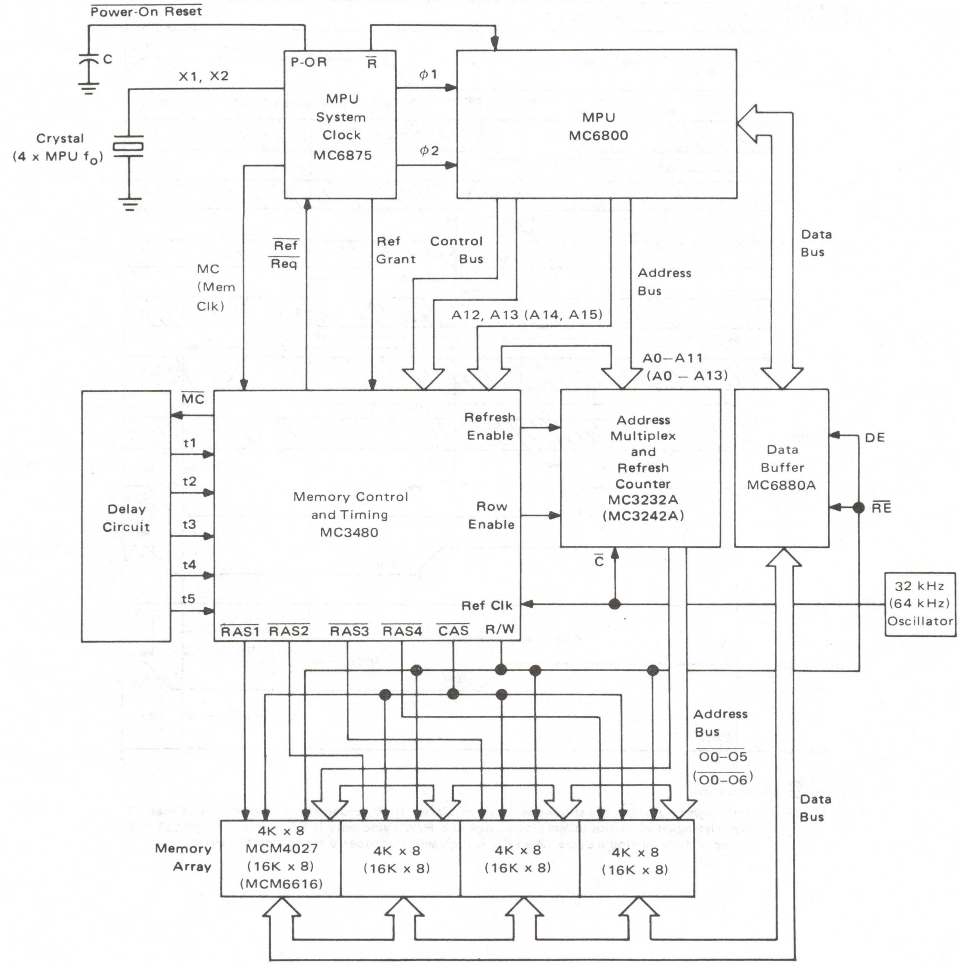
TIMING REQUIREMENT CONSTRAINTS

$\Delta t1$	Minimum is determined by MPU Address Delay (t_{AD}), plus RAM Row Address Set-Up Time (t_{ASR}), minus MC3480 Propagation Delay (t_{PT1}).
$\Delta t2 - \Delta t1$	Minimum is determined by RAM Row Address Hold Time (t_{RAH}) minus the minimum MC3232A/3242A Row Enable to Output Delay (t_{00MIN}).
$\Delta t3 - \Delta t2$	Minimum is determined by RAM Column Address Set-Up Time ($t_{ASC\ minimum}$) plus maximum MC3232A/3242A Row Enable to Output Delay (t_{001MAX}).
$\Delta t4 - \Delta t3$	No Minimum
$\Delta t5 - \Delta t3$	Minimum is determined by RAM minimum $\overline{CAS}$ Pulse Width (t_{CAS}) or Access Time from $\overline{CAS}$ (t_{CAC}) plus Data Set-Up Time of MPU (t_{DSR}).
$\Delta t5 - \Delta t4$	Minimum is determined by the RAM minimum Write Pulse Width (t_{WP}).

Note: Also required in computing time delays are the various delays incurred by the particular delay scheme used; i.e., delays between 4 x f_o, 2 x f_o, and f_o from the MC6875 which are used as inputs or the gate delays of the gates used in **Figures 5A through 5C.**

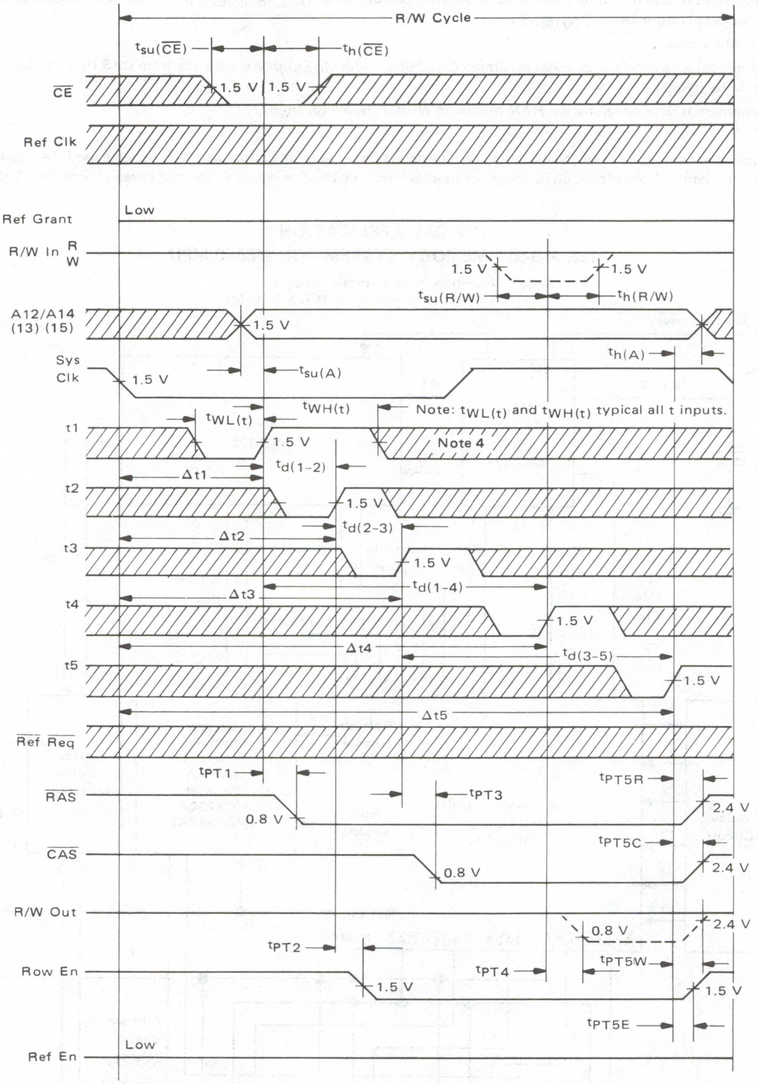
TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



$\overline{\text{Power-On Reset}}$
C
X1, X2
Crystal (4 x MPU f_o)
P-OR
$\overline{R}$
MPU System Clock MC6875
$\phi 1$
$\phi 2$
MPU MC6800
Data Bus
MC (Mem Clk)
$\overline{\text{Ref}}$ $\overline{\text{Req}}$
Ref Grant
Control Bus
Address Bus
A12, A13 (A14, A15)
A0—A11 (A0 — A13)
$\overline{MC}$
t1
t2
t3
t4
t5
Delay Circuit
Memory Control and Timing MC3480
Refresh Enable
Row Enable
Ref Clk
$\overline{RAS1}$ $\overline{RAS2}$ $\overline{RAS3}$ $\overline{RAS4}$ $\overline{CAS}$ R/W
Address Multiplex and Refresh Counter MC3232A (MC3242A)
$\overline{C}$
Data Buffer MC6880A
DE
$\overline{RE}$
32 kHz (64 kHz) Oscillator
Address Bus
$\overline{O0-O5}$
($\overline{O0-O6}$)
Data Bus
Memory Array
4K x 8 MCM4027 (16K x 8) (MCM6616)
4K x 8 (16K x 8)
4K x 8 (16K x 8)
4K x 8 (16K x 8)

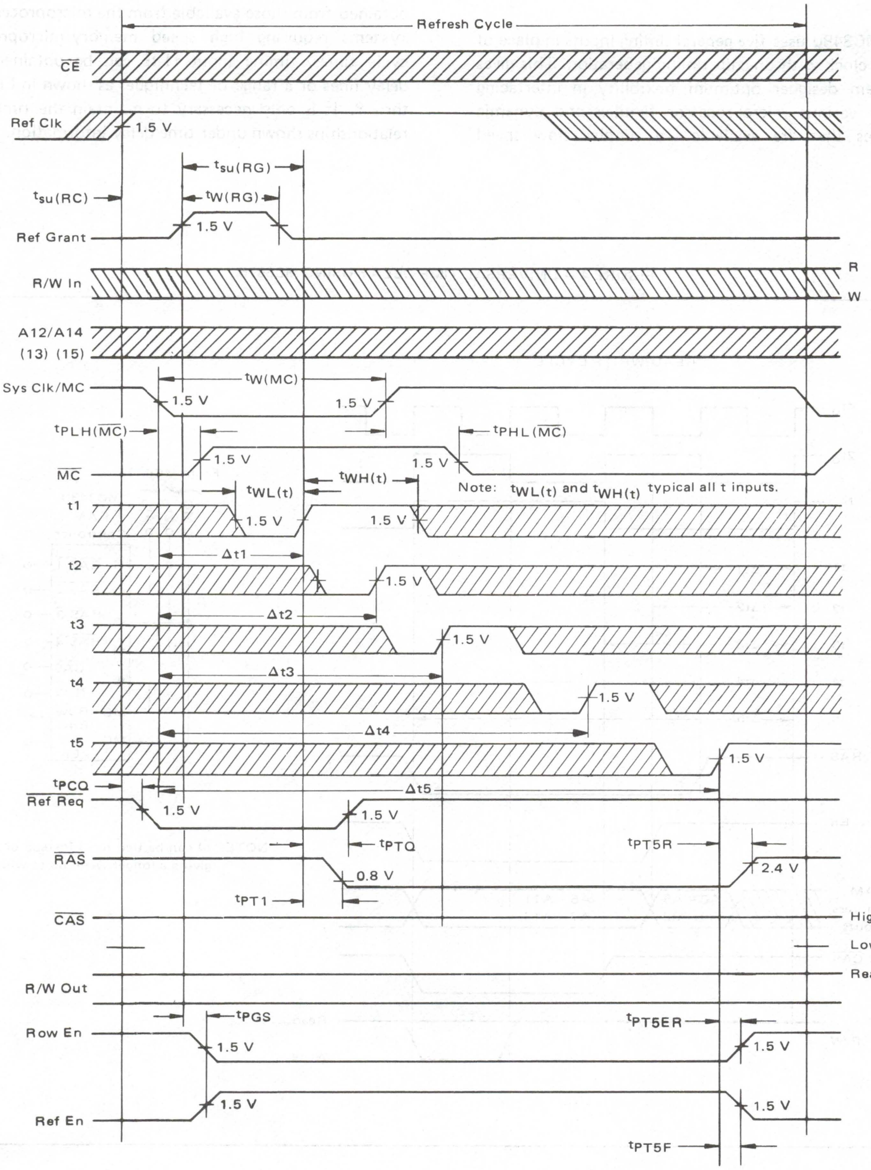
FIGURE 2 – READ/WRITE TIMING CYCLE


R/W Cycle
$t_{su(\overline{CE})}$
$t_{h(\overline{CE})}$
$\overline{CE}$
1.5 V
1.5 V
Ref Clk
Ref Grant
Low
R/W In R W
1.5 V
1.5 V
$t_{su(R/W)}$
$t_{h(R/W)}$
A12/A14 (13) (15)
1.5 V
$t_{h(A)}$
Sys Clk
1.5 V
$t_{su(A)}$
$t_{WH(t)}$
$t_{WL(t)}$
Note: $t_{WL(t)}$ and $t_{WH(t)}$ typical all t inputs.
t1
1.5 V
Note 4
$\Delta t1$
$t_{d(1-2)}$
t2
1.5 V
$t_{d(2-3)}$
$\Delta t2$
t3
1.5 V
$t_{d(1-4)}$
$\Delta t3$
t4
1.5 V
$\Delta t4$
$t_{d(3-5)}$
t5
1.5 V
$\Delta t5$
$\overline{Ref}$ $\overline{Req}$
t_{PT1}
t_{PT3}
t_{PT5R}
$\overline{RAS}$
0.8 V
2.4 V
t_{PT5C}
$\overline{CAS}$
0.8 V
2.4 V
R/W Out
0.8 V
2.4 V
t_{PT2}
t_{PT5W}
Row En
t_{PT4}
1.5 V
1.5 V
t_{PT5E}
Ref En
Low

▨ = Don't care.

NOTE 4: Although t1 and $\overline{CE}$ are shown as don't care after their respective minimum hold times, t1 may rise again after the initial rising edge in a R/W cycle only if $\overline{CE}$ is low. Bringing t1 high a second time during a cycle when $\overline{CE}$ is high will improperly terminate the cycle.

FIGURE 3 – REFRESH TIMING CYCLE

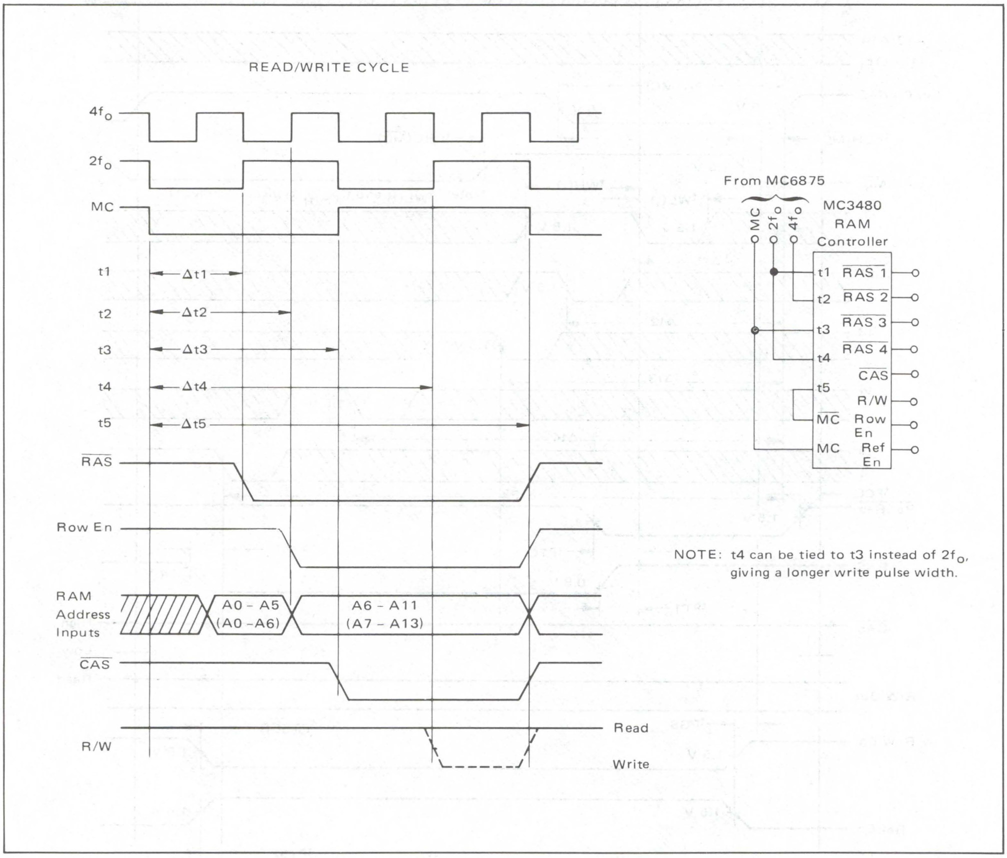

Refresh Cycle
CE
Ref Clk
1.5 V
$t_{su(RG)}$
$t_{su(RC)}$
$t_{W(RG)}$
1.5 V
Ref Grant
R/W In
R
W
A12/A14
(13) (15)
Sys Clk/MC
$t_{W(MC)}$
1.5 V
1.5 V
$t_{PLH(\overline{MC})}$
$t_{PHL(\overline{MC})}$
1.5 V
1.5 V
$\overline{MC}$
$t_{WH(t)}$
$t_{WL(t)}$
Note: $t_{WL(t)}$ and $t_{WH(t)}$ typical all t inputs.
t1
1.5 V
1.5 V
Δt1
t2
1.5 V
Δt2
t3
1.5 V
Δt3
t4
1.5 V
Δt4
t5
1.5 V
t_{PCQ}
Δt5
$\overline{\text{Ref Req}}$
1.5 V
1.5 V
t_{PTQ}
t_{PT5R}
$\overline{RAS}$
2.4 V
0.8 V
t_{PT1}
$\overline{CAS}$
High
Low
Read
R/W Out
t_{PGS}
t_{PT5ER}
Row En
1.5 V
1.5 V
1.5 V
1.5 V
Ref En
t_{PT5F}

APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The MC3480 uses five general timing inputs in place of a master clock with on-chip timing generation. This gives the system designer optimum flexibility in interfacing with the various microprocessor families and dynamic memories that are available. In simpler slow speed systems, the timing signals required can be directly obtained from those available from the microprocessor. In systems requiring high speed memory/microprocessor cycle times, timing input t1-t5 can be obtained using delay lines or a range of techniques as shown in Figures 4 thru 8. It is only necessary to maintain the time delay relationships shown under time delay information.

FIGURE 4 – UNIVERSAL TIME DELAY USING MC6875


READ/WRITE CYCLE
4fo
2fo
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0 – A5 (A0 – A6)
A6 – A11 (A7 – A13)
CAS
R/W
Read
Write
From MC6875
MC
2fo
4fo
MC3480 RAM Controller
t1
t2
t3
t4
t5
MC
MC
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W
Row En
Ref En

NOTE: t4 can be tied to t3 instead of 2fo, giving a longer write pulse width.

FIGURE 5 – ALTERNATE TIME DELAYS USING MC6875
(Read/Write Cycle Shown)

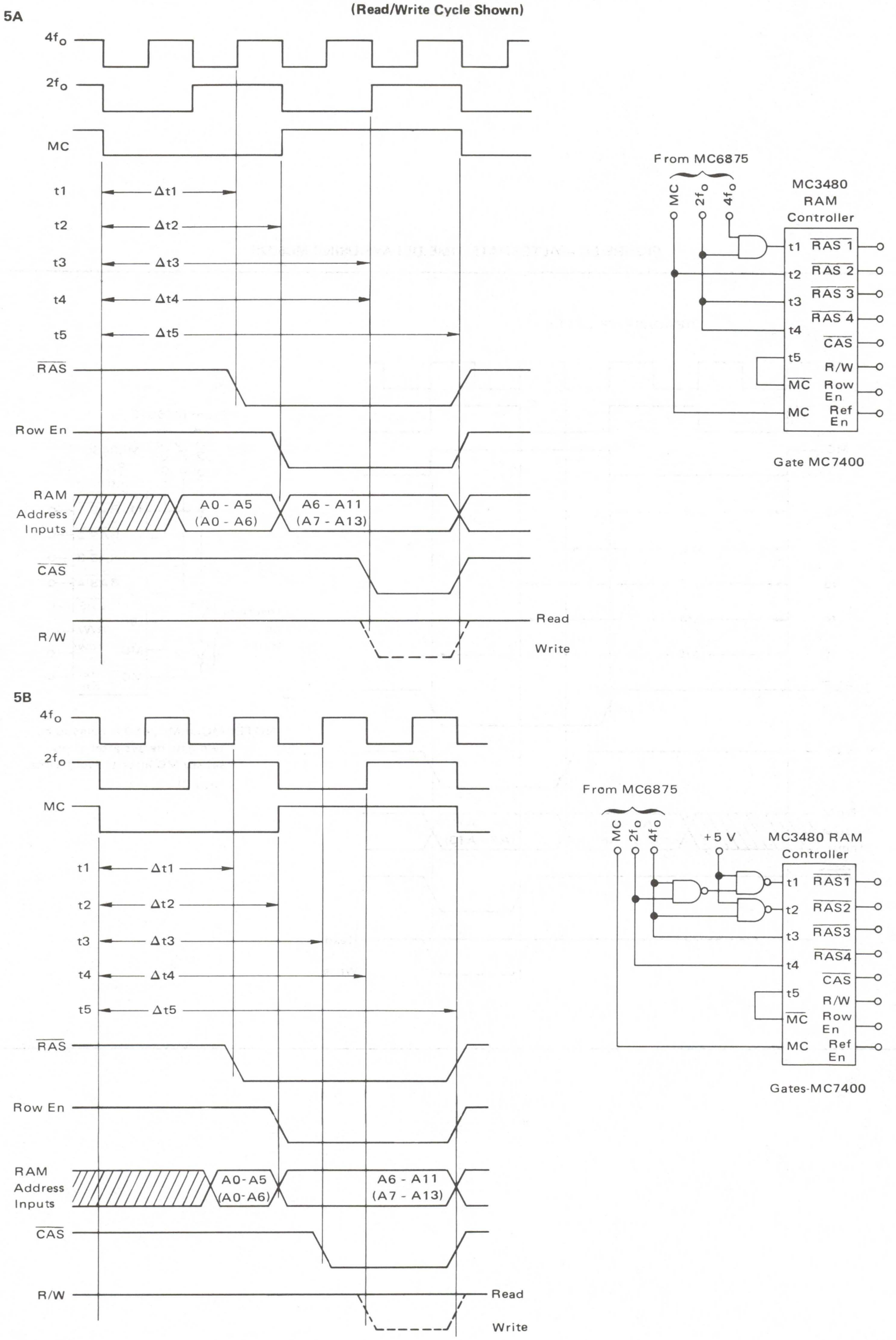
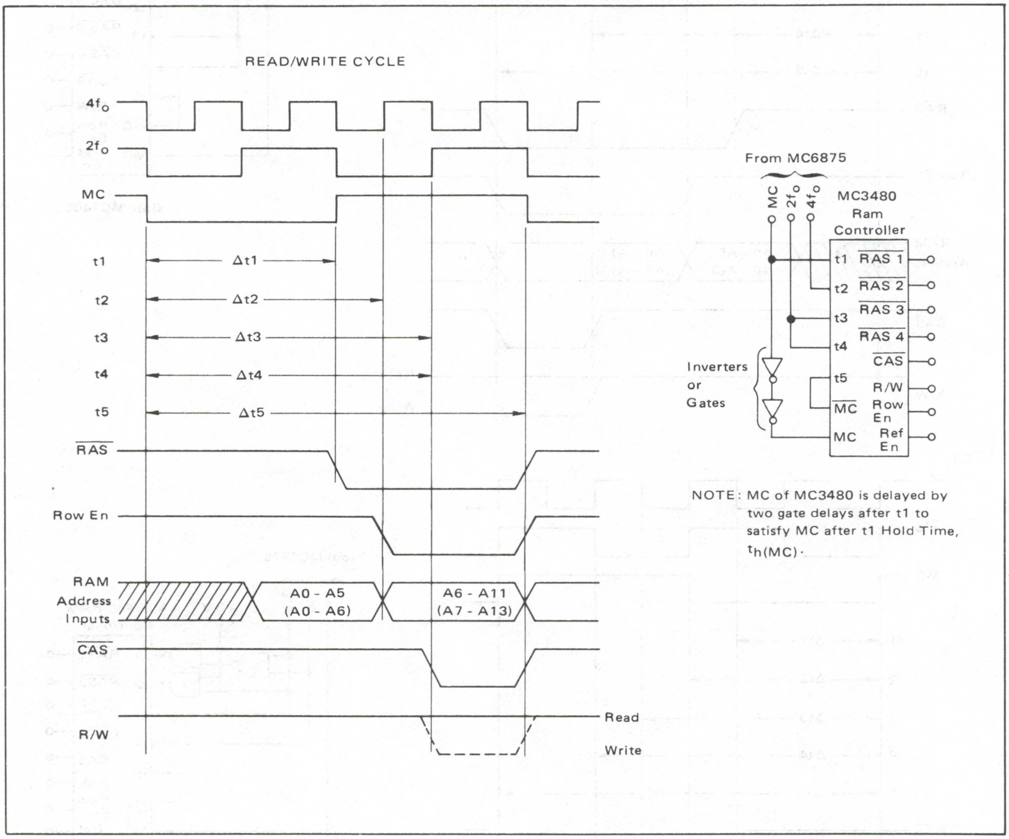
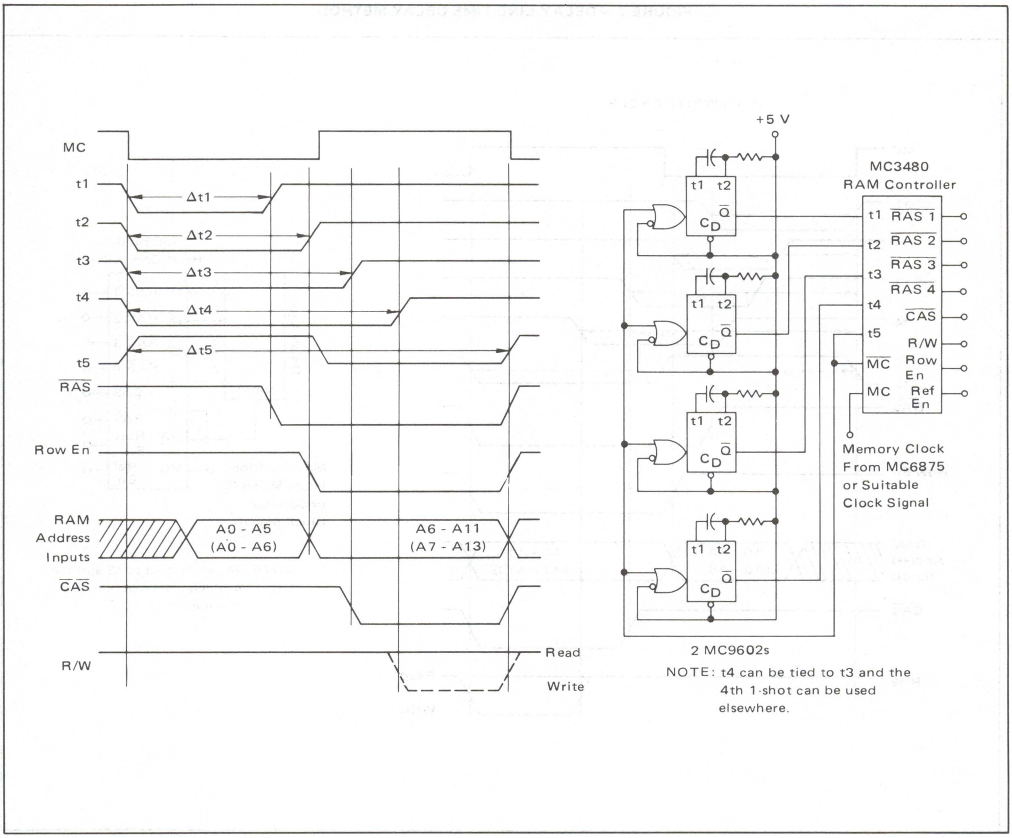

5A
4fo
2fo
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0 - A5 (A0 - A6)
A6 - A11 (A7 - A13)
CAS
R/W
Read
Write
From MC6875
MC
2fo
4fo
MC3480 RAM Controller
t1
t2
t3
t4
t5
MC
MC
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W
Row En
Ref En
Gate MC7400
5B
4fo
2fo
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0-A5 (A0-A6)
A6 - A11 (A7 - A13)
CAS
R/W
Read
Write
From MC6875
MC
2fo
4fo
+5 V
MC3480 RAM Controller
t1
t2
t3
t4
t5
MC
MC
RAS1
RAS2
RAS3
RAS4
CAS
R/W
Row En
Ref En
Gates-MC7400

FIGURE 5C – ALTERNATE TIME DELAYS USING MC6875


READ/WRITE CYCLE
$4f_o$
$2f_o$
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0 - A5 (A0 - A6)
A6 - A11 (A7 - A13)
CAS
R/W
Read
Write
From MC6875
MC
$2f_o$
$4f_o$
MC3480 Ram Controller
t1
RAS 1
t2
RAS 2
t3
RAS 3
t4
RAS 4
CAS
t5
R/W
MC
Row En
MC
Ref En
Inverters or Gates

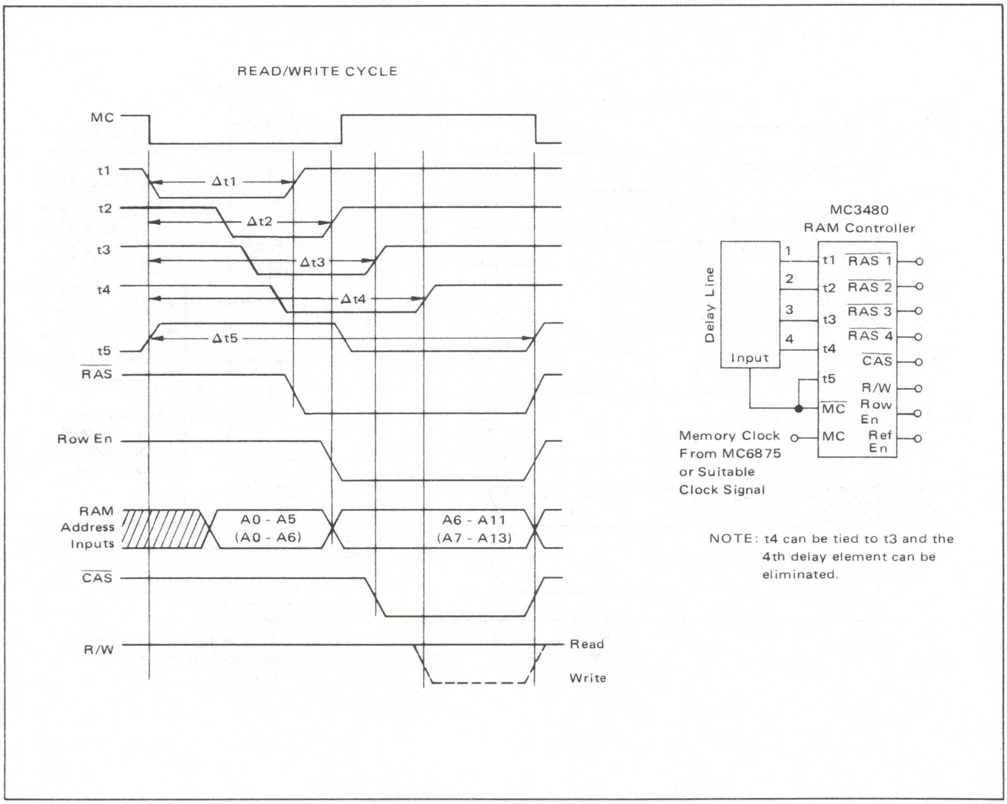
NOTE: MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

FIGURE 6 — ONE SHOT TIME DELAY METHOD


MC
t1
t2
t3
t4
t5
$\overline{RAS}$
Row En
RAM Address Inputs
$\overline{CAS}$
R/W
Δt1
Δt2
Δt3
Δt4
Δt5
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
Read
Write
+5 V
t1 t2
C_D
$\overline{Q}$
MC3480
RAM Controller
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS\ 1}$
$\overline{RAS\ 2}$
$\overline{RAS\ 3}$
$\overline{RAS\ 4}$
$\overline{CAS}$
R/W
Row En
Ref En
Memory Clock From MC6875 or Suitable Clock Signal
2 MC9602s

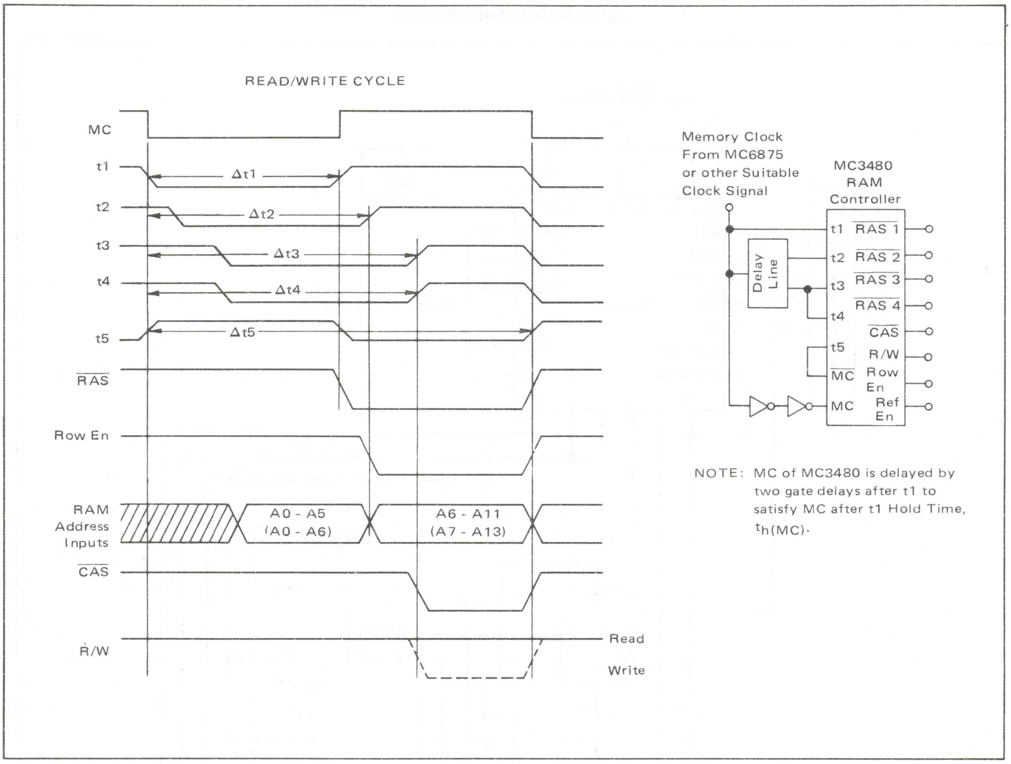
NOTE: t4 can be tied to t3 and the 4th 1-shot can be used elsewhere.

FIGURE 7 — DELAY LINE TIME DELAY METHOD


READ/WRITE CYCLE
MC
t1
Δt1
t2
Δt2
t3
Δt3
t4
Δt4
t5
Δt5
$\overline{\text{RAS}}$
Row En
RAM Address Inputs
A0 - A5 (A0 - A6)
A6 - A11 (A7 - A13)
$\overline{\text{CAS}}$
R/W
Read
Write
MC3480 RAM Controller
Delay Line
Input
1
2
3
4
t1
t2
t3
t4
t5
$\overline{\text{MC}}$
MC
$\overline{\text{RAS 1}}$
$\overline{\text{RAS 2}}$
$\overline{\text{RAS 3}}$
$\overline{\text{RAS 4}}$
$\overline{\text{CAS}}$
R/W
Row En
Ref En
Memory Clock From MC6875 or Suitable Clock Signal

NOTE: t4 can be tied to t3 and the 4th delay element can be eliminated.

FIGURE 8 – DELAY LINE TIME DELAY (ALTERNATE METHOD)


READ/WRITE CYCLE
MC
t1
t2
t3
t4
t5
$\overline{RAS}$
Row En
RAM Address Inputs
$\overline{CAS}$
R/W
Δt1
Δt2
Δt3
Δt4
Δt5
A0 - A5 (A0 - A6)
A6 - A11 (A7 - A13)
Read
Write
Memory Clock From MC6875 or other Suitable Clock Signal
MC3480 RAM Controller
Delay Line
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS\ 1}$
$\overline{RAS\ 2}$
$\overline{RAS\ 3}$
$\overline{RAS\ 4}$
$\overline{CAS}$
R/W
Row En
Ref En

NOTE: MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

REFRESH CONSIDERATIONS

The MC3480/MC3232A (MC3242A) memory control system can be used with either cycle steal or transparent refresh methods. Figure 9 shows one transparent technique employing refresh during $\phi 2$ low in an M6800 microprocessor-based system. Using this technique requires that the memory be capable of completing a Read/Write Cycle and a Refresh Cycle sequentially during the M6800 cycle. The minimum cycle time at the time of printing for dynamic multiplexed RAMs is 320 ns, therefore limiting the microprocessor to 1.56 MHz operation. The D flip-flops of Figure 9 produce a trigger at the beginning of both $\phi 1$ and $\phi 2$. For a 1.0 MHz system, the t1–t5 inputs should be adjusted for the following delays:

$\overline{RAS}$ falls at 150 ns (triggered by t1)
Row En falls at 250 ns (triggered by t2)
$\overline{CAS}$, R/W falls at 300 ns (triggered by t3)
t5 rises at 500 ns.

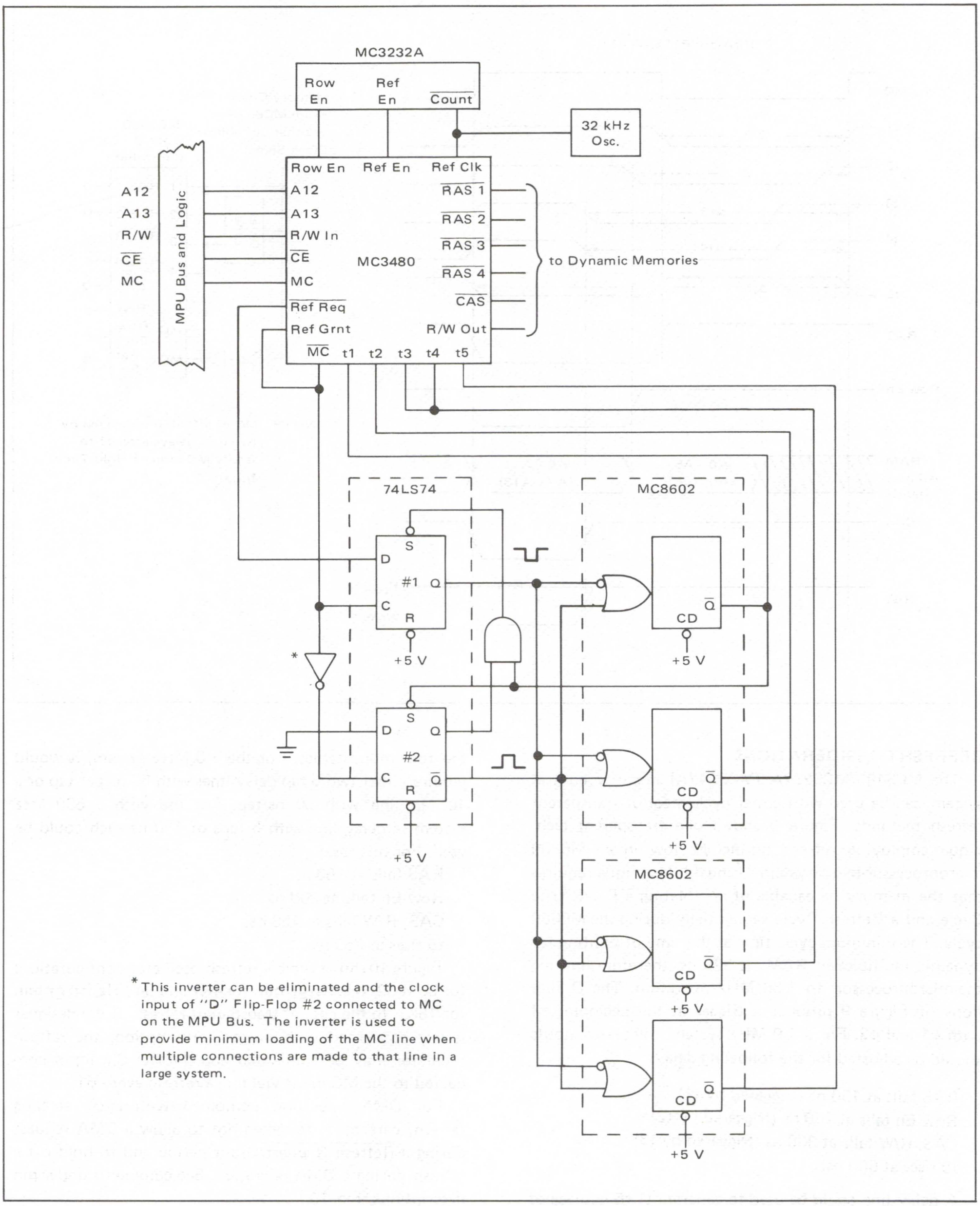
A delay line could be used to generate t1-t5 in place of the four monostables. For the 1.0 MHz system, it would require either two 5 tap delay lines with 50 ns per tap or a 10 tap line with 50 ns/tap. For use with a 600 kHz system, a delay line with 5 taps of 150 ns each could be used. For this case:

$\overline{RAS}$ falls at 150 ns
Row En falls at 300 ns
$\overline{CAS}$, R/W falls at 450 ns
t5 rises at 750 ns

Figure 10 shows typical refresh oscillator configurations for both 32 kHz (f_{REF} min for 4K) and 64 kHz (f_{REF}min for 16K). In the case of transparent refresh, if the designer is not concerned with power consumption, the refresh oscillator may be eliminated and the Ref Clk input connected to the MC input yielding a refresh every $\phi 1$.

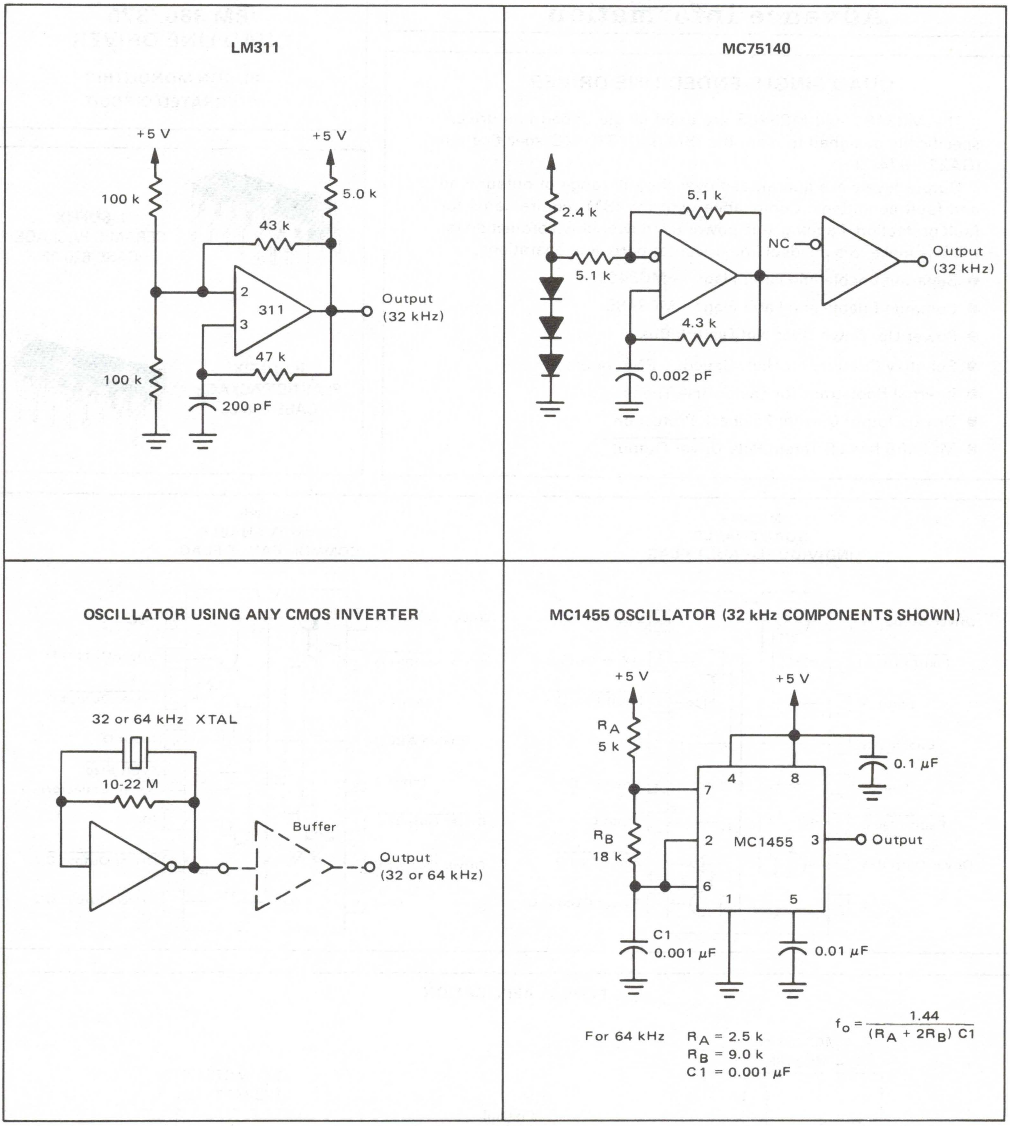
For DMA operation combined with cycle stealing refresh, care must be taken not to allow a DMA request during a $\overline{\text{Refresh Request}}$/Grant period and to hold off a refresh during a DMA operation. See comments under pin descriptions, Pin 19.

FIGURE 9 – EXAMPLE OF $\phi 2$ LOW METHOD OF HIDDEN REFRESH USING MC3480 AND 4K RAMS


MC3232A
Row En
Ref En
$\overline{\text{Count}}$
32 kHz Osc.
MPU Bus and Logic
A12
A13
R/W
$\overline{\text{CE}}$
MC
Row En
Ref En
Ref Clk
A12
A13
R/W In
$\overline{\text{CE}}$
MC
MC3480
$\overline{\text{Ref Req}}$
Ref Grnt
$\overline{\text{MC}}$
t1
t2
t3
t4
t5
$\overline{\text{RAS 1}}$
$\overline{\text{RAS 2}}$
$\overline{\text{RAS 3}}$
$\overline{\text{RAS 4}}$
$\overline{\text{CAS}}$
R/W Out
to Dynamic Memories
74LS74
S
D
#1
Q
C
R
+5 V
*
S
D
Q
#2
C
$\overline{\text{Q}}$
R
+5 V
MC8602
$\overline{\text{Q}}$
CD
+5 V
$\overline{\text{Q}}$
CD
+5 V
MC8602
$\overline{\text{Q}}$
CD
+5 V
$\overline{\text{Q}}$
CD
+5 V

*This inverter can be eliminated and the clock input of "D" Flip-Flop #2 connected to MC on the MPU Bus. The inverter is used to provide minimum loading of the MC line when multiple connections are made to that line in a large system.

FIGURE 10 — SUGGESTED 32 kHz OSCILLATORS


LM311

MC75140

OSCILLATOR USING ANY CMOS INVERTER

MC1455 OSCILLATOR (32 kHz COMPONENTS SHOWN)

+5 V
+5 V
100 k
5.0 k
43 k
2
311
3
Output
(32 kHz)
47 k
100 k
200 pF
2.4 k
5.1 k
5.1 k
NC
Output
(32 kHz)
4.3 k
0.002 pF
32 or 64 kHz XTAL
10-22 M
Buffer
Output
(32 or 64 kHz)
+5 V
+5 V
RA
5 k
4
8
0.1 μF
7
RB
18 k
2
MC1455
3
Output
6
1
5
C1
0.001 μF
0.01 μF
For 64 kHz RA = 2.5 k
RB = 9.0 k
C1 = 0.001 μF
fo = 1.44 / (RA + 2RB) C1

MC3481
MC3485

MOTOROLA

Advance Information

QUAD SINGLE-ENDED LINE DRIVER

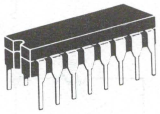
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole $\overline{\text{Driver Output}}$

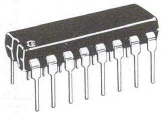
IBM 360/370 QUAD LINE DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

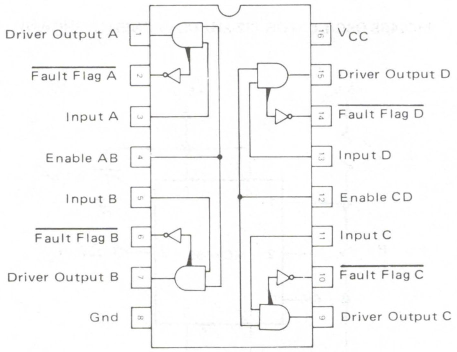


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

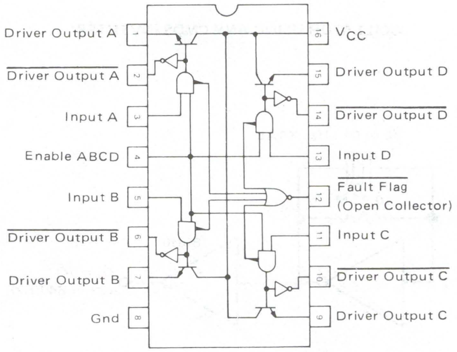
P SUFFIX
PLASTIC PACKAGE
CASE 648-05



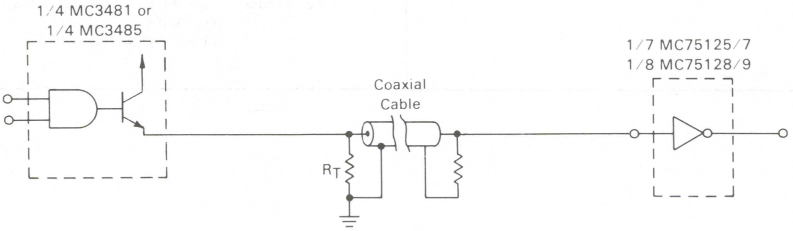
MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG


Driver Output A
1
$\overline{\text{Fault Flag A}}$
2
Input A
3
Enable AB
4
Input B
5
$\overline{\text{Fault Flag B}}$
6
Driver Output B
7
Gnd
8
16
V_{CC}
15
Driver Output D
14
$\overline{\text{Fault Flag D}}$
13
Input D
12
Enable CD
11
Input C
10
$\overline{\text{Fault Flag C}}$
9
Driver Output C

MC3485
COMMON ENABLE
COMMON FAULT FLAG


Driver Output A
1
$\overline{\text{Driver Output A}}$
2
Input A
3
Enable ABCD
4
Input B
5
$\overline{\text{Driver Output B}}$
6
Driver Output B
7
Gnd
8
16
V_{CC}
15
Driver Output D
14
$\overline{\text{Driver Output D}}$
13
Input D
12
$\overline{\text{Fault Flag}}$
(Open Collector)
11
Input C
10
$\overline{\text{Driver Output C}}$
9
Driver Output C

TYPICAL APPLICATION


1/4 MC3481 or
1/4 MC3485
Coaxial
Cable
R_T
1/7 MC75125/7
1/8 MC75128/9

This document contains information on a new product. Specifications and information herein are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.95	Vdc
High Level Output Current	I_{OH}	—	—	-59.3	mA
Operating Ambient Temperature Range	T_A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at $T_A = 25°C$ and $V_{CC} = +5.0$ V)

Characteristic	Symbol	MC3481			MC3485			Unit
		Min	Typ	Max	Min	Typ	Max	
High-Level Input Voltage Note 2	V_{IH}	2.0	—	—	2.0	—	—	V
Low-Level Input Voltage Note 2	V_{IL}	—	—	0.8	—	—	0.8	V
High-Level Input Current	I_{IH}							µA
($V_{CC} = 4.5$ V, $V_{IH} = 2.7$ V) - Input		—	—	20	—	—	20	
Enable		—	—	40	—	—	80	
($V_{CC} = 4.5$ V, $V_{IH} = 5.5$ V) - Input		—	—	100	—	—	100	
Enable		—	—	200	—	—	400	
Low-Level Input Current	I_{IL}							µA
($V_{CC} = 5.95$ V, $V_{IL} = 0.4$ V) - Input		—	—	-250	—	—	-250	
Enable		—	—	-500	—	—	-1000	
Input Clamp Voltage ($I_{IC} = -18$ mA)	V_{IC}	—	—	-1.5	—	—	-1.5	V
High-Level Driver Output Voltage								V
($V_{CC} = 4.5$ V, $V_{IH} = 2.0$ V, $I_{OH} = -59.3$ mA)	$V_{OH(D)}$	3.11	3.6	—	3.11	3.6	—	
($V_{CC} = 5.25$ V, $V_{IH} = 2.0$ V, $I_{OH} = -41$ mA)	$V_{OH(DS)}$	3.9	—	—	3.9	—	—	
Low-Level Driver Output Voltage								V
($V_{CC} = 5.5$ V, $V_{IL} = 0.8$ V, $I_{OL} = -240$ µA)	$V_{OL(D)}$	—	—	+0.15	—	—	+0.15	
($V_{CC} = 5.95$ V, $V_{IL} = 0.8$ V, $I_{OL} = -1.0$ mA)	$V_{OL(DS)}$	—	—	+0.15	—	—	+0.15	
Driver Output Short Circuit Current								mA
($V_{CC} = 5.5$ V, $V_{IH} = 2.0$ V, $V_{OS} = 0$ V)	$I_{OS(D)}$	—	—	-5.0	—	—	-5.0	
($V_{CC} = 5.95$ V, $V_{IH} = 2.0$ V, $V_{OS} = 0$ V)	$I_{OS(DS)}$	—	—	-5.0	—	—	-5.0	
Driver Output Reverse Leakage Current								µA
($V_{CC} = 4.5$ V, $V_{IL} = 0$ V, $V_O = 3.11$ V)	I_{OR1}	—	—	+100	—	—	+100	
($V_{CC} = 0$ V, $V_{IL} = 0$ V, $V_O = 3.11$ V)	I_{OR2}	—	—	+200	—	—	+200	
High-Level $\overline{\text{Driver Output}}$ Voltage ($V_{CC} = 4.5$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ µA)	$V_{OH(\overline{D})}$	—	—	—	2.5	3.0	—	V
Low-Level $\overline{\text{Driver Output}}$ Voltage ($V_{CC} = 4.5$ V, $V_{IH} = 2.0$ V, $I_{OL} = +8.0$ mA)	$V_{OL(\overline{D})}$	—	—	—	—	—	0.5	V
$\overline{\text{Driver Output}}$ Short Circuit Current								mA
($V_{CC} = 5.5$ V, $V_{OS} = 0$ V, only one output shorted at a time)	$I_{OS(\overline{D})}$	—	—	—	-15	-60	-100	
($V_{CC} = 5.95$ V, $V_{OS} = 0$ V, only one output shorted at a time)	$I_{OS(\overline{DS})}$	—	—	—	-15	—	-110	
High-Level $\overline{\text{Fault Flag}}$ Output Voltage ($V_{CC} = 4.5$ V, $I_{OH} = -400$ µA)	$V_{OH(\overline{F})}$	2.5	3.0	—	—	—	—	V
Low-Level $\overline{\text{Fault Flag}}$ Output Voltage ($V_{CC} = 4.5$ V, $V_{IH} = 2.0$ V, $I_{OL} = +8.0$ mA, Driver Output shorted to Ground	$V_{OL(\overline{F})}$	—	—	0.5	—	—	0.5	V
$\overline{\text{Fault Flag}}$ Output Short Circuit Current								mA
($V_{CC} = 5.5$ V, $V_{OS} = 0$ V, only one output shorted at a time)	$I_{OS(\overline{F})}$	-15	—	-100	—	—	—	
($V_{CC} = 5.95$ V, $V_{OS} = 0$ V, only one output shorted at a time)	$I_{OS(\overline{FS})}$	-15	—	-110	—	—	—	
High-Level $\overline{\text{Fault Flag}}$ Output Current ($V_{CC} = 5.95$ V, $V_{OH} = 5.95$ V)	$I_{OH(\overline{F})}$	—	—	—	—	—	+100	µA
High-Level Power Supply Current								mA
($V_{CC} = 5.5$ V, $V_{IH} = 2.0$ V, no output loading)	I_{CCH}	—	50	70	—	55	75	
($V_{CC} = 5.95$ V, $V_{IH} = 2.0$ V, no output loading)	I_{CCHS}	—	—	80	—	—	85	
Low-Level Power Supply Current								mA
($V_{CC} = 5.5$ V, $V_{IL} = 0.8$ V, no output loading)	I_{CCL}	—	35	55	—	35	55	
($V_{CC} = 5.95$ V, $V_{IL} = 0.8$ V, no output loading)	I_{CCLS}	—	—	70	—	—	70	

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+7.0	V
Input Voltage		V_I	10	V
Driver Output Voltage		V_O	5.5	V
Power Dissipation (Package Limitation)	Ceramic Package Plastic Package	P_D	1150 962	mW
Derate Above T_A = 25°C		$1/R_{\theta JA}$	7.7	mW/°C
Operating Ambient Temperature Range		T_A	0 to +70	°C
Junction Temperature	Ceramic Package Plastic Package	T_J	+175 +150	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

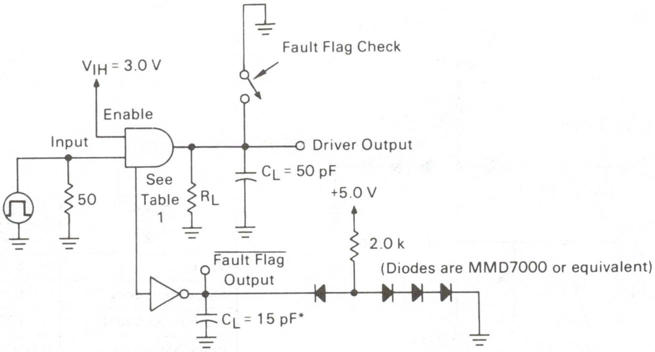
SWITCHING CHARACTERISTICS (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for V_{CC} = 5.0 V ±10% and Select-Out Driver characteristics are guaranteed for V_{CC} = 5.25 to 5.95 V. Typical values measured at T_A = 25°C and V_{CC} = 5.0 V. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
High-to-Low-Level, Driver Output					
As I/O Driver	$t_{PHL(D)}$	—	18	—	
As Select-Out Driver	$t_{PHL(DS)}$	—	19	—	
Low-to-High-Level, Driver Output					
As I/O Driver	$t_{PLH(D)}$	—	20	—	
As Select-Out Driver	$t_{PLH(DS)}$	—	21	—	
High-to-Low-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PHL(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PHL(\overline{DS})}$	—	26	—	
Low-to-High-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PLH(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PLH(\overline{DS})}$	—	26	—	
High-to-Low-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PHL(\overline{F})}$	—	45	—	
As Select-Out Driver	$t_{PHL(\overline{FS})}$	—	47	—	
Low-to-High-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PLH(\overline{F})}$	—	40	—	
As Select-Out Driver	$t_{PLH(\overline{FS})}$	—	42	—	
Ratio of Propagation Delay Times As I/O Driver	$\frac{t_{PLH(D)}}{t_{PHL(D)}}$	—	1.0	—	

Note 1. Reference IBM specification GA22-6974-3 for test terminology.

2. The fault protection circuitry of the MC3481/85 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

FIGURE 1 — MC3481 AC TEST CIRCUIT AND WAVEFORMS


Fault Flag Check
V_{IH} = 3.0 V
Enable
Input
Driver Output
C_L = 50 pF
See Table 1
R_L
50
+5.0 V
2.0 k
(Diodes are MMD7000 or equivalent)
Fault Flag Output
C_L = 15 pF*

* Load Capacitance shown includes Fixture and Probe Capacitance

Table 1	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90

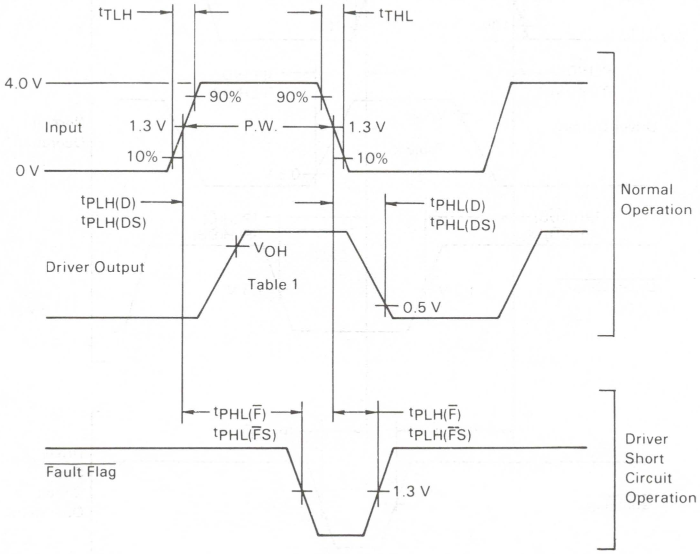
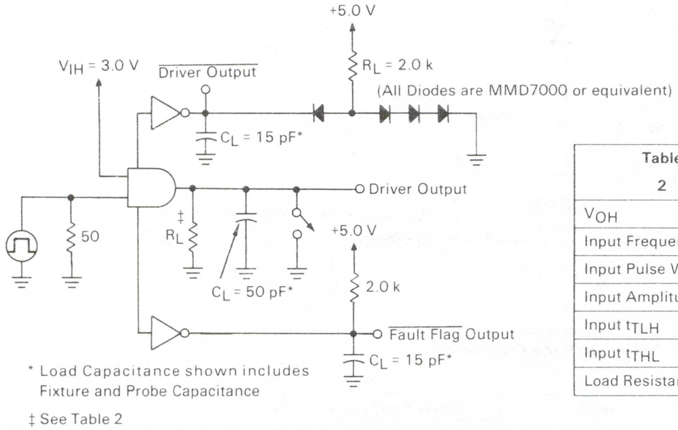

t_{TLH}
t_{THL}
4.0 V
90%
90%
Input
1.3 V
P.W.
1.3 V
10%
10%
0 V
$t_{PLH(D)}$
$t_{PLH(DS)}$
$t_{PHL(D)}$
$t_{PHL(DS)}$
V_{OH}
Driver Output
Table 1
0.5 V
Normal Operation
$t_{PHL(\overline{F})}$
$t_{PHL(\overline{FS})}$
$t_{PLH(\overline{F})}$
$t_{PLH(\overline{FS})}$
$\overline{\text{Fault Flag}}$
1.3 V
Driver Short Circuit Operation

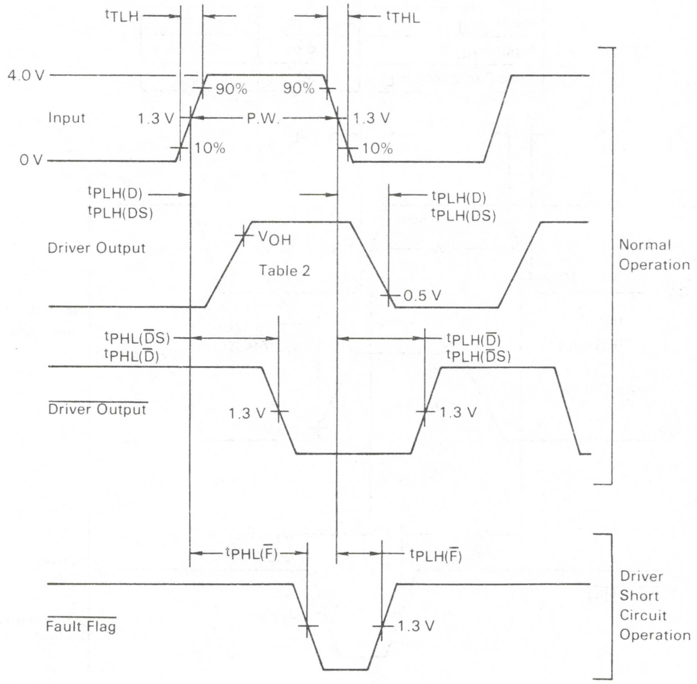
FIGURE 2 — MC3485 AC TEST CIRCUIT AND WAVEFORMS


+5.0 V
R_L = 2.0 k
(All Diodes are MMD7000 or equivalent)
V_{IH} = 3.0 V
Driver Output
C_L = 15 pF*
Driver Output
50
‡
R_L
+5.0 V
2.0 k
C_L = 50 pF*
Fault Flag Output
C_L = 15 pF*

* Load Capacitance shown includes Fixture and Probe Capacitance

‡ See Table 2

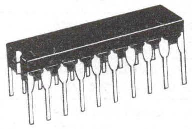
Table 2	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90


t_{TLH}
t_{THL}
4.0 V
90%
90%
Input
1.3 V
P.W.
1.3 V
10%
10%
0 V
$t_{PLH(D)}$
$t_{PLH(DS)}$
$t_{PLH(D)}$
$t_{PLH(DS)}$
Driver Output
V_{OH}
Table 2
0.5 V
Normal Operation
$t_{PHL(\overline{DS})}$
$t_{PHL(\overline{D})}$
$t_{PLH(\overline{D})}$
$t_{PLH(\overline{DS})}$
Driver Output
1.3 V
1.3 V
$t_{PHL(\overline{F})}$
$t_{PLH(\overline{F})}$
Fault Flag
1.3 V
Driver Short Circuit Operation

MC3482A/MC6882A
MC3482B/MC6882B

OCTAL THREE-STATE BUFFER/LATCH

SILICON MONOLITHIC INTEGRATED CIRCUITS



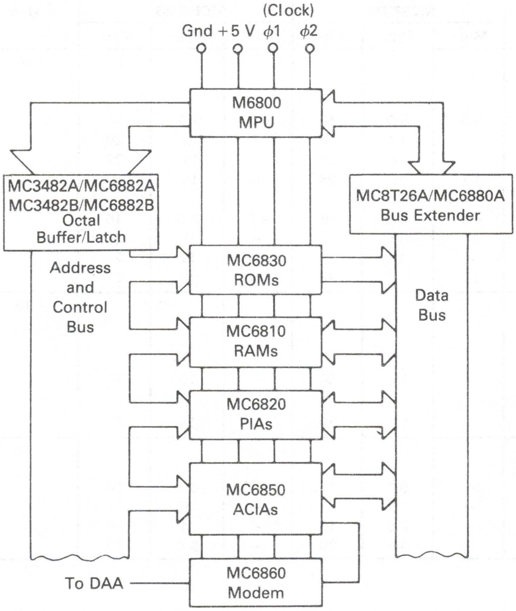
L SUFFIX
CASE 732-03

OCTAL THREE-STATE BUFFER/LATCH

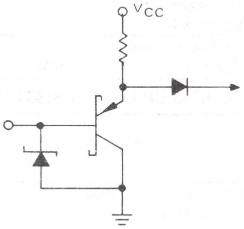
This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

- Inverting and Non-Inverting Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All Inputs Have Hysteresis to Improve Noise Rejection
- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

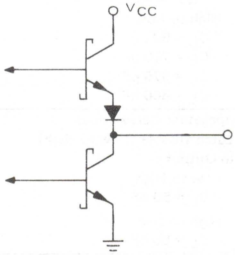
MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
Gnd +5 V ϕ1 ϕ2
M6800 MPU
MC3482A/MC6882A MC3482B/MC6882B Octal Buffer/Latch
MC8T26A/MC6880A Bus Extender
Address and Control Bus
Data Bus
MC6830 ROMs
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 Modem
To DAA

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C.)

Device	Alternate	Package
MC3482AL	MC6882AL	Ceramic DIP
MC3482BL	MC6882BL	Ceramic DIP

MAXIMUM RATINGS ($T_A = 25^oC$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC
Operating Junction Temperature	T_J		^oC
Ceramic Package		175	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^oC \leqslant T_A \leqslant 75^oC$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State ($V_{CC} = 4.75$ V, $T_A = 25^oC$)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State ($V_{CC} = 4.75$ V, $T_A = 25^oC$)	V_{IL}	—	—	0.8	V
Input Current — High Logic State ($V_{CC} = 5.25$ V, $V_{IH} = 2.4$ V)	I_{IH}	—	—	40	µA
Input Current — Low Logic State ($V_{CC} = 5.25$ V, $V_{IL} = 0.5$ V, $V_{IL(\overline{OE})} = 0.5$ V)	I_{IL}	—	—	−250	µA
Output Voltage — High Logic State ($V_{CC} = 4.75$ V, $I_{OH} = -20$ mA)	V_{OH}	2.4	—	—	V
Output Voltage — Low Logic State ($I_{OL} = 48$ mA)	V_{OL}	—	—	0.5	V
Output Current — High Impedance State ($V_{CC} = 5.25$ V, $V_{OH} = 2.4$ V) ($V_{CC} = 5.25$ V, $V_{OL} = 0.5$ V)	I_{OZ}	 — —	 — —	 100 −100	µA
Output Short-Circuit Current ($V_{CC} = 5.25$ V, $V_O = 0$) (only one output can be shorted at a time)	I_{OS}	−30	−80	−130	mA
Power Supply Current ($V_{CC} = 5.25$ V) MC3482A/MC6882A MC3482B/MC6882B	I_{CC}	—		130 150	mA
Input Clamp Voltage ($V_{CC} = 4.75$ V, $I_{IK} = -12$ mA)	V_{IK}	—	—	−1.2	V

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $0^\circ C \leqslant T_A \leqslant +75^\circ C$, unless otherwise noted, typical @ $T_A = 25^\circ C$.)

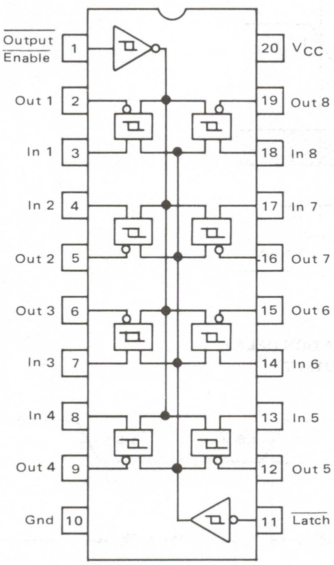
Characteristics	Symbol	MC3482A/ MC6882A			MC3482B/ MC6882B			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Times								ns
Data to Output								
Low to High	$t_{PLH(D)}$							
$C_L = 50$ pF		4.0	9.0	16	4.0	9.0	16	
$C_L = 250$ pF		—	12	20	—	12	20	
$C_L = 375$ pF		—	14	22	—	14	22	
$C_L = 500$ pF		10	16	24	10	16	24	
High to Low	$t_{PHL(D)}$							
$C_L = 50$ pF		4.0	8.0	16	4.0	8.0	16	
$C_L = 250$ pF		—	15	22	—	15	22	
$C_L = 375$ pF		—	18	25	—	17	24	
$C_L = 500$ pF		16	21	28	14	18	27	
Propagation Delay Times Latch Disable (Low to High) to Output								ns
Low to High $C_L = 50$ pF	$t_{PLH(L)}$	—	22	30	—	18	30	
High to Low $C_L = 50$ pF	$t_{PHL(L)}$	—	23	30	—	14	25	
Propagation Delay Times ($C_L = 20$ pF)								ns
High Output Level to High Impedance	$t_{PHZ(\overline{OE})}$	—	8.0	15	—	6.0	13	
Low Output to High Impedance	$t_{PLZ(\overline{OE})}$	—	20	27	—	15	23	
High Impedance to High Output	$t_{PZH(\overline{OE})}$	—	9.0	16	—	11	18	
High Impedance to Low Output	$t_{PZL(\overline{OE})}$	—	13	20	—	9.0	16	

AC SETUP CHARACTERISTICS (V_{CC} = 5.0 V, 0°C $\leqslant T_A \leqslant$ +75°C, unless otherwise noted, typical @ T_A = 25°C.)

Characteristic	Symbol	MC3482A/ MC6882A			MC3482B/ MC6882B			Unit
		Min	Typ	Max	Min	Typ	Max	
Setup Time (Data to Negative Going Latch Enable)	$t_{su(D)}$	10	0	–	7.0	0	–	ns
Hold Time (Data to Negative Going Latch Enable)	$t_{h(D)}$	10	–	–	8.0	–	–	ns
Minimum Latch Enable Pulse Width (High or Low)	$t_{W(L)}$	–	15	–	–	15	–	ns

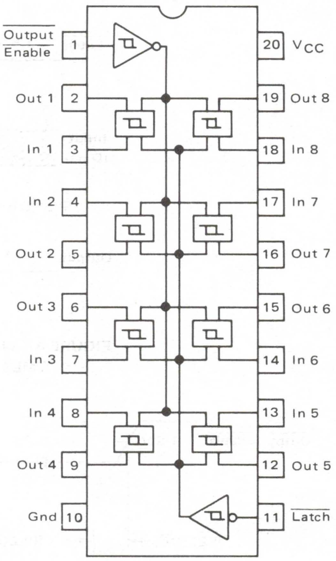
PIN CONNECTIONS AND TRUTH TABLES

MC3482A/MC6882A


$\overline{\text{Output Enable}}$
1
Out 1
2
In 1
3
In 2
4
Out 2
5
Out 3
6
In 3
7
In 4
8
Out 4
9
Gnd
10
20
V_{CC}
19
Out 8
18
In 8
17
In 7
16
Out 7
15
Out 6
14
In 6
13
In 5
12
Out 5
11
$\overline{\text{Latch}}$

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$	Input	Output
0	1	0	1
0	1	1	0
0	0	X	Q_o
1	X	X	Z

MC3482B/MC6882B


$\overline{\text{Output Enable}}$
1
Out 1
2
In 1
3
In 2
4
Out 2
5
Out 3
6
In 3
7
In 4
8
Out 4
9
Gnd
10
20
V_{CC}
19
Out 8
18
In 8
17
In 7
16
Out 7
15
Out 6
14
In 6
13
In 5
12
Out 5
11
$\overline{\text{Latch}}$

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$	Input	Output
0	1	0	0
0	1	1	1
0	0	X	Q_o
1	X	X	Z

FIGURE 1 — TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

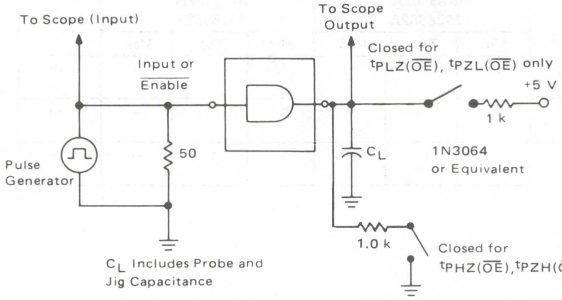
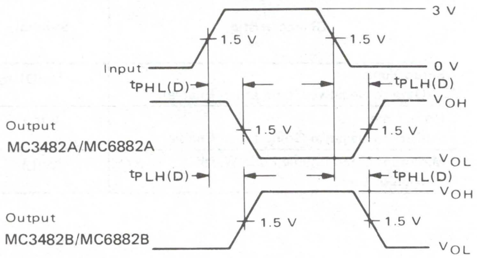

To Scope (Input)
Input or Enable
To Scope Output
Closed for tPLZ(OE), tPZL(OE) only
+5 V
1 k
Pulse Generator
50
CL
1N3064 or Equivalent
1.0 k
Closed for tPHZ(OE), tPZH(OE) only
CL Includes Probe and Jig Capacitance

FIGURE 2 — WAVEFORMS FOR PROPAGATION DELAY TIMES DATA TO OUTPUT


3 V
1.5 V
1.5 V
Input
0 V
tPHL(D)
tPLH(D)
VOH
Output MC3482A/MC6882A
1.5 V
1.5 V
VOL
tPLH(D)
tPHL(D)
VOH
Output MC3482B/MC6882B
1.5 V
1.5 V
VOL

Input Pulse Conditions
$t_{THL} = t_{TLH} \leq 5$ ns
f = 1.0 MHz

FIGURE 3 — WAVE FORMS FOR AC SETUP AND LATCH DISABLE TO OUTPUT DELAY

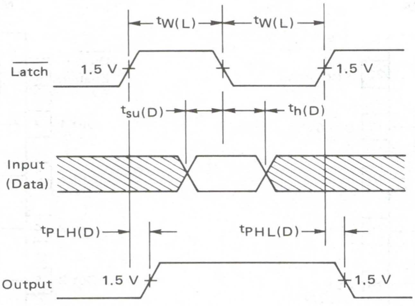
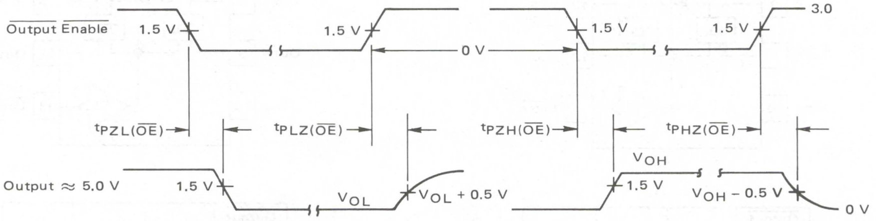

tW(L)
tW(L)
Latch
1.5 V
1.5 V
tsu(D)
th(D)
Input (Data)
tPLH(D)
tPHL(D)
Output
1.5 V
1.5 V

FIGURE 4 — WAVEFORMS FOR PROPAGATION DELAY TIMES — OUTPUT ENABLE TO OUTPUT


Output Enable
1.5 V
1.5 V
0 V
1.5 V
1.5 V
3.0
tPZL(OE)
tPLZ(OE)
tPZH(OE)
tPHZ(OE)
VOH
Output ≈ 5.0 V
1.5 V
VOL
VOL + 0.5 V
1.5 V
VOH − 0.5 V
0 V

MOTOROLA

MC3486

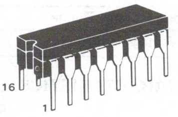
QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

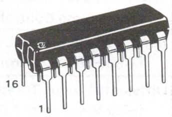
QUAD RS-422/423 LINE RECEIVER

Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reachs a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times – 25 ns (Typ)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source

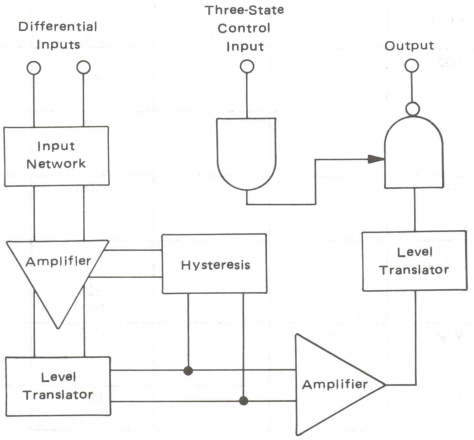


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

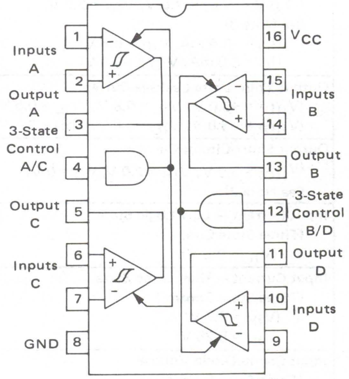


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

RECEIVER CHAIN BLOCK DIAGRAM


Differential Inputs
Three-State Control Input
Output
Input Network
Amplifier
Hysteresis
Level Translator
Level Translator
Amplifier

PIN CONNECTIONS


Inputs A
1
2
Output A
3
3-State Control A/C
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
Inputs B
14
Output B
13
3-State Control B/D
12
Output D
11
Inputs D
10
9

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3486L	0 to +70°C	Ceramic DIP
MC3486P	0 to +70°C	Plastic DIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	±15	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	−7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^{\circ}C$, $V_{CC} = 5.0$ V and $V_{IK} = 0$ V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage (Note 4) ($-7.0 \text{ V} \leqslant V_{IC} \leqslant 7.0 \text{ V}$, $V_{IH} = 2.0$ V)	$V_{TH(D)}$				V
($I_O = -0.4$ mA, $V_{OH} \geqslant 2.7$ V)		—	—	0.2	
($I_O = 8.0$ mA, $V_{OL} \geqslant 0.5$ V)		—	—	−0.2	
Input Bias Current ($V_{CC} = 0$ V or 5.25) (Other Inputs at 0 V)	$I_{IB(D)}$				mA
($V_I = -10$ V)		—	—	−3.25	
($V_I = -3.0$ V)		—	—	−1.50	
($V_I = +3.0$ V)		—	—	+1.50	
($V_I = +10$ V)		—	—	+3.25	
Input Balance and Output Level ($-7.0 \text{ V} \leqslant V_{IC} \leqslant 7.0 \text{ V}$, $V_{IH} = 2.0$ V, See Note 3)					V
($I_O = -0.4$ mA, $V_{ID} = 0.4$ V)	V_{OH}	2.7	—	—	
($I_O = 8.0$ mA, $V_{ID} = -0.4$ V)	V_{OL}	—	—	0.5	
Output Third State Leakage Current	I_{OZ}				μA
($V_{I(D)} = +3.0$ V, $V_{IL} = 0.8$ V, $V_{OL} = 0.5$ V)		—	—	−40	
($V_{I(D)} = -3.0$ V, $V_{IL} = 0.8$ V, $V_{OH} = 2.7$ V)		—	—	40	
Output Short-Circuit Current ($V_{I(D)} = 3.0$ V, $V_{IH} = 2.0$ V, $V_O = 0$ V) See Note 2)	I_{OS}	−15	—	−100	mA
Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.5$ V)	I_{IL}	—	—	−100	μA
Input Current — High Logic State (Three-State Control)	I_{IH}				μA
($V_{IH} = 2.7$ V)		—	—	20	
($V_{IH} = 5.25$ V)		—	—	100	
Input Clamp Diode Voltage (Three-State Control) ($I_{IK} = -10$ mA)	V_{IK}	—	—	−1.5	V
Power Supply Current ($V_{IL} = 0$ V)	I_{CC}	—	—	85	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

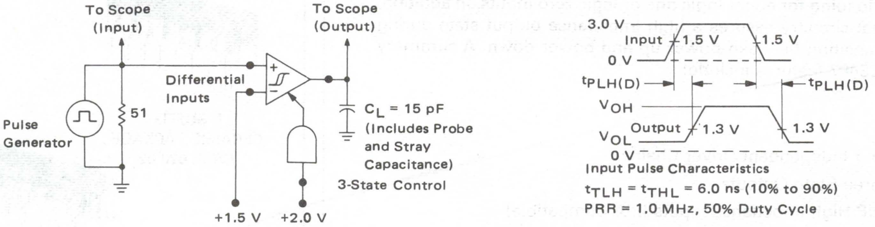
Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	35	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS

Propagation Delay Differential Input to Output


To Scope (Input)
To Scope (Output)
Differential Inputs
Pulse Generator
51
C_L = 15 pF (Includes Probe and Stray Capacitance)
3-State Control
+1.5 V
+2.0 V
3.0 V
Input
1.5 V
1.5 V
0 V
$t_{PLH(D)}$
$t_{PLH(D)}$
V_{OH}
Output
1.3 V
1.3 V
V_{OL}
0 V

Input Pulse Characteristics

$t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%)

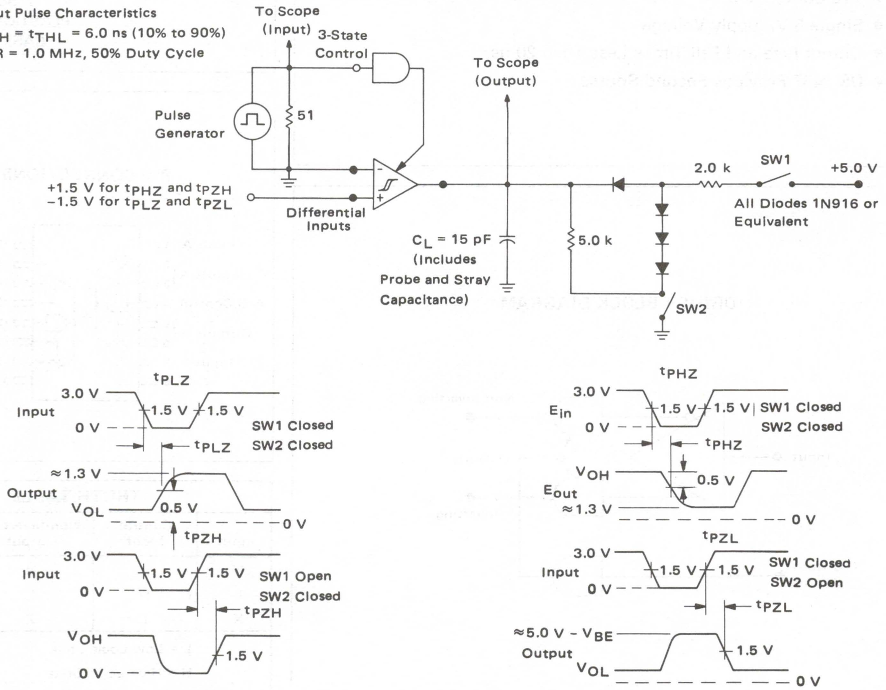
PRR = 1.0 MHz, 50% Duty Cycle

FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT

Input Pulse Characteristics

$t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%)

PRR = 1.0 MHz, 50% Duty Cycle


To Scope (Input)
3-State Control
To Scope (Output)
Pulse Generator
51
+1.5 V for t_{PHZ} and t_{PZH}
−1.5 V for t_{PLZ} and t_{PZL}
Differential Inputs
C_L = 15 pF (Includes Probe and Stray Capacitance)
5.0 k
2.0 k
SW1
+5.0 V
All Diodes 1N916 or Equivalent
SW2
t_{PLZ}
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Closed
t_{PLZ}
≈1.3 V
Output
V_{OL}
0.5 V
0 V
t_{PZH}
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Open
SW2 Closed
t_{PZH}
V_{OH}
1.5 V
0 V
t_{PHZ}
3.0 V
E_{in}
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Closed
t_{PHZ}
V_{OH}
0.5 V
E_{out}
≈1.3 V
0 V
t_{PZL}
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Open
t_{PZL}
≈5.0 V − V_{BE}
Output
1.5 V
V_{OL}
0 V

MC3487

MOTOROLA

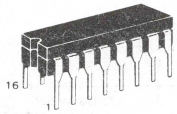
QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

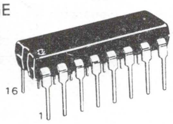
QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad RS-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

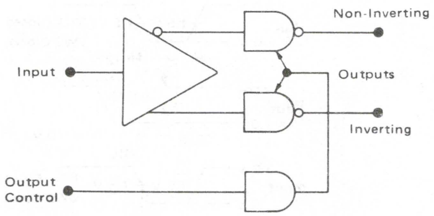


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

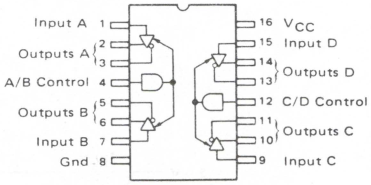


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

DRIVER BLOCK DIAGRAM


Non-Inverting
Input
Outputs
Inverting
Output
Control

PIN CONNECTIONS


Input A 1
Outputs A 2
3
A/B Control 4
Outputs B 5
6
Input B 7
Gnd 8
16 V_{CC}
15 Input D
14
13 Outputs D
12 C/D Control
11
10 Outputs C
9 Input C

TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$ and $0^{\circ}C \leqslant T_A \leqslant 70^{\circ}C$. Typical values measured at $V_{CC} = 5.0\ V$, and $T_A = 25^{\circ}C$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State ($V_{IL} = 0.5\ V$)	I_{IL}	–	–	-400	µA
Input Current – High Logic State	I_{IH}				µA
($V_{IH} = 2.7\ V$)		–	–	+50	
($V_{IH} = 5.5\ V$)		–	–	+100	
Input Clamp Voltage ($I_{IK} = -18\ mA$)	V_{IK}	–	–	–1.5	V
Output Voltage – Low Logic State ($I_{OL} = 48\ mA$)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State ($I_{OH} = -20\ mA$)	V_{OH}	2.5	–	–	V
Output Short-Circuit Current ($V_{IH} = 2.0\ V$) 2	I_{OS}	-40	–	-140	mA
Output Leakage Current – Hi-Z State	$I_{OL(Z)}$				µA
($V_{IL} = 0.5\ V$, $V_{IL(Z)} = 0.8\ V$)		–	–	±100	
($V_{IH} = 2.7\ V$, $V_{IL(Z)} = 0.8\ V$)		–	–	±100	
Output Leakage Current – Power OFF	$I_{OL(off)}$				µA
($V_{OH} = 6.0\ V$, $V_{CC} = 0\ V$)		–	–	+100	
($V_{OL} = -0.25\ V$, $V_{CC} = 0\ V$)		–	–	-100	
Output Offset Voltage Difference[1]	$V_{OS} - \overline{V}_{OS}$	–	–	±0.4	V
Output Differential Voltage 1	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference 1	$\lvert\Delta V_{OD}\rvert$	–	–	±0.4	V
Power Supply Current					mA
(Control Pins = Gnd)[3]	I_{CCX}	–	–	105	
(Control Pins = 2.0 V)	I_{CC}	–	–	85	

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\ V$, $T_A = 25^{\circ}C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	–	–	20	
Low to High Output	t_{PLH}	–	–	20	
Output Transition Times – Differential					ns
High to Low Output	t_{THL}	–	–	20	
Low to High Output	t_{TLH}	–	–	20	
Propagation Delay – Control to Output					ns
($R_L = 200\ \Omega$, $C_L = 50\ pF$)	$t_{PHZ(E)}$	–	–	25	
($R_L = 200\ \Omega$, $C_L = 50\ pF$)	$t_{PLZ(E)}$	–	–	25	
($R_L = \infty$, $C_L = 50\ pF$)	$t_{PZH(E)}$	–	–	30	
($R_L = 200\ \Omega$, $C_L = 50\ pF$)	$t_{PZL(E)}$	–	–	30	

FIGURE 1 — THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

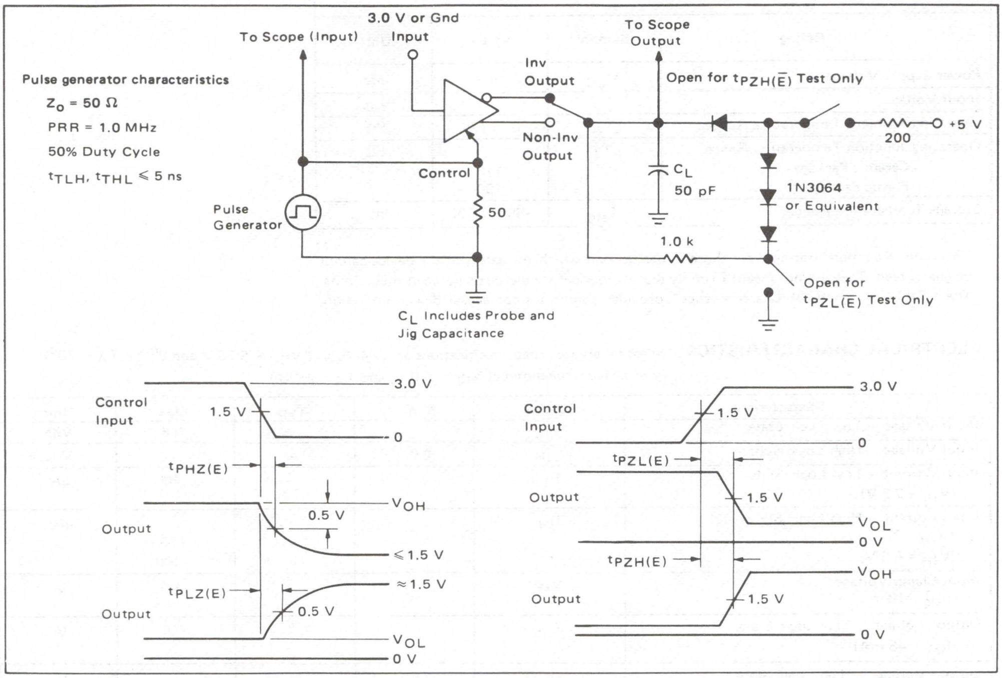

3.0 V or Gnd
Input
To Scope (Input)
To Scope
Output
Inv
Output
Non-Inv
Output
Open for $t_{PZH(\overline{E})}$ Test Only
200
+5 V
Pulse generator characteristics
Z_o = 50 Ω
PRR = 1.0 MHz
50% Duty Cycle
t_{TLH}, t_{THL} ≤ 5 ns
Control
Pulse
Generator
50
C_L
50 pF
1N3064
or Equivalent
1.0 k
Open for
$t_{PZL(\overline{E})}$ Test Only
C_L Includes Probe and
Jig Capacitance
Control
Input
1.5 V
3.0 V
0
$t_{PHZ(E)}$
Output
0.5 V
V_{OH}
≤1.5 V
$t_{PLZ(E)}$
Output
≈1.5 V
0.5 V
V_{OL}
0 V
Control
Input
1.5 V
3.0 V
0
$t_{PZL(E)}$
Output
1.5 V
V_{OL}
0 V
$t_{PZH(E)}$
Output
V_{OH}
1.5 V
0 V

FIGURE 2 — PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT

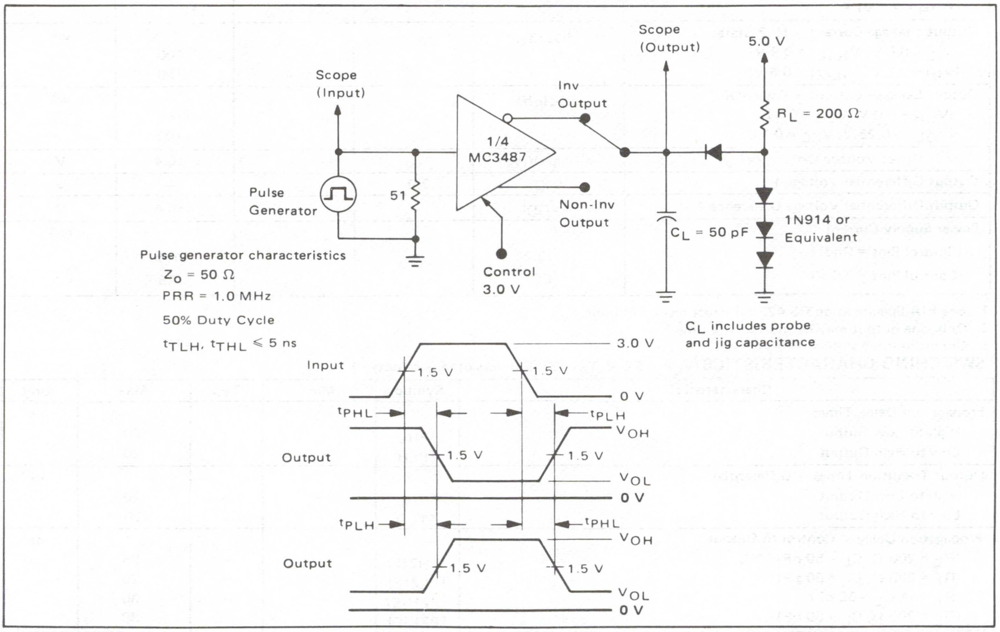

Scope
(Output)
5.0 V
Scope
(Input)
Inv
Output
1/4
MC3487
R_L = 200 Ω
Pulse
Generator
51
Non-Inv
Output
C_L = 50 pF
1N914 or
Equivalent
Control
3.0 V
Pulse generator characteristics
Z_o = 50 Ω
PRR = 1.0 MHz
50% Duty Cycle
t_{TLH}, t_{THL} ≤ 5 ns
C_L includes probe
and jig capacitance
Input
1.5 V
1.5 V
3.0 V
0 V
t_{PHL}
t_{PLH}
V_{OH}
Output
1.5 V
1.5 V
V_{OL}
0 V
t_{PLH}
t_{PHL}
V_{OH}
Output
1.5 V
1.5 V
V_{OL}
0 V

FIGURE 3 — OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

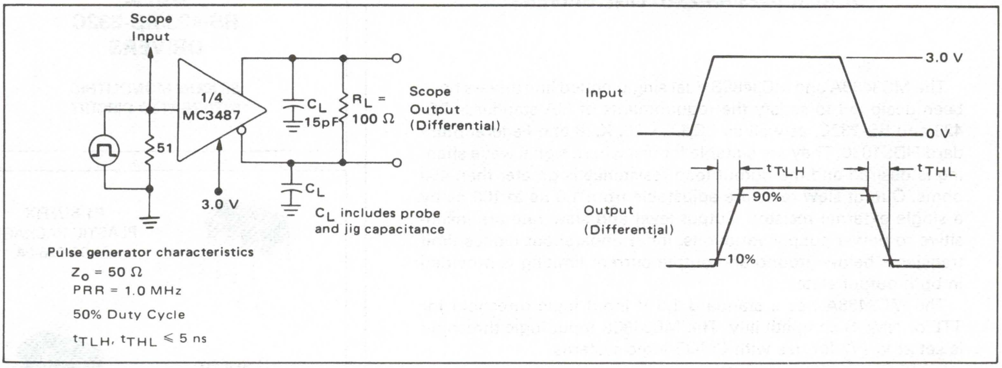

Scope
Input
1/4
MC3487
51
3.0 V
C_L
15pF
R_L =
100 Ω
Scope
Output
(Differential)
C_L
C_L includes probe
and jig capacitance
Pulse generator characteristics
Z_o = 50 Ω
PRR = 1.0 MHz
50% Duty Cycle
t_{TLH}, t_{THL} ≤ 5 ns
Input
3.0 V
0 V
t_{TLH}
t_{THL}
90%
10%
Output
(Differential)

FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE

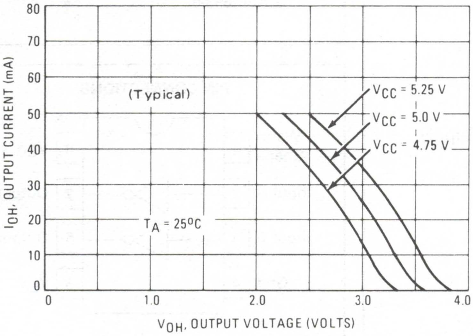
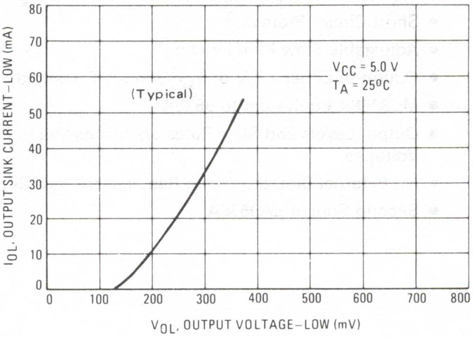


FIGURE 5 — OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



MC3488A
MC3488B

MOTOROLA

DUAL RS-423/RS-232C LINE DRIVERS

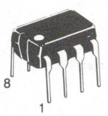
The MC3488A and MC3488B dual single-ended line drivers have been designed to satisfy the requirements of EIA standards RS-423 and RS-232C, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. They are suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μs to 100 μs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility. The MC3488B input logic threshold is set at $V_{CC}/2$ for use with CMOS logic systems.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- Option of Either 1.5 V or $V_{CC}/2$ Input Threshold
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V_{EE} Supply
- Second Source μA9636A

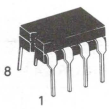
DUAL
RS-423/RS-232C
DRIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

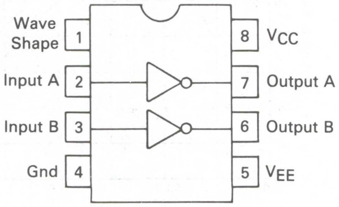


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04

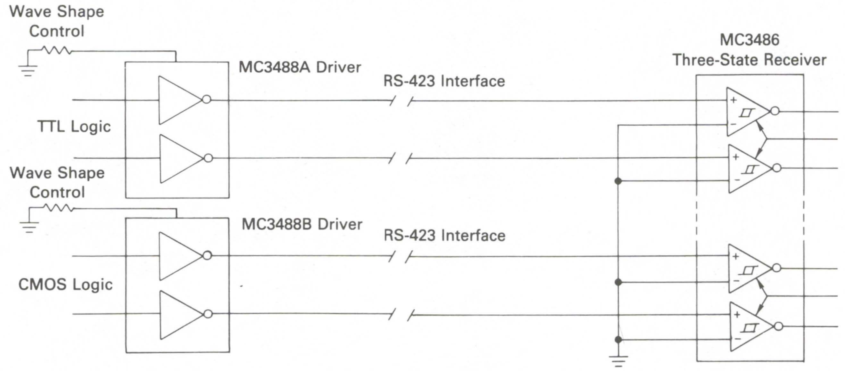
U SUFFIX
CERAMIC PACKAGE
CASE 693-02



PIN CONNECTIONS


Wave Shape
1
Input A
2
Input B
3
Gnd
4
8
V_{CC}
7
Output A
6
Output B
5
V_{EE}

TYPICAL APPLICATION


Wave Shape Control
MC3488A Driver
RS-423 Interface
TTL Logic
Wave Shape Control
MC3488B Driver
RS-423 Interface
CMOS Logic
MC3486
Three-State Receiver

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+15 −15	V
Output Current Source Sink	 I_{O+} I_{O-}	 +150 −150	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITION

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	10.8 −13.2	12 −12	13.2 −10.8	V
Operating Temperature Range	T_A	0	25	70	°C
Wave Shaping Resistor	R_{WS}	10	—	1000	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State MC3488A MC3488B	V_{IL}	 — —	 — —	 0.8 $V_{CC}/2 - 2.0$	V
Input Voltage — High Logic State MC3488A MC3488B	V_{IH}	 2.0 $V_{CC}/2 + 2.0$	 — —	 — —	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	−80	—	—	μA
Input Current — High Logic State (V_{IH} = 2.4 V MC3488A; V_{IH} = 10V MC3488B) (V_{IH} = 5.5 V MC3488A; V_{IH} = V_{CC} MC3488B)	 I_{IH1} I_{IH2}	 — —	 — —	 10 100	μA
Input Clamp Diode Voltage (I_{IK} = −15 mA)	V_{IK}	−1.5	—	—	V
Output Voltage — Low Logic State (R_L = ∞) RS-423 (R_L = 3.0 kΩ) RS-232C (R_L = 450 Ω) RS-423	V_{OL}	 −6.0 −6.0 −6.0	 — — —	 −5.0 −5.0 −4.0	V
Output Voltage — High Logic State (R_L = ∞) RS-423 (R_L = 3.0 kΩ) RS-232C (R_L = 450 Ω) RS-423	V_{OH}	 5.0 5.0 4.0	 — — —	 6.0 6.0 6.0	V
Output Resistance (R_L ≥ 450 Ω)	R_O	—	25	50	Ω
Output Short-Circuit Current (Note 2) (V_{in} = V_{out} = 0 V) (V_{in} = $V_{IH(Min)}$, V_{out} = 0 V)	 I_{OSH} I_{OSL}	 −150 +15	 — —	 −15 +150	mA
Output Leakage Current (Note 3) (V_{CC} = V_{EE} = 0 V, −6.0 V ≤ V_O ≤ 6.0 V)	I_{ox}	−100	—	100	μA
Power Supply Currents (R_W = 100 kΩ, R_L = ∞, V_{IL} ≤ V_{in} ≤ V_{IH})	I_{CC} I_{EE}	— −18	— —	+18 —	mA

Note 2: One output shorted at a time.
3: No V_{EE} diode required.

TRANSITION TIMES (Unless otherwise noted, C_L = 30 pF, f = 1.0 kHz, $V_{CC} = -V_{EE}$ = 12.0 V ± 10%, T_A = 25°C, R_L = 450 Ω. Transition times measured 10% to 90% and 90% to 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low-to-High State Output	t_{TLH}				µs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 50 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	
Transition Time, High-to-Low State Output	t_{THL}				µs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 500 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	

FIGURE 1 — TEST CIRCUIT & WAVEFORMS FOR TRANSITION TIMES

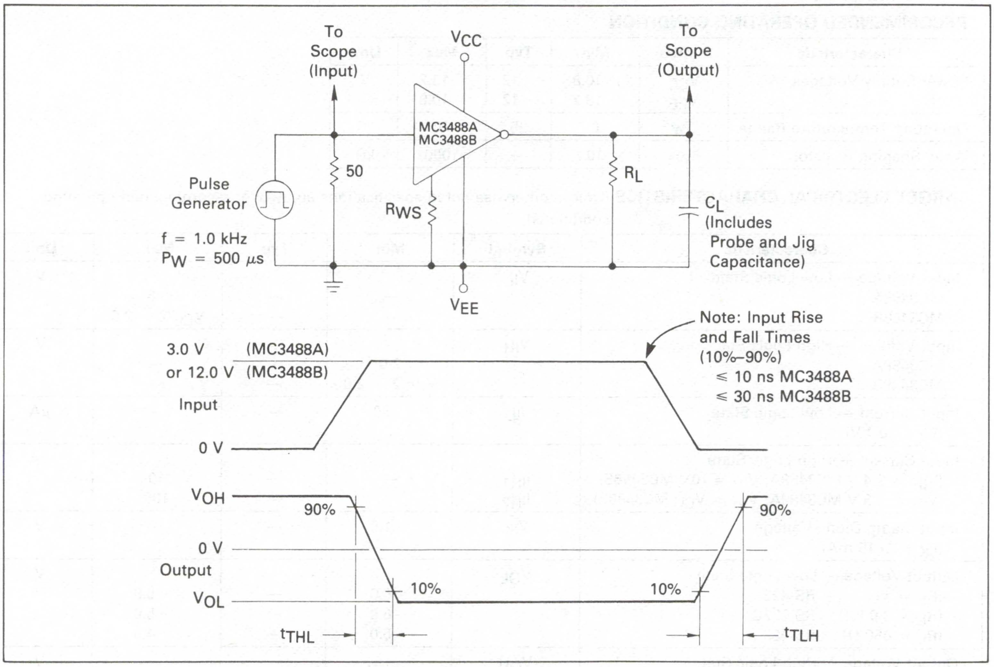

To Scope (Input)
VCC
To Scope (Output)
MC3488A
MC3488B
50
RL
Pulse Generator
RWS
CL (Includes Probe and Jig Capacitance)
f = 1.0 kHz
PW = 500 µs
VEE
Note: Input Rise and Fall Times (10%–90%)
≤ 10 ns MC3488A
≤ 30 ns MC3488B
3.0 V (MC3488A)
or 12.0 V (MC3488B)
Input
0 V
VOH
90%
90%
0 V
Output
VOL
10%
10%
tTHL
tTLH

FIGURE 2 — OUTPUT TRANSITION TIMES versus WAVE SHAPE RESISTOR VALUE

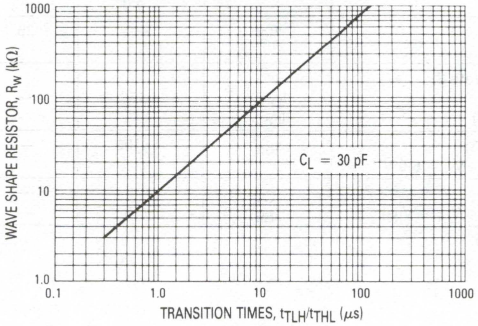


FIGURE 3 — INPUT/OUTPUT CHARACTERISTICS versus TEMPERATURE

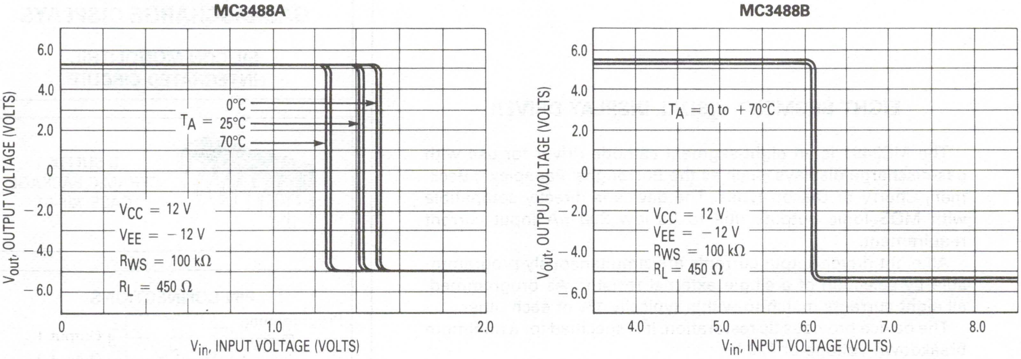


FIGURE 4 — MC3488A/B OUTPUT CURRENT versus OUTPUT VOLTAGE

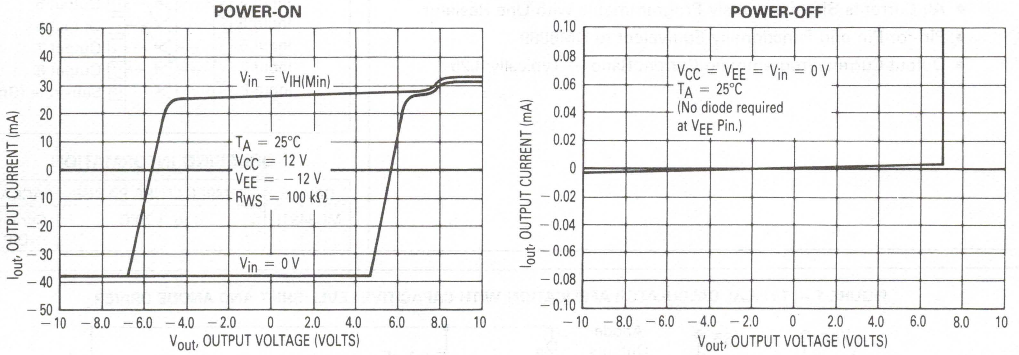


FIGURE 5 — SUPPLY CURRENT versus TEMPERATURE

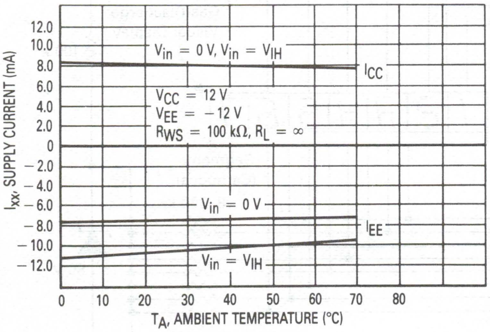
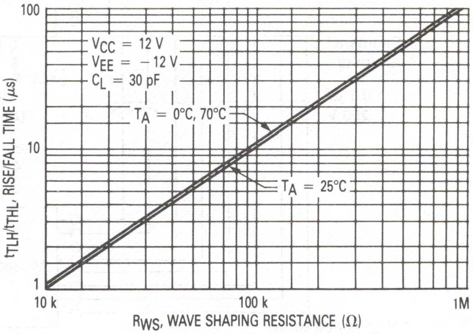


FIGURE 6 — RISE/FALL TIME versus R_{WS}



MC3491

MOTOROLA

SEGMENT DRIVER FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC INTEGRATED CIRCUIT

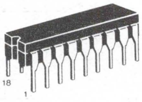
EIGHT-SEGMENT VISUAL DISPLAY DRIVER

The MC3491 is an eight-segment cathode driver for use with gas-discharge displays, such as the Burroughs' Panaplex®, Beckman, Cherry or Diacon types. The device is directly compatible with MOS logic outputs due to its low 300 μA input current requirement.

All eight driver output currents are simultaneously programmable by selection of a single external resistor. As programmed, all eight currents match to within typically 1% of each other.

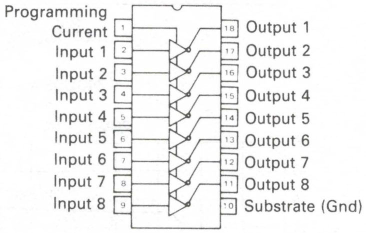
The device provides dc restoration. It is specified for a minimum breakdown voltage of 120 V.

- High Breakdown Voltage — 120 V Min
- Drives Seven Cathode Segments plus Decimal Point
- All Currents Simultaneously Programmable with One Resistor
- Pin-for-Pin and Functionally Equivalent to DM8889
- Output Current/Programming Current Ratio — Typically 4.25:1



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

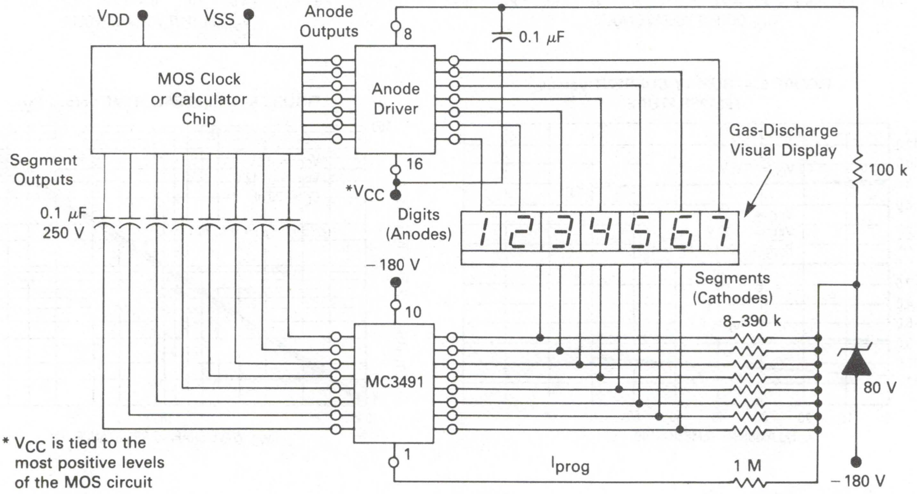
PIN CONNECTIONS


Programming Current 1
Input 1 2
Input 2 3
Input 3 4
Input 4 5
Input 5 6
Input 6 7
Input 7 8
Input 8 9
18 Output 1
17 Output 2
16 Output 3
15 Output 4
14 Output 5
13 Output 6
12 Output 7
11 Output 8
10 Substrate (Gnd)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3491L	0 to +70°C	Ceramic DIP

FIGURE 1 — TYPICAL CALCULATOR APPLICATION WITH CAPACITIVE LEVEL SHIFT AND ANODE DRIVER


V$_{DD}$
V$_{SS}$
Anode Outputs
8
0.1 μF
MOS Clock or Calculator Chip
Anode Driver
Gas-Discharge Visual Display
100 k
Segment Outputs
16
*V$_{CC}$
0.1 μF 250 V
Digits (Anodes)
1 2 3 4 5 6 7
−180 V
10
Segments (Cathodes)
8–390 k
MC3491
80 V
1
I$_{prog}$
1 M
−180 V

* V$_{CC}$ is tied to the most positive levels of the MOS circuit

MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25°C$)

Rating	Symbol	Value	Unit
Output OFF Voltage (Current Limited to 0.5 mA)	$V_{O(off)}$	150	V
Output ON Voltage (Current Limited to 2.0 mA)	$V_{O(on)}$	50	V
Input Voltage	V_I	20	V
Programming Current	I_{prog}	400	µA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 0°C to +70°C, $V_{CC} < 120$ V, Typ @ 25°C, Pin 10 = Gnd. All voltages with respect to Gnd.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{IH} = 7.0 V) (V_{IH} = 3.5 V)	I_{IH}	200 75	300 —	500 200	µA
Input Clamp Voltage (I_{IK} = −1.0 mA)	V_{IK}	—	—	−1.0	V
Input OFF Voltage (V_{out} = 80 V)	V_{IL}	0.9	1.6	—	V
Input ON Voltage	V_{IH}	—	1.6	3.5	V
Output OFF Current (V_{IL} = 0.9 V, V_O = 120 V)	$I_{O(off)}$	—	0.05	1.0	µA
Output ON Current (V_{IH} = 3.5 V, V_{out} = 20 V) (I_{prog} = 100 µA) (I_{prog} = 350 µA)	$I_{O(on)}$	350 800 —	425 1490 —	550 1700 —	µA
Output Current Matching (All eight outputs)	ΔI_O	—	≤1	≤10	%
Output Voltage Compliance Range (I_{prog} = 350 µA, V_{IH} = 3.5 V) (See Figure 3)	$V_{OR(on)}$	 20 —	 — —	 50 —	V

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 — OUTPUT CURRENT versus PROGRAMMING CURRENT (T_A = 25°C)

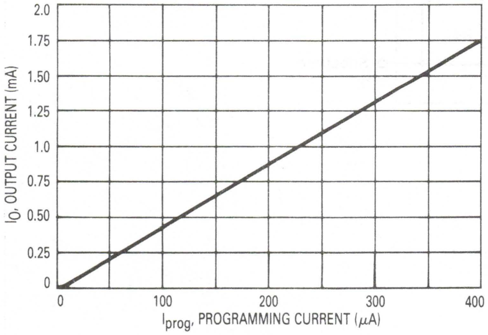
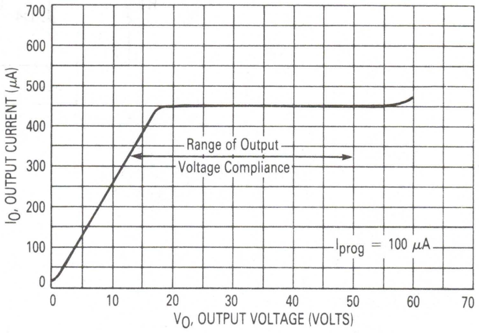


FIGURE 3 — OUTPUT CURRENT versus OUTPUT VOLTAGE (V_{IH} = 7.0 V, T_A = 25°C)



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 4 — TYPICAL INPUT CURRENT AND OUTPUT VOLTAGE versus INPUT VOLTAGE

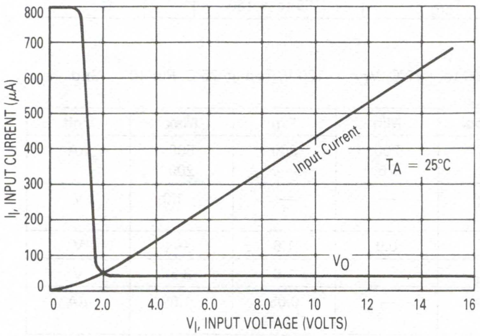
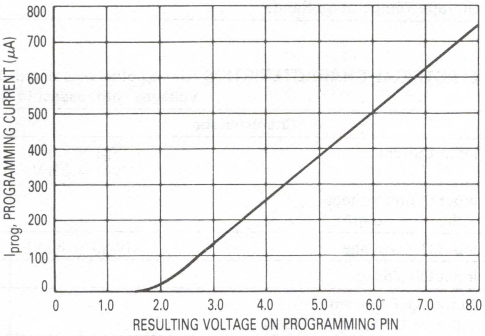
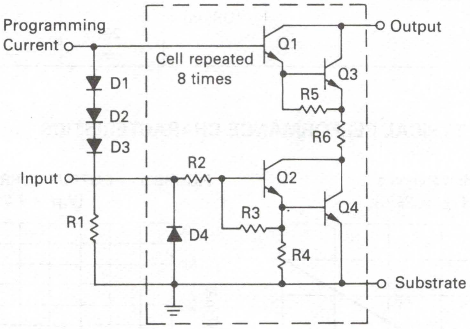


FIGURE 5 — TYPICAL PROGRAMMING CURRENT versus VOLTAGE ON PROGRAMMING PIN
(T_A = 25°C)



REPRESENTATIVE CIRCUIT SCHEMATIC


Programming Current
Cell repeated 8 times
Output
Q1
Q3
D1
D2
D3
R5
R6
Input
R2
Q2
Q4
R3
R1
D4
R4
Substrate

3½-DIGIT VOLTMETER

This specific application provides a 3½-digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3½-digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the Anode Drivers. Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors connected in a common-base, constant-current configuration are turned on by the negative-going digit select output pulses of the MC14435. The current of approximately 330 μA is compatible with 200 μA typical input current of anode drivers and the sink current capability of the MC14435.

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 Segment Driver. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment current is increased accordingly to 1.1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

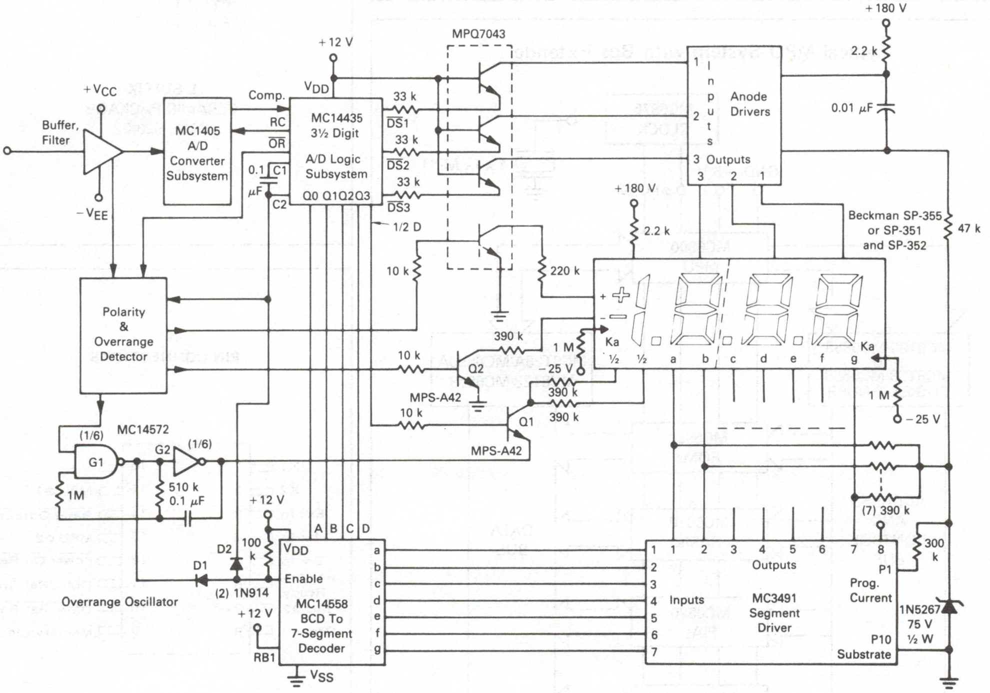
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The ½-digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8.0 Hz). This is accomplished by blanking the ½ digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 — 3½ DIGIT DIGITAL VOLTMETER



+VCC
Buffer, Filter
−VEE
MC1405 A/D Converter Subsystem
Comp.
RC
OR
VDD
+12 V
MC14435 3½ Digit A/D Logic Subsystem
0.1 μF
C1
C2
Q0 Q1 Q2 Q3
33 k
DS1
DS2
DS3
1/2 D
MPQ7043
10 k
220 k
Polarity & Overrange Detector
+180 V
2.2 k
1 2 3 Inputs
Anode Drivers
Outputs 3 2 1
0.01 μF
Beckman SP-355 or SP-351 and SP-352
47 k
390 k
1 M
−25 V
Ka
½
a b c d e f g
Q2
MPS-A42
Q1
MPS-A42
(7) 390 k
MC14572
(1/6)
G1
G2
1M
510 k
0.1 μF
D2
100 k
D1
(2) 1N914
Overrange Oscillator
A B C D
VDD
Enable
MC14558 BCD To 7-Segment Decoder
RB1
VSS
Inputs
Outputs
MC3491 Segment Driver
Prog. Current
P1
P10 Substrate
300 k
1N5267 75 V ½ W

MC6875
MC6875A

MOTOROLA

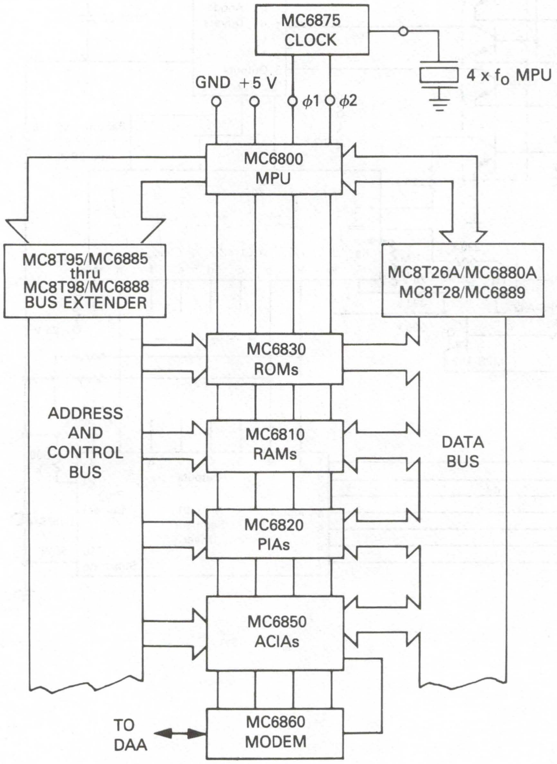
Specifications and Applications Information

M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi1$ and $\phi2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

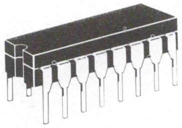
Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

Typical MPU System with Bus Extenders


MC6875 CLOCK
4 x f_o MPU
GND
+5 V
ϕ1
ϕ2
MC6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T26A/MC6880A MC8T28/MC6889
MC6830 ROMs
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 MODEM
ADDRESS AND CONTROL BUS
DATA BUS
TO DAA

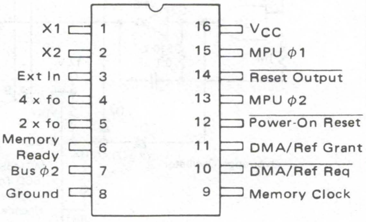
M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620-02

PIN CONNECTIONS


X1 1
X2 2
Ext In 3
4 x fo 4
2 x fo 5
Memory Ready 6
Bus ϕ2 7
Ground 8
16 VCC
15 MPU ϕ1
14 Reset Output
13 MPU ϕ2
12 Power-On Reset
11 DMA/Ref Grant
10 DMA/Ref Req
9 Memory Clock

ORDERING INFORMATION

Device	Temperature Range	Package
MC6875L	0 to +70°C	Ceramic DIP
MC6875AL	-55 to +125°C	

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted T_A = 25°C.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_I	+5.5	Vdc
Operating Ambient Temperature Range MC6875L MC6875AL	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	175	°C

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum T_A) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A \approx 95°C$.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State MPU ϕ1 and ϕ2 Outputs (V_{CC} = 4.75 V, I_{OHM} = -200 μA)	V_{OHM}	V_{CC} - 0.6	—	—	V
(V_{CC} = 5.25 V, I_{OHMK} = +5.0 mA)	V_{OHMK}	—	—	V_{CC} + 1.0	
Bus ϕ2 Output (V_{CC} = 4.75 V, I_{OHB} = -10 mA)	V_{OHB}	2.4	—	—	V
(V_{CC} = 5.25 V, I_{OHBK} = +5.0 mA)	V_{OHBK}	—	—	V_{CC} + 1.0	
4 x fo Output (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OH4X} = -500 μA)	V_{OH4X}	2.4	—	—	V
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OH} = -500 μA)	V_{OH}	2.4	—	—	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IH} = 3.3 V, $I_{OH\overline{R}}$ = -100 μA)	$V_{OH\overline{R}}$	2.4	—	—	V
Output Voltage — Low Logic State MPU ϕ1 and ϕ2 Outputs (V_{CC} = 4.75 V, I_{OLM} = +200 μA)	V_{OLM}	—	—	0.4	V
(V_{CC} = 4.75 V, I_{OLMK} = -5.0 mA)	V_{OLMK}	—	—	-1.0	
Bus ϕ2 Output (V_{CC} = 4.75 V, I_{OLB} = +48 mA)	V_{OLB}	—	—	0.5	V
(V_{CC} = 4.75 V, I_{OLBK} = -5.0 mA)	V_{OLBK}	—	—	-1.0	
4 x fo Output (V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL4X} = 16 mA)	V_{OL4X}	—	—	0.5	V
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OL} = 16 mA)	V_{OL}	—	—	0.5	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IL} = 0.8 V, $I_{OL\overline{R}}$ = 3.2 mA)	$V_{OL\overline{R}}$	—	—	0.5	V
Input Voltage — High Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IL}	—	—	0.8	V
Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2) Output Low to High	V_{ILH}	—	2.8	3.6	V
Output High to Low	V_{IHL}	0.8	1.4	—	
Input Clamp Voltage MC6875L (V_{CC} = 4.75 V, I_{IC} = -5.0 mA)	V_{IK}	—	—	-1.0	V
MC6875AL		—	—	-1.5	
Input Current — High Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 4.75 V, V_{IH} = 5.0 V)	I_{IH}	—	—	25	μA
$\overline{\text{Power-On Reset}}$ (V_{CC} = 5.0 V, $V_{IH\overline{R}}$ = 5.0 V)	$I_{IH\overline{R}}$	—	—	50	μA
Input Current — Low Logic State Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	I_{IL}	—	—	-250	μA
$\overline{\text{Power-On Reset}}$ Input (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	$I_{IL\overline{R}}$	—	—	-250	μA

OPERATING DYNAMIC POWER SUPPLY CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Currents (V_{CC} = 5.25 V, f_{osc} = 8.0 MHz, V_{IL} = 0 V, V_{IH} = 3.0 V) Normal Operation (Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs at High Logic State)	I_{CCN}	–	–	150	mA
Memory Ready Stretch Operation (Memory Ready Input at Low Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at High Logic State)	I_{CCMR}	–	–	135	mA
$\overline{\text{DMA/Refresh Request}}$ Stretch Operation (Memory Ready Input at High Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at Low Logic State)	I_{CCDR}	–	–	135	mA

SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10).
Typical values measured at V_{CC} = 5.0 V, T_A = 25°C, fo = 1.0 MHz (see Figure 8).

Characteristic	Symbol	Min	Typ	Max	Unit
MPU φ1 AND φ2 CHARACTERISTICS					
Output Period (Figure 3)	t_o	500	–	–	ns
Pulse Width (Figure 3)	t_{PWM}				ns
(fo = 1.0 MHz)		400	–	–	
(fo = 1.5 MHz)		230	–	–	
(fo = 2.0 MHz)		180	–	–	
Total Up Time (Figure 3)	t_{UPM}				ns
(fo = 1.0 MHz)		900	–	–	
(fo = 1.5 MHz)		600	–	–	
(fo = 2.0 MHz)		440	–	–	
Delay Time Referenced to Output Complement (Figure 3) Output High to Low State (Clock Overlap at 1.0 V)	t_{PLHM}	0	–	–	ns
Delay Times Referenced to 2 x fo (Figure 4 MPU φ2 only)					
Output Low to High Logic State	t_{PLHM2X}	–	–	85	ns
Output High to Low Logic State	t_{PHLM2X}	–	–	70	ns
Transition Times (Figure 3)					
Output Low to High Logic State	t_{TLHM}	–	–	25	ns
Output High to Low Logic State	t_{THLM}	–	–	25	ns
BUS φ2 CHARACTERISTICS					
Pulse Width – Low Logic State (Figure 4)	t_{PWLB}				ns
(fo = 1.0 MHz)		430	–	–	
(fo = 1.5 MHz)		280	–	–	
(fo = 2.0 MHz)		210	–	–	
Pulse Width – High Logic State	t_{PWHB}				ns
(fo = 1.0 MHz)		450	–	–	
(fo = 1.5 MHz)		295	–	–	
(fo = 2.0 MHz)		235	–	–	
Delay Times – (Referenced to MPU φ1) (Figure 4)					
Output Low to High Logic State	t_{PLHBM1}				ns
(fo = 1.0 MHz)		480	–	–	
(fo = 1.5 MHz)		320	–	–	
(fo = 2.0 MHz)		240	–	–	
Output High to Low Logic State	t_{PHLBM1}				
(C_L = 300 pF)		–	–	25	
(C_L = 100 pF)		–	–	20	
Delay Times (Referenced to MPU φ2) (Figure 4)					
Output Low to High Logic State	t_{PLHBM2}	-30	–	+25	ns
Output High to Low Logic State	t_{PHLBM2}	0	–	+40	ns
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLHB}	–	–	20	ns
Output High to Low Logic State	t_{THLB}	–	–	20	ns

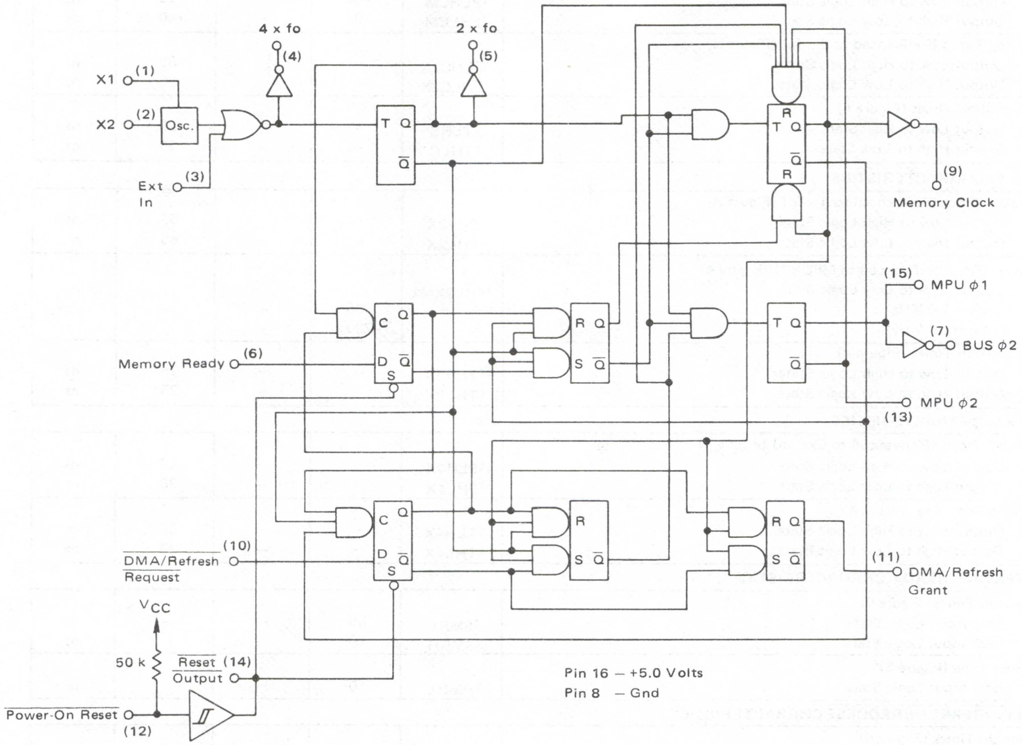
SWITCHING CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
MEMORY CLOCK CHARACTERISTICS					
Delay Times (Referenced to MPU $\phi 2$) (Figure 4)					
Output Low to High Logic State	t_{PLHCM}	-50	–	+25	ns
Output High to Low Logic State	t_{PHLCM}	0	–	+40	ns
Delay Times (Referenced to 2 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLHC2X}	–	–	65	ns
Output High to Low Logic State	t_{PHLC2X}	–	–	85	ns
Transition Times (Figure 4)					
Output Low to High State	t_{TLHC}	–	–	25	ns
Output High to Low State	t_{THLC}	–	–	25	ns
2 x fo CHARACTERISTICS					
Delay Times (Referenced to 4 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLH2X}	–	–	50	ns
Output High to Low Logic State	t_{PHL2X}	–	–	65	ns
Delay Time (Referenced to MPU $\phi 1$) (Figure 4)					
Output High to Low Logic State	$t_{PHL2XM1}$				ns
(fo = 1.0 MHz)		365	–	–	
(fo = 1.5 MHz)		220	–	–	
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLH2X}	–	–	25	ns
Output High to Low Logic State	t_{THL2X}	–	–	25	ns
4 x fo CHARACTERISTICS					
Delay Times (Referenced to Ext. In) (Figure 4)					
Output Low to High Logic State	t_{PLH4X}	–	–	50	ns
Output High to Low Logic State	t_{PHL4X}	–	–	30	ns
Transition Time (Figure 4)					
Output Low to High Logic State	t_{TLH4X}	–	–	25	ns
Output High to Low Logic State	t_{THL4X}	–	–	25	ns
MEMORY READY CHARACTERISTICS					
Set-Up Times (Figure 5)					
Low Input Logic State	t_{SMRL}	55	–	–	ns
High Input Logic State	t_{SMRH}	75	–	–	ns
Hold Time (Figure 5)					
Low Input Logic State	t_{HMRL}	10	–	–	ns
$\overline{\text{DMA/REFRESH REQUEST}}$ CHARACTERISTICS					
Set-Up Times (Figure 6)					
Low Input Logic State	t_{SDRL}	65	–	–	ns
High Input Logic State	t_{SDRH}	75	–	–	ns
Hold Time (Figure 6)					
Low Input Logic State	t_{HDRL}	10	–	–	ns
DMA/REFRESH GRANT CHARACTERISTICS					
Delay Time Referenced to Memory Clock (Figure 6)					
Output Low to High Logic State	t_{PLHG}	-15	–	+25	ns
Output High to Low Logic State	t_{PHLG}	-25	–	+15	ns
Transition Times (Figure 6)					
Output Low to High Logic State	t_{TLHG}	–	–	25	ns
Output High to Low Logic State	t_{THLG}	–	–	25	ns
$\overline{\text{RESET}}$ CHARACTERISTICS					
Delay Time Referenced to $\overline{\text{Power-On Reset}}$ (Figure 7)					
Output Low to High Logic State	$t_{PLH\overline{R}}$	–	–	1000	ns
Output High to Low Logic State	$t_{PHL\overline{R}}$	–	–	250	ns
Transition Times (Figure 7)					
Output Low to High Logic State	$t_{TLH\overline{R}}$	–	–	100	ns
Output High to Low Logic State	$t_{THL\overline{R}}$	–	–	50	ns

DESCRIPTION OF PIN FUNCTIONS

• 4 x fo	– A free running oscillator at four times the MPU clock rate useful for a system sync signal.
• 2 x fo	– A free running oscillator at two times the MPU clock rate.
• $\overline{\text{DMA/REF REQ}}$	– An asynchronous input used to freeze the MPU clocks in the $\phi 1$ high, $\phi 2$ low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
• REF GRANT	– A synchronous output used to synchronize the refresh or DMA operation to the MPU.
• MEMORY READY	– An asynchronous input used to freeze the MPU clocks in the $\phi 1$ low, $\phi 2$ high state for slow memory interface.
• MPU $\phi 1$ MPU $\phi 2$	– Capable of driving the $\phi 1$ and $\phi 2$ inputs on two MC6800s.
• BUS $\phi 2$	– An output nominally in phase with MPU $\phi 2$ having MC8T26A type drive capability.
• $\underline{\text{MEMORY CLOCK}}$	– An output nominally in phase with MPU $\phi 2$ which free runs during a refresh request cycle.
• $\overline{\text{POWER-ON RESET}}$	– A Schmitt trigger input which controls $\overline{\text{Reset}}$. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to V_{CC}. See General Design Suggestions for Manual Reset Operation.
• $\overline{\text{RESET}}$	– An output to the MPU and I/O devices.
• X1, X2	– Provision to attach a series resonant crystal or RC network.
• EXT IN	– Allows driving by an external TTL signal to synchronize the MPU to an external system.

FIGURE 1 – BLOCK DIAGRAM


4 x fo
(4)
2 x fo
(5)
X1 (1)
X2 (2)
Osc.
Ext In (3)
T Q
Q̄
R
T Q
Q̄
R
(9)
Memory Clock
(15) MPU ϕ1
(7) BUS ϕ2
MPU ϕ2
(13)
C Q
D Q̄
S
R Q
S Q̄
T Q
Q̄
Memory Ready (6)
DMA/Refresh Request (10)
C Q
D Q̄
S
R
S Q̄
R Q
S Q̄
(11) DMA/Refresh Grant
VCC
50 k
Reset Output (14)
Power-On Reset (12)

Pin 16 – +5.0 Volts
Pin 8 – Gnd

FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF $\overline{\text{RESET}}$ FUNCTION

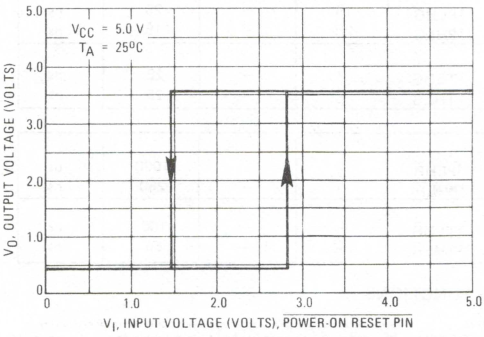
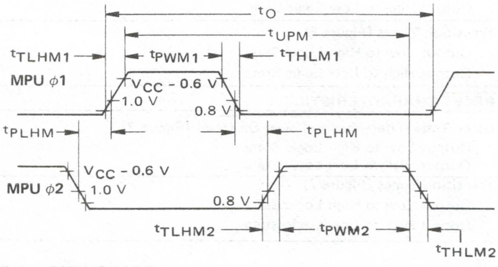


FIGURE 3 – TIMING DIAGRAM FOR MPU ϕ1 AND ϕ2


t_O
t_{UPM}
t_{TLHM1}
t_{PWM1}
t_{THLM1}
MPU ϕ1
V_{CC} - 0.6 V
1.0 V
0.8 V
t_{PLHM}
t_{PLHM}
V_{CC} - 0.6 V
MPU ϕ2
1.0 V
0.8 V
t_{TLHM2}
t_{PWM2}
t_{THLM2}

V_{OV} = 1.0 V = Clock Overlap measurement point

FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION
(Memory Ready and $\overline{\text{DMA/Refresh Request}}$ held high continuously)
Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns

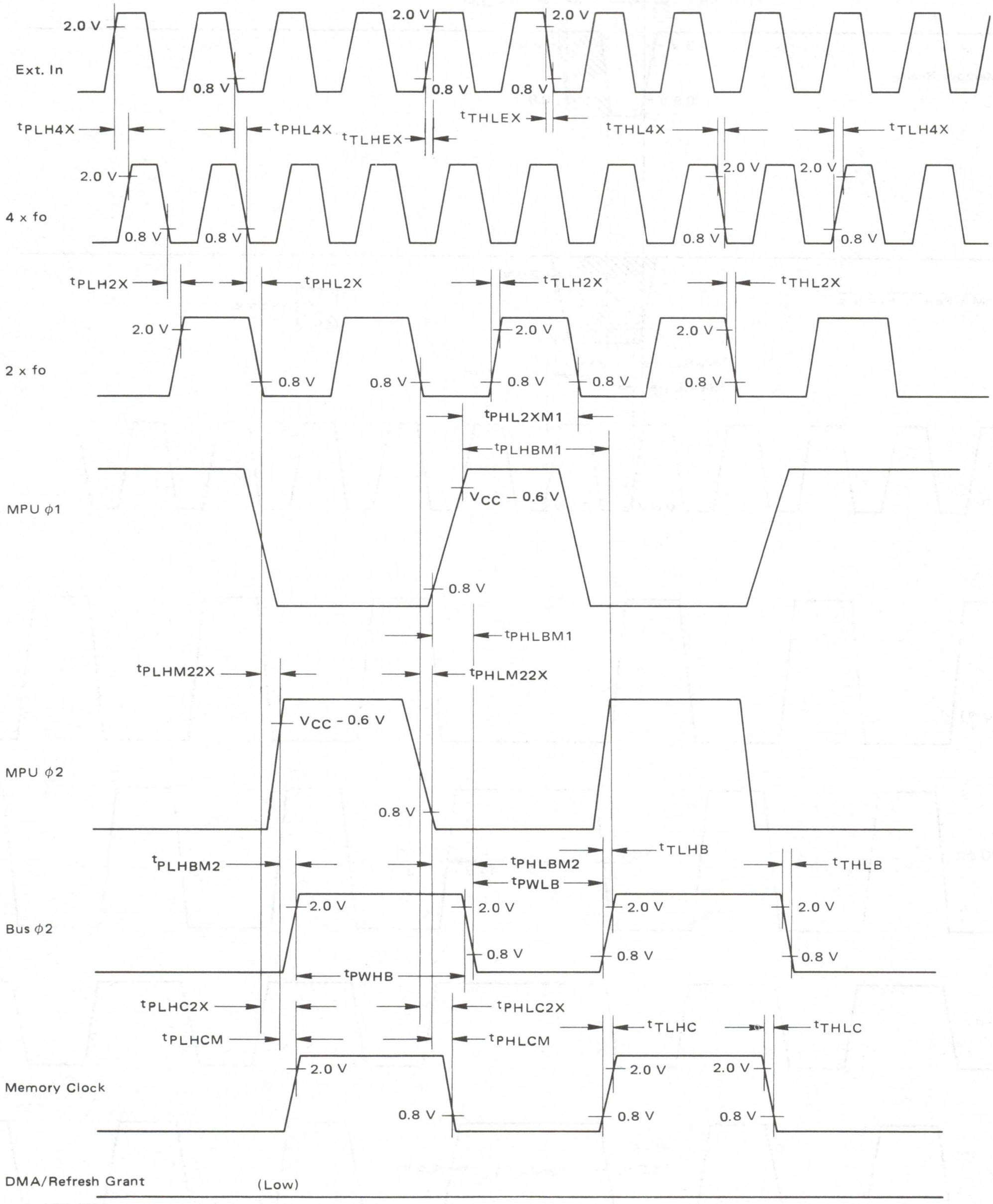

Ext. In
2.0 V
0.8 V
tPLH4X
tPHL4X
tTLHEX
tTHLEX
tTHL4X
tTLH4X
4 x fo
tPLH2X
tPHL2X
tTLH2X
tTHL2X
2 x fo
tPHL2XM1
tPLHBM1
MPU ϕ1
VCC – 0.6 V
tPHLBM1
tPLHM22X
tPHLM22X
MPU ϕ2
tPLHBM2
tPHLBM2
tPWLB
tTLHB
tTHLB
Bus ϕ2
tPWHB
tPLHC2X
tPHLC2X
tPLHCM
tPHLCM
tTLHC
tTHLC
Memory Clock
DMA/Refresh Grant
(Low)

FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns

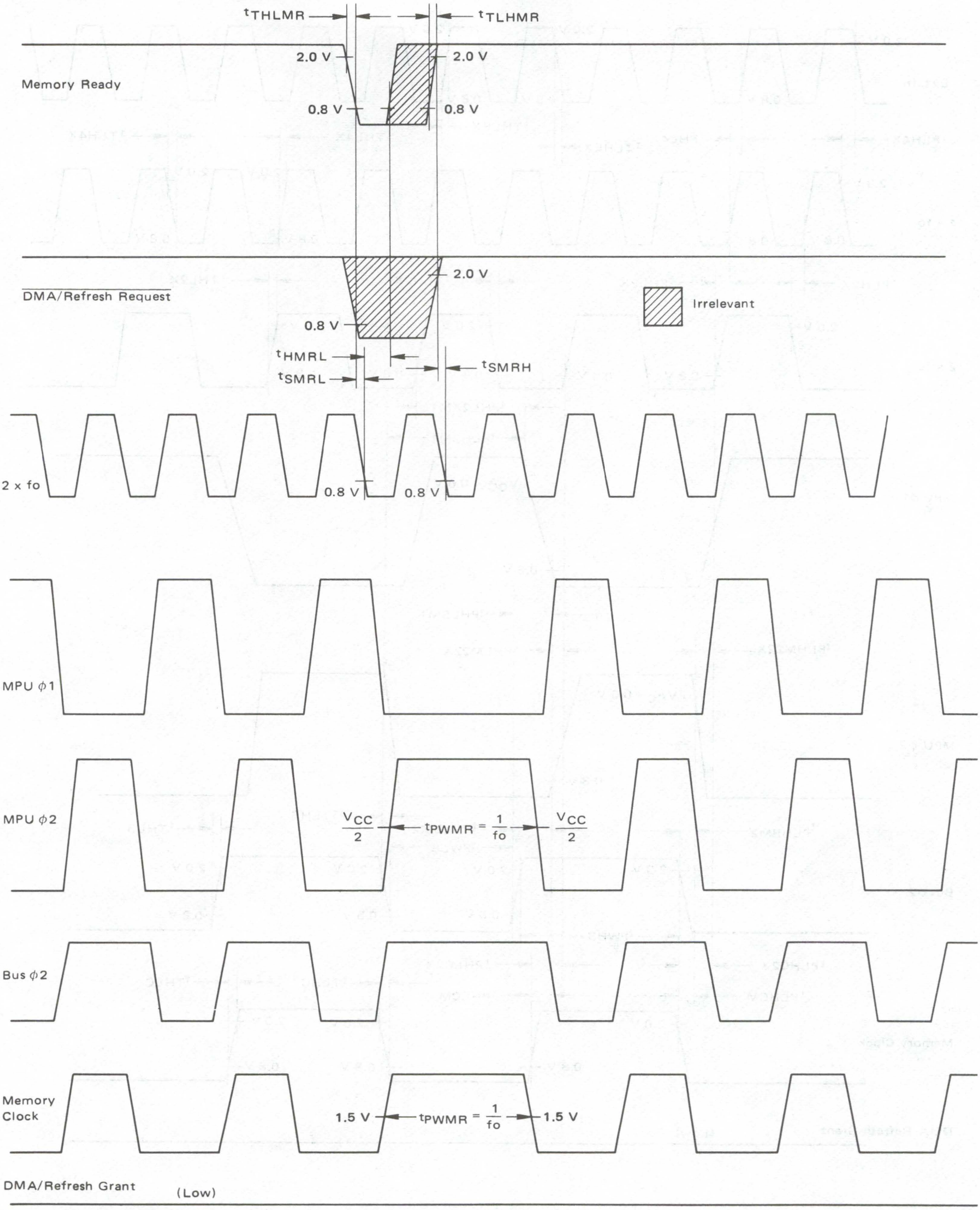
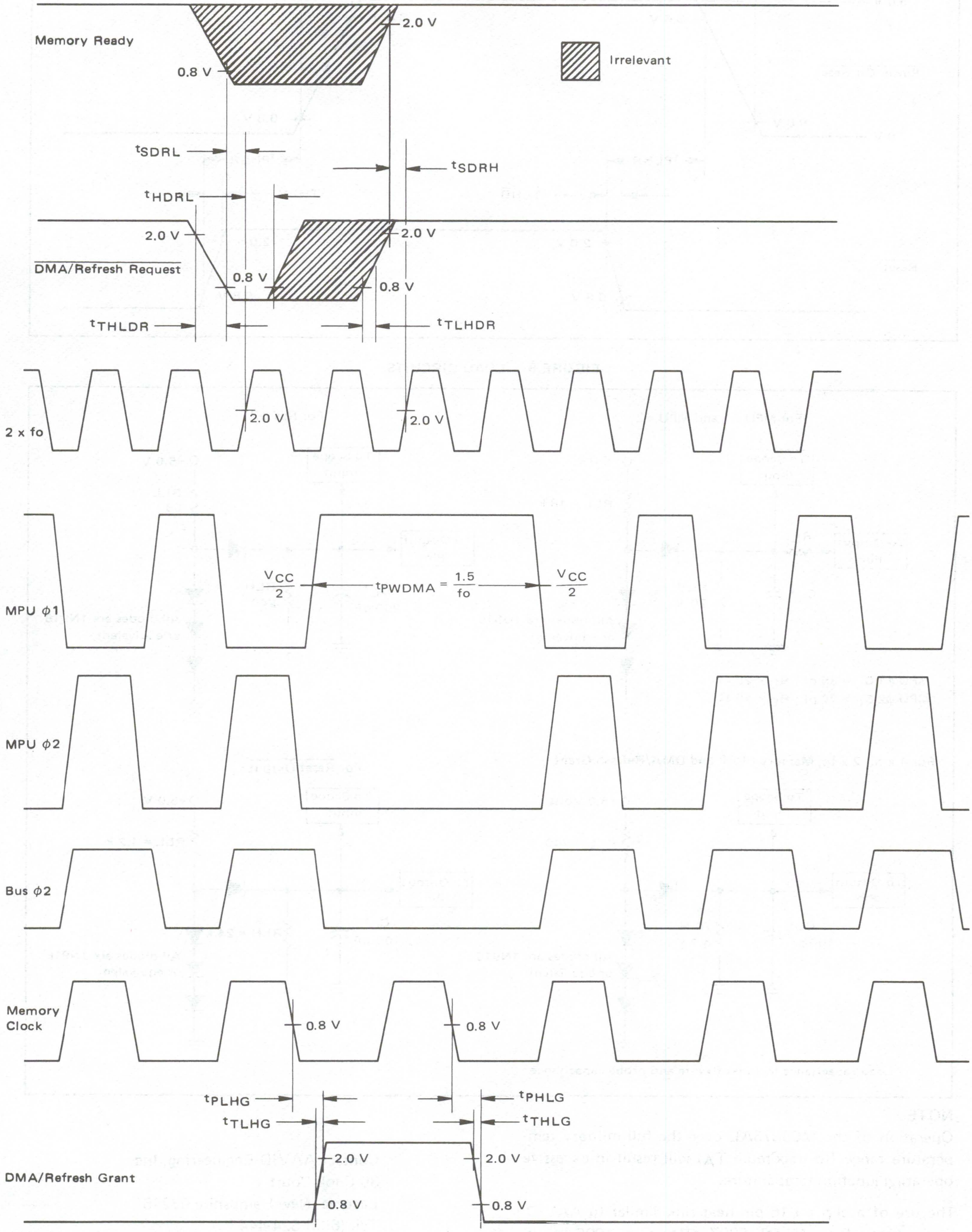

tTHLMR
tTLHMR
2.0 V
2.0 V
Memory Ready
0.8 V
0.8 V
2.0 V
DMA/Refresh Request
0.8 V
Irrelevant
tHMRL
tSMRL
tSMRH
2 x fo
0.8 V
0.8 V
MPU φ1
MPU φ2
VCC/2
tPWMR = 1/fo
VCC/2
Bus φ2
Memory Clock
1.5 V
tPWMR = 1/fo
1.5 V
DMA/Refresh Grant
(Low)

FIGURE 6 – TIMING DIAGRAM FOR $\overline{\text{DMA/REFRESH REQUEST}}$ STRETCH OPERATION

(Minimum Stretch Shown)

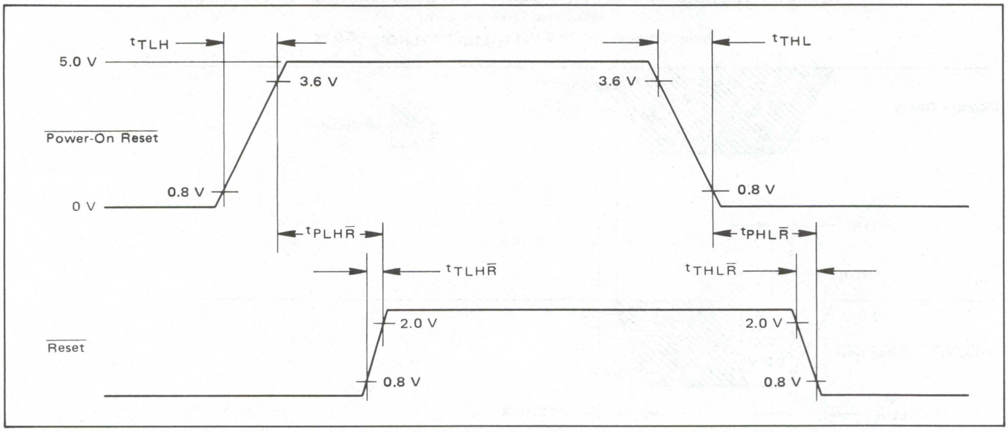
Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns



Memory Ready
2.0 V
0.8 V
Irrelevant
tSDRL
tSDRH
tHDRL
2.0 V
2.0 V
DMA/Refresh Request
0.8 V
0.8 V
tTHLDR
tTLHDR
2 x fo
2.0 V
2.0 V
MPU ϕ1
VCC/2
tPWDMA = 1.5/fo
VCC/2
MPU ϕ2
Bus ϕ2
Memory Clock
0.8 V
0.8 V
tPLHG
tPHLG
tTLHG
tTHLG
DMA/Refresh Grant
2.0 V
2.0 V
0.8 V
0.8 V

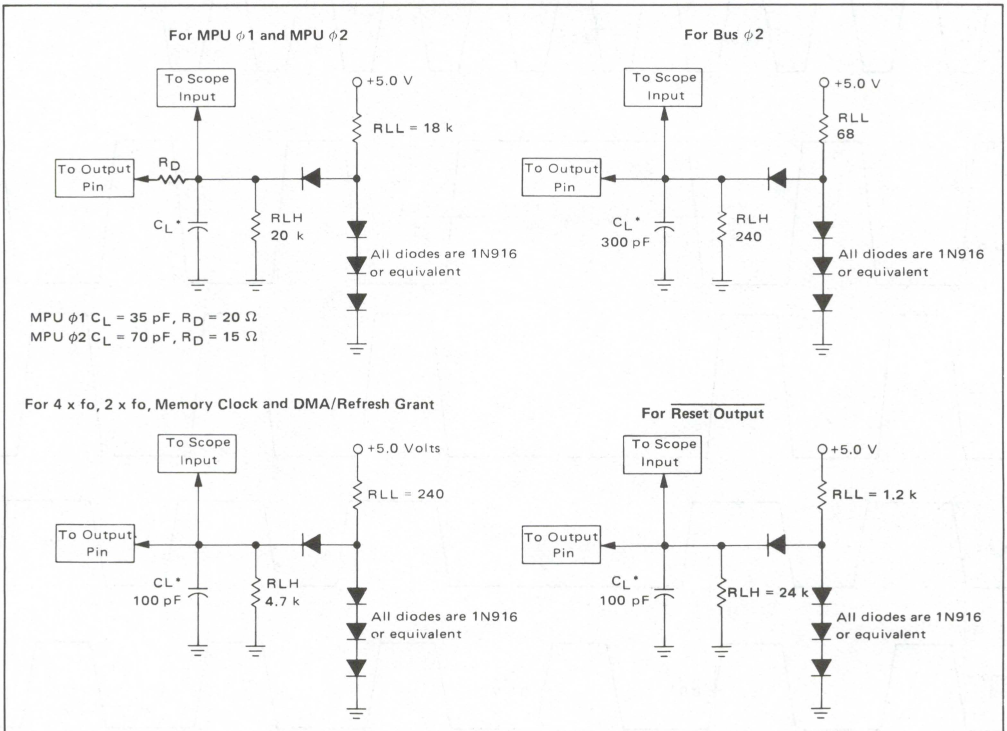
FIGURE 7 – POWER ON RESET

Input Voltage: 0 to 5.0 V, f = 100 kHz – Pulse Width = 1.0 μs, $t_{TLH} = t_{THL}$ = 25 ns



t_{TLH}
t_{THL}
5.0 V
3.6 V
3.6 V
Power-On Reset
0.8 V
0 V
0.8 V
$t_{PLH\overline{R}}$
$t_{PHL\overline{R}}$
$t_{TLH\overline{R}}$
$t_{THL\overline{R}}$
2.0 V
2.0 V
Reset
0.8 V
0.8 V

FIGURE 8 – LOAD CIRCUITS



For MPU φ1 and MPU φ2
To Scope Input
+5.0 V
RLL = 18 k
To Output Pin
RD
CL*
RLH 20 k
All diodes are 1N916 or equivalent
MPU φ1 CL = 35 pF, RD = 20 Ω
MPU φ2 CL = 70 pF, RD = 15 Ω
For Bus φ2
To Scope Input
+5.0 V
RLL 68
To Output Pin
CL* 300 pF
RLH 240
All diodes are 1N916 or equivalent
For 4 x fo, 2 x fo, Memory Clock and DMA/Refresh Grant
To Scope Input
+5.0 Volts
RLL = 240
To Output Pin
CL* 100 pF
RLH 4.7 k
All diodes are 1N916 or equivalent
For Reset Output
To Scope Input
+5.0 V
RLL = 1.2 k
To Output Pin
CL* 100 pF
RLH = 24 k
All diodes are 1N916 or equivalent

*Load capacitance includes fixture and probe capacitance

NOTE:

Operation of the MC6875AL over the full military temperature range (to maximum T_A) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A \approx 95°C$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

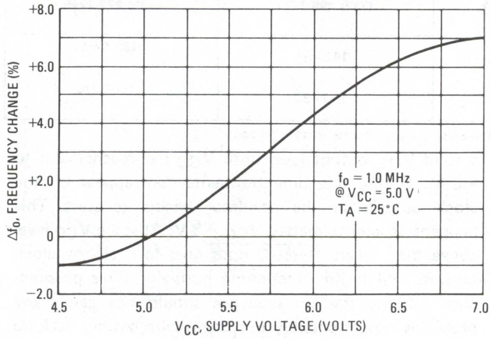


FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

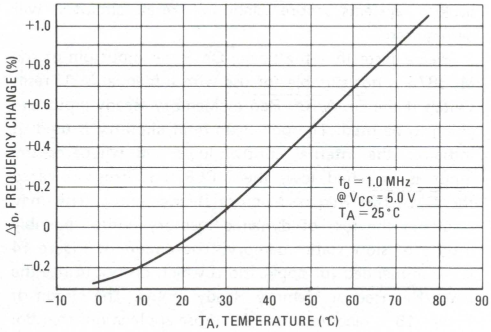
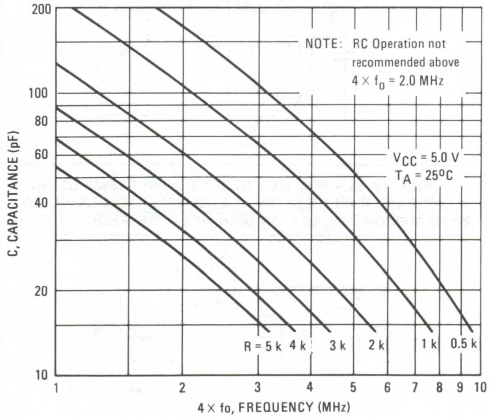


FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The V_{CC} pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 μF capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

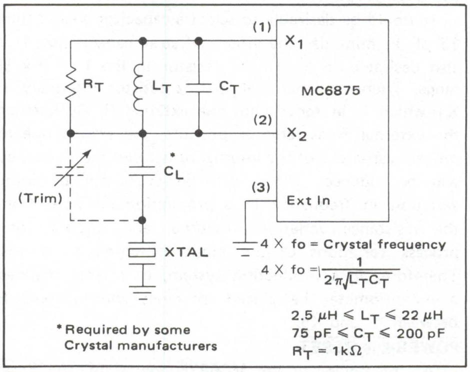
Unused inputs should be connected to V_{CC} or ground. $\overline{\text{Memory Ready}}$, DMA/Refresh Request and $\overline{\text{Power-On Reset}}$ should be connected to V_{CC} when not used. The External Input should be connected to ground when not used.

OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals X_1 and X_2 as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1kΩ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance (C_L) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and V_{CC} supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION



$4 \times f_o$ = Crystal frequency

$$4 \times f_o = \frac{1}{2\pi\sqrt{L_T C_T}}$$

$2.5\ \mu H \leq L_T \leq 22\ \mu H$
$75\ pF \leq C_T \leq 200\ pF$
$R_T = 1 k\Omega$

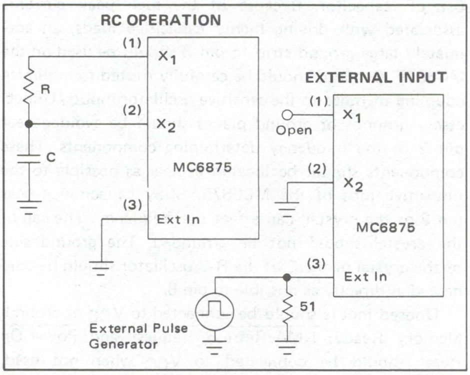
*Required by some Crystal manufacturers

TABLE 1 – OSCILLATOR COMPONENTS

TANK CIRCUIT PARAMETERS		APPROXIMATE CRYSTAL PARAMETERS				CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411	McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411	TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945
L_T µH	C_T pF	R_S Ohms	Co pF	C_1 mpF	fo MHz			
10	150	15-75	3-6	12	4.0	MP-04A * 390 pF	113-31	150-3260
4.7	82	8-45	4-7	23	8.0	MP-080 * 47 pF	113-32	150-3270

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for C_T and L_T, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency ($M\phi1$) is approximately:

Formula

$$4 \times f_o \approx \frac{320}{C\,(R+.27)+23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at X_1 which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between X_1 and X_2.

POWER-ON RESET

As the power to the MC6875 comes up, the $\overline{\text{Reset}}$ Output will be in a high impedance state and will not give a solid V_{OL} output level until V_{CC} has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately V_{CC} = 3 V. At some V_{CC} level above that, where $\overline{\text{Reset}}$ Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the $\overline{\text{Reset}}$ Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the $\overline{\text{Power-On Reset}}$ input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING $\overline{\text{DMA/REFRESH REQUEST}}$ OR MEMORY READY INPUTS

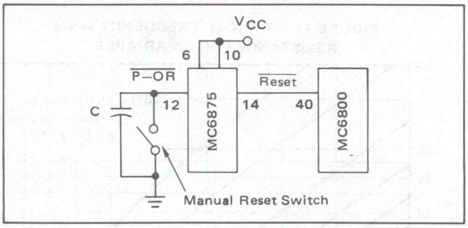
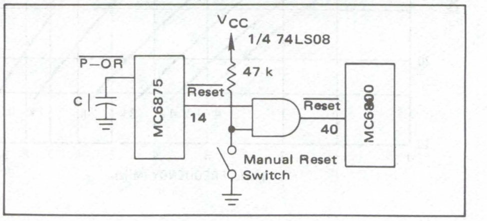


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR $\overline{\text{DMA/REFRESH REQUEST}}$ INPUTS



MOTOROLA

MC6890

Advance Information

MPU-BUS-COMPATIBLE 8-BIT D-TO-A CONVERTER

The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

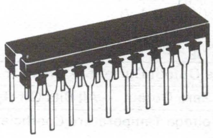
Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

A reset pin provides for overriding stored data and forcing I_{out} to zero.

- Direct Data Bus Link with All Popular TTL Level MPU's
- ±1/2 LSB Nonlinearity Over Temperature
- Fast Settling Time: 200 ns Typ
- Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Minimum $\overline{\text{Enable}}$ Pulse Width: 70 ns
- Fast $\overline{\text{Enable}}$: 10 ns Maximum Data Hold Time
- $\overline{\text{Reset}}$ Pin to Override Data
- Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts
- Low Power: 90 mW Typ
- +5 V and −5 V to −15 V Supplies

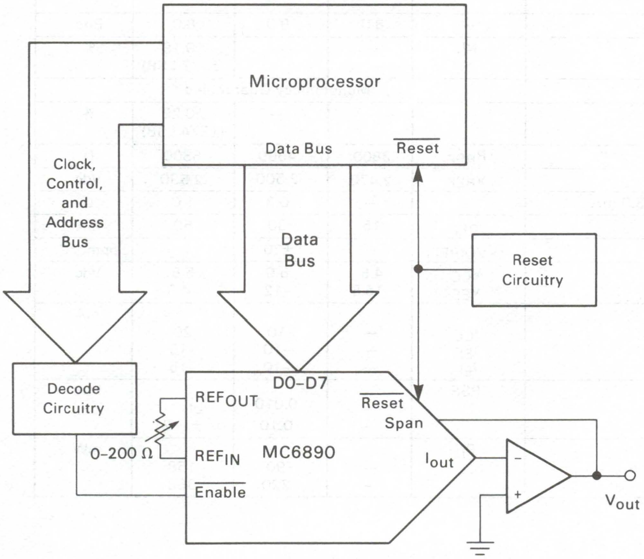
8-BIT MPU-BUS-COMPATIBLE DAC

SILICON MONOLITHIC INTEGRATED CIRCUIT

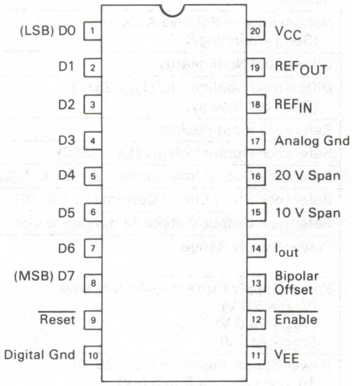


L SUFFIX
CASE 732-03

OPERATION WITH AN MPU


Microprocessor
Data Bus
Reset
Clock, Control, and Address Bus
Data Bus
Reset Circuitry
Decode Circuitry
D0–D7
REFOUT
Reset
Span
0–200 Ω
REFIN
MC6890
Iout
Enable
Vout

PIN CONNECTIONS


(LSB) D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
(MSB) D7 8
Reset 9
Digital Gnd 10
20 VCC
19 REFOUT
18 REFIN
17 Analog Gnd
16 20 V Span
15 10 V Span
14 Iout
13 Bipolar Offset
12 Enable
11 VEE

ORDERING INFORMATION

Device	Temperature Range	Package
MC6890L	0° to +70°C	Ceramic DIP
MC6890AL	−55° to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −18	Vdc
Digital Input Voltage, Pins 1-8, 12 Pin 9	V_{in}	−3.0 to +7.0 0 to +7.0	Vdc
Applied Output Voltage	V_{14}	V_{EE} +2.0 to V_{EE} +24	Vdc
Reference Amplifier Input	V_{18}	±7.5	Vdc
Operating Temperature Range MC6890L, MC6890AL	T_A	 0 to +70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −12 V, Pin 18 loaded only by Pin 19 through 100 Ω. Reset high, T_A = T_{low} to T_{high}[1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Logic Levels					Vdc
High Level, Logic 1	V_{IH}	2.0	—	—	
Low Level, Logic 0	V_{IL}	—	—	0.8	
Digital Input Current					
Data (V_{IH} = 3.0 V)	I_{IH}	—	0.001	1.0	μA
(V_{IL} = 0.4 V)	I_{IL}	—	0.5	−10	μA
Enable (V_{IH} = 3.0 V)	I_{IH}	—	0.001	1.0	μA
(V_{IL} = 0.4 V)	I_{IL}	—	−6.5	−100	μA
Reset (V_{IH} = V_{CC})	I_{IH}	—	0.001	1.0	μA
(V_{IL} = 0.4 V)	I_{IL}	—	−1.0	−15	μA
Full Scale Output Current — Unipolar	I_O	−1.50	−1.992	−2.50	mA
Unipolar Zero Output — All Bits Off (T_A = 25°C)	—	—	0.010	0.20	μA
Output Voltage Temperature Coefficient	TC_{VO}				ppm of FSR/°C
Unipolar Zero		—	±1.0	±2.0	
Bipolar Zero		—	±5.0	±15	
Full Scale Range		—	±20	±50	
Output Voltage, Full Scale Range (See Figure 3) (T_A = 25°C)	V_O				Vdc
(10 V Span)		9.861	9.961	10.061	
(20 V Span)		19.722	19.922	20.122	
(5.0 V Span)		4.930	4.980	5.030	
Output Voltage, Bipolar Zero (MSB on) (See Figure 4) (T_A = 25°C)	V_O				mV
(10 V Span)		—	0	±20	
(20 V Span)		—	0	±40	
(5.0 V Span)		—	0	±10	
DAC Output Resistance — Exclusive of Span Resistors (T_A = 25°C) (See Figure 5)	R_O	1.0	5.0	—	MΩ
Resolution	—	8.0	8.0	8.0	Bits
Nonlinearity — Relative Accuracy (See Terminology)	NL	—	—	±0.19 (±1/2 LSB)	%
Differential Nonlinearity	Monotonicity Guaranteed				
Differential Nonlinearity (T_A = 25°C) (See Terminology)	—	—	—	±0.29 (±3/4 LSB)	%
Reference Input Resistor	R_{REF}	3800	4900	6800	Ω
Reference Output Voltage (T_A = 25°C)	V_{REF}	2.470	2.500	2.530	Vdc
Reference Output Impedance (T_A = 25°C) I_{load} = 0–3.0 mA	—	—	0.3	1.0	Ω
Reference Short Circuit Current (T_A = 25°C)	I_{REF}	15	30	50	mA
Reference Output Voltage Temperature Coefficient	$TC_{VO(REF)}$	—	±20	—	ppm/°C
Power Supply Range	V_{CC} V_{EE}	4.5 −16.5	5.0 −12	5.5 −4.5	Vdc
Power Supply Current — All Bits Low					mA
(V_{CC} = 5.0 V)	I_{CC}	—	10	20	
(V_{EE} = −5.0 V)	I_{EE}	—	−10	−15	
(V_{EE} = −15 V)	I_{EE}	—	−10	−15	
Power Supply Rejection (T_A = 25°C)	PSR				LSB
To V_{CC} (V_{CC} = 4.5 to 5.5 V)		—	0.010	±1/10	
To V_{EE} (V_{EE} = −4.5 V to −16.5 V)		—	0.10	±1/2	
Power Dissipation — All Bits Low	P_D				mW
For V_{CC} = 4.5 V, V_{EE} = −4.5 V		—	90	158	
For V_{CC} = 5.5 V, V_{EE} = −16.5 V		—	220	358	

NOTE 1: T_{low} = −55°C for MC6890A, 0° for MC6890
T_{high} = +125°C for MC6890A, +70°C for MC6890

AC SPECIFICATIONS (V_{CC} = 5.0 V, V_{EE} = −12 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Settling Time (Enable Positive Edge to ±1/2 LSB Output)	t_s	—	200	300*	ns
Data Setup Time	$t_{su(D)}$	70	40	—	ns
Data Hold Time	$t_{h(D)}$	10	0	—	ns
Pulse Widths $\overline{\text{Enable}}$ $\overline{\text{Reset}}$	 $t_{W(\overline{E})}$ $t_{W(\overline{R})}$	 70 100*	 20 —	 — —	ns
Propagation Delays $\overline{\text{Enable}}$, Low to High Reset, High to Low ($I_O < 1.0\ \mu A$)	 $t_{PLH(\overline{E})}$ $t_{PHL(\overline{R})}$	 — —	 100 250	 — —	ns

*Not 100% tested , guaranteed by design

FIGURE 1 — TIMING DIAGRAM

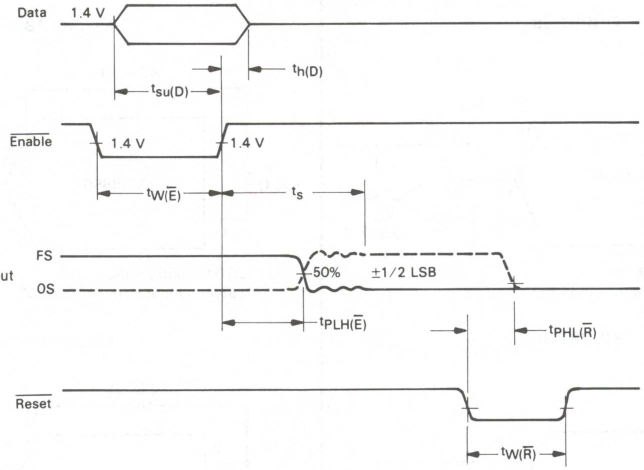
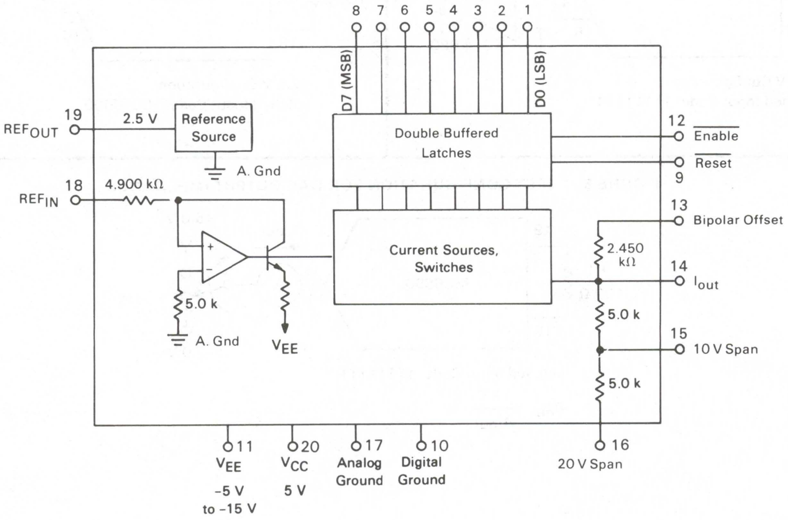

Data
1.4 V
$t_{h(D)}$
$t_{su(D)}$
$\overline{\text{Enable}}$
1.4 V
1.4 V
$t_{W(\overline{E})}$
t_s
FS
I_{out}
OS
50%
±1/2 LSB
$t_{PLH(\overline{E})}$
$t_{PHL(\overline{R})}$
$\overline{\text{Reset}}$
$t_{W(\overline{R})}$

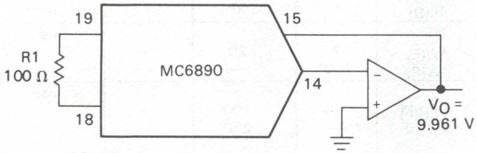
FIGURE 2 — BLOCK DIAGRAM


8 7 6 5 4 3 2 1
D7 (MSB)
D0 (LSB)
19
REF_{OUT}
2.5 V
Reference Source
A. Gnd
18
REF_{IN}
4.900 kΩ
Double Buffered Latches
12
$\overline{\text{Enable}}$
$\overline{\text{Reset}}$
9
13
Bipolar Offset
Current Sources, Switches
2.450 kΩ
14
I_{out}
5.0 k
15
10 V Span
5.0 k
5.0 k
A. Gnd
V_{EE}
11
V_{EE}
−5 V to −15 V
20
V_{CC}
5 V
17
Analog Ground
10
Digital Ground
16
20 V Span

TEST FIGURES

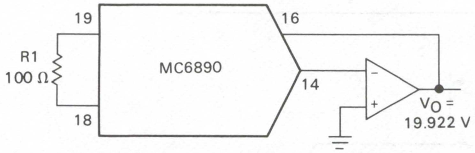
UNIPOLAR CONFIGURATIONS

FIGURE 3A


19
15
R1
100 Ω
MC6890
14
18
−
+
VO =
9.961 V

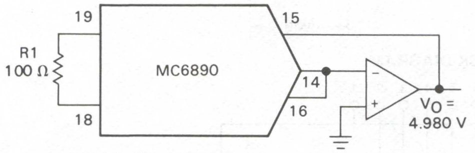
+10 V Configuration
Latched Input Code: 11111111

FIGURE 3B


19
16
R1
100 Ω
MC6890
14
18
−
+
VO =
19.922 V

+20 V Configuration
Latched Input Code: 11111111

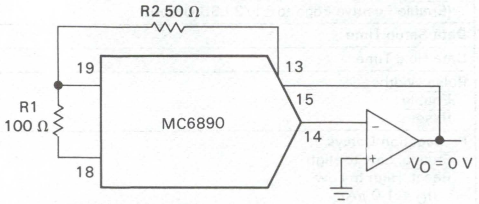
FIGURE 3C


19
15
R1
100 Ω
MC6890
14
16
18
−
+
VO =
4.980 V

+5.0 V Configuration
Latched Input Code: 11111111

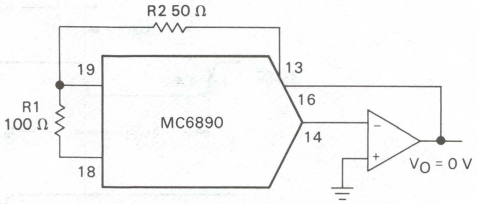
BIPOLAR CONFIGURATIONS

FIGURE 4A


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
18
−
+
VO = 0 V

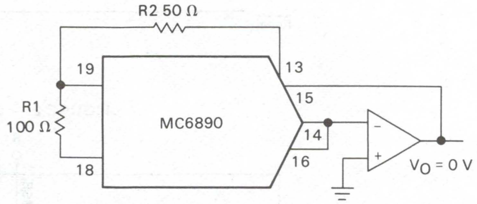
±5.0 V Configuration
Latched Input Code: 10000000

FIGURE 4B


R2 50 Ω
19
13
16
R1
100 Ω
MC6890
14
18
−
+
VO = 0 V

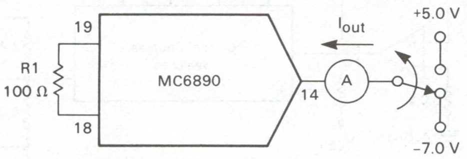
±10 V Configuration
Latched Input Code: 10000000

FIGURE 4C


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
16
18
−
+
VO = 0 V

±2.5 V Configuration
Latched Input Code: 10000000

FIGURE 5 TEST CONFIGURATION FOR DAC OUTPUT IMPEDANCE


19
R1
100 Ω
MC6890
18
14
Iout
A
+5.0 V
−7.0 V

Latched Input Code: 11111111

$$R_{out} = \frac{12\ V}{\Delta I_{out}}$$

TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to non-monotonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases. The MC6890 is guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the $\overline{\text{Enable}}$ positive transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are latched "on," which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the current output to settle to within ±1/2 LSB for 8 bit accuracy. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{255}{256} \times 10$ V = 9.961 V.

Gain error is laser trimmed to less than ±1.0% with R1 = 100 Ω (Figure 3) and can be user trimmed to zero error with R1 = 200 Ω pot.

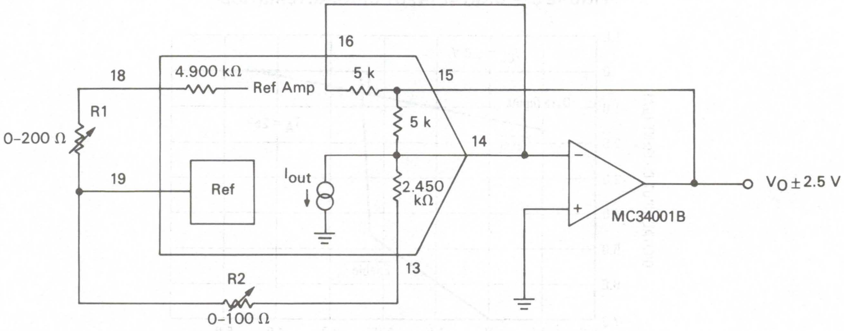
Bipolar Zero — Using the configuration shown in Figure 6 with R1 = 100 Ω, R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to analog ground is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled. Bipolar Zero error is laser trimmed to less than 0.20% and can be user trimmed to zero with R2 = 100 Ω pot.

Temperature Coefficients — (Unipolar zero, Bipolar zero, Gain and Reference Output). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

Power Supply Rejection — The change in full scale current caused by the specified change in V_{EE} or V_{CC} is expressed in LSB's.

$\overline{\text{Reset}}$ Function — The MC6890 has a $\overline{\text{Reset}}$ pin (9) that will force the DAC's registers, and therefore the DAC output current, to zero. This input is active low and should not occur simultaneously with an active $\overline{\text{Enable}}$ signal although no harm would result to the converter. The power dissipation increases slightly during $\overline{\text{Reset}}$ low. $\overline{\text{Reset}}$ should not be allowed to become more negative than ground.

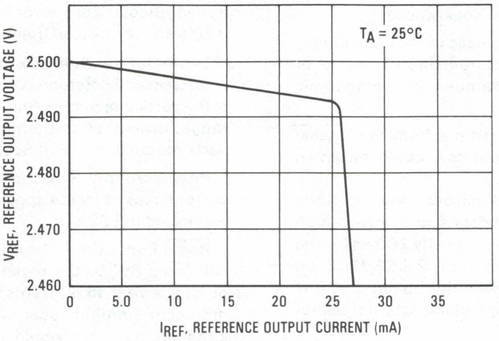
FIGURE 6 — MC6890 IN TYPICAL BIPOLAR ±2.5 V OPERATION



D7	D6	D5	D4	D3	D2	D1	D0	VO (Volts)	
								R2 ≅ 60 Ω	R2 ≅ 50 Ω
1	1	1	1	1	1	1	1	+2.490	+2.480
1	1	1	1	1	1	1	0	+2.470	+2.460
1	0	0	0	0	0	0	0	+0.010	+0.000
0	1	1	1	1	1	1	1	−0.010	−0.020
0	0	0	0	0	0	0	1	−2.470	−2.480
0	0	0	0	0	0	0	0	−2.490	−2.500

TYPICAL PERFORMANCE CURVES

FIGURE 7 — REFERENCE VOLTAGE versus EXTERNAL LOAD CURRENT*



*External load current is in addition to Reference Input Current (Pin 18) of D/A converter.

FIGURE 8 — DIGITAL INPUT CHARACTERISTICS

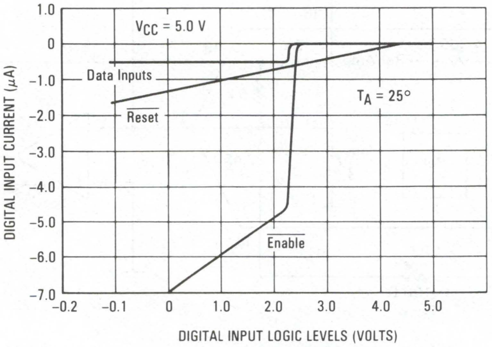
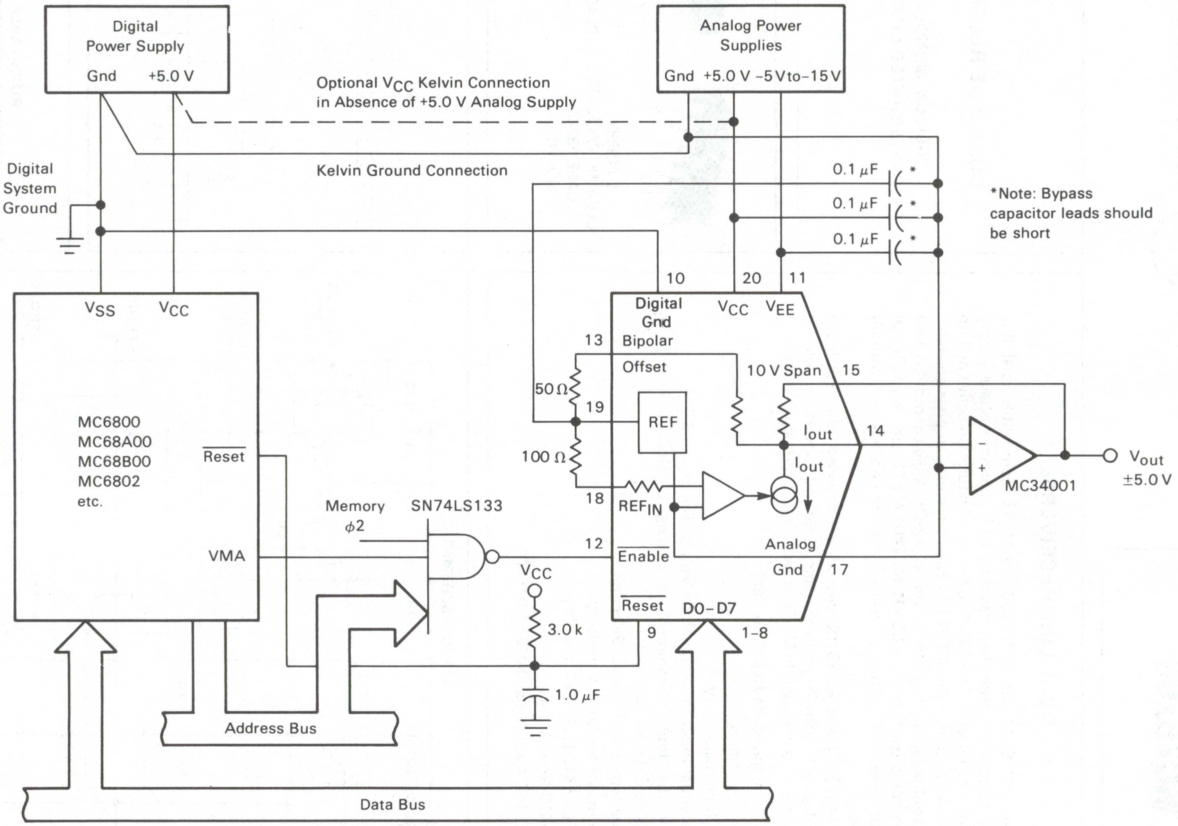


FIGURE 9 — TYPICAL APPLICATION OF THE MC6890 IN A MC6800 SERIES MPU SYSTEM



Digital Power Supply
Gnd
+5.0 V
Analog Power Supplies
Gnd
+5.0 V
-5 V to -15 V
Optional V_{CC} Kelvin Connection in Absence of +5.0 V Analog Supply
Kelvin Ground Connection
Digital System Ground
0.1 µF *
0.1 µF *
0.1 µF *
10
20
11
V_{SS}
V_{CC}
Digital Gnd
V_{CC}
V_{EE}
13
Bipolar Offset
50 Ω
19
REF
10 V Span
15
I_{out}
14
100 Ω
I_{out}
18
REF_{IN}
MC34001
V_{out} ±5.0 V
MC6800
MC68A00
MC68B00
MC6802
etc.
$\overline{Reset}$
VMA
Memory
$\phi2$
SN74LS133
12
$\overline{Enable}$
Analog Gnd
17
V_{CC}
3.0 k
$\overline{Reset}$
D0–D7
9
1–8
1.0 µF
Address Bus
Data Bus

*Note: Bypass capacitor leads should be short

MC75107
MC75108

MOTOROLA

DUAL LINE RECEIVERS

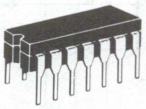
The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

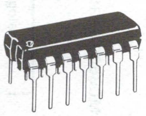
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

DUAL LINE RECEIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

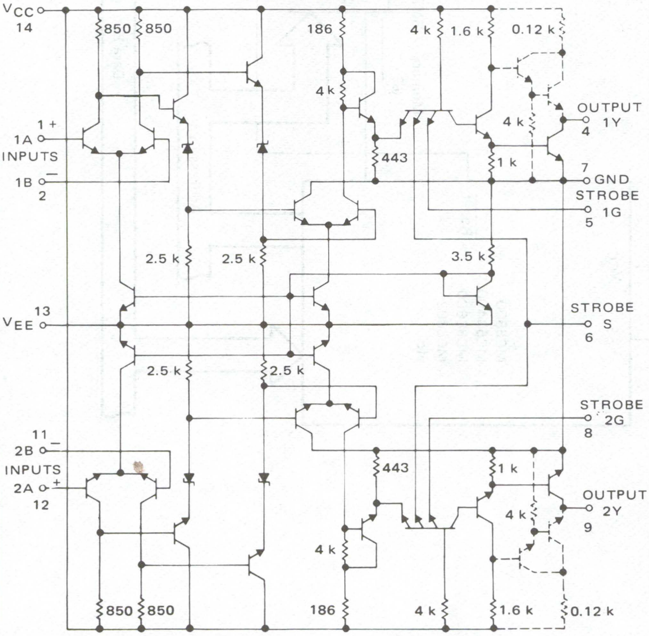


L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

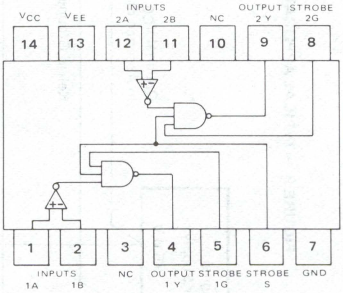


P SUFFIX
PLASTIC PACKAGE
CASE 646-05

CIRCUIT SCHEMATIC


VCC 14
850
850
186
4 k
1.6 k
0.12 k
4 k
OUTPUT 1Y 4
1 +
1A
INPUTS
1B −
2
4 k
443
1 k
7 GND
STROBE 1G 5
2.5 k
2.5 k
3.5 k
13
VEE
STROBE S 6
2.5 k
2.5 k
STROBE 2G 8
11 −
2B
INPUTS
2A +
12
443
1 k
4 k
OUTPUT 2Y 9
4 k
850
850
186
4 k
1.6 k
0.12 k

Components shown with dashed lines are applicable to the MC75107 only.


VCC
VEE
INPUTS 2A 2B
NC
OUTPUT 2Y
STROBE 2G
14
13
12
11
10
9
8
+
−
+
−
1
2
3
4
5
6
7
INPUTS 1A 1B
NC
OUTPUT 1Y
STROBE 1G
STROBE S
GND

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

MAXIMUM RATINGS (T_A = 0°C to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Plastic and Ceramic Dual-In-Line Packages Derate above T_A = +25°C		625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}	–	–	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5.0	–	+3.0	Vdc
Operating Temperature Range	T_A	0	–	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5.0†	-0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IH}	2	–	30	75	μA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = -2.0 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IL}	2	–	–	-10	μA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 40 1.0	 μA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	 – –	 – –	 80 2.0	 μA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-3.2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = –400 μA, V_{IC} = -3.0 V to +3.0 V)‡	V_{OH}	3	–	–	–	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = -3.0 V to +3.0 V)‡	V_{OL}	3	–	–	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max)‡	I_{CEX}	3	–	–	250	μA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max)‡	I_{OSC}	5	–	–	–	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) ‡	I_{CCH+}	6	–	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C)‡	I_{CCH-}	6	0	8.4	-15	mA

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.

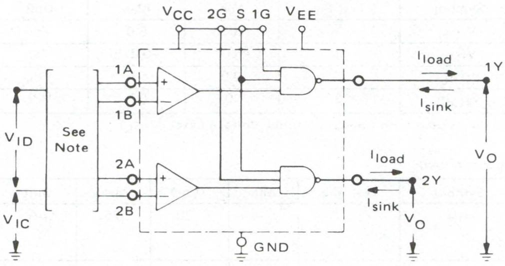
#Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(D)}$	7	 – –	 – 19	 – 25	ns
Propagation Delay Time, high-to-low level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(D)}$	7	 – –	 – 19	 – 25	ns
Propagation Delay Time, low-to-high level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(S)}$	7	 – –	 – 13	 – 20	ns
Propagation Delay Time, high-to-low level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(S)}$	7	 – –	 – 13	 – 20	ns

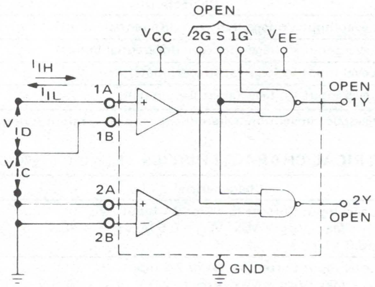
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}


VCC
2G
S
1G
VEE
1A
1B
2A
2B
1Y
2Y
Iload
Isink
VO
VID
VIC
See Note
GND

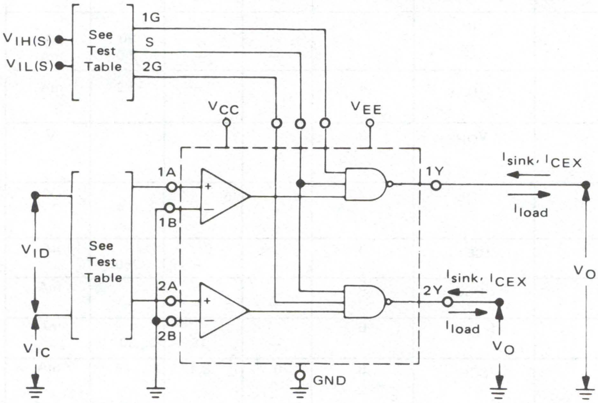
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}


OPEN
VCC
2G
S
1G
VEE
IIH
IIL
1A
1B
2A
2B
VID
VIC
OPEN
1Y
2Y
OPEN
GND

NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}


VIH(S)
VIL(S)
See Test Table
1G
S
2G
VCC
VEE
1A
1B
2A
2B
1Y
2Y
Isink, ICEX
Iload
VO
VID
VIC
See Test Table
GND

TEST TABLE

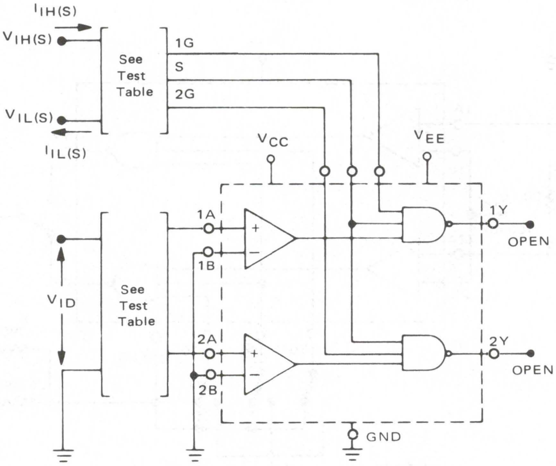
MC75107	MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES: 1. V_{IC} = −3.0 V to +3.0 V.

2. When testing one channel, the inputs of the other channel should be grounded.

TEST CIRCUITS (continued)

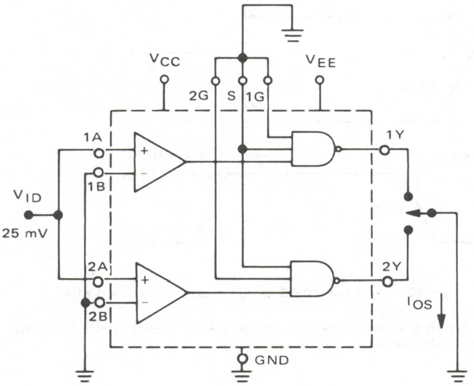
FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



$I_{IH(S)}$
$V_{IH(S)}$
$V_{IL(S)}$
$I_{IL(S)}$
See Test Table
1G
S
2G
V_{CC}
V_{EE}
1A
1B
1Y
OPEN
V_{ID}
See Test Table
2A
2B
2Y
OPEN
GND

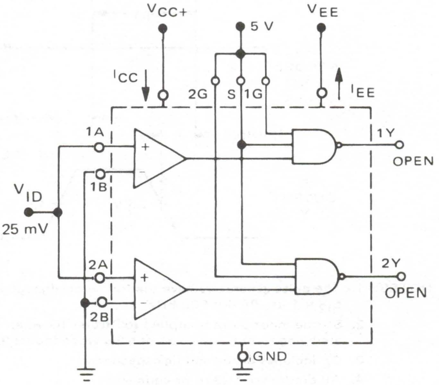
TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	−25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	−25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	−25 mV	−25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}



V_{CC}
V_{EE}
2G
S
1G
1A
1B
1Y
V_{ID}
25 mV
2A
2B
2Y
I_{OS}
GND

FIGURE 6 – I_{CC} and I_{EE}

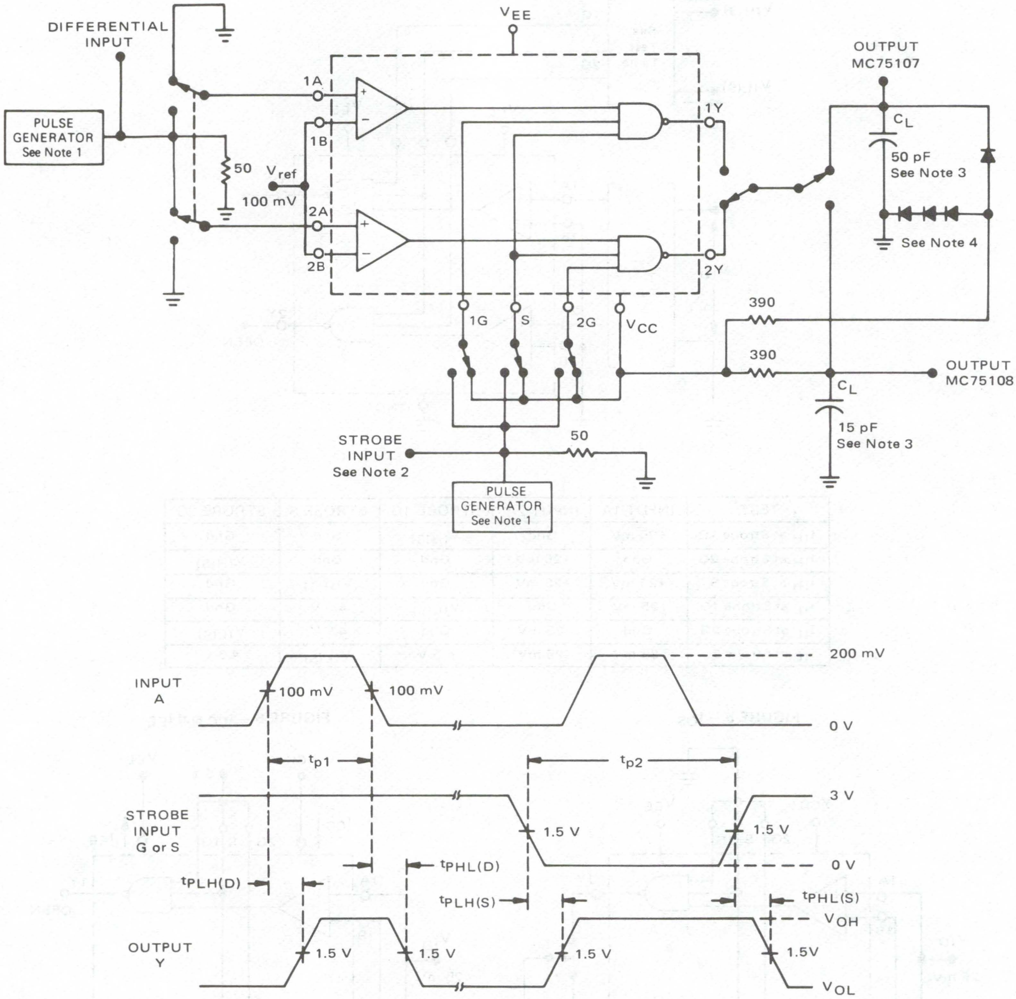


V_{CC+}
5 V
V_{EE}
I_{CC}
I_{EE}
2G
S
1G
1A
1B
1Y
OPEN
V_{ID}
25 mV
2A
2B
2Y
OPEN
GND

NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

TEST CIRCUITS (continued)

FIGURE 7 — PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS


DIFFERENTIAL INPUT
PULSE GENERATOR See Note 1
50
V_{ref}
100 mV
1A
1B
2A
2B
V_{EE}
1Y
2Y
1G
S
2G
V_{CC}
OUTPUT MC75107
C_L
50 pF See Note 3
See Note 4
390
390
OUTPUT MC75108
C_L
15 pF See Note 3
STROBE INPUT See Note 2
50
PULSE GENERATOR See Note 1
INPUT A
100 mV
100 mV
200 mV
0 V
t_{p1}
t_{p2}
STROBE INPUT G or S
3 V
1.5 V
1.5 V
0 V
$t_{PLH(D)}$
$t_{PHL(D)}$
$t_{PLH(S)}$
$t_{PHL(S)}$
OUTPUT Y
1.5 V
1.5 V
1.5 V
1.5V
V_{OH}
V_{OL}

NOTES:
1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1\ \mu s$, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

MOTOROLA

MC75125
MC75127

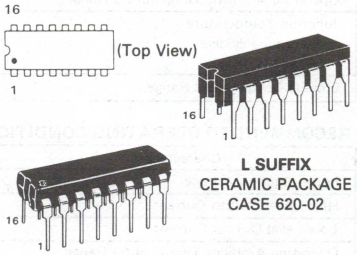
SEVEN CHANNEL LINE RECEIVERS

SEVEN CHANNEL LINE RECEIVERS

The MC75125 and MC75127 are seven-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The MC75125 and MC75127 are characterized for operation from 0 to 70°C.

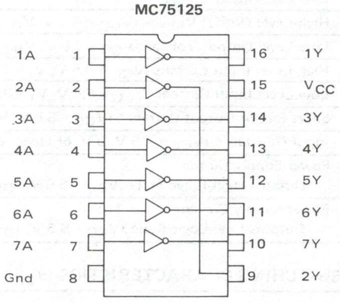
- Meets IBM 360/370 I/O Specification
- Input Resistance — 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed — Low Propagation Delay
- Ratio Specification — t_{PLH}/t_{PHL}
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on MC75127


16
(Top View)
1
16
1
16
1

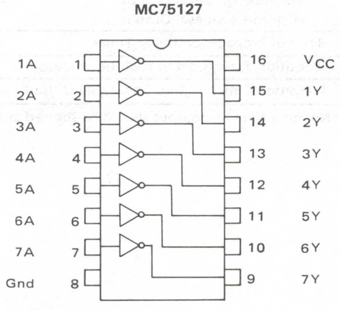
L SUFFIX
CERAMIC PACKAGE
CASE 620-02

P SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS

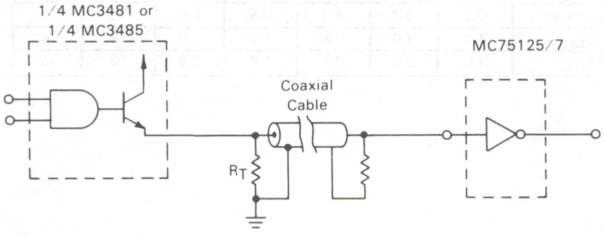

MC75125
1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 1Y
15 VCC
14 3Y
13 4Y
12 5Y
11 6Y
10 7Y
9 2Y

Logic: Y = $\overline{A}$


MC75127
1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 VCC
15 1Y
14 2Y
13 3Y
12 4Y
11 5Y
10 6Y
9 7Y

Logic: Y = $\overline{A}$

TYPICAL APPLICATIONS


1/4 MC3481 or
1/4 MC3485
Coaxial
Cable
MC75125/7
RT

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	−2.0 to +7.0	V
Power Dissipation (Package Limitation)			
Ceramic Package	P_D	1150	mW
Plastic Package		960	
Derate Above T_A = 25°C	$1/R_{\theta JA}$	7.7	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	−0.4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

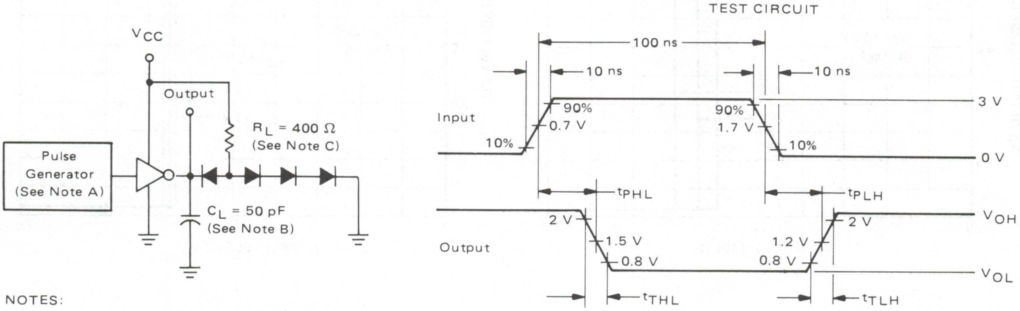
Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	1.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.7	V
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0.5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V)	I_{IH}	0.2	0.3	0.42	mA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V)	I_{IL}	–	–	−0.24	mA
Short Circuit Output Current* (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	−18	–	−60	mA
Input Resistance (V_{CC} = 4.5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_i	7.4	–	20	kΩ
Power Supply Current Outputs High-Logic State (V_{CC} = 5.5 V, I_{OH} = −0.4 mA, all inputs at 0.7 V)	I_{CCH}	–	15	25	mA
Power Supply Current Outputs Low-Logic State (V_{CC} = 5.5 V, I_{OL} = 16 mA, all inputs at 4.0 V)	I_{CCL}	–	28	47	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted. See Figure 1)

Characteristic	Symbol	MC75125			MC75127			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time								ns
Low-to-High-Level Output	t_{PLH}	7.0	14	25	7.0	14	25	
High-to-Low-Level Output	t_{PHL}	10	18	30	10	18	30	
Ratio of Propagation Delay Times	t_{PLH}/t_{PHL}	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION


VCC
Output
RL = 400 Ω
(See Note C)
Pulse
Generator
(See Note A)
CL = 50 pF
(See Note B)
100 ns
10 ns
10 ns
Input
90%
0.7 V
10%
90%
1.7 V
10%
3 V
0 V
tPHL
tPLH
Output
2 V
1.5 V
0.8 V
1.2 V
0.8 V
2 V
VOH
VOL
tTHL
tTLH

TEST CIRCUIT

VOLTAGE WAVEFORMS

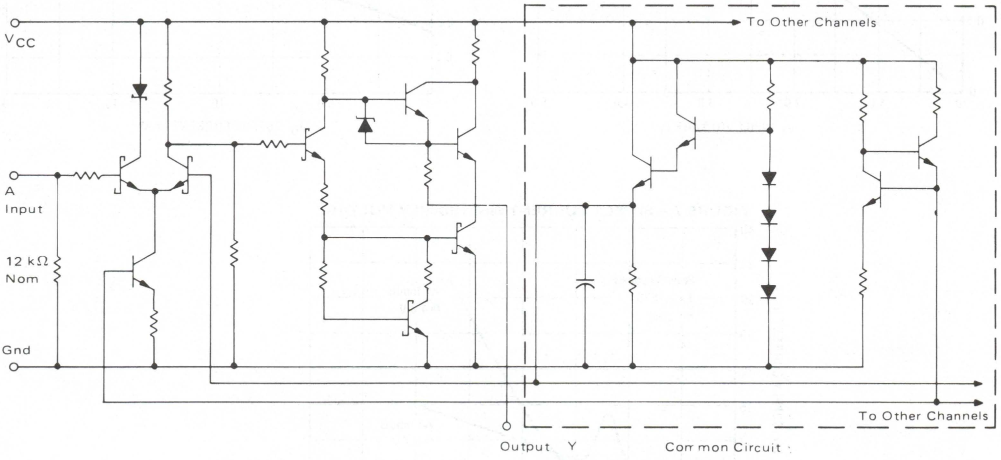
NOTES:

A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.

B. C_L includes probe and jig capacitance.

C. All diodes are MMD7000 or equivalent.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)


VCC
To Other Channels
A
Input
12 kΩ
Nom
Gnd
To Other Channels
Output Y
Common Circuit

TYPICAL CHARACTERISTICS

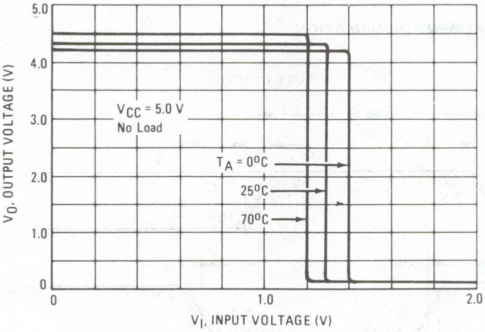


FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

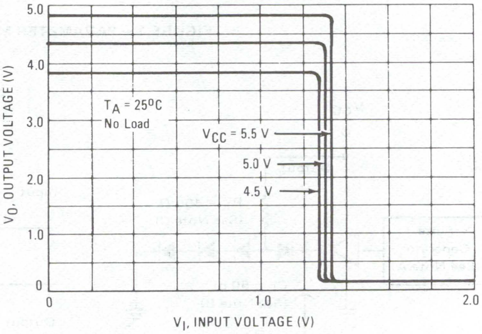


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

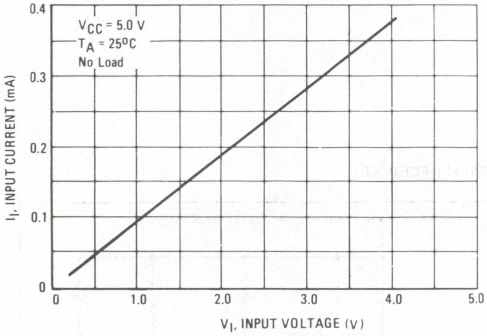


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

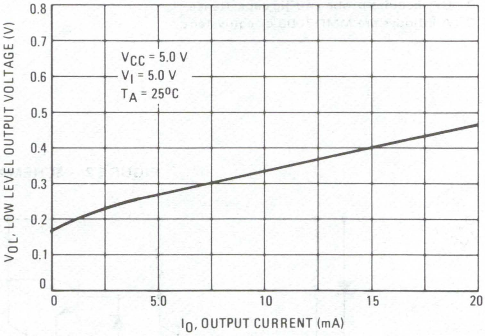


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

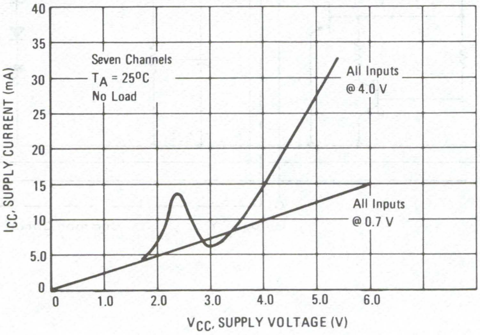


FIGURE 7 — SUPPLY CURRENT versus SUPPLY VOLTAGE

MOTOROLA

MC75128
MC75129

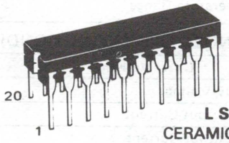
EIGHT-CHANNEL LINE RECEIVERS

EIGHT-CHANNEL LINE RECEIVERS

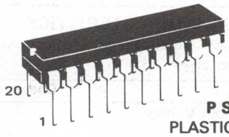
The MC75128 and MC75129 are eight-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The MC75128 has an active-high strobe; the MC75129 has an active-low strobe.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. Both devices are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance – 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed – Low Propagation Delay
- Ratio Specification – t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- MC75128 Strobe – Active-High
  MC75129 Strobe – Active-Low



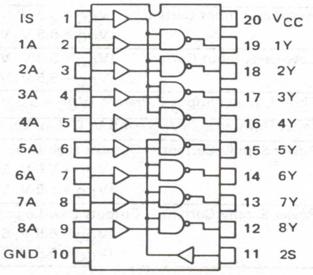
L SUFFIX
CERAMIC PACKAGE
CASE 732-03



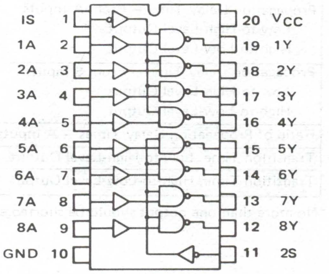
P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN CONNECTIONS

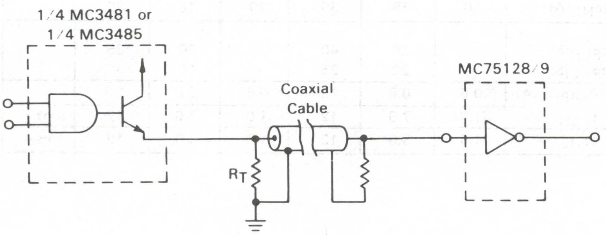
MC75128


IS 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
GND 10
20 VCC
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

MC75129


IS 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
GND 10
20 VCC
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

TYPICAL APPLICATION


1/4 MC3481 or
1/4 MC3485
Coaxial
Cable
RT
MC75128/9

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
A Input Voltage	V_{IA}	−0.15 to +7.0	V
Strobe Input Voltage	V_{IS}	+7.0	V
Power Dissipation (Package Limitation) Ceramic Package Plastic Package Derate Above T_A = 25°C	 P_D $1/R_{\theta JA}$	 1150 960 −7.7	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
High Level Output Current	I_{OH}	–	–	−0.4	mA
Low Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage A Inputs S Inputs	V_{IH}	 1.7 2.0	 – –	 – –	V
Low-Level Input Voltage A Inputs S Inputs	V_{IL}	 – –	 – –	 0.7 0.7	V
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA)	V_{OH}	2.4	3.1	–	V
Low-Level Output Voltage (V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA)	V_{OL}	–	0.4	0.5	V
Input Clamp Voltage (V_{CC} = 4.5 V, I_I = −18 mA, S Inputs)	V_{IK}	–	–	−1.5	V
High-Level Input Current (V_{CC} = 5.5 V, V_I = 3.11 V, A Inputs) (V_{CC} = 5.5 V, V_I = 2.7 V, S Inputs)	I_{IH}	– –	0.3 –	0.42 20	mA µA
Low-Level Input Current (V_{CC} = 5.5 V, V_I = 0.15 V, A Inputs) (V_{CC} = 5.5 V, V_I = 0.4 V, S Inputs)	I_{IL}	– –	– –	−0.24 −0.4	mA
Short Circuit Output Current * (V_{CC} = 5.5 V, V_O = 0)	I_{OS}	−18	–	−60	mA
Input Resistance (V_{CC} = 4.5 V, 0 V, or Open, ΔV_I = 0.15 V to 4.15 V)	r_i	7.0	–	20	kΩ
Power Supply Current – Outputs High-Logic State, all inputs at 0.7 V (V_{CC} = 5.5 V, Strobe at 2.4 V – MC75128) (V_{CC} = 5.5 V, Strobe at 0.4 V – MC75129)	I_{CCH}	 – –	 19 19	 31 31	mA
Power Supply Current – Outputs Low-Logic State, all inputs at 4.0 V (V_{CC} = 5.5 V, Strobe at 2.4 V – MC75128) (V_{CC} = 5.5 V, Strobe at 0.4 V – MC75129)	I_{CCL}	 – –	 32 32	 53 53	mA

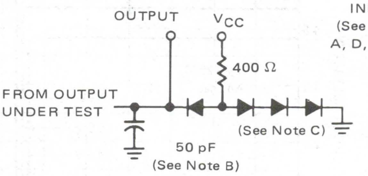
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, R_L = 400 Ω, C_L = 50 pF, unless otherwise noted, See Figures 1 and 2)

Characteristic	Symbol	MC75128			MC75129			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time – From A Inputs Low-to-High-Level Output High-to-Low-Level Output	 $t_{PLH}(A)$ $t_{PHL}(A)$	 7.0 10	 14 18	 25 30	 7.0 10	 14 18	 25 30	ns
Propagation Delay Time – From S Inputs Low-to-High-Level Output High-to-Low-Level Output	 $t_{PLH}(S)$ $t_{PHL}(S)$	 – –	 26 22	 40 35	 – –	 20 16	 35 30	ns
Ratio of Propagation Delay Times – A Inputs	$t_{PLH}(A)/t_{PHL}(A)$	0.5	0.8	1.3	0.5	0.8	1.3	
Transition Time, Low-to-High-Level Output	t_{TLH}	1.0	7.0	12	1.0	7.0	12	ns
Transition Time, High-to-Low-Level Output	t_{THL}	1.0	3.0	12	1.0	3.0	12	ns

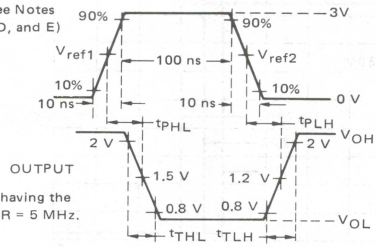
*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

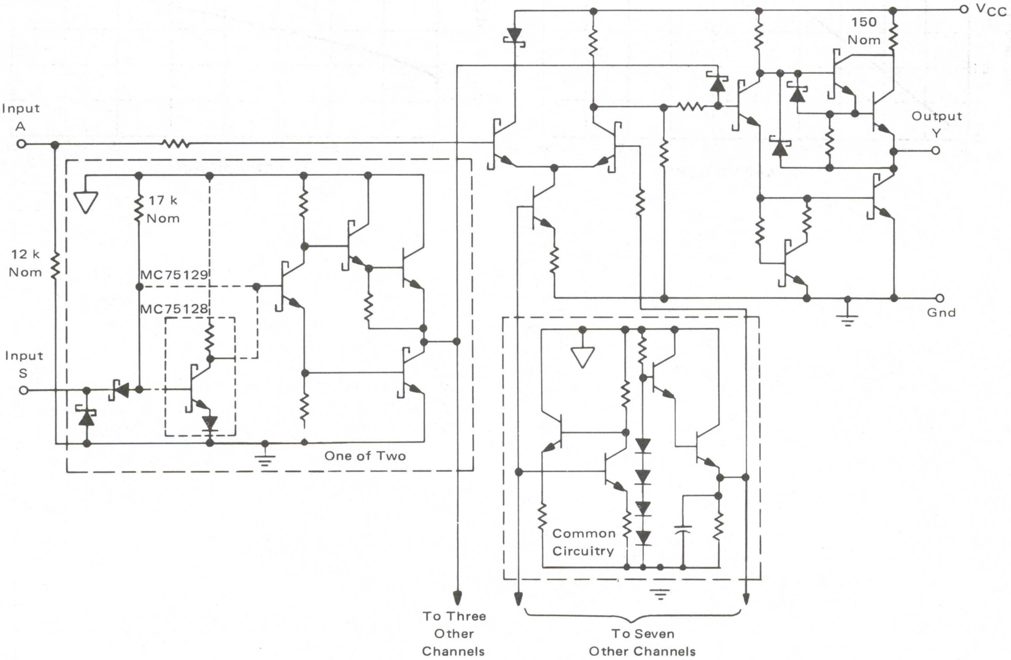

OUTPUT
V_{CC}
400 Ω
FROM OUTPUT UNDER TEST
(See Note C)
50 pF
(See Note B)

VOLTAGE WAVEFORMS


INPUT
(See Notes
A, D, and E)
90%
90%
3V
V_{ref1}
100 ns
V_{ref2}
10%
10%
0 V
10 ns
10 ns
t_{PHL}
t_{PLH}
V_{OH}
2 V
2 V
OUTPUT
1.5 V
1.2 V
0.8 V
0.8 V
V_{OL}
t_{THL}
t_{TLH}

NOTES:
- A. Input pulses are supplied by a generator having the following characteristics: $Z_o = 50\ \Omega$, PRR = 5 MHz.
- B. Includes probe and jig capacitance.
- C. All diodes are MMD7000 or equivalent.
- D. The strobe inputs of MC75129 are in-phase with the output.
- E. $V_{ref1} = 0.7$ V and $V_{ref2} = 1.7$ V for testing data (A) Inputs, $V_{ref1} = V_{ref2} = 1.3$ V for strobe inputs.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)


V_{CC}
150
Nom
Input
A
Output
Y
12 k
Nom
17 k
Nom
MC75129
MC75128
Input
S
One of Two
Gnd
Common
Circuitry
To Three
Other
Channels
To Seven
Other Channels

TYPICAL CHARACTERISTICS

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

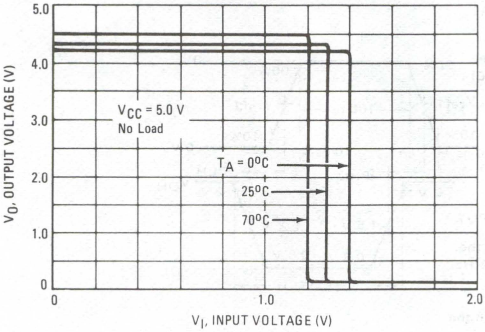


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

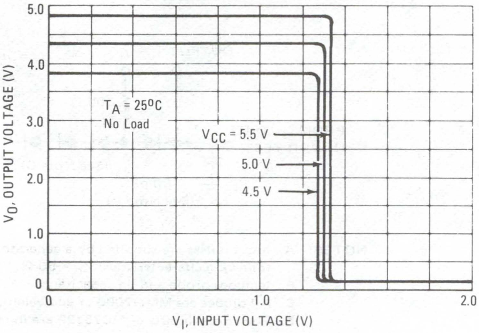


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

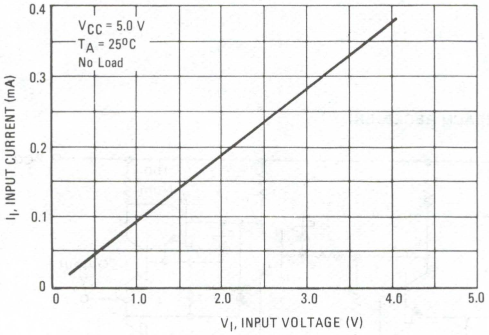
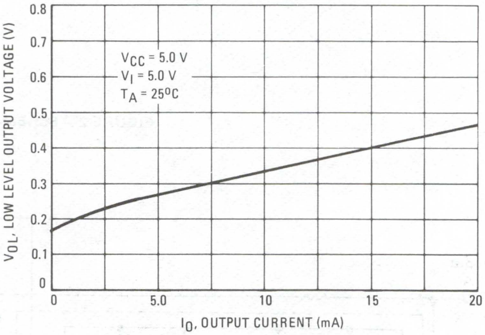


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT



MOTOROLA

SN75172
SN75174

Product Preview

QUAD LINE DRIVERS WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola SN75172/174 are monolithic quad differential line drivers with three-state outputs. They are designed specifically to meet the requirements of EIA standards RS-485, RS-422A, and CCITT recommendations V.11 and X.27.

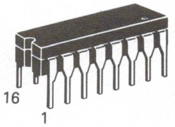
The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172/174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. These devices offer optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

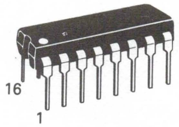
- Meets RS-485 Standard for Party-Line Operation
- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range . . . −7.0 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5.0 Volt Supply
- Low Power Requirements
- Functionally Interchangeable With
  AM26LS31 (SN75172)
  MC3487 (SN75174)

QUAD RS-485 LINE DRIVERS WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



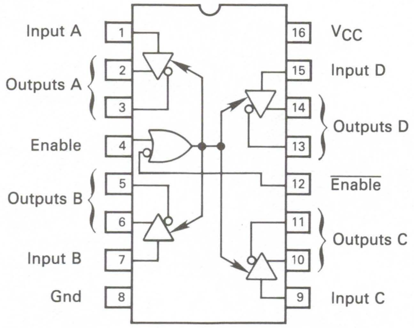
J SUFFIX
CERAMIC PACKAGE
CASE 620-02



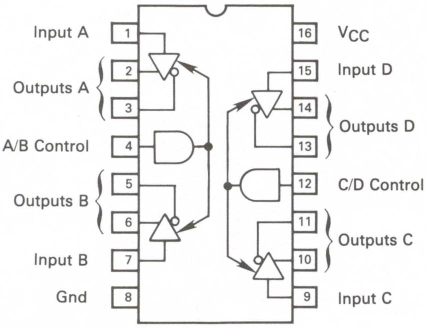
N SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS

SN75172


Input A
1
Outputs A
2
3
Enable
4
Outputs B
5
6
Input B
7
Gnd
8
16
VCC
15
Input D
14
Outputs D
13
12
Enable
11
Outputs C
10
9
Input C

SN75174


Input A
1
Outputs A
2
3
A/B Control
4
Outputs B
5
6
Input B
7
Gnd
8
16
VCC
15
Input D
14
Outputs D
13
12
C/D Control
11
Outputs C
10
9
Input C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SN75172

TRUTH TABLE

Input	Control Inputs (E/$\overline{E}$)	Noninverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

SN75174

TRUTH TABLE

Input	Control Input	Noninverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

MOTOROLA

SN75173
SN75175

Product Preview

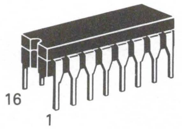
QUAD RS-485 LINE RECEIVERS

The Motorola SN75173/175 are monolithic quad differential line receivers with three-state outputs. They are designed specifically to meet the requirements of EIA standards RS-485, RS-422A/23A and CCITT recommendations.

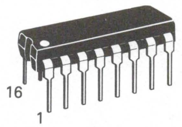
The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. They also feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75173/175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

- Meets EIA Standard RS-485
- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5.0 Volt Supply
- Low Power Requirements
- Plug-In Replacement for
  MC3486 (SN75175)
  AM26LS32 (SN75173)

QUAD RS-485 LINE RECEIVERS WITH THREE-STATE OUTPUTS

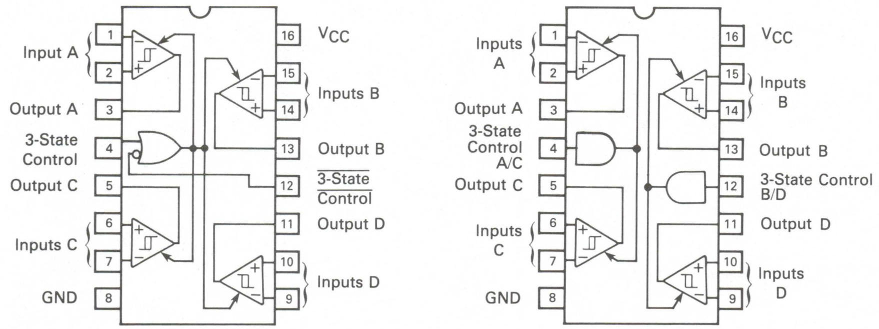


J SUFFIX
CERAMIC PACKAGE
CASE 620-02



N SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS


SN75173

SN75175
Input A
1
2
Output A
3
3-State Control
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control
11
Output D
10
Inputs D
9
Inputs A
1
2
Output A
3
3-State Control A/C
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control B/D
11
Output D
10
Inputs D
9

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SN75173

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs A–B	Enables G	Enables $\overline{G}$	Output Y
$V_{ID} \geq 0.2$ V	H X	X L	H H
-0.2 V $< V_{ID} < 0.2$ V	H X	X L	? ?
$V_{ID} \leq -0.2$ V	H X	X L	L L
X	L	H	Z

SN75175

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs A–B	Enable	Output Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

MOTOROLA

ULN2068B

QUAD 1.5 A SINKING HIGH-CURRENT SWITCH

The ULN2068B is a high-voltage, high-current quad Darlington switch array designed for high-current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high-current loads.

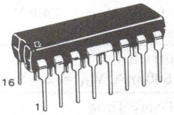
The Motorola ULN2068B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

It is supplied in an improved 16-lead plastic dual-in-line package with heat sink contact tabs (Pins 4,5 and 12,13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



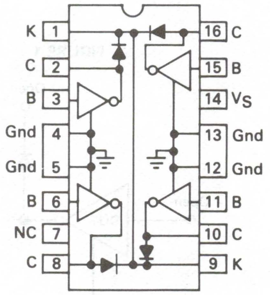
B SUFFIX
PLASTIC PACKAGE
CASE 648C-01

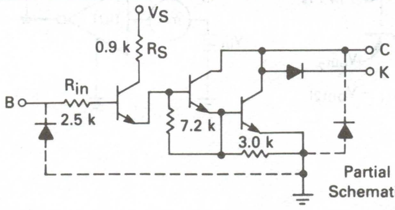
MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage — Note 2	V_I	15	V
Supply Voltage	V_S	10	V
Collector Current — Note 1	I_C	1.75	A
Input Current — Note 3	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

Notes:
1. Allowable output conditions shown in curves on Page 3.
2. Input voltage referenced to ground.
3. May be limited by max input voltage.

PIN CONNECTIONS





Partial Schematic

ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2068B	0°C to +70°C	Plastic DIP

* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current	1	I_{CEX}				µA
(V_{CE} = 50 V)			—	—	100	
(V_{CE} = 50 V, T_A = 70°C)			—	—	500	
Collector-Emitter Saturation Voltage	2	$V_{CE(sat)}$				V
(I_C = 500 mA, V_{in} = 2.4 V)			—	—	1.13	
(I_C = 750 mA, V_{in} = 2.4 V)			—	—	1.25	
(I_C = 1.0 A, V_{in} = 2.4 V)			—	—	1.40	
(I_C = 1.25 A, V_{in} = 2.4 V)			—	—	1.60	
Input Current — On Condition	4	$I_{I(on)}$				mA
(V_I = 2.4 V)			—	—	0.25	
(V_I = 3.75 V)			—	—	1.0	
Input Voltage — On Condition (V_{CE} = 2.0 V, I_C = 1.5 A)	5	$V_{I(on)}$	—	—	2.4	V
Inductive Load Test (V_S = 5.5 V, V_{CC} = 24.5 V, t_{PW} = 4.0 µs)	3	ΔV_{out}	—	—	100	mV
Supply Current (I_C = 500 mA, V_{in} = 2.4 V, V_S = 5.5 V)	8	I_S	—	—	6.0	mA
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	µs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	4.0	µs
Clamp Diode Leakage Current	6	I_R				µA
(V_R = 50 V)			—	—	50	
(V_R = 50 V, T_A = 70°C)			—	—	100	
Clamp Diode Forward Voltage	7	V_F				V
(I_F = 1.0 A)			—	—	1.75	
(I_F = 1.5 A)			—	—	2.0	

TEST FIGURES

FIGURE 1

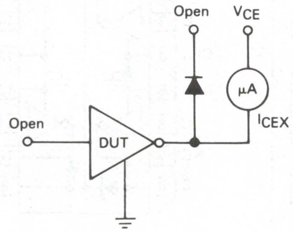

Open
V_{CE}
µA
I_{CEX}
Open
DUT

FIGURE 2

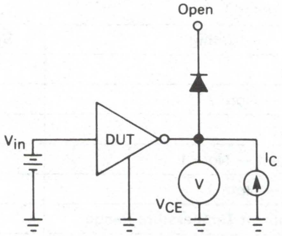

Open
V_{in}
DUT
I_C
V
V_{CE}

FIGURE 3

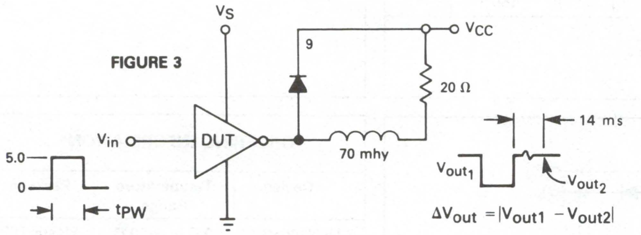
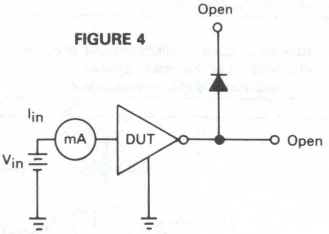

V_S
9
V_{CC}
20 Ω
V_{in}
DUT
70 mhy
5.0
0
t_{PW}
14 ms
V_{out1}
V_{out2}
$\Delta V_{out} = |V_{out1} - V_{out2}|$

FIGURE 4


Open
I_{in}
mA
V_{in}
DUT
Open

TEST FIGURES (CONTINUED)

FIGURE 5

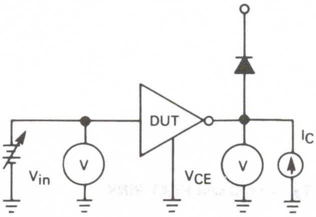

Open
DUT
V_{in}
V
V_{CE}
V
I_C

FIGURE 6

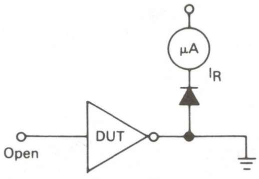

V_R
μA
I_R
DUT
Open

FIGURE 7

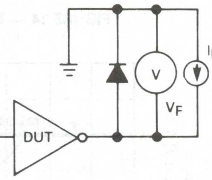
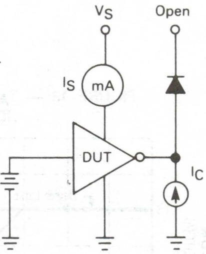

V
I_F
V_F
DUT
Open

FIGURE 8


V_S
Open
I_S
mA
V_{in}
DUT
I_C

TYPICAL CHARACTERISTIC CURVES — T_A = 25°C

FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE

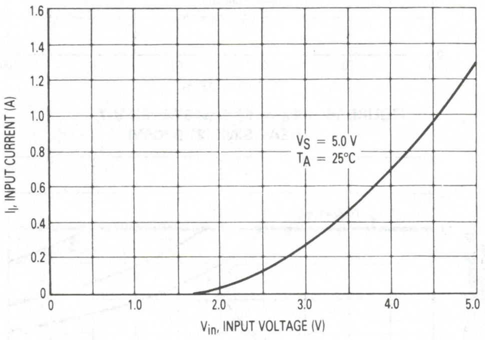


FIGURE 10 — COLLECTOR CURRENT versus INPUT CURRENT

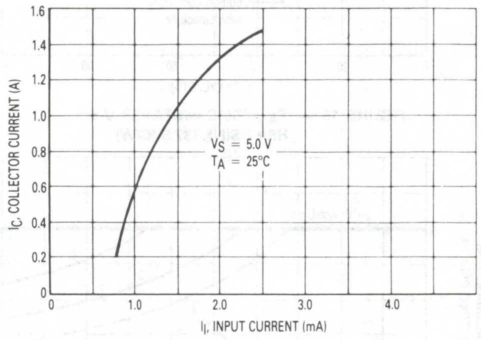


FIGURE 11 — T_A = 70°C w/o HEAT SINK

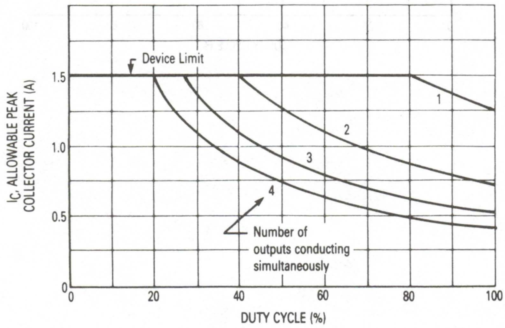


FIGURE 12 — T_A = 70°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

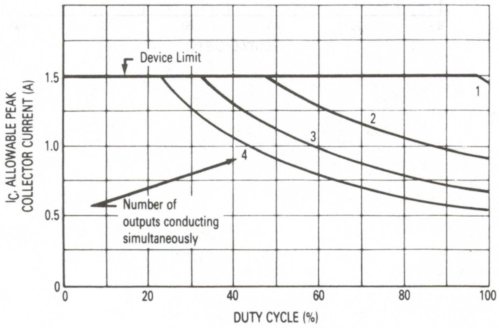


FIGURE 13 — T_A = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

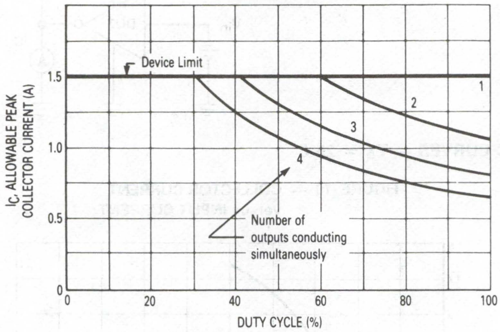


FIGURE 14 — T_A = 50°C w/o HEAT SINK

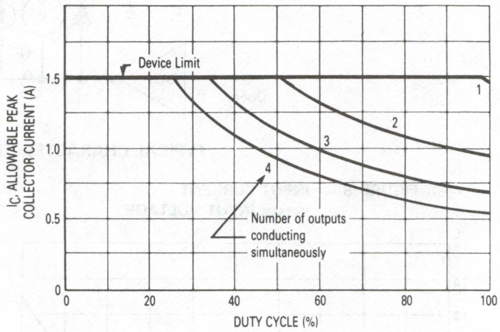


FIGURE 15 — T_A = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

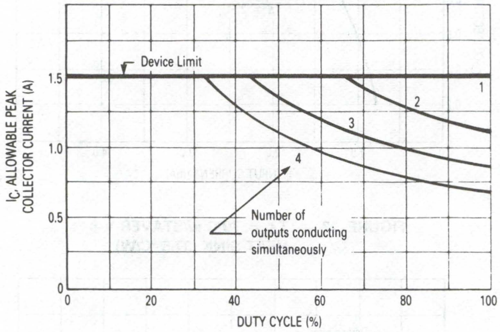
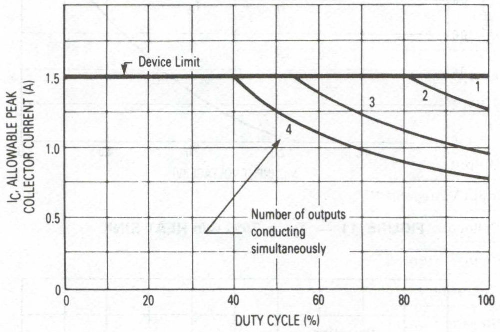


FIGURE 16 — T_A = 50°C w/ STAVER V-7 HEAT SINK (27.5 °C/W)



MOTOROLA

ULN2074B

QUAD 1.5 A SINKING HIGH-CURRENT SWITCH

The ULN2074B is a high-voltage, high-current quad Darlington switch array designed for high-current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high-current loads.

The Motorola ULN2074B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load.

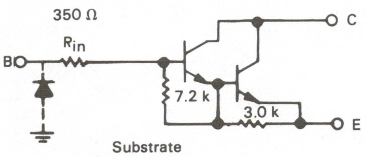
It is supplied in an improved 16-lead plastic dual-in-line package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp maximum Output Current
- Low Input Current
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package unless otherwise noted).

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage — Note 2	V_I	30	V
Collector Current — Note 1	I_C	1.75	A
Input Current — Note 3	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	150	°C

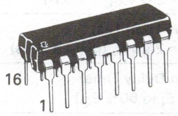
Notes:
1. Allowable output conditions shown in curves on Page 3.
2. Input voltage referenced to ground (substrate)
3. May be limited by max input voltage



Partial Schematic

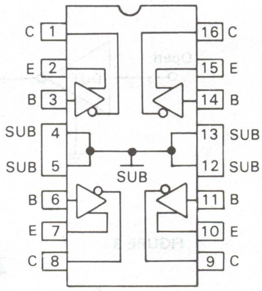
QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



B SUFFIX
PLASTIC PACKAGE
CASE 648C-01

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2074B	0°C to +70°C	Plastic DIP

* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				µA
(V_{CE} = 50 V)	1		—	—	100	
(V_{CE} = 50 V, T_A = 70°C)			—	—	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 500 mA, I_I = 625 µA)			—	—	1.13	
(I_C = 750 mA, I_I = 935 µA)	2		—	—	1.25	
(I_C = 1.0 A, I_I = 1.25 mA)			—	—	1.40	
(I_C = 1.25 A, I_I = 2.0 mA)			—	—	1.60	
Input Current — On Condition		$I_{I(on)}$				mA
(V_I = 2.4 V)	4		2.0	—	4.3	
(V_I = 3.75 V)			4.5	—	9.6	
Input Voltage — On Condition	5	$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 1.0 A)			—	—	2.0	
(V_{CE} = 2.0 V, I_C = 1.5 A)			—	—	2.5	
Inductive Load Test (V_{CC} = 24.5 V, t_{PW} = 4.0 µs)	3	ΔV_{out}	—	—	100	mV
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	µs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	1.5	µs

TEST FIGURES

FIGURE 1

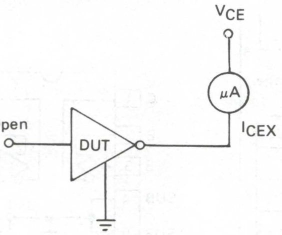

VCE
µA
Open
DUT
ICEX

FIGURE 2

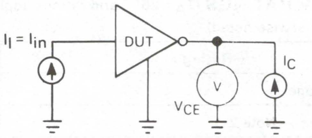

II = Iin
DUT
IC
V
VCE

FIGURE 3

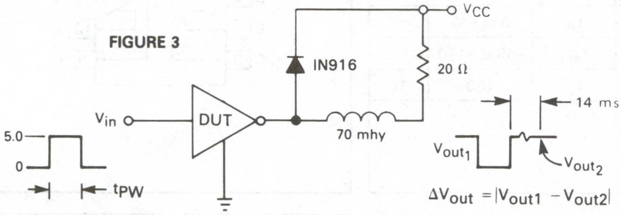

VCC
IN916
20 Ω
Vin
DUT
70 mhy
5.0
0
tPW
14 ms
Vout1
Vout2
ΔVout = |Vout1 − Vout2|

FIGURE 4

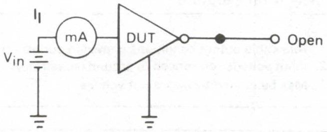
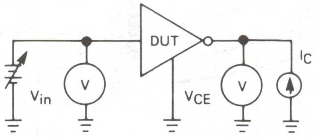

II
mA
DUT
Open
Vin

FIGURE 5



TYPICAL CHARACTERISTIC CURVES

FIGURE 6 — INPUT CURRENT versus INPUT VOLTAGE

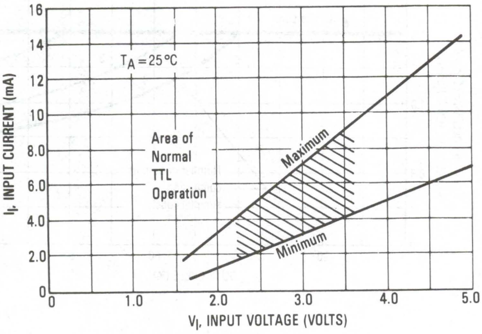


FIGURE 7 — COLLECTOR CURRENT versus INPUT CURRENT

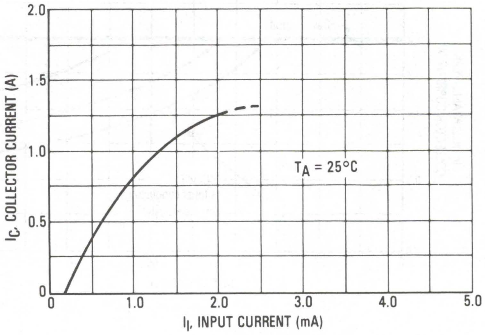


FIGURE 8 — $T_A = 70°C$ w/o HEAT SINK

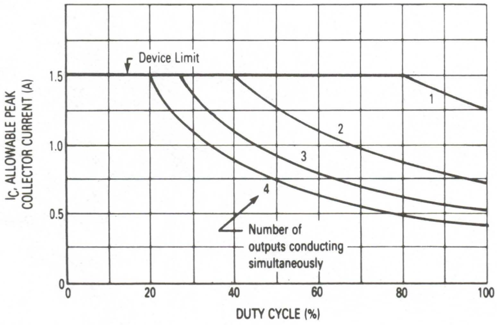


FIGURE 9 — $T_A = 70°C$ w/STAVER V-8 HEAT SINK (37.5 °C/W)

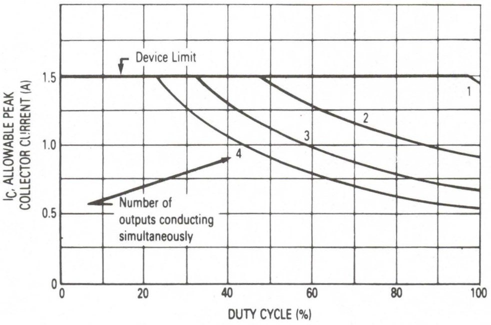


FIGURE 10 — T_A = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

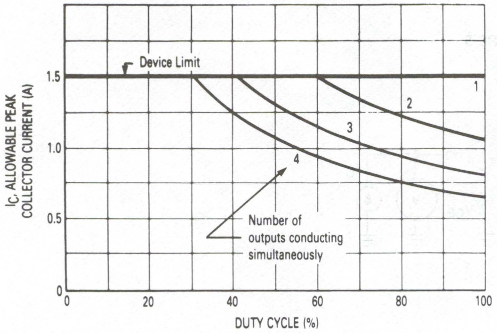


FIGURE 11 — T_A = 50°C w/o HEAT SINK

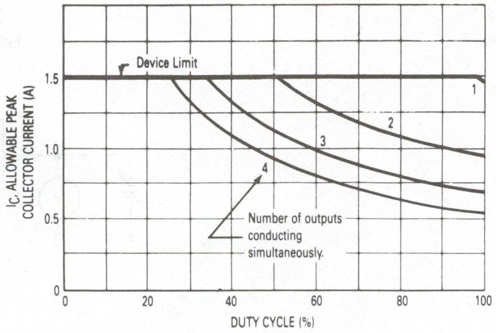


FIGURE 12 — T_A = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

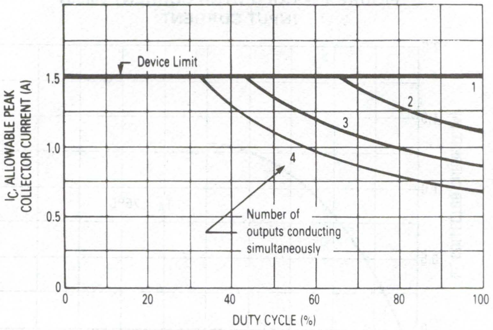
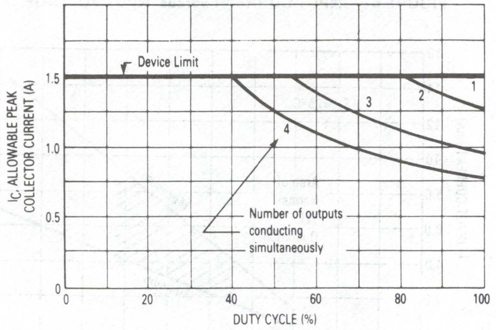
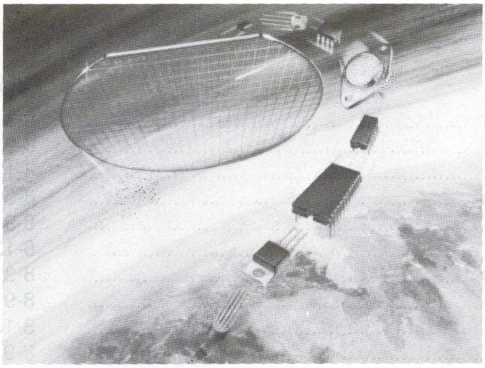


FIGURE 13 — T_A = 50°C w/STAVER V-7 HEAT SINK (27.5 °C/W)





Comparators

COMPARATORS

Device	Function	Page
LM111	High Performance Voltage Comparator	8-3
LM139,A	Quad Single-Supply Comparators	8-9
LM193,A	Dual Comparators	8-13
LM211	High Performance Voltage Comparator	8-3
LM239,A	Quad Single-Supply Comparators	8-9
LM293,A	Dual Comparators	8-13
LM311	High Performance Voltage Comparator	8-3
LM339,A	Quad Single-Supply Comparators	8-9
LM393,A	Dual Comparators	8-13
LM2901	Quad Single-Supply Comparators	8-9
LM2903	Dual Comparators	8-13
MC1414	Dual Differential Comparator	8-18
MC1514	Dual Differential Comparator	8-18
MC1710,C	Differential Comparator	8-22
MC1711,C	Dual Differential Comparator	8-26
MC3302	Quad Single-Supply Comparators	8-9
MC3324,A	Power Supply Supervisory Circuit/Dual-Voltage Comparator	8-30
MC3424,A	Power Supply Supervisory Circuit/Dual-Voltage Comparator	8-30
MC3430	High-Speed Quad Comparator	8-46
MC3431	High-Speed Quad Comparator	8-46
MC3432	High-Speed Quad Comparator	8-46
MC3433	High-Speed Quad Comparator	8-46
MC3524,A	Power Supply Supervisory Circuit/Dual-Voltage Comparator	8-30

MOTOROLA

LM111
LM211
LM311

HIGHLY FLEXIBLE VOLTAGE COMPARATORS

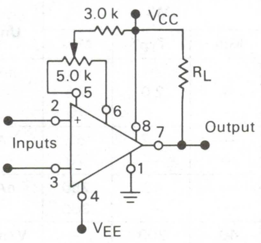
The ability to operate from a single power supply of 5.0 to 30 volts or ±15 volt split supplies, as commonly used with operational amplifiers, makes the LM111/LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the LM111/LM211/LM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

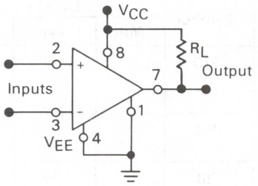
SILICON MONOLITHIC INTEGRATED CIRCUIT

TYPICAL COMPARATOR DESIGN CONFIGURATIONS

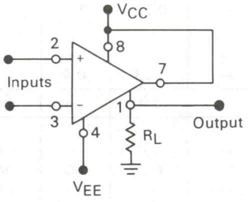
Split Power-Supply with Offset Balance


3.0 k
VCC
5.0 k
5
6
RL
2
8
7
Output
Inputs
3
1
4
VEE

Single Supply

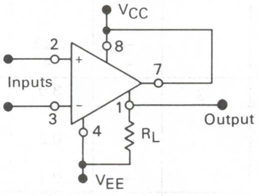

VCC
2
8
RL
7
Output
Inputs
3
1
VEE
4

Ground-Referred Load


VCC
2
8
Inputs
7
3
1
Output
4
RL
VEE

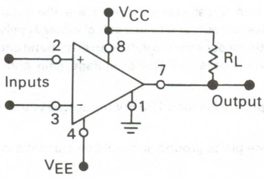
Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Negative Supply

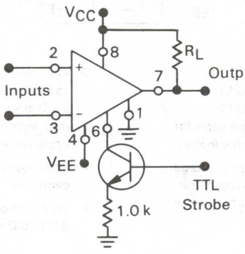

VCC
2
8
Inputs
7
3
1
Output
4
RL
VEE

Input polarity is reversed when Gnd pin is used as an output.

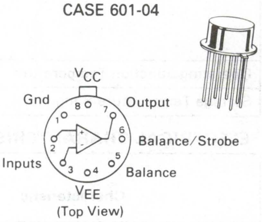
Load Referred to Positive Supply


VCC
2
8
RL
Inputs
7
Output
3
1
4
VEE

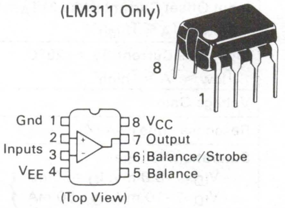
Strobe Capability


VCC
2
8
RL
7
Output
Inputs
3
1
4
6
VEE
TTL Strobe
1.0 k

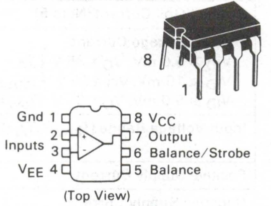
H SUFFIX
METAL PACKAGE
CASE 601-04


VCC
Gnd
Output
8
1
7
2
6
Balance/Strobe
Inputs
3
4
5
Balance
VEE
(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 626-04
(LM311 Only)


8
1
Gnd 1
Inputs 2
3
VEE 4
8 VCC
7 Output
6 Balance/Strobe
5 Balance
(Top View)

J-8 SUFFIX
CERAMIC PACKAGE
CASE 693-02


8
1
Gnd 1
Inputs 2
3
VEE 4
8 VCC
7 Output
6 Balance/Strobe
5 Balance
(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM111H LM111J-8	−55°C to +125°C	Metal Can Ceramic DIP
LM211H LM211J-8	−25°C to +85°C	Metal Can Ceramic DIP
LM311H LM311J-8 LM311N	0°C to +70°C	Metal Can Ceramic DIP Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		LM111 LM211	LM311	
Total Supply Voltage	$V_{CC} + \|V_{EE}\|$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	—	V_{CC} to $V_{CC}-5$	V_{CC} to $V_{CC}-5$	Vdc
Power Dissipation and Thermal Characteristics				
Metal Package	P_D	680		mW
Derate above T_A = +25°C	$1/\theta_{JA}$	5.5		mW/°C
Plastic and Ceramic Dual In-Line Packages	P_D	625		mW
Derate above T_A = +25°C	$1/\theta_{JA}$	5.0		mW/°C
Operating Ambient Temperature Range	T_A			°C
LM111		-55 to +125	—	
LM211		-25 to +85	—	
LM311		—	0 to +70	
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C unless otherwise noted [Note 1].)

Characteristic	Symbol	LM111 LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V_{IO}							mV
$R_S \leqslant 50\ k\Omega$, T_A = +25°C		—	0.7	3.0	—	2.0	7.5	
$R_S \leqslant 50\ k\Omega$, $T_{low} \leqslant T_A \leqslant T_{high}$*		—	—	4.0	—	—	10	
Input Offset Current (Note 3) T_A = +25°C	I_{IO}	—	1.7	10	—	1.7	50	nA
$T_{low} \leqslant T_A \leqslant T_{high}$*		—	—	20	—	—	70	
Input Bias Current, T_A = +25°C	I_{IB}	—	45	100	—	45	250	nA
$T_{low} \leqslant T_A \leqslant T_{high}$*		—	—	150	—	—	300	
Voltage Gain	A_V	40	200	—	40	200	—	V/mV
Response Time (Note 4)		—	200	—	—	200	—	ns
Saturation Voltage	V_{OL}							V
$V_{ID} \leqslant -5.0$ mV, I_O = 50 mA } T_A = +25°C		—	0.75	1.5	—	—	—	
$V_{ID} \leqslant -10$ mV, I_O = 50 mA } T_A = +25°C		—	—	—	—	0.75	1.5	
$V_{CC} \geqslant 4.5$ V, V_{EE} = 0, $T_{low} \leqslant T_A \leqslant T_{high}$*								
$V_{ID} \leqslant -6.0$ mV, $I_{sink} \leqslant 8.0$ mA		—	0.23	0.4	—	—	—	
$V_{ID} \leqslant -10$ mV, $I_{sink} \leqslant 8.0$ mA		—	—	—	—	0.23	0.4	
Strobe "On" Current (Note 5)	I_S	—	3.0	—	—	3.0	—	mA
Output Leakage Current								
$V_{ID} \geqslant 5.0$ mV, V_O = 35 V { T_A = +25°C		—	0.2	10	—	—	—	nA
$V_{ID} \geqslant 10$ mV, V_O = 35 V } I_{strobe} = 3.0 mA		—	—	—	—	0.2	50	nA
$V_{ID} \geqslant 5.0$ mV, V_O = 35 V, $T_{low} \leqslant T_A \leqslant T_{high}$*		—	0.1	0.5	—	—	—	µA
Input Voltage Range ($T_{low} \leqslant T_A \leqslant T_{high}$*)	V_{IR}	-14.5	-14.7 to 13.8	13.0	-14.5	-14.7 to 13.8	13.0	V
Positive Supply Current	I_{CC}	—	+2.4	+6.0	—	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	—	-1.3	-5.0	—	-1.3	-5.0	mA

NOTES:

* T_{low} = -55°C for LM111 T_{high} = +125°C for LM111
= -25°C for LM211 = +85°C for LM211
= 0°C for LM311 = +70°C for LM311

1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 volt supply up to ± 15 volt supplies.

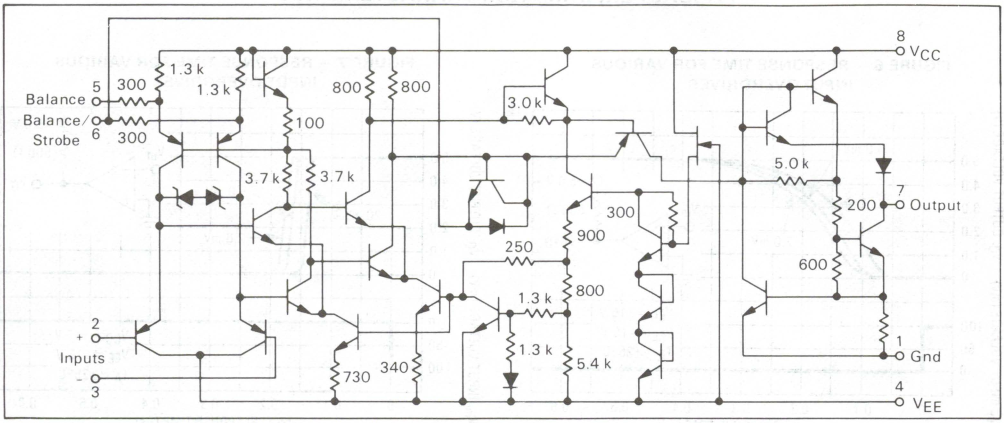
2. This rating applies for ±15 volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.

3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.

4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.

5. Do not short the strobe pin to ground; it should be current driven at 3.0 to 5.0 mA.

FIGURE 1 — CIRCUIT SCHEMATIC


8
VCC
Balance
5
300
1.3 k
1.3 k
Balance/
Strobe
6
300
100
800
800
3.0 k
3.7 k
3.7 k
5.0 k
200
7
Output
300
900
250
800
1.3 k
1.3 k
600
2
+
Inputs
−
3
730
340
5.4 k
1
Gnd
4
VEE

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

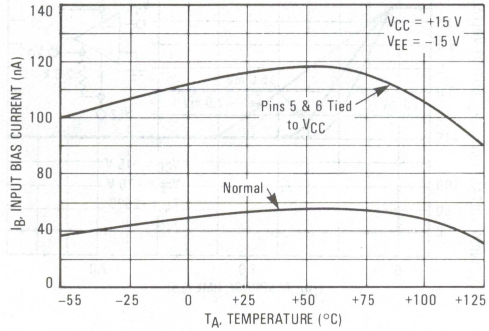


FIGURE 3 — INPUT OFFSET CURRENT versus TEMPERATURE

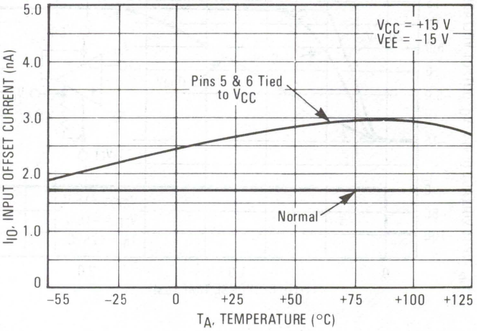


FIGURE 4 — INPUT BIAS CURRENT versus DIFFERENTIAL INPUT VOLTAGE

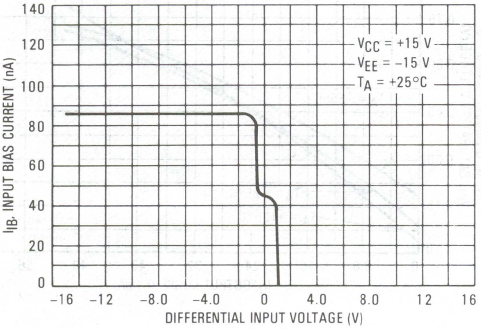
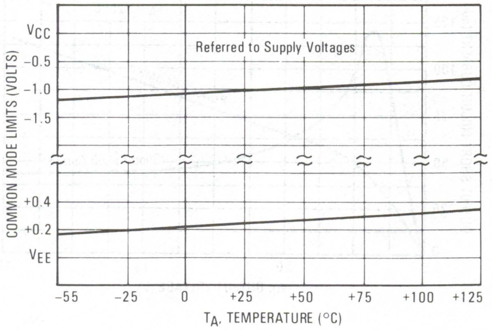


FIGURE 5 — COMMON MODE LIMITS versus TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 6 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

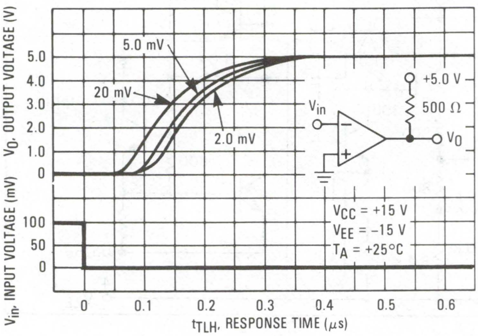


FIGURE 7 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

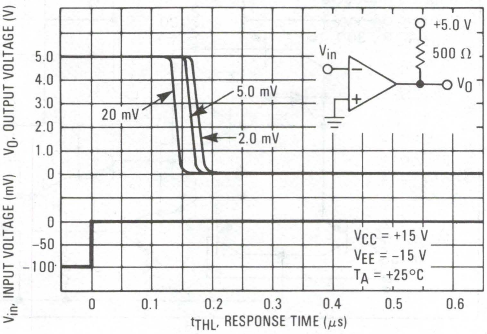


FIGURE 8 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

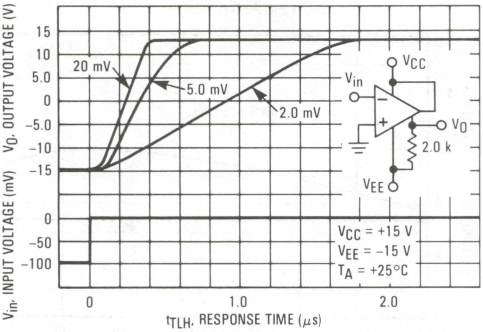


FIGURE 9 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

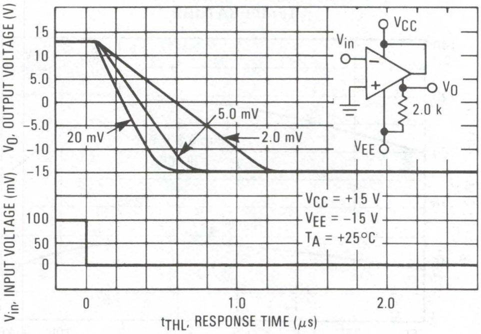


FIGURE 10 — OUTPUT SHORT CIRCUIT CURRENT CHARACTERISTICS AND POWER DISSIPATION

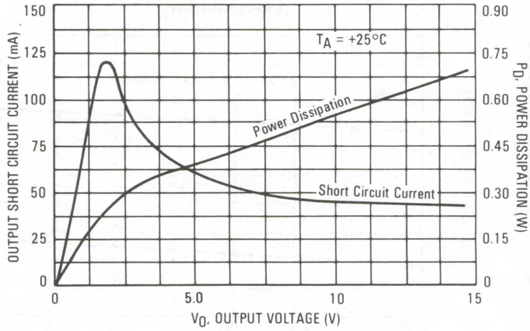
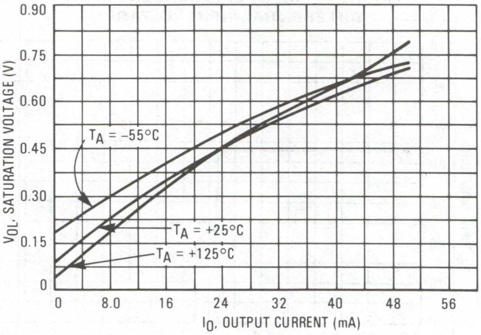


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

FIGURE 12 — OUTPUT LEAKAGE CURRENT versus TEMPERATURE

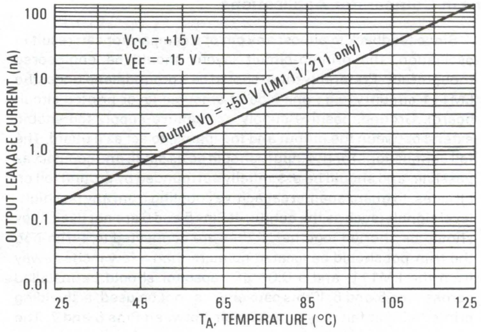


FIGURE 13 — POWER SUPPLY CURRENT versus SUPPLY VOLTAGE

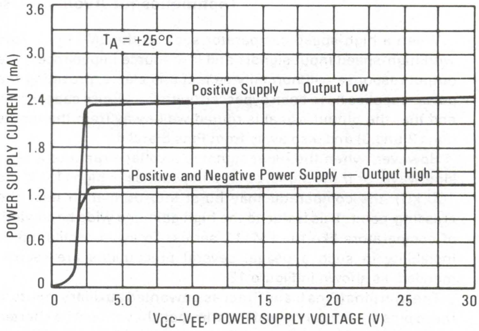
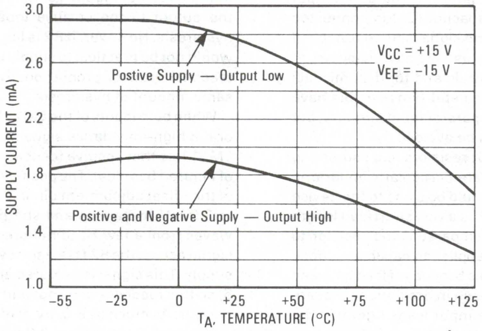


FIGURE 14 — POWER SUPPLY CURRENT versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 15 — IMPROVED METHOD OF ADDING HYSTERESIS WITHOUT APPLYING POSITIVE FEEDBACK TO THE INPUTS

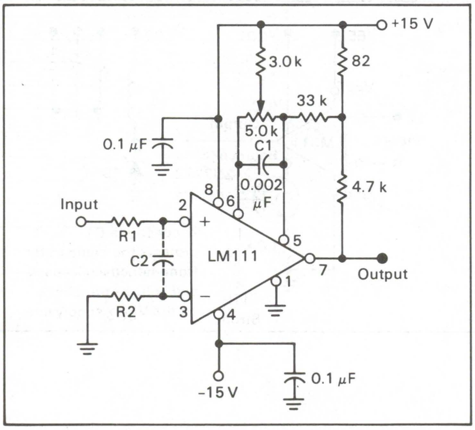
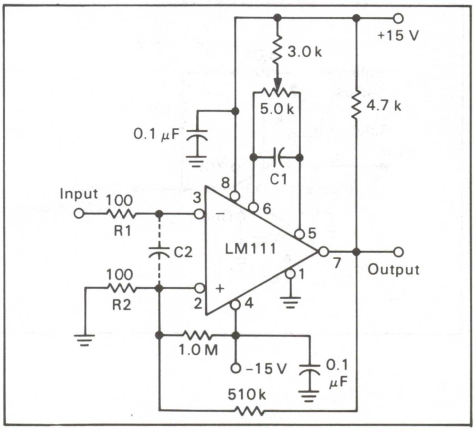

+15 V
3.0 k
82
33 k
5.0 k
C1
0.1 μF
0.002 μF
4.7 k
8
6
2
+
Input
R1
C2
LM111
5
7
Output
1
R2
3
−
4
−15 V
0.1 μF

FIGURE 16 — CONVENTIONAL TECHNIQUE FOR ADDING HYSTERESIS


+15 V
3.0 k
5.0 k
4.7 k
0.1 μF
C1
8
6
Input
100
R1
3
−
5
C2
LM111
7
Output
1
100
R2
2
+
4
1.0 M
−15 V
0.1 μF
510 k

APPLICATIONS INFORMATION

Techniques for Avoiding Oscillations in Comparator Applications

When a high-speed comparator such as the LM111 is used with high-speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to ac coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for dc and for dynamic (ac) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM111, and a 0.01 μF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

FIGURE 17 — ZERO-CROSSING DETECTOR DRIVING CMOS LOGIC

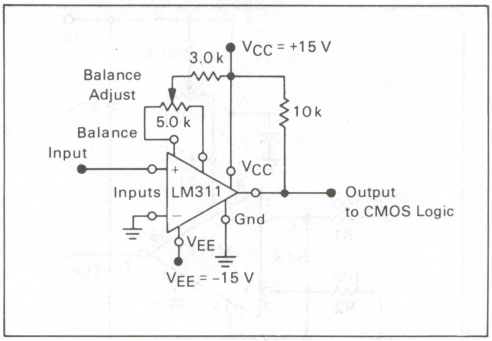
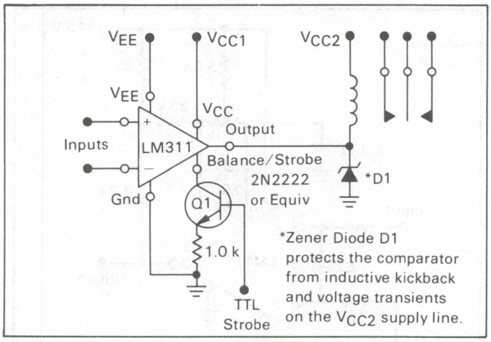


FIGURE 18 — RELAY DRIVER WITH STROBE CAPABILITY



*Zener Diode D1 protects the comparator from inductive kickback and voltage transients on the V_{CC2} supply line.

MOTOROLA

LM139, A
LM239, A LM2901
LM339, A MC3302

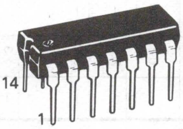
QUAD SINGLE-SUPPLY COMPARATORS

These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

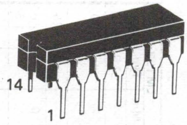
- Single of Split Supply Operation
- Low Input Bias Current — 25 nA (Typ)
- Low Input Offset Current — ±5.0 nA (Typ)
- Low Input Offset Voltage — ±1.0 mV (Typ LM139A Series)
- Input Common-Mode Voltage Range to Gnd
- Low Output Saturation Voltage — 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646-05

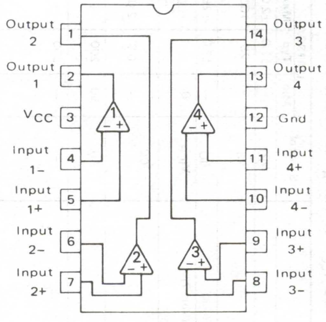


CERAMIC PACKAGE
CASE 632-02
MO-001AA

MAXIMUM RATINGS

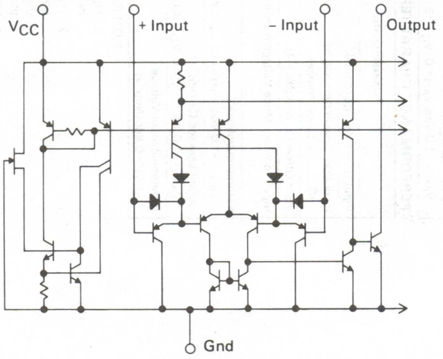
Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/ LM339A/LM2901 MC3302	V_{CC}	+36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to V_{CC}	Vdc
Output Short-Circuit to Gnd (Note 1)	I_{SC}	Continuous	
Input Current (V_{in} < -0.3 Vdc) (Note 2)	I_{in}	50	mA
Power Dissipation @ T_A = 25°C Ceramic Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 1.0 8.0 1.0 8.0	 Watts mW/°C Watts mW/°C
Operating Ambient Temperature Range LM139, A LM239, A LM2901/MC3302 LM339, A	T_A	 −55 to +125 −25 to +85 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS



(Top View)

FIGURE 1 — CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	-55°C to +125°C	Ceramic DIP
LM239J, AJ LM239N, AN	-25°C to +85°C	Ceramic DIP Plastic DIP
LM339J, AJ LM339N, AN	0°C to +70°C	Ceramic DIP Plastic DIP
LM2901N MC3302L MC3302P	-40°C to +85°C	Plastic DIP Ceramic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	—	±2.0	±7.0	—	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	—	±3.0	±100	nA
Input Common-Mode Voltage Range (Note 7)	V_{ICR}	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	V
Supply Current	I_{CC}																			
R_L = ∞ (For All Comparators)		—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	—	0.8	2.0	mA
R_L = ∞, V_{CC} = 30 Vdc		—	—	—	—	—	—	—	—	—	—	—	—	—	1.0	2.5	—	—	—	
Voltage Gain $R_L \geq 15\ k\Omega$, V_{CC} = 15 Vdc	A_V	50	200	—	50	200	—	—	200	—	—	200	—	25	100	—	2	30	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, $R_L = 5.1\ k\Omega$	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, $R_L = 5.1\ k\Omega$	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	μs
Output Sink Current $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $V_O \leq 1.5$ Vdc	I_{sink}	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $I_{sink} \leq 4.0$ mA	V_{sat}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current $V_I(+) \geq +1.0$ Vdc, $V_I(-) = 0$, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	±4.0	—	—	±4.0	—	—	±9.0	—	—	+9.0	—	—	±15	—	—	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	±100	—	—	±150	—	—	±100	—	—	±150	—	—	±200	—	—	±300	nA
Input Common-Mode Voltage Range	V_{ICR}	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	V
Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $I_{sink} \leq 4.0$ mA	V_{sat}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current $V_I(+) \geq +1.0$ Vdc, $V_I(-) = 0$, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	μA
Differential Input Voltage All $V_I \geq 0$ Vdc (Note 7)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

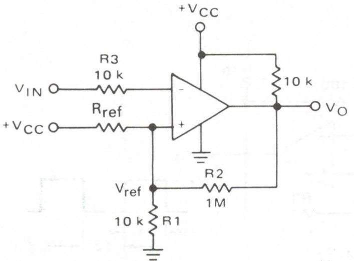
NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
3. LM139/139A — T_{low} = -55°C, T_{high} = +125°C
3. LM239/239A — T_{low} = -25°C, T_{high} = +85°C

LM339/339A — T_{low} = 0°C, T_{high} = +70°C
LM2901/MC3302 — T_{low} = -40°C, T_{high} = +85°C

4. At the output switch point, $V_O \simeq 1.4$ Vdc, $R_S \leq 100\ \Omega$, 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common-mode range (0 Vdc to V_{CC} - 1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.
7. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state. With V_{CC} = 5.0 Vdc, V_I should be limited to 25 volts max. Limiting resistors should be used on all inputs that might exceed V_{CC}.

FIGURE 2 — INVERTING COMPARATOR WITH HYSTERESIS


+VCC
R3
10 k
VIN
+VCC
Rref
10 k
VO
Vref
R2
1M
10 k
R1

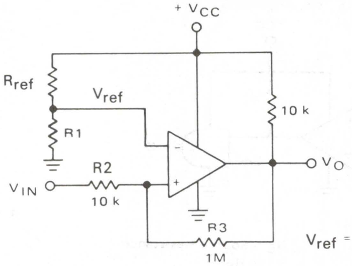
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \simeq R1 // R_{ref} // R2$$

$$V_H = \frac{R1 // R_{ref}}{R1 // R_{ref} + R2}\,(V_{O\,max} - V_{O\,min})$$

$$R2 >> R_{ref} // R1$$

FIGURE 3 — NON-INVERTING COMPARATOR WITH HYSTERESIS


+ VCC
Rref
Vref
R1
10 k
VO
R2
VIN
10 k
R3
1M

$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1 // R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,(V_{O\,max} - V_{O\,min})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 4 — NORMALIZED INPUT OFFSET VOLTAGE

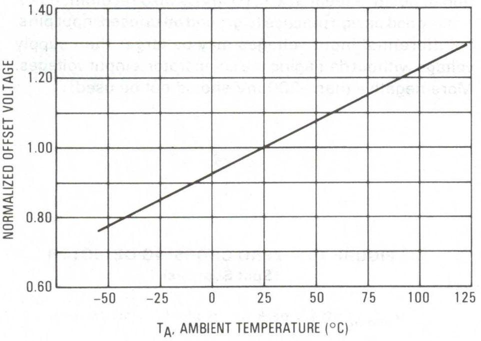


FIGURE 5 — INPUT BIAS CURRENT

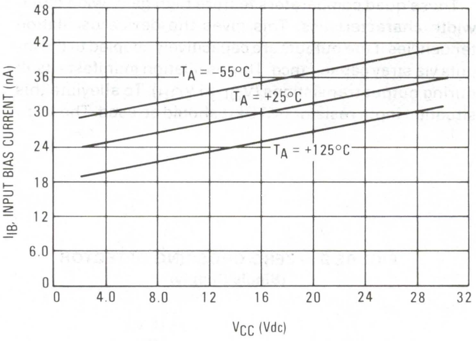


FIGURE 6 — OUTPUT SINK CURRENT versus OUTPUT SATURATION VOLTAGE

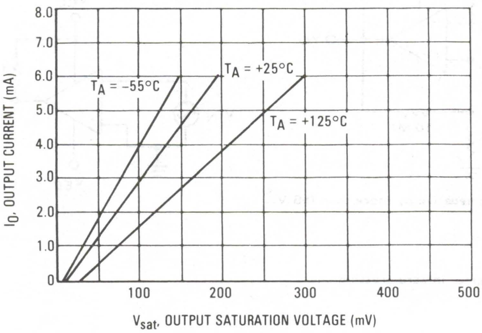
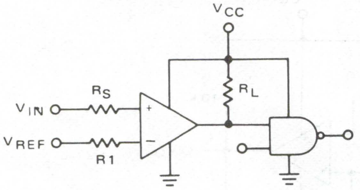


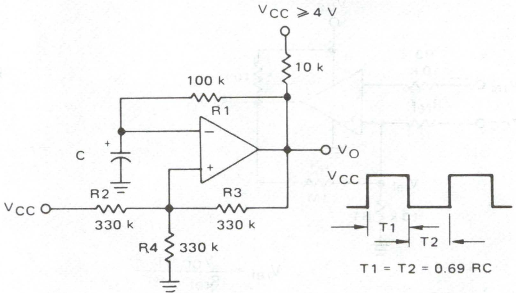
FIGURE 7 — DRIVING LOGIC


VCC
RS
RL
VIN
VREF
R1
+
−

R_S = Source Resistance
$R1 \simeq R_S$

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 8 — SQUAREWAVE OSCILLATOR


VCC ≥ 4 V
10 k
100 k
R1
C
+
−
VO
R2
330 k
R3
330 k
VCC
R4
330 k
VCC
T1
T2

$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C\,(\mu F)}$

$R2 = R3 = R4$

$R1 \approx R2//R3//R4$

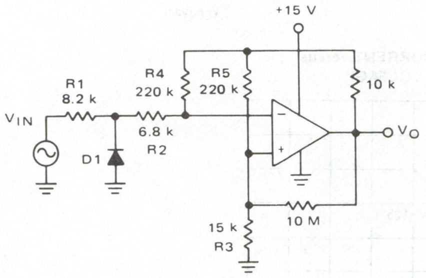
APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transistions (V_{OL} to V_{OH}). To alleviate this situation input resistors $<10\,k\Omega$ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −300 mV should not be used.

FIGURE 9 — ZERO CROSSING DETECTOR
(Single Supply)


+15 V
R1
8.2 k
R4
220 k
R5
220 k
10 k
VIN
6.8 k
R2
D1
−
+
VO
15 k
R3
10 M

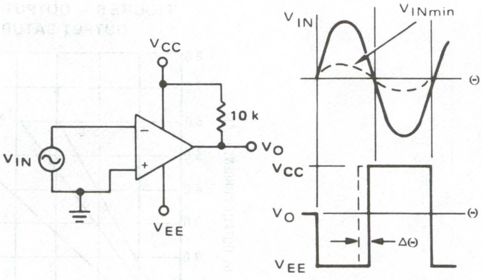
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leqslant \frac{R5}{10}$ for small error in zero crossing

FIGURE 10 — ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).


VIN
VINmin
Θ
VCC
10 k
VO
VIN
−
+
VEE
VCC
VO
Θ
ΔΘ
VEE

MOTOROLA

LM193 LM193A
LM293 LM293A
LM393 LM393A
LM2903

SINGLE-SUPPLY, LOW-POWER, LOW-OFFSET-VOLTAGE DUAL COMPARATORS

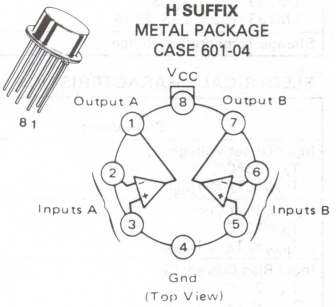
The LM193 series are dual independent precision voltage comparators capable of single- or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset-voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
- Split-Supply Range — ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply-Voltage — 0.4 mA
- Low Input Bias Current — 25 nA
- Low Input Offset Current — 5.0 nA
- Low Input Offset Voltage — 2.0 mV (max) LM193A/293A/393A
  — 5.0 mV (max) LM193/293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

DUAL COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

H SUFFIX
METAL PACKAGE
CASE 601-04


8 1
VCC
Output A
Output B
8
1
7
2
6
Inputs A
Inputs B
3
5
4
Gnd
(Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 626-04

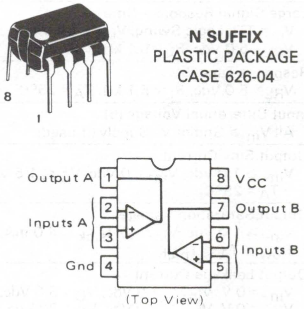
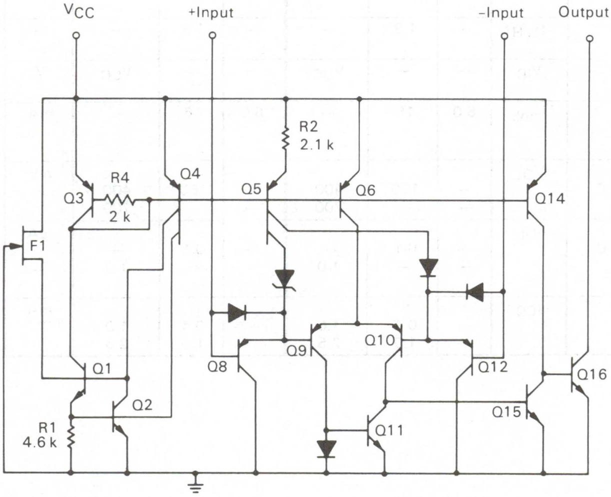

8
1
Output A
1
8
VCC
2
7
Output B
Inputs A
3
6
Inputs B
Gnd
4
5
(Top View)

FIGURE 1 — CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)


VCC
+Input
-Input
Output
R2
2.1 k
R4
2 k
Q3
Q4
Q5
Q6
Q14
F1
Q1
Q2
R1
4.6 k
Q8
Q9
Q10
Q11
Q12
Q15
Q16

ORDERING INFORMATION

Device	Temperature Range	Package
LM193AH,H	-55 to +125°C	Metal Can
LM293AH,H	-25 to +85°C	Metal Can
LM393AH,H	0 to +70°C	Metal Can
LM393AN,N	0 to +70°C	Plastic Mini DIP
LM2903N	-40 to +85°C	Plastic Mini DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Input Current (1) ($V_{in} < -0.3$ Vdc)	I_{in}	50	mA
Output Short Circuit-to-Ground Output Sink Current	I_{SC} I_{sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C			
Molded DIP	P_D	570	mW
Derate above 25°C	$1/R_{\theta JA}$	5.7	mW/°C
Metal Can	P_D	830	mW
Derate above 25°C	$1/R_{\theta JA}$	6.64	mW/°C
Operating Ambient Temperature Range	T_A		°C
LM193, 193A		-55 to +125	
LM293, 293A		-25 to +85	
LM393, 393A		0 to +70	
LM2903		-40 to +85	
Maximum Operating Junction Temperature	$T_{J(max)}$		°C
LM393, 393A, 2903		125	
LM193, 193A, 293, 293A		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193A			LM293A, LM393A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (2)	V_{IO}							mV
T_A = 25°C		—	±1.0	±2.0	—	±1.0	±2.0	
$T_{low} \leq T_A \leq T_{high}$		—	—	4.0	—	—	4.0	
Input Offset Current	I_{IO}							nA
T_A = 25°C		—	±3.0	±25	—	±5.0	±50	
$T_{low} \leq T_A \leq T_{high}$		—	—	±100	—	—	±150	
Input Bias Current (3)	I_{IB}							nA
T_A = 25°C		—	25	100	—	25	250	
$T_{low} \leq T_A \leq T_{high}$		—	—	300	—	—	400	
Input Common Mode Voltage Range (4)	V_{ICR}							Volts
T_A = 25°C		0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	
$T_{low} \leq T_A \leq T_{high}$		0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	
Voltage Gain $R_L \geq 15$ kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	—	50	200	—	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	—	—	300	—	—	300	—	ns
Response Time (5) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	—	1.3	—	—	1.3	—	μs
Input Differential Voltage (6) All $V_{in} \geq$ Gnd or V- Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \leq 1.5$ Vdc T_A = 25°C	I_{sink}	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage	V_{OL}							mV
$V_{in-} \geq 1.0$ Vdc, V_{in+} = 0, $I_{sink} \leq 4.0$ mA, T_A = 25°C		—	150	400	—	150	400	
$T_{low} \leq T_A \leq T_{high}$		—	—	700	—	—	700	
Output Leakage Current	I_{OL}							μA
V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 5.0 Vdc, T_A = 25°C		—	0.1	—	—	0.1	—	
V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$		—	—	1.0	—	—	1.0	
Supply Current	I_{CC}							mA
$R_L = \infty$ Both Comparators, T_A = 25°C		—	0.4	1.0	—	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		—	1.0	2.5	—	1.0	2.5	

*LM193/193A — T_{low} = -55°C, T_{high} = +125°C
LM293/293A — T_{low} = -25°C, T_{high} = +85°C
LM393/393A — T_{low} = 0°C, T_{high} = +70°C
LM2903 — T_{low} = -40°C, T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193			LM293, LM393			LM2903			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (2)	V_{IO}										mV
T_A = 25°C		—	±1.0	±5.0	—	±1.0	±5.0	—	±2.0	±7.0	
$T_{low} \leq T_A \leq T_{high}$		—	—	9.0	—	—	9.0	—	9.0	15	
Input Offset Current	I_{IO}										nA
T_A = 25°C		—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	
$T_{low} \leq T_A \leq T_{high}$		—	—	±100	—	—	±150	—	±50	±200	
Input Bias Current (3)	I_{IB}										nA
T_A = 25°C		—	25	100	—	25	250	—	25	250	
$T_{low} \leq T_A \leq T_{high}$		—	—	300	—	—	400	—	200	500	
Input Common Mode Voltage Range (4)	V_{ICR}										Volts
T_A = 25°C		0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	0	—	V_{CC} -1.5	
$T_{low} \leq T_A \leq T_{high}$		0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	0	—	V_{CC} -2.0	
Voltage Gain $R_L \geq 15\ k\Omega$, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	—	50	200	—	25	200	—	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, $R_L = 5.1\ k\Omega$, T_A = 25°C	—	—	300	—	—	300	—	—	300	—	ns
Response Time (5) V_{RL} = 5.0 Vdc, $R_L = 5.1\ k\Omega$, T_A = 25°C	t_{TLH}	—	1.3	—	—	1.3	—	—	1.5	—	μs
Input Differential Voltage (6) All $V_{in} \geq$ Gnd or V– Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \leq 1.5$ Vdc T_A = 25°C	I_{sink}	6.0	16	—	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage	V_{OL}										mV
$V_{in-} \geq 1.0$ Vdc, V_{in+} = 0, $I_{sink} \leq 4.0$ mA, T_A = 25°C		—	150	400	—	150	400	—	—	400	
$T_{low} \leq T_A \leq T_{high}$		—	—	700	—	—	700	—	200	700	
Output Leakage Current	I_{OL}										nA
V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 5.0 Vdc, T_A = 25°C		—	0.1	—	—	0.1	—	—	0.1	—	
V_{in-} = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$		—	—	1000	—	—	1000	—	—	1000	
Supply Current	I_{CC}										mA
$R_L = \infty$ Both Comparators, T_A = 25°C		—	0.4	1.0	—	0.4	1.0	—	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		—	—	2.5	—	—	2.5	—	—	2.5	

*LM193/193A — T_{low} = -55°C, T_{high} = +125°C
LM293/293A — T_{low} = -25°C, T_{high} = +85°C
LM393/393A — T_{low} = 0°C, T_{high} = +70°C

NOTES:

(1) This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become > -0.3 V of ground or negative supply.

(2) At output switch point, $V_O \simeq 1.4$ Vdc, $R_s = 0\ \Omega$ with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common-mode range (0 volts to V_{CC} -1.5 volts)

(3) Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.

(4) Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} -1.5 V, but either or both inputs can be taken to as high as 30 volts without damage.

(5) Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive, faster response times are obtainable.

(6) The comparator will exhibit proper output state, if one of the inputs become greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than -0.3 volts of ground or minus supply.

(7) If input signals exceed V_{CC}, only the overdriven comparator is affected.

(8) Overdriven inputs should be limited to 25 V when using a 5.0 V supply. Input current limiting resistors should be used when inputs are likely to exceed supply positive supply voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

LM193,A/293,A/393,A

FIGURE 2 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

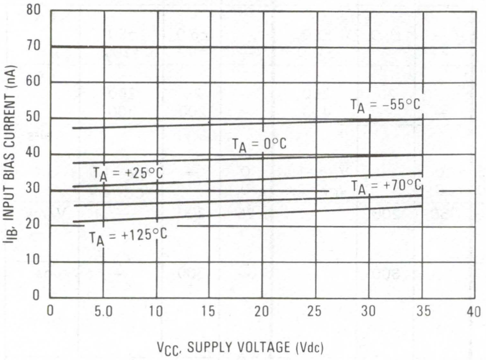


FIGURE 3 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

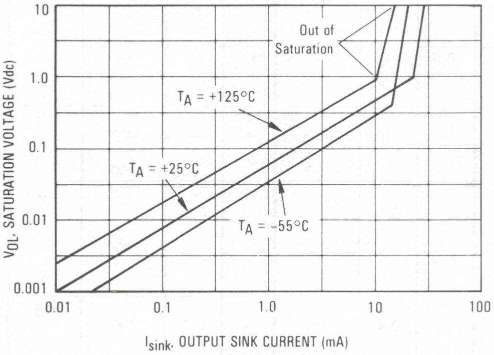
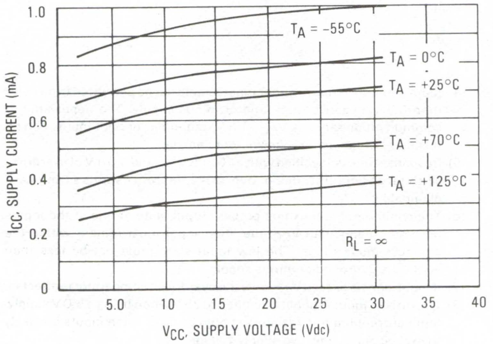


FIGURE 4 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



LM2903

FIGURE 5 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

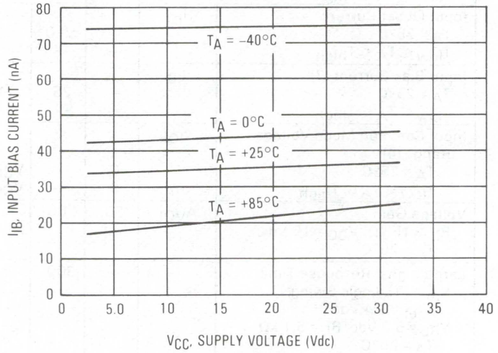


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

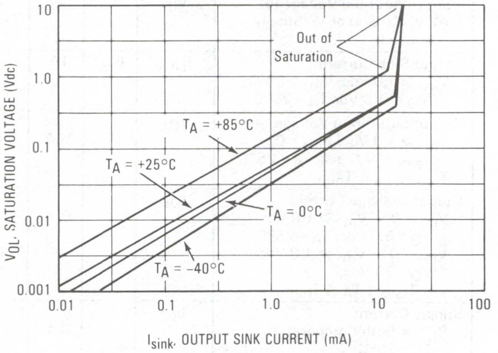
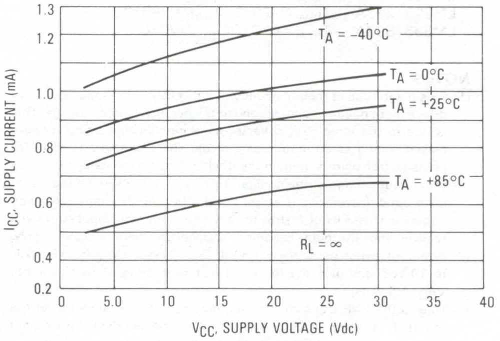


FIGURE 7 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



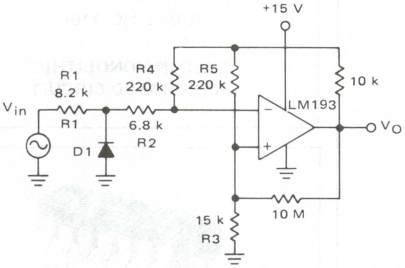
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −0.3 V should not be used.

FIGURE 8 — ZERO CROSSING DETECTOR
(Single Supply)


+15 V
R1
8.2 k
R4
220 k
R5
220 k
10 k
Vin
R1
6.8 k
R2
LM193
VO
D1
15 k
R3
10 M

D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leqslant \frac{R5}{10}$ for small error in zero crossing

FIGURE 9 — ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).

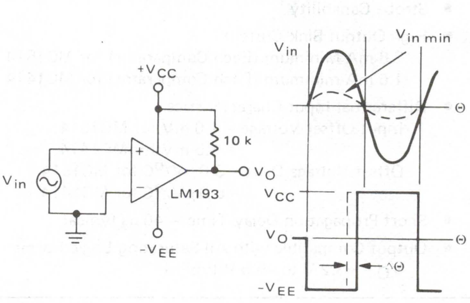

Vin min
Vin
+VCC
Θ
10 k
Vin
VO
LM193
VCC
VO
Θ
−VEE
ΔΘ
−VEE

FIGURE 10 — FREE-RUNNING SQUARE-WAVE OSCILLATOR

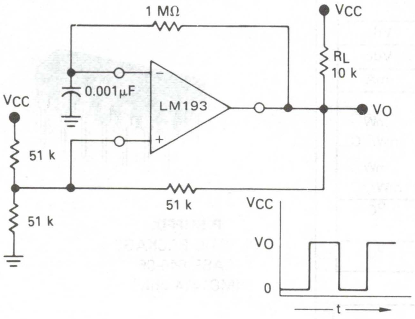
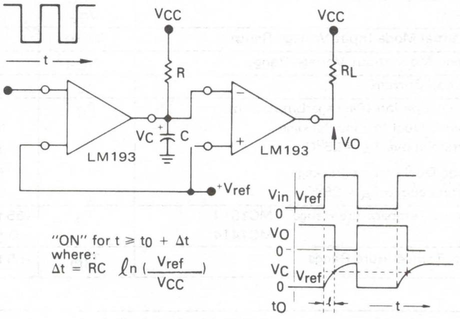
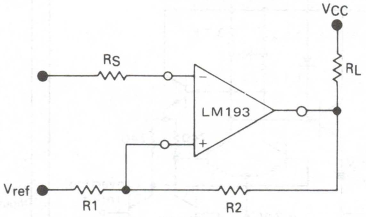

1 MΩ
VCC
RL
10 k
0.001μF
VCC
LM193
VO
51 k
51 k
51 k
VCC
VO
0
t

FIGURE 11 — TIME DELAY GENERATOR


t
VCC
VCC
R
RL
VC
C
LM193
LM193
VO
+Vref
Vin
Vref
0
VO
0
VC
Vref
0
t0
t

"ON" for $t \geqslant t_0 + \Delta t$
where:
$\Delta t = RC \; \ell n \left(\frac{V_{ref}}{V_{CC}}\right)$

FIGURE 12 — COMPARATOR WITH HYSTERESIS


VCC
RS
RL
LM193
Vref
R1
R2

$R_S = R1 \parallel R2$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O}\,\text{Low})\,R1}{R1 + R2 + R_L}$$

MC1414
MC1514

MOTOROLA

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

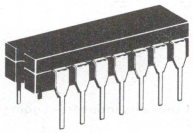
. . . designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
  2.8 mA Minimum (Each Comparator) for MC1514
  1.6 mA minimum (Each Comparator) for MC1414
- Differential Input Characteristics
  Input Offset Voltage = 1.0 mV for MC1514
  = 1.5 mV for MC1414
  Offset Voltage Drift = 3.0 μV/°C for MC1514
  = 5.0 μV/°C for MC1414
- Short Propagation Delay Time – 40 ns typical
- Output Compatible with All Saturating Logic Forms
  V_O = +3.2 V to -0.5 V typical

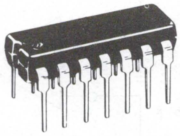
DUAL DIFFERENTIAL COMPARATOR

(DUAL MC1710)

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

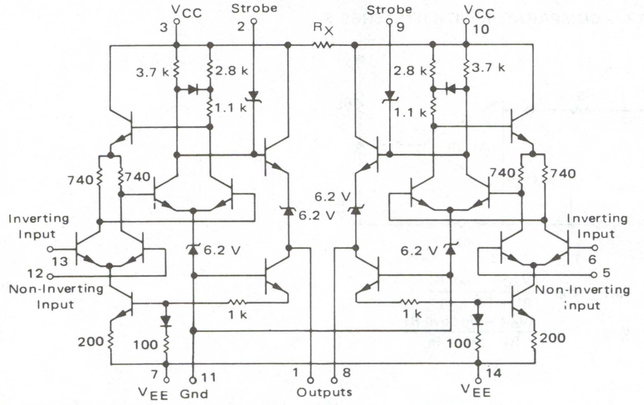


P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC1414 only)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

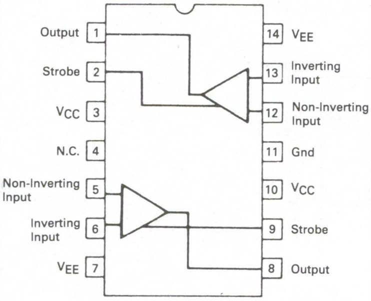
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	±5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = 25°C		6.0	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = 25°C		5.0	mW/°C
Operating Temperature Range MC1514 MC1414	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



VCC
3
Strobe
2
RX
Strobe
9
VCC
10
3.7 k
2.8 k
1.1 k
2.8 k
3.7 k
1.1 k
740
740
740
740
6.2 V
6.2 V
6.2 V
6.2 V
Inverting Input
13
12
Non-Inverting Input
Inverting Input
6
5
Non-Inverting Input
1 k
1 k
200
100
100
200
7
VEE
11
Gnd
1
8
Outputs
14
VEE

R_X = Low Resistance Value, usually < 100Ω, not specified.



Output 1
Strobe 2
VCC 3
N.C. 4
Non-Inverting Input 5
Inverting Input 6
VEE 7
14 VEE
13 Inverting Input
12 Non-Inverting Input
11 Gnd
10 VCC
9 Strobe
8 Output

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = −6 Vdc, T_A = 25°C unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514 Min	MC1514 Typ	MC1514 Max	MC1414 Min	MC1414 Typ	MC1414 Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	2.0	–	1.5	5.0	
(V_O = 1.8 Vdc, T_A = T_{low}*)		–	–	3.0	–	–	6.5	
(V_O = 1.0 Vdc, T_A = T_{high}*)		–	–	3.0	–	–	6.5	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	3.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	3.0	–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	7.0	–	–	7.5	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	3.0	–	–	7.5	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	12	20	–	15	25	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	45	–	18	40	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	20	–	–	40	
Open Loop Voltage Gain	A_{vol}							V/V
(T_A = 25°C)		1250	1700	–	1000	1500	–	
(T_A = T_{low} to T_{high})		1000	–	–	800	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage	V_{OL}							Vdc
($V_{ID} \geq -5.0$ mV, I_{OS} = 2.8 mA)		-1.0	-0.5	0	–	–	–	
($V_{ID} \geq -5.0$ mV, I_{OS} = 1.6 mA)		–	–	–	-1.0	-0.5	0	
Output Sink Current ($V_{ID} \geq -5.0$ mV, $V_{OL} \leq 0.4$ V, T_A = T_{low} to T_{high})	I_{OS}	2.8	3.4	–	1.6	2.5	–	mAdc
Input Common Mode Voltage Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Vdc
Common-Mode Rejection Ratio (V_{EE} = -7.0 Vdc, $R_S \leq 200\ \Omega$)	CMRR	80	100	–	70	100	–	dB
Strobe Low Level Current (V_{IL} = 0)	I_{IL}	–	–	2.5	–	–	2.5	mA
Strobe High Level Current (V_{IH} = 5.0 Vdc)	I_{IH}	–	–	1.0	–	–	1.0	μA
Strobe Disable Voltage ($V_{OL} \leq 0.4$ Vdc)	V_{IL}	–	–	0.4	–	–	0.4	Vdc
Strobe Enable Voltage ($V_{OH} \geq 2.4$ Vdc)	V_{IH}	3.5	–	6.0	3.5	–	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH}	–	20	–	–	20	–	ns
	t_{PHL}	–	40	–	–	40	–	
Strobe Response Time (Figure 2)	t_{so}	–	15	–	–	15	–	ns
	t_{sr}	–	6.0	–	–	6.0	–	
Total Power Supply Current, Both Comparators ($V_O \leq 0$)	I_{CC}	–	12.8	18	–	12.8	18	mAdc
	I_{EE}	–	11	14	–	11	14	
Total Power Consumption, Both Comparators	P_D	–	230	300	–	230	300	mW

*T_{low} = -55°C for MC1514, 0°C for MC1414
T_{high} = +125°C for MC1514, +75°C for MC1414

FIGURE 1 – PROPAGATION DELAY TIME

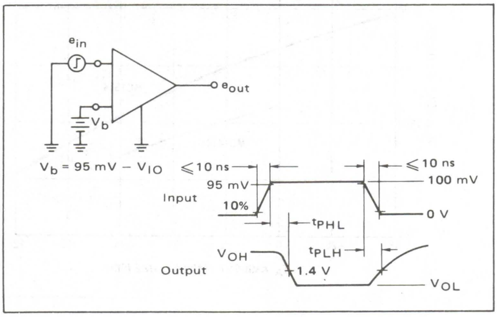
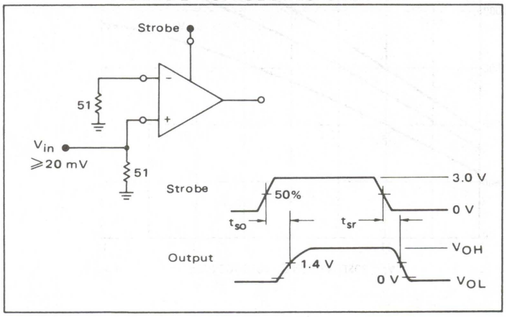


FIGURE 2 – STROBE RESPONSE TIME



TYPICAL CHARACTERISTICS
(Each Comparator)

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS

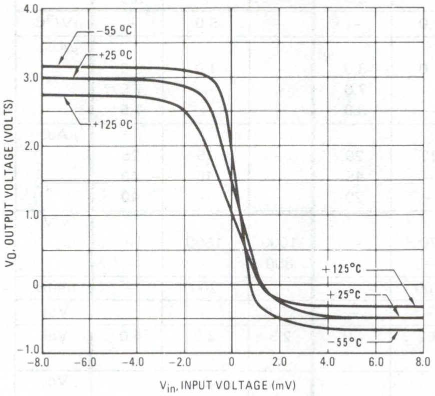


FIGURE 4 – INPUT OFFSET VOLTAGE versus TEMPERATURE

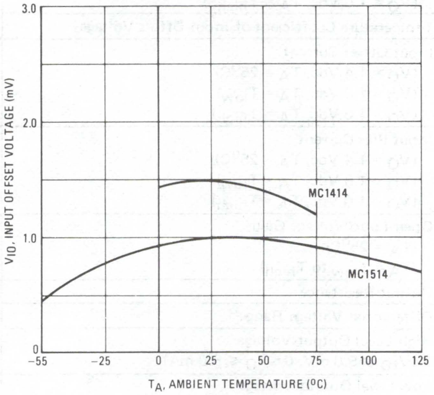


FIGURE 5 – INPUT OFFSET CURRENT versus TEMPERATURE

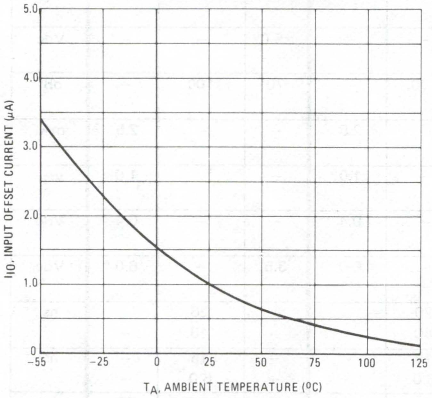


FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

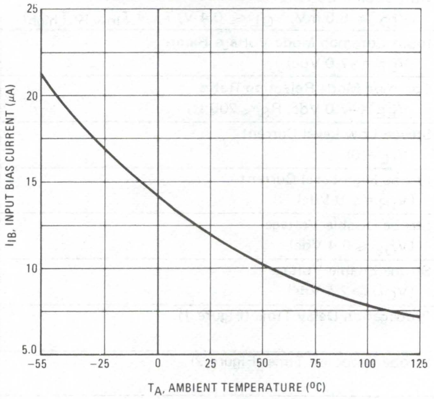


FIGURE 7 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

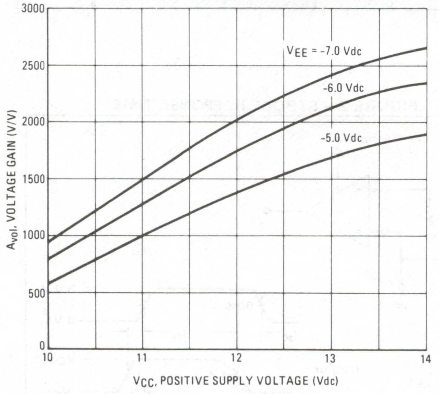


FIGURE 8 – VOLTAGE GAIN versus TEMPERATURE

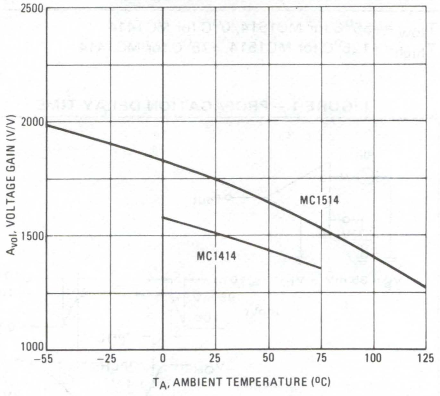


FIGURE 9 – RESPONSE TIME

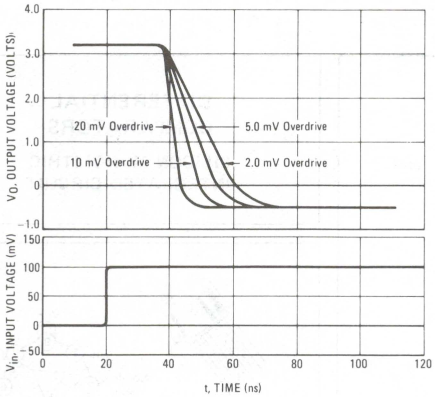


FIGURE 10 – POWER DISSIPATION versus TEMPERATURE

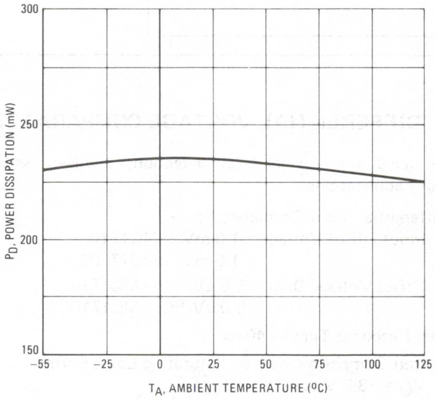


FIGURE 11 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

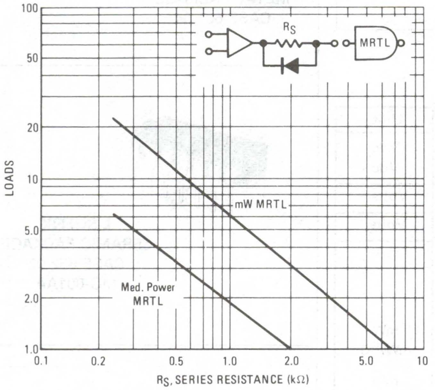


FIGURE 12 – SINK CURRENT versus TEMPERATURE

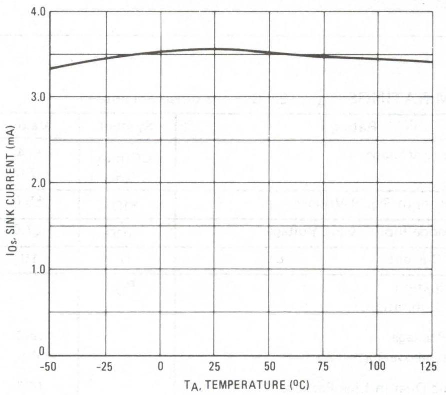
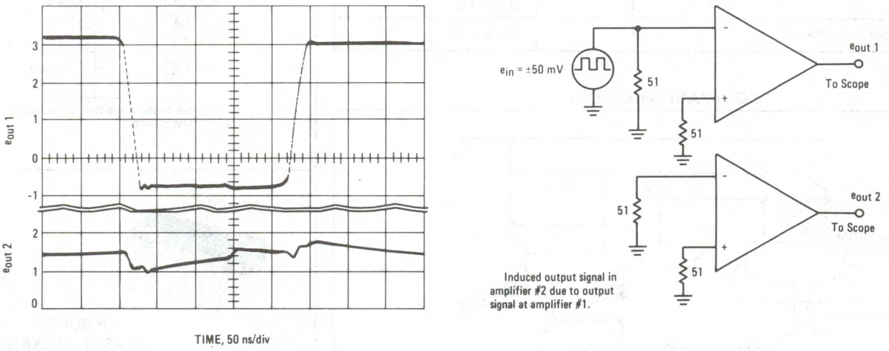


FIGURE 13 – CROSSTALK†



†Worst case condition shown – no load.

MC1710
MC1710C

MOTOROLA

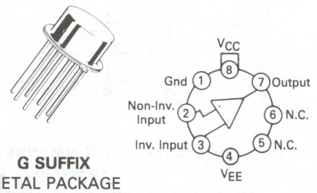
DIFFERENTIAL VOLTAGE COMPARATORS

. . . designed for use in level detection, low-level sensing, and memory applications.

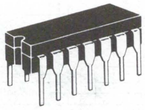
- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV – MC1710
  = 1.5 mV – MC1710C
  Offset Voltage Drift = 3.0 μV/°C – MC1710
  = 5.0 μV/°C – MC1710C
- Fast Response Time – 40 ns
- Output Compatible with all Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V (Typ)
- Low Output Impedance – 200 Ohms

DIFFERENTIAL COMPARATORS

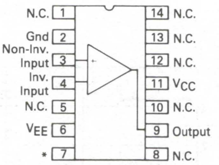
SILICON MONOLITHIC INTEGRATED CIRCUIT


V_{CC}
8
Gnd 1
7 Output
Non-Inv. Input 2
6 N.C.
Inv. Input 3
5 N.C.
4
V_{EE}

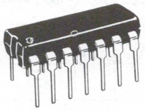
G SUFFIX
METAL PACKAGE
CASE 601-04



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA


N.C. 1
Gnd 2
Non-Inv. Input 3
Inv. Input 4
N.C. 5
V_{EE} 6
* 7
14 N.C.
13 N.C.
12 N.C.
11 V_{CC}
10 N.C.
9 Output
8 N.C.

*Connected to pin 6 via the substrate on some plastic units.

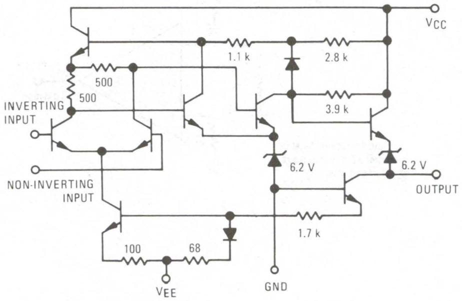


P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC1710C Only)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$ $V_{EE(max)}$	+14 -7.0	Vdc Vdc
Differential Input Signal Voltage	V_{ID}	±5.0	Volts
Common Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitations)	P_D		
Metal Package Derate above T_A = +25°C		680 4.6	mW mW/°C
Ceramic Dual In-Line Package Derate above T_A = +25°C		625 5.0	mW mW/°C
Operating Temperature Range MC1710 MC1710C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT


V_{CC}
1.1 k
2.8 k
500
500
3.9 k
INVERTING INPUT
NON-INVERTING INPUT
6.2 V
6.2 V
OUTPUT
1.7 k
100
68
V_{EE}
GND

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = –6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage		V_{IO}				mVdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	2.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = –55°C)	MC1710		–	–	3.0	
(V_O = 1.0 Vdc, T_A = +125°C	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	6.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	6.5	
Temperature Coefficient of Input Offset Voltage		$\Delta V_{IO}/\Delta T$	–	3.0	–	µV/°C
Input Offset Current		I_{IO}				µAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	3.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = –55°C)	MC1710		–	–	7.0	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	7.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	7.5	
Input Bias Current		I_{IB}				µAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	12	20	
	MC1710C		–	12	25	
(V_O = 1.8 Vdc, T_A = –55°C)	MC1710		–	–	45	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	20	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	40	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	40	
Voltage Gain		A_{vol}				V/V
(T_A = +25°C)	MC1710		1250	1700	–	
	MC1710C		1000	1700	–	
(T_A = T_{low} to T_{high}) (1)	MC1710		1000	–	–	
	MC1710C		800	–	–	
Output Resistance		r_o	–	200	–	Ohms
Differential Voltage Range		V_{ID}	±5.0	–	–	Vdc
Positive Output Voltage ($V_{ID} \geqslant 5.0$ mV, $0 \leqslant I_O \leqslant 5.0$ mA)		V_{OH}	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{ID} \geqslant -5.0$ mV)		V_{OL}	-1.0	-0.5	0	Vdc
Output Sink Current		I_{Os}				mAdc
($V_{ID} \geqslant -5.0$ mV, $V_O \leqslant 0$)	MC1710		2.0	2.5	–	
	MC1710C		1.6	2.5	–	
($V_{ID} \geqslant -5.0$ mV, $V_O \geqslant 0$, $T_A = T_{low}$)	MC1710		1.0	2.0	–	
	MC1710C		0.5	–	–	
Input Common-Mode Voltage Range (V_{EE} = –7.0 Vdc)		V_{ICR}	±5.0	–	–	Volts
Common-Mode Rejection Ratio		CMRR				dB
(V_{EE} = –7.0 Vdc, $R_S \leqslant 200$ Ohms)	MC1710		80	100	–	
	MC1710C		70	100	–	
Propagation Delay Time for Positive and Negative Going Input Pulse (V_{ID}= 5.0 mV + V_{IO})		t_{PLH} t_{PHL}	– –	40 35	– –	ns
Power Supply Current						mAdc
($V_O \leqslant 0$)		I_{D+} I_{D-}	– –	6.4 5.5	9.0 7.0	
Power Consumption		P_D	–	115	150	mW

(1) T_{low} = -55°C for MC1710, 0°C for MC1710C
T_{high} = +125°C for MC1710, +75°C for MC1710C

TYPICAL CHARACTERISTICS

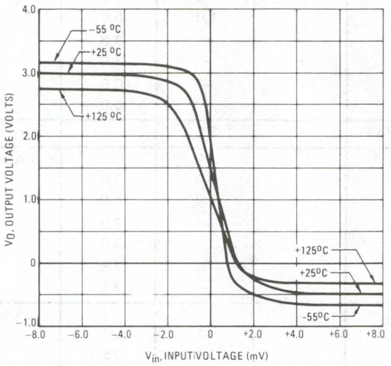


FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

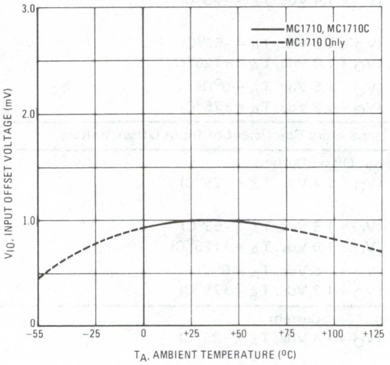


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

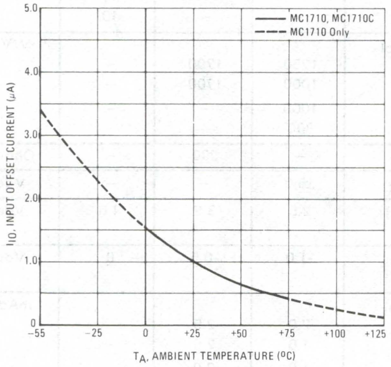


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

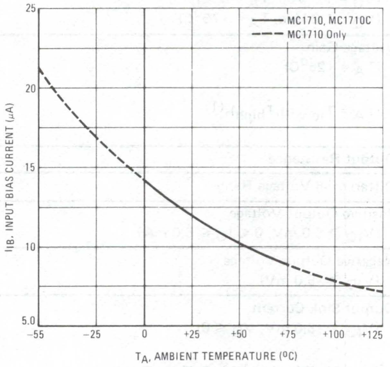


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

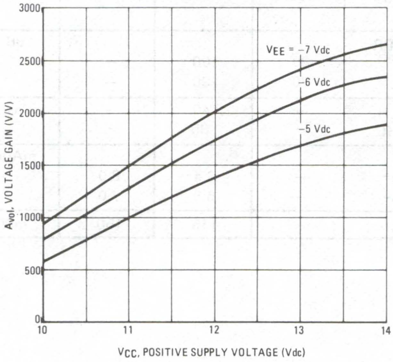


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

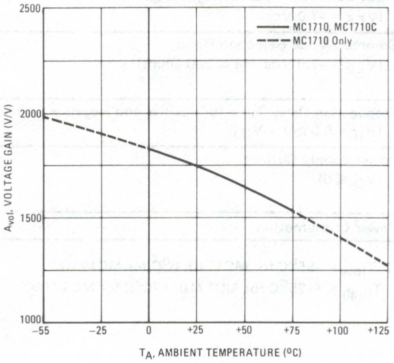


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

TYPICAL CHARACTERISTICS (Continued)

FIGURE 7 – RESPONSE TIME

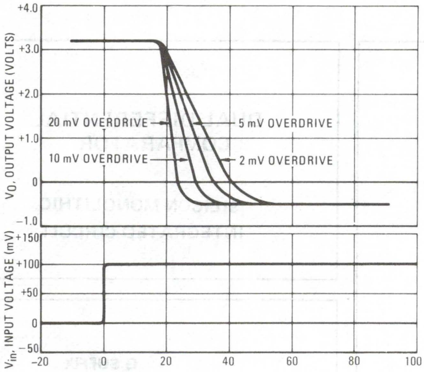


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

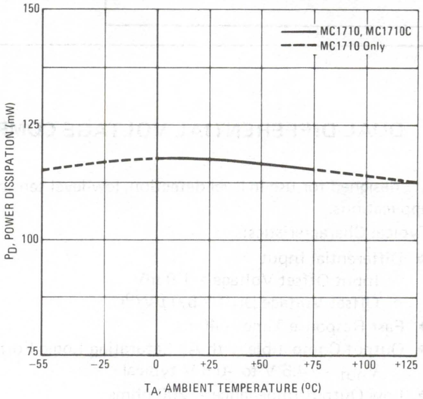


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

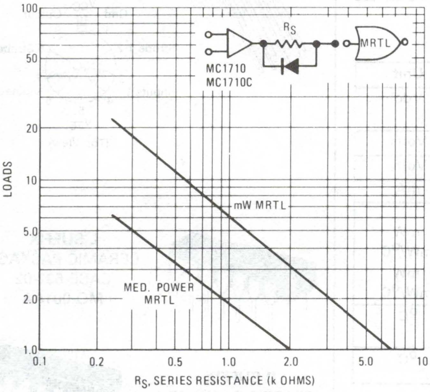
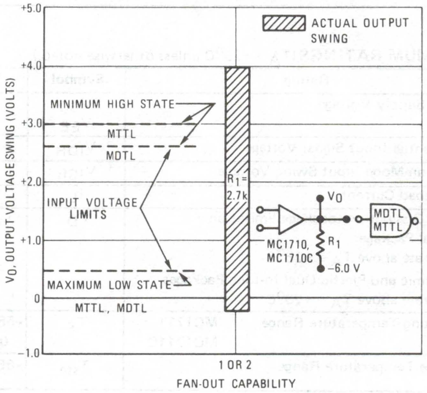


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MC1711
MC1711C

MOTOROLA

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

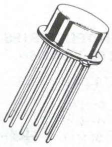
Typical Characteristics:

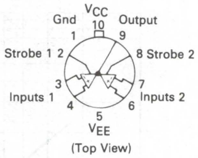
- Differential Input
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/°C
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance — 200 ohms

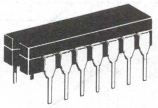
DUAL DIFFERENTIAL COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 603-04
TO-100

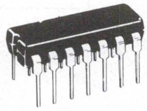


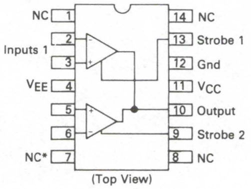

Gnd
VCC
10
Output
1
9
Strobe 1 2
8 Strobe 2
3
7
Inputs 1
4
6
Inputs 2
5
VEE
(Top View)



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC1711C only)



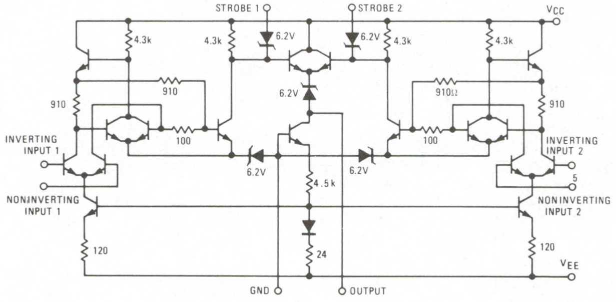

NC 1
Inputs 1
2
3
VEE 4
5
6
NC* 7
14 NC
13 Strobe 1
12 Gnd
11 VCC
10 Output
9 Strobe 2
8 NC
(Top View)

*Connected to pin 4 via the substrate on some plastic units.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Input Signal Voltage	V_{IDR}	±5.0	Volts
Common-Mode Input Swing Voltage	V_{ICR}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Package Derate above T_A = +25°C Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25°C	P_D	 680 4.6 625 5.0	 mW mW/°C mW mW/°C
Operating Temperature Range MC1711 MC1711C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC


STROBE 1
STROBE 2
VCC
4.3k
4.3k
6.2V
6.2V
4.3k
4.3k
910
6.2V
910Ω
910
910
INVERTING INPUT 1
100
100
INVERTING INPUT 2
6.2V
6.2V
4.5k
5
NONINVERTING INPUT 1
NONINVERTING INPUT 2
120
24
120
VEE
GND
OUTPUT

ELECTRICAL CHARACTERISTICS (each comparator) (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1711 Min	MC1711 Typ	MC1711 Max	MC1711C Min	MC1711C Typ	MC1711C Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_{ICR} = 0 Vdc, T_A = +25°C)		–	1.0	3.5	–	1.0	5.0	
(V_{ICR} ≠ 0 Vdc, T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(V_{ICR} = 0 Vdc, T_A = T_{low} to T_{high}*)		–	–	4.5	–	–	6.0	
(V_{ICR} ≠ 0 Vdc, T_A = T_{low} to T_{high})		–	–	6.0	–	–	10	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	5.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	0.5	10	–	0.5	15	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	20	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	25	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	20	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	25	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	25	75	–	25	100	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	150	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	150	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	150	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	150	
Voltage Gain	A_{vol}							V/V
(T_A = +25°C)		700	1500	–	700	1500	–	
(T_A = T_{low} to T_{high})		500	–	–	500	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geqslant 10$ mVdc, $0 \leqslant I_O \leqslant 5.0$ mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Low Level Output Voltage ($V_{ID} \geqslant -10$ mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level ($V_{strobe} \leqslant 0.3$ Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geqslant -10$ mV, $V_O \geqslant 0$)	I_{Os}	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Input Common-Mode Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Volts
Response Time (V_b = 5.0 mV + V_{IO})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current ($V_O \leqslant 0$ Vdc)	I_{CC} I_{EE}	– –	8.6 3.9	– –	– –	8.6 3.9	– –	mAdc
Power Consumption		–	130	200	–	130	200	mW

*T_{low} = -55°C for MC1711, 0°C for MC1711C
T_{high} = +125°C for MC1711, +75°C for MC1711C

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

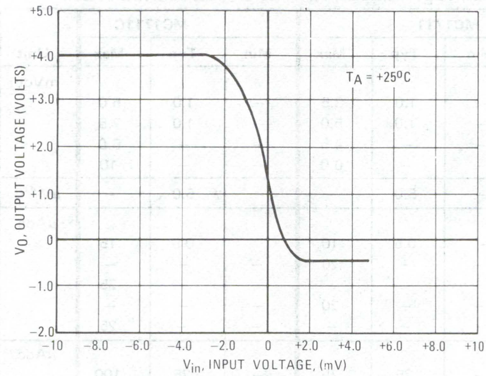


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

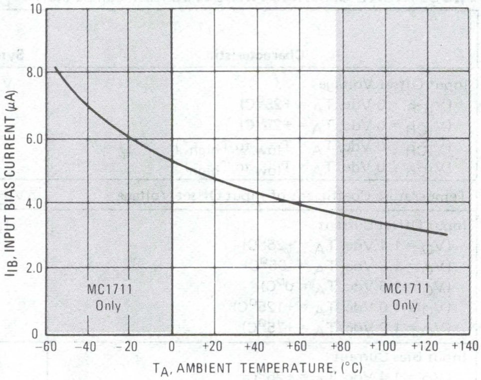


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

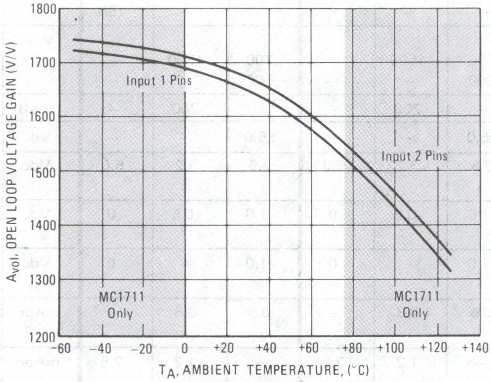


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

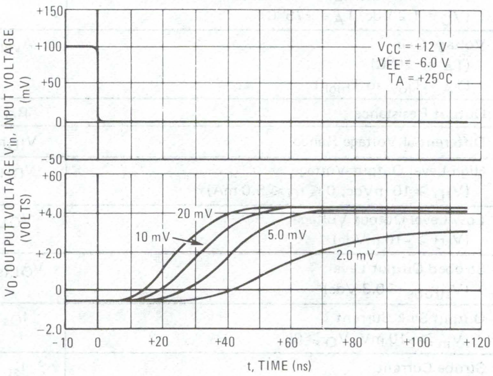


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

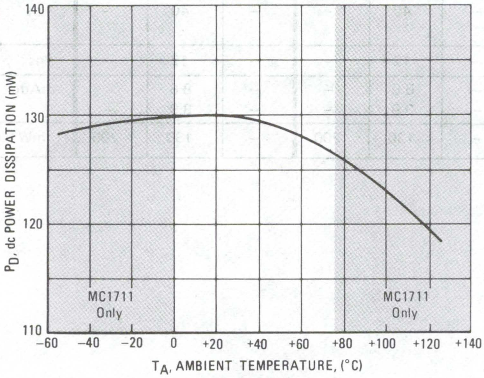


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

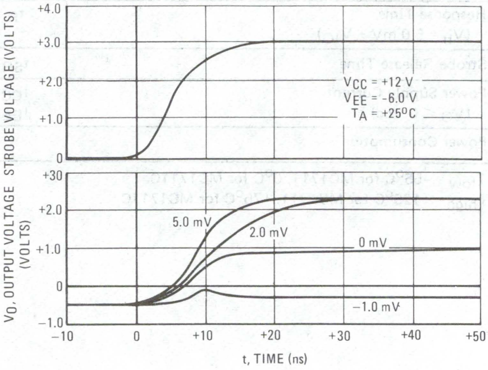


FIGURE 7 – COMMON-MODE PULSE RESPONSE

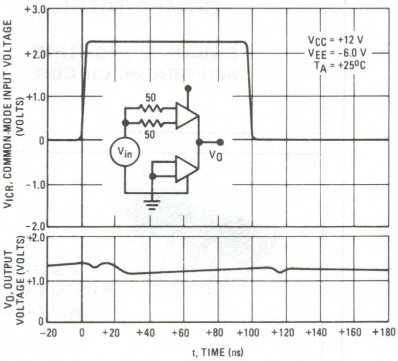


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

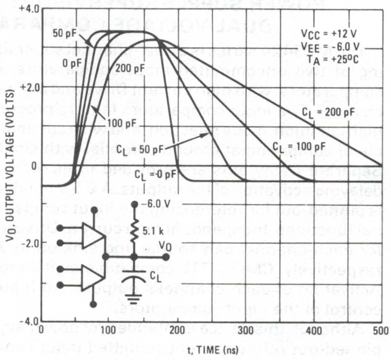


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

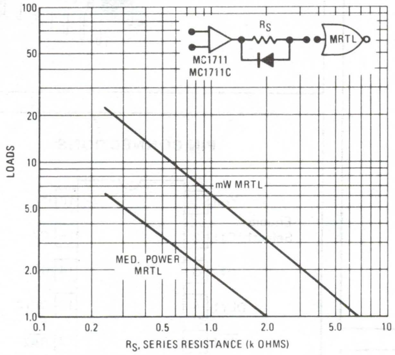
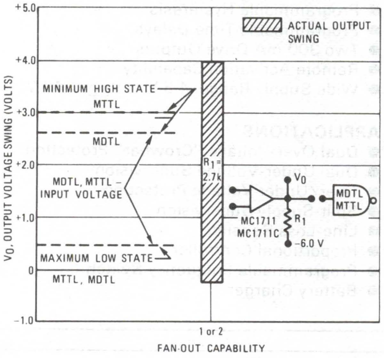


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



MC3424,A
MC3524,A
MC3324,A

MOTOROLA

Advance Information

POWER SUPPLY SUPERVISORY CIRCUIT/ DUAL-VOLTAGE COMPARATOR

The MC3424 series is a dual-channel supervisory circuit, consisting of two uncommitted input comparators, a reference, output comparators, with high current Drive and Indicator outputs for each channel. The input comparators feature programmable hysteresis, high common-mode rejection, and wide common-mode range, capable of comparing at ground potential with single-supply operation. Separate Delay pins are provided to increase noise immunity by delaying activation of the outputs. A 2.5 V bandgap voltage reference is pinned-out for referencing the input comparators, or other external functions. Independent high current Drive and Indicator outputs for each channel can source and sink up to 300 mA and 30 mA respectively. CMOS/TTL compatible digital inputs provide Remote Activation of each channel's outputs. An Input Enable pin allows control of the input comparators.

Although this device is intended for power supply supervision, the pinned-out reference, uncommitted input comparators, and many other features, enable the MC3424 series to be utilized for a wide range of applications.

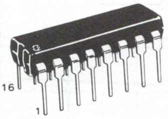
- Pinned-Out 2.5 V Reference
- Wide Common-Mode Range
- Programmable Hysteresis
- Programmable Time Delays
- Two 300 mA Drive Outputs
- Remote Activation Capability
- Wide Supply Range: 4.5 V ⩽ V_{CC} ⩽ 40 V

APPLICATIONS

- Dual Over-Voltage "Crowbar" Protection
- Dual Under-Voltage Supervision
- Over/Under Voltage Protection
- Split-Supply Supervision
- Line-Loss Sensing
- Proportional Controller
- Programmable Frequency Switch
- Battery Charger

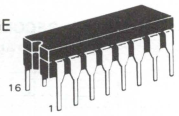
POWER SUPPLY SUPERVISORY CIRCUIT/DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

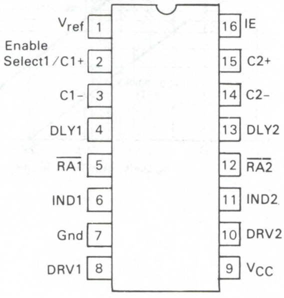


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

L SUFFIX
CERAMIC PACKAGE
CASE 620-02



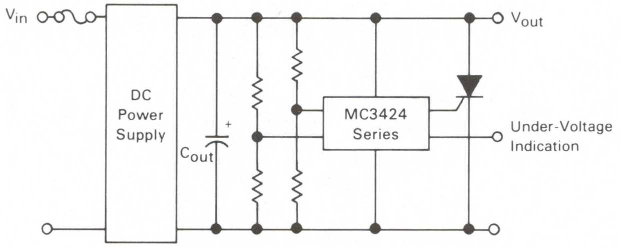
PIN CONNECTIONS



(Top View)

TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



ORDERING INFORMATION

Device	Temperature Range	Package
MC3524L, AL	−55 to +125°C	Ceramic DIP
MC3324L, AL	−40 to +85°C	Ceramic DIP
MC3324P, AP		Plastic DIP
MC3424L, AL	0 to +70°C	Ceramic DIP
MC3424P, AP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Differential Voltage Range	V_{IDR}	±40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Input Enable Voltage Range	V_{IE}	-0.3 to +40	Vdc
Remote Activation Input Voltage Range	V_{RA}	-0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Reference Short-Circuit Current	$I_{OS(ref)}$	Internally Limited	mA
Power Dissipation and Thermal Characteristics Ceramic Package Maximum Power Dissipation @ $T_A = 95°C$ Thermal Resistance Junction to Air Plastic Package Maximum Power Dissipation @ $T_A = 70°C$ Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1000 80 1000 80	 mW °C/W mW °C/W
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Operating Ambient Temperature Range MC3524, MC3524A MC3324, MC3324A MC3424, MC3424A	T_A	 -55 to +125 -40 to +85 0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +175 -55 to +150	°C

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ V_{CC} ≤ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage $V_{CC} = 15V$; $I_L = 0$ mA $T_A = 25°C$ T_{low} to T_{high} (Note 1)	V_{ref}	 2.475 2.45	 2.5 2.5	 2.525 2.55	 2.4 2.33	 2.5 2.5	 2.6 2.63	Vdc
Line Regulation 4.5 V ≤ V_{CC} ≤ 40 V; $I_L = 0$ mA; $T_J = 25°C$	Reg_{line}	—	7.0	15	—	7.0	15	mV
Load Regulation 0 mA ≤ I_L ≤ 10 mA; $V_{CC} = 15$ V; $T_J = 25°C$	Reg_{load}	—	4.0	12	—	4.0	12	mV
Output Short-Circuit Current ($T_A = 25°C$)	$I_{OS(ref)}$	—	23	—	—	23	—	mA
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	4.5	—	40	Vdc
Power Supply Current $V_{CC} = 40$ V; $T_A = 25°C$; No Output Loads $V_{C1-}, V_{C2-} = V_{CC}$; $V_{C1+}, V_{C2+} = 0$ V	$I_{CC(off)}$	—	12	15	—	12	15	mA
$V_{C1+}, V_{C2+} = V_{CC}$; $V_{C1-}, V_{C2-} = 0$ V	$I_{CC(on)}$	—	27	32	—	27	32	mA

NOTES:

(1) T_{low} = -55°C for MC3524, MC3524A
= -40°C for MC3324, MC3324A
= 0°C for MC3424, MC3424A

T_{high} = +125°C for MC3524, MC3524A
= +85°C for MC3324, MC3324A
= +70°C for MC3424, MC3424A

(2) The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 300 mV. The upper functional limit of the common-mode voltage range is typically V_{CC} -1.4 volts, but either or both inputs can go to 40 volts, independent of V_{CC}, without device destruction.

(3) The $V_{th(ES1)}$ limits are approximately 0.9 times the V_{ref} limits over the applicable temperature range.

(4) The $V_{th(OC)}$ limits are approximately the V_{ref} limits over the applicable temperature range.

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{CC} ≤ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT SECTION								
Input Offset Voltage	V_{IO}							mV
T_A = 25°C		—	±3.0	±8.0	—	±5.0	±10	
T_{low} to T_{high} (Note 1)		—	±3.0	±12	—	±5.0	±15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		—	±3.0	±25	—	±3.0	±25	
T_{low} to T_{high} (Note 1)		—	±3.0	±250	—	±3.0	±250	
Input Bias Current	I_{IB}							nA
T_A = 25°C		—	50	250	—	50	250	
T_{low} to T_{high} (Note 1)		—	500	1000	—	500	1000	
Comparator Input Functional Common Mode Range (T_A = 25°C, Note 2)	V_{ICR}	-0.1	V_{CC}-1.4	—	-0.1	V_{CC}-1.4	—	V
Hysteresis Activation Voltage V_{CC} = 15 V; V_{C1+}, V_{C2+} = V_{CC}; T_A = 25°C	$V_{H(act)}$							V
I_H = 10%		—	1.2	—	—	1.2	—	
I_H = 90%		—	1.4	—	—	1.4	—	
Hysteresis Current V_{CC} = 15 V; V_{C1-}, V_{C2-} = 2.5 V; V_{C1+}, V_{C2+} = V_{CC}; T_A = 25°C	I_H	10	12.5	15	9.0	12.5	16	µA
Common Mode Rejection Ratio	CMRR	60	72	—	60	72	—	dB
Power Supply Rejection Ratio	PSRR	—	95	—	—	95	—	dB
Input Enable Threshold (Pin 16; Note 3)	$V_{th(IE)}$	0.9	1.4	1.9	0.9	1.4	1.9	V
Input Enable Current (Pin 16)								µA
$V_{IL(IE)}$ = 0 V	$I_{IL(IE)}$	—	-0.5	-2.5	—	-0.5	-2.5	
$V_{IH(IE)}$ = 40 V	$I_{IH(IE)}$	—	0.05	1.0	—	0.05	1.0	
Enable Select 1 Threshold Voltage (Pin 2)	$V_{th(ES1)}$	2.2	2.25	2.3	2.1	2.25	2.4	V
Delay Pin Voltage (I_{DLY} = 0 mA)								V
Low State	$V_{OL(DLY)}$	—	0.2	0.5	—	0.2	0.5	
High State	$V_{OH(DLY)}$	V_{CC}-0.5	V_{CC}-0.15	—	V_{CC}-0.5	V_{CC}-0.15	—	
Delay Pin Source Current V_{CC} = 15 V; V_{DLY1}, V_{DLY2} = 0 V	$I_{DLY(source)}$	150	200	250	140	200	260	µA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY1}, V_{DLY2} = 2.5 V	$I_{DLY(sink)}$	1.8	3.0	—	1.8	3.0	—	mA
OUTPUT SECTION								
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	200	300	—	mA
Drive Output V (I_{DRV} = 100 mA; T_A = 25°C)	$V_{OH(DRV)}$	V_{CC}-2.5	V_{CC}-2.0	—	V_{CC}-2.5	V_{CC}-2.0	—	V
Drive Output Leakage Current (V_{DRV} = 0 V)	$I_{DRV(leak)}$	—	15	200	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	—	2.0	—	A/µS
Drive Output Transient Rejection (T_A = 25°C) V_{CC} = 0 V to 15 V at dV/dt = 200 V/µs; V_{C1-}, V_{C2-} = V_{ref}; V_{C1+}, V_{C2+} = 0 V	$I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	—	25	200	nA
Output Comparator Threshold V (Note 4)	$V_{th(OC)}$	2.45	2.5	2.55	2.33	2.5	2.63	V
Remote Activation Threshold Voltage	$V_{th(RA)}$	1.3	1.4	1.5	1.1	1.4	1.7	V
Remote Activation Current								µA
$V_{IL(RA)}$ = 0 V	$I_{IL(RA)}$	—	-100	-250	—	-100	-250	
$V_{IH(RA)}$ = 40 V	$I_{IH(RA)}$	—	70	250	—	70	250	
Propagation Delay (V_{CC} = 15 V; T_A = 25°C)								
Input to Drive Output 100 mV Overdrive, C_{DLY} = 0 µF	$t_{PLH(IN/DRV)}$	—	1.0	—	—	1.0	—	µs
Remote Activation to Drive Output 1.4 V Overdrive (2.5 V to 0 V Step)	$t_{PLH(RA/DRV)}$	—	600	—	—	600	—	ns

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

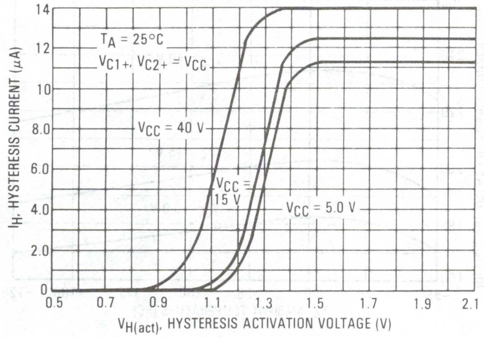


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

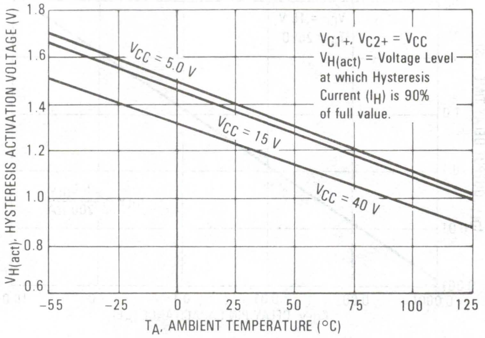


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

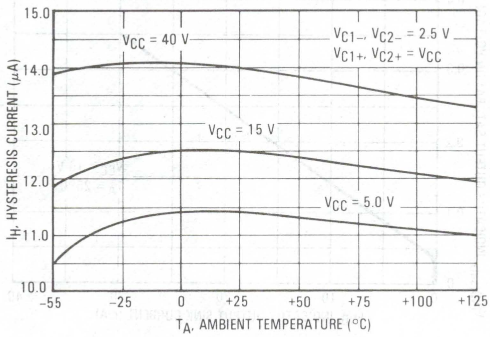


FIGURE 4 — REFERENCE VOLTAGE CHANGE versus OUTPUT CURRENT

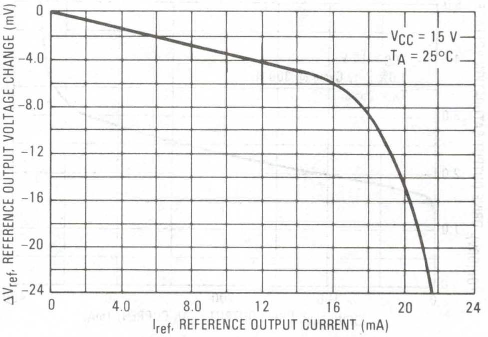


FIGURE 5 — REFERENCE VOLTAGE CHANGE versus TEMPERATURE

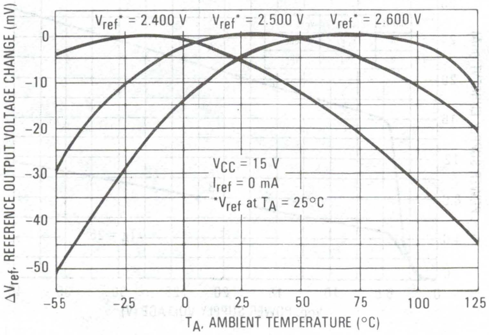


FIGURE 6 — REFERENCE SHORT-CIRCUIT CURRENT versus TEMPERATURE

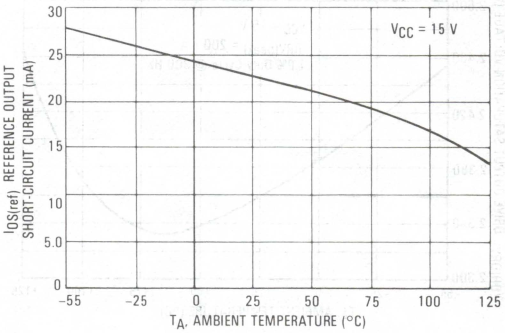


FIGURE 7 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

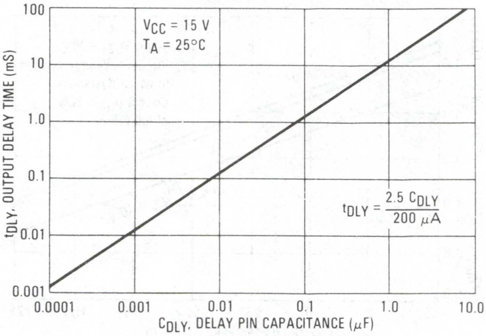


FIGURE 8 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

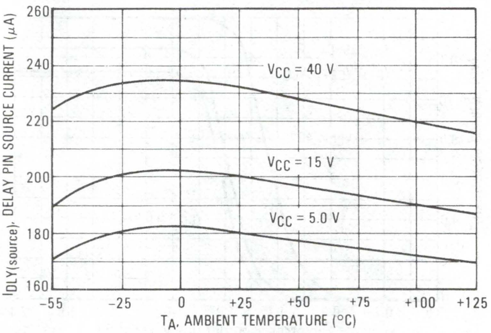


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

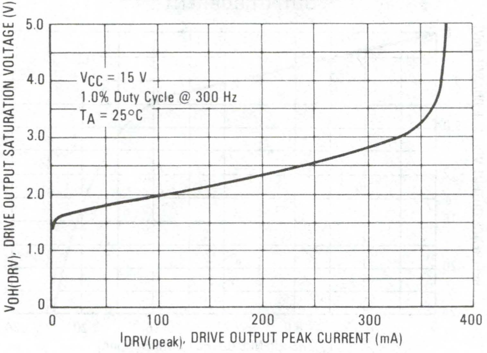


FIGURE 10 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

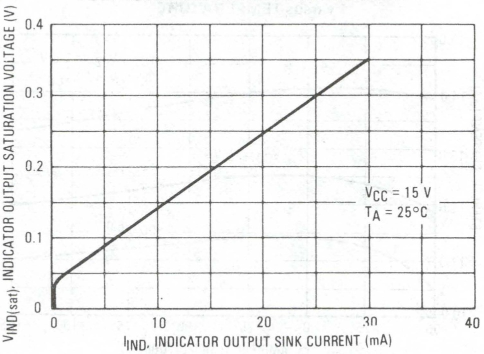


FIGURE 11 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

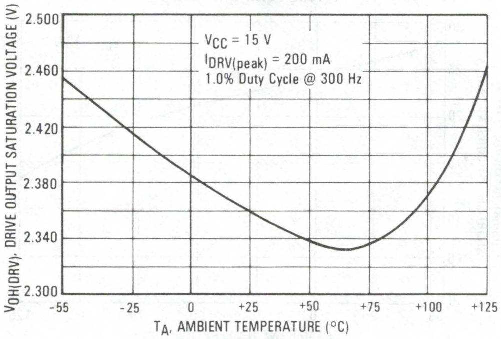
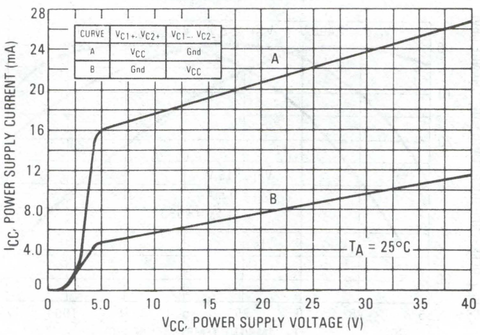
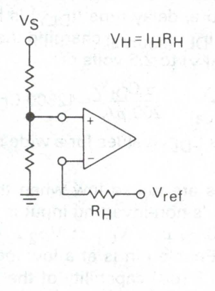


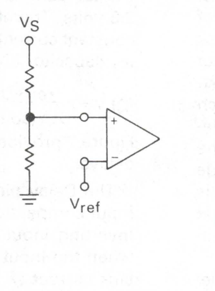
FIGURE 12 — POWER SUPPLY CURRENT versus VOLTAGE



CURVE	V_{C1+}, V_{C2+}	V_{C1-}, V_{C2-}
A	V_{CC}	Gnd
B	Gnd	V_{CC}

FIGURE 13 — THE COMPLETE VOLTAGE SENSE CAPABILITY OF THE INPUT COMPARATORS, WITH OR WITHOUT PROGRAMMABLE HYSTERESIS.

<table>
<tr><th rowspan="3"></th><th colspan="4">VOLTAGE SENSE (V_S)</th></tr>
<tr><th colspan="2">OVER</th><th colspan="2">UNDER</th></tr>
<tr><th>WITH HYSTERESIS</th><th>WITHOUT HYSTERESIS</th><th>WITH HYSTERESIS</th><th>WITHOUT HYSTERESIS</th></tr>
<tr><td>$V_S > V_{ref}$</td>
<td>
V_S
$V_H = I_H R_H$
+
−
V_{ref}
R_H

</td>
<td>
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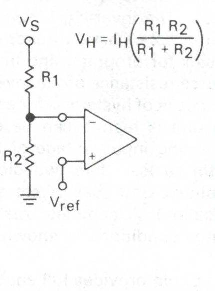
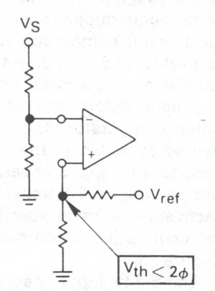
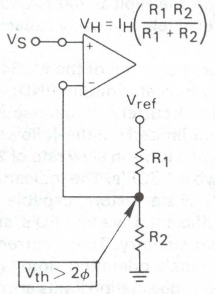
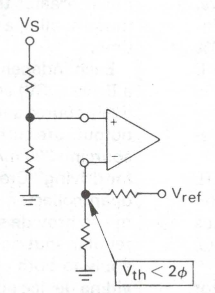
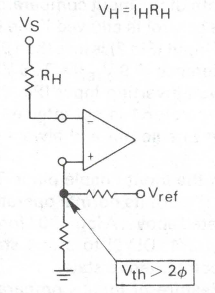
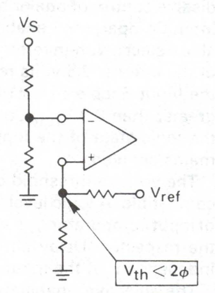
<td>
V_S
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
R_1
−
+
R_2
V_{ref}

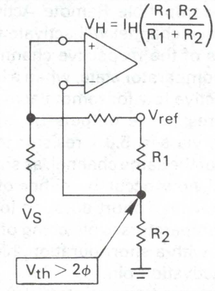
</td>
<td>
V_S
−
+
V_{ref}
$V_{th} < 2\phi$

</td></tr>
<tr><td>$V_S \leqslant V_{ref}$
$V_S \geqslant 2\phi$*</td>
<td>
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
V_S
+
−
V_{ref}
R_1
R_2
$V_{th} > 2\phi$

</td>
<td>
V_S
+
−
V_{ref}
$V_{th} < 2\phi$

</td>
<td>
$V_H = I_H R_H$
V_S
R_H
−
+
V_{ref}
$V_{th} > 2\phi$

</td>
<td>
V_S
−
+
V_{ref}
$V_{th} < 2\phi$

</td></tr>
<tr><td>$V_S < 2\phi$*
$V_S \geqslant 0$ V</td>
<td>
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
+
−
V_{ref}
R_1
V_S
R_2
$V_{th} > 2\phi$

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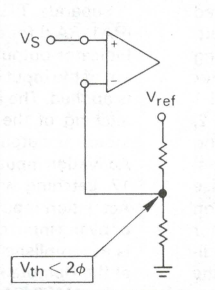
<td>
V_S
+
−
V_{ref}
$V_{th} < 2\phi$

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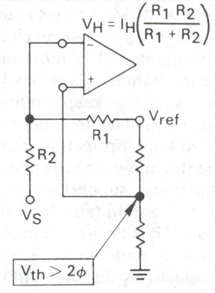
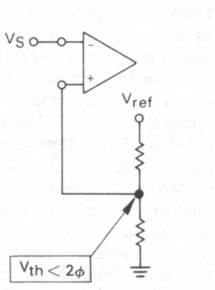
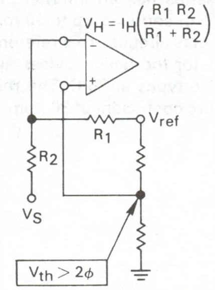
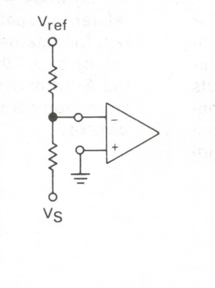
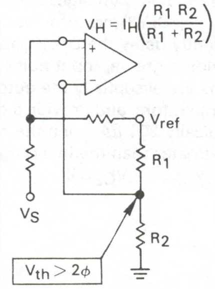
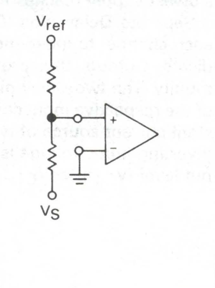
<td>
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
−
+
V_{ref}
R_1
R_2
V_S
$V_{th} > 2\phi$

</td>
<td>
V_S
−
+
V_{ref}
$V_{th} < 2\phi$

</td></tr>
<tr><td>$V_S < 0$ V</td>
<td>
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
−
+
V_{ref}
R_1
R_2
V_S
$V_{th} > 2\phi$

</td>
<td>
</td>
<td>
$V_H = I_H \left(\frac{R_1 R_2}{R_1 + R_2}\right)$
+
−
V_{ref}
R_1
R_2
V_S
$V_{th} > 2\phi$

</td>
<td>
</td></tr>
</table>

*$2\phi \simeq 1.1$ Volts at $T_J = 25°C$

CIRCUIT DESCRIPTION

The MC3424 series is a high current output, dual channel power supply supervisory circuit. Basic circuit configuration is shown in Figure 29. Each channel features a true differential input comparator with a common-mode range from ground potential to $V_{CC} - 1.4$ volts, with single supply operation. The inverting inputs of each input comparator (C1−, C2−) have a feedback activated 12.5 μA current sink for programming input comparator hysteresis. Source resistance of the inverting inputs determines the amount of hysteresis for each input comparator. The hysteresis feature can be defeated by reducing the inverting input voltage of the respective input comparator to less than two diode drops ($2\ \phi \simeq 1.1$ volts) above Gnd (See Hysteresis Activation Voltage specification). A complete matrix of various input comparator conditions is shown in Figure 13.

The digital Input Enable (IE) pin provides full enable/disable control of one or both of the input comparators. Input Comparator 1 enable control is allowed if the Enable Select1/Non-Inverting Input (Pin 2) is less than 90% of the internal 2.5 volts reference ($0.9\ V_{ref} \cong 2.25$ V). If the Input Enable Select1/Non-Inverting Input (Pin 2) is greater than $0.9\ V_{ref}$, Comparator 1 is not affected by the logic state of the Input Enable pin and always remains enabled.

The voltage threshold of the Input Enable pin is TTL compatible. A logic level "1" permits normal operation of input comparators, as stated above. A logic "0" forces the respective Delay pin (DLY1, DLY2) to a low state, independent of the input comparator's state.

The selective enabling feature of Input Comparator 1 is directly applicable when the MC3424 series is used as an over- and under-voltage supervisory circuit, where channel 2 (Input Comparator 2) is monitoring under-voltage conditions, and channel 1 is utilized for over-voltage protection. The ability to keep channel 1 (Input Comparator 1) active, while disabling channel 2, provides immediate over-voltage protection during power supply turn-on, while the under-voltage channel (2) can be disabled during the power supply turn-on rise time to the regulated level, preventing false indication of an under-voltage condition. If it is desired to monitor two independent voltages for an under-voltage condition, both channels can be selectively disabled until the slowest supply reaches its regulated voltage.

Separate Delay pins (DLY1, DLY2) are provided for each channel to independently delay the Drive and Indicator Outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source of typically 200 μA when the non-inverting input voltage is greater than the inverting input level ($V_{C1+} > V_{C1-}$; $V_{C2+} > V_{C2-}$).

A capacitor (C_{DLY}) tied to these Delay pins will establish a predictable delay time (t_{DLY}) of the Drive and Indicator outputs for the respective channel. The Delay pins are internally tied to the non-inverting input of Output Comparators 1 and 2, which are referenced to 2.5 volts. Therefore, delay time (t_{DLY}) is based on the constant current $I_{DLY(source)}$ charging the external delay capacitor (C_{DLY}) to 2.5 volts or;

$$t_{DLY} = \frac{V_{ref}\ C_{DLY}}{I_{DLY(source)}} = \frac{2.5\ C_{DLY}}{200\ \mu A} = 12500\ C_{DLY}.$$

Figure 7 provides C_{DLY} values for a wide range of time delays.

The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input ($V_{C1+} < V_{C1-}$; $V_{C2+} < V_{C2-}$), or when the Input Enable pin is at a low logic level. The sink current ($\geqslant 1.8$ mA) capability of the Delay pins is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

Each independent channel of the MC3424 series has a Drive (DRV) and Indicator output (IND) which respectively source and sink current simultaneously. The Drive outputs are current-limited emitter-followers capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Indicator outputs are open collector, NPN transistors, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or regular shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

Separate TTL-compatible Remote Activation inputs ($\overline{RA1}$, $\overline{RA2}$) for each channel will activate the Drive and Indicator outputs of the respective channel, independent of the input comparator state, when a low logic level is applied. The active low for remote activation permits latching of the respective outputs by connecting the Indicator output, via a $\leqslant 5.0$ k resistor to the Remote Activation input of the same channel, as shown in Figure 17. Latching will now occur by either of the Remote Activation inputs with a short duration low logic level, or by the input comparators. Unlatching of each channel is accomplished with a short duration, high logic level at the Remote Activation pin.

The MC3424 series has an internal 2.5 V bandgap reference capable of sourcing up to 10 mA of load current for external bias circuits. This reference has an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

CROWBAR SCR CONSIDERATIONS

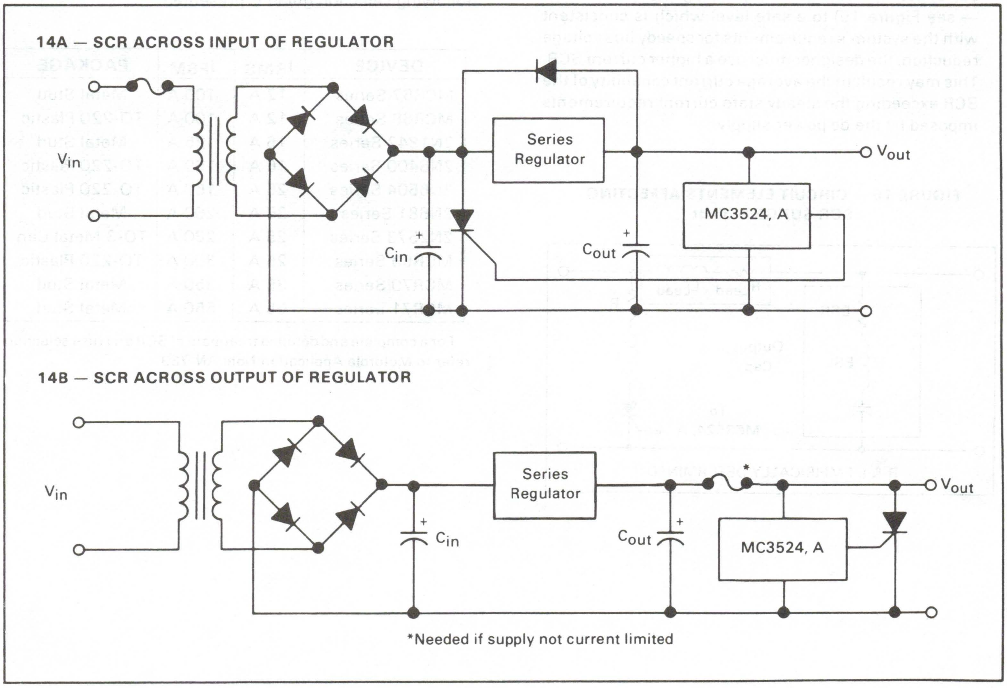
Referring to Figure 14, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 14A, the supply's input filter capacitors. This surge current is illustrated in Figure 15, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

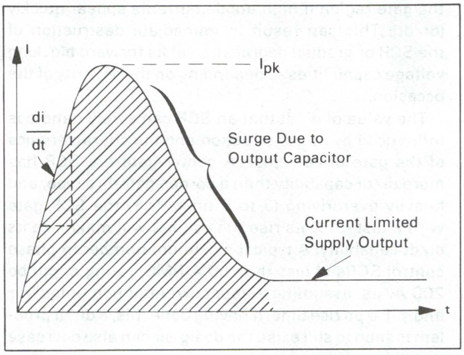
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 16. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 14 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

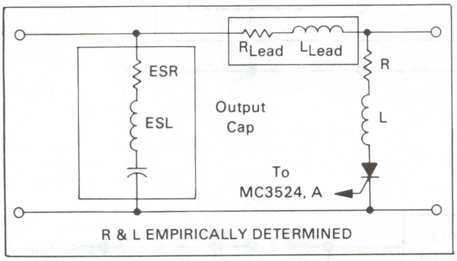
FIGURE 15 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 16) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 16 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 14A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 14B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

APPLICATIONS INFORMATION

FIGURE 17 — OVERVOLTAGE PROTECTION OF SPLIT SUPPLIES WITH DELAY AND LATCHED-FAULT INDICATION.

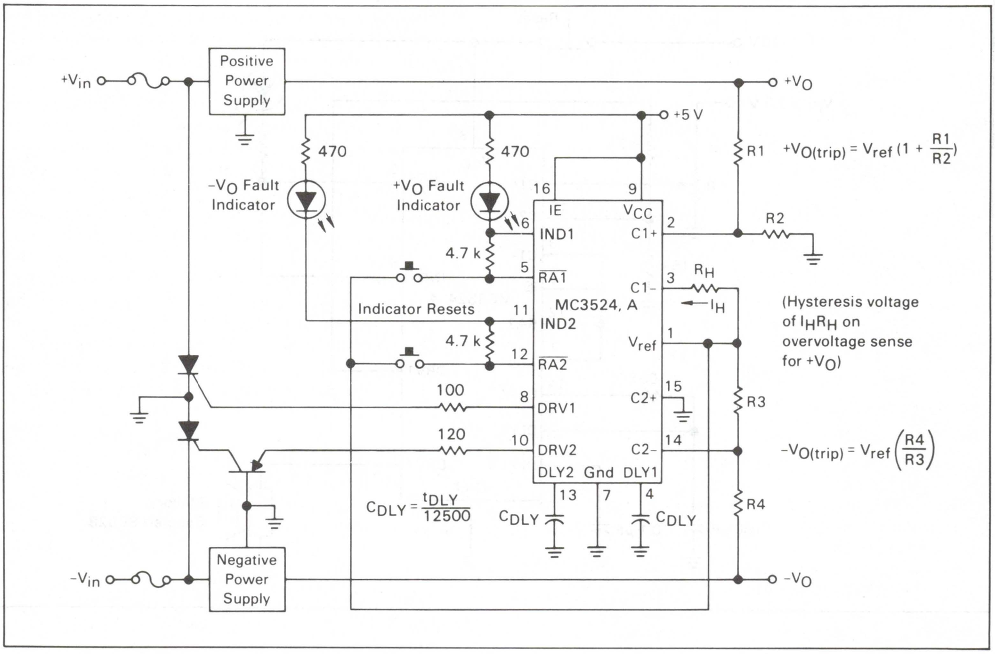

+Vin
Positive Power Supply
+VO
+5 V
470
470
R1
+VO(trip) = Vref (1 + R1/R2)
−VO Fault Indicator
+VO Fault Indicator
16
9
IE
VCC
6
IND1
C1+
2
R2
4.7 k
5
RA1
C1−
3
RH
IH
MC3524, A
Indicator Resets
11
IND2
(Hysteresis voltage of IHRH on overvoltage sense for +VO)
4.7 k
12
RA2
Vref
1
100
8
DRV1
C2+
15
R3
120
10
DRV2
C2−
14
−VO(trip) = Vref (R4/R3)
DLY2
Gnd
DLY1
13
7
4
CDLY = tDLY/12500
CDLY
CDLY
R4
−Vin
Negative Power Supply
−VO

FIGURE 18 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

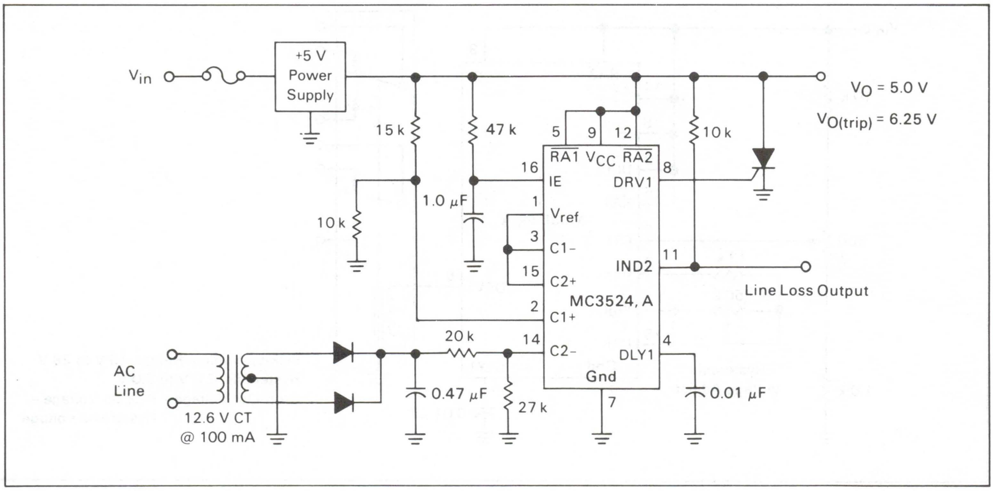

Vin
+5 V Power Supply
VO = 5.0 V
VO(trip) = 6.25 V
15 k
47 k
5
9
12
10 k
RA1
VCC
RA2
16
IE
8
DRV1
1.0 µF
1
Vref
10 k
3
C1−
15
C2+
11
IND2
Line Loss Output
2
MC3524, A
C1+
20 k
14
C2−
4
DLY1
AC Line
Gnd
0.47 µF
27 k
7
0.01 µF
12.6 V CT @ 100 mA

FIGURE 19 — LATCHING OVERVOLTAGE SENSING CIRCUIT WITH INTERMITTENT AUDIO ALARM

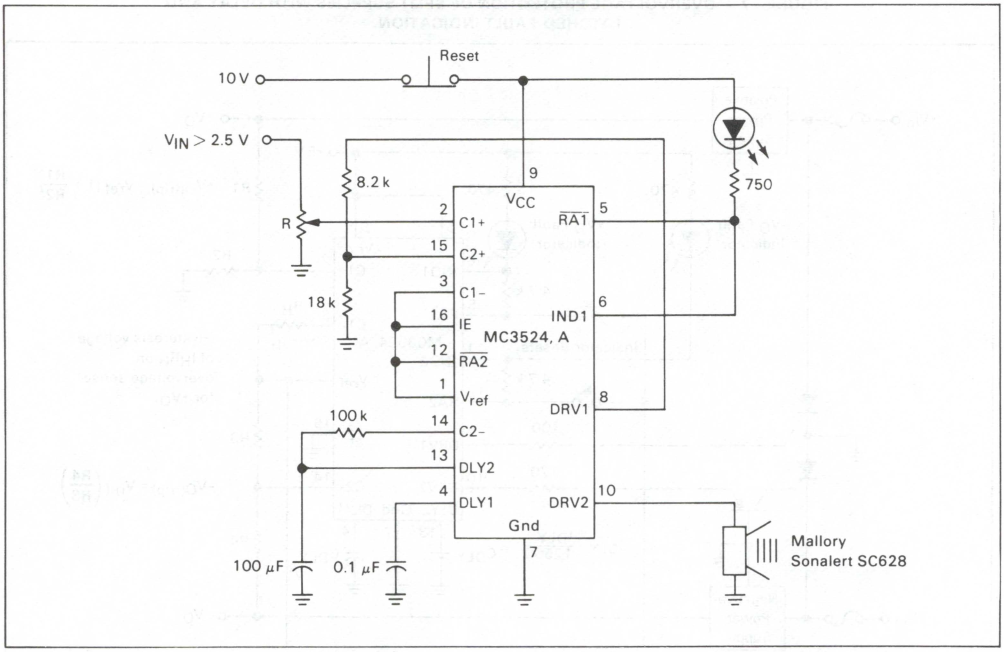
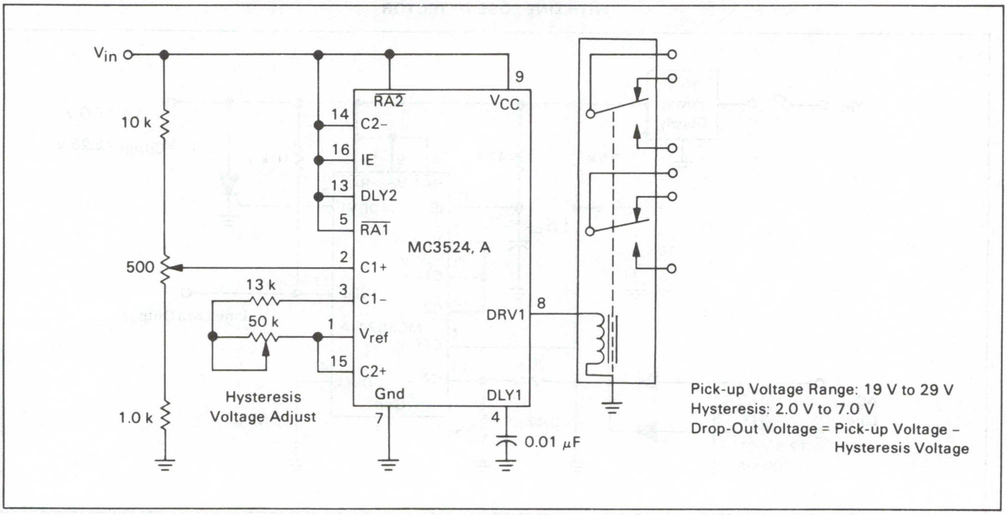
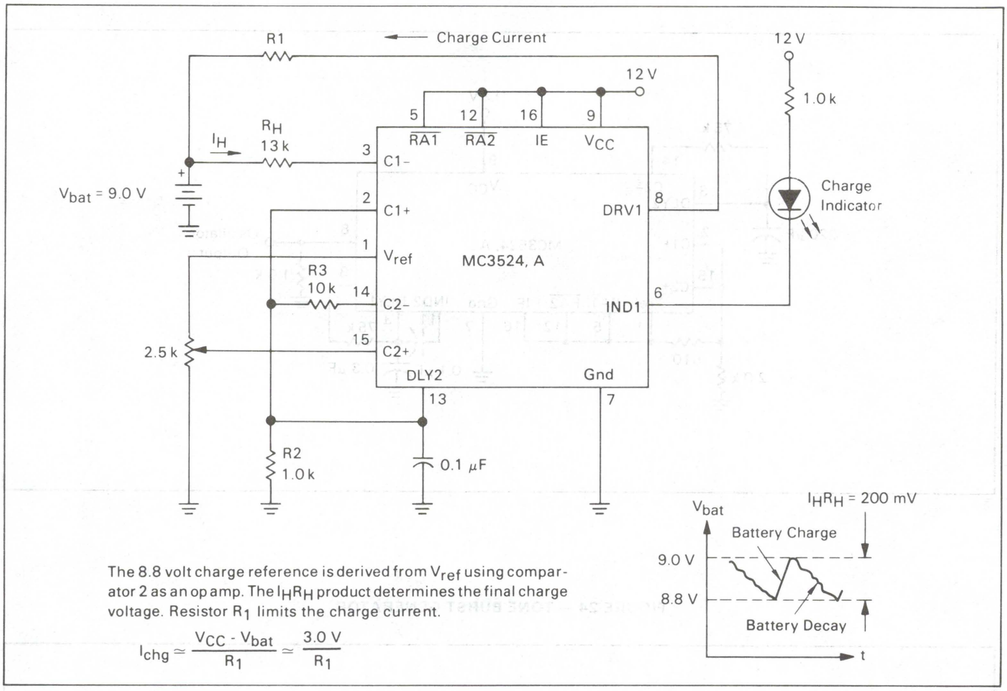

Reset
10 V
V_{IN} > 2.5 V
8.2 k
R
18 k
100 k
100 μF
0.1 μF
750
9
V_{CC}
2
C1+
15
C2+
3
C1−
16
IE
12
RA2
1
V_{ref}
14
C2−
13
DLY2
4
DLY1
Gnd
7
5
RA1
6
IND1
8
DRV1
10
DRV2
MC3524, A
Mallory
Sonalert SC628

FIGURE 20 — ADJUSTABLE D.C. PICK-UP/DROP-OUT RELAY CIRCUIT


V_{in}
10 k
500
1.0 k
13 k
50 k
Hysteresis
Voltage Adjust
9
V_{CC}
RA2
14
C2−
16
IE
13
DLY2
5
RA1
2
C1+
3
C1−
1
V_{ref}
15
C2+
Gnd
7
MC3524, A
8
DRV1
DLY1
4
0.01 μF

Pick-up Voltage Range: 19 V to 29 V
Hysteresis: 2.0 V to 7.0 V
Drop-Out Voltage = Pick-up Voltage − Hysteresis Voltage

FIGURE 21 — 9.0 V BATTERY CHARGER with ZERO SENSE LOAD CURRENT


R1
Charge Current
12 V
12 V
1.0 k
5
12
16
9
RA1
RA2
IE
VCC
RH
13 k
IH
3
C1−
Vbat = 9.0 V
+
2
C1+
DRV1
8
Charge
Indicator
1
Vref
MC3524, A
R3
10 k
14
C2−
IND1
6
2.5 k
15
C2+
DLY2
Gnd
13
7
R2
1.0 k
0.1 µF
Vbat
IHRH = 200 mV
Battery Charge
9.0 V
8.8 V
Battery Decay
t

The 8.8 volt charge reference is derived from V_{ref} using comparator 2 as an op amp. The $I_H R_H$ product determines the final charge voltage. Resistor R_1 limits the charge current.

$$I_{chg} \simeq \frac{V_{CC} - V_{bat}}{R_1} \simeq \frac{3.0\ V}{R_1}$$

FIGURE 22 — PROPORTIONAL CONTROL CIRCUIT

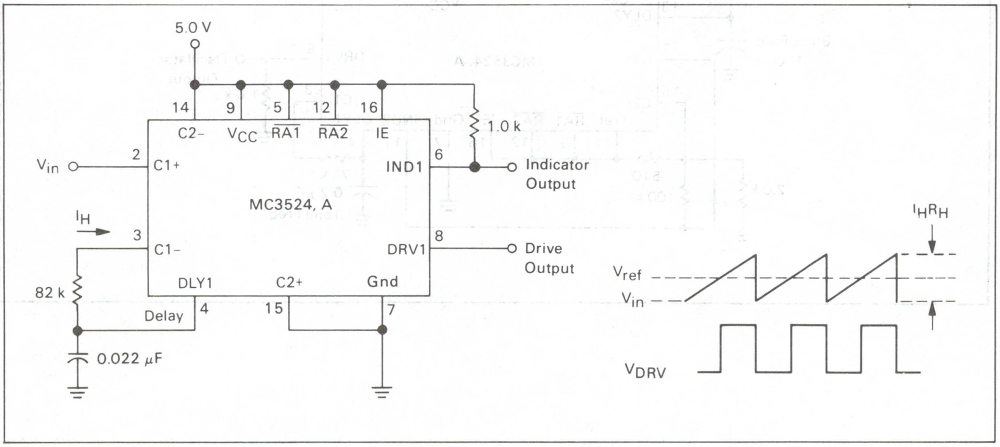
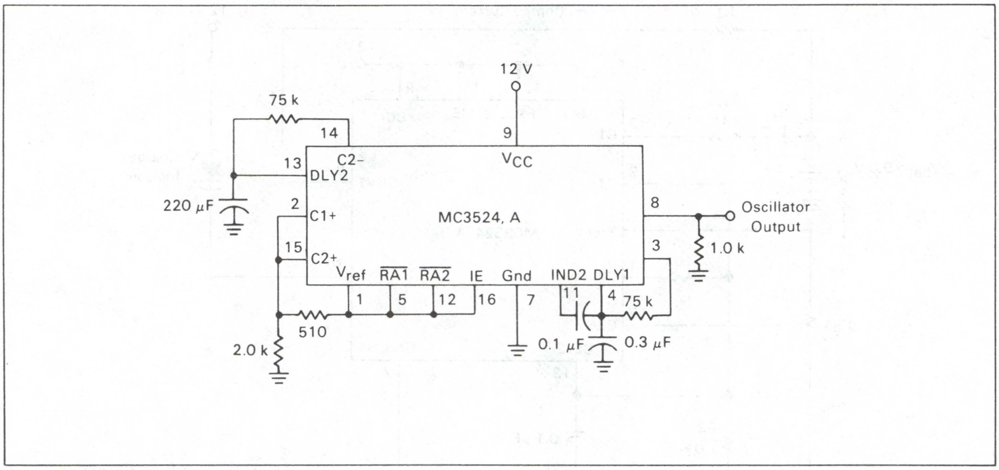

5.0 V
14
9
5
12
16
C2−
VCC
RA1
RA2
IE
1.0 k
Vin
2
C1+
IND1
6
Indicator
Output
MC3524, A
IH
3
C1−
8
DRV1
Drive
Output
82 k
DLY1
C2+
Gnd
Delay
4
15
7
0.022 µF
IHRH
Vref
Vin
VDRV

FIGURE 23 — ALTERNATING TWO TONE GENERATOR (EUROPEAN SIREN)


12 V
75 k
14
9
13
C2−
DLY2
VCC
220 μF
2
C1+
MC3524, A
8
Oscillator Output
15
C2+
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
75 k
510
2.0 k
0.1 μF
0.3 μF

8

FIGURE 24 — TONE BURST GENERATOR

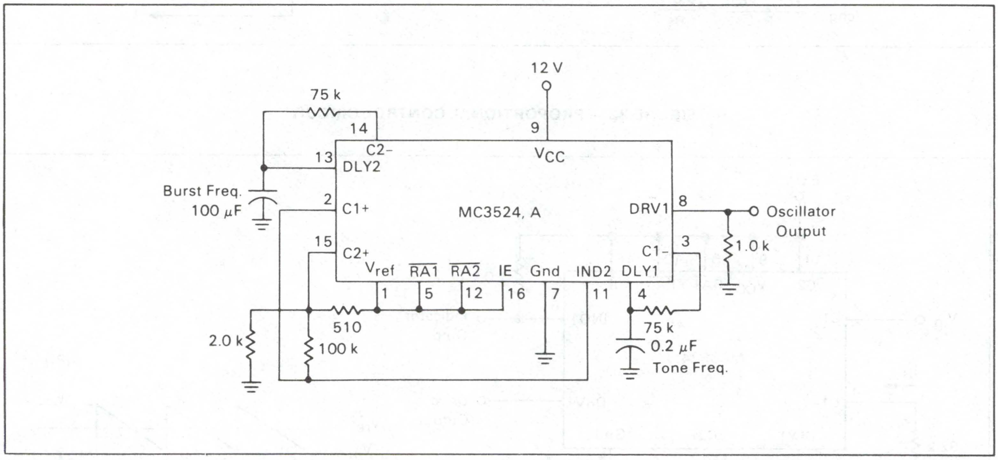

12 V
75 k
14
9
13
C2−
DLY2
VCC
Burst Freq. 100 μF
2
C1+
MC3524, A
DRV1
8
Oscillator Output
15
C2+
C1−
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
510
75 k
2.0 k
100 k
0.2 μF
Tone Freq.

FIGURE 25 — PHOTOFLASH CONVERTER

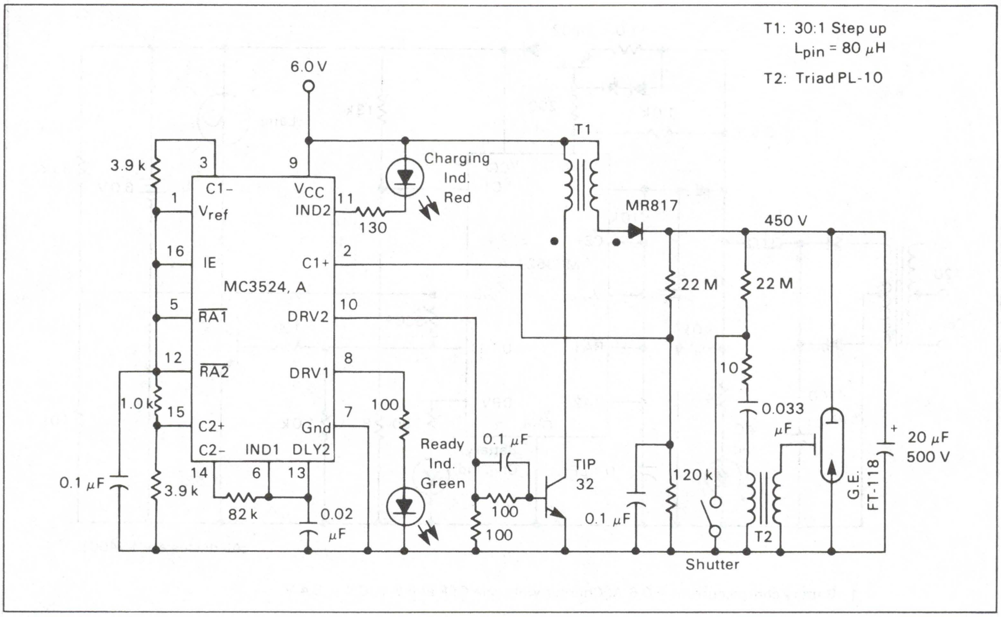

T1: 30:1 Step up
L_{pin} = 80 μH
T2: Triad PL-10
6.0 V
3.9 k
3
9
C1−
V_{CC}
1
V_{ref}
IND2
11
130
Charging Ind. Red
T1
MR817
450 V
16
IE
C1+
2
MC3524, A
5
RA1
DRV2
10
22 M
22 M
12
RA2
DRV1
8
10
1.0 k
15
C2+
Gnd
7
100
0.033 μF
C2−
IND1
DLY2
Ready Ind. Green
0.1 μF
TIP 32
20 μF 500 V
0.1 μF
14
6
13
3.9 k
82 k
120 k
G.E. FT-118
0.02 μF
100
100
0.1 μF
T2
Shutter

FIGURE 26 — PROGRAMMABLE FREQUENCY SWITCH

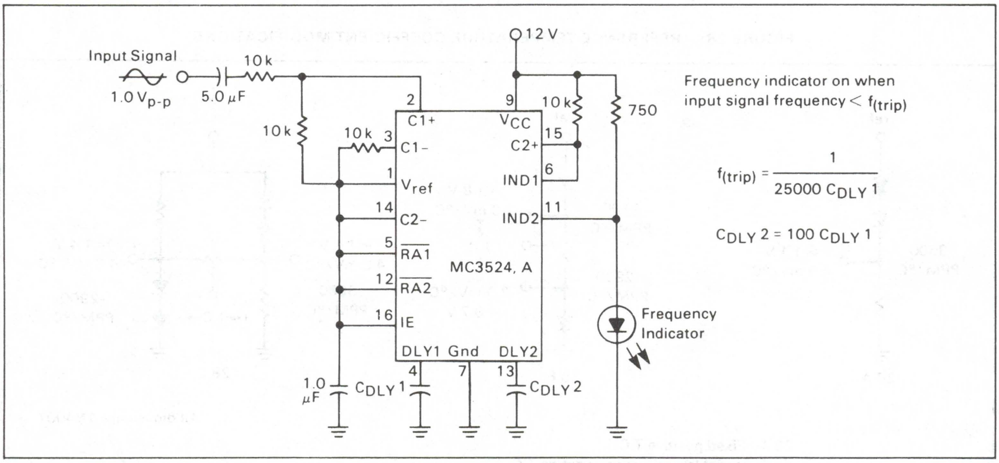
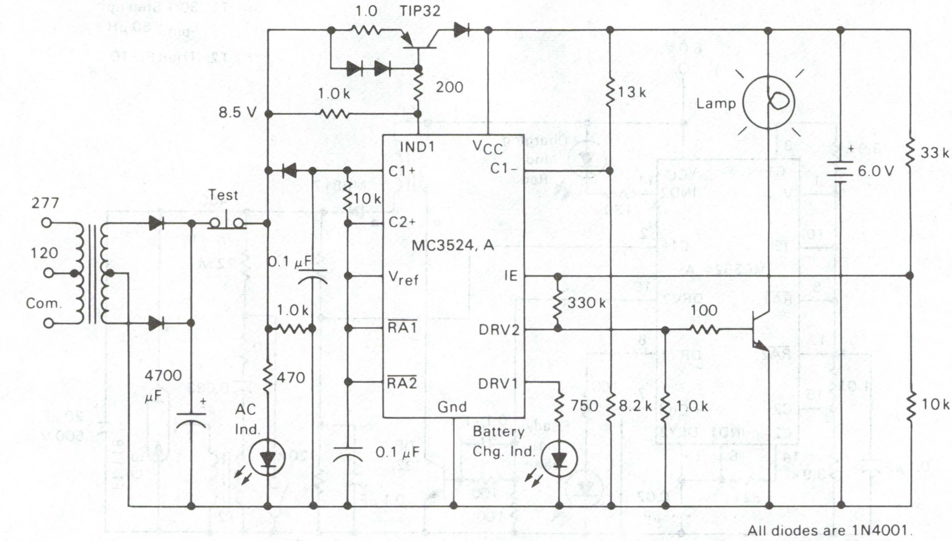

12 V
Input Signal
1.0 V_{p-p}
10 k
5.0 μF
2
9
10 k
750
C1+
V_{CC}
10 k
10 k
3
C1−
C2+
15
1
V_{ref}
IND1
6
14
C2−
IND2
11
5
RA1
MC3524, A
12
RA2
16
IE
Frequency Indicator
DLY1
Gnd
DLY2
4
7
13
1.0 μF
C_{DLY} 1
C_{DLY} 2
Frequency indicator on when input signal frequency < $f_{(trip)}$
$f_{(trip)} = \frac{1}{25000\, C_{DLY\,1}}$
$C_{DLY\,2} = 100\, C_{DLY\,1}$

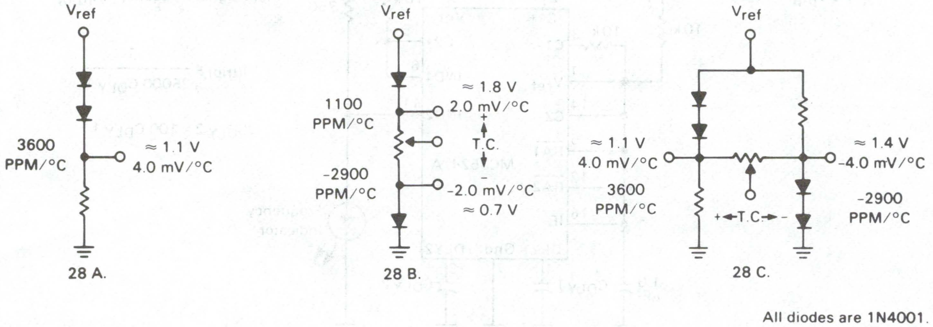
FIGURE 27 — EMERGENCY LIGHTING SYSTEM


1.0
TIP32
200
1.0 k
8.5 V
13 k
Lamp
33 k
6.0 V
IND1
VCC
C1+
C1-
10 k
Test
277
120
Com.
C2+
MC3524, A
0.1 μF
Vref
IE
330 k
1.0 k
RA1
DRV2
100
4700 μF
470
RA2
DRV1
AC Ind.
Gnd
750
8.2 k
1.0 k
10 k
Battery Chg. Ind.
0.1 μF
All diodes are 1N4001.

1. Battery charge current ≈ 0.6 A. Charger will cycle OFF at 6.6 V, ON at 6.4 V.

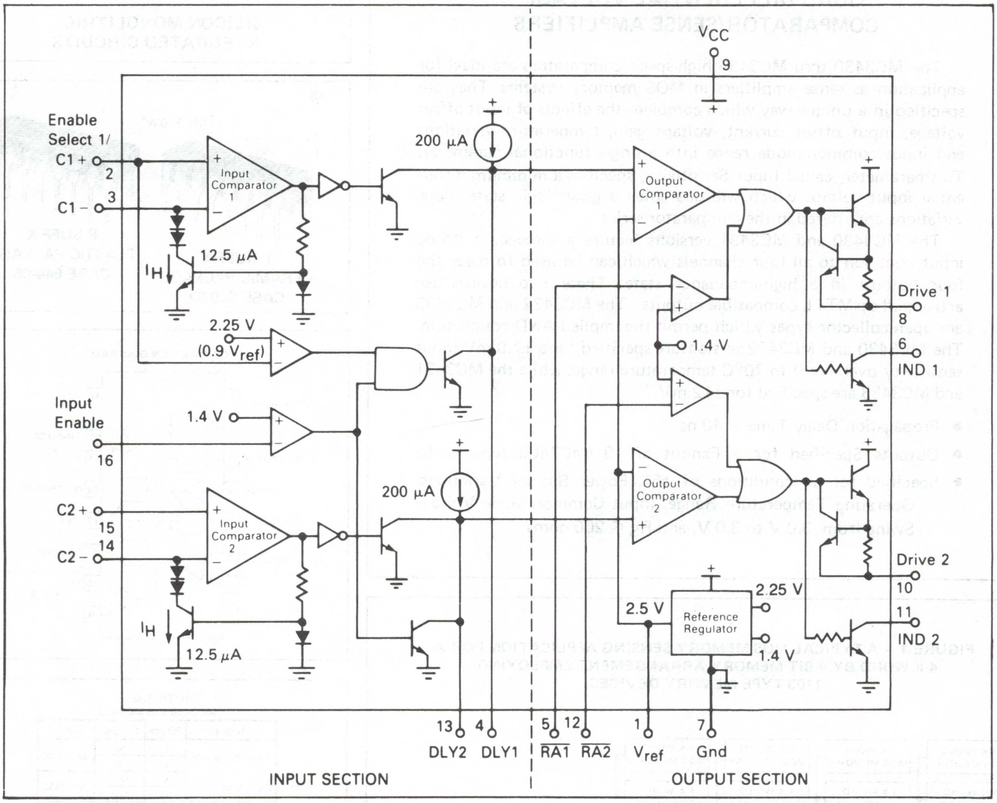
2. Lamp is ON with loss of ac and battery voltage ≥ 5.7 V. As battery discharges to < 5.3 V, lamp will turn OFF.

FIGURE 28 — REFERENCE TEMPERATURE COEFFICIENT MODIFICATIONS


Vref
3600 PPM/°C
≈ 1.1 V
4.0 mV/°C
28 A.
Vref
1100 PPM/°C
≈ 1.8 V
2.0 mV/°C
+
T.C.
-
-2900 PPM/°C
-2.0 mV/°C
≈ 0.7 V
28 B.
Vref
≈ 1.1 V
4.0 mV/°C
3600 PPM/°C
+ T.C. -
≈ 1.4 V
-4.0 mV/°C
-2900 PPM/°C
28 C.
All diodes are 1N4001.

28 A. Fixed positive T.C.
28 B. Variable positive or negative T.C.
28 C. Variable positive or negative T.C. with almost constant voltage.

FIGURE 29 — MC3524/3424/3324 BLOCK DIAGRAM


VCC
9
Enable
Select 1/
C1+
2
C1−
3
Input Comparator 1
+
−
200 µA
12.5 µA
IH
2.25 V
(0.9 Vref)
Input
Enable
16
1.4 V
C2+
15
14
C2−
Input Comparator 2
200 µA
IH
12.5 µA
Output Comparator 1
Output Comparator 2
1.4 V
Drive 1
8
6
IND 1
Drive 2
10
11
IND 2
2.5 V
Reference Regulator
2.25 V
1.4 V
13
4
5
12
1
7
DLY2
DLY1
RA1
RA2
Vref
Gnd
INPUT SECTION
OUTPUT SECTION

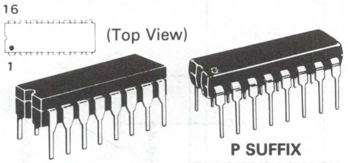
Note: All voltages and currents are nominal.

MC3430
thru
MC3433

MOTOROLA

QUAD HIGH-SPEED VOLTAGE COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS


16
(Top View)
1

L SUFFIX
CERAMIC PACKAGE
CASE 620-02

P SUFFIX
PLASTIC PACKAGE
CASE 648-05

QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versionsare specified for a ±7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leqslant 200$ ohms.

CONNECTION DIAGRAM

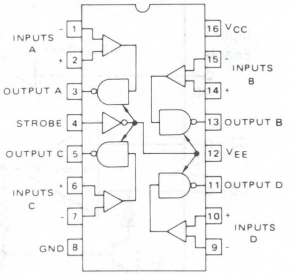
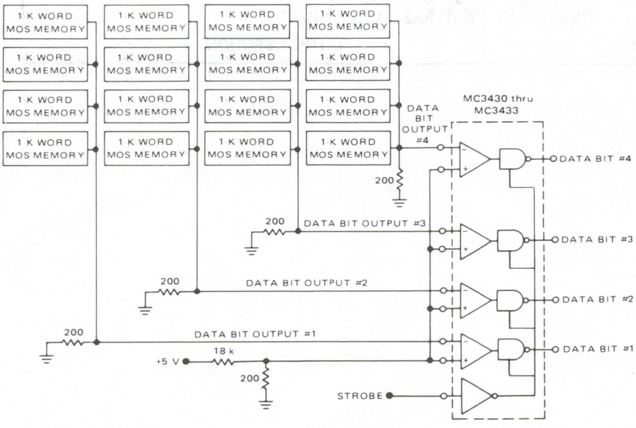

INPUTS A
-
1
+
2
OUTPUT A
3
STROBE
4
OUTPUT C
5
INPUTS C
+
6
-
7
GND
8
16
VCC
15
-
INPUTS B
14
+
13
OUTPUT B
12
VEE
11
OUTPUT D
10
+
INPUTS D
9
-

FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES


1-K WORD MOS MEMORY
DATA BIT OUTPUT #4
MC3430 thru MC3433
200
DATA BIT #4
DATA BIT OUTPUT #3
DATA BIT #3
DATA BIT OUTPUT #2
DATA BIT #2
DATA BIT OUTPUT #1
DATA BIT #1
18 k
+5 V
200
STROBE

Only four devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE
MC3430 and MC3432

Input	Strobe	Output	Device
$V_{ID} \geqslant 7.0$ mV	L	H	MC3430
	H	Z	
T_A = 0 to 70°C	L	Off	MC3432
	H	Off	
-7.0 mV $\leqslant V_{ID}$	L	I	MC3430
	H	Z	
$\leqslant$ 7.0 mV T_A = 0 to 70°C	L	I	MC3432
	H	Off	
$V_{ID} \leqslant$ -7.0 mV	L	L	MC3430
	H	Z	
T_A = 0 to 70°C	L	On	MC3432
	H	Off	

TRUTH TABLE
MC3431 and MC3433

Input	Strobe	Output	Device
$V_{ID} \geqslant 12$ mV	L	H	MC3431
	H	Z	
T_A = 0 to 70°C	L	Off	MC3433
	H	Off	
-12 mV $\leqslant V_{ID}$	L	I	MC3431
	H	Z	
$\leqslant$+12 mV T_A = 0 to 70°C	L	I	MC3433
	H	Off	
$V_{ID} \leqslant$ -12 mV	L	L	MC3431
	H	Z	
T_A = 0 to 70°C	L	On	MC3433
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
$R_S \leqslant 200\ \Omega$

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432 – 33 versions)	V_O	+7.0	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0°C to +70°C unless otherwise noted.)
Typical Values are Measured at T_A = 25°C

Characteristic	Symbol	MC3430, MC3431			MC3432, MC3433			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Sensitivity (See Discussion on Page 3) ($R_S \leqslant$ 200 Ohms)	V_{IS}							mV
(Common Mode Voltage Range = $-3.0\ V \leqslant V_{in} \leqslant 3.0\ V$) $4.75 \leqslant V_{CC} \leqslant 5.25$ V, $-4.75 \geqslant V_{EE} \geqslant -5.25$ V, T_A = 25°C, MC3430, MC3432		–	–	±6.0	–	–	±6.0	
MC3431, MC3433		–	–	±10	–	–	±10	
(Common Mode Voltage Range = $-3.0\ V \leqslant V_{in} \leqslant 3.0\ V$) $4.75 \leqslant V_{CC} \leqslant 5.25$ V, $-4.75 \geqslant V_{EE} \geqslant -5.25$ V, T_A = 0 to 70°C, MC3430, MC3432		–	–	±7.0	–	–	±7.0	
MC3431, MC3433		–	–	±12	–	–	±12	
Input Offset Voltage ($R_S \leqslant$ 200 Ohms)	V_{IO}	–	2.0	–	–	2.0	–	mV
Input Bias Current	I_{IB}							µA
(V_{CC} = 5.25 V, V_{EE} = -5.25 V) MC3430, MC3432		–	20	40	–	20	40	
MC3431, MC3433		–	20	40	–	20	40	
Input Offset Current	I_{IO}	–	1.0	–	–	1.0	–	µA
Voltage Gain	A_{vol}	–	1200	–	–	1200	–	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	–	–	-1.6	–	–	-1.6	mA
Strobe Current (High State)	$I_{IH(S)}$							
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 2.4 V)		–	–	40	–	–	40	µA
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 5.25 V)		–	–	1.0	–	–	1.0	mA
Output Voltage (High State) (I_O = -400 µA, V_{CC} = 4.75 V, V_{EE} = -4.75 V)	V_{OH}	2.4	–	–	–	–	–	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = -4.75 V, V_O = 5.25 V)	I_{CEX}	–	–	–	–	–	250	µA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{os}	-18	–	-70	–	–	–	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{off}	–	–	40	–	–	–	µA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{CC} I_{EE}	– –	45 -17	60 -30	– –	45 -17	60 -30	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{vol}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analagous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range – 0 to 70°C
Power Supply Variations – ±5% (all conditions)
Input Source Resistance – ⩽200 Ohms
Common-Mode Voltage Range – -3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V (V_{OH}min – V_{OL}max = 2.4 V – 0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

TABLE I – WORST CASE COMPARISONS

	T_A = 25°C						T_A = 0 to 70°C					
Type Number	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV
MC3430, MC3432	–	–	–	–	–	6.0	–	–	–	–	–	7.0
MC3431, MC3433	–	–	–	–	–	10	–	–	–	–	–	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
LM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

*Typical values given, as minimum gain not always specified.
**I_{IO} measured in nA

FIGURE 2 – GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

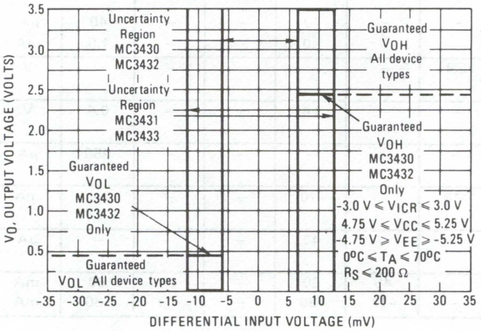
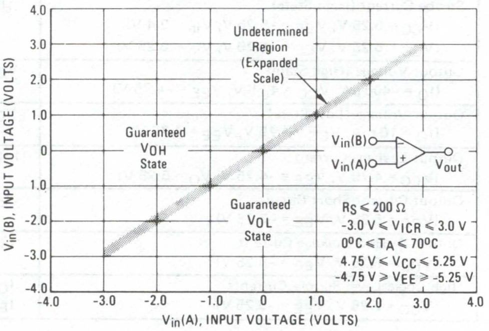


FIGURE 3 – GUARANTEED OUTPUT STATE versus INPUT VOLTAGE

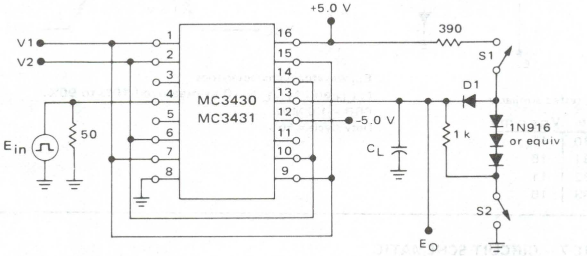


SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431 Min	MC3430, MC3431 Typ	MC3430, MC3431 Max	MC3432, MC3433 Min	MC3432, MC3433 Typ	MC3432, MC3433 Max	Unit
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PHL(D)}$	6,8-11	–	20	45	–	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PLH(D)}$	6,8-11	–	33	55	–	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	–	–	35	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	–	–	35	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	–	–	40	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	–	–	35	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	–	–	–	–	–	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	–	–	–	–	–	35	ns

TEST CIRCUITS

FIGURE 4 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$


+5.0 V
390
S1
V1
V2
D1
MC3430
MC3431
-5.0 V
1N916 or equiv
1 k
C_L
50
E_in
S2
E_O
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{in} waveform characteristics:

t_{TLH} and t_{THL} $\leqslant$ 10 ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

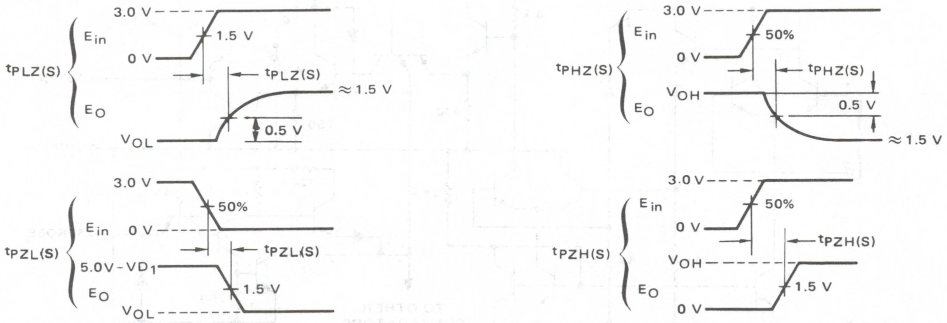
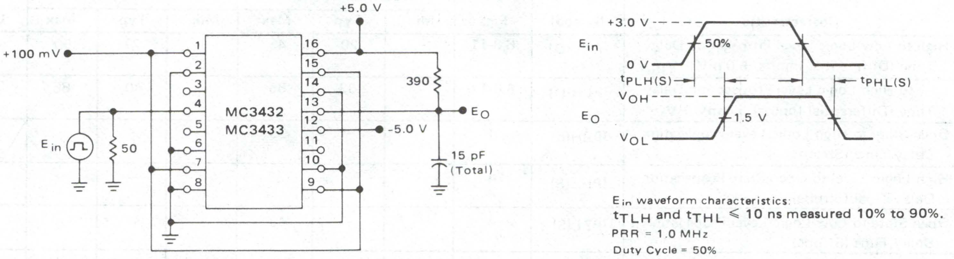

t_PLZ(S)
3.0 V
E_in
1.5 V
0 V
t_PLZ(S)
≈1.5 V
E_O
0.5 V
V_OL
t_PHZ(S)
3.0 V
E_in
50%
0 V
t_PHZ(S)
V_OH
0.5 V
E_O
≈1.5 V
t_PZL(S)
3.0 V
50%
E_in
0 V
t_PZL(S)
5.0V - VD1
E_O
1.5 V
V_OL
t_PZH(S)
3.0 V
E_in
50%
0 V
t_PZH(S)
V_OH
E_O
1.5 V
0 V

FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$


+5.0 V
+100 mV
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3432
MC3433
390
E_O
-5.0 V
E_in
50
15 pF
(Total)
+3.0 V
E_in
50%
0 V
t_PLH(S)
t_PHL(S)
V_OH
E_O
1.5 V
V_OL

E_{in} waveform characteristics:

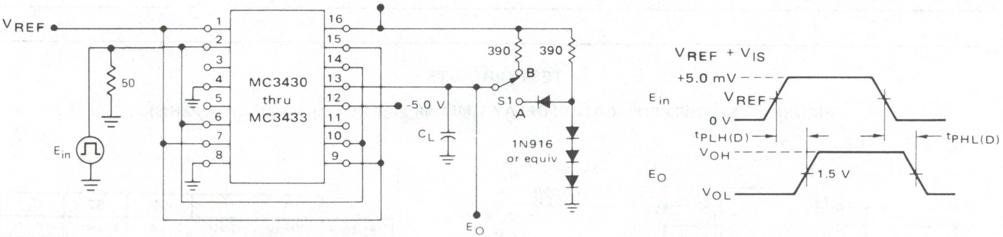
t_{TLH} and t_{THL} ⩽ 10 ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$


+5.0 V
V_REF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3430
thru
MC3433
50
E_in
-5.0 V
C_L
390
390
B
S1
A
1N916
or equiv
E_O
V_REF + V_IS
+5.0 mV
E_in
V_REF
0 V
t_PLH(D)
t_PHL(D)
V_OH
E_O
1.5 V
V_OL

E_{in} waveform characteristics:

t_{TLH} and t_{THL} ⩽ 10 ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3430, MC3431

S1 at "B" for MC3432, MC3433

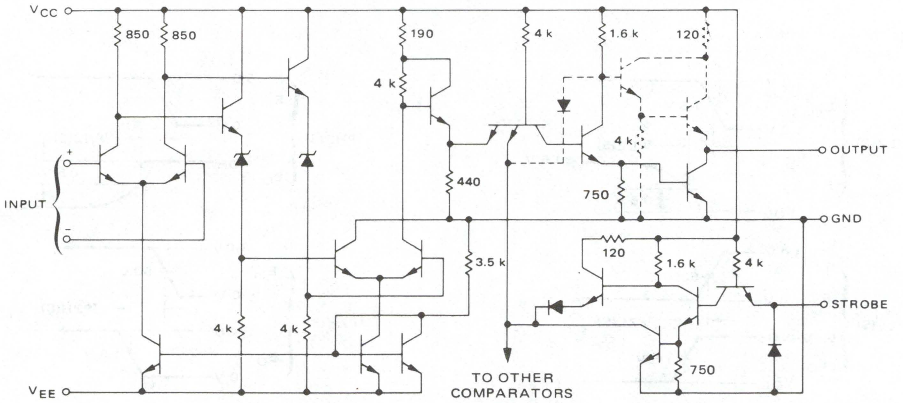
C_L = 50 pF total for MC3430, MC3431

C_L = 15 pF total for MC3432, MC3433

Device	V_{REF} mV
MC3430	11
MC3431	15
MC3432	11
MC3433	15

FIGURE 7 – CIRCUIT SCHEMATIC

(1/4 Circuit Shown)


V_CC
850
850
190
4 k
1.6 k
120
4 k
4 k
440
750
OUTPUT
GND
INPUT
+
–
3.5 k
120
1.6 k
4 k
STROBE
4 k
4 k
750
V_EE
TO OTHER
COMPARATORS

Dashed components apply to the MC3430 and MC3431 circuits only.

TYPICAL PERFORMANCE CURVES

RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

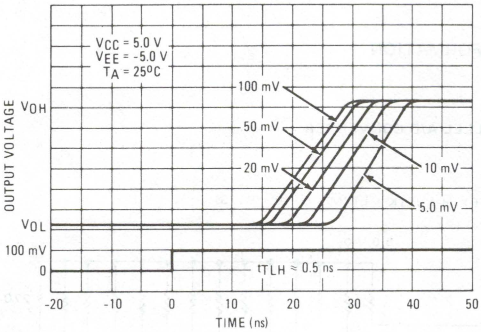
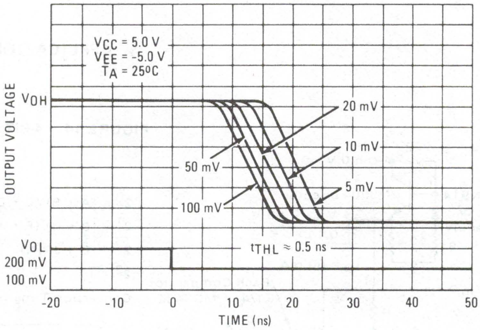


FIGURE 9 – OUTPUT HIGH TO LOW



RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

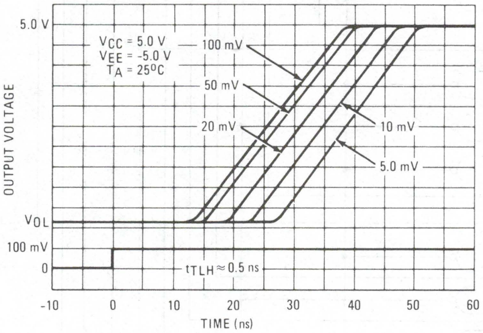


FIGURE 11 – OUTPUT HIGH TO LOW

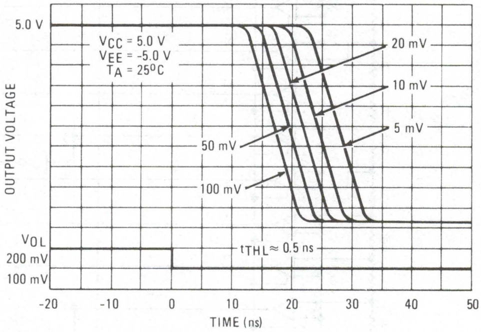


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

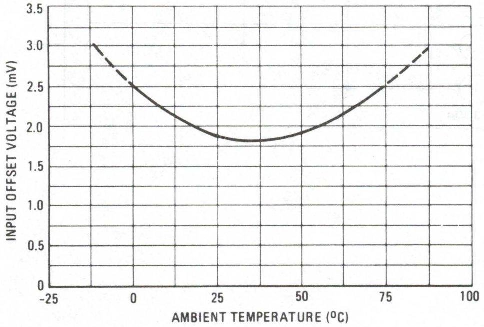
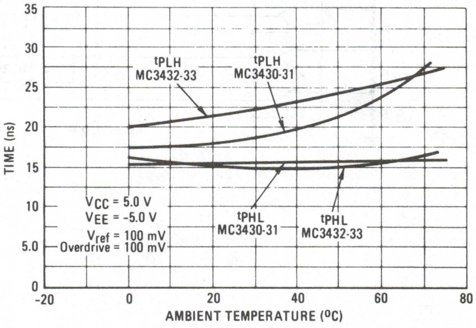
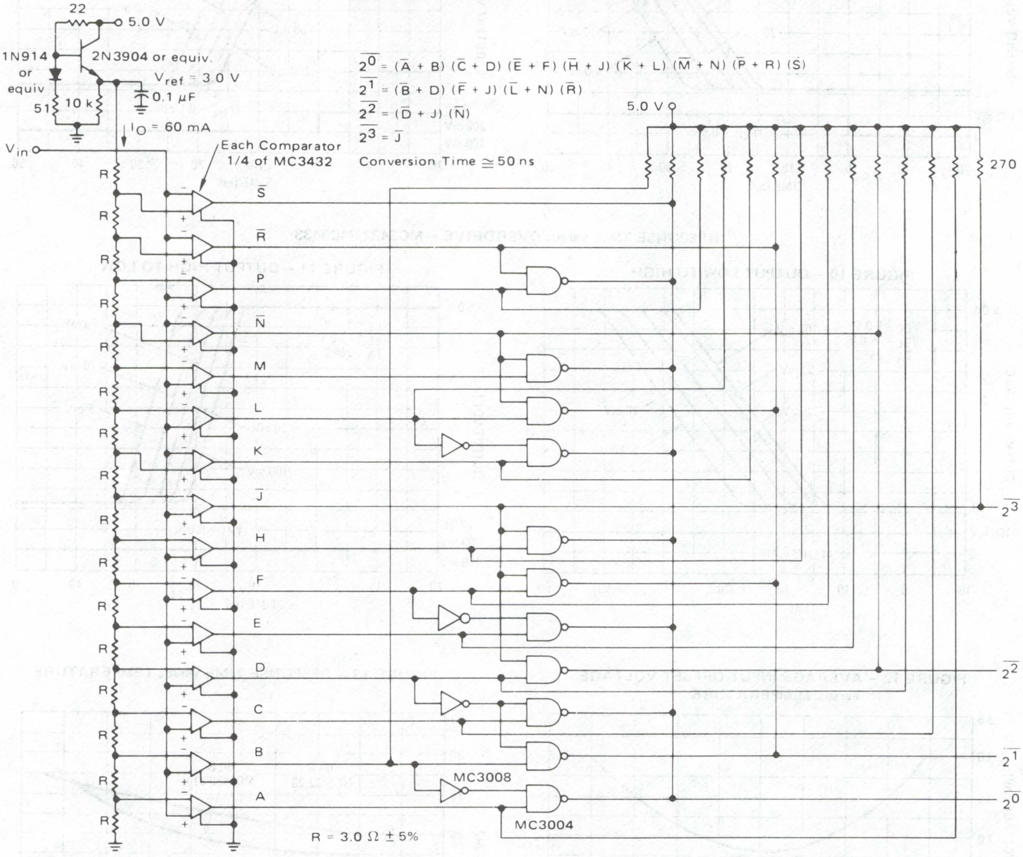


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 14 – 4-BIT PARALLEL A/D CONVERTER


22
5.0 V
1N914 or equiv
2N3904 or equiv.
V_{ref} = 3.0 V
0.1 µF
51
10 k
I_O = 60 mA
V_{in}
Each Comparator 1/4 of MC3432
R
$\overline{S}$
$\overline{R}$
P
$\overline{N}$
M
L
K
$\overline{J}$
H
F
E
D
C
B
A
5.0 V
270
$\overline{2^3}$
$\overline{2^2}$
$\overline{2^1}$
$\overline{2^0}$
MC3008
MC3004

$\overline{2^0} = (\overline{A} + B)(\overline{C} + D)(\overline{E} + F)(\overline{H} + J)(\overline{K} + L)(\overline{M} + N)(\overline{P} + R)(\overline{S})$

$\overline{2^1} = (\overline{B} + D)(\overline{F} + J)(\overline{L} + N)(\overline{R})$

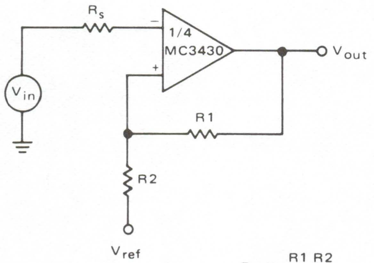
$\overline{2^2} = (\overline{D} + J)(\overline{N})$

$\overline{2^3} = \overline{J}$

Conversion Time ≅ 50 ns

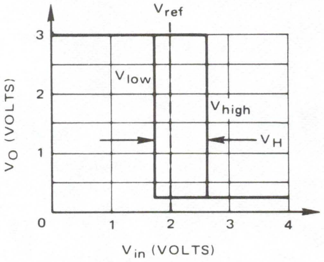
R = 3.0 Ω ± 5%

FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS


R_S
1/4
MC3430
–
+
V_out
V_in
R1
R2
V_ref

$$R_S \approx \frac{R1\ R2}{R1 + R2}$$

FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15



$$V_{high} = V_{ref} + \frac{R2\ [V_{O(max)} - V_{REF}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\ [V_{O(min)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_h)

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\ [V_{O(max)} - V_{O(min)}]$$

FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

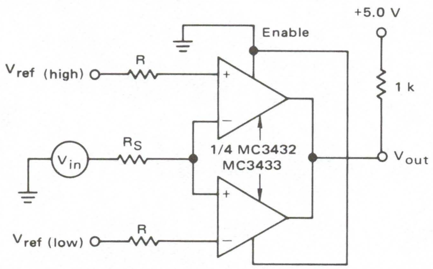
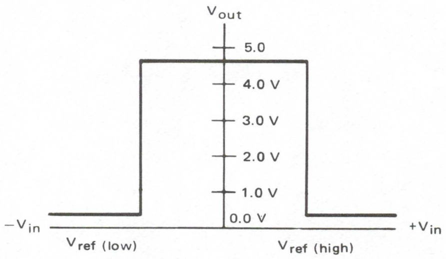
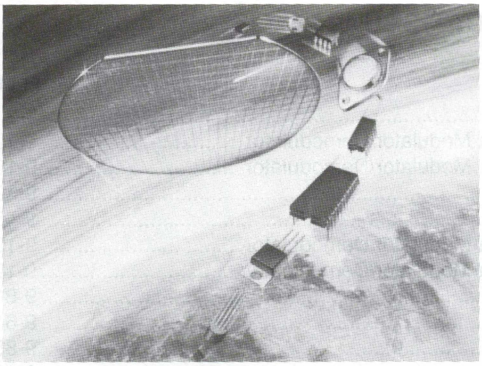

+5.0 V
Enable
V_ref (high)
R
+
–
1 k
R_S
V_in
1/4 MC3432
MC3433
V_out
+
–
V_ref (low)
R

FIGURE 18 – VOLTAGE TRANSFER FUNCTION





Telecommunications

TELECOMMUNICATIONS

Device	Function	Page
MC3416	Crosspoint Switch	9-3
MC3417	Continuously-Variable-Slope Delta Modulator/Demodulator	9-12
MC3418	Continuously-Variable-Slope Delta Modulator/Demodulator	9-12
MC3419,A,C	Subscriber Loop Interface Circuit	9-30
MC3419-1L, A-1L, C-1L	Subscriber Loop Interface Circuit	9-45
MC3517	Continuously-Variable-Slope Delta Modulator/Demodulator	9-12
MC3518	Continuously-Variable-Slope Delta Modulator/Demodulator	9-12
MC34010 P	Electronic Telephone Circuit	9-61
MC34011 P	Electronic Telephone Circuit	9-61
MC34012 Series	Telephone Tone Ringer	9-85
MC34013	Speech Network and Tone Dialer	9-93
MC34015	Telephone Tone Dialer	9-94
MC34017	Telephone Tone Ringer	9-95

MOTOROLA

MC3416

Specifications and Applications Information

4 x 4 x 2 CROSSPOINT SWITCH

DIELECTRICALLY ISOLATED MONOLITHIC INTEGRATED CIRCUIT

4 x 4 x 2 CROSSPOINT SWITCH

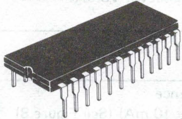
The MC3416 consists of a pair of 4 x 4 matrices of dielectrically isolated SCR's, triggered by a common selection matrix. The device is intended for switching analog signals in communication systems. The use of dielectric isolation processing provides excellent crosstalk isolation while maintaining minimal insertion loss.

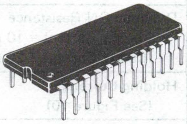
The selection array consists of PNP transistors with the input thresholds compatible with either CMOS or TTL logic families.

The MC3416 is a monolithic pin-for-pin replacement for the discontinued MCBH7601 hybrid device.

- Low Series Resistance — r_{on} = 6.0 Ohms (Typ) @ I_{AK} = 20 mA
- High Series Resistance — r_{off} = 100 MΩ (Min)
- Pin Compatible with MCBH7601 or RC4444
- High Breakdown Voltage — 30 V (Typ)
- Selection Matrix Compatible with TTL or CMOS Logic Levels
- Dielectric Isolation Insures Low Crosstalk and Low Insertion Loss

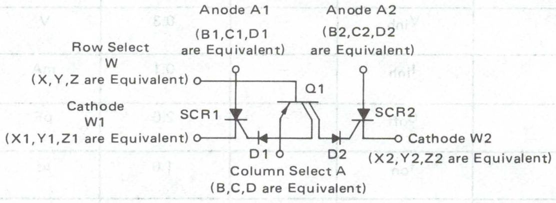
L SUFFIX
CERAMIC PACKAGE
CASE 623-05





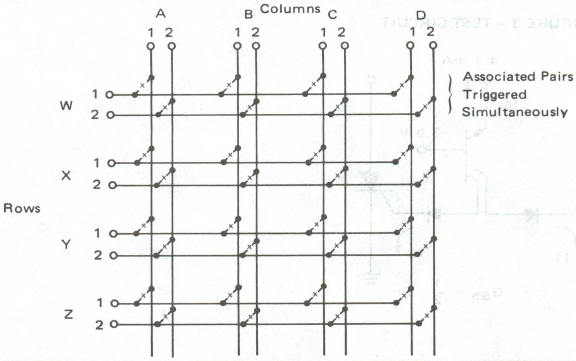
P SUFFIX
PLASTIC PACKAGE
CASE 649-03

FIGURE 1 — REPRESENTATIVE CELL SCHEMATIC
(Repeated 16 Times)



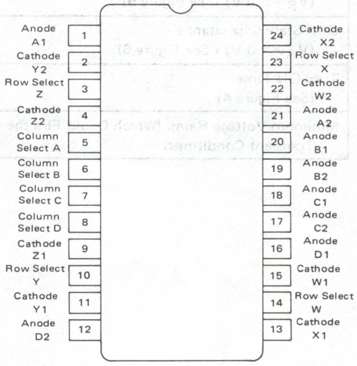
Anode A1
(B1,C1,D1 are Equivalent)
Anode A2
(B2,C2,D2 are Equivalent)
Row Select W
(X,Y,Z are Equivalent)
Q1
Cathode W1
(X1,Y1,Z1 are Equivalent)
SCR1
SCR2
D1
D2
Cathode W2
(X2,Y2,Z2 are Equivalent)
Column Select A
(B,C,D are Equivalent)

FIGURE 2 — MATRIX CONFIGURATION AND NOMENCLATURE
(X Indicates a Possible Connection)



Columns
A
B
C
D
1 2
1 2
1 2
1 2
Associated Pairs Triggered Simultaneously
Rows
W
X
Y
Z
1
2
1
2
1
2
1
2

PIN CONNECTIONS



Anode A1 1
Cathode Y2 2
Row Select Z 3
Cathode Z2 4
Column Select A 5
Column Select B 6
Column Select C 7
Column Select D 8
Cathode Z1 9
Row Select Y 10
Cathode Y1 11
Anode D2 12
24 Cathode X2
23 Row Select X
22 Cathode W2
21 Anode A2
20 Anode B1
19 Anode B2
18 Anode C1
17 Anode C2
16 Anode D1
15 Cathode W1
14 Row Select W
13 Cathode X1

MAXIMUM RATINGS (Unless otherwise noted, T_A = 25°C)

Rating	Symbol	Value	Unit
Anode-Cathode Current – Continuous (only one SCR at a time)	I_{AK}	150	mA
Enable Current	I_{En}	10	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	150°C	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Max	Unit
Anode Cathode Breakdown Voltage (I_{AK} = 25μA)		$V_{(BR)AK}$	25	–	Vdc
Cathode-Anode Breakdown Voltage (I_{KA} = 25μA)		$V_{(BR)KA}$	25	–	Vdc
Base-Cathode Breakdown Voltage (I_{BK} = 25μA)		$V_{(BR)BK}$	25	–	Vdc
Cathode-Base Breakdown Voltage (I_{KB} = 25μA)		$V_{(BR)BE}$	25	–	Vdc
Base-Emitter Breakdown Voltage (I_{BE} = 25μA)		$V_{(BR)KB}$	25	–	Vdc
Emitter-Cathode Breakdown Voltage (I_{EK} = 25μA)		$V_{(BR)EK}$	25	–	Vdc
OFF State Resistance (V_{AK} = 10 V)		r_{off}	100	–	MΩ
Dynamic ON Resistance		r_{on}			Ω
(Center Current = 10 mA) (See Figure 8)			4.0	12	
(Center Current = 20 mA)			2.0	10	
Holding Current (See Figure 10)	+25°C to +70°C	I_H	0.7	3.0	mA
	0°C to +24°C		—	4.0	
Enable Current (V_B = 1.5 V) (See Figure 7)		I_{En}	4.0	–	mA
Anode-Cathode ON Voltage		V_{AK}			V
(I_{AK} = 10 mA)			–	1.0	
(I_{AK} = 20 mA)			–	1.1	
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open) (See Figure 3)		G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage (V_B = 3.0 V) (See Figure 9)		V_{inh}	–	0.3	V
Inhibit Current (V_B = 3.0 V) (See Figure 9)		I_{inh}	–	0.1	mA
OFF State Capacitance (V_{AK} = 0 V) (See Figure 6)		C_{off}	–	2.0	pF
Turn-ON Time (See Figure 4)		t_{on}	–	1.0	μs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)		dv/dt	800	–	V/μs

FIGURE 3 – TEST CIRCUIT

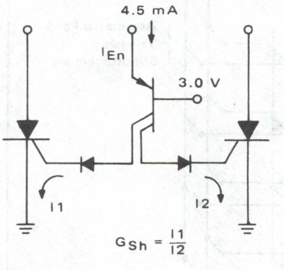


FIGURE 4 – TEST CIRCUIT FOR dv/dt AND t_{on}

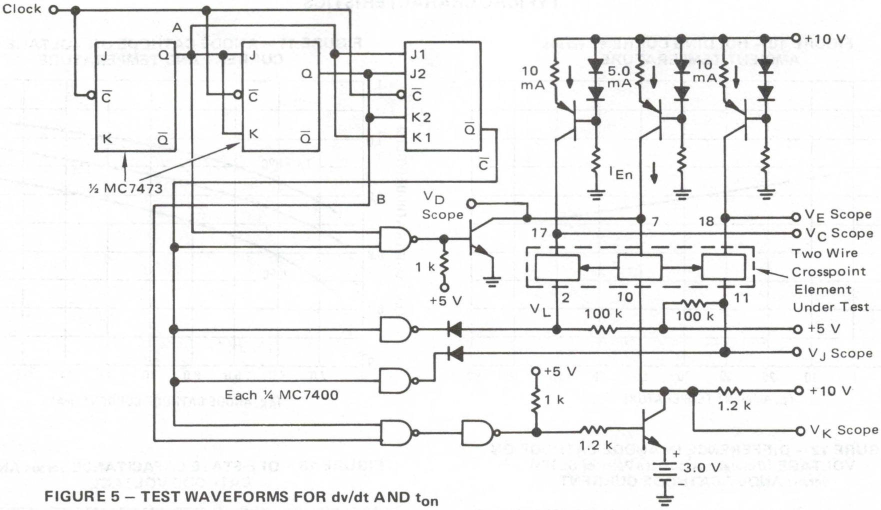

Clock
A
J
Q
C̄
K
Q̄
½ MC7473
J1
J2
K2
K1
B
+10 V
10 mA
5.0 mA
10 mA
I_En
V_D Scope
17
7
18
V_E Scope
V_C Scope
Two Wire Crosspoint Element Under Test
1 k
+5 V
2
10
11
V_L
100 k
100 k
+5 V
V_J Scope
Each ¼ MC7400
+5 V
1 k
+10 V
1.2 k
1.2 k
V_K Scope
3.0 V

FIGURE 5 – TEST WAVEFORMS FOR dv/dt AND t_{on}

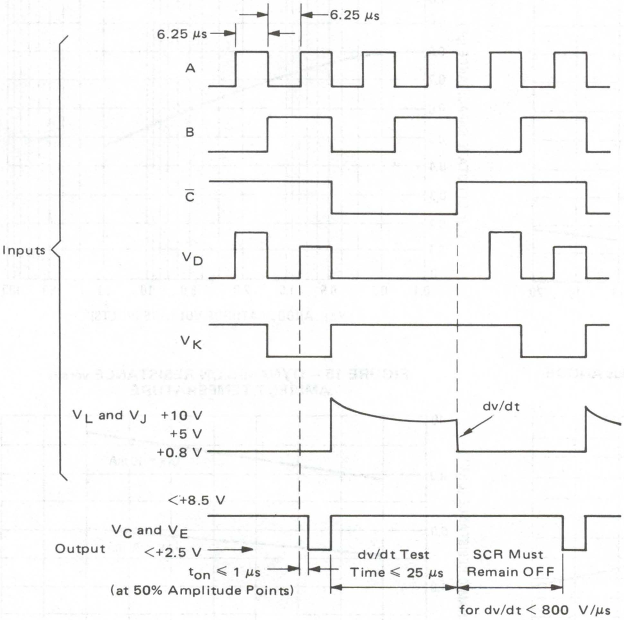
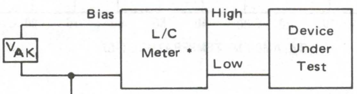


FIGURE 6 – TEST CIRCUIT FOR OFF-STATE CAPACITANCE


Bias
High
V_AK
L/C Meter *
Low
Device Under Test

All Device Pins Other Than Pins Under Test Are Connected to Test Equipment Ground Terminal

*Three-Terminal, Guarded, Differential Capacitance Meter

FIGURE 7 – ENABLE CURRENT (Both SCR's Must Turn On)

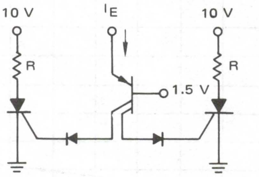

10 V
I_E
10 V
R
R
1.5 V

FIGURE 8 – THE CROSSPOINT SCR I-V CHARACTERISTIC ($I_G = 0$)

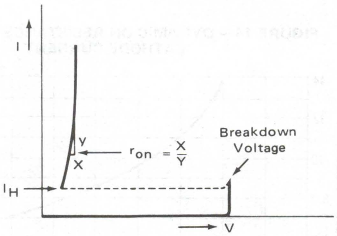
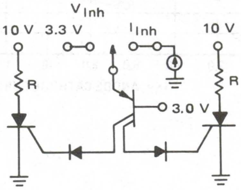


FIGURE 9 – INHIBIT VOLTAGE AND INHIBIT CURRENT (Both SCR's Must Remain OFF)


V_Inh
10 V
3.3 V
I_Inh
10 V
R
R
3.0 V

TYPICAL CHARACTERISTICS

FIGURE 10 – HOLDING CURRENT versus AMBIENT TEMPERATURE

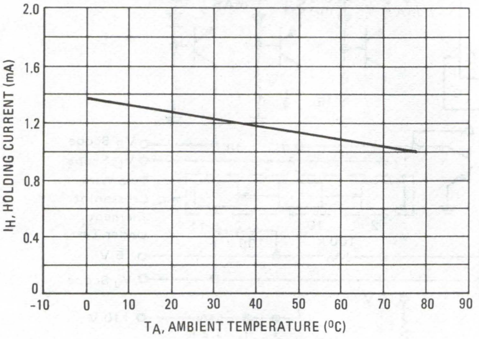


FIGURE 11 – ANODE-CATHODE ON VOLTAGE versus CURRENT AND TEMPERATURE

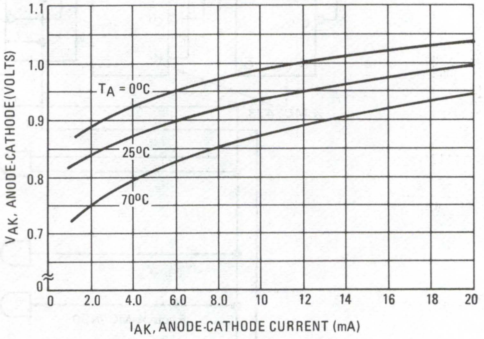


FIGURE 12 – DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) versus ANODE-CATHODE CURRENT

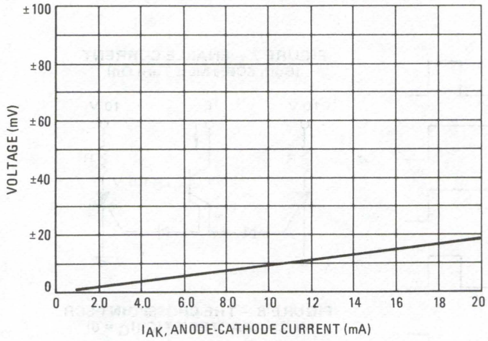


FIGURE 13 – OFF-STATE CAPACITANCE versus ANODE-CATHODE VOLTAGE

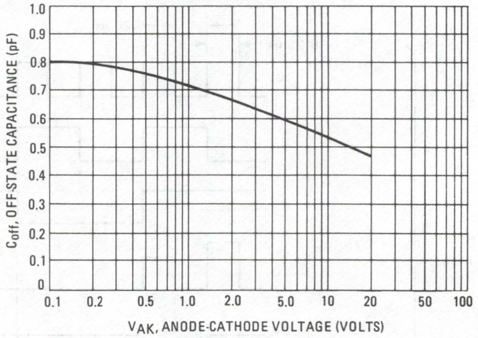


FIGURE 14 – DYNAMIC ON RESISTANCE versus ANODE-CATHODE CURRENT

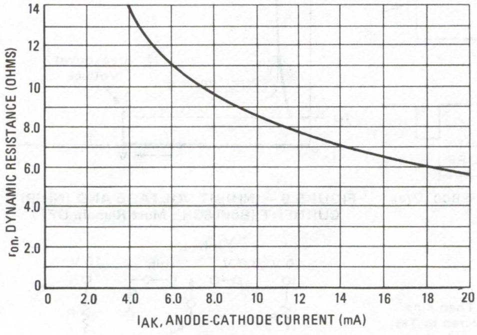


FIGURE 15 – DYNAMIC ON RESISTANCE versus AMBIENT TEMPERATURE

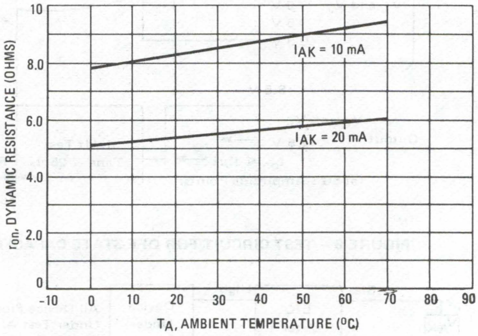


FIGURE 16 – FEEDTHROUGH versus SIGNAL FREQUENCY

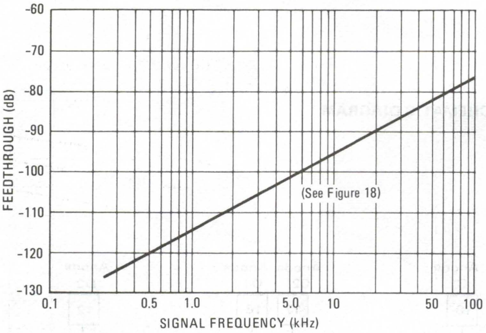


FIGURE 17 – CROSSTALK versus SIGNAL FREQUENCY

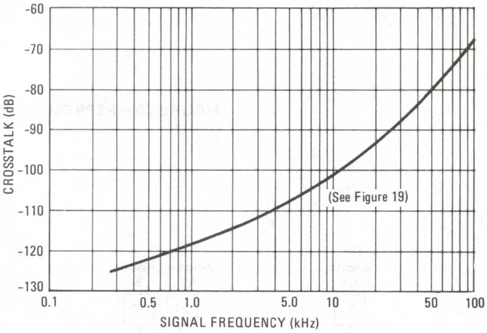
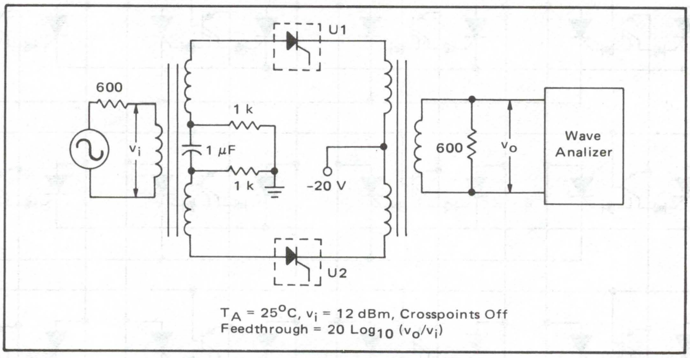
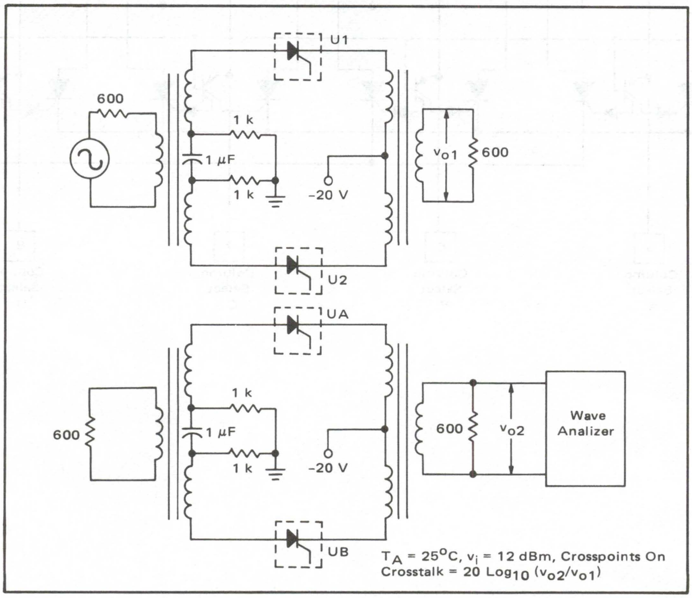


FIGURE 18 – TEST CIRCUIT FOR FEEDTHROUGH versus FREQUENCY


U1
600
1 k
v_i
1 µF
1 k
-20 V
600
v_o
Wave Analizer
U2

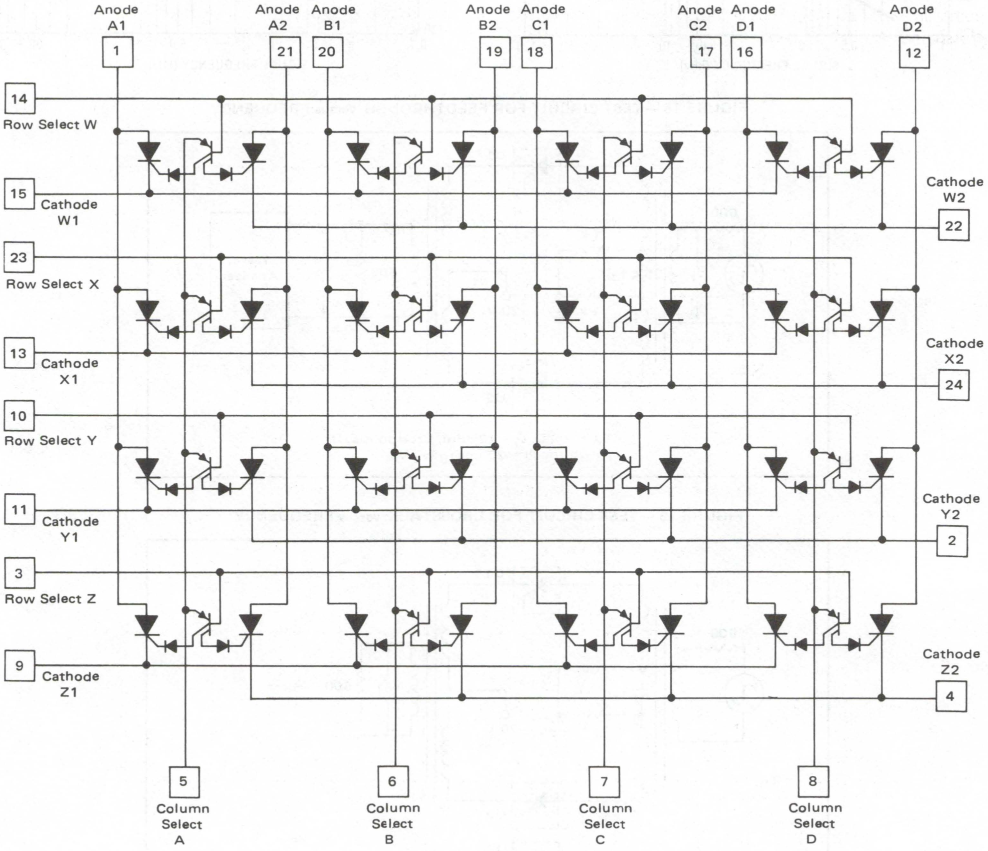
$T_A = 25^oC$, v_i = 12 dBm, Crosspoints Off
Feedthrough = 20 Log_{10} (v_o/v_i)

FIGURE 19 – TEST CIRCUIT FOR CROSSTALK versus FREQUENCY


U1
600
1 k
1 µF
1 k
-20 V
v_{o1}
600
U2
UA
1 k
600
1 µF
1 k
-20 V
600
v_{o2}
Wave Analizer
UB

$T_A = 25^oC$, v_i = 12 dBm, Crosspoints On
Crosstalk = 20 Log_{10} (v_{o2}/v_{o1})

FIGURE 20 – REPRESENTATIVE SCHEMATIC DIAGRAM


Anode A1
1
Anode A2
21
Anode B1
20
Anode B2
19
Anode C1
18
Anode C2
17
Anode D1
16
Anode D2
12
14
Row Select W
15
Cathode W1
Cathode W2
22
23
Row Select X
13
Cathode X1
Cathode X2
24
10
Row Select Y
11
Cathode Y1
Cathode Y2
2
3
Row Select Z
9
Cathode Z1
Cathode Z2
4
5
Column Select A
6
Column Select B
7
Column Select C
8
Column Select D

TELEPHONE APPLICATION OF THE CROSSPOINT SWITCH

The MC3416 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the MC3416 can significantly reduce the size and cost of existing crosspoint matrices.

SIGNAL PATH CONSIDERATIONS

The MC3416 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward dc current must be maintained through the SCR to retain an ac signal path. This requires that each subscriber-input to the array be capable of sourcing dc current as well as its ac signal. With each subscriber acting as a dc source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 21 shows this configuration. However, with each subscriber acting as a dc source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 22. Here both subscribers source dc current and exchange ac signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The dc

FIGURE 21 — INSTRUMENT-TO-TRUNK CONNECTION

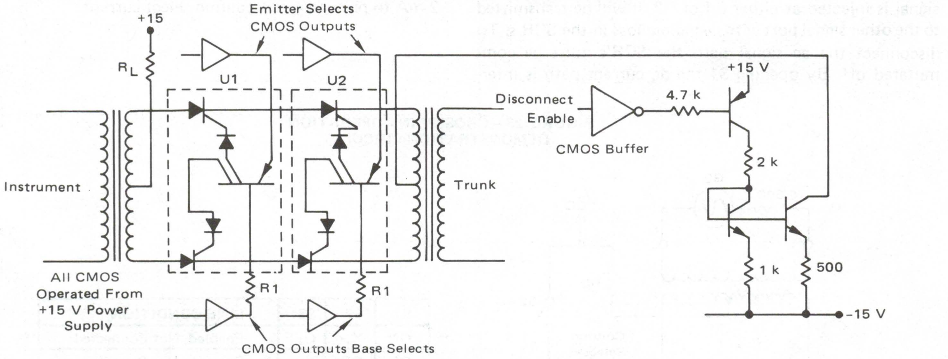
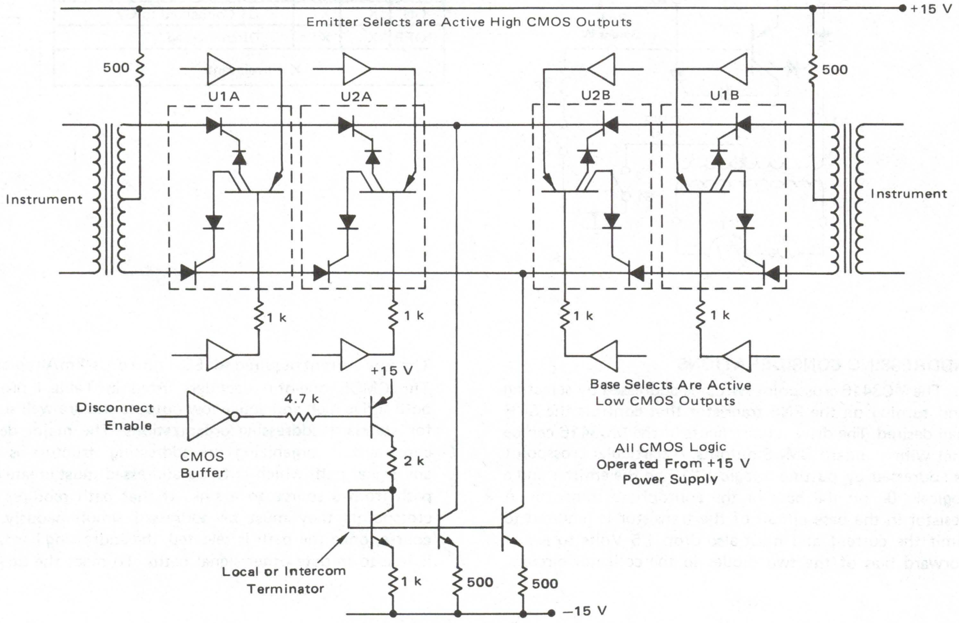

Emitter Selects
CMOS Outputs
+15
R_L
U1
U2
Instrument
Trunk
Disconnect
Enable
CMOS Buffer
4.7 k
+15 V
2 k
1 k
500
−15 V
R1
R1
All CMOS
Operated From
+15 V Power
Supply
CMOS Outputs Base Selects

FIGURE 22 – TYPICAL INSTRUMENT TO INSTRUMENT CONNECTION

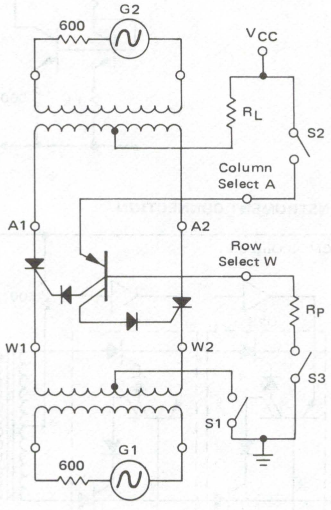

+15 V
Emitter Selects are Active High CMOS Outputs
500
500
U1A
U2A
U2B
U1B
Instrument
Instrument
1 k
1 k
1 k
1 k
+15 V
Disconnect
Enable
4.7 k
CMOS
Buffer
2 k
Base Selects Are Active
Low CMOS Outputs
All CMOS Logic
Operated From +15 V
Power Supply
Local or Intercom
Terminator
1 k
500
500
−15 V

current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 23 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCR's are off as they have no gate drive or dc current path through S1. By closing S2 and S3, gate drive is provided, but the SCR's still remain off as there is no dc current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed – current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an ac signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCR's. To disconnect the ac signal path the SCR's must be commutated off. By opening S1 the dc current path is interrupted and the SCR's switch off. The ac signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCR's simulate a relay contact in that the ac signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired dc current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(V_{CC} - V_{AK})/R_L = 20$ mA. The selection of R_P is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and R_P should drop at least 1.5 Volts. The PNP transistor has a typical gain of one. Thus, R_P should pass at least 2 mA to provide 4 mA column select current.

FIGURE 23– CROSSPOINT OPERATION DEMONSTRATION CIRCUIT



S1	S2	S3	LINE CONDITION
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected.

X = irrelevant

ADDRESSING CONSIDERATIONS

The MC3416 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the MC3416 can be met with standard CMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5 Volts to assure forward bias of the two diodes in the collector circuits. The gate current required for SCR turn on is 1 mA typically. The CMOS one-of-n decoders listed in Table I provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a dc path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the dc path

APPLICATIONS INFORMATION (continued)

requirement, crosspoint arrays should be designed in blocks such that any given dc path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two dc paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 22 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

TABLE I

	Active High Outputs	Active Low Outputs
Dual Binary to 1 of 4	MC14555	MC14556
4-bit latch/4 to 16	MC14514	MC14515
BCD to Decimal Decode	MC14028	

DISCONNECT TECHNIQUES

Since the crosspoint switch maintains signal paths by keeping dc currents through active SCR's, disconnects are easily accomplished by interrupting the dc current path. This can be done anywhere in the circuit, but if the disconnect is done at the terminator then all signal paths established to that terminator are broken simultaneously. In both Figures 21 and 22 this is done by turning off the current sink circuit with a CMOS buffer gate. MC14049 or MC14050 buffers will drive the transistor switch. Once a disconnect is completed, the terminator may be re-enabled and used for another call. Usage of the terminators may be easily monitored with optoelectronic couplers in the collectors of the current sinks without disturbing transmission characteristics.

MC3417, MC3517
MC3418, MC3518

MOTOROLA

Specifications and Applications Information

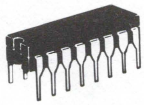
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

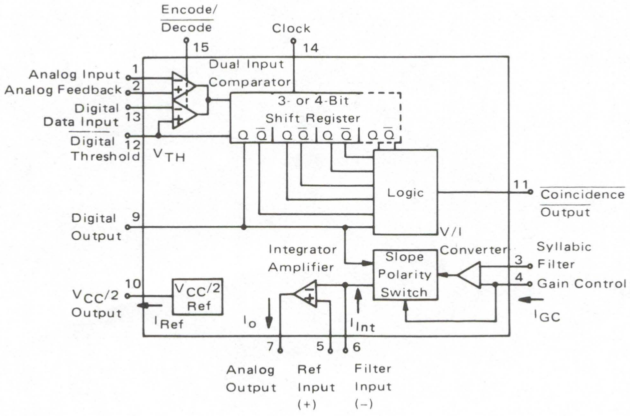
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT

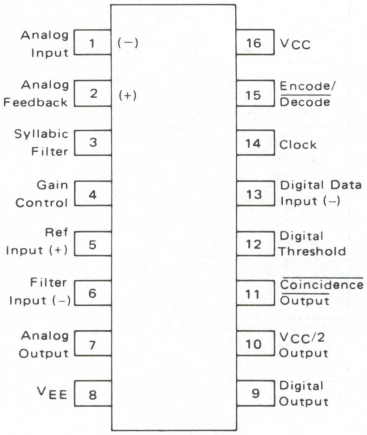


L SUFFIX
CERAMIC PACKAGE
CASE 620-02

CVSD BLOCK DIAGRAM


Encode/Decode
15
Clock
14
Analog Input
1
Analog Feedback
2
Digital Data Input
13
Digital Threshold
12
Dual Input Comparator
3- or 4-Bit Shift Register
Q Q̄ Q Q̄ Q Q̄ Q Q̄
V_TH
Logic
11
Coincidence Output
Digital Output
9
V/I Converter
Integrator Amplifier
Slope Polarity Switch
Syllabic Filter
3
4
Gain Control
I_GC
V_CC/2 Output
10
V_CC/2 Ref
I_Ref
I_o
I_Int
7
5
6
Analog Output
Ref Input (+)
Filter Input (−)

PIN CONNECTIONS


Analog Input 1 (−)
Analog Feedback 2 (+)
Syllabic Filter 3
Gain Control 4
Ref Input (+) 5
Filter Input (−) 6
Analog Output 7
V_EE 8
16 V_CC
15 Encode/Decode
14 Clock
13 Digital Data Input (−)
12 Digital Threshold
11 Coincidence Output
10 V_CC/2 Output
9 Digital Output

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, $T_A = 25^{\circ}C$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2 - 1.0$ to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ for MC3417/18, $T_A = -55^{\circ}C$ to $+125^{\circ}C$ for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.7	5.0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	–	$V_{CC} - 1.3$	1.3	–	$V_{CC} - 1.3$	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)	V_O	1.3	–	$V_{CC} - 1.3$	1.3	–	$V_{CC} - 1.3$	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							µA
Analog Input (I1)		–	0.5	1.5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							µA
Analog Input/Analog Feedback |I1−I2| – Figure 3		–	0.15	0.6	–	0.05	0.4	
Integrator Amplifier |I5−I6| – Figure 4		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) – Figure 5	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								µs
Clock Trigger to Digital Output (C_L = 25 pF to Gnd)	t_{PLH}	–	1.0	2.5	–	1.0	2.5	
	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output (C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage – Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current – High Logic State (V_{OH} = 15.0 V, $0^{\circ}C \leq T_A \leq 70^{\circ}C$)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	µA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

		MC3417/MC3517			MC3418/MC3518			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	V_{CC} − 2.0	+1.2	—	V_{CC} − 2.0	Vdc
Digital Threshold Input Current	$I_{I(th)}$							μA
(1.2 V ≤ V_{th} ≤ V_{CC} − 2.0 V)								
(V_{IL} applied to Pins 13, 14 and 15)		—	—	5.0	—	—	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		—	−10	−50	—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	±5.0	—	—	mA
V_{CC}/2 Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	+10	—	—	mA
V_{CC}/2 Generator Output Impedance (0 to +10 mA)	z_{Ref}	—	3.0	6.0	—	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance (4.75 V ≤ V_{CC} ≤ 16.5 V)	ϵr	—	—	±3.5	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	—	V_{th} − 0.4	Gnd	—	V_{th} − 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	—	18.0	V_{th} + 0.4	—	18.0	
Dynamic Total Loop Offset Voltage (Note 2) — Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12.0 μA, V_{CC} = 12 V								
T_A = 25°C		—	—	—	—	± 0.5	± 1.5	
0°C ≤ T_A ≤ +70°C MC3417/18		—	—	—	—	± 0.75	± 2.3	
−55°C ≤ T_A ≤ +125°C MC3517/18		—	—	—	—	± 1.5	± 4.0	
I_{GC} = 33.0 μA, V_{CC} = 12 V								
T_A = 25°C		—	± 2.5	± 5.0	—	—	—	
0°C ≤ T_A ≤ +70°C MC3417/18		—	± 3.0	± 7.5	—	—	—	
−55°C ≤ T_A ≤ +125°C MC3517/18		—	±4.5	± 10	—	—	—	
I_{GC} = 12.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		—	—	—	—	± 1.0	± 2.0	
0°C ≤ T_A ≤ +70°C MC3417/18		—	—	—	—	± 1.3	± 2.8	
−55°C ≤ T_A ≤ +125°C MC3517/18		—	—	—	—	± 2.5	± 5.0	
I_{GC} = 33.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		—	± 4.0	± 6.0	—	—	—	
0°C ≤ T_A ≤ +70°C MC3417/18		—	± 4.5	± 8.0	—	—	—	
−55°C ≤ T_A ≤ +125°C MC3517/18		—	± 5.5	± 10	—	—	—	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{OH} = −0.35 mA)	V_{OH}	V_{CC} − 1.0	V_{CC} − 0.2	—	V_{CC} − 1.0	V_{CC} − 0.2	—	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	—	V_{CC}	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int} \rvert$							
(I_{GC} = 12.0 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA)		1.45	1.50	1.55	1.45	1.50	1.55	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$	—	± 100	± 250	—	± 100	± 250	mV
Input Current — High Logic State	I_{IH}							μA
(V_{IH} = 18 V)								
Digital Data Input		—	—	+5.0	—	—	+5.0	
Clock Input		—	—	+5.0	—	—	+5.0	
Encode/$\overline{\text{Decode}}$ Input		—	—	+5.0	—	—	+5.0	
Input Current — Low Logic State	I_{IL}							μA
(V_{IL} = 0 V)								
Digital Data Input		—	—	−10	—	—	−10	
Clock Input		—	—	−360	—	—	−360	
Encode/$\overline{\text{Decode}}$ Input		--	—	−36	—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	—	—	−72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 – Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 – Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and pin 3. The active voltage to current (V-I) converter drives pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_x resistance. Figure 6 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_x resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is tied to pin 10.

Pin 6 – Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into pin 6 when the analog input (pin 1) is high with respect to the analog feedback (pin 2) in the encode mode or when the digital data input (pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between pins 6 and 7. Multipole configurations will have different circuitry. The resistance between pins 6 and 7 should always be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 – Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 – V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 – $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long

DEFINITIONS AND FUNCTIONS OF PINS (continued)

while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 – Digital Threshold

This input sets the switching threshold for pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is applied to pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 µs before and after the clock trigger for proper clocking.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 – Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 – POWER SUPPLY CURRENT

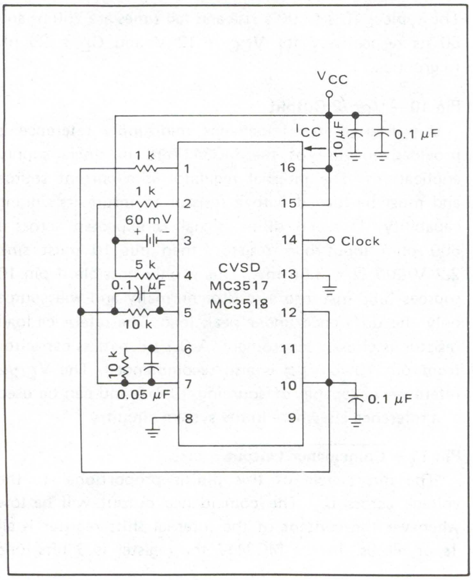
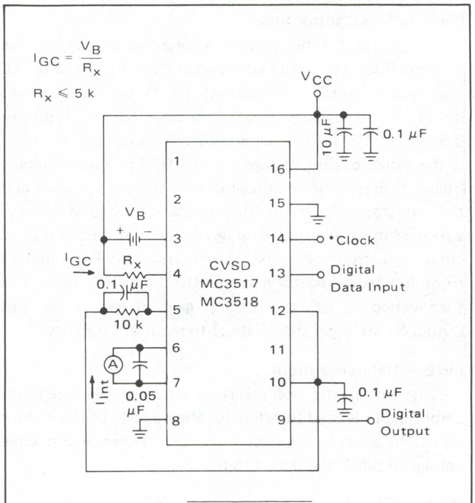


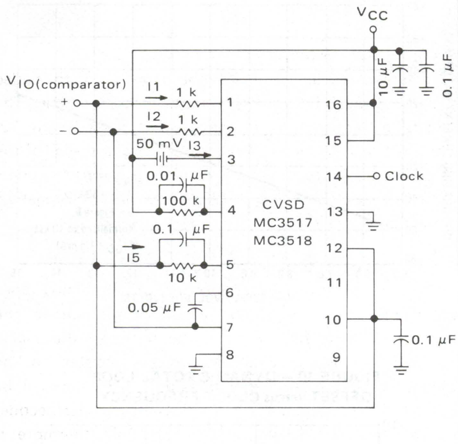
FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{Int} – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT


VCC
10 μF
0.1 μF
VIO(comparator)
+
–
I1
1 k
I2
1 k
50 mV
I3
0.01 μF
100 k
0.1 μF
I5
10 k
0.05 μF
CVSD
MC3517
MC3518
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
Clock
0.1 μF

Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

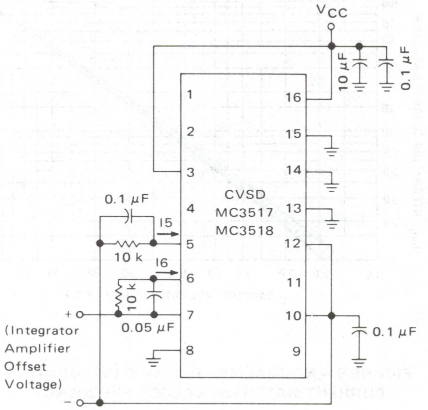
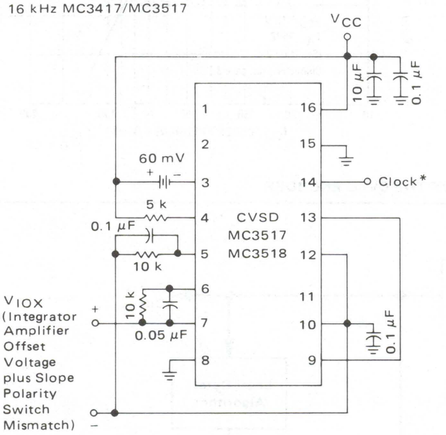

VCC
10 μF
0.1 μF
CVSD
MC3517
MC3518
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
0.1 μF
I5
10 k
I6
10 k
0.05 μF
+
(Integrator Amplifier Offset Voltage)
–
0.1 μF

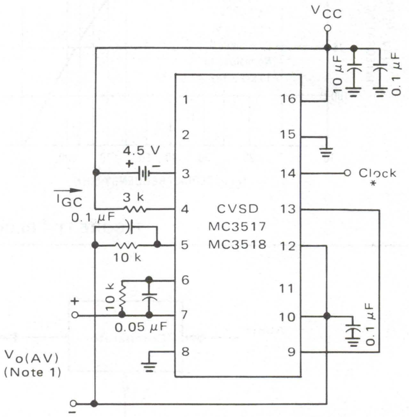
FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}

*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517


VCC
10 μF
0.1 μF
CVSD
MC3517
MC3518
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
60 mV
+
–
Clock*
5 k
0.1 μF
10 k
10 k
0.05 μF
0.1 μF
VIOX
(Integrator Amplifier Offset Voltage plus Slope Polarity Switch Mismatch)
+
–

Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH


VCC
10 μF
0.1 μF
CVSD
MC3517
MC3518
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
4.5 V
+
–
Clock*
IGC
3 k
0.1 μF
10 k
10 k
0.05 μF
+
Vo(AV)
(Note 1)
–
0.1 μF

*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{o(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

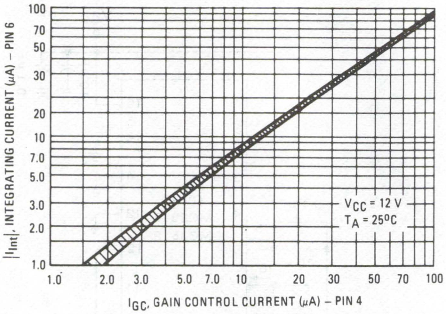


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

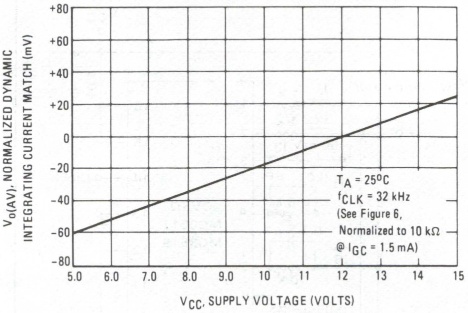


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

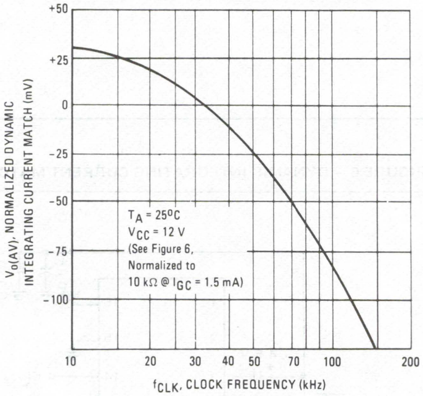


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

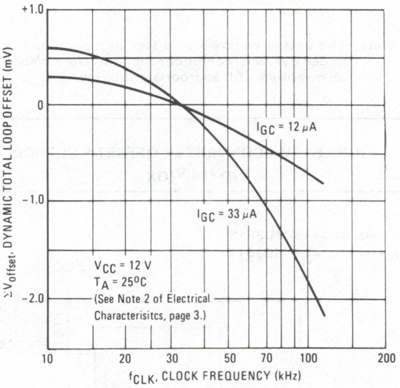


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

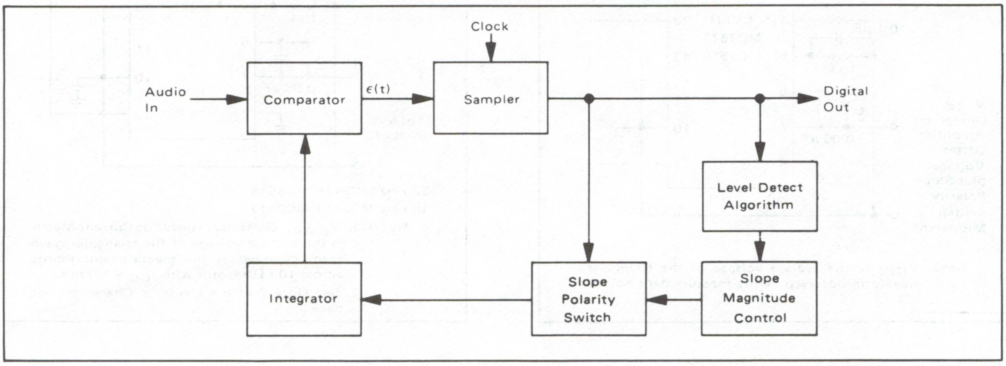

Clock
Audio In
Comparator
ε(t)
Sampler
Digital Out
Level Detect Algorithm
Slope Magnitude Control
Slope Polarity Switch
Integrator

FIGURE 12 – CVSD WAVEFORMS

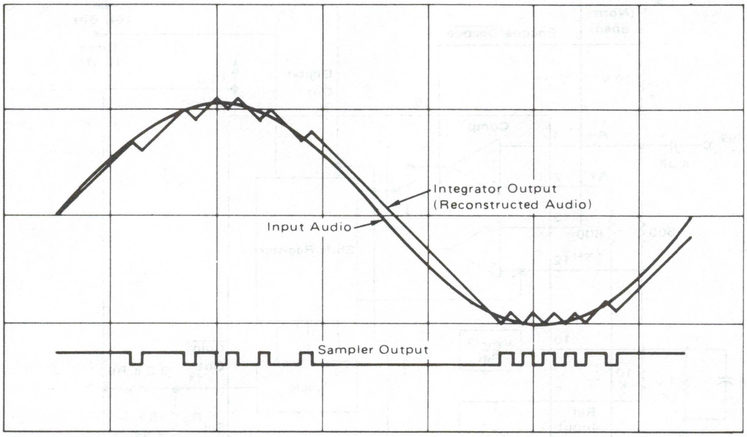


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

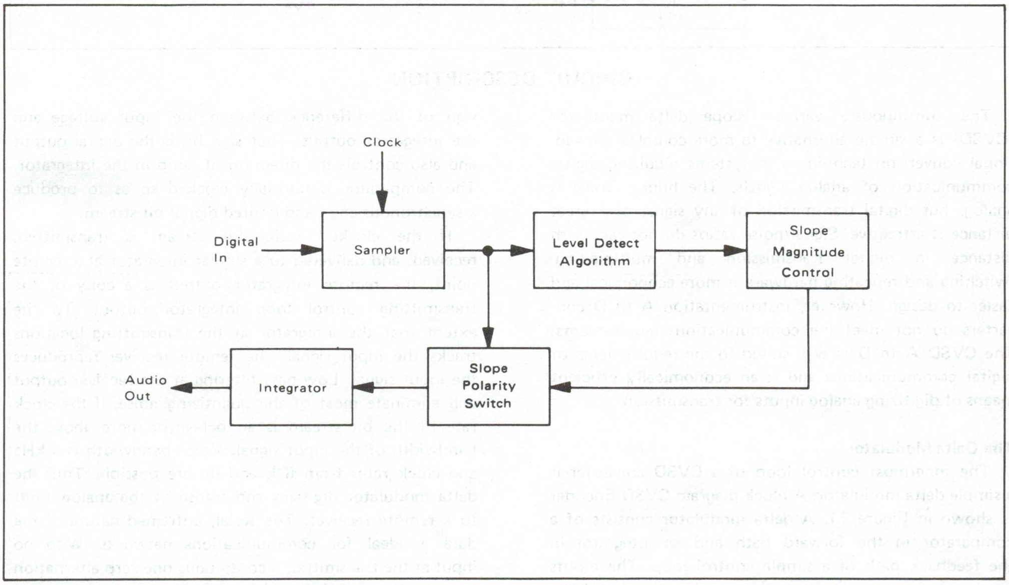
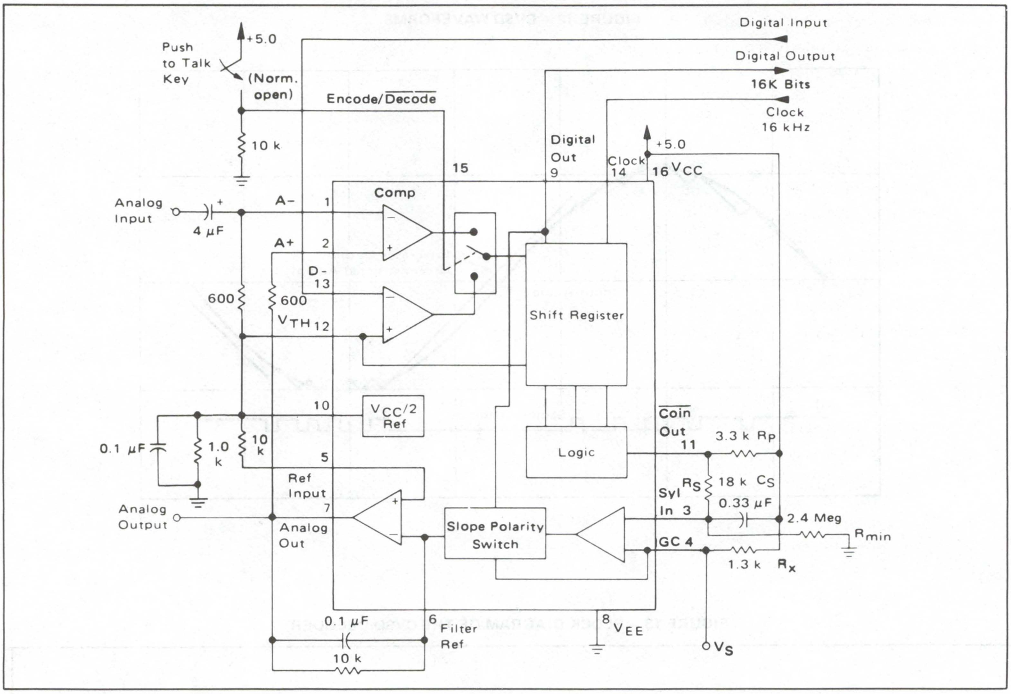

Clock
Digital In
Sampler
Level Detect Algorithm
Slope Magnitude Control
Slope Polarity Switch
Integrator
Audio Out

FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)


+5.0
Push
to Talk
Key
(Norm.
open)
Encode/$\overline{\text{Decode}}$
Digital Input
Digital Output
16K Bits
Clock
16 kHz
10 k
Digital
Out
9
Clock
14
+5.0
16 V_{CC}
15
Analog
Input
4 μF
A−
1
Comp
A+
2
D−
13
600
600
V_{TH} 12
Shift Register
10
$V_{CC}/2$
Ref
$\overline{\text{Coin}}$
Out
11
3.3 k R_P
0.1 μF
1.0
k
10
k
5
Logic
Ref
Input
7
R_S
18 k C_S
0.33 μF
Syl
In 3
2.4 Meg
R_{min}
Analog
Output
Analog
Out
Slope Polarity
Switch
GC 4
1.3 k R_x
0.1 μF
6
Filter
Ref
8
V_{EE}
V_S
10 k

CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

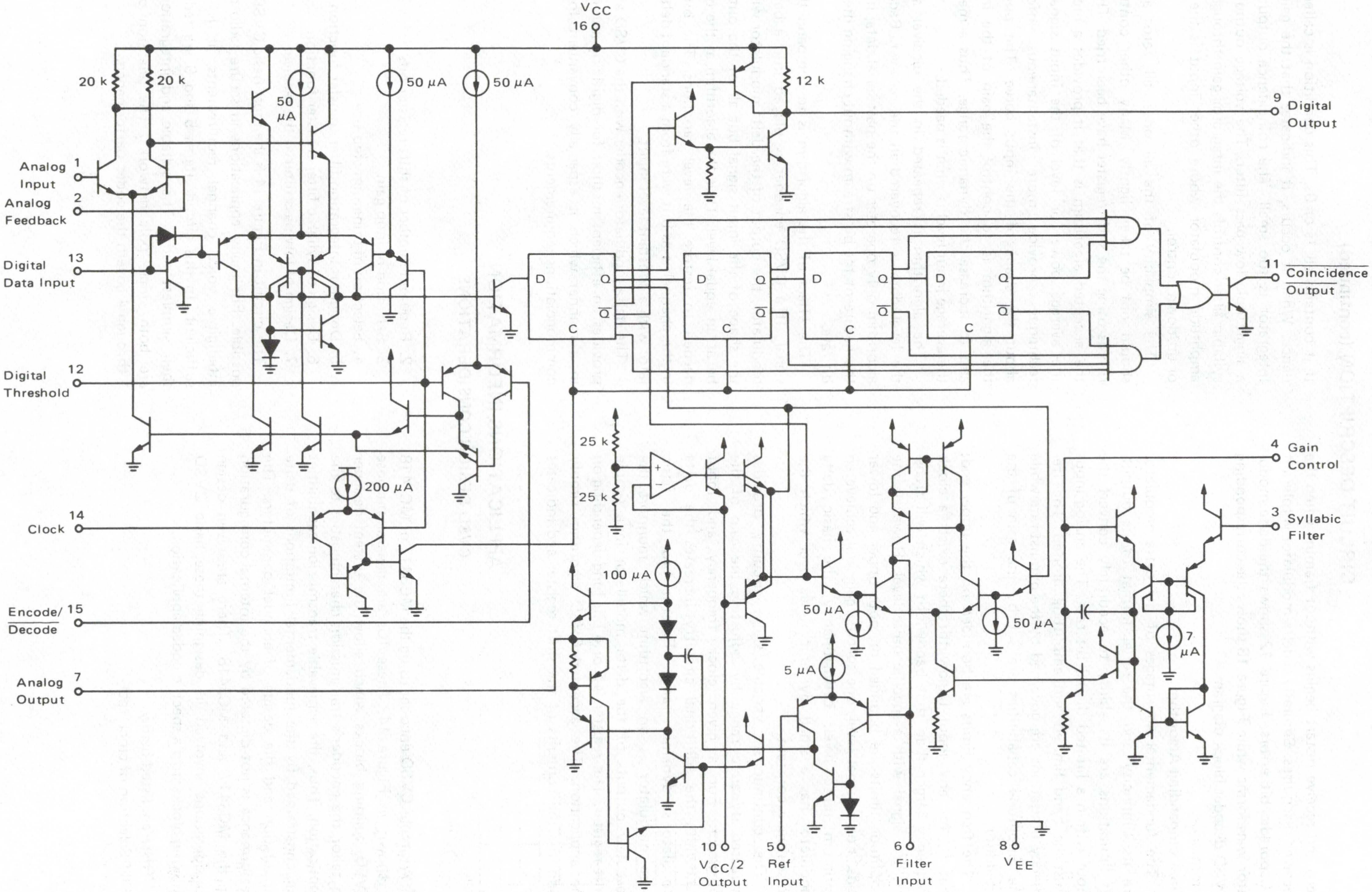
A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

CVSD CIRCUIT SCHEMATIC


VCC
16
20 k
20 k
50 µA
50 µA
50 µA
12 k
9 Digital Output
Analog Input 1
Analog Feedback 2
Digital Data Input 13
D
Q
Q̅
C
11 Coincidence Output
Digital Threshold 12
25 k
25 k
4 Gain Control
200 µA
Clock 14
3 Syllabic Filter
100 µA
Encode/Decode 15
50 µA
50 µA
7 µA
5 µA
Analog Output 7
10 VCC/2 Output
5 Ref Input
6 Filter Input
8 VEE

CVSD DESIGN CONSIDERATIONS (continued)

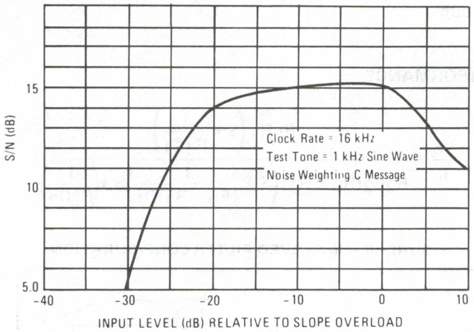
Layout Considerations

Care should be exercised to isolate all digital signal paths (pins 9, 11, 13, and 14) from analog signal paths (pins 1-7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ \text{k}\Omega,\ C = 0.1\ \mu\text{F}$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ \text{Hz}$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R} + \frac{C_d V_o}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ \text{V}}{{}^{*}2(10\ \text{k}\Omega)} + \frac{0.1\ \mu\text{F}(1.1)}{0.125\ \text{ms}} = 0.935\ \text{mA}$$

*The maximum voltage across RI when maximum slew is required is:

$$\frac{1.1\ \text{V}}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_x = 0.25(V_{CC})\ \frac{1}{0.935\ \text{mA}}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

CVSD DESIGN CONSIDERATIONS (continued)

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 33\ \mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_x.

$$I_i R_x = V_{Smin}\text{; for } 33\ \mu A,\ V_{Smin} = 41.6\ mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \qquad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters – clock rate, number of shift register bits, loop gain and minimum step size – the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

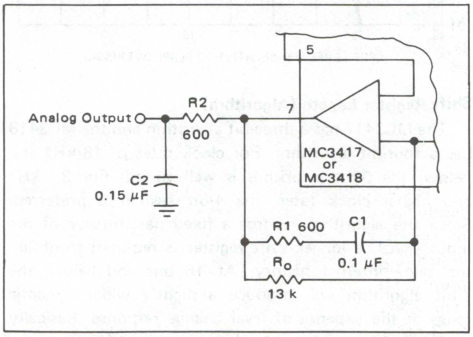
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 – IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on pin 1.

INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}.$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

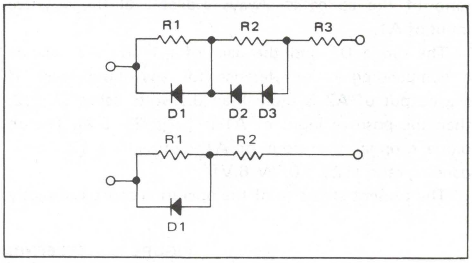
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is $(V_{CC}/2 - 0.7)$. The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

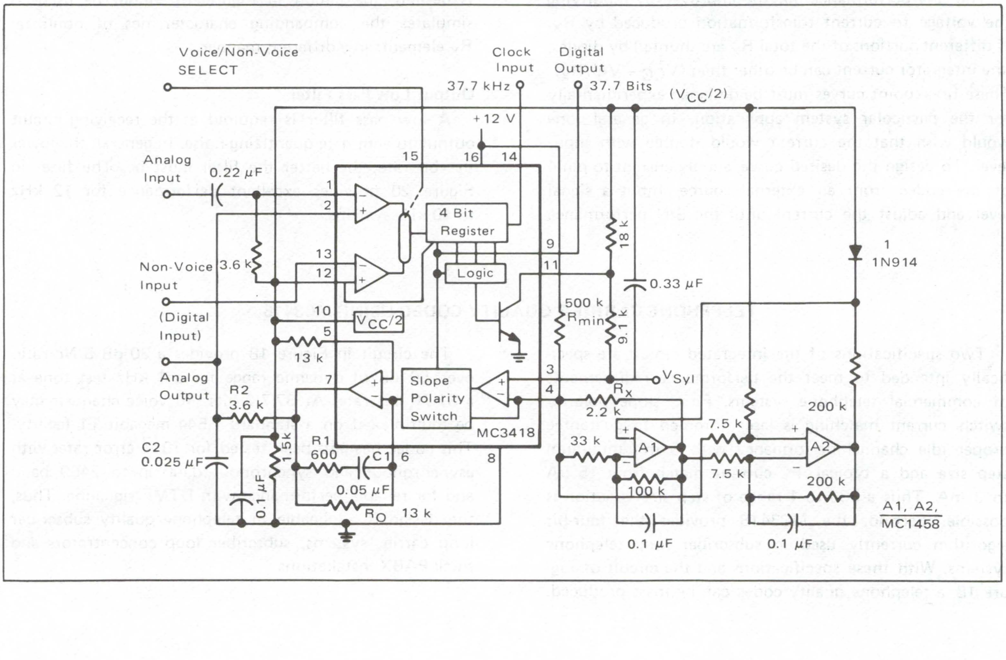
The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

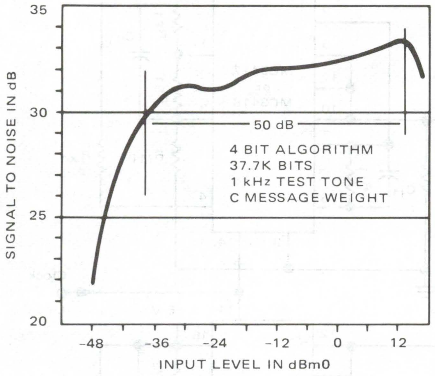
(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)


Voice/Non-Voice SELECT
Clock Input
37.7 kHz
Digital Output
37.7 Bits
(VCC/2)
+12 V
Analog Input
0.22 μF
15
16
14
1
2
4 Bit Register
9
18 k
1
1N914
Non-Voice Input
3.6 k
13
12
Logic
11
0.33 μF
(Digital Input)
10
VCC/2
5
500 k
Rmin
9.1 k
13 k
Analog Output
7
Slope Polarity Switch
3
4
VSyl
R2 3.6 k
Rx
2.2 k
200 k
MC3418
7.5 k
C2 0.025 μF
R1 600
C1
6
8
33 k
A1
A2
1.5k
0.1 μF
0.05 μF
RO
13 k
7.5 k
100 k
200 k
A1, A2, MC1458
0.1 μF
0.1 μF

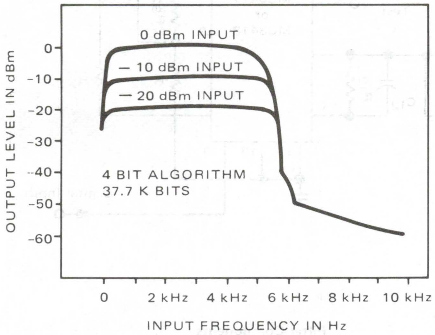
TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

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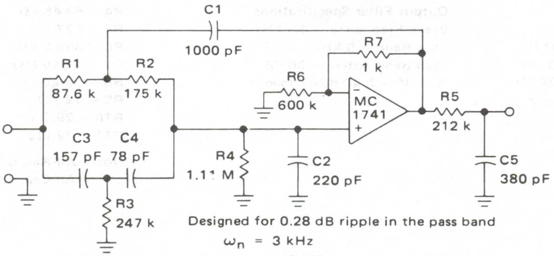
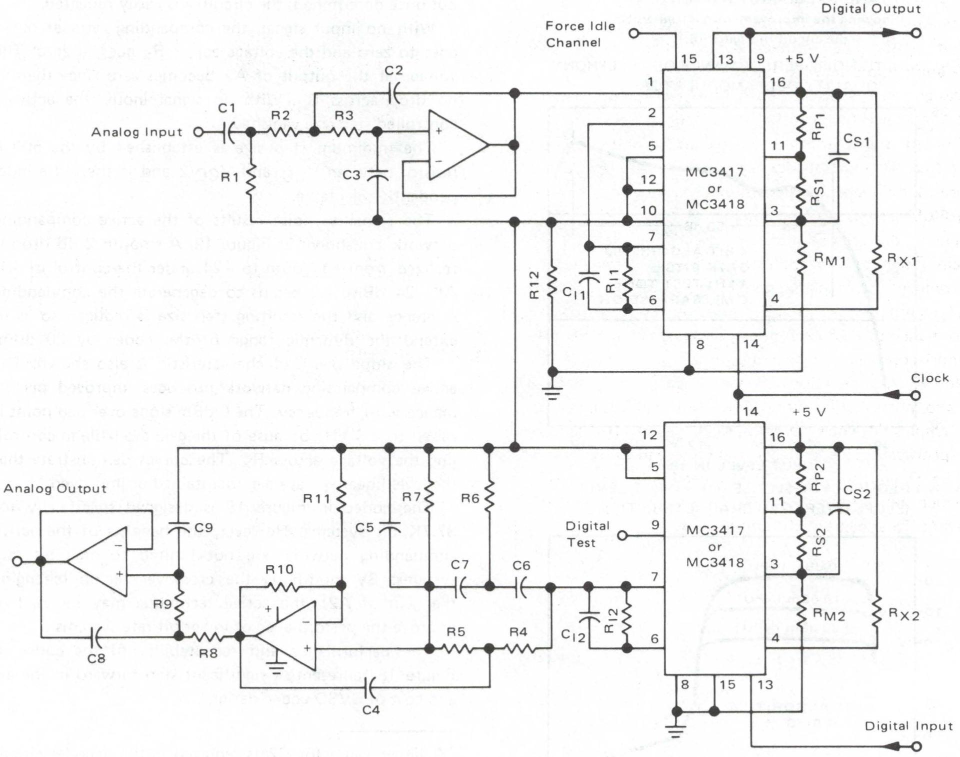
*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
ω_n = 3 kHz
ω_s = ≅ 6 kHz
AdB at ω_s and above 29.5 dB

FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP


Digital Output
Force Idle Channel
15
13
9
+5 V
1
16
2
5
11
12
10
7
3
4
6
8
14
MC3417 or MC3418
R_P1
C_S1
R_S1
R_M1
R_X1
C2
C1
R2
R3
C3
R1
Analog Input
R12
C_I1
R_I1
Clock
14
+5 V
12
16
5
11
9
3
7
4
6
8
15
13
MC3417 or MC3418
R_P2
C_S2
R_S2
R_M2
R_X2
Digital Test
C_I2
R_I2
Digital Input
Analog Output
R11
R7
R6
C9
C5
R10
C7
C6
R9
R5
R4
C8
R8
C4

Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} – 5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 kΩ
R11 – 72 kΩ

C1 – 3.3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

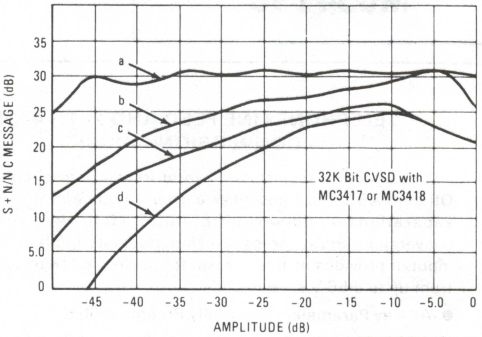
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 — COMPARATIVE CODEC PERFORMANCE — SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18 — MC3418)

Curve b — Double integration (Figure 21 using Figure 6 — MC3418)

Curve c — Single integration (Figure 21 — MC3418) with 6 mV step size

Curve d — Single integration (Figure 21 — MC3417) with 25 mV step size

MC3419
MC3419A
MC3419C

MOTOROLA

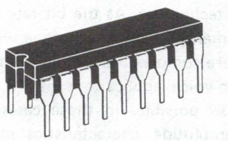
TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Central Office, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 56 V supply

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

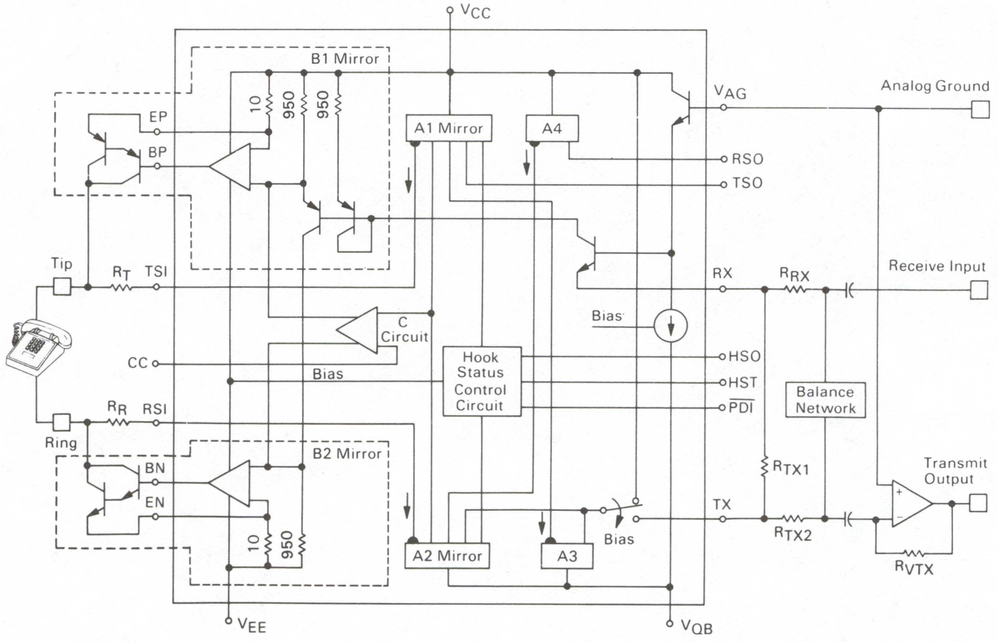
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

FUNCTIONAL BLOCK DIAGRAM


VCC
B1 Mirror
10
950
950
EP
BP
A1 Mirror
A4
VAG
Analog Ground
RSO
TSO
Tip
RT
TSI
RX
RRX
Receive Input
C Circuit
Bias
CC
Bias
Hook Status Control Circuit
HSO
HST
PDI
Balance Network
RR
RSI
Ring
B2 Mirror
BN
EN
RTX1
Transmit Output
TX
RTX2
RVTX
10
950
A2 Mirror
A3
Bias
VEE
VQB

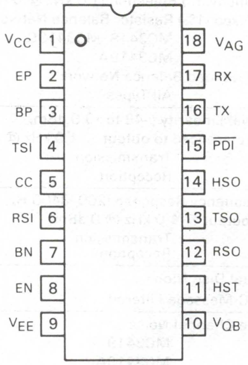
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage (Referenced to V_{CC})	V_{EE} V_{QB}	-60 V_{EE} -1	Vdc
Sense Current Steady State Pulse - Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	20 to 120	mA
Voltage	V_{EE} V_{QB}	-20 to -56 -20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to -12 -2.5 to -12	Vdc
Supervisory Output Voltage	V_{RSO}, V_{TSO}, V_{HSO}	-2.0 to -20	Vdc

PIN CONNECTIONS



PIN DESCRIPTIONS

Name	Function
V_{CC}	The most positive supply voltage. This point is Earth Ground in most typical applications.
BP & BN	Are the base drive outputs for the PNP and NPN Darlington transistors.
EP & EN	Are loop current sensing inputs and are connected to the emitter of the PNP & NPN Darlington transistors.
TSI & RSI	Are the tip and ring current sensing inputs. They are low impedance inputs (approximately 600 Ω each) that translate the voltage on tip and ring to a current through Resistors R_T and R_R.
CC	Compensation capacitor input.
V_{EE}	Is the most negative supply voltage.
V_{QB}	Is the quiet battery connection. The voltage on this pin must not go more negative than V_{EE}.
HST	Hook Status Threshold programming resistor input pin. This pin programs the value of loop resistance which determines on-hook or off-hook status.
RSO	Ring Sense current Output. This output reflects the status of the Ring terminal. The current is sourced from this output and is one-sixth I_{RSI}.
TSO	Tip Sense current Output. This output reflects the status of the Tip terminal. The current is sourced from this output and is one-sixth I_{TSI}.
HSO	Hook Status Output. This is a digital output (open collector PNP) that sources current when the loop resistance is less than the threshold resistance value set by R_H.
$\overline{PDI}$	Power-Down Input pin. A logic level "0" powers down the MC3419.
TX	Transmit current output. This output sinks current proportional to I_{TSI} + I_{RSI}.
RX	Receive input. This input sums the currents from the TX output and signal input. This pin has a low input impedance.
V_{AG}	Analog ground reference supply voltage input.

ELECTRICAL CHARACTERISTICS (V_{EE} = -48 V, V_{QB} = -48 V, V_{AG} = -6.0 V, R_L = 900 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transhybrid Gain Variation (1.0 kHz @ 0 dBm Input)	1					dB
Transmission/Reception						
MC3419		V_{TX}/V_L,	-0.3	0	+0.3	
MC3419A		V_L/V_{RX}	-0.15	0	+0.15	
MC3419C			-0.4	0	+0.4	
Transhybrid Rejection (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_{RX}				dB
Fixed (1%) Resistor Balance Network						
MC3419, MC3419C			-23	—	—	
MC3419A			-33	—	—	
Trimmed Balance Network						
All Types			—	-55	—	
Level Linearity (-48 to +3.0 dBm, referenced to output @ 1.0 kHz @ 0 dBm)	1					dB
Transmission		V_{TX}/V_L	-0.1	0	+0.1	
Reception		V_L/V_{RX}	-0.1	0	+0.1	
Frequency Response (200-3400 Hz, referenced to output @ 1.0 kHz @ 0 dBm)	1					dB
Transmission		V_{TX}/V_L	-0.1	0	+0.1	
Reception		V_L/V_{RX}	-0.1	0	+0.1	
Total Distortion	1	V_L/V_{RX}	—	-60	—	dB
C-Message Filtered		V_{TX}/V_L	—	-60	—	
Idle Channel Noise	1	V_{TX}				dBrnc0
MC3419			—	—	13	
MC3419A			—	—	10	
MC3419C			—	—	18	
Termination Resistance Tolerance @ 1.0 kHz	1	ΔR_o				%
MC3419A			—	—	±3.0	
MC3419, MC3419C			—	—	±5.0	
Longitudinal Induction — 60 Hz (I_L = 30 to 100 mA, I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnc0
Longitudinal Balance	2	V_{TX}/V_{LON}				dB
MC3419 (200-3400 Hz)			-45	—	—	
MC3419A (200-1000 Hz)			50	—	—	
MC3419A (3000 Hz)			48	—	—	
MC3419C (200-3400 Hz)			-40	—	—	
Propagation Delay	1	T_P, V_{RX} to V_L	—	750	—	ns
		V_{RX} to I_{TX}	—	1.2	—	µs
Power Dissipation (R_L > 100 MΩ)		P_D				mW
MC3419, MC3419A			—	1.0	—	
MC3419C			—	2.5	—	
Supply Current — On-Hook (V_{EE} = V_{QB} = -56 V, R_L > 100 MΩ)		I_{CC}				µA
MC3419, MC3419A			—	40	200	
MC3419C			—	100	500	
Power Supply Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{ee}				dB
MC3419, MC3419A			-40	—	—	
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{qb}	—	-6.0	—	dB
Sense Current	4					mA/mA
Tip		I_{TSO}/I_{TSI}	0.15	0.17	0.19	
Ring		I_{RSO}/I_{RSI}	0.15	0.17	0.19	
Fault Currents — On-Hook	1					mA
Tip to V_{CC}		I_{Tip}	—	0	—	
Ring to V_{CC}		I_{Ring}	—	2.5	—	
Tip to Ring		I_{Loop}	—	120	—	
Tip & Ring to V_{CC}		I_{Tip} & I_{Ring}	—	2.5	—	
Analog Ground Current		I_{AG}	—	1.0	10	µA
Power Down Logic Levels		$I_{\overline{PDI}}$	—	-1.0	—	µA
		V_{IH}	-1.2	0	—	Vdc
		V_{IL}	-20	—	-4.0	Vdc
Hook Status Output Current	1	I_{HSO}				µA
(R_L < 2.5 kΩ, $\overline{PDI}$ = Logic 1)			200	400	—	
(R_L > 10 kΩ, or $\overline{PDI}$ = Logic 0)			—	0	2.0	

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram, line-sensing resistors at TSI and RSI convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. The output of A1 is mirrored by A3 and summed together with an output of A2 at the TX terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TX output.

All the dc current at the TX output is fed back through the RX terminal to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a low gain output (×1) of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (×95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TX output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less than the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TX output were returned to the B1 input along with the dc current. Instead, the MC3419 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp and a feedback resistor external to the MC3419 which produce the transmit output at the 4-wire interface. The transhybrid transmission gain is programmed by the op amp feedback resistor.

Transhybrid reception is realized by converting the ac coupled receive input voltage to a current through an external resistor at the low impedance RX terminal. This current is summed at RX with the dc and ac feedback current from the A-Circuit mirror and drives the B1 mirror input. The B-Circuit mirror outputs drive the line with balanced ac current proportional to the receive input voltage. The transhybrid reception gain is programmed by the resistor at the RX input.

Since receive input signals are transmitted through the MC3419 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419 by two methods. The first mode of suppression is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit and summed together at TX, the total current at TX remains unchanged. Therefore, the ac currents due to the common-mode signals are cancelled before reaching the transmit output.

The second longitudinal suppression method is dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals. Through an error-detecting circuit, the input of which is a difference current between outputs of A1 and A2, the impedance at Tip and Ring to longitudinal currents is kept very low. This is accomplished with a high gain C-Circuit which produces B1 and B2 output currents that are equal and in phase to cancel the longitudinal line currents. Operation of this circuit does not affect the dc line-current or the processing of normal differential line signals.

The hook-status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419. If the $\overline{\text{PDI}}$ pin is a logic "one", the control circuit senses two outputs from the A1 and A2 mirrors. If both of these output currents are greater than the preprogrammed current at the HST terminal, the control circuit supplies currents to power up the SLIC. At the same time it activates a digital status output, HSO.

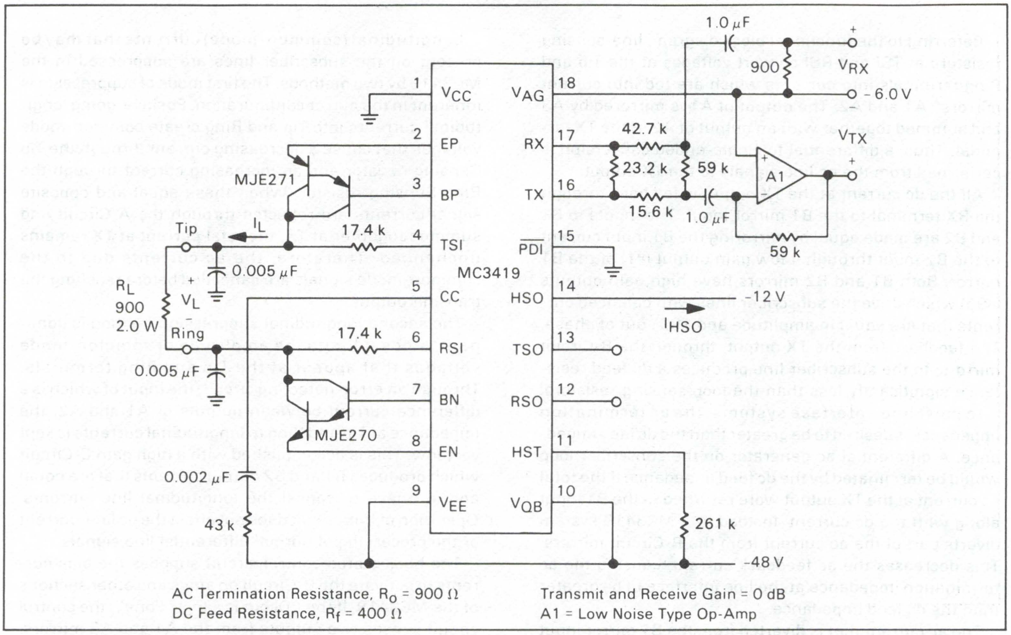
In addition to the digital hook status output, the condition of Tip and Ring can be monitored at the TSO and RSO outputs of the MC3419. These outputs source currents proportional to the TSI and RSI input currents respectively, and operate independently of the $\overline{\text{PDI}}$ logic input.

The MC3419 has two negative battery terminals. V_{EE} supplies the high current through the B2 mirror to drive the line. B2 has a high output impedance and battery noise will not be coupled to the line from the V_{EE} terminal. However, V_{QB} is quite sensitive to noise, since the line-sensing resistor is referenced to this pin through the A2 mirror, and should be bypassed with a filter network to guarantee a high rejection of battery noise.

The V_{AG} input also plays a key role in reducing power-supply related noise that can occur when the MC3419 system is coupled to a switching system. The analog ground isolates the 4-wire receive and transmit signal paths from noise on the system power ground by establishing a common ac signal reference.

*A current mirror is a circuit which behaves as a current controlled, current source. It has a single low-impedance input terminal and one or more high impedance outputs.

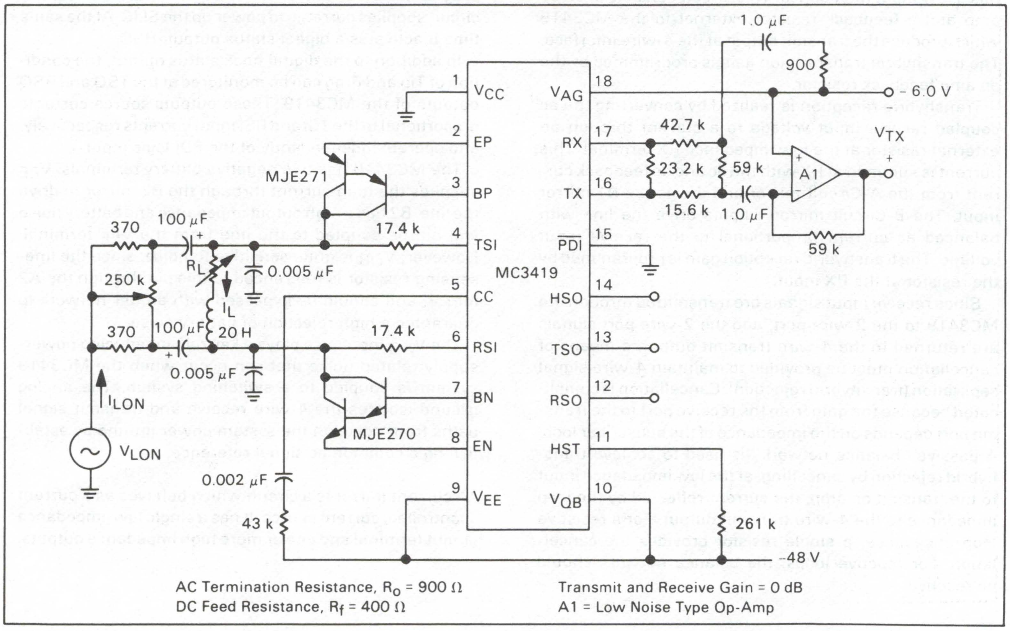
FIGURE 1 — AC TEST CIRCUIT


1.0 μF
900
V_{RX}
−6.0 V
1 V_{CC}
V_{AG} 18
2 EP
RX 17
42.7 k
V_{TX}
MJE271
23.2 k
59 k
A1
3 BP
TX 16
15.6 k
1.0 μF
Tip
I_L
17.4 k
4 TSI
$\overline{PDI}$ 15
59 k
0.005 μF
MC3419
R_L
900
2.0 W
V_L
5 CC
HSO 14
−12 V
Ring
I_{HSO}
17.4 k
6 RSI
TSO 13
0.005 μF
7 BN
RSO 12
MJE270
8 EN
HST 11
0.002 μF
9 V_{EE}
V_{QB} 10
43 k
261 k
−48 V

AC Termination Resistance, R_O = 900 Ω
DC Feed Resistance, R_f = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = Low Noise Type Op-Amp

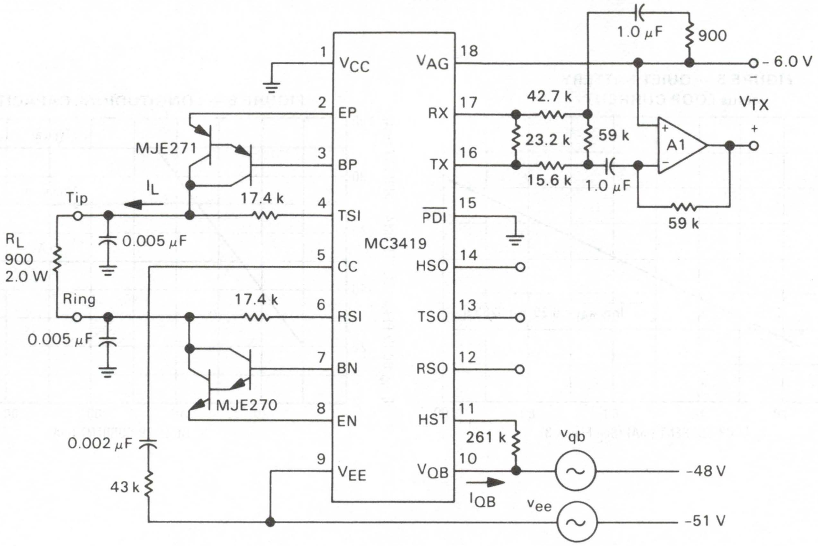
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT


1.0 μF
900
−6.0 V
1 V_{CC}
V_{AG} 18
2 EP
RX 17
42.7 k
V_{TX}
MJE271
23.2 k
59 k
A1
3 BP
TX 16
15.6 k
1.0 μF
370
100 μF
17.4 k
4 TSI
$\overline{PDI}$ 15
59 k
R_L
250 k
0.005 μF
MC3419
I_L
5 CC
HSO 14
370
100 μF
20 H
17.4 k
6 RSI
TSO 13
0.005 μF
I_{LON}
7 BN
RSO 12
MJE270
8 EN
HST 11
V_{LON}
0.002 μF
9 V_{EE}
V_{QB} 10
43 k
261 k
−48 V

AC Termination Resistance, R_O = 900 Ω
DC Feed Resistance, R_f = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = Low Noise Type Op-Amp

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT


1.0 μF
900
-6.0 V
1 VCC
VAG 18
2 EP
RX 17
42.7 k
VTX
23.2 k
59 k
A1
MJE271
3 BP
TX 16
15.6 k
1.0 μF
IL
17.4 k
Tip
4 TSI
PDI 15
59 k
RL
900
2.0 W
0.005 μF
MC3419
5 CC
HSO 14
Ring
17.4 k
6 RSI
TSO 13
0.005 μF
7 BN
RSO 12
MJE270
8 EN
HST 11
0.002 μF
261 k
vqb
9 VEE
VQB 10
-48 V
43 k
IQB
vee
-51 V

AC Termination Resistance, R_o = 900 Ω
DC Feed Resistance, R_f = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = Low Noise Type Op-Amp

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

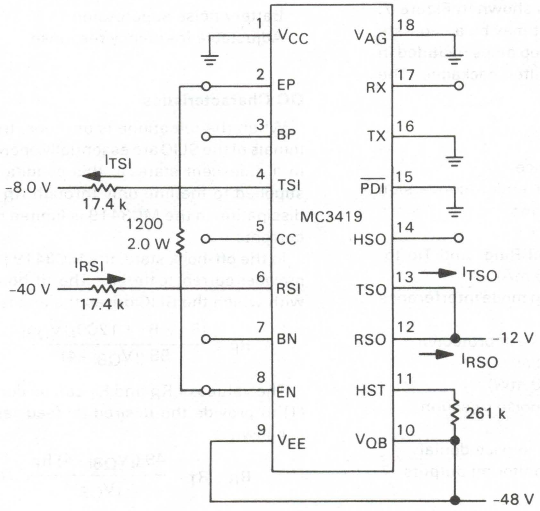

1 VCC
VAG 18
2 EP
RX 17
3 BP
TX 16
ITSI
4 TSI
PDI 15
-8.0 V
17.4 k
MC3419
1200
2.0 W
5 CC
HSO 14
IRSI
6 RSI
TSO 13
ITSO
-40 V
17.4 k
7 BN
RSO 12
-12 V
IRSO
8 EN
HST 11
261 k
9 VEE
VQB 10
-48 V

FIGURE 5 — QUIET BATTERY versus LOOP CURRENT

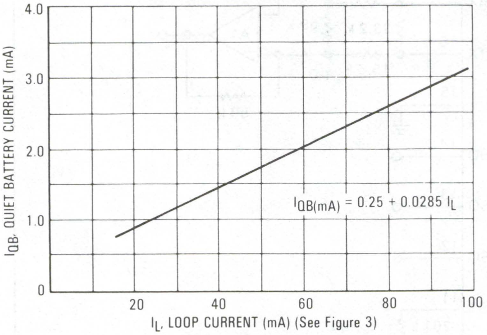
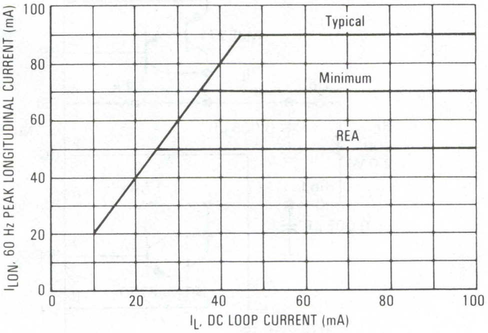


FIGURE 6 — LONGITUDINAL CAPACITY



APPLICATIONS INFORMATION

The Motorola Subscriber Loop Interface Circuit (SLIC) is comprised of a bipolar laser-trimmed integrated circuit, MC3419, two complimentary Darlington power transistors, MJE270 and 271, a bridge rectifier, MDA220, ten resistors, and five capacitors, as shown in Figure 7. The op amp providing the V_{TX} output may be a separate component or may be one of the two op amps included in the MC14413 or MC14414 PCM filter packages. The circuit of Figure 7 will provide:

Adjustable resistive dc power feed
Adjustable maximum loop range
Adjustable ac termination impedance
2-wire balanced to 4-wire single ended conversion
Adjustable transmit and receive gains
Independent transhybrid null
Ring-to-ground, Tip-to-ground, and Ring- and Tip-to-ground fault current limiting (2.5 mA)
Rejection of longitudinal or common mode interference from dc to greater than 4.0 kHz
1500 volt secondary lightning transient protection
Temporary power-line fault protection
On-hook power-down (less than 10 mW)
Floating 4-wire common input for noise rejection
Hook-status output signal
Power-down control for subscriber service denial
Continuous Tip and Ring status monitoring outputs
Wide battery range (20 V to 56 V)

In addition, the SLIC can provide the following optional features:

Constant current battery feed
Current limiting battery feed
Battery noise suppression
Adjustable frequency response

DC Characteristics

When the telephone is on-hook, the Tip and Ring terminals of the SLIC are essentially open and the MC3419 is in a quiescent state. In this condition, current is being supplied to the line only through R_R and R_T and power dissipation in the MC3419 is limited primarily to leakage currents.

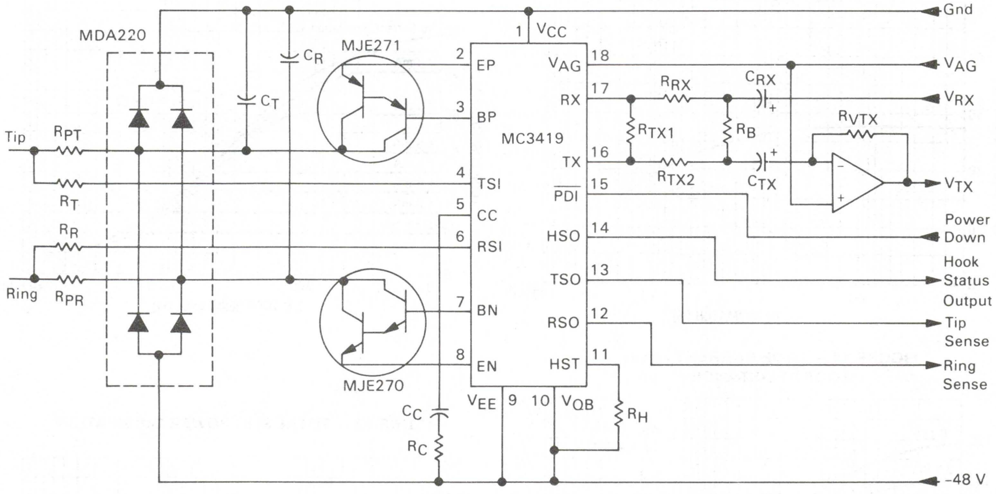
In the off-hook state, the MC3419 powers itself up and provides current to the line. The off-hook dc feed resistance with which the SLIC drives the line is given by

$$R_F = \frac{(R_R + R_T + 1200)\,|V_{QB}|}{98\,(|V_{QB}|\ -4)} \qquad (1)$$

The values of R_R and R_T can be derived from equation (1) to provide the desired dc feed resistance once V_{QB} is known.

$$R_R = R_T = \frac{49\,(|V_{QB}|\ -4)\,R_F}{|V_{QB}|} - 600 \qquad (2)$$

FIGURE 7 — SLIC CIRCUIT


Gnd
MDA220
CR
MJE271
CT
Tip
RPT
RT
RR
Ring
RPR
MJE270
1 VCC
2 EP
3 BP
4 TSI
5 CC
6 RSI
7 BN
8 EN
VEE 9
10 VQB
MC3419
18 VAG
17 RX
16 TX
15 PDI
14 HSO
13 TSO
12 RSO
11 HST
RRX
CRX
RTX1
RB
RTX2
CTX
RVTX
VAG
VRX
VTX
Power Down
Hook Status Output
Tip Sense
Ring Sense
CC
RC
RH
-48 V

The line-feed current flows between ground and V_{EE}; however, the control electronics is referenced to V_{QB} and ground. Therefore, the dc feed resistance appears to be referenced to V_{QB} and ground.

The matching of R_R and R_T is critical to a number of ac performance parameters as shown in Figures 8, 9 and 10. One percent tolerance or better is recommended for these resistors. In addition, these resistors must withstand any voltage transients on the line. Resistors able to withstand voltage transients of 1000 V or more are recommended.

FIGURE 8 — RETURN LOSS versus TIP/RING RESISTOR MISMATCH

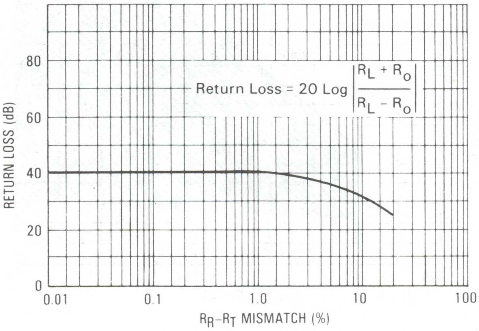
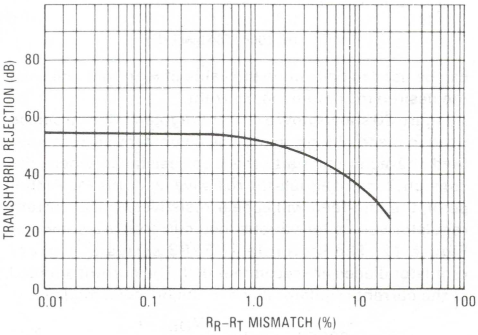


FIGURE 9 — TRANSHYBRID REJECTION versus TIP/RING RESISTOR MISMATCH



Power dissipation on short loops can be significantly reduced by either of two methods of current limiting. The dc feed resistance R_F is shown in equation (1) to be a function of V_{QB} as well as R_T and R_R. The current I_{QB} from the V_{QB} pin is proportional to loop current. Therefore, a resistor R_{QB} placed between the V_{QB} pin and V_{EE} supply will reduce the V_{QB} supply voltage as the loop current increases. This slightly increases the value of R_F while at the same time reducing the effective value of the battery voltage, thereby limiting loop current. Figure 11

FIGURE 10 — IMPEDANCE BALANCE versus TIP/RING RESISTOR MISMATCH

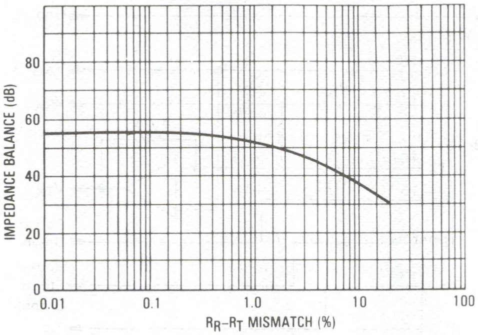
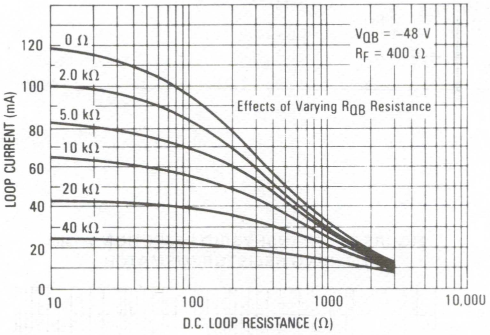


FIGURE 11 — LOOP CURRENT versus LOOP RESISTANCE



can be used to determine the value of R_{QB} that will yield the desired maximum loop current.

Figure 20 shows how a current regulator device can be used in place of R_{QB} to provide a constant current line-feed characteristic up to the loop resistance where the constant current equals the resistive feed current. At that point, the line-feed will appear resistive. Typical current regulator values for various loop currents are shown in Figure 12. The Motorola 1N5283 series of current regulator diodes are recommended. The current sourced to the current regulator diode in the off-hook mode is:

$$I_{QB} = 0.0285\, I_L + 0.25 + \frac{|V_{QB}| - 4}{R_H} \qquad 3(a)$$

I_L in mA, R_H in kΩ

In the on-hook mode the current is:

$$I_{QB} = 2.15\, I_{RSI} + 0.7\, I_{TSI} \qquad 3(b)$$

Figure 13 is a graph of SLIC power dissipation for both 400 Ω resistive battery feed and constant current battery feed, (or current limiting) showing the power savings of constant current techniques.

FIGURE 12 — LOOP CURRENT REGULATION

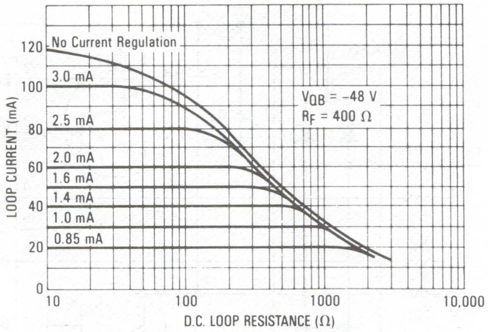


FIGURE 13 — TOTAL SLIC POWER DISSIPATION

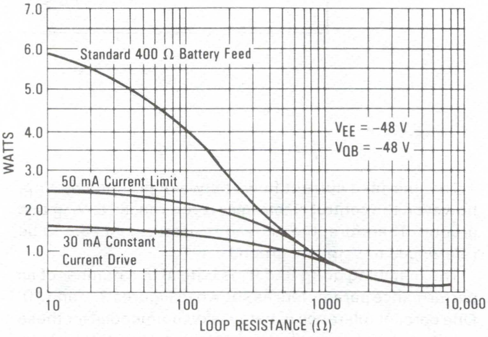
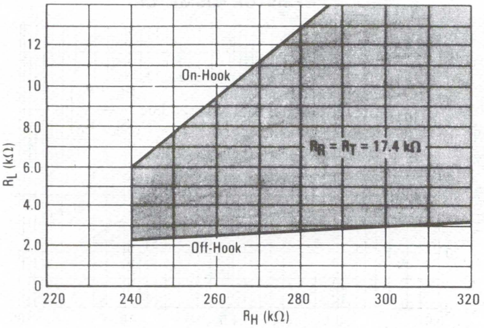


FIGURE 14 — HOOK STATUS DETECTION



Either R_{QB} or the current regulator diode and a capacitor to V_{CC} provide an effective means of filtering any noise on the V_{EE} line and prevent it from reaching the V_{QB} pin.

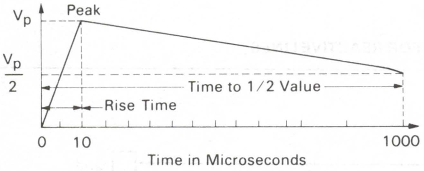
The loop resistances which the SLIC recognizes as on-hook and off-hook are determined by R_H.

$$R_L\,(\text{On-Hook}) \geqslant 0.17\,R_H - (R_R + R_T) \qquad 4\text{(a)}$$

$$R_L\,(\text{Off-Hook}) \leqslant 0.011\,R_H - 0.010\,(R_R + R_T) \qquad 4\text{(b)}$$

The value of R_H can be selected from Figure 14. All loop resistances below the shaded area at the point where R_H was selected are recognized as off-hook. All loop resistances above the shaded area at the value of R_H are recognized as on-hook. The shaded area represented an undefined region where the hook status output may indicate either on-hook or off-hook due to element tolerances and comparator hysteresis.

FIGURE 15 — TRANSIENT VOLTAGE WAVE SHAPE



Transient Protection

The SLIC shown in Figure 7 will withstand positive or negative voltage transients on Tip and Ring up to 1500 V_{peak} having the waveshape shown in Figure 15. The resistors R_{PT}, R_{PR}, R_T, and R_R must be chosen to withstand such a voltage transient without arcing across or failing due to the resulting current surge. The values of R_{PT} and R_{PR} should be between 30 and 50 Ω. Tolerance of 20% is adequate. The values of R_T and R_R are determined per equation (2). The peak currents at RSI and TSI should not exceed 200 mA during these transients.

The circuit of Figure 7 will also withstand crosses to ac power lines of up to 700 V_{RMS} for 11 cycles of the 60 Hz line per REA Form 522a. The ability to withstand continuous power-line crosses is determined mainly by the power handling ability of R_{PT}, R_{PR}, R_T, and R_R. The circuit wiring to the MDA 220 diode bridge must be adequate to handle the large voltages and currents caused by transients, as well.

None of the pins on the MC3419 should be operated more positive than V_{CC} or more negative than V_{EE}. However, under transient conditions, EP and BP may go up to one volt more positive than V_{CC} and BN, EN, and V_{QB} may go up to one volt more negative than V_{EE} without permanent damage to the MC3419. When a capacitor is used on the V_{QB} pin in conjunction with R_{QB}, a 1N4001 or similar diode is recommended between V_{EE} and V_{QB}. The diode cathode should be connected to V_{QB}. For single short transients of less than one millisecond, EP and BP may exceed V_{CC} and EN and BN may exceed V_{EE} by up to 30 V.

Transmission Characteristics

The ac termination impedance R_o of the SLIC is determined by R_T, R_R, and the ratio of R_{TX2} to R_{TX1}.

$$R_o = \frac{R_T + R_R + 1200}{1 + 97K_5} \qquad (5)$$

$$K_5 = \frac{R_{TX2}}{R_{TX2} + R_{TX1}} \qquad (6)$$

The required value of K_5 is derived from equation (5) after choosing R_o.

$$K_5 = \frac{1}{97}\left[\frac{R_T + R_R + 1200}{R_o} - 1\right] \qquad (7)$$

The value of R_{TX1} must be selected first to assure that the internal current mirrors in the MC3419 do not saturate at the minimum voltage provided at V_{QB}. The value of R_{TX1} is determined by:

$$R_{TX1} = \frac{(R_R + R_T + 1200)\,(|V_{QB}|\ \text{min} - |V_{AG}|\ \text{max} - 6.5)}{|V_{QB}|\ \text{min} - 5.4} \qquad (8)$$

If current limiting or constant current-feed is used where the minimum value of V_{QB} may not be known, R_{TX1} is found by:

$$R_{TX1} = \frac{0.01\,I_{L(max)}\,(R_R + R_T + 600) - |V_{AG}|\,(max) - 3.9}{0.01\,I_{L(max)}} \qquad (9)$$

The value of R_{TX2} may be derived from equation (6).

$$R_{TX2} = \frac{K_5 R_{TX1}}{1 - K_5} \qquad (10)$$

Transhybrid reception gain (G_{RX}) from V_{RX} to Tip and Ring is given by:

$$G_{RX} = \frac{95\,R_L\,R_o}{(R_L + R_o)\,R_{RX}} \qquad (11)$$

The value of R_{RX} may be calculated to provide the desired G_{RX} for a given R_o and R_L.

$$R_{RX} = \frac{95\,R_L\,R_o}{(R_L + R_o)\,G_{RX}} \qquad (12)$$

Transhybrid transmission gain (G_{TX}) from Tip and Ring to V_{TX} is given by:

$$G_{TX} = \frac{1.02\,R_{VTX}\,(1 - K_5)}{R_R + R_T + 1200} \qquad (13)$$

The value of R_{VTX} may be calculated to provide the desired G_{TX}.

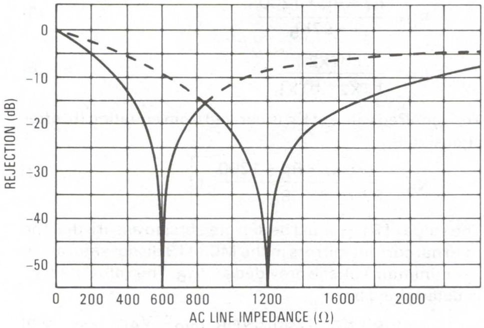
$$R_{VTX} = \frac{(R_R + R_T + 1200)\,G_{TX}}{1.02\,(1 - K_5)} \qquad (14)$$

Transhybrid rejection is achieved with the SLIC by taking advantage of the 180° phase reversal of the current at the TX pin with respect to the V_{RX} input. A balance resistor, R_B, is placed between the V_{RX} input and the virtual ground point between C_{TX} and R_{TX2}. The value of this resistor is selected to exactly cancel out the return current from the TX pin and is determined by:

$$R_B = \frac{R_{RX}(1 + 97K_5)(R_o + R_L)}{97(1-K_5)(R_L)} \qquad (15)$$

Maximum rejection will only occur at one value of R_L across Tip and Ring, as shown in Figure 16, for a given value of R_B. Figure 16 shows that more than one value of R_B may be required to provide adequate rejection over wide ranges of loop resistance.

FIGURE 16 — TRANSHYBRID REJECTION



Maximum rejection on a line that is reactive can be obtained with the circuit shown in Figure 17. This will balance any capacitive load on the line, where

$$R_{B1} = \frac{R_{RX}(R_R + R_T + 1200)}{97\,R_L\,(1-K_5)} \qquad (16)$$

$$R_{B2} = \frac{R_{RX}(R_R + R_T + 1200)}{97\,R_o\,(1-K_5)} \qquad (17)$$

$$C_B = \frac{R_L\,C_L}{R_{B2}} \qquad (18)$$

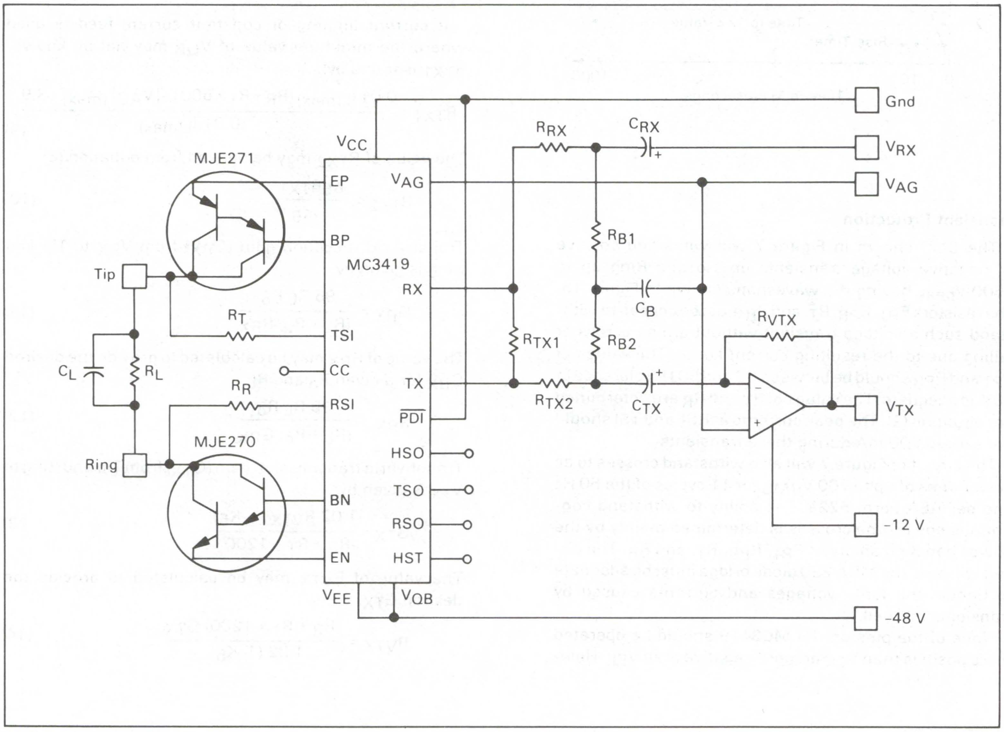
Signaling and Supervision

The $\overline{PDI}$ function shuts off all power to the subscriber with the exception of the small current provided by R_R and R_T. The power-down state occurs when a logic low-level, any voltage more negative than V_{CC} -4.0 V but not exceeding -20 V, is applied to the $\overline{PDI}$ pin.

The $\overline{PDI}$ pin is designed to be TTL compatible if the logic power supplies are 0 V and -5.0 V. It is also compatible with CMOS powered from 0 V and -12 V supplies, otherwise a level-shifter is required. If the power-down feature is not desired, this pin can be tied to V_{CC}.

Hook status is indicated by the presence or absence of current at the Hook Status Output (HSO). On-hook status is indicated by no current output at HSO. When an off-hook condition is detected by the MC3419, the HSO pin sources a dc current of at least 200 µA. A resistor can be used to translate the current into a voltage for further

FIGURE 17 — BALANCE NETWORK FOR REACTIVE LINES



processing by the digital logic. This pin also passes dial pulse information. If the $\overline{PDI}$ pin is at a logic low level, HSO is inactive.

Figures 18 (a), 18 (b), and 18 (c) show suggestions for interfacing with various digital logic levels.

The Tip Sense Output (TSO) and the Ring Sense Output (RSO) both source current that is proportional to the current that flows into and out of their respective inputs - the Tip Sense Input (TSI) and Ring Sense Input (RSI). The output currents are 1/6 that of the input currents. These outputs may be used as full time monitors of the line condition since they remain active even if the MC3419 is in the power-down state. Figure 19 shows how these outputs can be used for the ring-trip function and ring-fault indicator.

Ringing is the last function to describe on Figure 19. There are several ways of inserting the ringing signals on a line, any one of which the SLIC can be adapted to. Figure 19 shows one method.

When the ringing relay is enabled, the ring side of the SLIC is disconnected. The tip side of the line is connected to a grounded resistor (R_{G1}) to provide a complete signal path for the ring generator signal. While the phone is on-hook, the ringing signal is capacitively coupled to the tip line through the high impedance of the bell ringer and a capacitor in the phone. The dc currents are low and therefore the dc voltage drop across R_{G1} is low. When the subscriber goes off-hook, the impedance of the phone drops to a few hundred Ω of dc resistance and R_{G1} gets a large dc current along with a large ac current. The sensing resistor (R_T) will sense this change and the TSO output of the MC3419 will also reflect this change by an increased voltage drop on the R_{TS} resistor. The capacitor (C_{TS}) will filter the ac component of the signal. A comparator can now be used to determine the hook status and disable the ring relay.

Design Example

This example will illustrate the design procedure for a SLIC to meet the following specifications:

$V_{EE} = -48\ V \pm 6.0\ V$
$V_{AG} = -6.0\ V \pm 1.0\ V$
400 Ω resistive dc feed
Current limiting at 60 mA
Maximum loop resistance of 2500 Ω
900 Ω ac termination resistance
Transmit gain of 0 dB
Receive gain of 0 dB
Balanced for 600 Ω line resistance

The V_{QB} supply will be derived from the −48 V V_{EE} supply through a 1N5305 current regulator diode to provide loop current limiting at 60 mA. The voltage drop across the 1N5305 is less than 2.0 V until it reaches regulation and may be ignored in the calculation of R_T and R_R. C_{QB} is 10 μF at 60 V. From equation (2).

$$R_T = R_R = \frac{49\ (48-4)\ 400}{48} - 600$$
$$= 17367\ \Omega$$

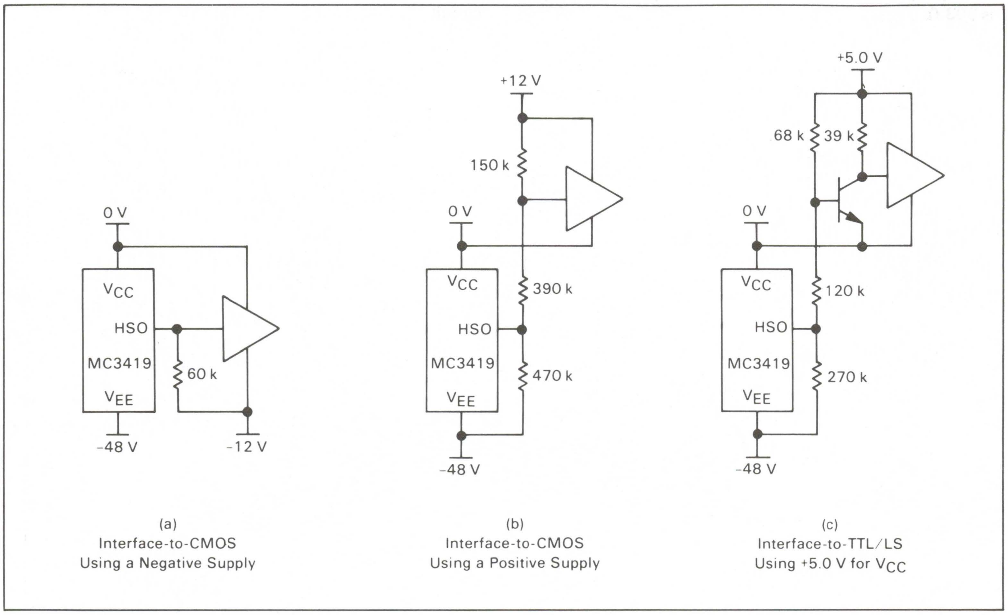
The closest standard value with ±1.0% tolerance is 17.4 kΩ. 17.4 kΩ will be used in all the rest of the equations.

The protection resistors (R_{PR} and R_{PT}) should be 30 Ω to 50 Ω. For this example we will use 40 Ω ±20%. C_T and C_R are stabilization capacitors whose values, including line capacity, should be a minimum of 2000 pF.

R_C and C_C are determined by $(R_T + 600)\ C_T = R_C\ C_C$. 18 kΩ ±5% and 2000 pF will be used for R_C and C_C.

The value of R_H is determined from Figure 14. To guarantee off-hook detection at the maximum loop resistance of 2500 Ω, R_H can be 261 kΩ ±1%, which is a standard value. A 270 kΩ ±5% resistor can be used if the on-hook resistance of the loop is specified larger than 14 kΩ.

FIGURE 18 — INTERFACE-TO-DIGITAL LOGIC



(a)
Interface-to-CMOS
Using a Negative Supply

(b)
Interface-to-CMOS
Using a Positive Supply

(c)
Interface-to-TTL/LS
Using +5.0 V for V_{CC}

To obtain the desired 900 Ω ac termination resistance (R_o), K_5 is first calculated using equation (7).

$$K_5 = \frac{1}{97}\left[\frac{17400 + 17400 + 1200}{900} - 1\right]$$

$$= 0.402$$

The value of R_{TX1} is calculated from equation (9) since V_{QB} is supplied from a current regulator diode.

$$R_{TX1} = \frac{(0.01)(0.06)(17400 + 17400 + 600) - 7 - 3.9}{(0.01)(0.06)}$$

$$= 17233\ \Omega$$

17233 Ω is the largest value of R_{TX1} that can be used. A 16.9 kΩ ±1% resistor is the standard value selected. From equation (10), R_{TX2} is now calculated.

$$R_{TX2} = \frac{(0.402)(16900)}{(1-0.402)}$$

$$= 11361\ \Omega$$

A 11.3 kΩ ±1% resistor is selected. When selecting R_{TX2}, select the nearest standard value lower than the calculated value. This is because C_{TX} adds a small impedance to the value of R_{TX2} and the virtual ground node (negative input to the current to voltage converter) will also add a slight amount of impedance to R_{TX2}. The impedance of the virtual ground point is

$$Z_{in} = \frac{R_{VTX}}{1 + A}$$

where A is the open loop gain of the op amp. At 1.0 kHz, Z_{in} will probably range from 50 Ω to 100 Ω. The C_{TX} capacitor, 1.0 μF (50 V) adds a reactance of 160 Ω to the value of R_{TX2} so the total impedance is:

$$\sqrt{(11300 + 75)^2 + (160)^2} = 11376\ \Omega$$

With the nominal values selected for R_{TX1}, R_{TX2}, C_{TX} and Z_{in}, K_5 nominal value is 0.4007 and R_o nominal value is 903 Ω.

Transhybrid reception gain (G_{RX}) is set to 0 dB (voltage gain of one) by calculating R_{RX} using equation (12). A nominal line resistance (R_L) of 900 Ω will be assumed.

$$R_{RX} = \frac{(95)(900)(903)}{(900 + 903)(1)}$$

$$= 42821\ \Omega$$

A 43.2 kΩ ±1% resistor should be used for R_{RX}. Use a 1.0 μF 20 V capacitor for C_{RX}.

Transhybrid transmission gain (G_{TX}) is set for unity gain by calculating R_{VTX}, using equation (13).

$$R_{VTX} = \frac{(17400 + 17400 + 1200)(1)}{(1-0.4007)}$$

$$= 60070\ \Omega$$

A 60.4 kΩ ±1% resistor should be used for R_{VTX}.

The balance resistor (R_B) is selected to maximize transhybrid rejection with R_L of 600 Ω using equation (15).

$$R_B = \frac{43200\,[1 + 97\,(0.4007)]\,(903 + 600)}{97\,(1-0.4007)\,(600)}$$

$$= 74216\ \Omega$$

A 75 kΩ ±1% resistor would be selected.

The digital Hook Status Output resistor (R_{HS}) is determined from a consideration of the type of logic with which the output must interface and the power supply voltages of that logic. Assuming CMOS at V_{DD} = 0 V and V_{SS} = 12 V, then

$$R_{HS} = \frac{V_{SS}}{I_{HS}}$$

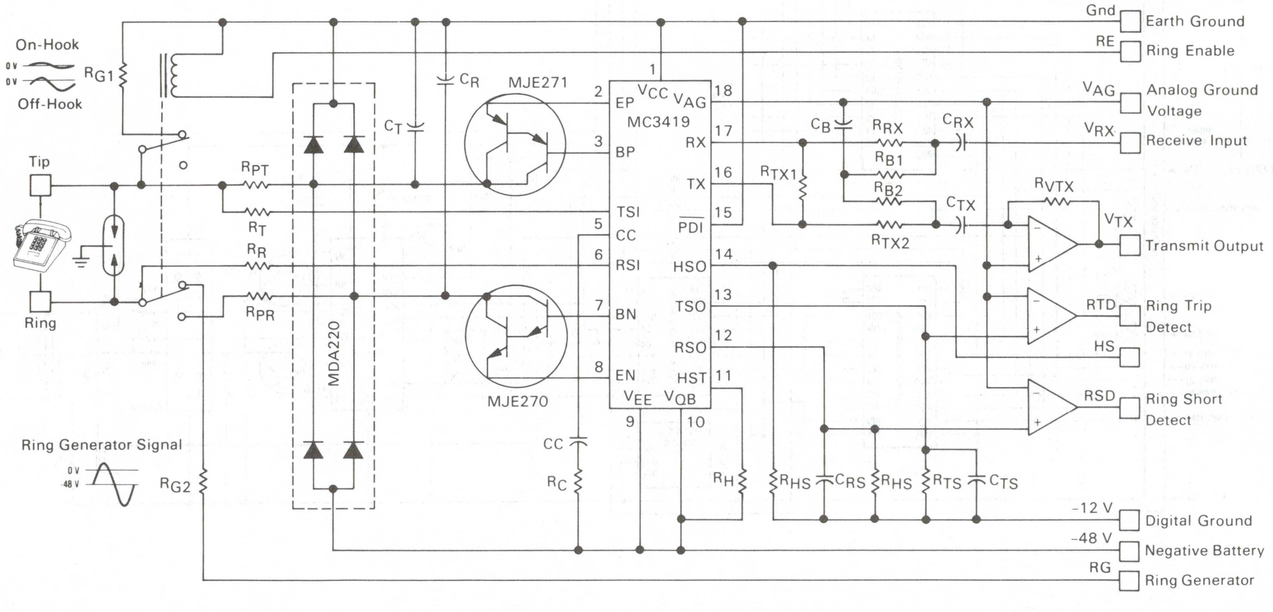
$$= \frac{12\ V}{200\ \mu A}$$

$$= 60\ k\Omega$$

A 62 kΩ ±5% resistor is suitable.

The complete SLIC design is shown in Figure 20, along with the codec, filter, time-slot assigner/channel controller, and reference voltage needed for a complete line circuit.

FIGURE 19 — RING INSERTION


On-Hook
0 V
0 V
Off-Hook
RG1
Tip
Ring
RPT
RT
RR
RPR
CR
CT
MJE271
MJE270
MDA220
2
3
5
6
7
8
1
9
10
EP
BP
TSI
CC
RSI
BN
EN
VCC
VAG
MC3419
RX
TX
PDI
HSO
TSO
RSO
HST
VEE
VQB
18
17
16
15
14
13
12
11
CB
RRX
CRX
RB1
RB2
RTX1
RTX2
CTX
RVTX
VTX
CC
RC
RH
RHS
CRS
RHS
RTS
CTS
Ring Generator Signal
0 V
-48 V
RG2
Gnd
Earth Ground
RE
Ring Enable
VAG
Analog Ground Voltage
VRX
Receive Input
Transmit Output
RTD
Ring Trip Detect
HS
RSD
Ring Short Detect
-12 V
Digital Ground
-48 V
Negative Battery
RG
Ring Generator

Note: Ring Relay is shown in energized position

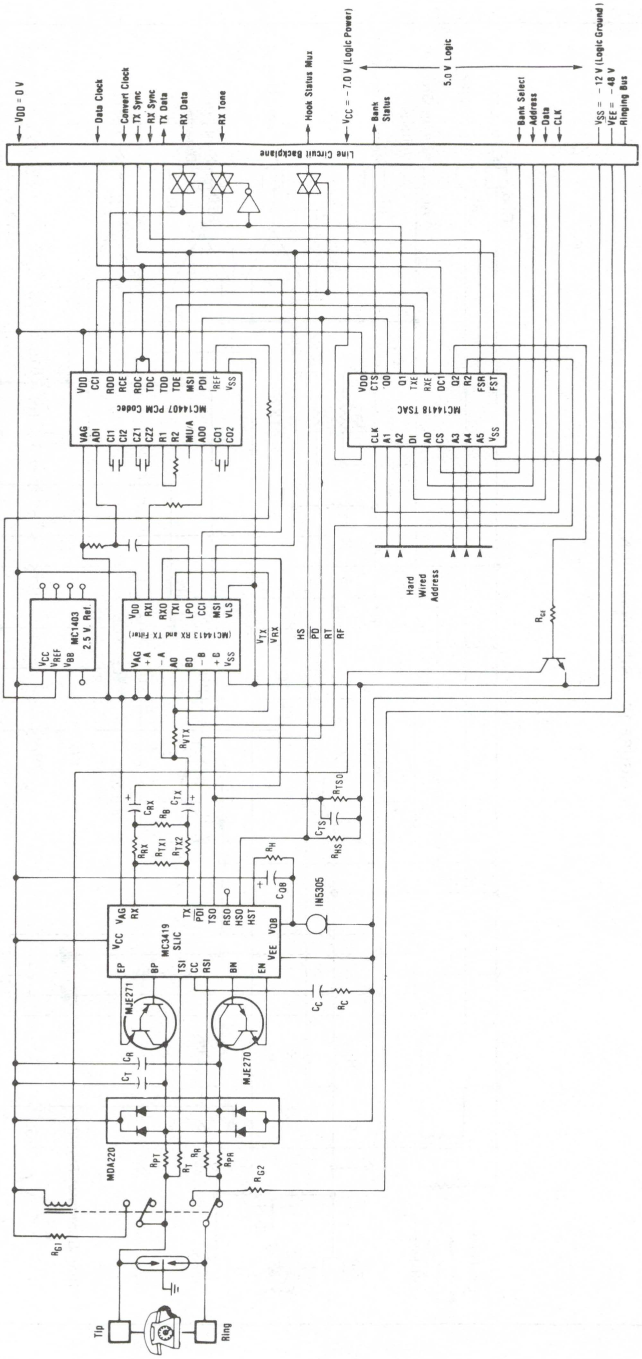

VDD = 0 V
Data Clock
Convert Clock
TX Sync
RX Sync
TX Data
RX Data
RX Tone
Hook Status Mux
VCC = −7.0 V (Logic Power)
Bank Status
5.0 V Logic
Bank Select
Address
Data
CLK
VSS = −12 V (Logic Ground)
VEE = −48 V
Ringing Bus
Line Circuit Backplane
MC14407 PCM Codec
VDD CCI RDD RCE RDC TDC TDD TDE MSI PDI IREF VSS
VAG ADI CI1 CI2 CZ1 CZ2 R1 R2 MU/A AD0 CO1 CO2
MC14418 TSAC
VDD CTS Q0 Q1 TXE RXE DC1 Q2 R2 FSR FST
CLK A1 A2 DI AD CS A3 A4 A5 VSS
Hard Wired Address
MC1403 2.5 V Ref
VCC VREF VBB
MC14413 RX and TX Filter
VDD RXI RXO TXI LPO CCI MSI VLS
VAG +A −A A0 B0 −B +B VSS
VTX
VRX
HS
PD
RT
RF
RGE
RVTX
RTSO
CTS
RHS
CRX
RB
CTX
RRX
RTX1
RTX2
RH
COB
1N5305
MC3419 SLIC
VCC VAG RX TX PDI TSO RSO HSO HST VQB
EP BP TSI CC RSI BN EN VEE
CC
RC
MJE271
MJE270
CT
CR
MDA220
RPT
RT
RR
RPR
RG2
RG1
Tip
Ring

FIGURE 20 — LINE CIRCUIT USING SLIC, FILTER, CODEC AND TSAC

MOTOROLA

MC3419-1L
MC3419A-1L
MC3419C-1L

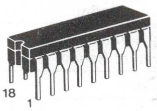
TELEPHONE LINE-FEED CIRCUIT

. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.

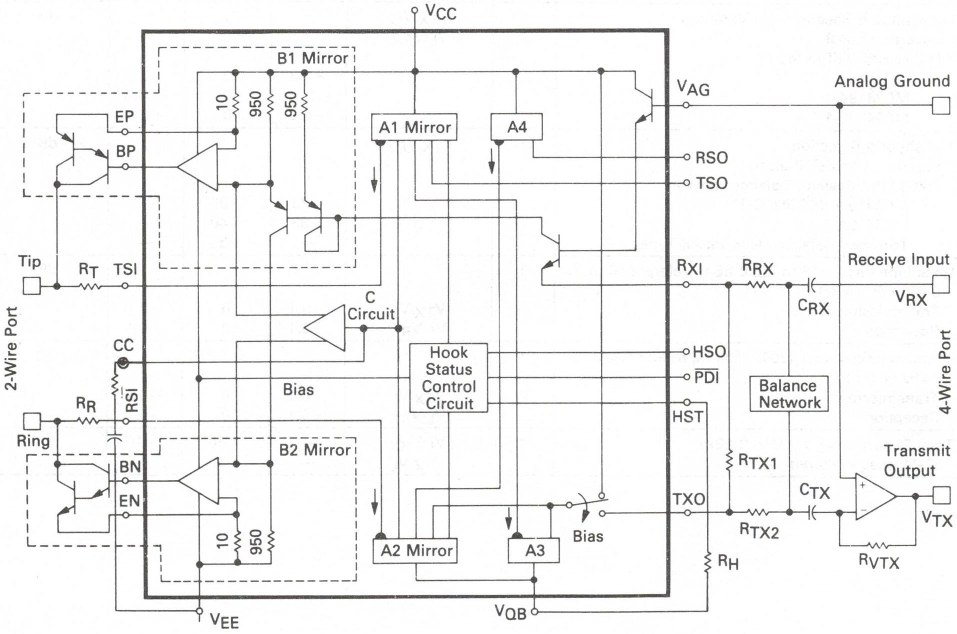
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

FUNCTIONAL BLOCK DIAGRAM


V_{CC}
B1 Mirror
EP
BP
10
950
950
A1 Mirror
A4
V_{AG}
Analog Ground
RSO
TSO
Tip
R_T
TSI
R_{XI}
R_{RX}
Receive Input
C_{RX}
V_{RX}
C Circuit
2-Wire Port
CC
Hook Status Control Circuit
HSO
$\overline{PDI}$
Bias
R_R
$\overline{RSI}$
Ring
HST
Balance Network
4-Wire Port
B2 Mirror
BN
EN
Transmit Output
R_{TX1}
TXO
C_{TX}
V_{TX}
10
950
A2 Mirror
A3
Bias
R_{TX2}
R_H
R_{VTX}
V_{EE}
V_{QB}

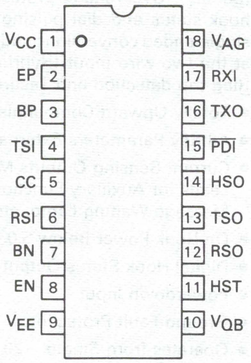
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} −1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}				dB
MC3419-1			−0.3	0	+0.3	
MC3419A-1			−0.15	0	+0.15	
MC3419C-1			−0.4	0	+0.4	
Transhybrid Rejection (Input — 1 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network	1	V_{TX}/V_{RX}				dB
MC3419-1, MC3419C-1			−23	−35	—	
MC3419A-1			−33	−40	—	
Trimmed Balance Network All Types			—	−55	—	
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1 kHz)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

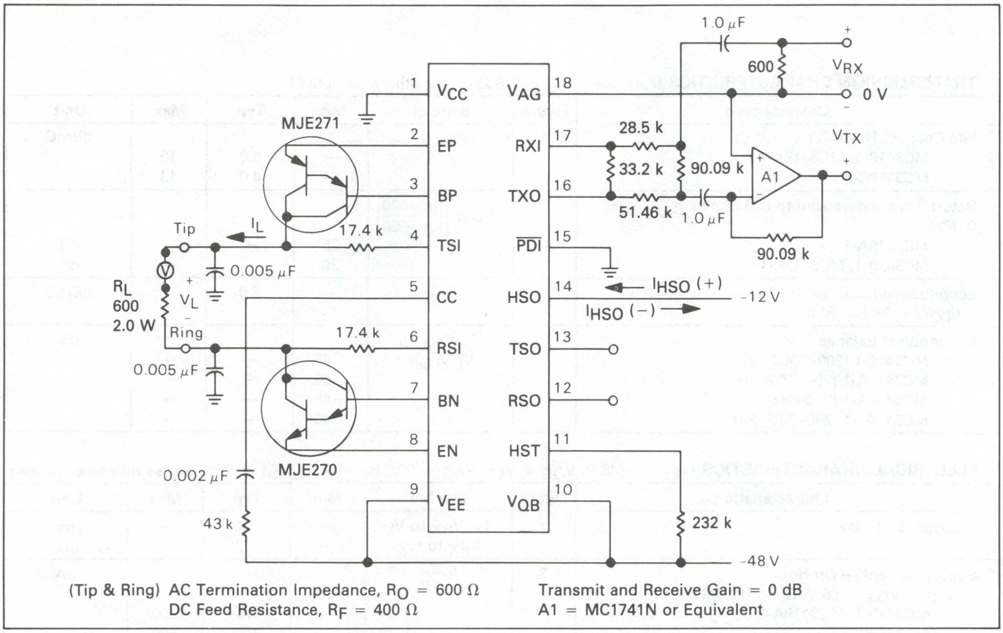
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V)	1	V_{TX}, V_L				dBrnC
MC3419-1, MC3419A-1			—	3.0	10	
MC3419C-1			—	4.0	13	
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm	1	$20\ \text{Log}\left\lvert\frac{R_0-600}{R_0+600}\right\rvert$				
MC3419A-1			36	—	—	dB
MC3419-1, MC3419C-1			30	—	—	dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnC
Longitudinal Balance	2	V_{TX}/V_{LON}, V_L/V_{LON}				dB
MC3419-1 (200–3000 Hz)			−45	—	—	
MC3419A-1 (200–1000 Hz)			−50	—	—	
MC3419A-1 (3000 Hz)			−48	—	—	
MC3419C-1 (200–3000 Hz)			−40	—	—	

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ)	3	I_{VCC}				μA
MC3419-1, MC3419A-1			—	40	200	
MC3419C-1			—	100	500	
On-Hook Power Dissipation (R_L > 100 MΩ)	3	P_D				mW
MC3419-1, MC3419A-1			—	1.0	—	
MC3419C-1			—	2.5	—	
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{ee}				dB
MC3419-1, MC3419A-1			−40	—	—	
MC3419C-1			−30	—	—	
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	—	−6.0	—	dB
Sense Current	4					mA/mA
Tip		I_{TSO}/I_{TSI}	0.15	0.17	0.19	
Ring		I_{RSO}/I_{RSI}	0.15	0.17	0.19	
Fault Currents	1					mA
Tip to V_{CC}		I_{Tip}	—	0	—	
Ring to V_{CC}		I_{Ring}	—	2.5	—	
Tip to Ring		I_{Loop}	—	120	—	
Tip and Ring to V_{CC}		I_{Tip} and I_{Ring}	—	2.5	—	
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— −1.2 —	−1.0 — —	−10 — −4.0	μA Vdc Vdc
Hook Status Output Current	1	I_{HSO}				
(R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc)			+1.0	+3.0	—	mA
V_{HSO} = −0.4 Vdc)			−0.4	−1.5	—	mA
(R_L > 10 kΩ, V_{HSO} = +12 Vdc)			—	0	+50	μA
V_{HSO} = −12 Vdc)			—	0	−2.0	μA

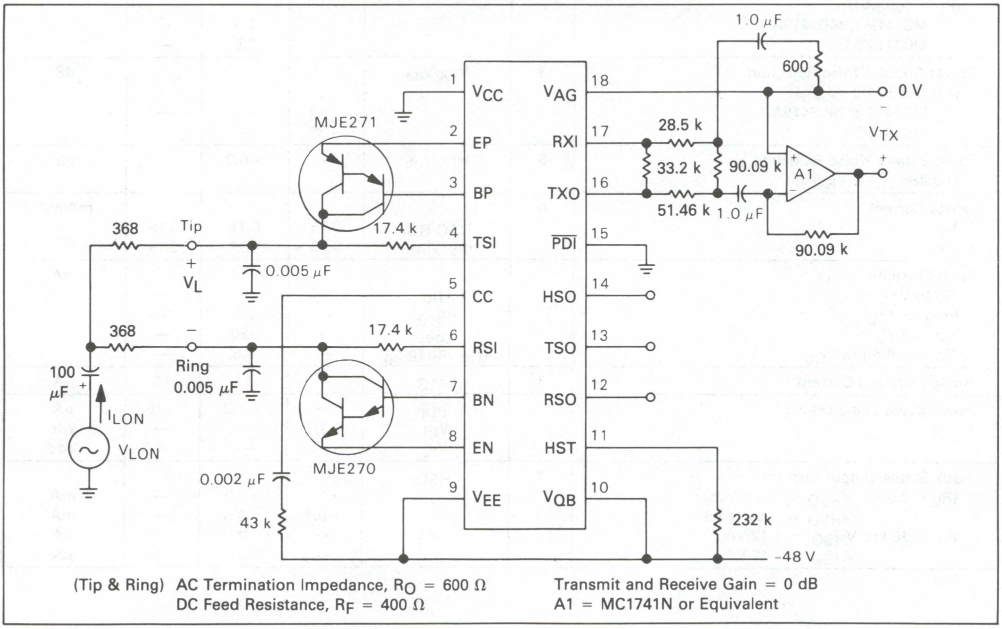
FIGURE 1 — AC TEST CIRCUIT


1.0 µF
+
600
VRX
0 V
−
VTX
+
28.5 k
33.2 k
90.09 k
A1
51.46 k
1.0 µF
90.09 k
1 VCC
2 EP
3 BP
4 TSI
5 CC
6 RSI
7 BN
8 EN
9 VEE
18 VAG
17 RXI
16 TXO
15 PDI
14 HSO
13 TSO
12 RSO
11 HST
10 VQB
MJE271
Tip
IL
17.4 k
V
0.005 µF
RL
600
2.0 W
+
VL
−
Ring
IHSO (+)
IHSO (−)
−12 V
17.4 k
0.005 µF
MJE270
0.002 µF
43 k
232 k
−48 V

(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

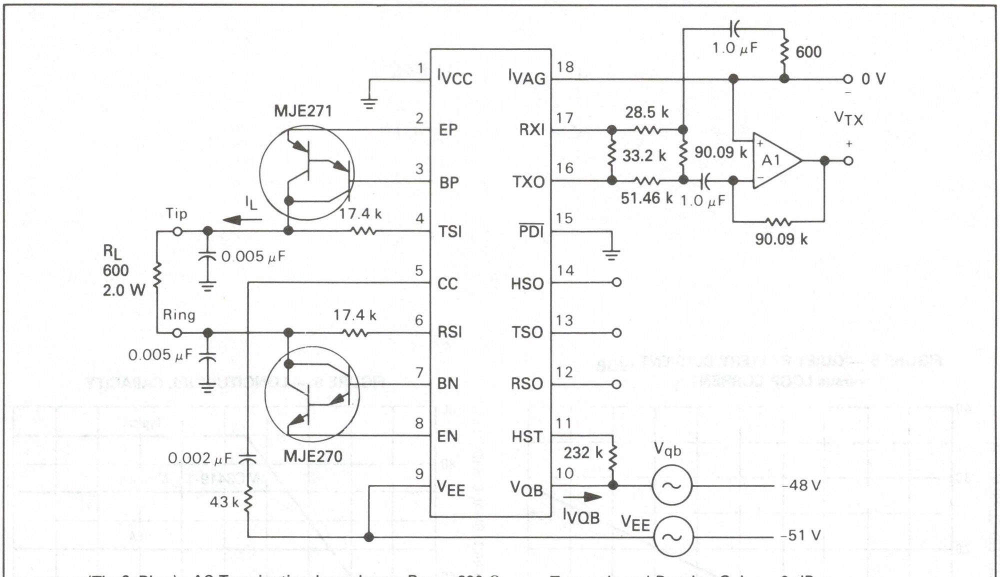
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT


1.0 µF
600
0 V
−
VTX
+
28.5 k
33.2 k
90.09 k
A1
51.46 k
1.0 µF
90.09 k
1 VCC
2 EP
3 BP
4 TSI
5 CC
6 RSI
7 BN
8 EN
9 VEE
18 VAG
17 RXI
16 TXO
15 PDI
14 HSO
13 TSO
12 RSO
11 HST
10 VQB
MJE271
368
Tip
+
VL
17.4 k
0.005 µF
368
−
Ring
0.005 µF
17.4 k
100 µF
+
ILON
VLON
MJE270
0.002 µF
43 k
232 k
−48 V

(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT


1
IVCC
2
EP
3
BP
4
TSI
5
CC
6
RSI
7
BN
8
EN
9
VEE
18
IVAG
17
RXI
16
TXO
15
PDI
14
HSO
13
TSO
12
RSO
11
HST
10
VQB
MJE271
MJE270
Tip
Ring
IL
17.4 k
17.4 k
RL
600
2.0 W
0.005 μF
0.005 μF
0.002 μF
43 k
1.0 μF
600
0 V
28.5 k
33.2 k
90.09 k
51.46 k
1.0 μF
90.09 k
A1
VTX
232 k
Vqb
-48 V
IVQB
VEE
-51 V

(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

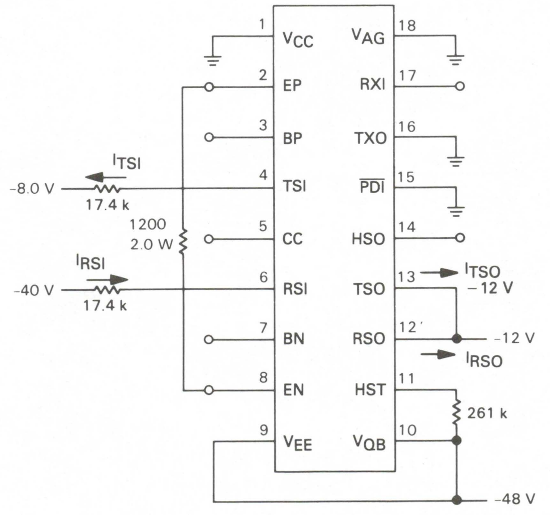

1
VCC
2
EP
3
BP
4
TSI
5
CC
6
RSI
7
BN
8
EN
9
VEE
18
VAG
17
RXI
16
TXO
15
PDI
14
HSO
13
TSO
12
RSO
11
HST
10
VQB
ITSI
-8.0 V
17.4 k
1200
2.0 W
IRSI
-40 V
17.4 k
ITSO
-12 V
-12 V
IRSO
261 k
-48 V

FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

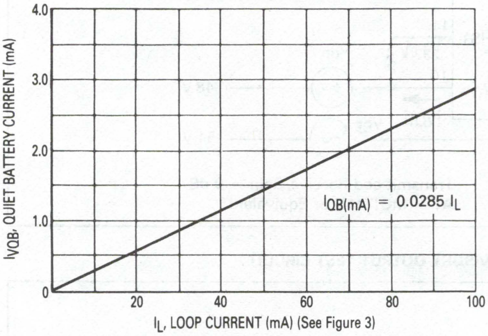
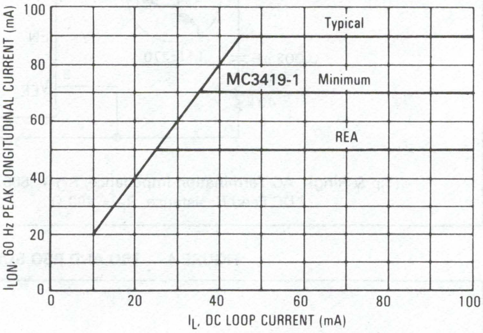


FIGURE 6 — LONGITUDINAL CAPACITY



PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{HSO}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually $R_L < 2.5$ kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually $R_L > 10$ kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{PDI}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "O" ($V_{IL} < -4.0$ V) powers down the MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to $I_{TSI} + I_{RSI}$ by a ratio of K1 where: K1 = 1.02. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

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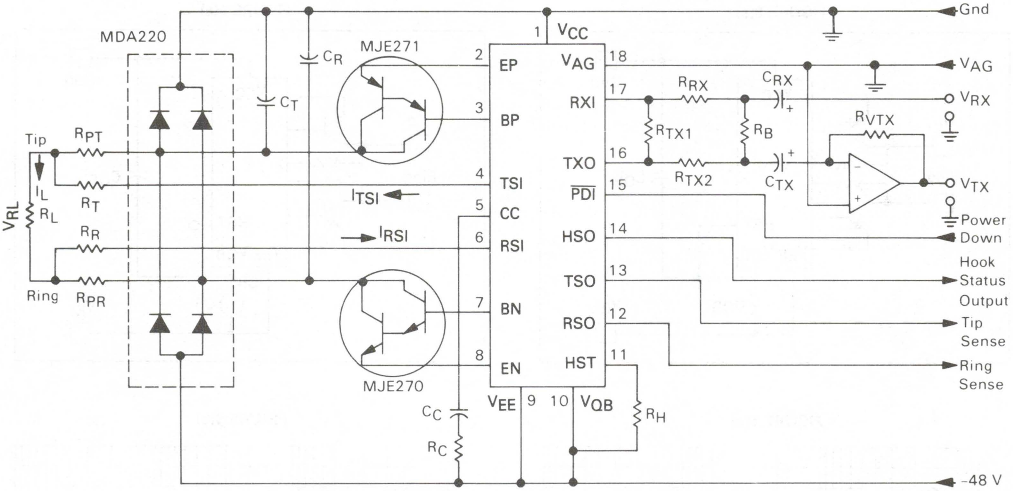
*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{\text{PDI}}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from $I_{TSI} + I_{RSI}$ to TXO only during an off-hook power-up condition. K1 = 1.02 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance $(1 + K1K2) = 1 + 1.02 \times 95 = 97.9$ is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

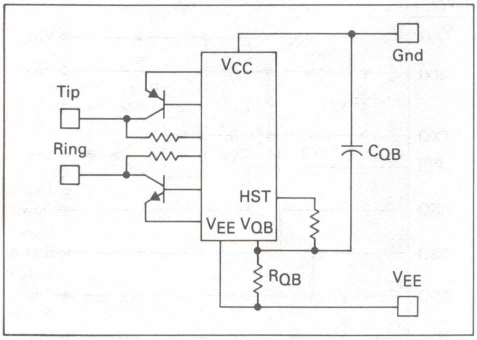


FIGURE 9(a)

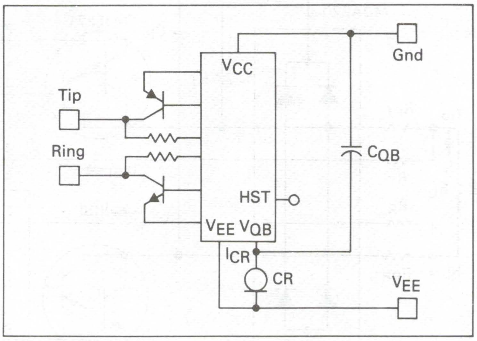


FIGURE 8(b)

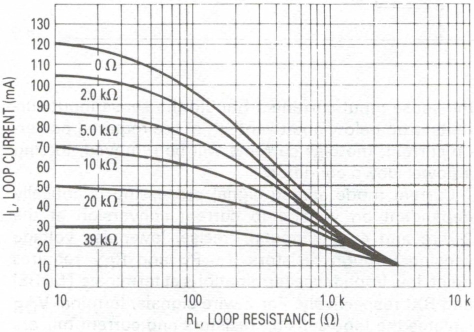
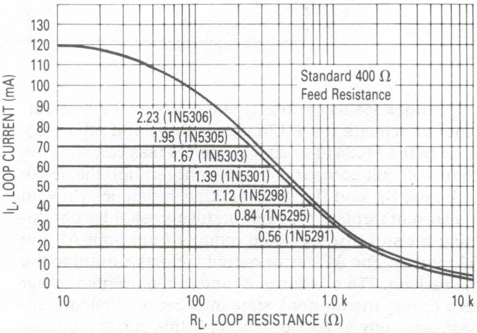


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \qquad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|(V_{QB}|\ - 4.0\ V)} - R_L \qquad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}|\ - 4.0\ V)} \qquad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}|\ - 4.0\ V)}{|V_{QB}|} - 600 \qquad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\, I_{RSI} + 0.7\, I_{TSI} \qquad (5)$$

$$I_{VQB} = 0.029\, I_L \qquad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ \text{V})} - R_L \qquad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ \text{V})} \qquad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ \text{V}) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \qquad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\ R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\ R_{QB}\ (R_R + R_T + 1200\ \Omega)} \qquad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

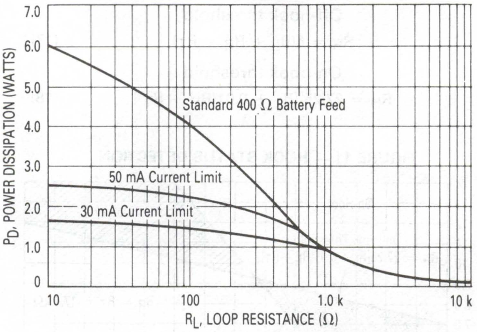
I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

$$I_L = 34.5\, I_{CRQB} \qquad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

$$R_{PT} < R_T/196 - 15 \qquad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \qquad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \qquad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L^2(R_T/98 - R_{PT} - 4) + (2.0\ \text{V})I_L \qquad (15)$$

$$P_{QR} = I_L\ [|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \qquad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or $I_L(\text{max})$ in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \qquad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \qquad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

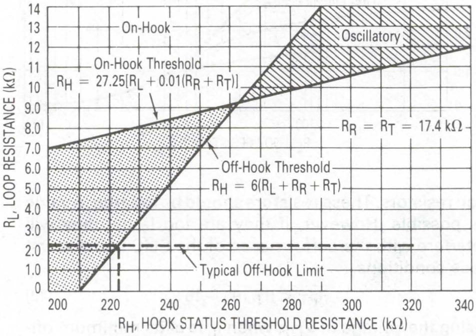


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{\text{PDI}}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \qquad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \qquad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \qquad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\ G_{TX}}{1020\ (1 - K3)} = \frac{R_{VTX}}{1000} \qquad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\ (|V_{QB}|\text{min} - |V_{AG}|\text{max} - 6.5\ \text{V})}{|V_{QB}|\text{min} - 5.4\ \text{V}} \qquad (23)$$

Where:

$$|V_{QB}|\text{min} = \frac{(R_R + R_T + 1200\ \Omega)\ (|V_{EE}|\text{min} - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\ R_{QB})} \qquad (24)$$

or if a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(\text{max})\ (R_R + R_T + 600\ \Omega) - |V_{AG}|\text{max} - 3.9\ \text{V}}{0.01\ I_L(\text{max})} \qquad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\ R_{TX1}}{1 - K3} - Z_{in} \qquad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu\text{F.} \qquad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\ (1 - K3)\ R_{VTX}}{R_R + R_T + 1200\ \Omega} \qquad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\ (1 - K3)} \qquad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\ R_L\ (R_R + R_T + 1200\ \Omega)}{R_{RX}\ [(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \qquad (30)$$

$$G_{RX} = \frac{-95\ R_L\ R_O}{R_{RX}(R_L + R_O)} \qquad (31)$$

$$R_{RX} = \frac{95\ R_L\ R_O}{G_{RX}(R_L + R_O)} \qquad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\ f\ R_{RX}R_B} \qquad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\ (R_O + R_L)}{97R_L\ (1 - K3)} \qquad (34)$$

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

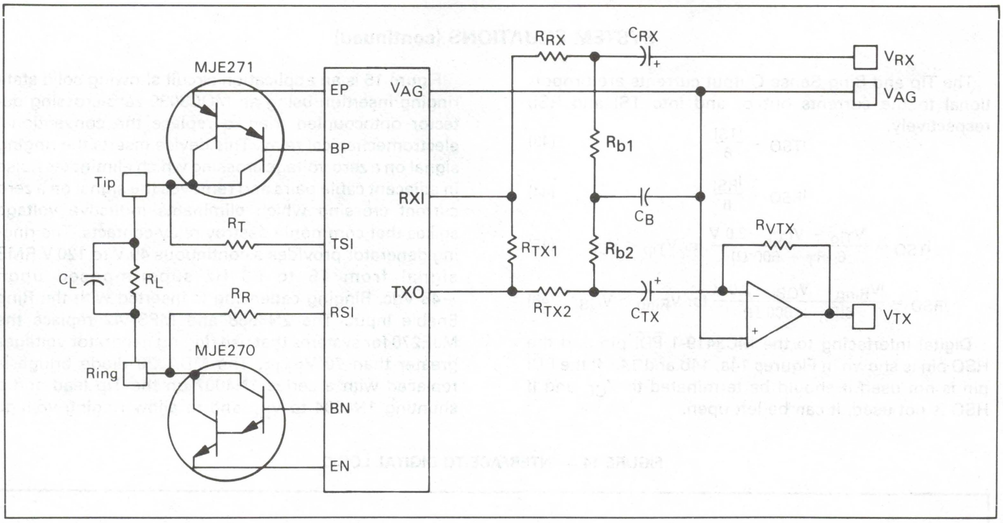
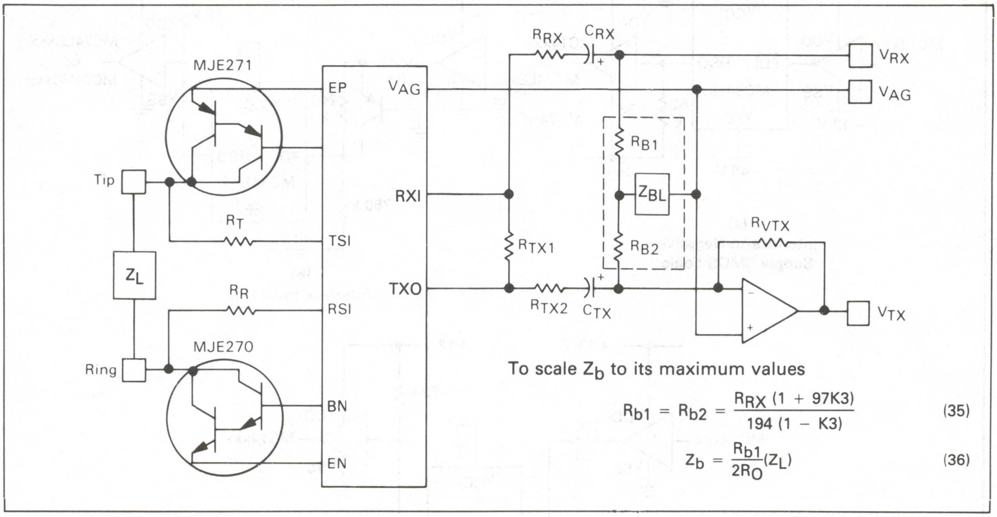

MJE271
EP
V_{AG}
BP
Tip
RXI
R_T
TSI
C_L
R_L
R_R
TXO
RSI
MJE270
Ring
BN
EN
R_{RX}
C_{RX}
V_{RX}
V_{AG}
R_{b1}
C_B
R_{VTX}
R_{TX1}
R_{b2}
R_{TX2}
C_{TX}
V_{TX}

FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES


MJE271
EP
V_{AG}
Tip
RXI
R_T
TSI
Z_L
R_R
TXO
RSI
MJE270
Ring
BN
EN
R_{RX}
C_{RX}
V_{RX}
V_{AG}
R_{B1}
Z_{BL}
R_{VTX}
R_{TX1}
R_{B2}
R_{TX2}
C_{TX}
V_{TX}

To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}\,(1 + 97K3)}{194\,(1 - K3)} \tag{35}$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \tag{36}$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L\,(1 - K3)} \tag{37}$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \tag{38}$$

$$C_b = \frac{R_L C_L}{R_{b2}} \tag{39}$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \tag{40}$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \tag{41}$$

$$Z_b = Z_L \tag{42}$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \qquad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \qquad (44)$$

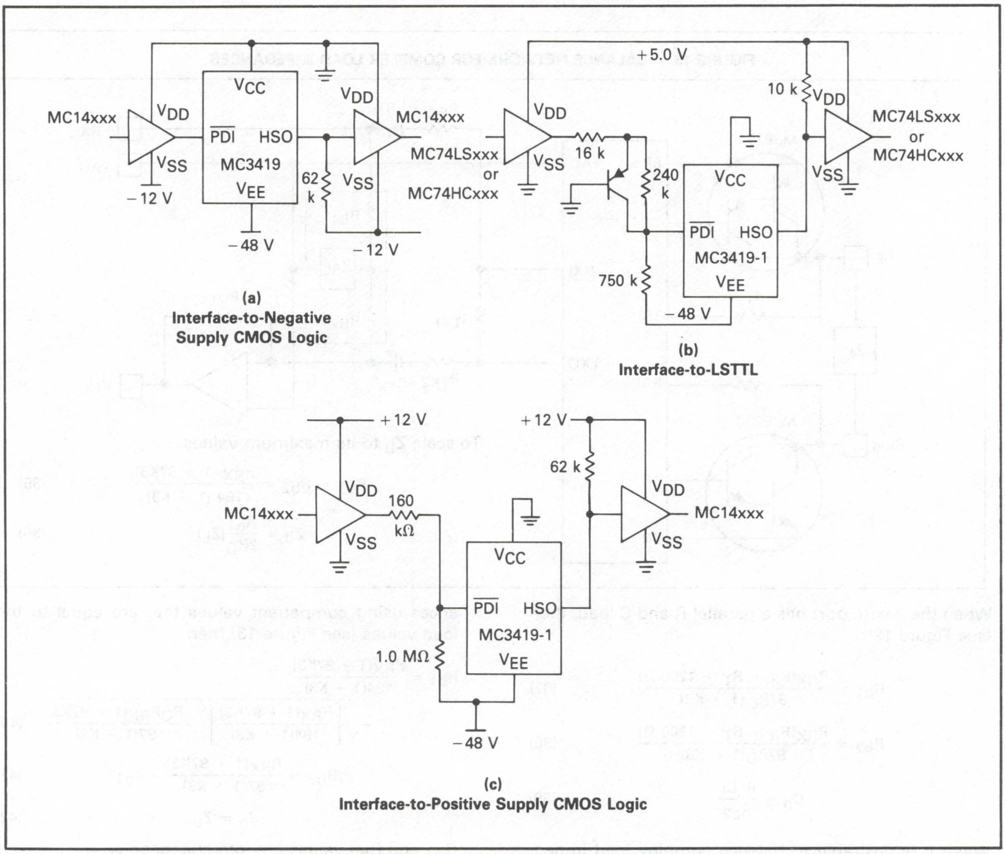
$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \qquad (45)$$

$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \qquad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC

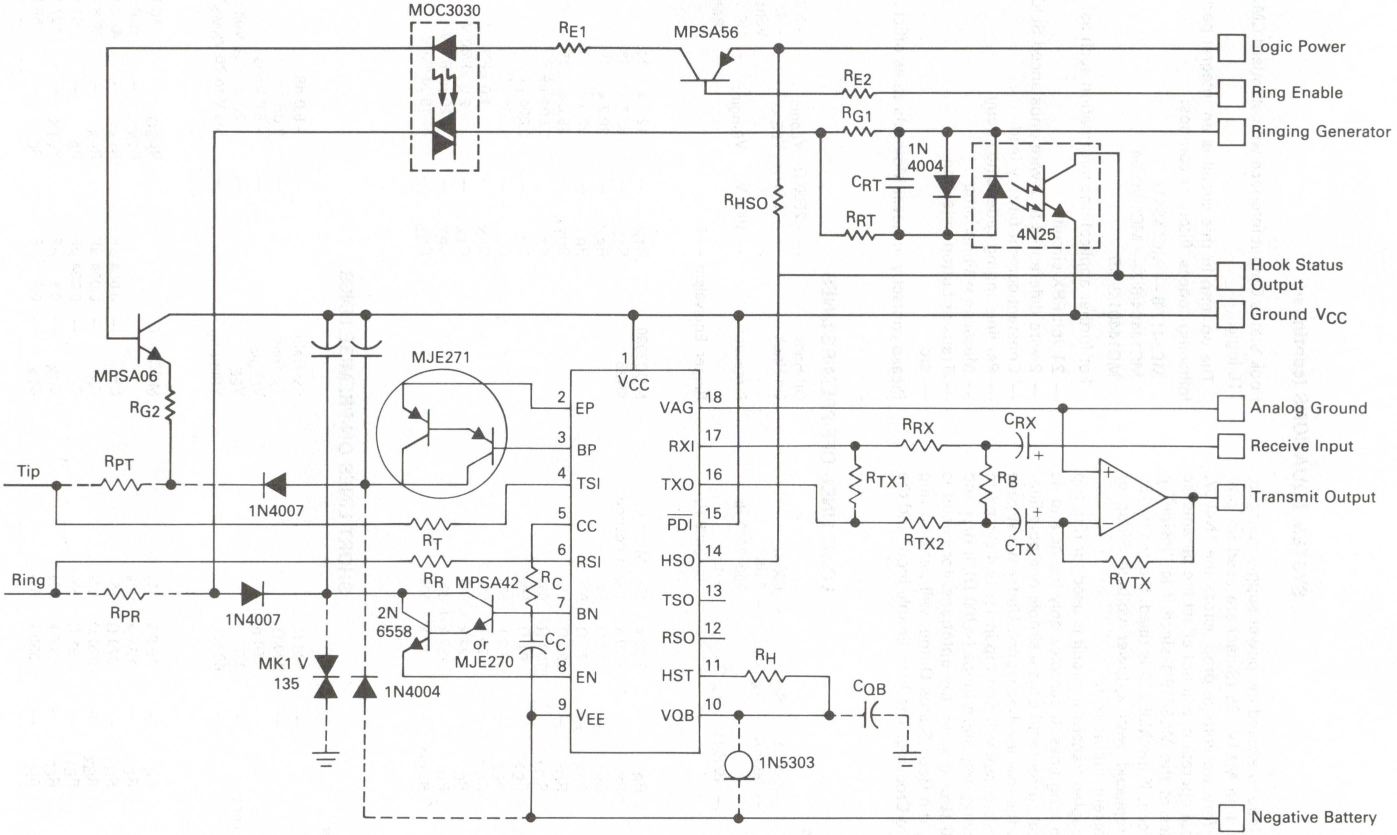

MC14xxx
VDD
VSS
−12 V
VCC
PDI
HSO
MC3419
VEE
−48 V
62 k
VDD
VSS
MC14xxx
MC74LSxxx
or
MC74HCxxx
−12 V
+5.0 V
VDD
VSS
16 k
240 k
750 k
VCC
PDI
HSO
MC3419-1
VEE
−48 V
10 k
VDD
VSS
MC74LSxxx
or
MC74HCxxx
+12 V
VDD
MC14xxx
VSS
160 kΩ
1.0 MΩ
VCC
PDI
HSO
MC3419-1
VEE
−48 V
+12 V
62 k
VDD
VSS
MC14xxx

(a)
Interface-to-Negative Supply CMOS Logic

(b)
Interface-to-LSTTL

(c)
Interface-to-Positive Supply CMOS Logic

FIGURE 15 — PBX LINE CIRCUIT


MOC3030
R_{E1}
MPSA56
Logic Power
R_{E2}
Ring Enable
R_{G1}
Ringing Generator
1N 4004
C_{RT}
R_{HSO}
R_{RT}
4N25
Hook Status Output
Ground V_{CC}
MPSA06
R_{G2}
MJE271
1
V_{CC}
2 EP
3 BP
4 TSI
5 CC
6 RSI
7 BN
8 EN
9 V_{EE}
18 VAG
17 RXI
16 TXO
15 $\overline{PDI}$
14 HSO
13 TSO
12 RSO
11 HST
10 VQB
Analog Ground
R_{RX}
C_{RX}
Receive Input
R_{TX1}
R_B
Transmit Output
R_{TX2}
C_{TX}
R_{VTX}
Tip
R_{PT}
1N4007
R_T
Ring
R_R
MPSA42
R_C
R_{PR}
1N4007
2N 6558
or MJE270
C_C
MK1 V 135
1N4004
R_H
C_{QB}
1N5303
Negative Battery

– – – – Indicates Optional Components

SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MoSorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

For further applications information such as:

- 24 volt PBX circuit
- 2-wire differential to 2-wire unbalanced SLIC
- Constant current battery feed
- Per line ringing cadencing circuit
- Message waiting lamp
- Transfer button detection
- etc.

Please contact your local Motorola sales office.

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω	Off-Hook	— <2500 Ω	V_{Logic}	— +5.0 V
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz	On-Hook	— >10 kΩ	V_{EE}	— −42 to −56 Volts
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz	Protection	— 1000 V	$V_{Ringing}$	— (40 V to 120 V_{RMS}) + V_{EE}
				Ringer Equivalent	— 5		

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched	MOC3030	R_{TX1}	—	12.1 k 1%
2N3905	R_T	—	9.09 k	1%	if desired	4N25	R_{TS2}	—	5.76 k 1%
2N6558	R_{PT}	—	47 Ω	5%			R_{RX}	—	28.7 k 1%
MPSA42	R_{PR}	—	75 Ω	5%			R_B	—	28.0 k 1%
MJE271	R_{G1}	—	620 Ω	5%			R_{VTX}	—	28.6 k 1%
1N4007	R_{G2}	—	100 Ω	5%			C_T		0.004 μF
MK1V135	R_{E1}	—	91 Ω	5%			C_R	—	0.004 μF
1N4007	R_{E2}	—	3.0 k	5%			C_C	—	0.001 μF
1N4007	R_{RT}	—	20 k	5%			C_{RX}	—	1.0 μF/20 V
1N5303	R_C	—	24 k	5%			C_{TX}	—	2.0 μF/40 V
1N4004	R_H	—	127 k	1–3%			C_{RT}	—	20 μF/5.0 V
MC3419-1	R_{HSO}	—	10 k	5%			C_{QB}	—	10 μF/60 V

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω	R_X Gain	—	−5.0 dB
R_L(max)	—	700 Ω	T_X Gain	—	0 dB
Ring Trip	—	<50 ms	V_{Logic}	—	+5.0 Volts
Ringer Equivalent	—	2.5	V_{EE}	—	−20 to −56 Volts
R_O	—	600 Ω	$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}

Parts List

MJE271	R_R	—	19.6 k	1%	MOC3030			R_{HSO}	—	10 k	5%
MJE270	R_T	—	19.6 k	1%				R_{TX1}	—	19.6 k	1%
MPSA56	R_{G1}	—	620 Ω	5%	C_T	—	0.004 μF	R_{TX2}	—	42.2 k	1%
2N3905	R_{G2}	—	620 Ω	5%	C_R	—	0.004 μF	R_{RX}	—	69.8 k	1%
1N4007	R_{E1}	—	91 Ω	5%	C_C	—	0.004 μF	R_B	—	301 k	1%
1N4007	R_{E2}	—	3.0 k	5%	C_{RX}	—	0.1 μF	R_{VTX}	—	127 k	1%
MC3419C-1	R_H	—	330 k	5%	C_{TX}	—	0.5 μF	R_C	—	56 k	5%

MOTOROLA

MC34012-1
MC34012-2
MC34012-3

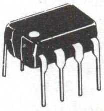
Advance Information

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

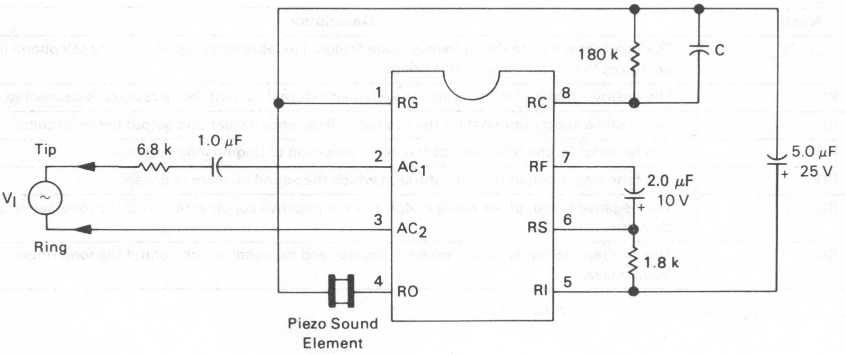
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^{2}L



PLASTIC PACKAGE CASE 626

APPLICATION CIRCUIT


180 k
C
1
RG
RC
8
Tip
6.8 k
1.0 µF
2
AC1
RF
7
5.0 µF
25 V
2.0 µF
10 V
VI
3
AC2
RS
6
Ring
1.8 k
4
RO
RI
5
Piezo Sound Element

MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies		
MC34012-1	832/1040	Hz
MC34012-2	1664/2080	
MC34012-3	416/520	
Warble Frequency	13	
Output Voltage ($V_I \geqslant 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leqslant$ 68 Hz)	150	V_{rms}
Impedance When Ringing		kΩ
$V_I = 40\ V_{rms}$, 15 Hz	20	
$V_I = 130\ V_{rms}$, 23 Hz	10	
Impedance When Not Ringing		
$V_I = 10\ V_{rms}$, 24 Hz	28	kΩ
$V_I = 2.5\ V_{rms}$, 24 Hz	>1.0	MΩ
$V_I = 10\ V_{rms}$, 5.0 Hz	55	kΩ
$V_I = 3.0\ V_{rms}$, 200–3200 Hz	>1.0	MΩ
Maximum Transient Input Voltage ($T \leqslant 2.0$ ms)	1500	V

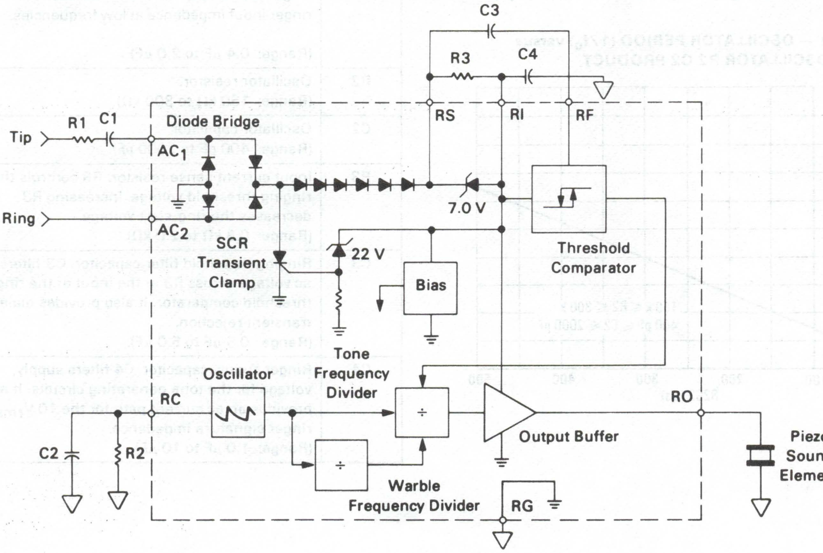
PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	−31	−34.5	−38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM


C3
R3
C4
RS
RI
RF
R1
C1
Tip
Diode Bridge
AC1
Ring
AC2
7.0 V
SCR
Transient
Clamp
22 V
Bias
Threshold
Comparator
Oscillator
RC
Tone
Frequency
Divider
÷
Output Buffer
RO
Piezo
Sound
Element
C2
R2
÷
Warble
Frequency Divider
RG

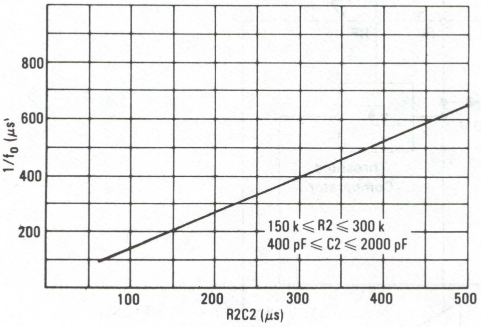
CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

The frequency of the tone ringer output signal at pin RO alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34012-1, $f_o/640$ for the MC34012-2, or $f_o/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

FIGURE 1 — OSCILLATOR PERIOD (1/f_o) versus OSCILLATOR R2 C2 PRODUCT



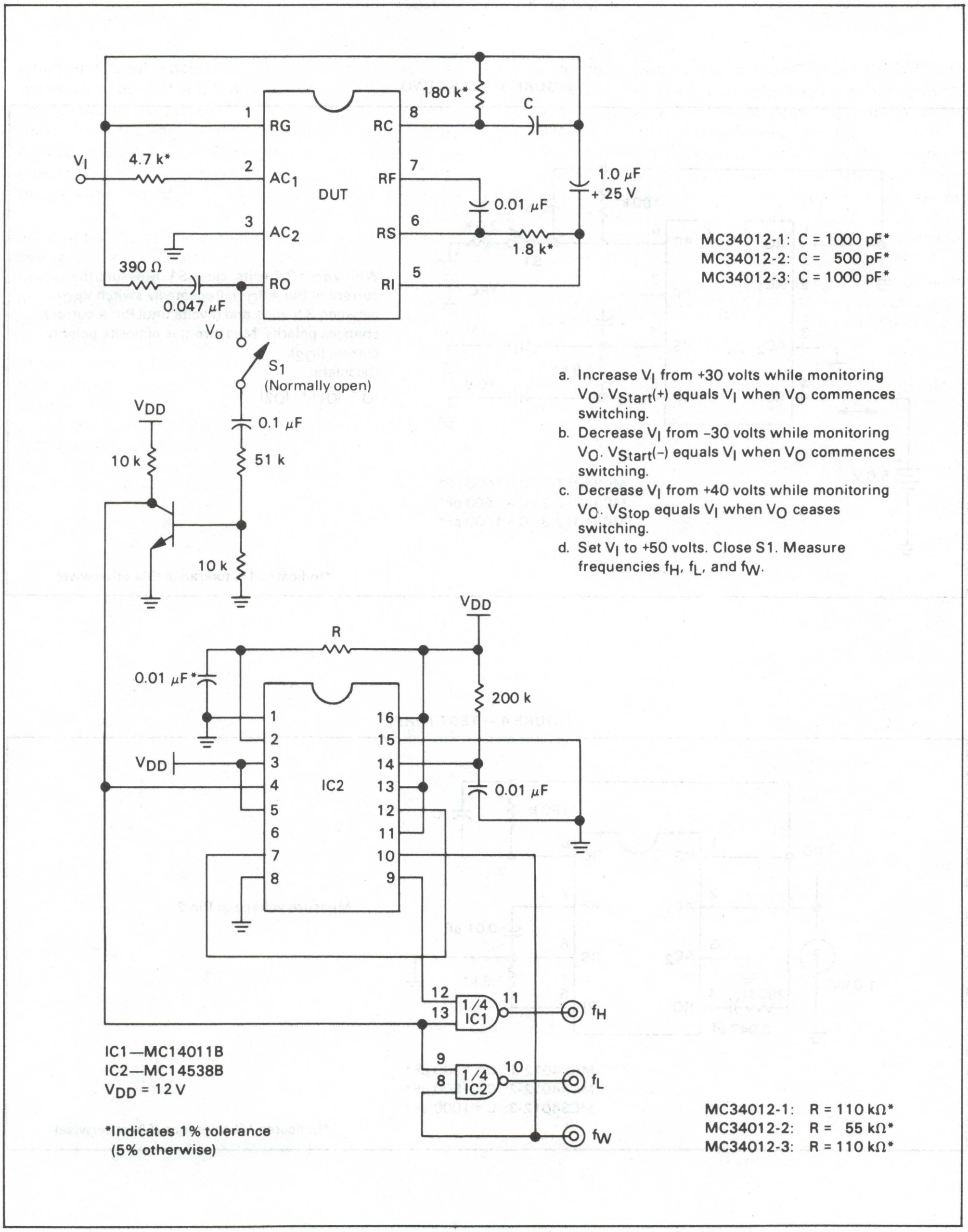
Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 µF to 2.0 µF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 µF to 5.0 µF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 µF to 10 µF).

FIGURE 2 — TEST ONE


180 k*
C
1
RG
8
RC
V_I
4.7 k*
2
AC_1
DUT
7
RF
1.0 μF
+ 25 V
0.01 μF
3
AC_2
6
RS
1.8 k*
390 Ω
RO
5
RI
0.047 μF
V_o
S_1
(Normally open)
V_{DD}
0.1 μF
10 k
51 k
10 k
V_{DD}
R
0.01 μF*
200 k
IC2
V_{DD}
0.01 μF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12
13
11
1/4 IC1
f_H
9
8
10
1/4 IC2
f_L
f_W

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

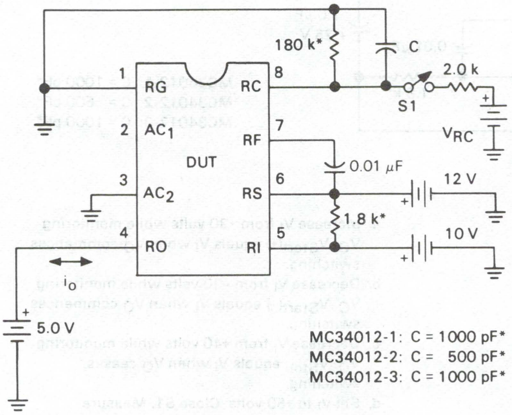
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from −30 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance
(5% otherwise)

MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 — TEST TWO

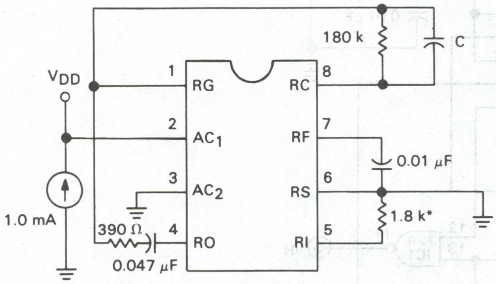

180 k*
C
1
RG
RC
8
2.0 k
S1
VRC
2
AC1
RF
7
DUT
0.01 µF
3
AC2
RS
6
12 V
1.8 k*
4
RO
RI
5
10 V
Io
5.0 V

With V_{RC} = 3.5 volts, close S1. Measure the current at Pin 4 (I_{O1}). Repeatedly switch V_{RC} between 3.5 volts and 0 volts until Pin 4 current changes polarity. Measure this opposite polarity current (I_{O2}).
Calculate:
$I_O = |I_{O1}| + |I_{O2}|$

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

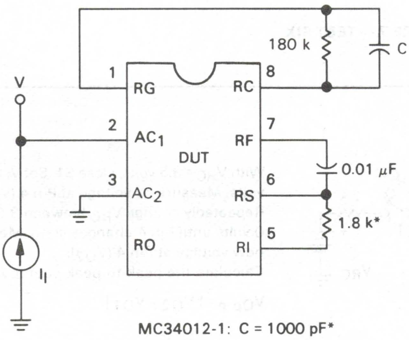

VDD
180 k
C
1
RG
RC
8
2
AC1
RF
7
0.01 µF
3
AC2
RS
6
1.0 mA
1.8 k*
390 Ω
4
RO
RI
5
0.047 µF

Measure voltage at Pin 2.

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR

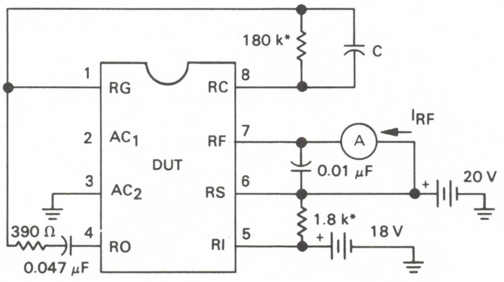

180 k
C
1
8
RG
RC
V
2
7
AC1
RF
DUT
0.01 μF
3
6
AC2
RS
1.8 k*
5
RO
RI
I_I

a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE


180 k*
C
1
RG
RC
8
I_RF
2
AC1
RF
7
A
DUT
0.01 μF
20 V
3
AC2
RS
6
1.8 k*
390 Ω
4
18 V
RO
RI
5
0.047 μF

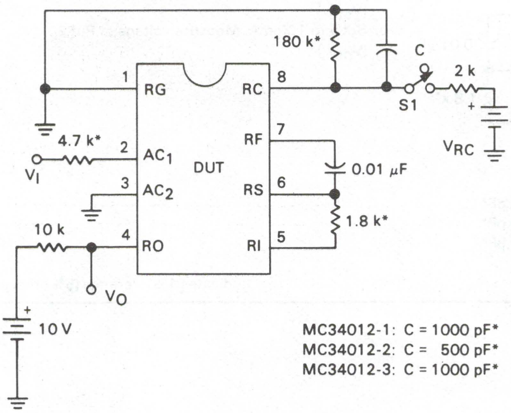
Measure current into Pin 7 (I_{RF}).
Calculate:

$R_{RF} = 2 \text{ volts} \div I_{RF}$

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX


180 k*
C
2 k
S1
+
V_RC
1
RG
RC
8
7
RF
4.7 k*
2
AC_1
V_I
DUT
3
AC_2
0.01 μF
RS
6
1.8 k*
10 k
4
RO
RI
5
V_O
+
10 V

With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}).
Calculate the peak-to-peak output voltage:

$V_{Op\text{-}p} = | V_{O2} - V_{O1} |$

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

MOTOROLA

MC34013

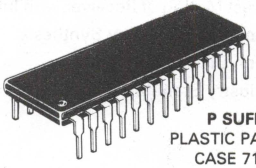
Product Preview

TELEPHONE SPEECH NETWORK AND TONE DIALER

- Linear/I^{2}L Technology Provides Low 1.4 Volt Operation in Both Speech or Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Speech Network Operational with Loop-Currents from 6.0 mA to 120 mA
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

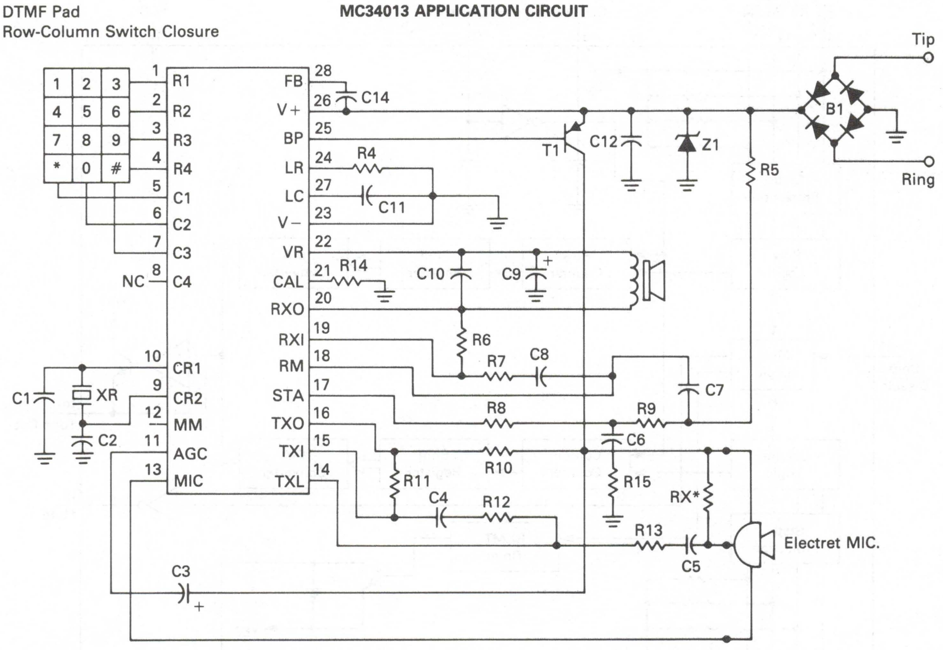
SPEECH NETWORK
AND
TONE DIALER

BIPOLAR LINEAR/I^{2}L



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

MC34013 APPLICATION CIRCUIT


DTMF Pad
Row-Column Switch Closure
1 2 3
4 5 6
7 8 9
* 0 #
1 R1
2 R2
3 R3
4 R4
5 C1
6 C2
7 C3
NC 8 C4
10 CR1
9 CR2
12 MM
11 AGC
13 MIC
C1
XR
C2
C3
28 FB
26 V+
25 BP
24 LR
27 LC
23 V−
22 VR
21 CAL
20 RXO
19 RXI
18 RM
17 STA
16 TXO
15 TXI
14 TXL
C14
R4
C11
R14
C10
C9
T1
C12
Z1
R5
B1
Tip
Ring
R6
R7
C8
C7
R8
R9
C6
R10
R11
R15
C4
R12
RX*
R13
C5
Electret MIC.

*RX used with 2-Technical mike only.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC34015

MOTOROLA

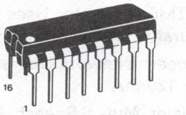
Product Preview

INTEGRATED TONE DIALER

- Low Voltage Operation
- On-Chip Filter Provides Low Distortion
- Inexpensive Ceramic Resonator Oscillator
- Direct Muting of Receiver with Internal Click Suppression Delay
- Accurate Frequency Synthesis
- Tone Disable Capability
- Industry Standard Pinout

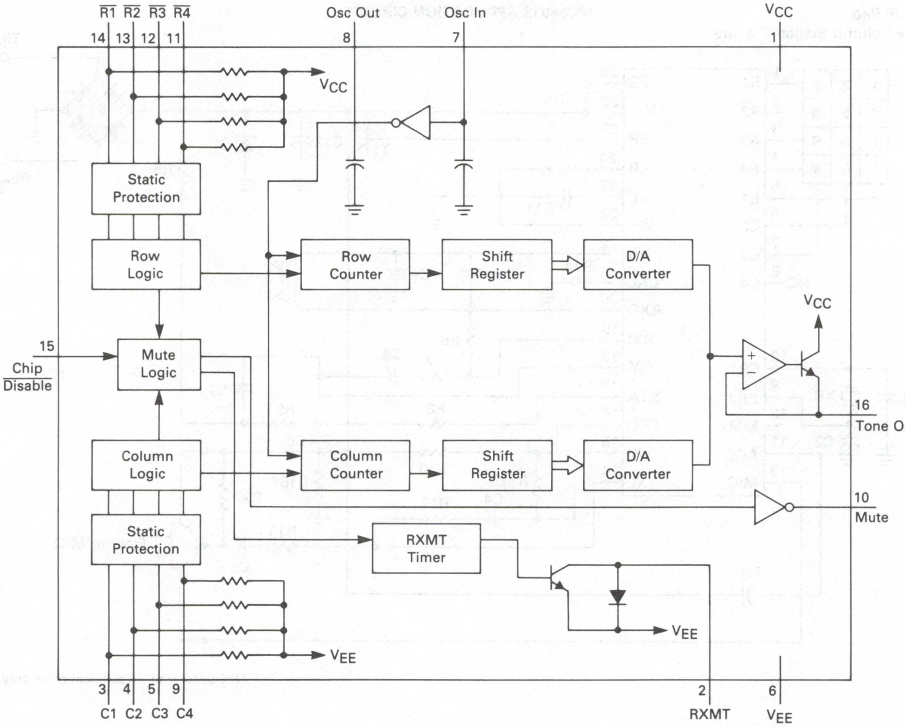
TELEPHONE TONE DIALER

BIPOLAR LINEAR/I^{2}L



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 — BLOCK DIAGRAM


R1 R2 R3 R4
14 13 12 11
Osc Out
8
Osc In
7
VCC
1
VCC
Static Protection
Row Logic
Row Counter
Shift Register
D/A Converter
VCC
15
Chip Disable
Mute Logic
+
−
16
Tone Out
Column Logic
Column Counter
Shift Register
D/A Converter
10
Mute
Static Protection
RXMT Timer
VEE
VEE
3 4 5 9
C1 C2 C3 C4
2
RXMT
6
VEE

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MOTOROLA

MC34017

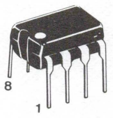
Product Preview

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients
- Push-Pull Output Stage for Greater Output Power Capability

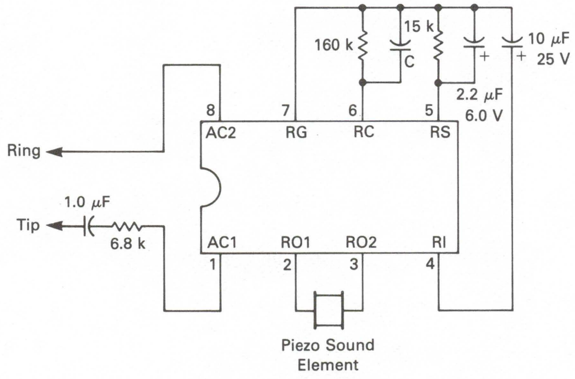
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^{2}L



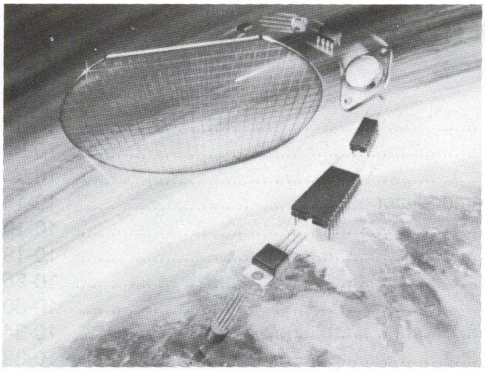
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

APPLICATION CIRCUIT


160 k
15 k
C
10 μF
25 V
2.2 μF
6.0 V
8
7
6
5
AC2
RG
RC
RS
Ring
1.0 μF
Tip
6.8 k
AC1
RO1
RO2
RI
1
2
3
4
Piezo Sound Element

MC34017-1: C = 1000 pF
MC34017-2: C = 500 pF
MC34017-3: C = 2000 pF

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



Consumer

10

CONSUMER

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MOTOROLA

CA3054

Advance Information

GENERAL PURPOSE TRANSISTOR ARRAY

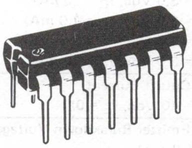
SILICON MONOLITHIC INTEGRATED CIRCUIT

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIER

The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from dc to 120 MHz.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage — ±5 mV

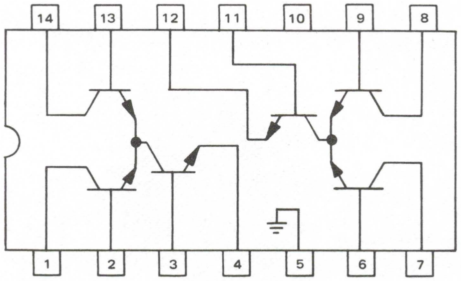


CASE 646-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS



Pin 5 is connected to substrate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER					
Input Offset Voltage (V_{CB} = 3.0 Vdc)	V_{IO}	–	–	5.0	mV
Input Offset Current (V_{CB} = 3.0 Vdc)	I_{IO}	–	–	2.0	μA
Input Bias Current (V_{CB} = 3.0 Vdc)	I_{IB}	–	–	24	μA
STATIC CHARACTERISTICS FOR EACH TRANSISTOR					
Base-Emitter Voltage	V_{BE}				Vdc
(V_{CB} = 3.0 Vdc, I_C = 50 μA)		–	–	0.70	
(V_{CB} = 3.0 Vdc, I_C = 1.0 mA)		–	–	0.80	
(V_{CB} = 3.0 Vdc, I_C = 3.0 mA)		–	–	0.85	
(V_{CB} = 3.0 Vdc, I_C = 10 mA)		–	–	0.90	
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	100	nA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mA)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	20	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	5.0	–	–	Vdc

MOTOROLA

MC1309

Advance Information

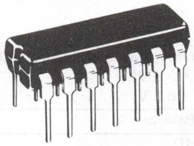
PHASE-LOCK LOOP FM STEREO DEMODULATOR

. . . a monolithic device using I^2L and ION Implant technology for use in solid-state stereo receivers.

- Requires No Inductors
- Low External Part Count
- Excellent Channel Separation Without Adjustment
- Only Single Potentiometer Oscillator Frequency Adjustment Necessary
- 50 mA Lamp or LED Driving Capability With Current Limiting
- Automatic, Transient-Free Stereo/Mono Switching
- Wide Dynamic Range: 0.25–1.7 V(p-p) Composite Input Signal
- Wide Supply Range: 4.5–16 Vdc
- Low Distortion: Typically 0.08% at 850 mV(p-p) Composite Input Signal
- Excellent SCA Rejection
- Gain Adjustable By Changing Load Resistors

PHASE-LOCK LOOP
FM STEREO
DEMODULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

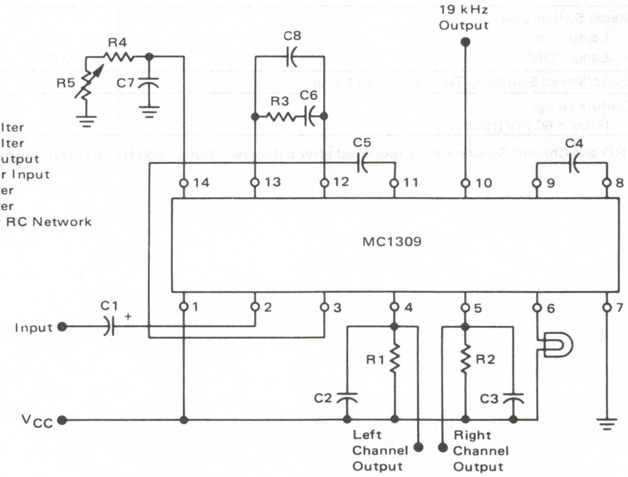
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}
Pin 2 = Input
Pin 3 = Amplifier Output
Pin 4 = Left Channel Output
Pin 5 = Right Channel Output
Pin 6 = Lamp Indicator
Pin 7 = Ground
Pin 8 = Switch Filter
Pin 9 = Switch Filter
Pin 10 = 19 kHz Output
Pin 11 = Modulator Input
Pin 12 = Loop Filter
Pin 13 = Loop Filter
Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 μF
C2 = 0.022 μF
C3 = 0.022 μF
C4 = 0.25 μF
C5 = 0.05 μF
C6 = 0.5 μF
C7 = 470 pF
C8 = 0.25 μF
R1 = 3.3 kΩ
R2 = 3.3 kΩ
R3 = 1.0 kΩ
R4 = 16 kΩ
R5 = 5.0 kΩ



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Lamp Current	50	mA
Junction Temperature	150	°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +9 Vdc, T_A = +25°C, 1.7 V(p-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level for stereo tests: 1.7 V(p-p) 1 kHz input signal for monaural tests; using circuit in Figure 1.

Characteristic	Min	Typ	Max	Unit
Current Drain	—	11	—	mAdc
Maximum Standard Composite Input Signal (0.5% THD)*				V(p-p)
(V_{CC} = 9.0 V)	1.7	2.1	—	
(V_{CC} = 6.0 V)	0.85	1.7		
Maximum Monaural Input Signal (1.0% THD)*				V(p-p)
(V_{CC} = 9.0 V)	1.7	2.2	—	
(V_{CC} = 6.0 V)	0.85	1.7	—	
Channel Balance	—	0	1.0	dB
Stereo THD (V_{in} = 0.85 V[p-p])	—	0.06	—	%
Monaural THD (V_{in} = 0.85 V[p-p])	—	0.08	—	%
Channel Separation				dB
(f = 100 Hz)	—	45	—	
(f = 1.0 kHz)	30	47	—	
(f = 10 kHz)	—	40	—	
Monaural Gain	0.6	0.9	—	V/V
Input Impedance	15	30	—	kΩ
Ultrasonic Frequency Rejection 19 kHz	—	35	—	dB
38 kHz	—	45	—	
SCA Rejection	—	75	—	dB
Stereo Switch Level				mV
Lamp "On"	—	9.0	12	
Lamp "Off"	2.0	4.5	—	
Mono/Stereo Switching Transient — No Lamp	—	0	—	mV
Capture Range (Pilot = 60 mV[RMS])	—	±7.0	—	%

*THD and Channel Separation are measured after a Bandpass Filter (200 Hz-10 kHz), unless otherwise specified.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1310P	−40°C to +85°C	Plastic DIP

MC1310P

Specifications and Applications Information

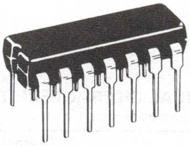
FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection



CASE 646-05

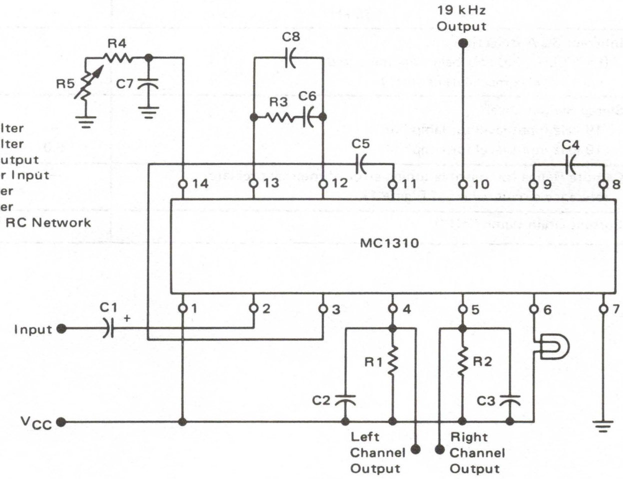
FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT

Pin Functions

Pin 1 = V_{CC}
Pin 2 = Input
Pin 3 = Amplifier Output
Pin 4 = Left Channel Output
Pin 5 = Right Channel Output
Pin 6 = Lamp Indicator
Pin 7 = Ground
Pin 8 = Switch Filter
Pin 9 = Switch Filter
Pin 10 = 19 kHz Output
Pin 11 = Modulator Input
Pin 12 = Loop Filter
Pin 13 = Loop Filter
Pin 14 = Oscillator RC Network

Parts List

C1 = 2.0 µF
C2 = 0.02 µF
C3 = 0.02 µF
C4 = 0.25 µF
C5 = 0.05 µF
C6 = 0.5 µF
C7 = 470 pF
C8 = 0.25 µF
R1 = 3.9 kΩ
R2 = 3.9 kΩ
R3 = 1.0 kΩ
R4 = 16 kΩ
R5 = 5.0 kΩ



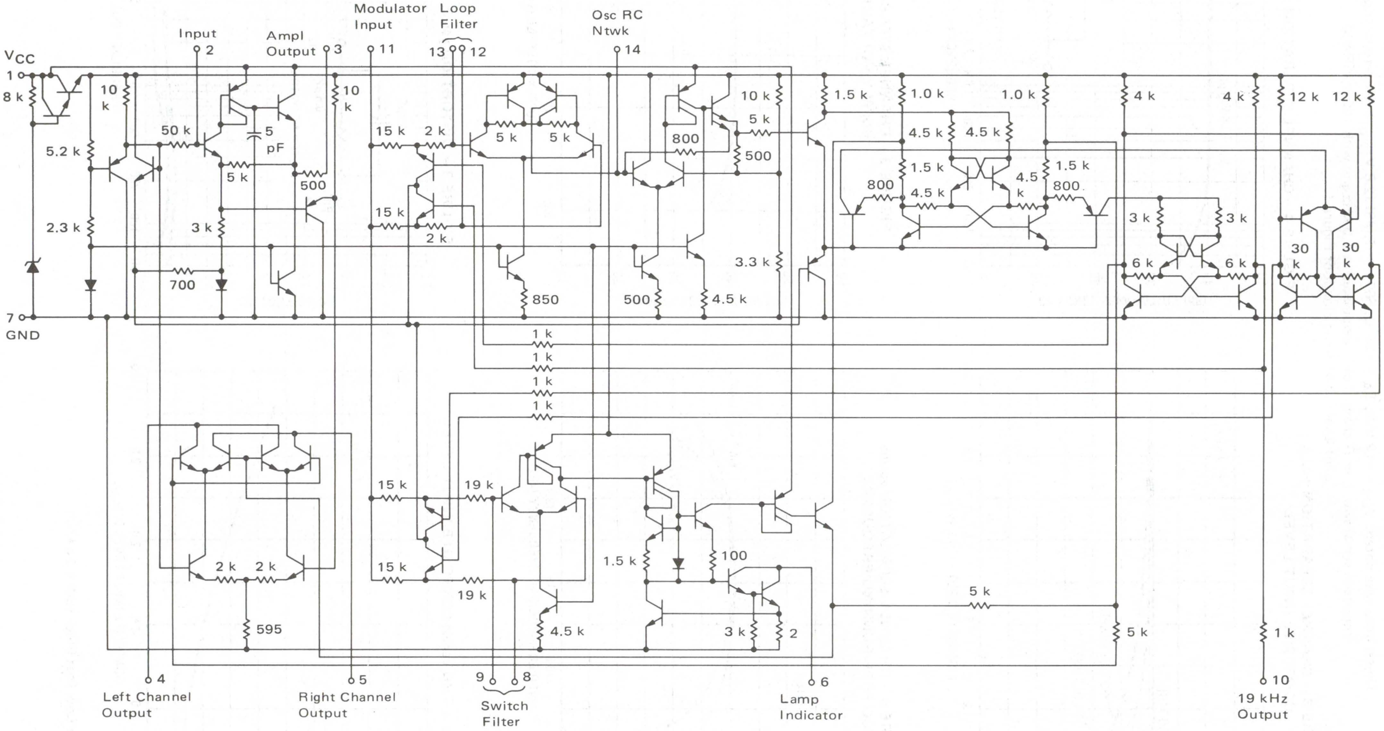
MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation)	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{[p-p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	–	–	$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8	–	–	$V_{(p-p)}$
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Audio Output Voltage (desired channel)	–	485	–	mV(RMS)
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.3	–	%
Ultrasonic Frequency Rejection 19 kHz	–	34.4	–	dB
38 kHz	–	45	–	
Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level				mV(RMS)
19 kHz input level for lamp "on"	–	–	20	
19 kHz input level for lamp "off"	5.0	–	–	
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	13	–	mAdc

FIGURE 2 – CIRCUIT SCHEMATIC


VCC
1
8 k
10 k
5.2 k
2.3 k
7
GND
700
Input
2
50 k
5 k
3 k
5 pF
Ampl Output
3
500
10 k
Modulator Input
11
Loop Filter
13
12
15 k
2 k
15 k
2 k
5 k
5 k
850
Osc RC Ntwk
14
800
500
10 k
5 k
500
4.5 k
3.3 k
1.5 k
1.0 k
1.0 k
4.5 k
4.5 k
1.5 k
4.5 k
1.5 k
800
4.5 k
800
4.5 k
4 k
4 k
3 k
3 k
6 k
6 k
12 k
12 k
30 k
30 k
1 k
1 k
1 k
1 k
2 k
2 k
595
15 k
19 k
15 k
19 k
4.5 k
1.5 k
100
3 k
2
5 k
5 k
1 k
4
Left Channel Output
5
Right Channel Output
9
8
Switch Filter
6
Lamp Indicator
10
19 kHz Output

TYPICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C; 560 mV(RMS) (2.8 $V_{[p\text{-}p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

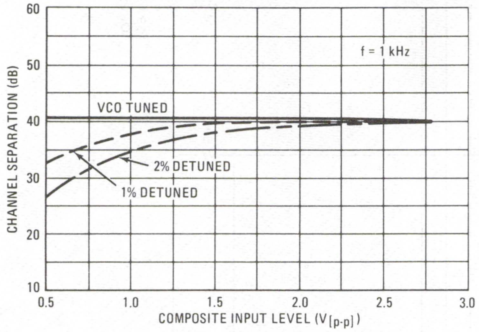


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

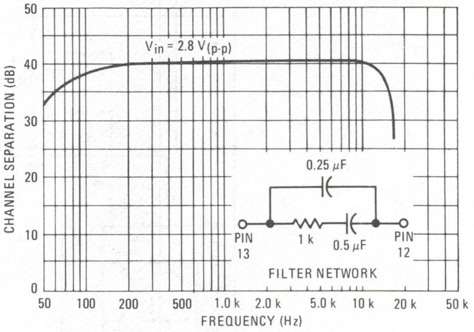


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE-RUNNING FREQUENCY

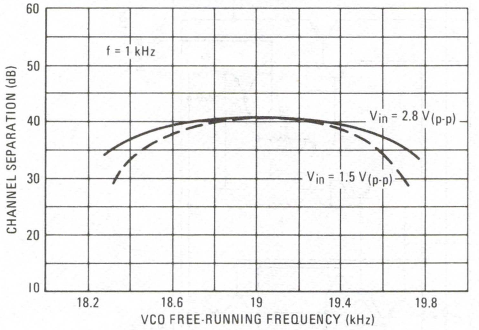


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

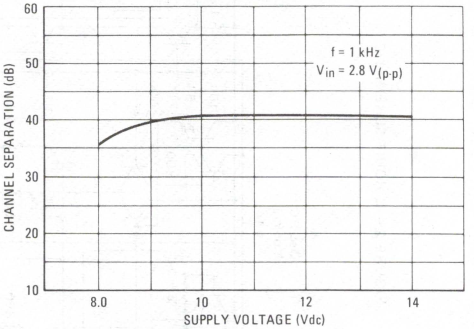


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL*

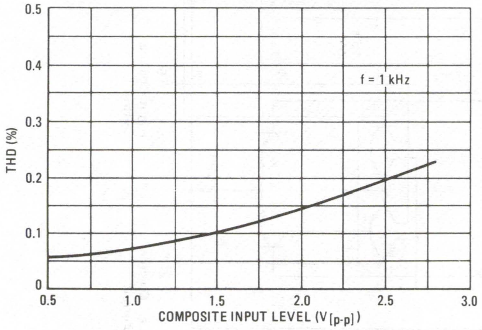
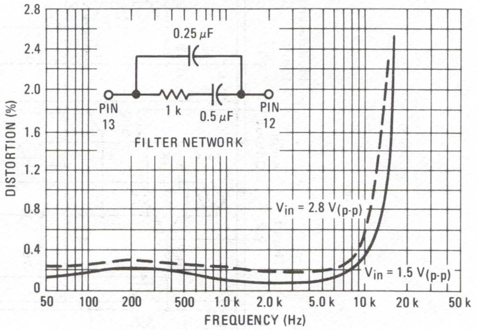


FIGURE 8 – DISTORTION versus FREQUENCY*



*Measured with Low Pass Filter (BW = 15 kHz).

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DISTORTION versus FREQUENCY*

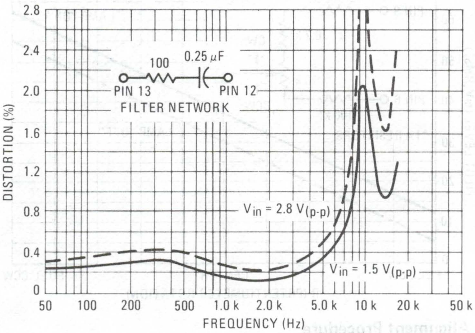


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

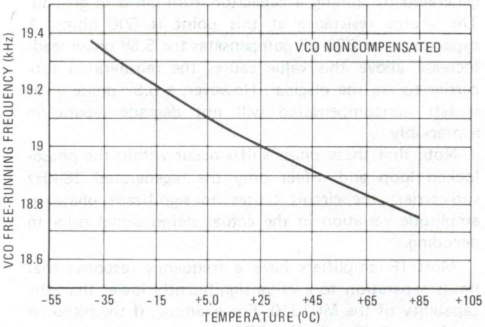


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE

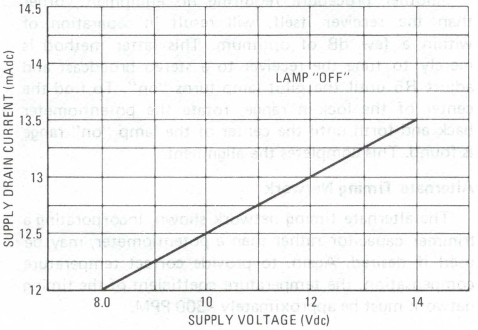
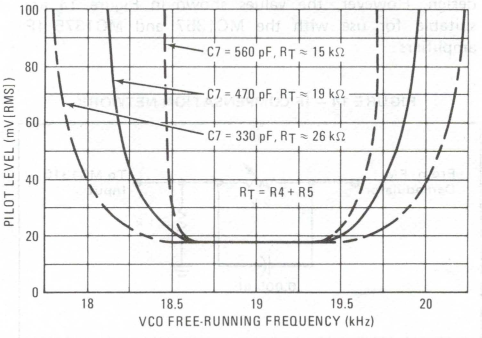
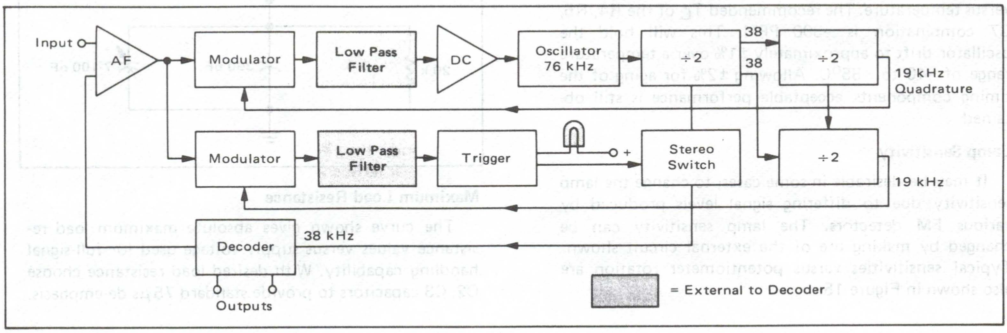


FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 13 – SYSTEM BLOCK DIAGRAM


Input
AF
Modulator
Low Pass Filter
DC
Oscillator 76 kHz
÷2
38
38
÷2
19 kHz Quadrature
Modulator
Low Pass Filter
Trigger
+
Stereo Switch
÷2
19 kHz
Decoder
38 kHz
Outputs
= External to Decoder

APPLICATIONS INFORMATION (continued)

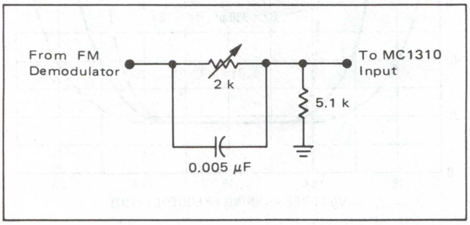
additional lead of 3.5° (for C5 = 0.05 µF) giving a total lead of 5.5°.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated subcarrier to lag the original. However, a 5.5° phase error if left noncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 – IF COMPENSATION NETWORK



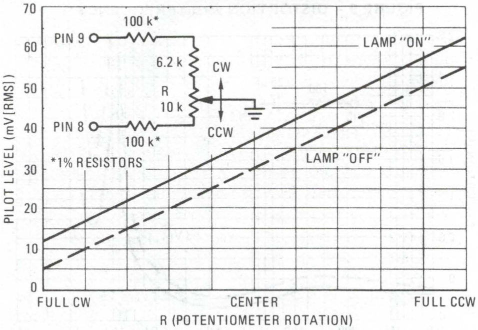
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM. This will hold the oscillator drift to approximately ±1% over a temperature range of -40 to +85°C. Allowing ±2% for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 – PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

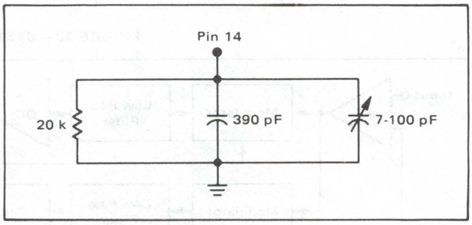
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM.

FIGURE 16



Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard 75 µs de-emphasis.

CIRCUIT OPERATION

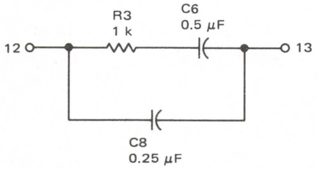
Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

C1	Input coupling capacitor; 2.0 μF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.
R1, R2, C2, C3	See Maximum Load Resistance section.
C4	Filter capacitor for stereo switch level detector; time constant is C4 x 53 kilohms ±30%, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.
C5	See Phase Compensation section.
R3, C6, C8	Phase-locked loop filter components; the following network is recommended:  When less performance is required a simpler network consisting of R3 = 100 ohms and C6 = 0.25 μF may be used (omit C8). See Figure 9.
R4, R5, C7	Oscillator timing network; recommended values: C7 = 470 pF 1% R4 = 16 kΩ 1% R5 = 5 kΩ Preset These values give ±3.5% typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.
Stereo Lamp	Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.
19-kHz Output	A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired. Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

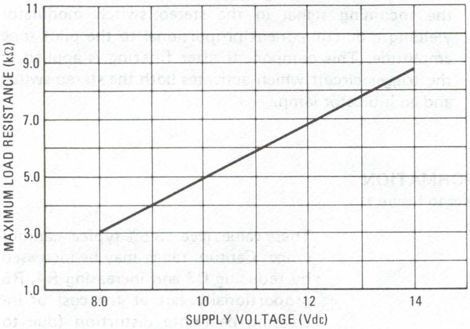
Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2^{o}. The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

FIGURE 17 – MAXIMUM LOAD RESISTANCE versus SUPPLY VOLTAGE



Audio Output

The ratio $G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}}$ for different types of input is as follows:

INPUT	
Single-Channel Composite Signal	Monaural Signal
0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

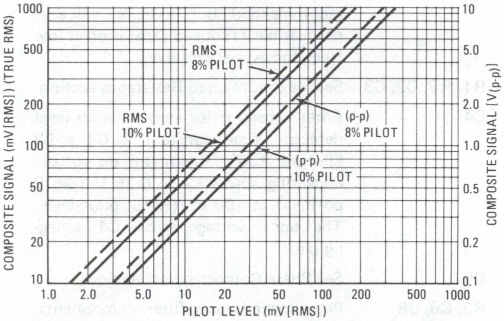
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 – COMPOSITE LEVEL versus PILOT (L or R Modulation Only)

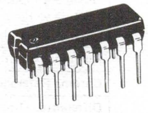


MC1327

DUAL DOUBLY BALANCED CHROMA DEMODULATOR for PAL or NTSC

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646-05



ORDERING INFORMATION

Device	Temperature Range	Package
MC1327P	−20°C to +75°C	Plastic DIP

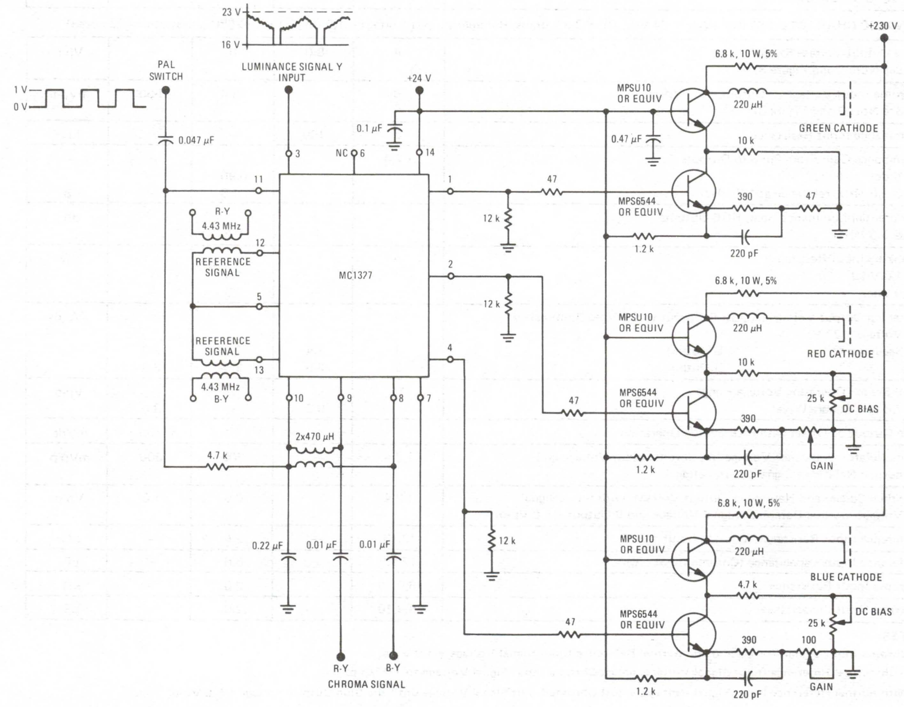
Advance Information

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Good Chroma Sensitivity — 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage — 0.6 V Maximum
- Differential DC Temperature Stability — 0.7 mV/°C
- High Blue Output Voltage Swing — 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

FIGURE 1 — TYPICAL APPLICATION CIRCUIT


23 V
16 V
LUMINANCE SIGNAL Y INPUT
PAL SWITCH
1 V
0 V
+24 V
+230 V
0.047 μF
0.1 μF
0.47 μF
3
NC 6
14
11
12
5
13
1
2
4
10
9
8
7
R-Y
4.43 MHz
REFERENCE SIGNAL
REFERENCE SIGNAL
4.43 MHz
B-Y
MC1327
47
12 k
12 k
12 k
47
47
2x470 μH
4.7 k
0.22 μF
0.01 μF
0.01 μF
R-Y
B-Y
CHROMA SIGNAL
6.8 k, 10 W, 5%
MPSU10 OR EQUIV
220 μH
GREEN CATHODE
10 k
MPS6544 OR EQUIV
390
47
1.2 k
220 pF
6.8 k, 10 W, 5%
MPSU10 OR EQUIV
220 μH
RED CATHODE
10 k
MPS6544 OR EQUIV
25 k
DC BIAS
390
1.2 k
220 pF
GAIN
6.8 k, 10 W, 5%
MPSU10 OR EQUIV
220 μH
BLUE CATHODE
4.7 k
MPS6544 OR EQUIV
DC BIAS
25 k
390
100
1.2 k
220 pF
GAIN

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage (See Figure 2)	1,2,4	13.2	14.5	15.8	Vdc
Quiescent Input Current from Supply (Figure 2) ($R_L = \infty$) (R_L = 3.3 k ohms)		 – 16	 7.5 19	 – 26	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (See Note 1 and Figure 2)	1,2,4	–	0.3	0.6	Vdc
Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	0.7	–	mV/°C
Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	+0.5	±5.0	mV/°C

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Characteristic	Pin No.	Min	Typ	Max	Unit
Blue Output Voltage Swing (See Note 2 and Figure 3)	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) (See Note 3 and Figure 3)	8	–	280	550	mVp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz, reference at 100 kHz)	1,2,4	 – –	 0.95 -1.8	 – –	– dB
Differential Luminance Gain, RGB Outputs (@ 5.0 MHz)		–	0.3	–	dB
Blanking Input Resistance (1.0 Vdc) (0 Vdc)	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) (See Note 4) G Output R Output	4 1 2	 1.4 2.5	 1.8 2.9	 2.2 3.3	Vp-p
PAL Switch Operating Voltage Range (7.8 kHz Square Wave)	11	0.3	–	3.0	Vp-p
R-Y Output dc Offset with PAL Switch Operation		–	–	100	mVdc
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	200	300	mVp-p
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1,2,4	–	0.6	1.0	Vp-p
Reference Input Resistance (Chroma Input = 0)	12,13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12,13	–	6.0	–	pF
Chroma Input Resistance	8,9,10	–	2.0	–	kΩ
Chroma Input Capacitance	8,9,10	–	2.0	–	pF

NOTES:

1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p.
4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 kilohms, T_A = +25°C unless otherwise noted)

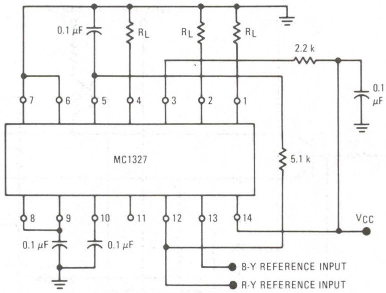
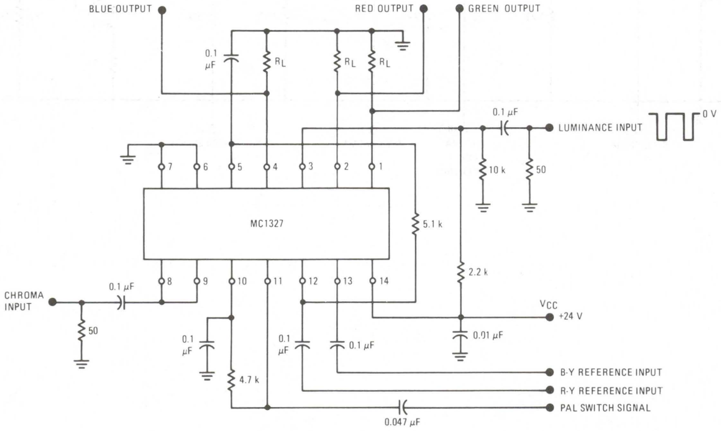
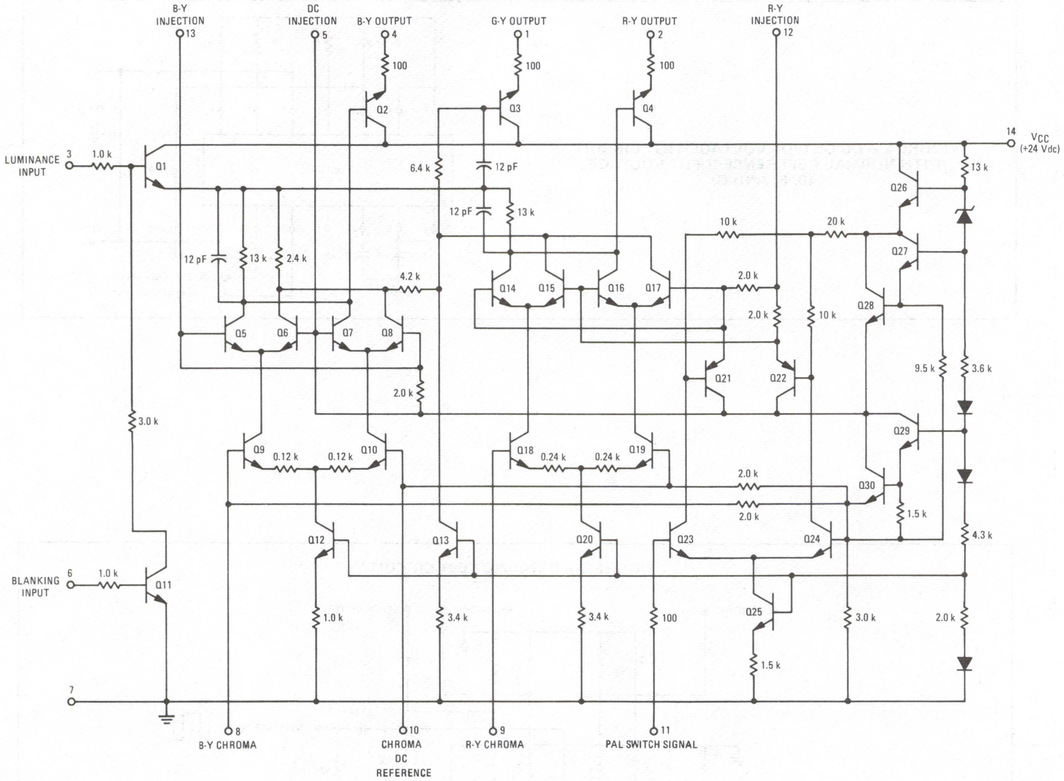

0.1 μF
RL
RL
RL
2.2 k
0.1 μF
7
6
5
4
3
2
1
MC1327
5.1 k
8
9
10
11
12
13
14
VCC
0.1 μF
0.1 μF
B-Y REFERENCE INPUT
R-Y REFERENCE INPUT

FIGURE 2 — DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

FIGURE 3 — DYNAMIC TEST CIRCUIT


BLUE OUTPUT
RED OUTPUT
GREEN OUTPUT
0.1 μF
RL
RL
RL
0.1 μF
LUMINANCE INPUT
0 V
7
6
5
4
3
2
1
10 k
50
MC1327
5.1 k
2.2 k
8
9
10
11
12
13
14
CHROMA INPUT
0.1 μF
50
VCC
+24 V
0.01 μF
0.1 μF
0.1 μF
0.1 μF
4.7 k
B-Y REFERENCE INPUT
R-Y REFERENCE INPUT
PAL SWITCH SIGNAL
0.047 μF

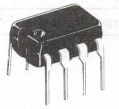
CHROMA DEMODULATOR


B-Y INJECTION 13
DC INJECTION 5
B-Y OUTPUT 4
G-Y OUTPUT 1
R-Y OUTPUT 2
R-Y INJECTION 12
14 VCC (+24 Vdc)
LUMINANCE INPUT 3
1.0 k
Q1
Q2
Q3
Q4
100
100
100
6.4 k
12 pF
12 pF
13 k
13 k
2.4 k
12 pF
4.2 k
Q5
Q6
Q7
Q8
Q14
Q15
Q16
Q17
10 k
20 k
2.0 k
2.0 k
10 k
Q21
Q22
Q26
Q27
Q28
Q29
Q30
13 k
9.5 k
3.6 k
2.0 k
3.0 k
Q9
0.12 k
0.12 k
Q10
Q18
0.24 k
0.24 k
Q19
2.0 k
2.0 k
1.5 k
4.3 k
Q12
Q13
Q20
Q23
Q24
Q25
BLANKING INPUT 6
1.0 k
Q11
1.0 k
3.4 k
3.4 k
100
1.5 k
3.0 k
2.0 k
7
8 B-Y CHROMA
10 CHROMA DC REFERENCE
9 R-Y CHROMA
11 PAL SWITCH SIGNAL

MC1330A1P
MC1330A2P

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626-04

ORDERING INFORMATION

Device	Temperature Range	Package
MC1330A1P	0°C to +75°C	Plastic DIP
MC1330A2P	0°C to +75°C	Plastic DIP

LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

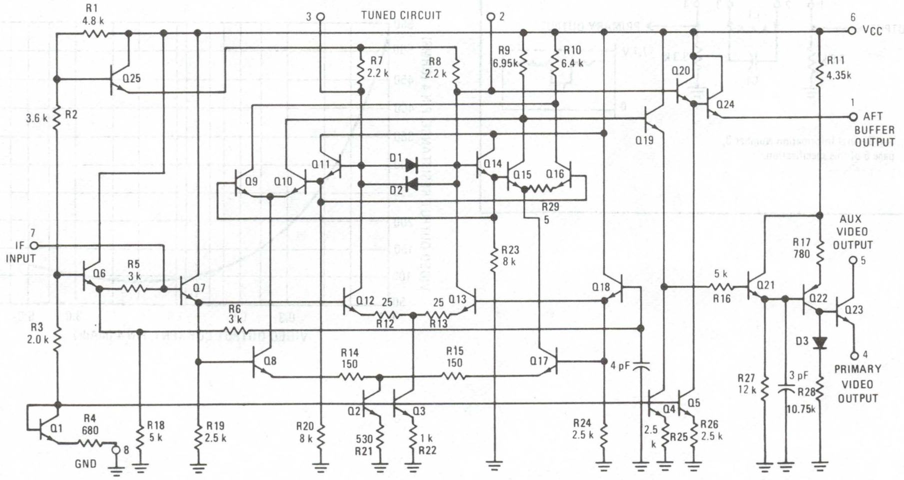
The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

OUTPUT VOLTAGE SELECTION

The MC1330A1P is identical to the MC1330A2P with the following exception:

	ZERO SIGNAL DC OUTPUT VOLTAGE
MC1330A1P	7.0 to 8.2 Vdc
MC1330A2P	7.8 to 9.0 Vdc

FIGURE 1 – CIRCUIT SCHEMATIC


R1
4.8 k
Q25
3.6 k R2
7
IF INPUT
Q6
R5
3 k
Q7
R6
3 k
R3
2.0 k
Q8
Q1
R4
680
8
GND
R18
5 k
R19
2.5 k
3
TUNED CIRCUIT
2
R7
2.2 k
R8
2.2 k
Q9
Q10
Q11
D1
D2
Q14
Q15
Q16
R29
5
R9
6.95k
R10
6.4 k
R23
8 k
Q12 25
R12
25 Q13
R13
R14
150
R15
150
Q2
Q3
R20
8 k
530
R21
1 k
R22
Q17
Q18
4 pF
R24
2.5 k
Q4
Q5
2.5 k
R25
R26
2.5 k
Q19
Q20
Q24
6
VCC
R11
4.35k
1
AFT BUFFER OUTPUT
AUX VIDEO OUTPUT
R17
780
5
5 k
R16
Q21
Q22
Q23
D3
4
PRIMARY VIDEO OUTPUT
R27
12 k
3 pF
R28
10.75k

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, fc = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	MC1330A1P MC1330A2P	4 4	7.0 7.8	– –	8.2 9.0	Vdc Vdc
Supply Current		5, 6	11	17.5	20	mA
Maximum Signal dc Output Voltage		4	–	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)		7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency		1	300	475	650	mVp-p

FIGURE 3 – INPUT ADMITTANCE

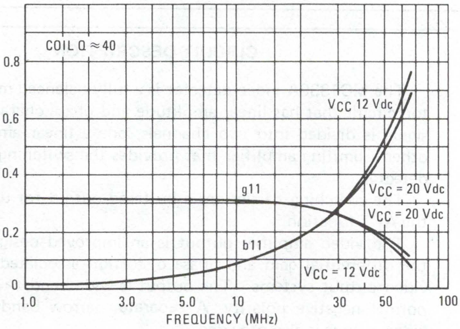


FIGURE 2 – TEST FIXTURE CIRCUIT

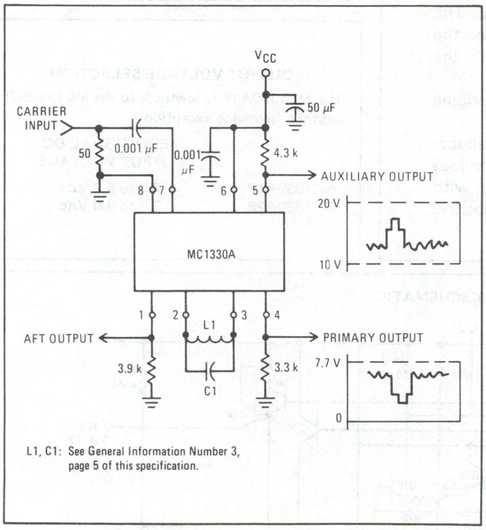
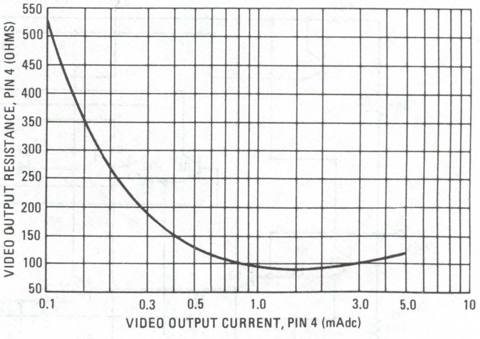

V_{CC}
50 μF
CARRIER INPUT
0.001 μF
50
0.001 μF
4.3 k
8
7
6
5
AUXILIARY OUTPUT
20 V
10 V
MC1330A
1
2
3
4
L1
AFT OUTPUT
PRIMARY OUTPUT
3.9 k
C1
3.3 k
7.7 V
0
L1, C1: See General Information Number 3, page 5 of this specification.

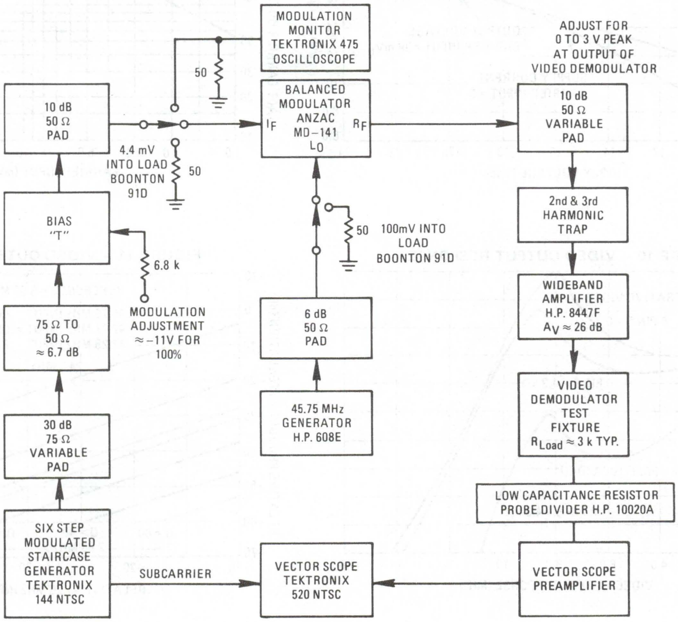
FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Typ	Unit
Input Resistance	7	4.9	kΩ
Input Capacitance	7	1.5	pF
Internal Resistance (Across Tuned Circuit)	2, 3	4.4	kΩ
Internal Capacitance (Across Tuned Circuit)	2, 3	1.0	pF
Negative Video Output Bandwidth (Figure 10)	4	10.8	MHz
Positive Video Output Bandwidth (Figure 10)	5	2.2	MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	4	7.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	4	4.0	%
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	4	8.0	Degrees
Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	4	6.0	%
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = - 6 dB 41.25 MHz = -20 dB	4	−38	dB
Video Output Resistance @ 1 MHz, 2 mA	4	94	Ω
Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.) V_{CC} = 12 Vdc V_{CC} = 15 Vdc V_{CC} = 20 Vdc V_{CC} = 24 Vdc	7	2.0 2.6 3.6 4.6	Volts
Power Supply Voltage Range	5	10 to 24	Volts

FIGURE 5 – DIFFERENTIAL PHASE AND GAIN TEST SET UP


MODULATION MONITOR TEKTRONIX 475 OSCILLOSCOPE
50
ADJUST FOR 0 TO 3 V PEAK AT OUTPUT OF VIDEO DEMODULATOR
10 dB 50 Ω PAD
BALANCED MODULATOR ANZAC MD−141
I_F
R_F
L_O
10 dB 50 Ω VARIABLE PAD
4.4 mV INTO LOAD BOONTON 91D
50
2nd & 3rd HARMONIC TRAP
BIAS "T"
50
100mV INTO LOAD BOONTON 91D
6.8 k
WIDEBAND AMPLIFIER H.P. 8447F $A_V \approx$ 26 dB
75 Ω TO 50 Ω ≈ 6.7 dB
MODULATION ADJUSTMENT ≈ −11V FOR 100%
6 dB 50 Ω PAD
VIDEO DEMODULATOR TEST FIXTURE $R_{Load} \approx$ 3 k TYP.
30 dB 75 Ω VARIABLE PAD
45.75 MHz GENERATOR H.P. 608E
LOW CAPACITANCE RESISTOR PROBE DIVIDER H.P. 10020A
SIX STEP MODULATED STAIRCASE GENERATOR TEKTRONIX 144 NTSC
SUBCARRIER
VECTOR SCOPE TEKTRONIX 520 NTSC
VECTOR SCOPE PREAMPLIFIER

TYPICAL CHARACTERISTICS

(V_{CC} = +20 Vdc, T_A = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

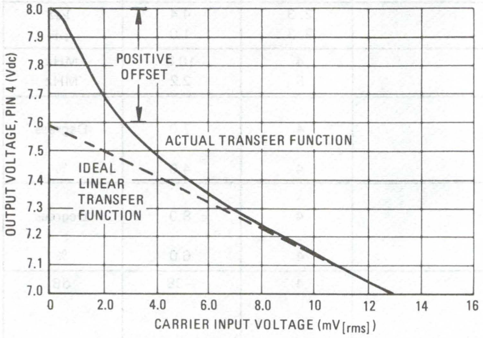


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

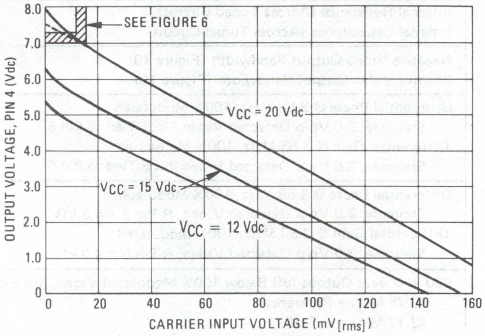


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

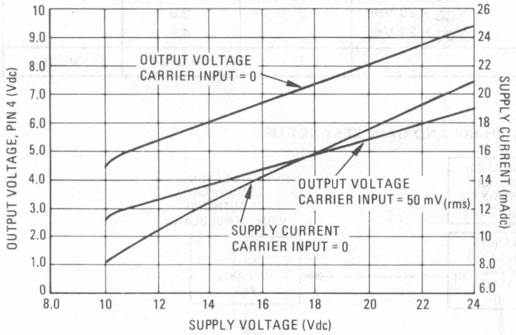


FIGURE 9 – AFT LIMITING

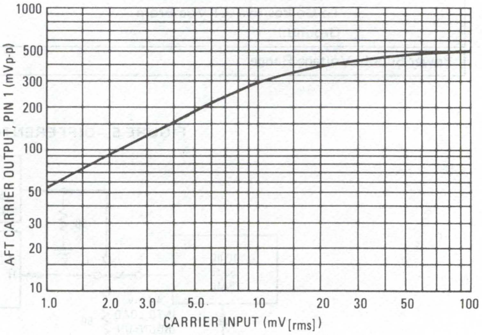


FIGURE 10 – VIDEO OUTPUT RESPONSE

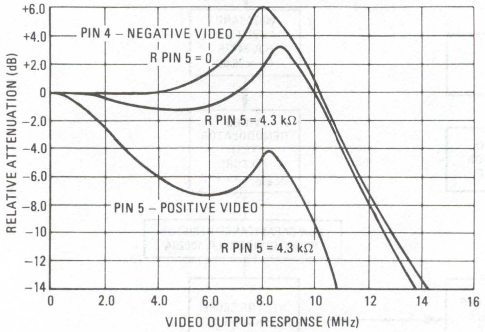
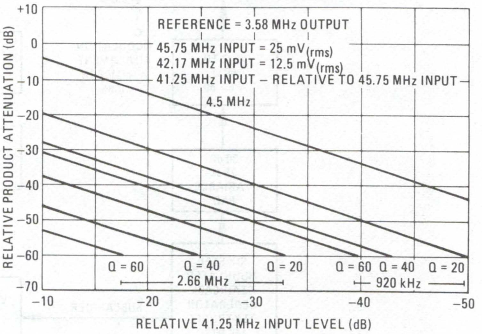


FIGURE 11 – VIDEO OUTPUT PRODUCTS



TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.
5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.
6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.
7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 — BANDPASS DISPLAYED BY CONVENTIONAL SWEEP

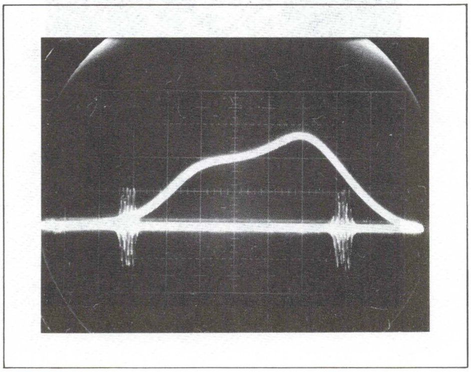


FIGURE 13 — BANDPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION

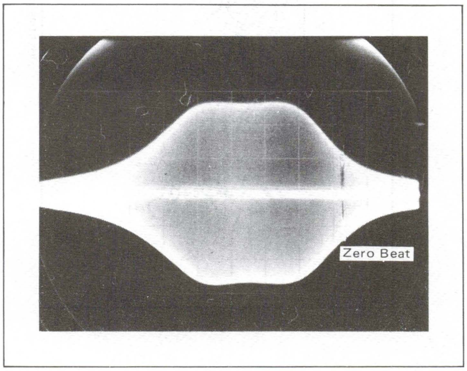
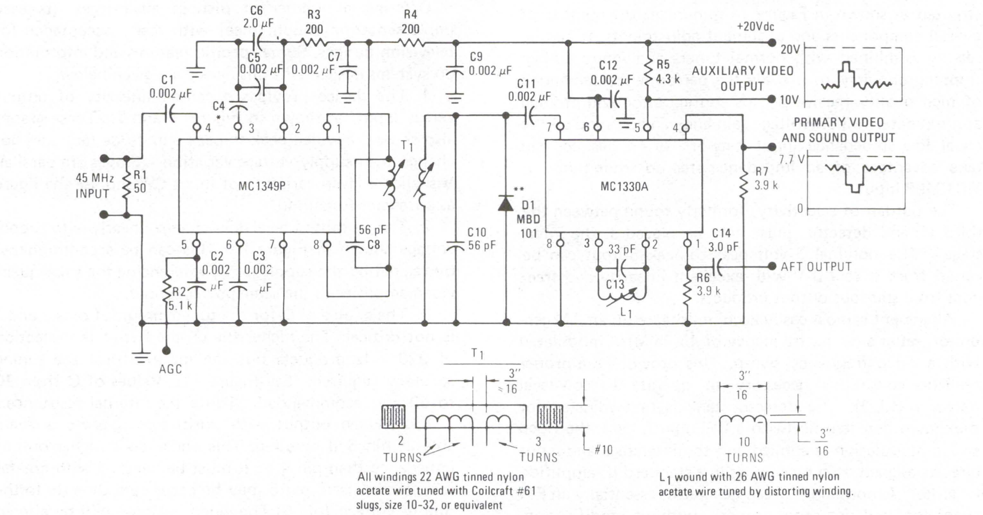


FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT


C6 2.0 μF
R3 200
R4 200
+20Vdc
C5 0.002 μF
C7 0.002 μF
C9 0.002 μF
C1 0.002 μF
C4 *
C11 0.002 μF
C12 0.002 μF
R5 4.3 k
20V
AUXILIARY VIDEO OUTPUT
10V
PRIMARY VIDEO AND SOUND OUTPUT
7.7 V
0
R7 3.9 k
45 MHz INPUT
R1 50
MC1349P
T1
56 pF C8
D1 MBD 101 **
C10 56 pF
MC1330A
33 pF
C13
L1
C14 3.0 pF
R6 3.9 k
AFT OUTPUT
C2 0.002 μF
C3 0.002 μF
R2 5.1 k
AGC
3"/16
2 TURNS
3 TURNS
#10
10 TURNS
All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent
L1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet.
**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6.

FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT

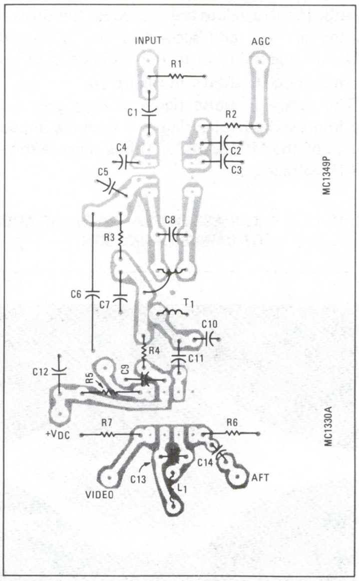
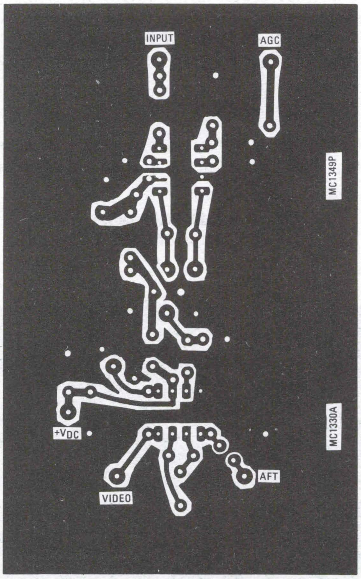

INPUT
AGC
R1
C1
R2
C4
C2
C3
C5
C8
R3
T1
C6
C7
C10
R4
C11
C12
R5
C9
R7
R6
+VDC
C14
C13
L1
VIDEO
AFT
MC1349P
COPPER SIDE UP
MC1330A

FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT


INPUT
AGC
MC1349P
COPPER SIDE UP
MC1330A
+VDC
AFT
VIDEO

MC1349P

IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

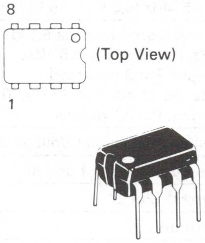
ORDERING INFORMATION

Device	Temperature Range	Package
MC1349P	0°C to +70°C	Plastic DIP

IF AMPLIFIER

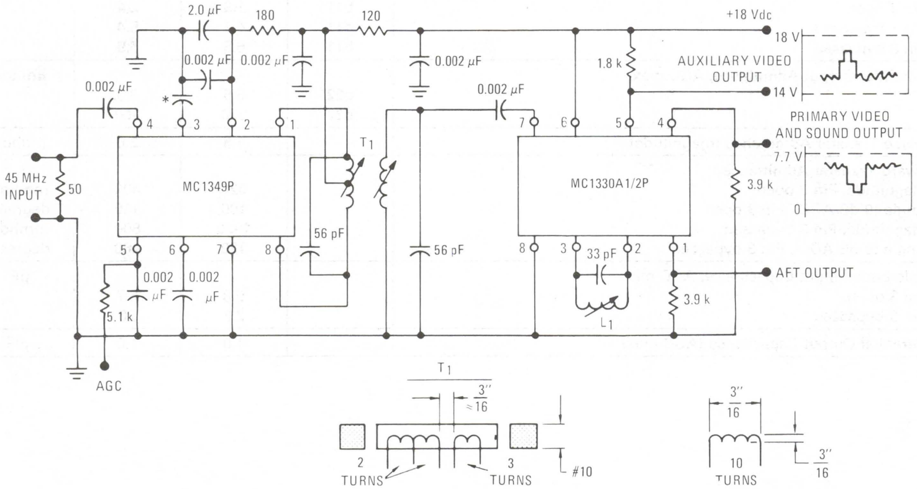
. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

- Power Gain — 60 dB typ at 45 MHz (Pin 3 open)
  - — 56 dB typ at 58 MHz (Pin 3 open)
  - — 61 dB typ at 45 MHz (Pin 3 bypassed)
  - — 59 dB typ at 58 MHz (Pin 3 bypassed)
- AGC Range — 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC



PLASTIC PACKAGE
CASE 626-04

FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT


2.0 μF
180
120
+18 Vdc
18 V
0.002 μF
0.002 μF
0.002 μF
1.8 k
AUXILIARY VIDEO OUTPUT
14 V
0.002 μF
*
0.002 μF
4
3
2
1
7
6
5
4
PRIMARY VIDEO AND SOUND OUTPUT
T1
7.7 V
45 MHz INPUT
50
MC1349P
MC1330A1/2P
3.9 k
0
56 pF
5
6
7
8
56 pF
8
3
33 pF
2
1
AFT OUTPUT
0.002 μF
0.002 μF
5.1 k
3.9 k
L1
AGC
T1
3″/16
≈16
2 TURNS
3 TURNS
#10
3″/16
10 TURNS
3″/16

All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L1 wound with ≈26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage (V_{CC1})	+18	Vdc
Output Supply Voltage (V_{CC2})	+18	Vdc
AGC Supply Voltage	≤ V_{CC1} (Pin 2)	Vdc
Differential Input Voltage	5.0	Vdc
Power Dissipation (Package Limitation)		
Plastic Package	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

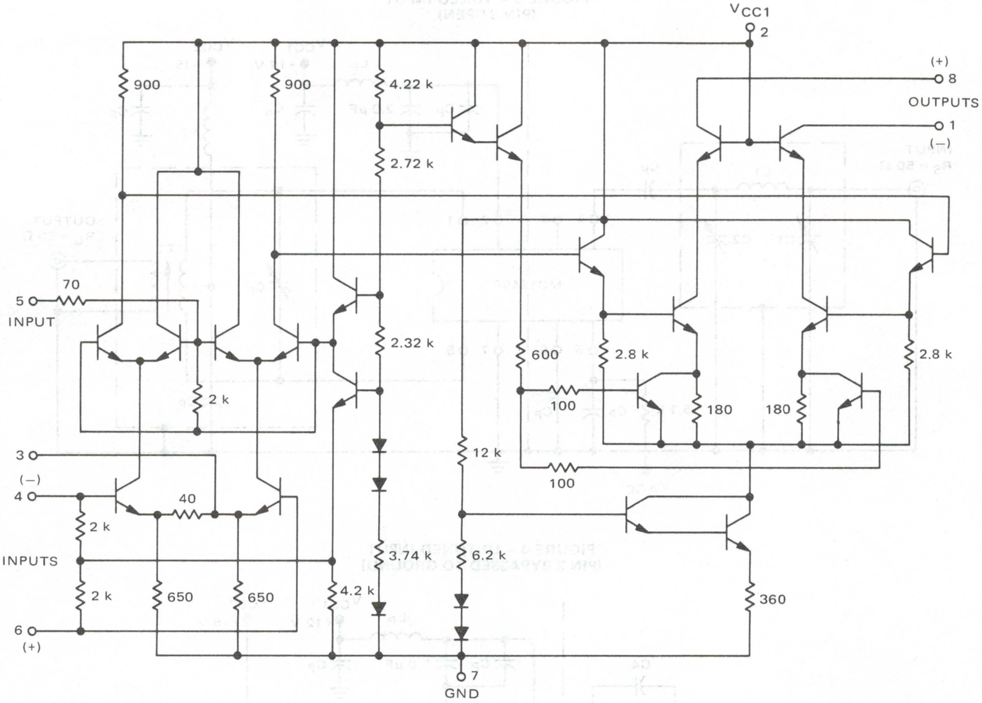
ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [Pin 2], V_{CC2} = +15 Vdc [Pins 1 and 8], T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3)	70	80	—	dB
Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input Pin 4)				dB
f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, Pin 3 open	52	60	—	
Untuned Input, Pin 3 bypassed	—	61	—	
f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, Pin 3 open	—	56	—	
Untuned Input, Pin 3 bypassed	—	59	—	
Maximum Differential Output Voltage Swing	—	6.0	—	Vp-p
Output Stage Current (Pins 1 and 8)	—	9.0	—	mA
Amplifier Current (Pin 2)	—	15	20	mAdc
Power Dissipation	—	315	400	mW
Noise Figure f = 45 MHz, Tuned Input, Pin 3 open, Gain Reduction = 15 dB	—	8.5	—	dB

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [Pin 2], V_{CC2} = +15 Vdc, [Pins 1 and 8], T_A = +25°C unless otherwise noted.)

		Frequency		
Parameter	Symbol	45 MHz	58 MHz	Unit
Single-Ended Input Admittance, input Pin 4, AGC min				mmhos
Pin 3 open	g_{11}	0.74	0.95	
Pin 3 open	b_{11}	1.9	2.4	
Pin 3 bypassed	g_{11}	4.1	5.4	
Pin 3 bypassed	b_{11}	6.5	6.9	
Differential Output Admittance, AGC max				μmhos
	g_{22}	5.5	8.3	
	b_{22}	270	360	
Reverse Transfer Admittance (magnitude)		1.5	2.0	μmhos
Forward Transfer Admittance				
Magnitude, Pin 3 open		520	400	mmhos
Angle (0 dB AGC), Pin 3 open		100	130	degrees
Magnitude, Pin 3 bypassed		1020	800	mmhos
Angle (0 dB AGC), Pin 3 bypassed		120	400	degrees
Single-Ended Input Capacitance, AGC min				pF
Pin 3 open		6.8	6.7	
Pin 3 bypassed		2.3	20	
Differential Output Capacitance (AGC max)		1.0	1.0	pF

FIGURE 2 – CIRCUIT SCHEMATIC



GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 µF at f = 45 MHz is a typical value for printed circuit applications.

TEST CIRCUITS

FIGURE 3 – TUNED INPUT (PIN 3 OPEN)

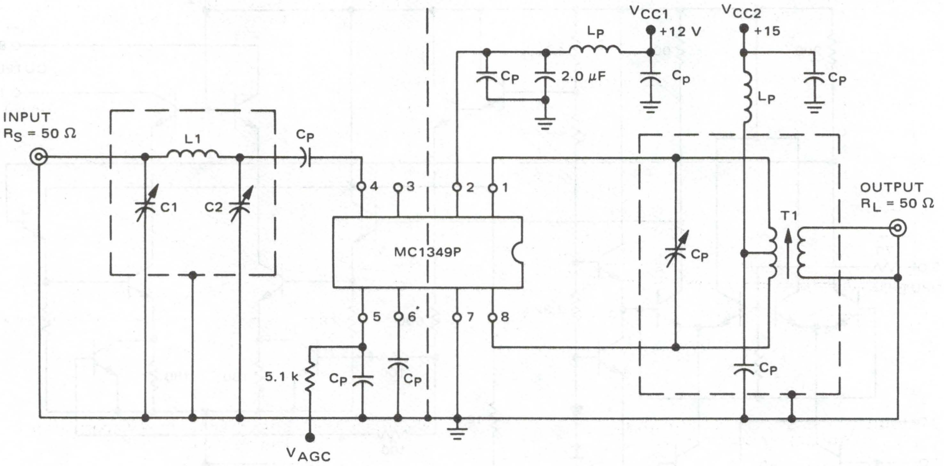
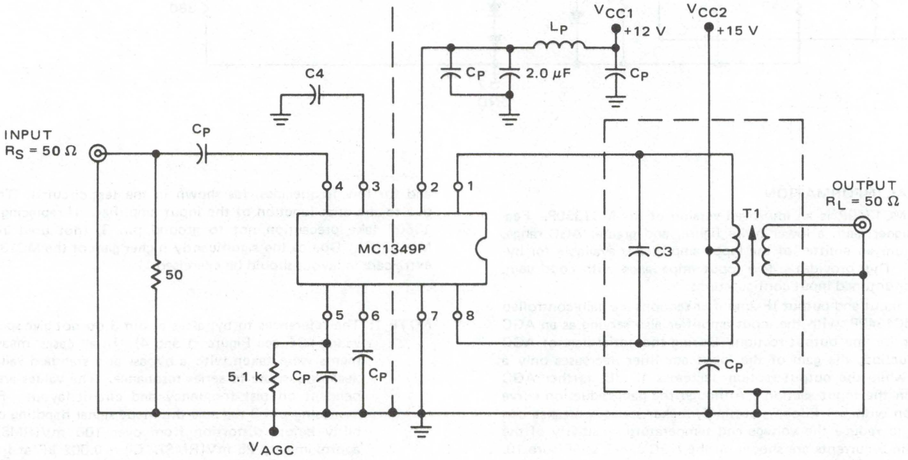

VCC1
+12 V
VCC2
+15
Lp
Cp
2.0 µF
Cp
Lp
Cp
INPUT
RS = 50 Ω
L1
Cp
C1
C2
4
3
2
1
MC1349P
5
6
7
8
OUTPUT
RL = 50 Ω
T1
Cp
Cp
5.1 k
Cp
Cp
VAGC

FIGURE 4 – UNTUNED INPUT (PIN 3 BYPASSED TO GROUND)


VCC1
+12 V
VCC2
+15 V
Lp
Cp
2.0 µF
Cp
C4
INPUT
RS = 50 Ω
Cp
4
3
2
1
MC1349P
50
5
6
7
8
OUTPUT
RL = 50 Ω
T1
C3
Cp
5.1 k
Cp
Cp
VAGC

PARTS LIST

COMPONENT	45 MHz	58 MHz
C1	8-60 pF	50-100 pF
C2	3-35 pF	3-35 pF
C3	1-7.0 pF	1-7.0 pF
C4	82-470 pF	82-470 pF
Cp	0.0015 µF	0.001 µF
L1	0.84 µH	0.33 µH
Lp	10 µH	10 µH

T1 Primary 14 turns center-tapped
Secondary 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
Wire: #26 AWG tinned nylon acetate wound on 1/4″ diameter coil form
Core: Arnold Type TH, 1/2″ long or equivalent.

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

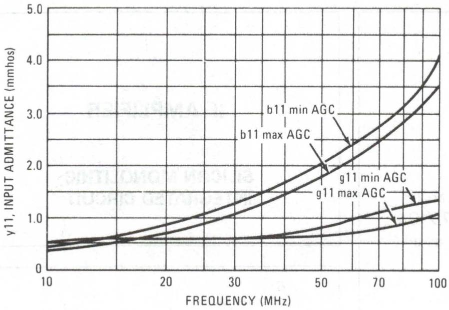


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

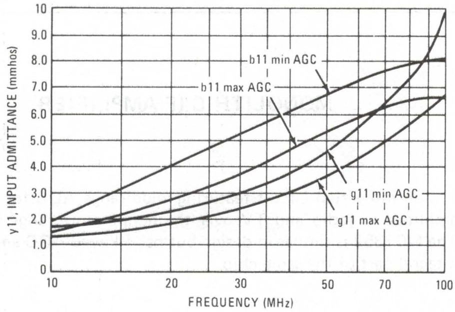


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

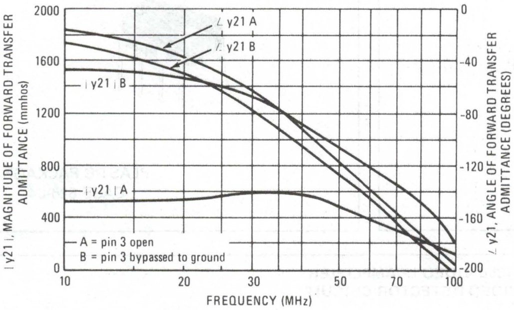


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

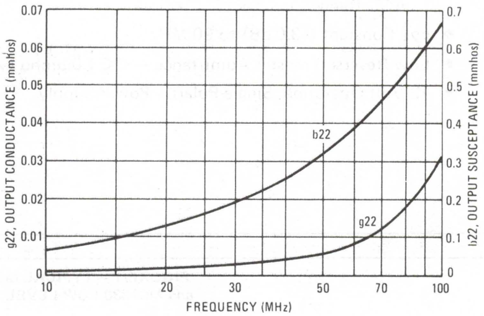


FIGURE 9 – NOISE FIGURE

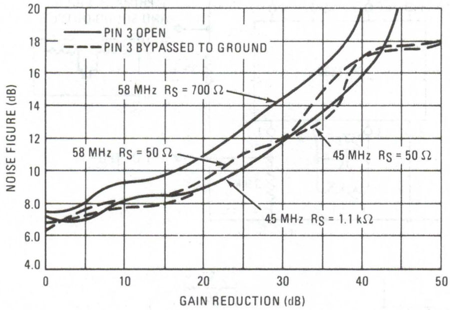
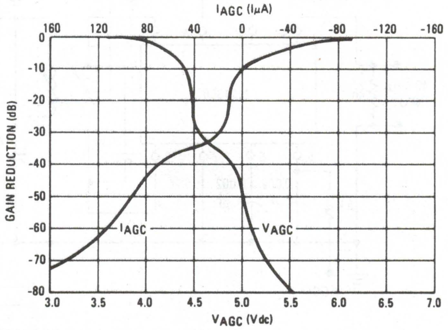


FIGURE 10 – GAIN REDUCTION



MC1350P

ORDERING INFORMATION

Device	Temperature Range	Package
MC1350P	0°C to +75°C	Plastic DIP

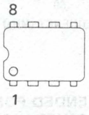
MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

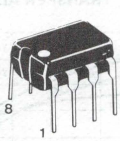
- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – << 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

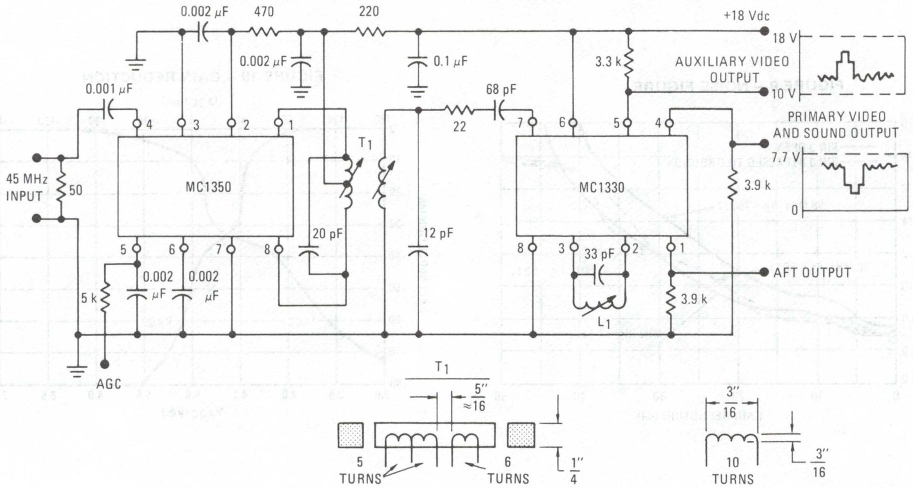


(Top View)



PLASTIC PACKAGE
CASE 626-04

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT


0.002 μF
470
220
+18 Vdc
0.002 μF
0.1 μF
3.3 k
18 V
AUXILIARY VIDEO OUTPUT
10 V
0.001 μF
68 pF
22
4
3
2
1
T1
7
6
5
4
PRIMARY VIDEO AND SOUND OUTPUT
7.7 V
45 MHz INPUT
50
MC1350
MC1330
3.9 k
0
20 pF
12 pF
5
6
7
8
8
3
33 pF
2
1
0.002 μF
0.002 μF
5 k
AFT OUTPUT
3.9 k
L1
AGC
T1
5″/16
≈16
1″/4
5 TURNS
6 TURNS
3″/16
16
10 TURNS
3″/16

All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.

L_1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)	A_p				dB
f = 58 MHz, BW = 4.5 MHz } See Figure 5		–	48	–	
f = 45 MHz, BW = 4.5 MHz } See Figure 5		46	50	–	
f = 10.7 MHz, BW = 350 kHz } See Figure 6		–	58	–	
f = 455 kHz, BW = 20 kHz } See Figure 6		–	62	–	
Maximum Differential Voltage Swing	V_o				V_{p-p}
0 dB AGC		–	20	–	
-30 dB AGC		–	8.0	–	
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	µmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	µmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	µmhos
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	<<1.0	<<1.0	<<1.0	<<1.0	µmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{21} \rvert$ $\angle y_{21}$ $\angle y_{21}$	 160 -5.0 -3.0	 160 -20 -18	 200 -80 -69	 180 -105 -90	 mmhos degrees degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

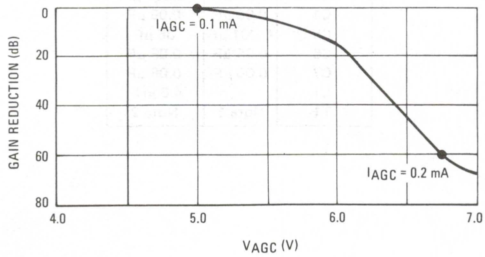
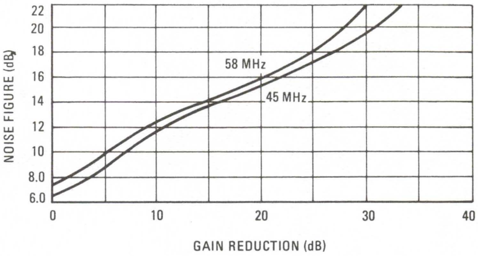


FIGURE 3 – NOISE FIGURE
(Figure 5)



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 – CIRCUIT SCHEMATIC

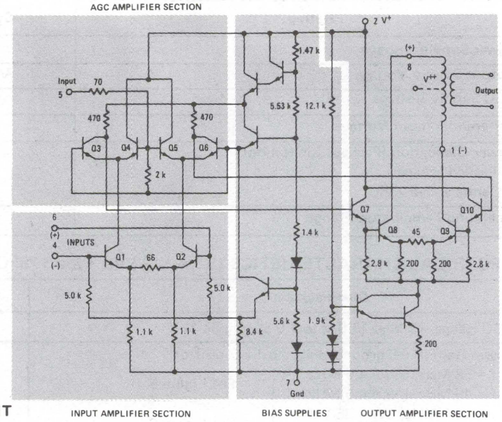
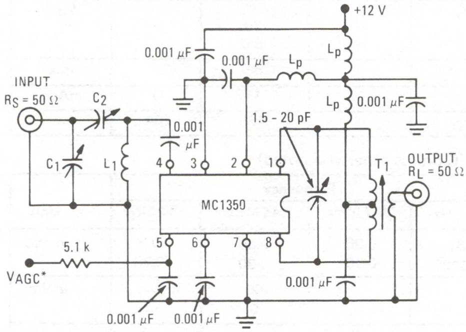

AGC AMPLIFIER SECTION
2 V+
1.47 k
(+)
8
V++
Output
Input
5
70
470
470
5.53 k
12.1 k
Q3
Q4
Q5
Q6
1 (-)
2 k
Q7
Q10
6
(+)
4
(-)
INPUTS
Q1
66
Q2
Q8
45
Q9
1.4 k
2.8 k
200
200
2.8 k
5.0 k
5.0 k
5.6 k
1.9 k
1.1 k
1.1 k
8.4 k
200
7
Gnd
INPUT AMPLIFIER SECTION
BIAS SUPPLIES
OUTPUT AMPLIFIER SECTION

FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)

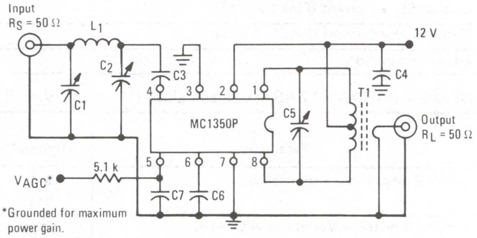

+12 V
0.001 µF
0.001 µF
Lp
Lp
Lp
INPUT
RS = 50 Ω
C2
0.001 µF
1.5 - 20 pF
0.001 µF
C1
L1
4
3
2
1
T1
OUTPUT
RL = 50 Ω
MC1350
5
6
7
8
5.1 k
VAGC*
0.001 µF
0.001 µF
0.001 µF

*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20\ k\Omega$
See Figure 10 for frequency response curve.

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4″ coil form.
@ 58 MHz = 6 Turns on a 1/4″ coil form
T_1 Primary Winding = 18 Turns on a 1/4″ coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2″ Long

	45 MHz		58 MHz	
L_1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T_1	1.3 -3.4 µH	Q ≥ 100 @ 2 µH	1.2 -3.8 µH	Q ≥ 100 @ 2 µH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)


Input
RS = 50 Ω
L1
12 V
C2
C3
C4
C1
4
3
2
1
T1
C5
MC1350P
Output
RL = 50 Ω
5
6
7
8
5.1 k
VAGC*
C7
C6

*Grounded for maximum power gain.

Note 1. Primary: 120 µH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 µH
Primary winding = 24 turns #36 AWG (close-wound on 1/4″ dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4″ dia. (wound over center-tap)

Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 µF	0.001 µF
C4	0.05 µF	0.05 µF
C5	0.001 µF	36 pF
C6	0.05 µF	0.05 µF
C7	0.05 µF	0.05 µF
L1	–	4.6 µH
T1	Note 1	Note 2

TYPICAL CHARACTERISTICS

(V^+ = 12 V, T_A = +25°C)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

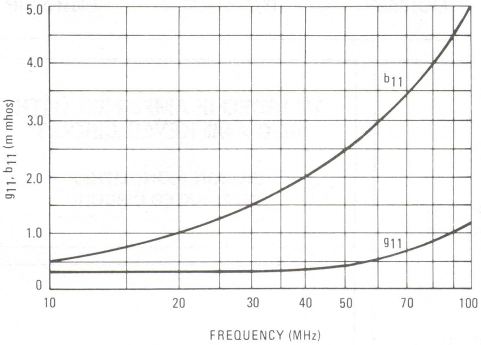


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

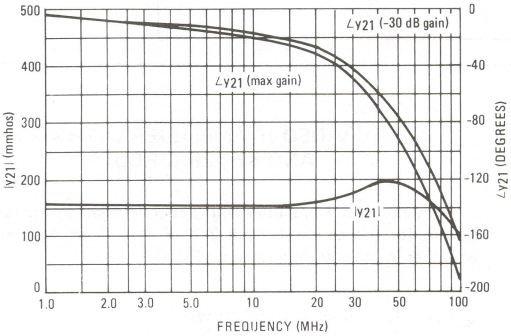


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

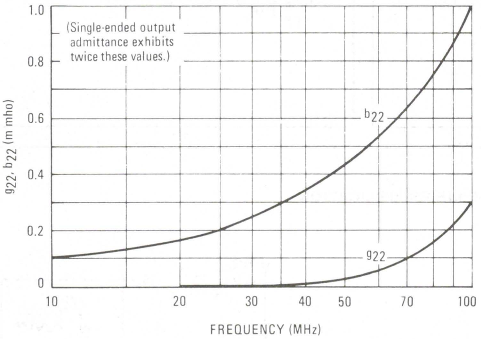


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)

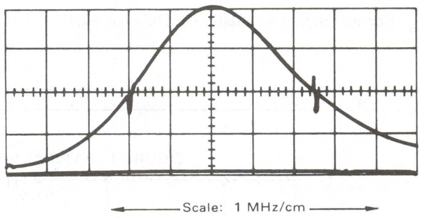
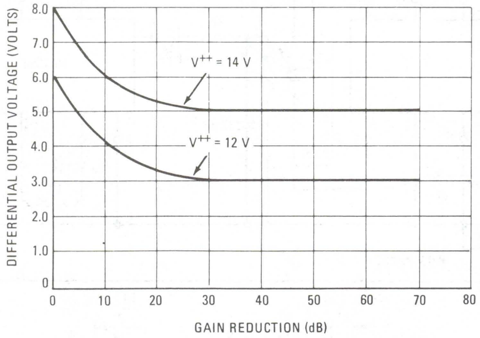


FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

MC1352

ORDERING INFORMATION

Device	Temperature Range	Package
MC1352P	0°C to +70°C	Plastic DIP

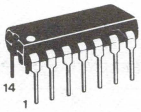
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner

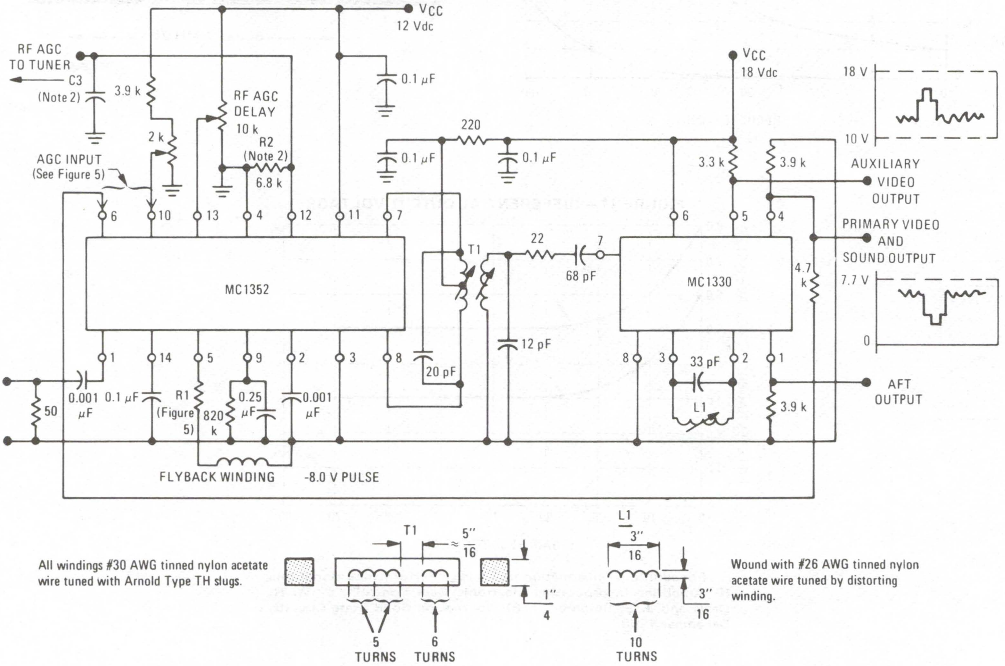
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION


VCC
12 Vdc
RF AGC TO TUNER
C3 (Note 2)
3.9 k
2 k
RF AGC DELAY
10 k
R2 (Note 2)
6.8 k
0.1 μF
220
0.1 μF
0.1 μF
AGC INPUT (See Figure 5)
6
10
13
4
12
11
7
MC1352
1
14
5
9
2
3
8
0.001 μF
0.1 μF
R1 (Figure 5)
820 k
0.25 μF
0.001 μF
50
FLYBACK WINDING
-8.0 V PULSE
T1
20 pF
12 pF
22
68 pF
7
VCC
18 Vdc
3.3 k
3.9 k
6
5
4
MC1330
4.7 k
8
3
33 pF
2
1
L1
3.9 k
18 V
10 V
AUXILIARY VIDEO OUTPUT
PRIMARY VIDEO AND SOUND OUTPUT
7.7 V
0
AFT OUTPUT
T1
5″/16 ≈
1″/4
5 TURNS
6 TURNS
L1
3″/16
3″/16
10 TURNS

All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.

Wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

MAXIMUM RATINGS (Voltages referenced to Pin 4, ground; T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply (Pin 11)	+18	Vdc
Output Supply (Pins 7 and 8)	+18	Vdc
Signal Input Voltage (Pin 1 or 2, other pin ac grounded)	10	V_{p-p}
AGC Input Voltage (Pin 6 or 10, other pin ac grounded)	+6.0	Vdc
Gating Voltage, Pin 5	+10, -20	Vdc
Power Dissipation Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range	–	75	–	dB
Power Gain				dB
f = 35 MHz or 45 MHz	–	52	–	
f = 58 MHz	–	50	–	
Maximum Differential Output Voltage Swing				V_{p-p}
0 dB AGC	–	16.8	–	
-30 dB AGC	–	8.4	–	
Voltage Range for RF-AGC at Pin 12				Vdc
Maximum	–	7.0	–	
Minimum	–	0.2	–	
IF Gain Change Over RF-AGC Range	–	10	–	dB
Output Stage Current ($I_7 + I_8$)	–	5.7	–	mAdc
Total Supply Current ($I_7 + I_8 + I_{11}$)	–	27	35	mAdc
Total Power Dissipation	–	325	370	mW

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted.)

Parameters	Symbol	f = 35 MHz	f = 45 MHz	f = 58 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.55 2.25	0.70 2.80	1.1 3.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	50 0	60 0	– –	µmhos
Differential Output Admittance	g_{22} b_{22}	20 430	40 570	75 780	µmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	3.0 80	4.0 100	– –	µmhos
Reverse Transfer Admittance	$\|y_{12}\|$	≪1.0	≪1.0	≪1.0	µmho
Forward Transfer Admittance					
Magnitude	$\|y_{12}\|$	260	240	210	mmhos
Angle (0 dB AGC)	$\angle y_{21}$	-73	-100	-135	degrees
Angle (-30 dB AGC)	$\angle y_{21}$	-52	-72	-96	
Single-Ended Input Capacitance	-	9.5	10	10.5	pF
Differential Output Capacitance	-	2.0	2.0	2.5	pF

FIGURE 2 – CIRCUIT SCHEMATIC

KEYER AND AGC AMPLIFIER

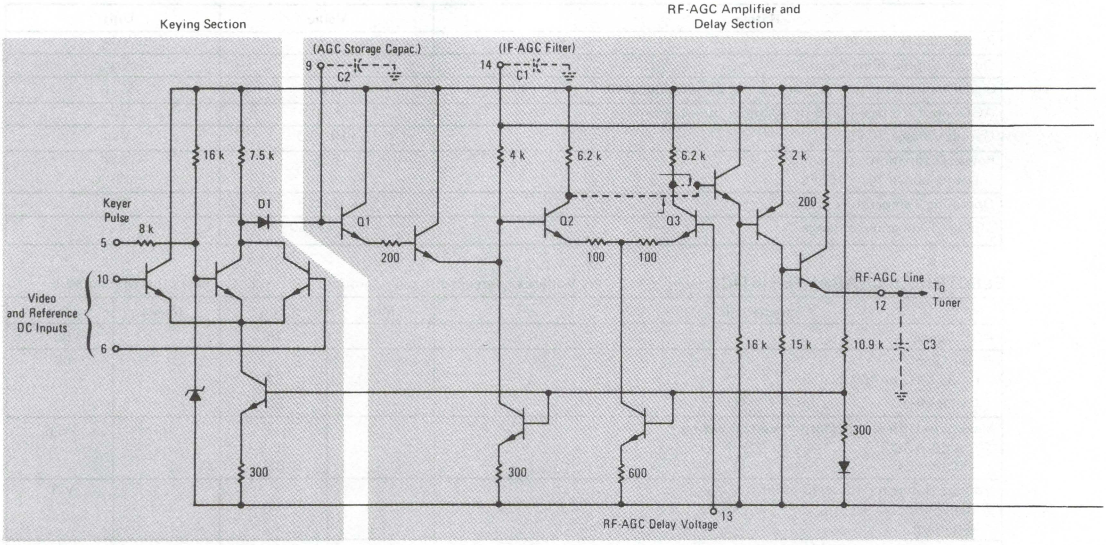
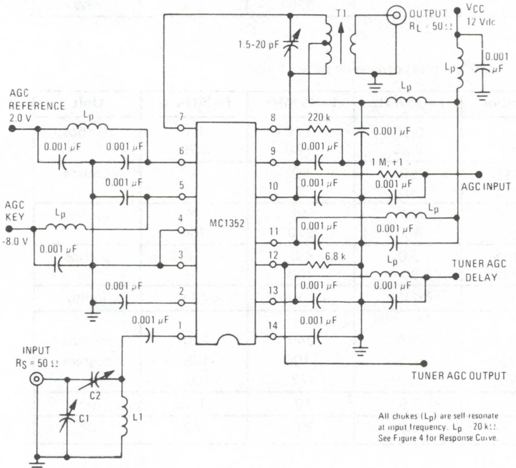

Keying Section
RF-AGC Amplifier and Delay Section
(AGC Storage Capac.)
9
C2
(IF-AGC Filter)
14
C1
16 k
7.5 k
4 k
6.2 k
6.2 k
2 k
200
Keyer Pulse
5
8 k
D1
Q1
Q2
Q3
200
100
100
10
Video and Reference DC Inputs
6
RF-AGC Line
12
To Tuner
16 k
15 k
10.9 k
C3
300
300
300
600
RF-AGC Delay Voltage
13

FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT


T1
OUTPUT
R_L = 50 Ω
V_{CC}
12 Vdc
1.5-20 pF
0.001 µF
Lp
Lp
AGC REFERENCE 2.0 V
Lp
7
8
220 k
0.001 µF
0.001 µF
0.001 µF
6
9
0.001 µF
1 M, +1
0.001 µF
5
10
0.001 µF
0.001 µF
AGC INPUT
AGC KEY
-8.0 V
Lp
4
MC1352
Lp
0.001 µF
3
11
0.001 µF
0.001 µF
12
6.8 k
Lp
TUNER AGC DELAY
0.001 µF
2
13
0.001 µF
0.001 µF
0.001 µF
1
14
0.001 µF
INPUT
R_S = 50 Ω
C2
C1
L1
TUNER AGC OUTPUT

All chokes (L_p) are self-resonate at input frequency. $L_p \geq 20$ kΩ. See Figure 4 for Response Curve.

	35 and 45 MHz		58 MHz	
L1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T1	1.3-3.4 µH	Q ≥ 100 @ 2 µH	1.2-3.8 µH	Q ≥ 100 @ 2 µH
C1	48-100 pF		40-80 pF	
C2	8-60 pF		12-45 pF	

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4" coil form
@ 58 MHz = 6 Turns on a 1/4" coil form
T1 Primary Winding = 18 Turns on a 1/4" coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Arnold TH Material 1/2" long

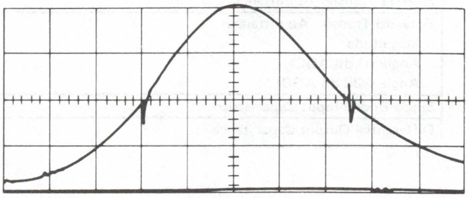
GENERAL OPERATING INFORMATION

The MC1352, consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

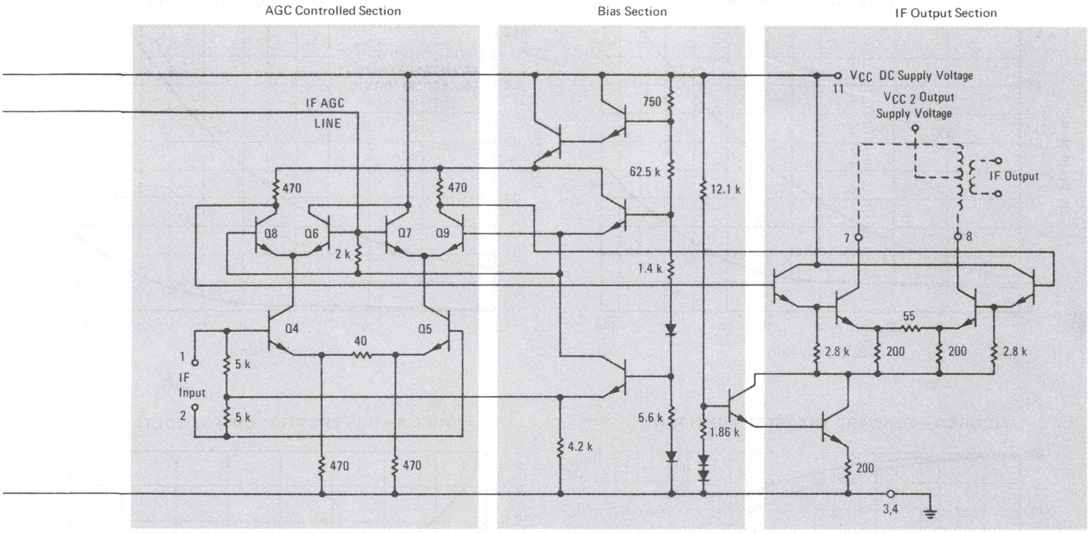
The action of the gating section is such that the proper voltage, V_C,

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

IF AMPLIFIER



is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of Q2 and shift the dc levels causing the RF-AGC voltage to vary.

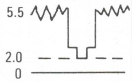
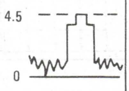
The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

NOTES:

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 μF).
2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 μF, C2 = 0.25 μF, C3 = 10 μF.
3. To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.
4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 R1 (Ω)
Negative-Going Sync.		Adj. 1.0–4.0 Vdc Nom 2.0 V	0
Positive-Going Sync.	Adj. 1.0–8.0 Vdc Nom 4.5 V		3.9 k

TYPICAL CHARACTERISTICS

(V_{CC} = +12 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

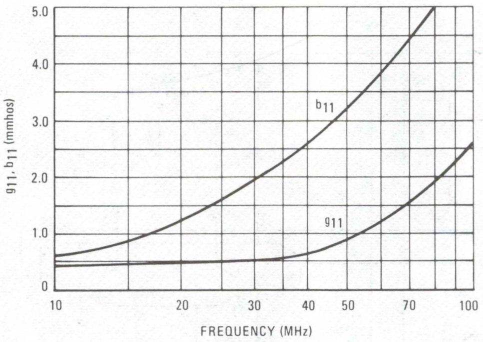


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

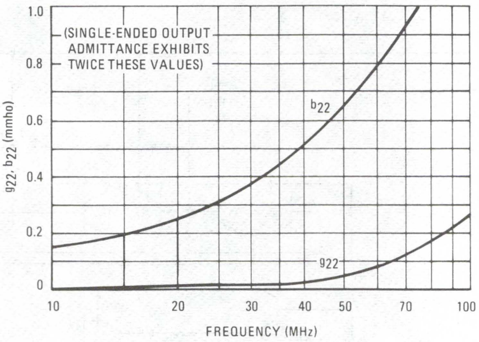


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

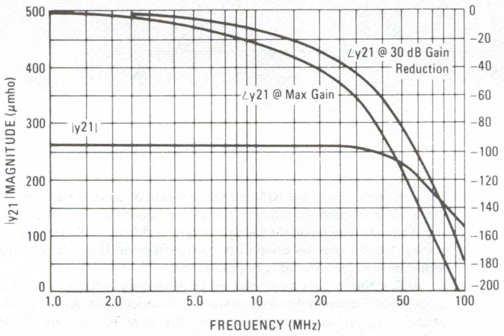


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

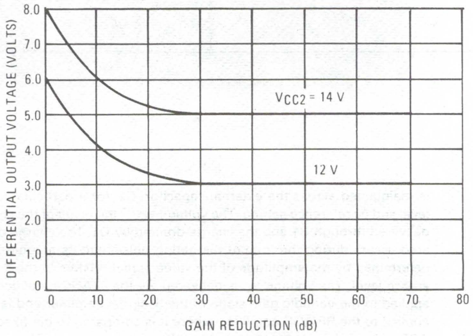


FIGURE 10 – AGC CHARACTERISTICS

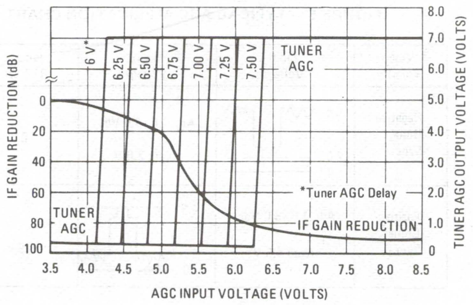
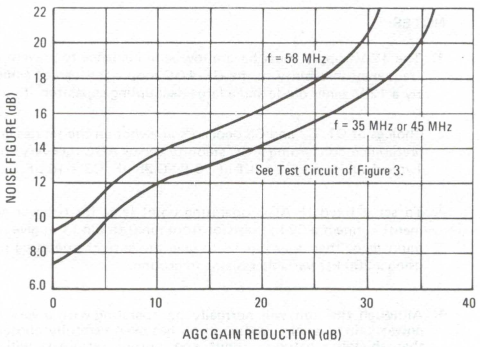


FIGURE 11 – TYPICAL NOISE FIGURE



MC1355

LIMITING FM IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

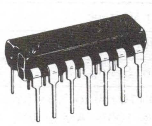
ORDERING INFORMATION

Device	Temperature Range	Package
MC1355P	0°C to +75°C	Plastic DIP

BALANCED FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

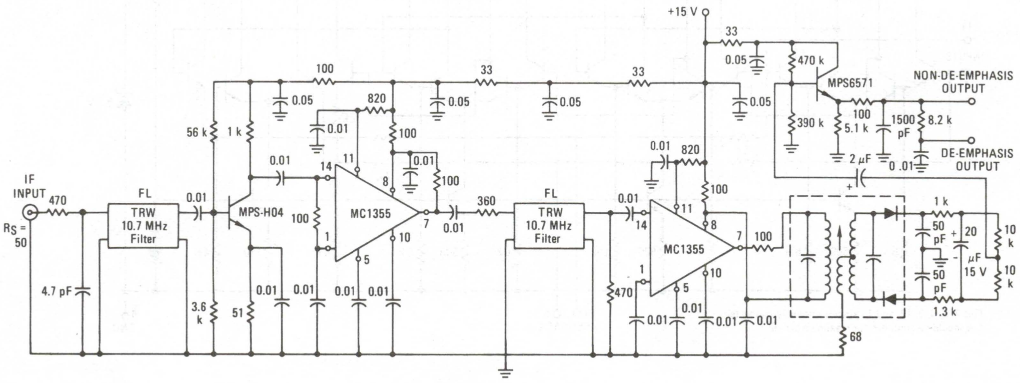
. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – DUAL MC1355 FM IF APPLICATION


+15 V
IF INPUT
Rs = 50
470
4.7 pF
FL
TRW 10.7 MHz Filter
0.01
56 k
1 k
3.6 k
51
MPS-H04
100
0.05
820
33
360
MC1355
14
11
8
7
1
5
10
470 k
390 k
MPS6571
5.1 k
1500 pF
8.2 k
2 μF
0 .01
NON-DE-EMPHASIS OUTPUT
DE-EMPHASIS OUTPUT
1 k
50 pF
20 μF 15 V
10 k
1.3 k
68

*All other pins grounded
T-Ratio Detector (input impedance ≅ 1.5 k) G.1. ≠36231 or equivalent

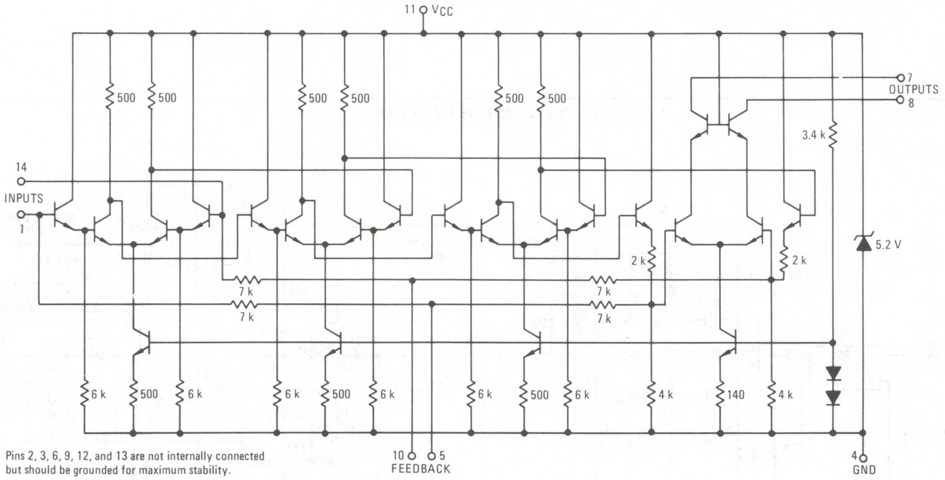
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Output Voltage (Pins 7 & 8)	40	Vdc
Supply Current to Pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, f = 10.7 MHz, T_A = +25°C)

Characteristic		Min	Typ	Max	Units
Power Supply Voltage Range		8.0	15	18	Vdc
Total Circuit Current		–	16	–	mAdc
Total Output Stage Current		–	4.2	–	mA
Device Dissipation		–	125	–	mW
Internal Zener Voltage		–	5.2	–	Vdc
Input Signal for 3 dB Limiting		–	175	250	μV(rms)
Output Current Swing		3.1	4.2	5.4	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)		–	60	–	dB
Admittance Parameters	Y_{11}	–	120 + j320	–	μmhos
	Y_{12}	–	j0.6	–	μmho
	Y_{21}	–	8 + j5.9	–	mhos
	Y_{22}	–	15 + j230	–	μmhos

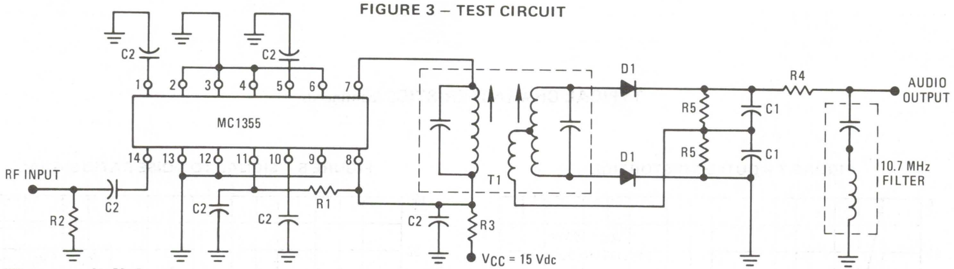
FIGURE 2 – CIRCUIT SCHEMATIC


11 VCC
500
500
500
500
500
500
14
INPUTS
1
7 k
7 k
7 k
7 k
2 k
2 k
3.4 k
5.2 V
7
OUTPUTS
8
6 k
500
6 k
6 k
500
6 k
6 k
500
6 k
4 k
140
4 k
10
5
FEEDBACK
4
GND

Pins 2, 3, 6, 9, 12, and 13 are not internally connected but should be grounded for maximum stability.

TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT


C2
C2
1 2 3 4 5 6 7
MC1355
14 13 12 11 10 9 8
RF INPUT
C2
R2
C2
C2
R1
C2
R3
VCC = 15 Vdc
D1
D1
T1
R5
R5
C1
C1
R4
AUDIO OUTPUT
10.7 MHz FILTER

R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0.01 μF
T1 10.7 MHz Foster-Seeley Discriminator, Primary Impedance = 3.9 k, Peak-to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

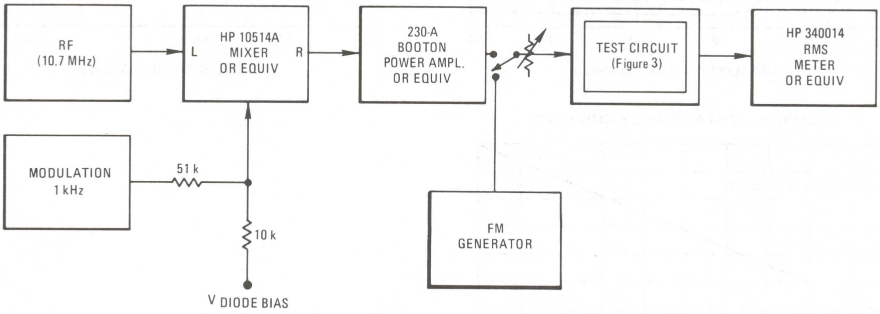

RF (10.7 MHz)
HP 10514A MIXER OR EQUIV
L
R
230-A BOOTON POWER AMPL. OR EQUIV
TEST CIRCUIT (Figure 3)
HP 340014 RMS METER OR EQUIV
MODULATION 1 kHz
51 k
10 k
V DIODE BIAS
FM GENERATOR

FIGURE 5 – LIMITING

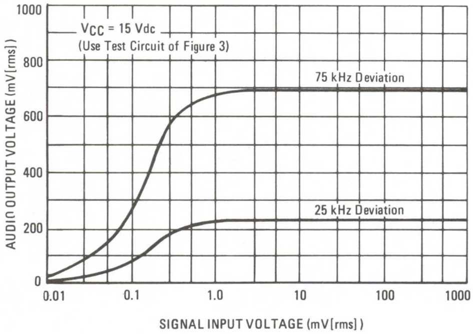
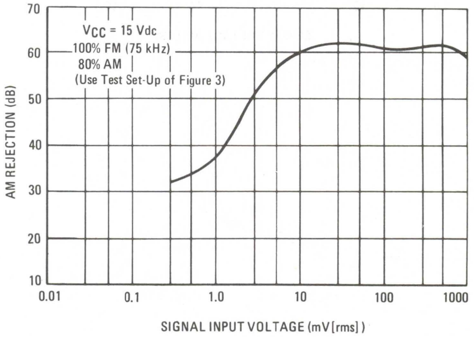


FIGURE 6 – AM REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

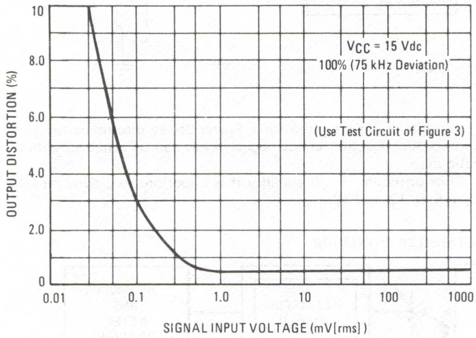


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

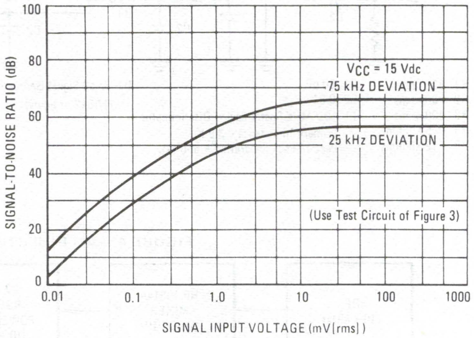
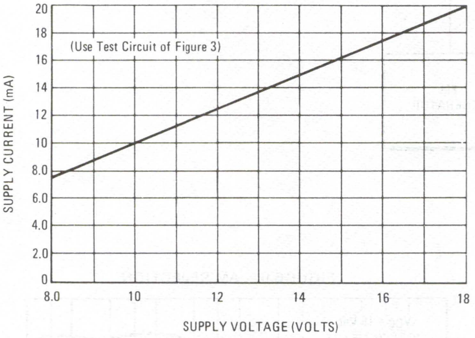


FIGURE 9 – TOTAL SUPPLY CURRENT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1357P	0°C to +75°C	Plastic DIP

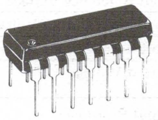
MC1357

IF AMPLIFIER AND QUADRATURE DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

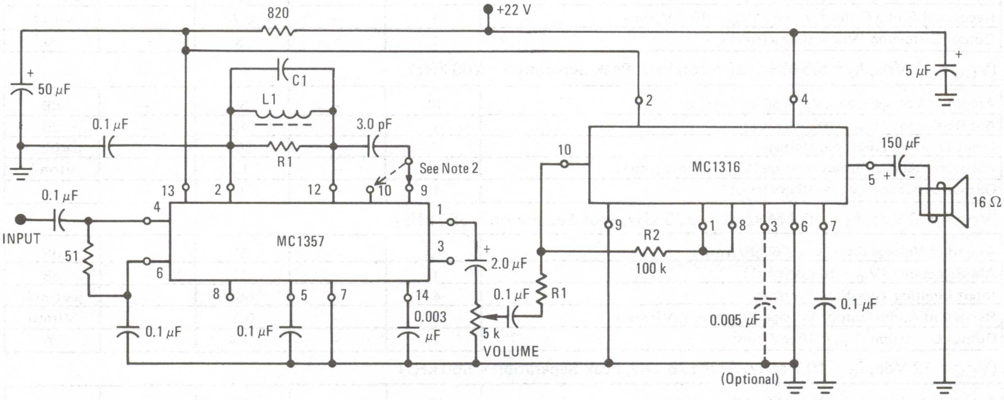
TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at V_{CC} = 8.0 Vdc



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – TV TYPICAL APPLICATION CIRCUIT


820
+22 V
50 µF
C1
L1
0.1 µF
3.0 pF
R1
See Note 2
13
2
12
10
9
4
0.1 µF
INPUT
51
6
MC1357
1
3
8
5
7
14
0.1 µF
0.1 µF
0.003 µF
2.0 µF
0.1 µF
R1
5 k
VOLUME
2
4
10
MC1316
5 µF
150 µF
5
16 Ω
9
1
8
3
6
7
R2
100 k
0.005 µF
0.1 µF
(Optional)

Typical Performance:
2 Watts Output
2% Distortion
250 µV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 µH
R1 = 20 kΩ
Q = 30

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V_p
Power Dissipation (Package Limitation) Plastic Packages Derate above $T_A = +25^{\circ}C$	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, $T_A = +25^{\circ}C$ unless otherwise noted.)

Characteristic		Pin	Min	Typ	Max	Units
Drain Current	V_{CC} = 8 V V_{CC} = 12 V	13	10 –	12 15	19 21	mA
Amplifier Input Reference Voltage		6	–	1.45	–	Vdc
Detector Input Reference Voltage		2	–	3.65	–	Vdc
Amplifier High Level Output Voltage		10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage		9	–	0.145	0.2	Vdc
Detector Output Voltage	V_{CC} = 8 V V_{CC} = 12 V	1	– –	3.7 5.4	– –	Vdc
Amplifier Input Resistance		4	–	5.0	–	kΩ
Amplifier Input Capacitance		4	–	11	–	pF
Detector Input Resistance		12	–	70	–	kΩ
Detector Input Capacitance		12	–	2.7	–	pF
Amplifier Output Resistance		10	–	60	–	ohms
Detector Output Resistance		1	–	200	–	ohms
De-Emphasis Resistance		14	–	8.8	–	kΩ

DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, $T_A = +25^{\circ}C$ for all tests.)

(V_{CC} = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	36	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.72	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	3	–	%

(V_{CC} = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	40	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	1.2	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	5	–	%

(V_{CC} = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	37	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.30	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

(V_{CC} = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	45	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.48	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

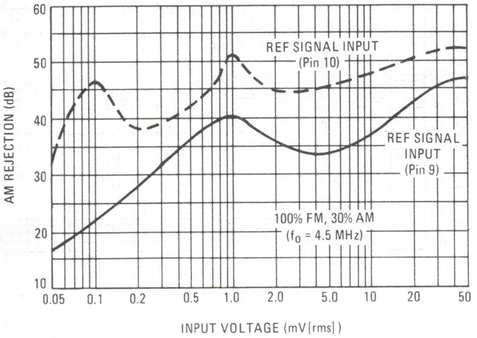
*100% FM, 30% AM Modulation

TYPICAL CHARACTERISTICS

(V_{CC} = 12 V, T_A = +25°C unless otherwise noted)
(Use Test Circuit of Figure 13)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

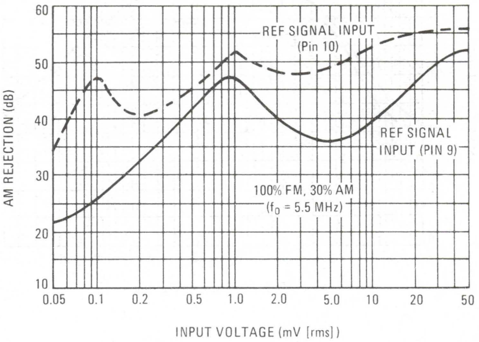


FIGURE 4 – DETECTED AUDIO OUTPUT

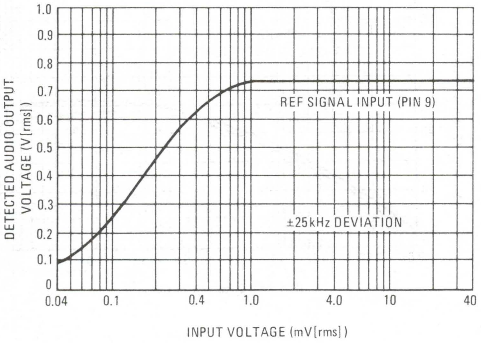


FIGURE 5 – DETECTED AUDIO OUTPUT

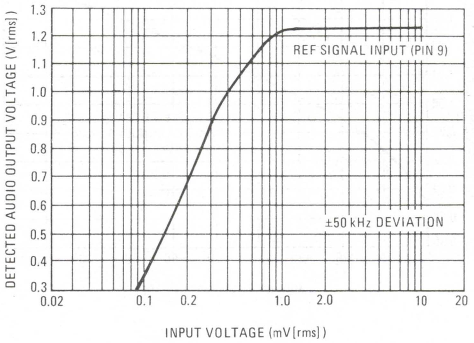


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

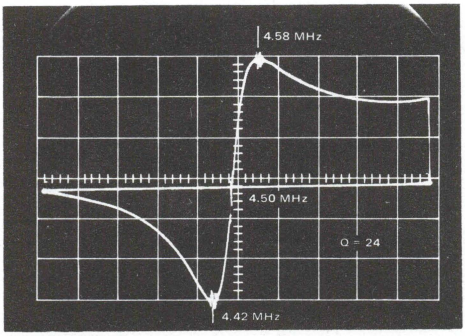
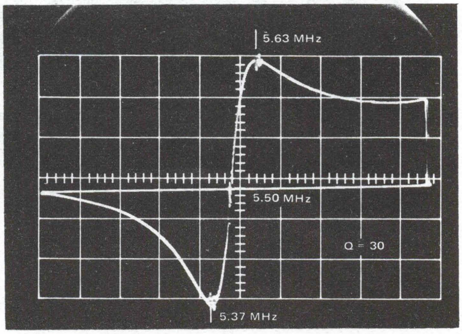


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



TYPICAL CHARACTERISTICS (continued)
(f_o = 10.7 MHz, T_A = +25°C unless otherwise noted.)
(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

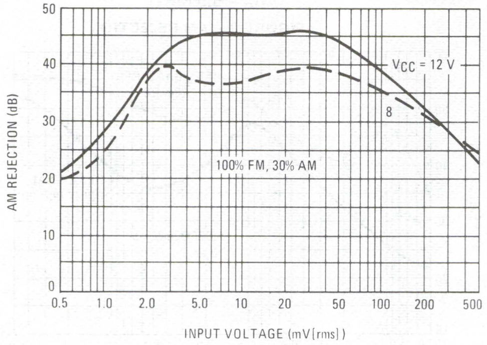


FIGURE 9 – AFC VOLTAGE DRIFT
(1.0 mV INPUT CARRIER @ 10.7 MHz)

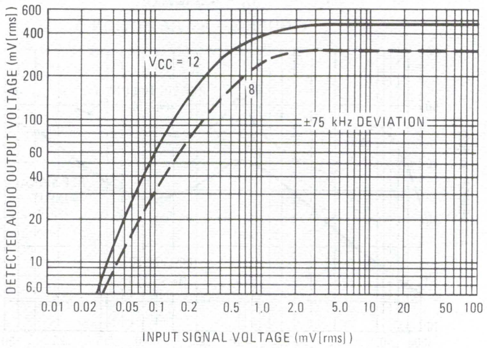


FIGURE 10 – LIMITING

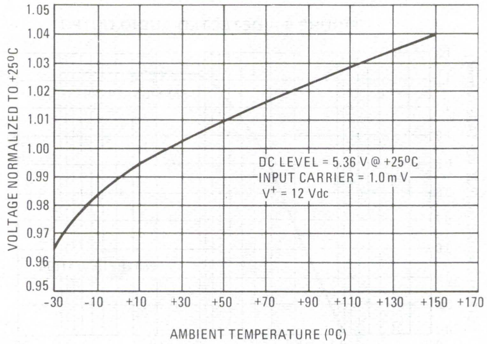


FIGURE 11 – SIGNAL-TO-NOISE RATIO

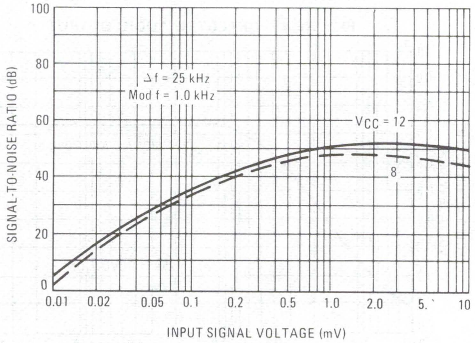


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

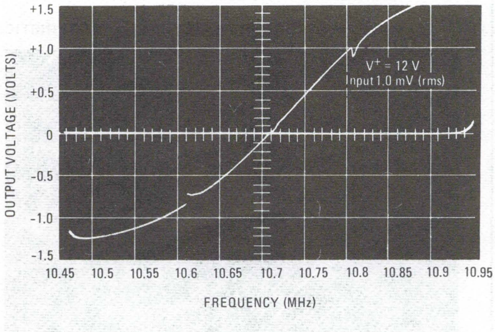
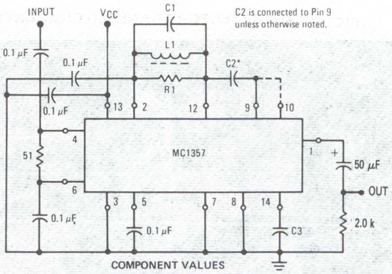


FIGURE 13 – TEST CIRCUIT

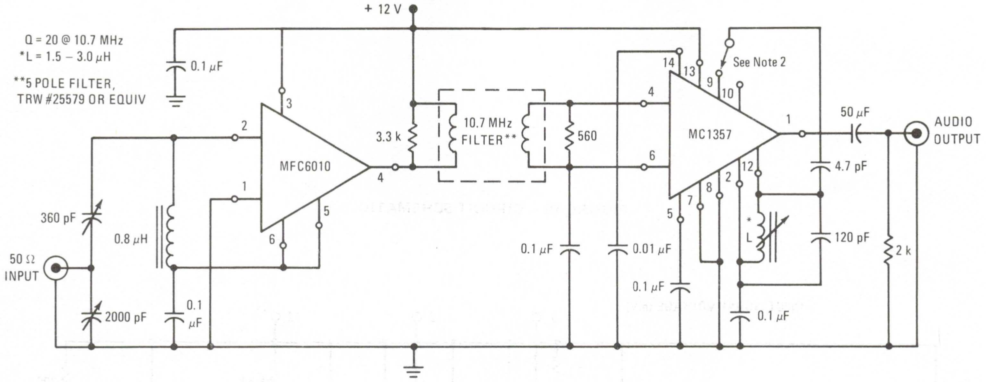

INPUT
VCC
C1
L1
R1
C2*
0.1 μF
0.1 μF
0.1 μF
0.1 μF
0.1 μF
51
MC1357
13
2
12
9
10
4
6
1
3
5
7
8
14
C3
+
50 μF
OUT
2.0 k

C2 is connected to Pin 9 unless otherwise noted.

COMPONENT VALUES

f	L1	C1	R1	Q(R1, L1)	C2	C3
MHz	μH	pF	kΩ		pF	μF
4.5	14	120	20	30	3.0	0.003
5.5	8.0	100	20	30	3.0	0.003
10.7	2.0	120	3.9	20	4.7	0.01

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT


+ 12 V
Q = 20 @ 10.7 MHz
*L = 1.5 – 3.0 μH
**5 POLE FILTER,
TRW #25579 OR EQUIV
0.1 μF
360 pF
0.8 μH
50 Ω
INPUT
2000 pF
0.1
μF
MFC6010
1
2
3
4
5
6
3.3 k
10.7 MHz
FILTER**
560
0.1 μF
0.01 μF
0.1 μF
MC1357
14
13
9
10
See Note 2
4
6
1
12
2
8
7
5
*
L
0.1 μF
50 μF
4.7 pF
120 pF
2 k
AUDIO
OUTPUT

Note 1:

Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:

Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 15 – OUTPUT DISTORTION

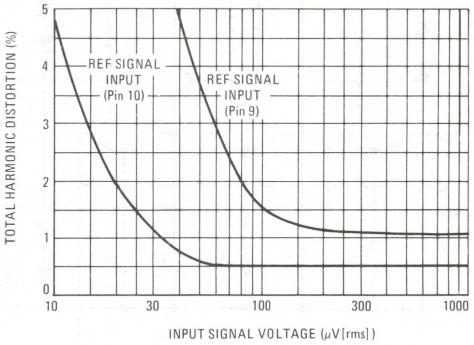


FIGURE 16 – SIGNAL-TO-NOISE RATIO

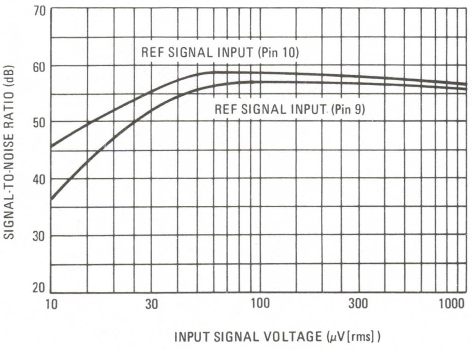


FIGURE 17 – RECOVERED AUDIO OUTPUT

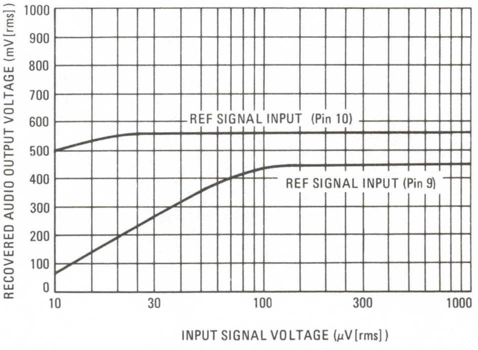
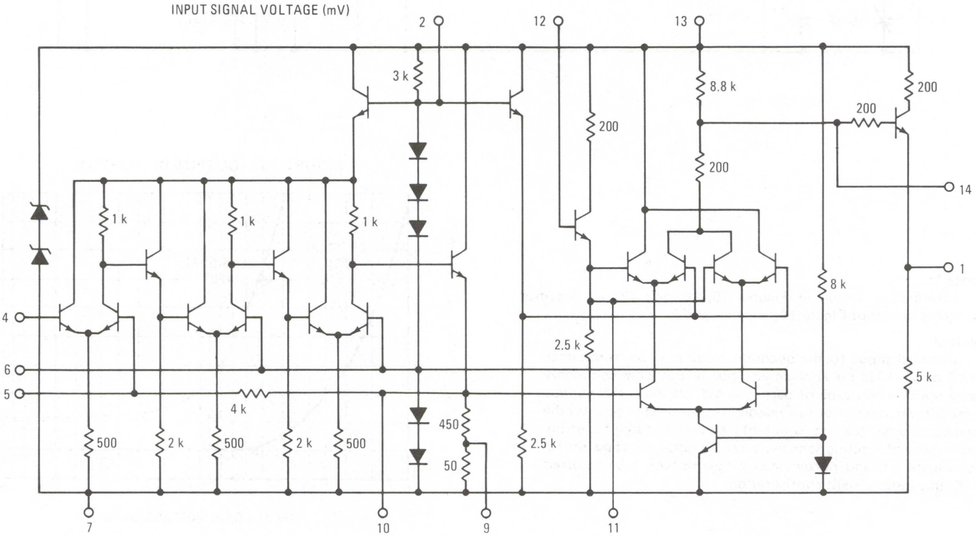


FIGURE 18 — CIRCUIT SCHEMATIC


INPUT SIGNAL VOLTAGE (mV)
2
12
13
3 k
8.8 k
200
200
200
200
14
1 k
1 k
1 k
1
8 k
4
2.5 k
6
5
5 k
4 k
450
500
2 k
500
2 k
500
2.5 k
50
7
10
9
11

MC1358

IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

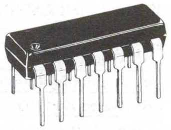
ORDERING INFORMATION

Device	Temperature Range	Package
MC1358P	−20°C to +75°C	Plastic DIP

TV SOUND IF AMPLIFIER

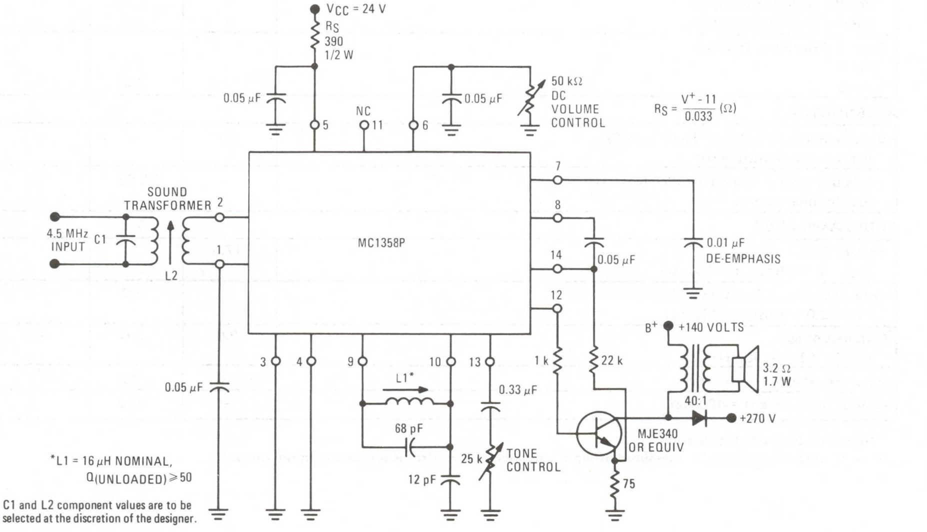
. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control – Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability – 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



V_{CC} = 24 V
R_S
390
1/2 W
0.05 μF
5
NC
11
6
0.05 μF
50 kΩ
DC
VOLUME
CONTROL
$R_S = \frac{V^+ - 11}{0.033}$ (Ω)
7
8
14
12
SOUND
TRANSFORMER
2
1
4.5 MHz
INPUT
C1
L2
MC1358P
0.05 μF
0.01 μF
DE-EMPHASIS
B+
+140 VOLTS
3
4
9
10
13
L1*
0.33 μF
1 k
22 k
3.2 Ω
1.7 W
40:1
+270 V
68 pF
25 k
TONE
CONTROL
MJE340
OR EQUIV
12 pF
75
0.05 μF

*L1 = 16 μH NOMINAL,
$Q_{(UNLOADED)} \geq 50$

C1 and L2 component values are to be selected at the discretion of the designer.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0.5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0.91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between Pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between Pin 9 and Gnd) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 – –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

(V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 — AM REJECTION

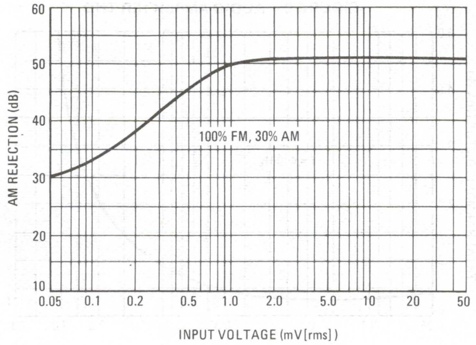


FIGURE 4 — DETECTED AUDIO OUTPUT

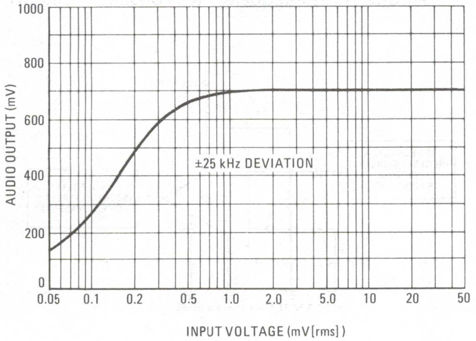
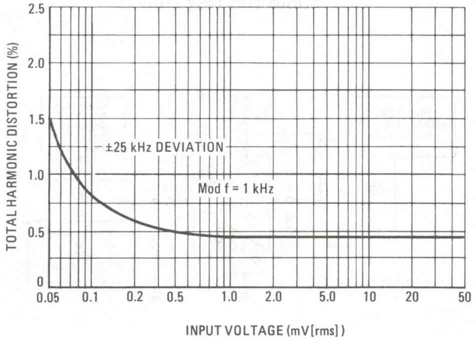


FIGURE 6 — IF AMPLIFIER AND DETECTOR THD



(f_o = 5.5 MHz)

FIGURE 3 — AM REJECTION

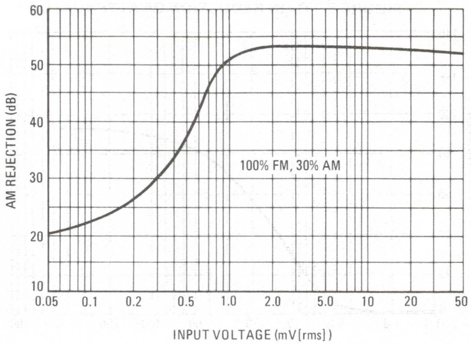


FIGURE 5 — DETECTED AUDIO OUTPUT

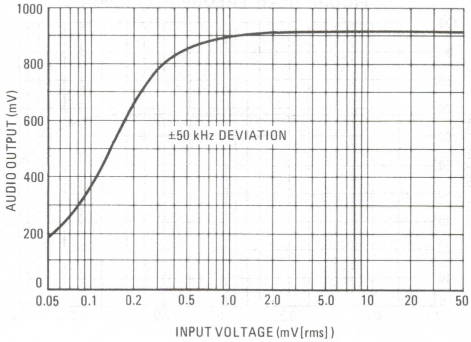
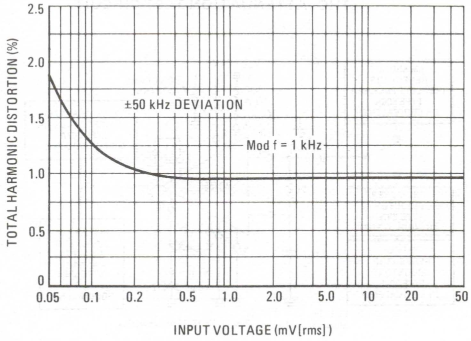


FIGURE 7 — IF AMPLIFIER AND DETECTOR THD



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — GAIN REDUCTION OF ATTENUATOR

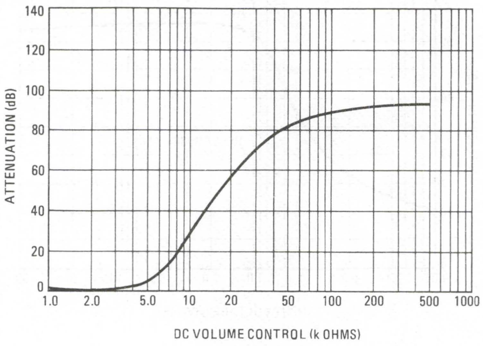


FIGURE 9 — AUDIO AMPLIFIER THD

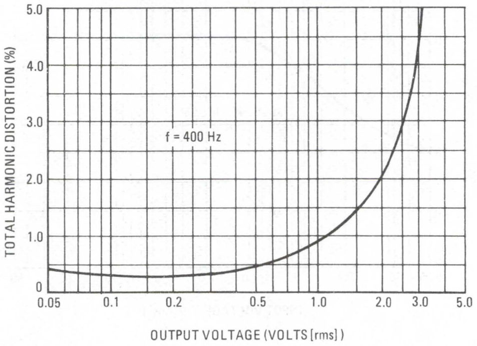


FIGURE 10 — IF FREQUENCY RESPONSE

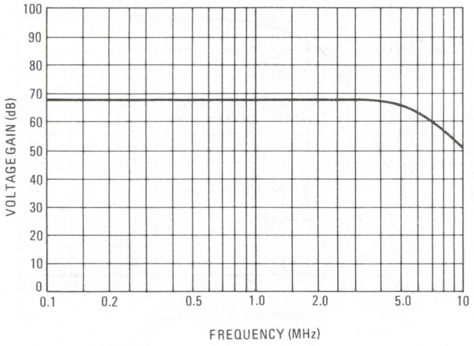


FIGURE 11 — IF FREQUENCY RESPONSE TEST CIRCUIT

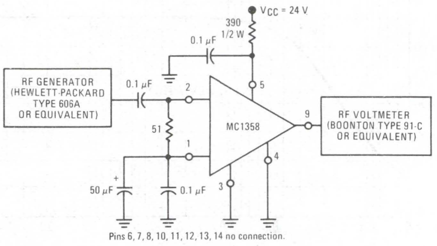

VCC = 24 V
390
1/2 W
0.1 μF
RF GENERATOR
(HEWLETT-PACKARD
TYPE 606A
OR EQUIVALENT)
0.1 μF
2
5
51
MC1358
9
RF VOLTMETER
(BOONTON TYPE 91-C
OR EQUIVALENT)
1
4
50 μF
0.1 μF
3
Pins 6, 7, 8, 10, 11, 12, 13, 14 no connection.

FIGURE 12 — AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

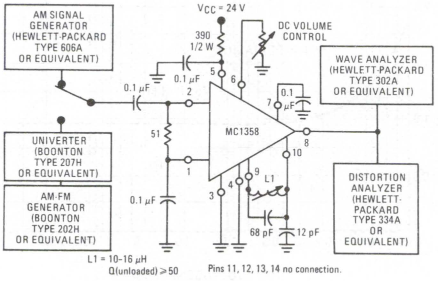

AM SIGNAL
GENERATOR
(HEWLETT-PACKARD
TYPE 606A
OR EQUIVALENT)
VCC = 24 V
390
1/2 W
DC VOLUME
CONTROL
0.1 μF
5
6
WAVE ANALYZER
(HEWLETT-PACKARD
TYPE 302A
OR EQUIVALENT)
0.1 μF
2
0.1
μF
7
UNIVERTER
(BOONTON
TYPE 207H
OR EQUIVALENT)
51
MC1358
8
10
1
9
L1
4
3
0.1 μF
AM-FM
GENERATOR
(BOONTON
TYPE 202H
OR EQUIVALENT)
68 pF
12 pF
DISTORTION
ANALYZER
(HEWLETT-
PACKARD
TYPE 334A
OR
EQUIVALENT)
L1 = 10-16 μH
Q(unloaded) ≥ 50
Pins 11, 12, 13, 14 no connection.

FIGURE 13 — AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

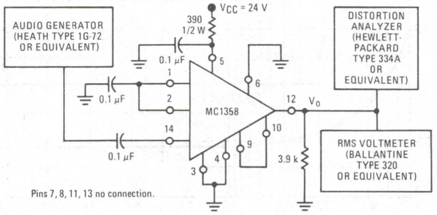
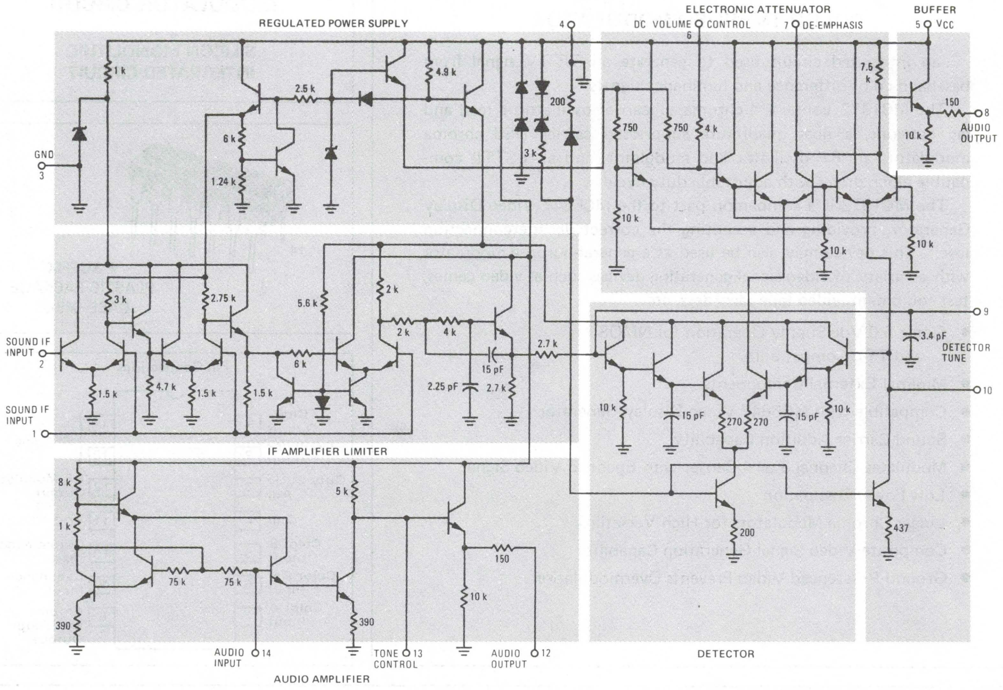

AUDIO GENERATOR
(HEATH TYPE 1G-72
OR EQUIVALENT)
VCC = 24 V
390
1/2 W
DISTORTION
ANALYZER
(HEWLETT-
PACKARD
TYPE 334A
OR
EQUIVALENT)
0.1 μF
5
1
6
0.1 μF
2
MC1358
12
Vo
14
10
0.1 μF
9
4
3.9 k
3
RMS VOLTMETER
(BALLANTINE
TYPE 320
OR EQUIVALENT)
Pins 7, 8, 11, 13 no connection.

FIGURE 14 — CIRCUIT SCHEMATIC


REGULATED POWER SUPPLY
ELECTRONIC ATTENUATOR
BUFFER
4
DC VOLUME CONTROL
6
7 DE-EMPHASIS
5 VCC
1 k
2.5 k
4.9 k
200
7.5 k
150
8
AUDIO OUTPUT
10 k
GND
3
6 k
1.24 k
3 k
750
750
4 k
10 k
10 k
10 k
3 k
2.75 k
5.6 k
2 k
2 k
4 k
SOUND IF INPUT
2
1.5 k
4.7 k
1.5 k
1.5 k
6 k
15 pF
2.7 k
2.25 pF
2.7 k
9
3.4 pF
DETECTOR TUNE
10
10 k
15 pF
270
270
15 pF
10 k
SOUND IF INPUT
1
IF AMPLIFIER LIMITER
8 k
1 k
5 k
75 k
75 k
390
390
150
10 k
200
437
AUDIO INPUT
14
TONE CONTROL
13
AUDIO OUTPUT
12
DETECTOR
AUDIO AMPLIFIER

MC1372

MOTOROLA

COLOR TV VIDEO MODULATOR

. . . an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

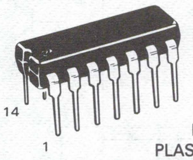
The MC1372 contains a chroma subcarrier oscillator, a lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and an LSTTL compatible clock driver with adjustable duty cycle.

The MC1372 is a companion part to the MC6847 Video Display Generator, providing and accepting the correct dc interconnection levels. This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Compatible with MC6847 Video Display Generator
- Sound Carrier Addition Capability
- Modulates Channel 3 or 4 Carrier with Encoded Video Signal
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation

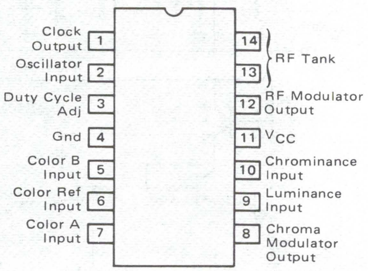
COLOR TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



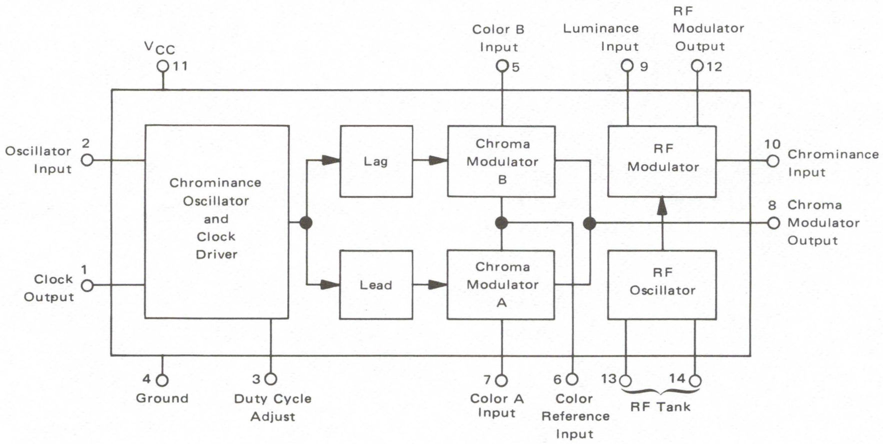
P SUFFIX
PLASTIC PACKAGE
CASE 646-05

Pin Connections


Clock Output 1
Oscillator Input 2
Duty Cycle Adj 3
Gnd 4
Color B Input 5
Color Ref Input 6
Color A Input 7
14
13
RF Tank
12 RF Modulator Output
11 VCC
10 Chrominance Input
9 Luminance Input
8 Chroma Modulator Output

10

FIGURE 1 – BLOCK DIAGRAM


VCC 11
Color B Input 5
Luminance Input 9
RF Modulator Output 12
Oscillator Input 2
Clock Output 1
Chrominance Oscillator and Clock Driver
Lag
Lead
Chroma Modulator B
Chroma Modulator A
RF Modulator
RF Oscillator
10 Chrominance Input
8 Chroma Modulator Output
4 Ground
3 Duty Cycle Adjust
7 Color A Input
6 Color Reference Input
13
14
RF Tank

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 13	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc
Color Reference Voltage	1.5	Vdc
Color A, B Input Voltage Range	1.0 to 2.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	—	25	—	mA
CHROMA OSCILLATOR/CLOCK DRIVER (Measured at Pin 1 unless otherwise noted)				
Output Voltage (V_{OL})	—	—	0.4	Vdc
(V_{OH})	2.4	—	—	
Rise Time (V1 = 0.4 to 2.4 Vdc)	—	—	50	ns
Fall Time (V1 = 2.4 to 0.4 Vdc)	—	—	50	ns
Duty Cycle Adjustment Range (V3 = 5.0 Vdc) (Measured at V1 = 1.4 V)	70	—	30	%
Inherent Duty Cycle (No connection to Pin 3)	—	50	—	%
CHROMA MODULATOR (V5 = V6 = V7 = 1.5 Vdc unless otherwise noted)				
Input Common Mode Voltage Range (Pins 5, 6, 7)	0.8	—	2.3	Vdc
Oscillator Feedthrough (Measured at Pin 8)	—	15	31	mV(p-p)
Modulation Angle [θ8(V7 = 2.0 Vdc) − θ8(V5 = 2.0 Vdc)]	85	100	115	degrees
Conversion Gain [V8/(V7 − V6); V8/(V5 − V6)]	—	0.6	—	V(p-p)/Vdc
Input Current (Pins 5, 6, 7)	—	—	−20	μA
Input Resistance (Pins 5, 6, 7)	100	—	—	kΩ
Input Capacitance (Pins 5, 6, 7)	—	—	5.0	pF
Chroma Modulator Linearity (V5 = 1.0 to 2.0 V; V7 = 1.0 to 2.0 V)	—	4.0	—	%
RF MODULATOR				
Luma Input Dynamic Range (Pin 9, Test Circuit 2)	0	—	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V9 = 1.0 V)	—	15	—	mVrms
Luma Conversion Gain (ΔV12/ΔV9; V9 = 0.1 to 1.0 Vdc) Test Circuit 2	—	0.8	—	V/V
Chroma Conversion Gain (ΔV12/ΔV10; V10 = 1.5 Vp-p; V9 = 1.0 Vdc) Test Circuit 2	—	0.95	—	V/V
Chroma Linearity (Pin 12, V10 = 1.5 Vp-p) Test Circuit 2	—	1.0	—	%
Luma Linearity (Pin 12, V9 = 0 to 1.5 Vdc) Test Circuit 2	—	2.0	—	%
Input Current (Pin 9)	—	—	−20	μA
Input Resistance (Pin 10)	—	800	—	Ω
Input Resistance (Pin 9)	100	—	—	kΩ
Input Capacitance (Pins 9, 10)	—	—	5.0	pF
Residual 920 kHz (Measured at Pin 12) See Note 1	—	50	—	dB
Output Current (Pin 12, V9 = 0 V) Test Circuit 2	—	1.0	—	mA
TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)				
Chroma Oscillator Deviation (f_o = 3.579545 MHz)	—	±50	—	Hz
RF Oscillator Deviation (f_o = 67.25 MHz)	—	±250	—	kHz
Clock Drive Duty Cycle Stability	±5.0	—	—	%

NOTE 1. V9 = 1.0 Vdc, V_C = 300 mV(p-p) @ 3.58 MHz,
V_S = 250 mV(p-p) @ 4.5 MHz, Source Impedance = 75 Ω.

FIGURE 2 — TEST CIRCUIT 1

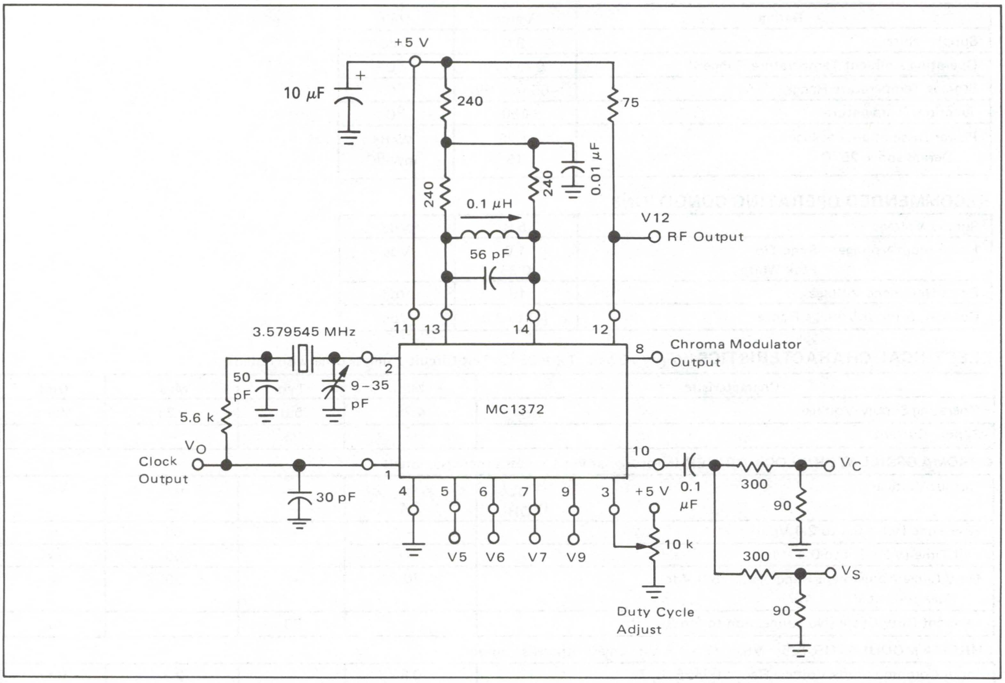

+5 V
10 μF
+
240
75
240
240
0.01 μF
0.1 μH
56 pF
V12
RF Output
11
13
14
12
3.579545 MHz
2
8
Chroma Modulator Output
50 pF
9–35 pF
5.6 k
MC1372
VO
Clock Output
1
10
30 pF
4
5
6
7
9
3
+5 V
0.1 μF
300
VC
90
10 k
V5
V6
V7
V9
300
VS
90
Duty Cycle Adjust

FIGURE 3 — TEST CIRCUIT 2

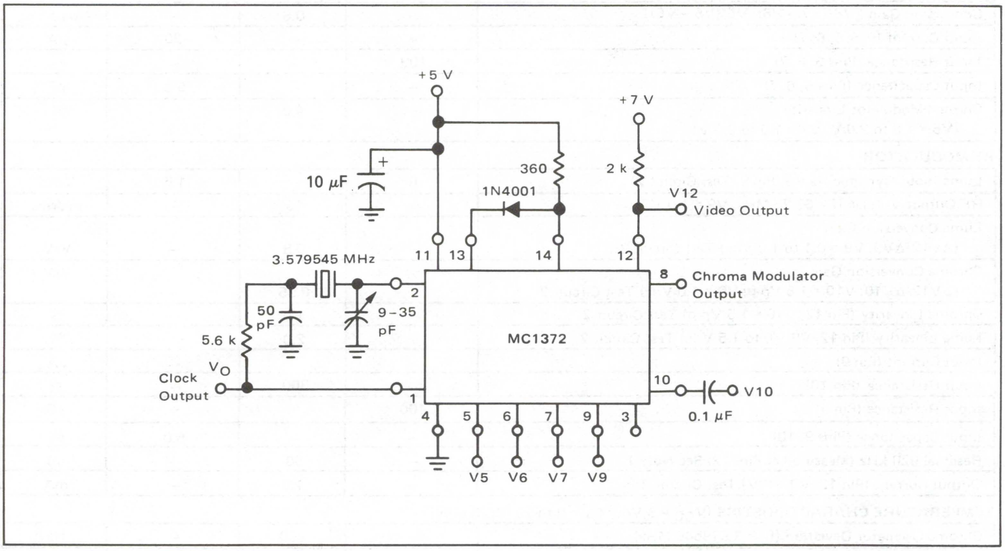
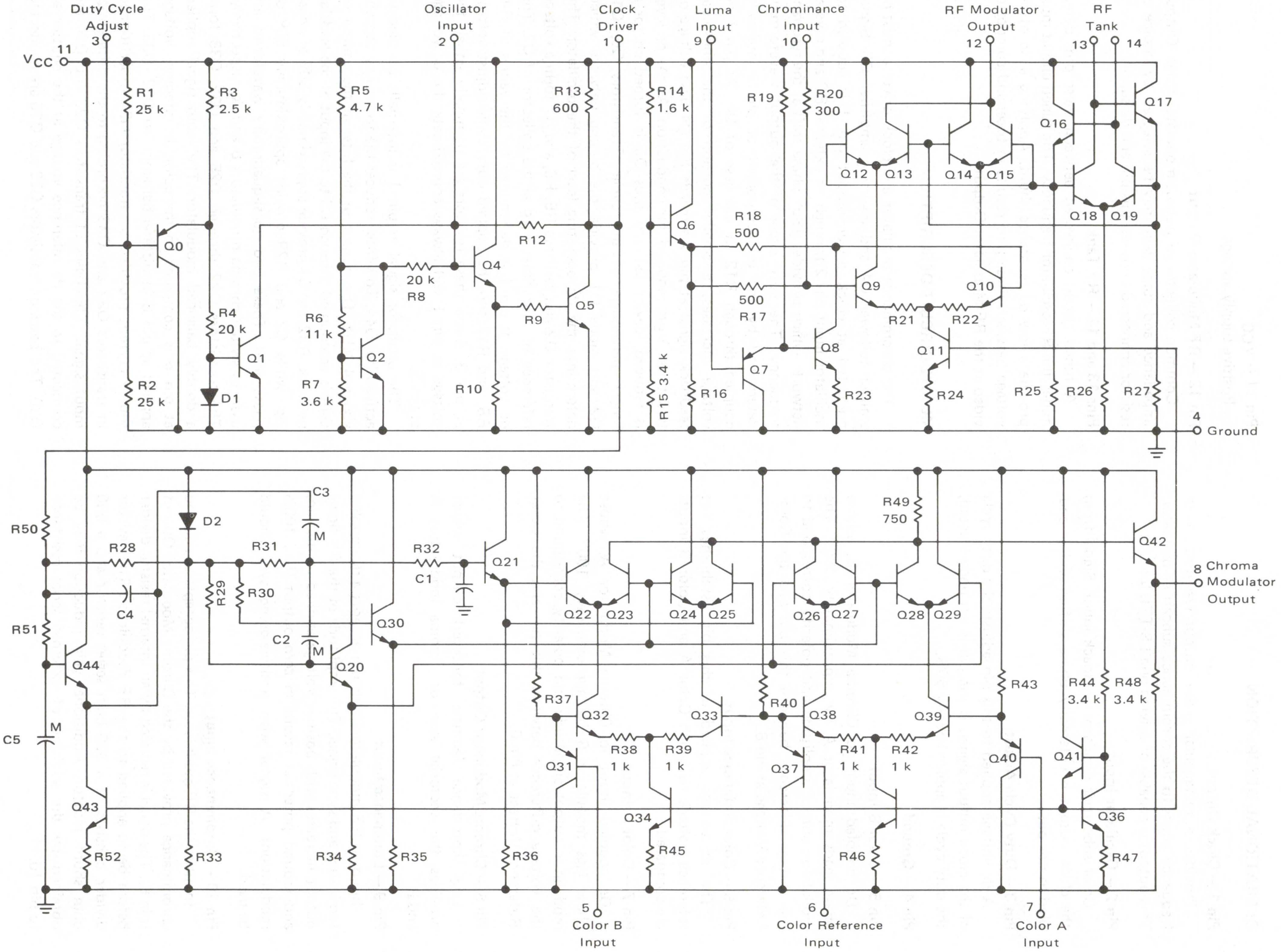

+5 V
+7 V
10 μF
+
360
2 k
1N4001
V12
Video Output
3.579545 MHz
11
13
14
12
8
Chroma Modulator Output
2
50 pF
9–35 pF
5.6 k
MC1372
VO
Clock Output
1
10
V10
0.1 μF
4
5
6
7
9
3
V5
V6
V7
V9

FIGURE 4 – SCHEMATIC DIAGRAM


Duty Cycle Adjust 3
Oscillator Input 2
Clock Driver 1
Luma Input 9
Chrominance Input 10
RF Modulator Output 12
RF Tank 13 14
VCC 11
R1 25 k
R3 2.5 k
R5 4.7 k
R13 600
R14 1.6 k
R19
R20 300
Q0
Q1
Q2
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
R12
R18 500
R8 20 k
R9
R17 500
R21
R22
R4 20 k
R6 11 k
R7 3.6 k
R2 25 k
D1
R10
R15 3.4 k
R16
R23
R24
R25
R26
R27
4 Ground
R50
R28
R31
R32
C1
C3 M
D2
C4
R29
R30
Q21
Q30
C2 M
Q20
R51
Q44
C5 M
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
R49 750
Q42
8 Chroma Modulator Output
R37
Q32
Q33
R40
Q38
Q39
R43
R44 3.4 k
R48 3.4 k
R38 1 k
R39 1 k
R41 1 k
R42 1 k
Q31
Q37
Q40
Q41
Q34
Q36
Q43
R52
R33
R34
R35
R36
R45
R46
R47
5 Color B Input
6 Color Reference Input
7 Color A Input

OPERATIONAL DESCRIPTION

Pin 1 – Clock Output

Provides a rectangular pulse output waveform with frequency equal to the chrominance subcarrier oscillator. This output is capable of driving one LS-TTL load.

Pin 2 – Oscillator Input

Color subcarrier oscillator feedback input. Signal from the clock output is externally phase shifted and ac coupled to this pin.

Pin 3 – Duty Cycle Adjust

A dc voltage applied to this pin adjusts the duty cycle of the clock output signal. If the pin is left unconnected, the duty cycle is approximately 50%.

Pin 4 – Ground

Pin 5 – Color B Input

Dc coupled input to Chroma Modulator B, whose phase leads modulator A by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 6 – Color Reference Input

The dc voltage applied to this pin establishes the reference voltage to which Color A and Color B inputs are compared.

Pin 7 – Color A Input

Dc coupled input to Chroma Modulator A, whose phase lags modulator B by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 8 – Chroma Modulator Output

Low impedance (emitter follower) output which provides the vectorial sum of chroma modulators A and B.

Pin 9 – Luminance Input

Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 10 – Chrominance Input

Input to the RF modulator. This pin accepts ac coupled chrominance provided by the Chroma Modulator Output (pin 8). The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. Additional gain reduction may be obtained by the addition of external series resistance to pin 10.

Pin 11 – V_{CC}

Positive supply voltage

Pin 12 – RF Modulator Output

Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pins 13 and 14 – RF Tank

A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

MC1372 CIRCUIT DESCRIPTION

The chrominance oscillator and clock driver consist of emitter follower Q4 and inverting amplifier Q5. Signal presented at clock driver output pin 1 is coupled to oscillator input pin 2 through an external RC and crystal network, which provides 180° phase shift at the resonant frequency. The duty cycle of the output waveform is determined by the dc component at pin 1 internally coupled through R12 to the base of Q4. As pin 1 dc voltage increases, a smaller portion of the sinusoidal feedback signal at pin 2 exceeds the Q4 base voltage of two times V_{BE} required for conduction. As the dc level is reduced, device Q4 and thus Q5 is turned on for a longer percentage of the cycle. Transistors Q0, Q1, Q2 and diode D1 provide the biasing network which determines the dc operating level of the oscillator. The transistor Q2 and resistors R5, R6, and R7 form a voltage reference of four times V_{BE} at the collector of Q2. The dc voltage at pin 1 is determined by the values of R4, R8, and R12 and the applied duty cycle adjust voltage at pin 3. Since these resistors are nominally equal, the voltage at pin 1 will always approximate the dc voltage at pin 3.

The oscillator signal at pin 1 is internally coupled to active filter Q44. This filter reduces the frequency content above 4 MHz. The output of the filter at the emitter of Q44 is ac coupled through C3 to the input of the lead/lag network. R32 and C1 provide approximately 50° of phase lag, while C2 and R29 provide approximately 50° of phase lead. These two quasi-quadrature waveforms are used to switch chroma modulators B and A, respectively. The transistors Q22 through Q25 and Q32–Q33 form a doubly balanced modulator. The input signal applied at pin 5 is compared to the color dc reference voltage applied at pin 6 in differential amplifier Q32–Q33. The source current provided by transistor Q34 is partitioned in transistors Q32 and Q33 according to the differential input signal. The bases of transistors Q23 and Q24 are connected to the dc reference voltage at the emitter of Q30. The bases of transistors Q22 and Q25 are connected to the phase delayed oscillator signal at the emitter of buffer transistor Q21. The differential signal currents provided by Q32 and Q33 are switched in transistors Q22 through Q25 and the resultant signal voltage is developed across R49. This signal has the phase and frequency of the oscillator signal at the emitter of Q21. The amplitude is proportional to the differential input signal applied between pins 5 and 6. Transistors Q26 through Q29 and Q38–Q39 form chroma modulator B. This modulator develops a signal voltage which is proportional to the differential voltage applied between pins 7 and 6. The phase and frequency of the output is equal to the phase advanced chroma oscillator at the emitter of buffer transistor Q20. Both chroma modulators A and B share the same output resistor, R49, so the output signal presented at the emitter of Q42 (pin 8) is the algebraic sum of modulators A and B.

The RF oscillator consists of differential amplifier Q18 and Q19 cross-coupled through emitter followers Q16 and Q17. The oscillator will operate at the parallel resonant frequency of the network connected between pins 13 and 14. The oscillator output is used to switch the doubly balanced RF modulator, Q9 through Q15. Transistors Q7 and Q8 provide level shifting and a high input impedance to the luminance input pin 9. The bases of transistors Q9 and Q10 are both biased through resistors R17 and R18, respectively, to the same dc reference voltage at Q6 emitter. The base voltage at Q10 may only be offset in a negative direction by luminance signal current source Q8. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal developed at pin 8 is externally ac coupled to pin 10 where it is reduced by resistor dividers R20 and R17, and added to the luminance signal in Q9. The resultant differential composite video currents are switched at the appropriate RF frequency in Q12 through Q15. The output signal current is presented at pin 12.

Transistors Q36, Q41 and resistors R44, R47 provide a highly stable voltage reference for biasing current sources Q43, Q34, Q35, and Q11.

MC1372 APPLICATION INFORMATION

Chrominance Oscillator

The oscillator is used as a clock signal for driving associated external circuitry, in addition to providing a switching signal for the chroma modulators. The IC uses an external crystal in a Colpitts configuration, as shown in Figure 5. Resistor R1 provides current limiting to reduce the signal swing. Capacitor C2 is adjusted for the exact frequency desired (3.579545 MHz).

In some applications, the duty cycle of the clock signal at pin 1 must be modified to overcome gate delays in associated equipment. The duty cycle may be adjusted by varying the dc voltage applied to pin 3. This adjustment may be made with the use of a potentiometer (10 kΩ) between supply and ground. With no connection to pin 3, the duty cycle is approximately 50%.

Chroma Modulator

The chrominance oscillator is internally phase shifted and applied to chroma modulators A and B. No external lead/lag networks are necessary. The phase relationship between the modulators is approximately 100°, which was chosen to provide the best rendition of colors using equal amplitude color-difference signals. The voltage applied to pin 5, 6, or 7 must always be within the Input Common Mode Voltage Range. Since the amplitude of chrominance output is proportional to the voltage difference between pins 5 and 6 or 7 and 6, it is desirable to select the Color Reference Voltage applied to pin 6 to be midway between $V5_{max}$ and $V5_{min}$ (which should be $V7_{max}$ and $V7_{min}$). The Chroma B Modulator will be defined as a (B-Y) modulator if a burst flag signal is applied to the Color B Input (pin 5) at the appropriate time. This voltage should be negative with respect to the Color Reference Voltage, and typically has an amplitude equal to $1/2[V6-V5_{min}]$. Since the phase of burst is always defined as –(B-Y), the Chroma A Modulator approximates an (R-Y) modulator; however, the phase is offset by 10° from the nominal 90°, to provide the 100° phase shift as discussed previously.

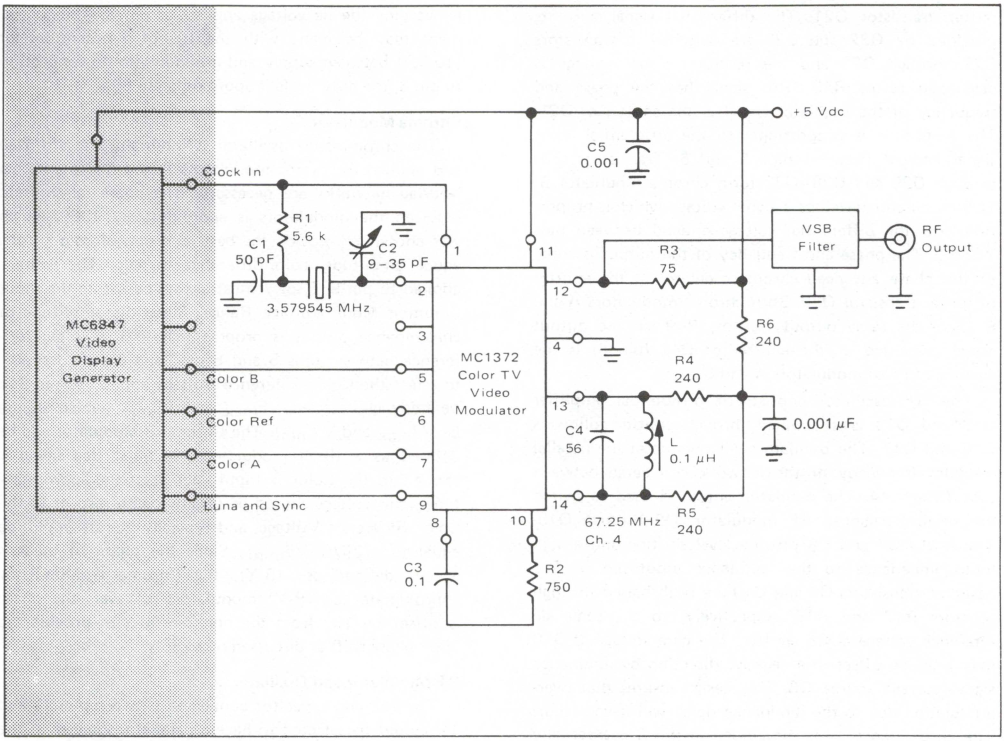
RF Modulator and Oscillator

The coil and capacitor connected between pins 13 and 14 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 5 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R4 and R5 are chosen to provide an adequate amplitude of switching voltage, whereas R6 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 9. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 9 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 10. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

FIGURE 5 – TYPICAL APPLICATION CIRCUIT


+5 Vdc
C5
0.001
MC6847
Video
Display
Generator
Clock In
R1
5.6 k
C1
50 pF
C2
9–35 pF
3.579545 MHz
Color B
Color Ref
Color A
Luna and Sync
1
2
3
4
5
6
7
8
9
10
11
12
13
14
MC1372
Color TV
Video
Modulator
R3
75
VSB
Filter
RF
Output
R6
240
R4
240
0.001 μF
C4
56
L
0.1 μH
R5
240
67.25 MHz
Ch. 4
C3
0.1
R2
750

The Luminance to Chrominance ratio (L:C) may be modified with the addition of an external resistor in series with pin 10 (as shown in Figure 5). The unmodified L:C (A_o) is determined by the ratio of the respective Conversion Gain for equal amplitude signals (typically, 0.883 = –1.6 dB). The modified L:C will be governed by the equation $A_o(1 + R_{ext}/800)$ for equal amplitude input signals.

The internal chrominance modulators are not internally connected to the RF modulator; therefore, the user has the option of connecting an externally generated chrominance signal to the RF modulator. In addition, the RF modulator is wideband, and a 4.5 MHz FM audio signal may be added to the chrominance input at pin 10. This may be accomplished by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

The modulated RF signal is presented as a current at RF Modulator Output, pin 12. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selection, as long as the voltage at pin 12 is high enough to prevent the output devices from reaching saturation (approximately 4.5 V with components in Figure 5). The peak current out of pin 12 is typically 2 mA. Hence, a load resistance of up to 250 ohms may be safely used with a 5 V supply.

Composite Video Signal Generation

The RF modulator may be easily used as a composite video generator by replacing the RF oscillator tank circuit with a diode as shown in Figure 3. This results in the output modulator being biased so the summation of luminance and chrominance appears unswitched at pin 12. The polarity of the output waveform is controlled by the direction of the diode. *Inverted video:* Anode to pin 14, cathode to pin 13. *Non-inverted video:* Anode to pin 13, cathode to pin 14. Note that the supply resistor must always be connected to the anode of the diode.

The amplitude of signal may be increased by increasing the load resistor on pin 12 and returning it to a higher supply voltage. Any voltage up to the Absolute Maximum Rating may be used.

Applications with MC6847 Video Display Generator

The MC1372 may be easily interfaced to the MC6847 as shown in Figure 5. The dc levels generated and required by the VDG are compatible with the MC1372, so that pins 1, 5, 6, 7, and 9 may be directly coupled to the appropriate MC6847 pins. Both integrated circuits as well as any associated NMOS MPU may be driven from a common 5 Vdc supply.

Recommended Chroma-Luma Signals

A chroma modulation angle of 100° was chosen to facilitate a desirable selection of colors with a minimum number of input signal levels. The following table demonstrates applicable signal levels for a variety of colors.

RECOMMENDED CHROMA-LUMA SIGNALS

	Pin #9 Luminance Input (Vdc)	Pin #7 Color A (Vdc)	Pin #6 Color Ref. (Vdc)	Pin #5 Color B (Vdc)
Sync	1.0	1.5	1.5	1.5
Blanking	0.75	1.5	1.5	1.5
Burst	0.75	1.5	1.5	1.25
Black	0.70	1.5	1.5	1.5
Green	0.50	1.0	1.5	1.0
Yellow	0.38	1.5	1.5	1.0
Blue	0.62	1.5	1.5	2.0
Red	0.62	2.0	1.5	1.5
Cyan	0.50	1.0	1.5	1.5
Magenta	0.50	2.0	1.5	2.0
Orange	0.50	2.0	1.5	1.0
Buff	0.38	1.5	1.5	1.5

MC1373

MOTOROLA

Advance Information

TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

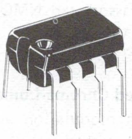
TV VIDEO MODULATOR

. . . an RF oscillator and dual-input modulator to generate a TV signal from baseband video inputs.

Applications include video games, home computer display, video tape recorders, and test equipment.

The very low level of intermodulation products, compact package and small external component count make this device superior to simple discrete circuits.

- Single 5.0 Vdc Supply
- Channel 3 or 4 Operation
- Excellent Oscillator Stability to 100 MHz
- Color and Sound Compabitility
- Dual Input Modulator for Ease of Signal Handling
- Low Intermodulation (−50 dB 920 kHz Beat)
- Overmodulation Protection



CASE 626-04
P SUFFIX

PIN CONNECTIONS

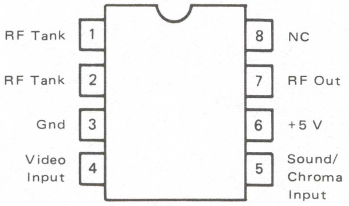
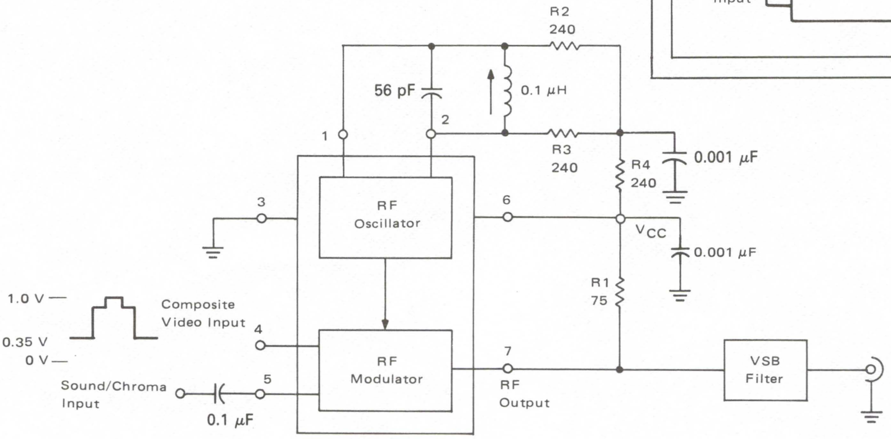

RF Tank 1
RF Tank 2
Gnd 3
Video Input 4
8 NC
7 RF Out
6 +5 V
5 Sound/Chroma Input

FIGURE 1 – BLOCK DIAGRAM AND APPLICATION CIRCUIT


R2
240
56 pF
0.1 μH
1
2
R3
240
R4
240
0.001 μF
3
RF Oscillator
6
VCC
0.001 μF
R1
75
1.0 V
0.35 V
0 V
Composite Video Input
4
RF Modulator
7
RF Output
VSB Filter
Sound/Chroma Input
5
0.1 μF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 10	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	—	12	—	mA
RF MODULATOR				
Luma Input Dynamic Range (Pin 4, Test Circuit 2)	0	—	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V4 = 1.0 V)	—	15	—	mVrms
Luma Conversion Gain ($\Delta V7/\Delta V4$, V4 = 0.1 to 1.0 Vdc) Test Circuit 2	—	0.8	—	V/V
Chroma Conversion Gain ($\Delta V7/\Delta V5$; V5 = 1.5 Vp-p;V4 = 1.0 Vdc) Test Circuit 2	—	0.95	—	V/V
Chroma Linearity (Pin 7, V5 = 1.5 Vp-p) Test Circuit 2	—	1.0	—	%
Luma Linearity (Pin 7, V4 = 0 to 1.5 Vdc) Test Circuit 2	—	2.0	—	%
Input Current (Pin 4)	—	—	−20	µA
Input Resistance (Pin 5)	—	800	—	Ω
Input Resistance (Pin 4)	100	—	—	kΩ
Input Capacitance (Pins 4, 5)	—	—	5.0	pF
Residual 920 kHz (Measured at Pin 7) See Note 1	—	60	—	dB
Output Current (Pin 7, V4 = 0 V) Test Circuit 2	—	1.5	—	mA

TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)

RF Oscillator Deviation (f_o = 67.25 MHz)	—	±250	—	kHz

NOTE 1. RF Reference Level = 6.0 mV @ Pin 7. Load Impedance = 75 Ω.
RF + 4.5 MHz = −13 dB.
RF + 3.58 MHz = −20 dB.

FIGURE 2 — TEST CIRCUIT 1

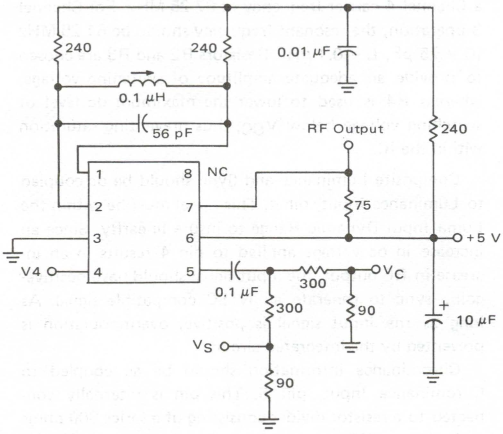


FIGURE 3 — TEST CIRCUIT 2

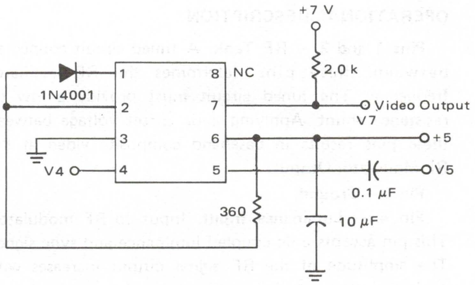
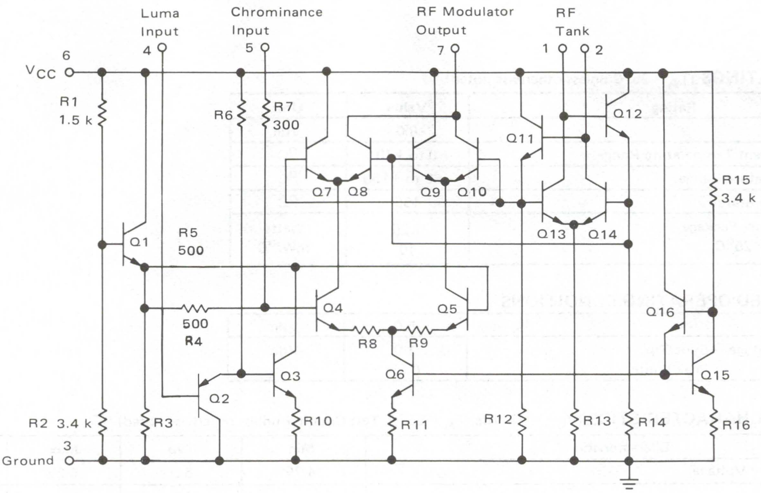


FIGURE 4 – SCHEMATIC DIAGRAM



SCHEMATIC DESCRIPTION

The RF oscillator consists of differential amplifier Q13 and Q14 cross-coupled through emitter followers Q11 and Q12. The oscillator will operate at the parallel resonant frequency of the network connected between pins 1 and 2. The oscillator output is used to switch the doubly balanced RF modulator, Q4 through Q10. Transistors Q2 and Q3 provide level shifting and a high input impedance to the luminance input pin 4. The bases of transistors Q4 and Q5 are both biased through resistors R4 and R5, respectively, to the same dc reference voltage at Q1 emitter. The base voltage at Q5 may only be offset in a negative direction by luminance signal current source Q3. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal is externally ac coupled to pin 5 where it is reduced by resistor dividers R7 and R4, and added to the luminance signal in Q4. The resultant differential composite video currents are switched at the appropriate RF frequency in Q7 through Q10. The output signal current is presented at pin 7.

Transistors Q15, Q16 and resistors R15, R16 provide a highly stable voltage reference for biasing the current source Q6.

OPERATIONAL DESCRIPTION

Pins 1 and 2 – RF Tank. A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

Pin 3 – Ground.

Pin 4 – Luminance Input. Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 5 – Chrominance/Sound Input. Input to the RF modulator. This pin accepts an ac coupled chrominance signal. The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. A 4.5 MHz FM audio signal may be added to the input by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

Pin 6 – V_{CC}. Positive supply voltage.

Pin 7 – RF Modulator Output. Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pin 8 – No Connection.

APPLICATIONS INFORMATION (Refer to Figure 1)

RF Modulator and Oscillator

The coil and capacitor connected between pins 1 and 2 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R4 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 4. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 4 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 5. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

MOTOROLA

MC1374

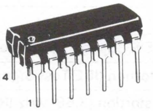
TV MODULATOR CIRCUIT

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, T.V. games and subscription decoders.

- Single Supply, 5 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

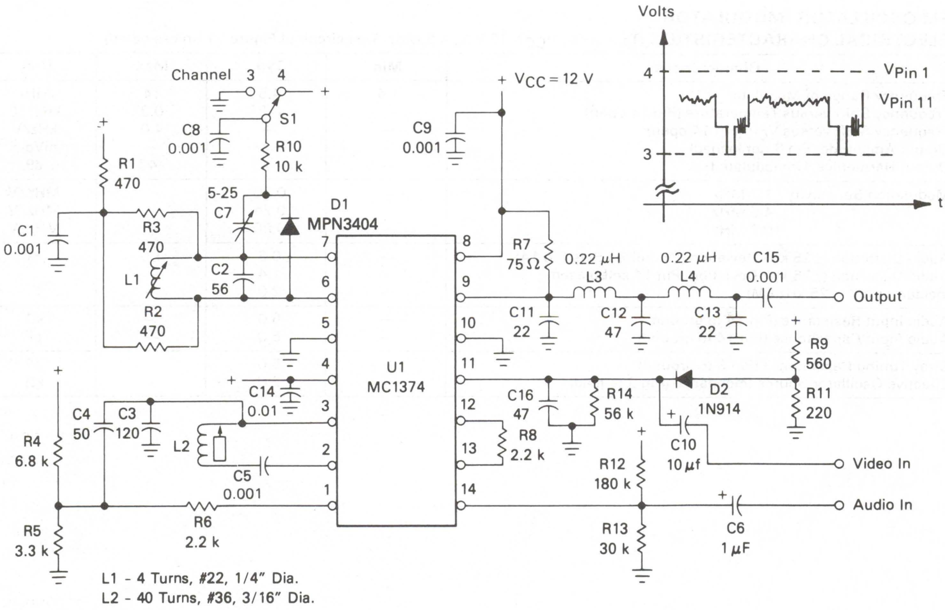
TV MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 — TYPICAL APPLICATION


Volts
4
3
VPin 1
VPin 11
t
Channel 3 4
S1
C8 0.001
R10 10 k
C9 0.001
+ VCC = 12 V
R1 470
C1 0.001
R3 470
5-25 C7
D1 MPN3404
L1
C2 56
R2 470
U1 MC1374
R7 75 Ω
0.22 µH L3
0.22 µH L4
C15 0.001
Output
C11 22
C12 47
C13 22
R9 560
R11 220
C16 47
R14 56 k
D2 1N914
R8 2.2 k
C10 10 µf
R12 180 k
Video In
Audio In
C6 1 µF
R13 30 k
C14 0.01
C4 50
C3 120
L2
C5 0.001
R4 6.8 k
R5 3.3 k
R6 2.2 k
1
2
3
4
5
6
7
8
9
10
11
12
13
14

L1 - 4 Turns, #22, 1/4" Dia.
L2 - 40 Turns, #36, 3/16" Dia.

Shaded Parts Optional

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	14	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 10 mW/°C	Watts

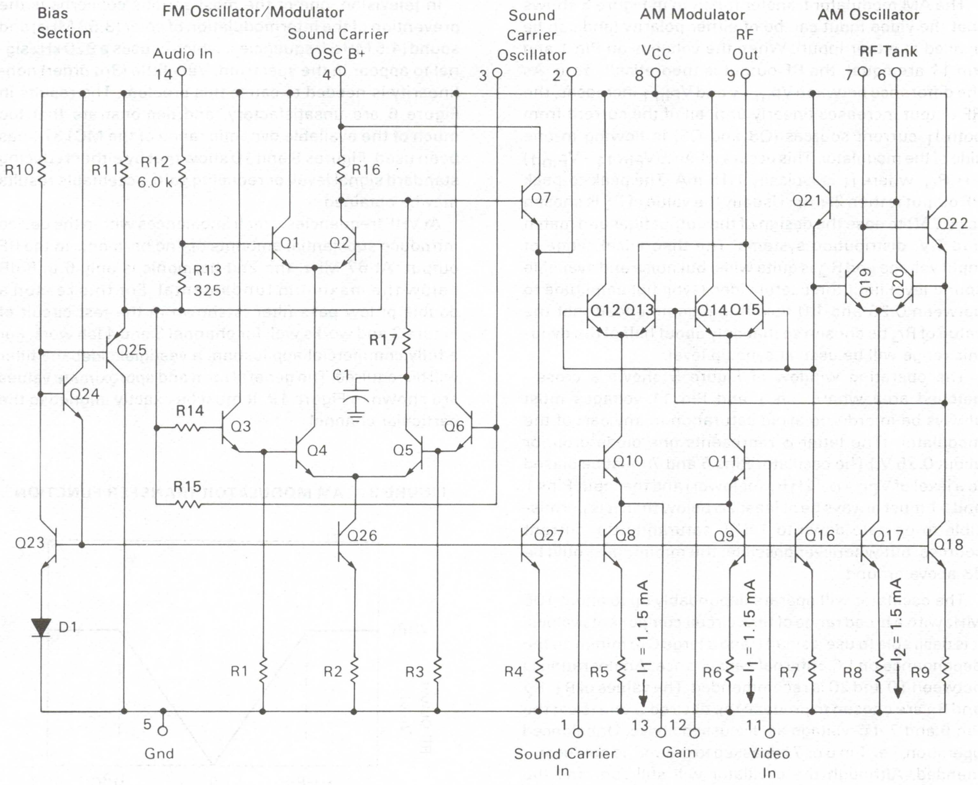
AM OSCILLATOR/MODULATOR ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, f_c = 67.25 MHz, Figure 4 circuit, unless noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	5.0	12	12	V
Supply Current (Figure 1)	—	13		mA
Video Input Dynamic Range (Sync Amplitude)	0.25	1.0	1.0	V Pk
RF Output (Pin 9, R7 = 75 Ω, No External Load)	—	170	—	mV pp
Carrier Suppression	36	40	—	dB
Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz)	—	—	2.0	%
Differential Gain Distortion (IRE Test Signal)	5.0	7.0	10	%
Differential Phase Distortion (3.58 MHz IRE Test Signal)	—	1.5	2.0	Degrees
920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%)	—	-57	—	dB
Video Bandwidth (75 Ω Input Source)	30	—	—	MHz
Oscillator Frequency Range	—	105	—	MHz
Internal Resistance across Tank (Pin 6 to Pin 7)	—	1.8	—	kΩ
Internal Capacitance across Tank (Pin 6 to Pin 7)	—	4.0	—	pF

FM OSCILLATOR/MODULATOR ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc, 4.5 MHz, Test circuit of Figure 11 unless noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range of Modulator	1.4	4.5	14	MHz
Frequency Shift versus Temperature (Pin 14 open)	—	0.2	0.3	kHz/°C
Frequency Shift versus V_{CC} (Pin 14 open)	—	—	4.0	kHz/V
Output Amplitude (Pin 3 not loaded)	—	900	—	mVp-p
Output Harmonics, Unmodulated	—	—	-40	dB
Modulation Sensitivity 1.7 MHz	—	0.20	—	MHz/V
4.5 MHz	—	0.24	—	MHz/V
10.7 MHz	—	0.80	—	MHz/V
Audio Distortion (±25 kHz Deviation ,Optimized Bias Pin 14)	—	0.6	1.0	%
Audio Distortion (±25 kHz Deviation, Pin 14 self biased)	—	1.4	—	
Incidental AM (±25 kHz FM)	—	2.0	—	
Audio Input Resistance (Pin 14 to ground)	—	6.0	—	kΩ
Audio Input Capacitance (Pin 14 to ground)	—	5.0	—	pF
Stray Tuning Capacitance (Pin 3 to ground)	—	5.0	—	pF
Effective Oscillator Source Impedance (Pin 3 to load)	—	2.0	—	kΩ

FIGURE 2 — TV MODULATOR


Bias Section
FM Oscillator/Modulator
Audio In
14
Sound Carrier OSC B+
4
Sound Carrier Oscillator
3
2
AM Modulator
VCC
8
RF Out
9
AM Oscillator
RF Tank
7
6
R10
R11
R12 6.0 k
R16
Q1
Q2
R13 325
Q25
Q24
R17
C1
R14
Q3
Q4
Q5
Q6
R15
Q7
Q12 Q13
Q14 Q15
Q21
Q22
Q19
Q20
Q10
Q11
Q23
Q26
Q27
Q8
Q9
Q16
Q17
Q18
D1
R1
R2
R3
R4
R5
R6
R7
R8
R9
I1 = 1.15 mA
I1 = 1.15 mA
I2 = 1.5 mA
5
Gnd
1
Sound Carrier In
13
12
Gain
11
Video In

GENERAL DESCRIPTION

The MC1374 contains an RF oscillator, RF modulator, and a phase-shift type FM modulator, arranged to permit good printed circuit layout of a complete T.V. modulation system. The RF oscillator is similar to the one used in MC1372 and MC1373, and is coupled internally in the same way. It's frequency is controlled by an external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to V_{CC}.

The FM system was designed specifically for the T.V. intercarrier function. For circuit economy, one phase shift circuit was built into the chip. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). At 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would offset the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a dc feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

THE AM SECTION

The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increases, the RF output increases linearly until all of the current from both I_1 current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin\ 11} - V_{Pin\ 1}) = I_1 R_G$, where I_1 is typically 1.15 mA. The peak-to-peak RF output is then $2I_1 R_L$. Usually the value of R_L is chosen to be 75Ω to ease the design of the output filter and match into T.V. distribution systems. The theoretical range of input voltage and R_G is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 and 1.0 Vpk. It is recommended that the value of R_G be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross-hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. (The letter ϕ represents one diode drop, or about 0.75 V.) The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least 2ϕ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be 3ϕ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit components values. It is desirable to use a small L and a large C to minimize the dependence on I.C. internal capacitance. An operating Q between 10 and 20 is recommended. The values of R_1, R_2 and R_3 are chosen to produce the desired Q and to set the Pin 6 and 7 d.c. voltage as discussed above. Unbalanced operation; i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ±20 kHz total shift from 0°C to 50°C as shown in Figure 7. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) nonlinearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 to 8 dB below the maximum fundamental. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

FIGURE 3 — AM MODULATOR TRANSFER FUNCTION

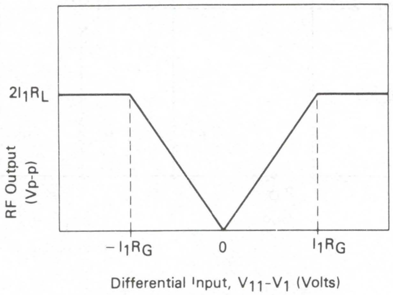


FIGURE 4 — AM TEST CIRCUIT

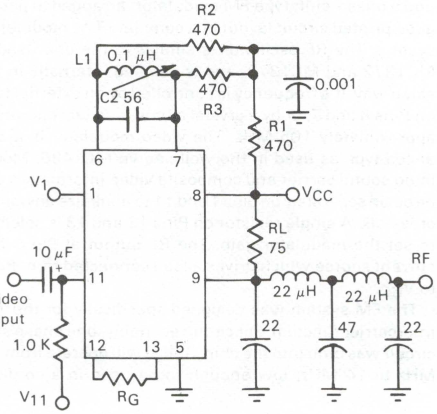


FIGURE 5 — THE OPERATING WINDOW

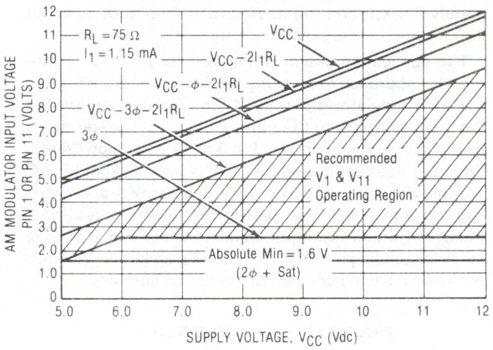


FIGURE 6 — 920 kHz BEAT

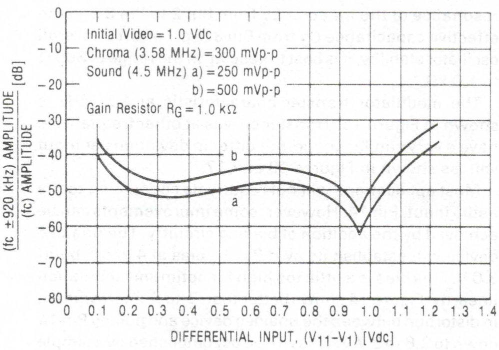


FIGURE 7 — RF OSCILLATOR FREQUENCY versus TEMPERATURE

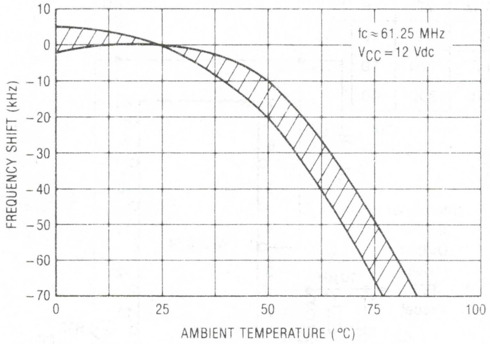


FIGURE 8 — 920 kHz BEAT

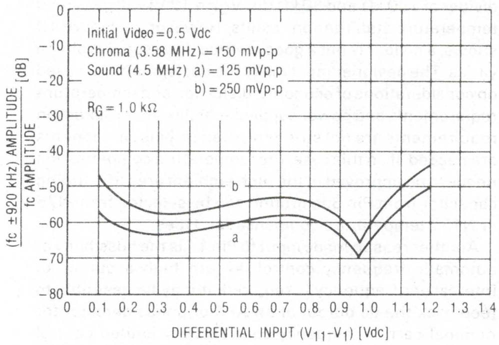


FIGURE 9 — RF OSCILLATOR FREQUENCY versus SUPPLY VOLTAGE

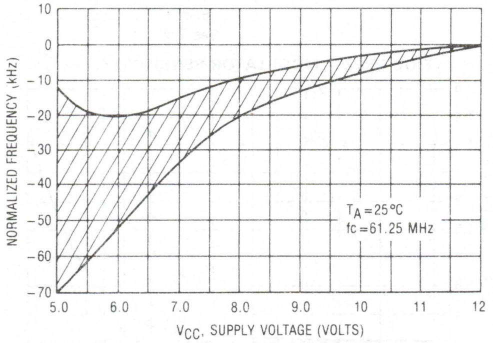
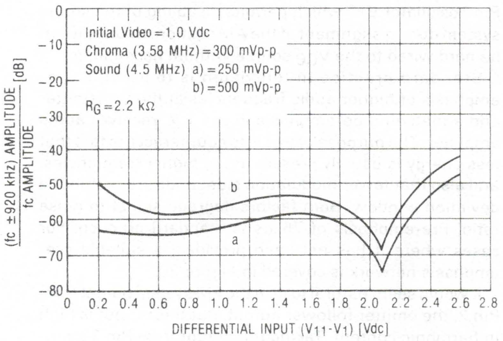


FIGURE 10 — 920 kHz BEAT



FM SECTION

The oscillator center frequency is approximately the resonance of the inductor L_2 from Pin 2 to Pin 3 and the effective capacitance C_3 from Pin 3 to ground. For overall oscillator stability, it is best to keep X_L in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require dc connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at $4\,\theta$, or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2-to-1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 kΩ and 30 kΩ (for $V_{CC} = 12$ V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for dc input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of intercarrier frequency is required, it may be desirable to feed back the dc output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

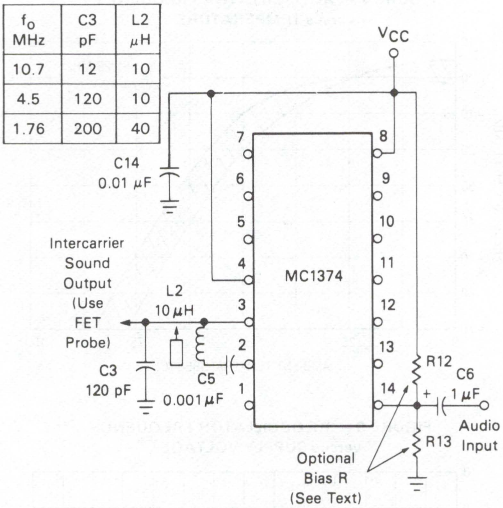
One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the V_{CC} source without decoupling.

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the T.V. receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ratio. Pre-emphasis of 75 μs is standard practice. For cases where it has not been provided, a suitable pre-emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering components. The source impedance of Pin 3 is approximately 2.0 kΩ, and the open circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C4 into the video bias circuit impedance of R4 and R5, about 2.2 K. This provides an intercarrier level of 500 mV p-p, which is correct for the 1.0 V peak video level chosen in this design. Resistor R6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

FIGURE 11 — FM TEST CIRCUIT



f_o MHz	C3 pF	L2 μH
10.7	12	10
4.5	120	10
1.76	200	40

FIGURE 12 — MODULATOR SENSITIVITY

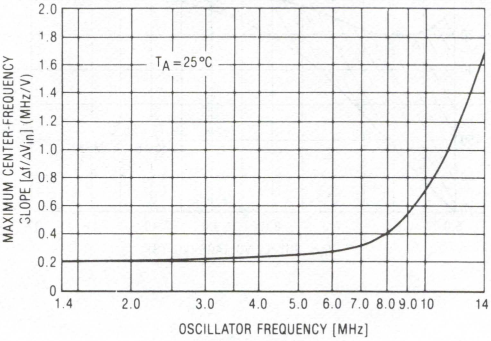


FIGURE 13 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

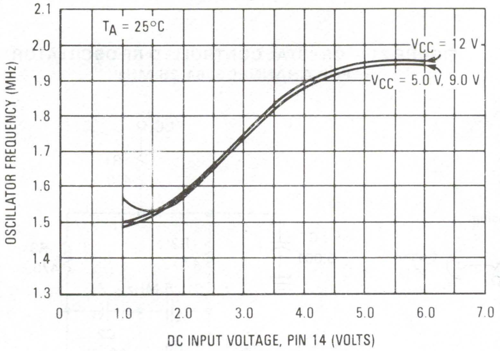


FIGURE 14 — DISTORTION versus MODULATION DEPTH

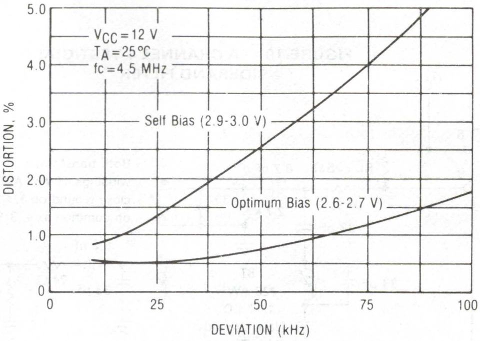


FIGURE 15 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

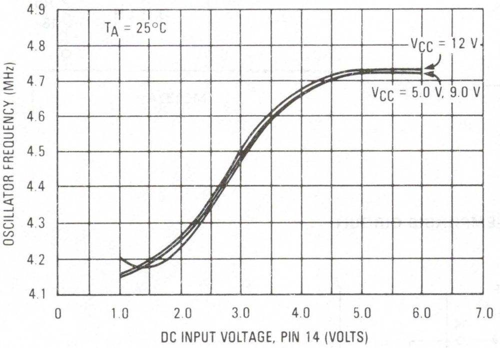


FIGURE 16 — FM SYSTEM FREQUENCY versus TEMPERATURE

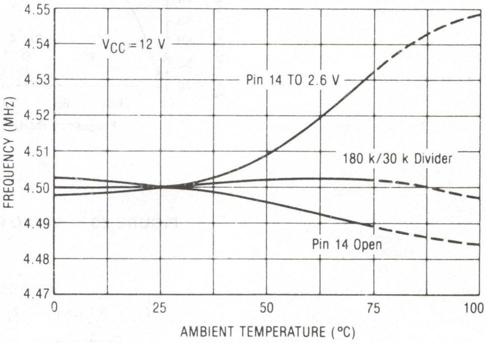


FIGURE 17 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

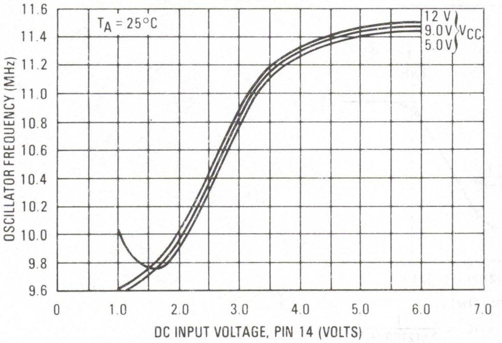


FIGURE 18 — FM SYSTEM FREQUENCY versus V_{CC}

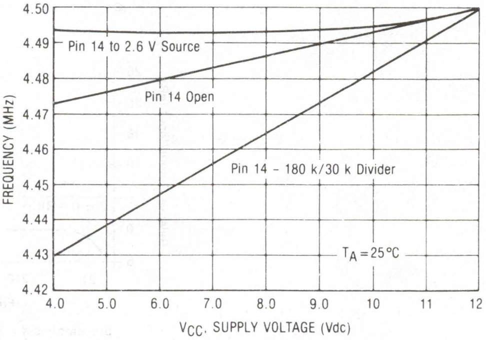


FIGURE 19 — A CHANNEL 4 VESTIGIAL SIDEBAND FILTER

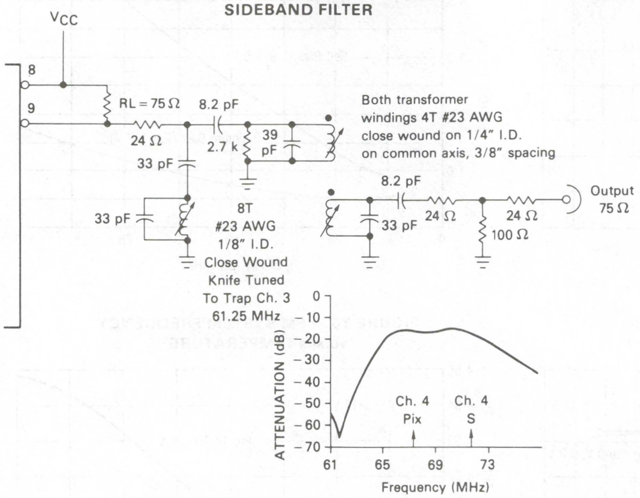

VCC
8
9
RL = 75 Ω
8.2 pF
24 Ω
2.7 k
39 pF
33 pF
33 pF
8T
#23 AWG
1/8″ I.D.
Close Wound
Knife Tuned
To Trap Ch. 3
61.25 MHz
Both transformer windings 4T #23 AWG close wound on 1/4″ I.D. on common axis, 3/8″ spacing
8.2 pF
33 pF
24 Ω
24 Ω
100 Ω
Output
75 Ω
ATTENUATION (dB)
0
− 10
− 20
− 30
− 40
− 50
− 60
− 70
Ch. 4
Pix
Ch. 4
S
61
65
69
73
Frequency (MHz)

FIGURE 21 — CRYSTAL CONTROLLED RF OSCILLATOR FOR CHANNEL 3, 61.25 MHz

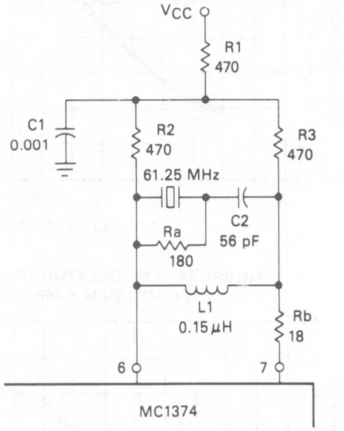
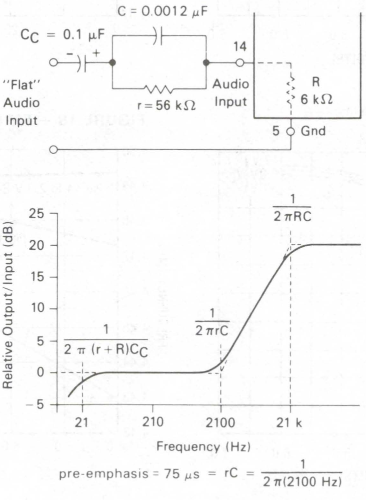

VCC
R1
470
C1
0.001
R2
470
R3
470
61.25 MHz
C2
56 pF
Ra
180
L1
0.15 μH
Rb
18
6
7
MC1374

FIGURE 20 — AUDIO PRE-EMPHASIS CIRCUIT


C = 0.0012 μF
CC = 0.1 μF
−
+
14
"Flat"
Audio
Input
r = 56 kΩ
Audio
Input
R
6 kΩ
5
Gnd
Relative Output/Input (dB)
25
20
15
10
5
0
− 5
1/(2 π (r + R)CC)
1/(2 πrC)
1/(2 πRC)
21
210
2100
21 k
Frequency (Hz)
pre-emphasis = 75 μs = rC = 1/(2 π(2100 Hz))

MOTOROLA

MC1376

Advance Information

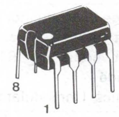
FM MODULATOR CIRCUIT

. . . a voltage-controlled oscillator/modulator ideally suited to cordless telephone and television intercarrier applications.

- Wide Supply Range (5.0–12 Vdc)
- Useful Frequency Range (1.4–14 MHz)
- Low Distortion (<1%)
- Excellent Oscillator Stability
- Output RF Driver Transistor Included
- Low Cost, Low Component Count Circuit
- Wide Deviation Capability

FM MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



CASE 626-04

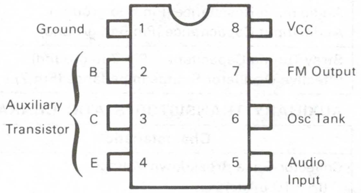
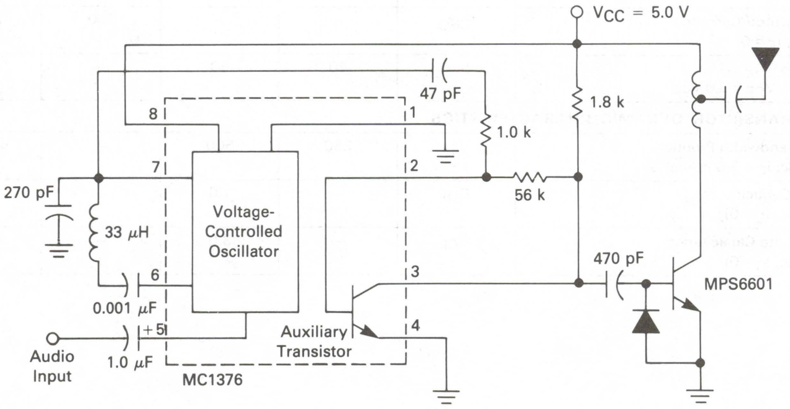

Ground
1
8
VCC
B
2
7
FM Output
Auxiliary Transistor
C
3
6
Osc Tank
E
4
5
Audio Input

FIGURE 1 — CORDLESS TELEPHONE BASE STATION TRANSMITTER (1.76 MHz)


VCC = 5.0 V
47 pF
1.8 k
1.0 k
56 k
8
1
7
2
270 pF
33 μH
Voltage-Controlled Oscillator
6
3
0.001 μF
470 pF
MPS6601
+
5
4
Audio Input
1.0 μF
Auxiliary Transistor
MC1376

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A 25°C unless otherwise noted)

Rating	Value	Unit
Modulator Supply Voltage	13	Vdc
Transistor Collector-Emitter Voltage	10	Vdc
Transistor Collector-Base Voltage	15	Vdc
Operating Ambient Temperature Range	0 to +75	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.2 10	Watts mW/°C

MODULATOR ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	5.0	—	12	Vdc
Supply Current, V_{CC} = 12 Vdc (excluding transistor)	—	5.0	8.0	mAdc
Frequency Range of Modulator	—	1.4–14	—	MHz
Frequency Shift versus Temperature (R1 = ∞)	—	—	0.3	kHz/°C
Frequency Shift versus V_{CC} (R1 = ∞)	—	3.3	—	kHz/V
Output Amplitude	80	150	—	mVp-p
Output Harmonics, Unmodulated	—	−43	—	dB
Modulation Sensitivity 1.7 MHz	—	0.20	—	MHz/V
4.5 MHz	—	0.24	—	MHz/V
10.7 MHz	—	0.80	—	MHz/V
Audio Distortion (±25 kHz, Deviation, R1 = 27 k, f_o = 4.5 MHz)	—	0.55	—	%
Incidental AM (±25 kHz FM, 4.5 MHz)	—	2.0	—	%
Audio Input Resistance (Pin 5 to ground)	—	6.0	—	kΩ
Audio Input Capacitance (Pin 5 to ground)	—	5.0	—	pF
Stray Tuning Capacitance (Pin 7 to ground)	—	6.0	—	pF
Effective Oscillator Source Impedance (Pin 7)	—	2.0	—	kΩ

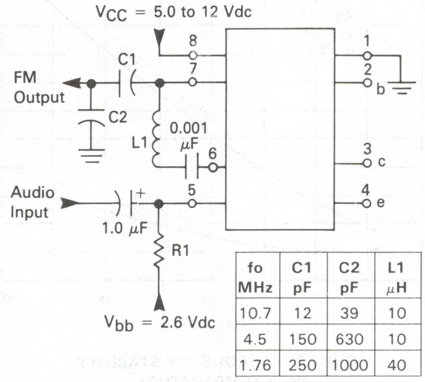
AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	15	40	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 μAdc)	$V_{(BR)CEO}$	10	—	—	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CIO}$	15	40	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector-Base Cutoff Current (I_{BE} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	200	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 3.0 Vdc)	h_{FE}	40	90	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	250	500	—	MHz
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	—	1.0	—	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	—	3.0	—	pF

FIGURE 2 — TEST CIRCUIT



fo MHz	C1 pF	C2 pF	L1 µH
10.7	12	39	10
4.5	150	630	10
1.76	250	1000	40

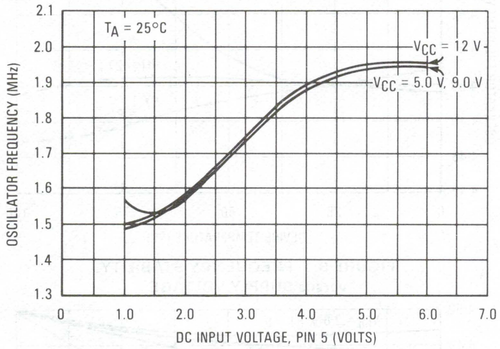


FIGURE 3 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

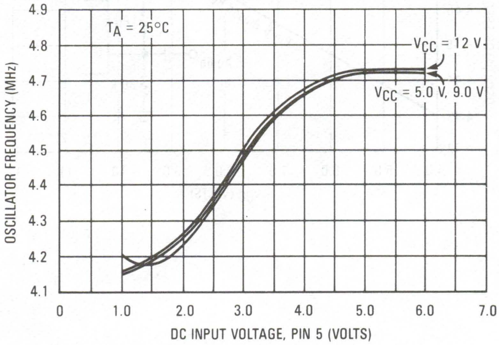


FIGURE 4 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

MC1376 GENERAL INFORMATION

This device was initially designed for the base station transmitter of a cordless telephone, the 1.76 MHz FM modulator shown in Figure 1. It also contains a "separate" transistor suitable for service as an output buffer or amplifier for up to 50 mA. Though the oscillator contains internal phase shift components which are not accessible, the MC1376 still has an operating frequency range of 1.4 to 14 MHz, making it a good companion to MC1372 or MC1373 as a 4.5 or 5.5 MHz intercarrier sound modulator for television signal generation. Also, the device can be used as a low cost FM IF (10.7 MHz) signal source for the production line or lab. Although not suitable for true high fidelity distortion measurements, it can handle quite wide deviation with very modest distortion, compared to other oscillator configurations. The modulator section is identical to the FM portion of the MC1374, TV modulator.

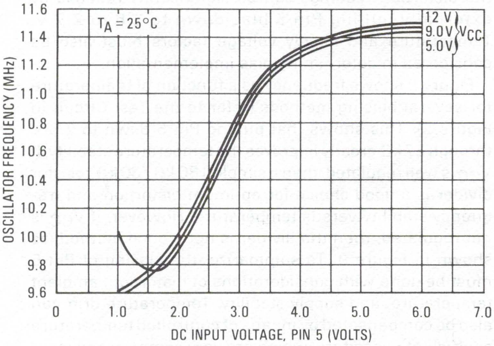


FIGURE 5 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

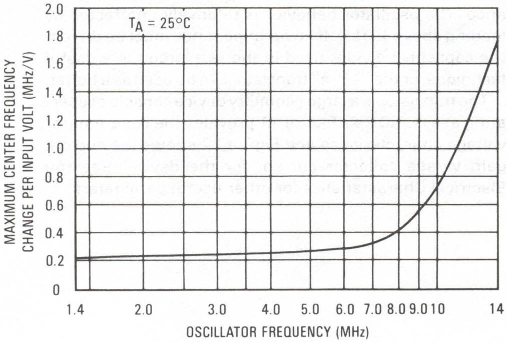


FIGURE 6 — MODULATOR SENSITIVITY

APPLICATIONS INFORMATION

The oscillator center frequency is approximately the resonance of the inductor (Pin 6 to Pin 7) and the total capacitance from Pin 7 to ground. Include 6.0 pF (internal) and the circuit strays in the resonant frequency calculations for the higher frequency applications. For overall oscillator stability, it is best to keep the X_L and X_C in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristics for three test frequencies are shown in Figures 3, 4 and 5. Although the horizontal axes of these curves are labelled "dc input voltage, Pin 5", they are valid transfer functions relating instantaneous Pin 5 voltage to output frequency.

Figure 6 is a plot of the maximum deviation per input volt over the usable frequency range of the part.

Most applications will require no dc connection at the audio input, Pin 5. However, some performance improvements can be achieved by addition of biasing circuitry. The unaided device will usually establish its own Pin 5 bias at 2.9 to 3.0 V. A brief study of Figures 3, 4, and 5 shows that this bias is a little high for optimum modulation linearity. This is verified by taking distortion measurments using a high quality FM detector (see Figure 7). Note that the distortion readings can be significantly reduced by externally pulling Pin 5 bias down to 2.6 to 2.7 V. Temperature and supply voltage factors must also be considered in determining bias implementation.

Figure 8 shows frequency as a function of temperature for several biasing methods (refer to the Test Circuit in Figure 2). This shows that pulling Pin 5 down to 2.6 V through 27 kΩ greatly improves the temperature stability. If V_{CC} is well regulated, then a simple 180 kΩ/30 kΩ resistor divider is a good choice for optimum distortion and frequency stability versus temperature. However, if V_{CC} is not regulated, then the divider is not a good method, as shown in Figure 9. To summarize, the biasing of Pin 5 must be done with considerations of distortion, ambient temperature, and supply stability. Temperature drift can also be compensated by means of controlled temperature coefficient capacitors, which are very common and inexpensive in this range of values. An N150 type used for C1 will nearly flatten the R1 = ∞ case in Figure 8.

The FM output at Pin 7 is usually about 600 mVp-p and has low harmonic content and high (2 kΩ) output impedance. The oscillator behavior is relatively unaffected by loading above 1.0 kΩ. If lower impedance must be driven, the capacitive divider used in the test circuit is a useful technique, or the "extra" transistor can be used as a buffer.

The transistor is a large geometry device capable of operating at over 50 mA. Figure 11 provides the base-emitter voltage characteristics and Figure 12 shows the current gain versus collector current for the device. See the Electrical Characteristics for other useful parameters.

FIGURE 7 — DISTORTION versus MODULATION DEPTH

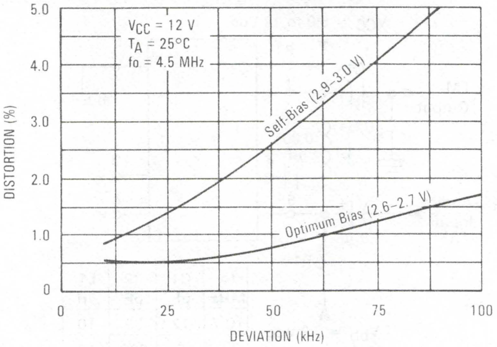


FIGURE 8 — FREQUENCY STABILITY versus TEMPERATURE

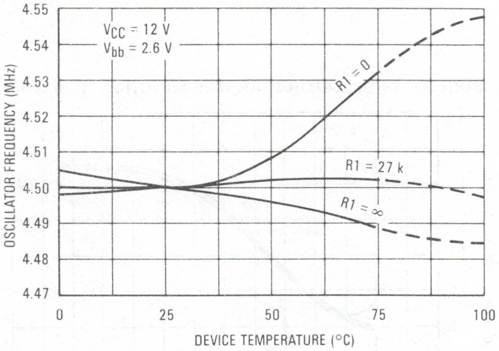


FIGURE 9 — FREQUENCY STABILITY versus SUPPLY VOLTAGE

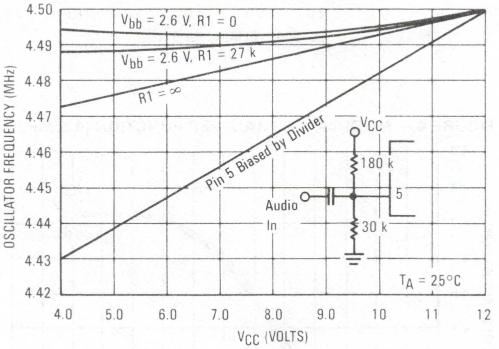


FIGURE 10 — INTERNAL SCHEMATIC

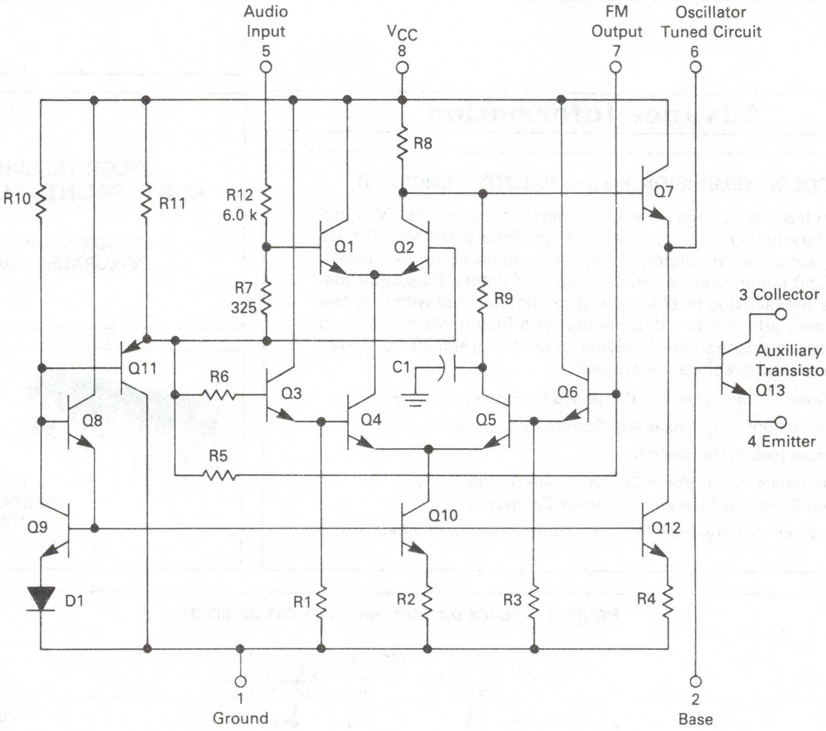

Audio Input 5
V_{CC} 8
FM Output 7
Oscillator Tuned Circuit 6
R8
R10
R11
R12 6.0 k
Q7
Q1
Q2
R7 325
R9
3 Collector
Auxiliary Transistor Q13
4 Emitter
Q11
R6
Q3
C1
Q6
Q8
Q4
Q5
R5
Q9
Q10
Q12
D1
R1
R2
R3
R4
1 Ground
2 Base

FIGURE 11 — BASE-EMITTER VOLTAGE

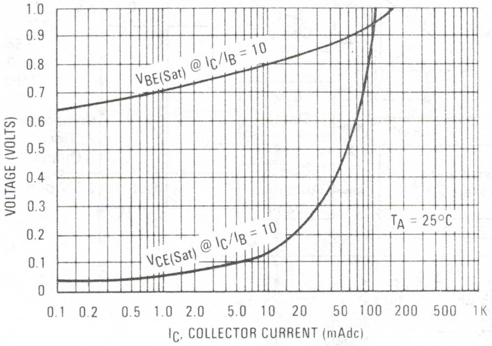
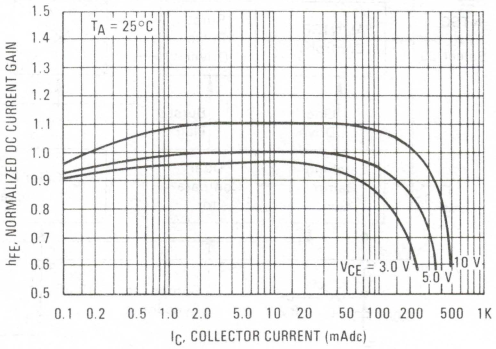


FIGURE 12 — NORMALIZED DC CURRENT GAIN



MOTOROLA

MC1377

Advance Information

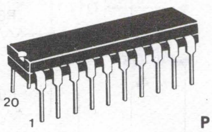
COLOR TELEVISION RGB to PAL/NTSC ENCODER

. . . an integrated circuit used to generate a composite TV signal from baseband red, blue, green and sync inputs. The MC1377 has color subcarrier oscillator, voltage controlled 90° phase shifter, two DSB suppressed carrier chroma modulators, RGB input matrices and blanking level clamps. It can be operated with very few external parts, but has the pinouts for a fully implemented, top quality composite signal. It is ideal for encoding signals from color cameras and graphics generators.

- Reference Oscillator Self-Contained Or Externally Driven
- Nominal 90° ±5.0° Axes Are Optionally Trimmable
- Simple PAL/NTSC Switch
- Luminance And Chroma Channels Can Accept Delay Line/Bandpass Elements Or Direct Connection
- Provides dc Reference To Permit Direct Drive To RF Modulator

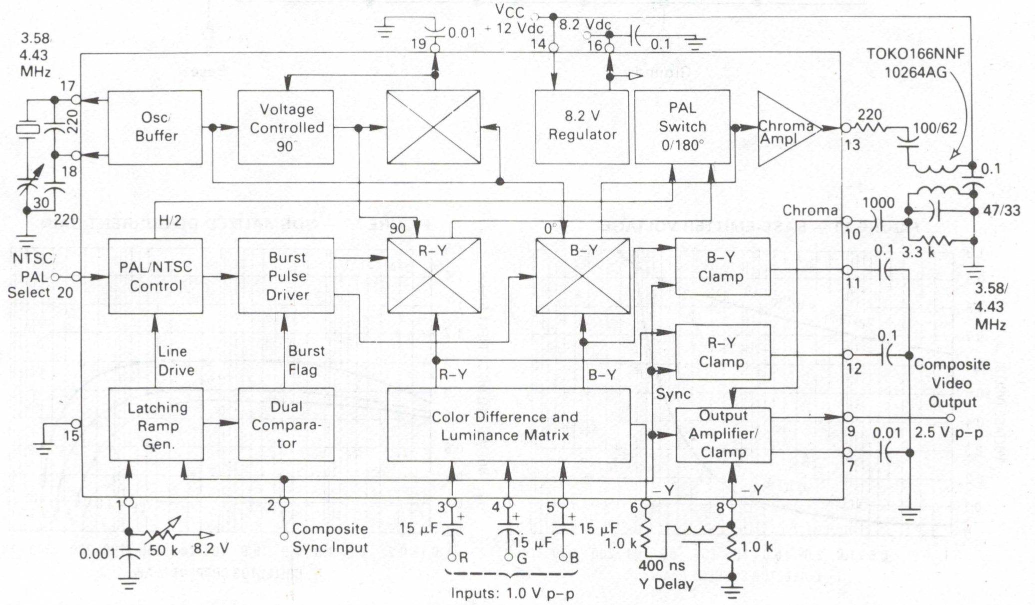
COLOR TELEVISION RGB to PAL/NTSC ENCODER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT



3.58/
4.43
MHz
17
220
18
30
220
Osc/
Buffer
Voltage
Controlled
90°
0.01
19
VCC
+12 Vdc
14
8.2 Vdc
16
0.1
8.2 V
Regulator
PAL
Switch
0/180°
Chroma
Ampl
TOKO166NNF
10264AG
220
13
100/62
0.1
47/33
Chroma
1000
10
0.1
3.3 k
11
3.58/
4.43
MHz
H/2
90
0°
NTSC/
PAL
Select 20
PAL/NTSC
Control
Burst
Pulse
Driver
R–Y
B–Y
B–Y
Clamp
R–Y
Clamp
0.1
12
Composite
Video
Output
Line
Drive
Burst
Flag
R–Y
B–Y
Sync
Latching
Ramp
Gen.
Dual
Compara-
tor
Color Difference and
Luminance Matrix
Output
Amplifier/
Clamp
9
0.01
2.5 V p–p
7
15
1
2
3
4
5
6
8
–Y
–Y
0.001
50 k
8.2 V
Composite
Sync Input
15 µF
15 µF
15 µF
R
G
B
Inputs: 1.0 V p–p
1.0 k
1.0 k
400 ns
Y Delay

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
8.2 Vdc Regulator Output Current	I_{REG}	10	mAdc
Operating Temperature	T_{AMB}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation, package Derate above 25°C	P_D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

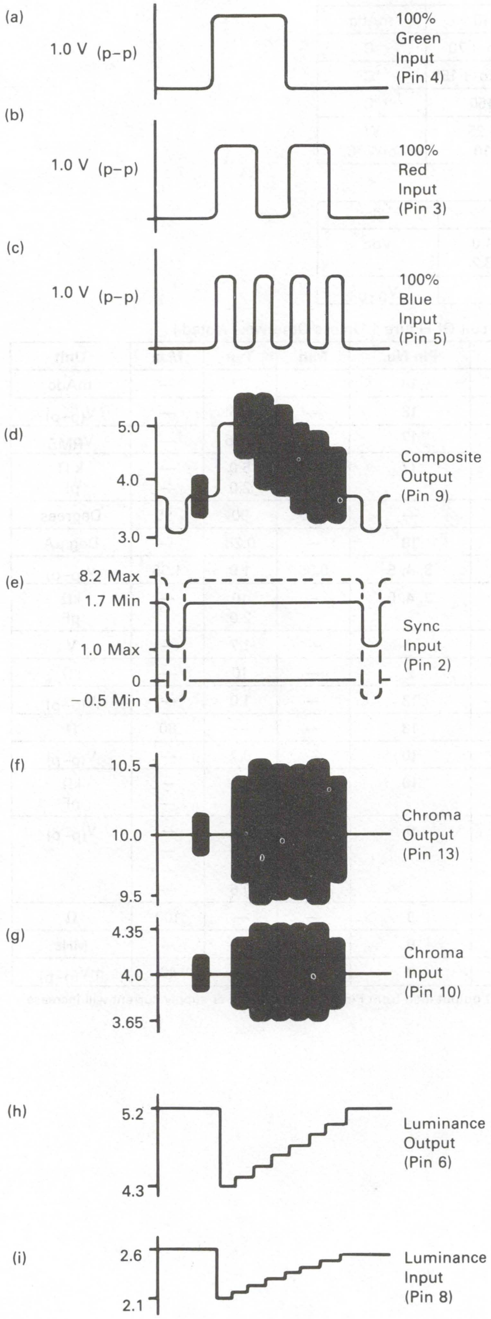
Supply Voltage	12 ± 2	Vdc
Sync Tip Level Sync, Blanking Level	−0.5 to +1.0 +1.7 to +8.2	Vdc
Red, Green, Blue Inputs (Saturated)	1.0	V_{p-p}

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, Circuit Of Figure 1 Unless Otherwise Noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
Supply Current	14	—	32	—	mAdc
Oscillator Amplitude	18	—	0.5	—	$V_{(p-p)}$
External Subcarrier Input (Oscillator Components Removed)	17	—	0.25	—	V_{RMS}
Subcarrier Input: Resistance Capacitance	17	— —	5.0 2.0	— —	k Ω pF
Modulation Angle (R−Y) to (B−Y)	—	85	90	95	Degrees
(R−Y) Angle Adjustment	19	—	0.25	—	Deg/μA
R, G, B Input For 100% Color Saturation	3, 4, 5	0.95	1.0	1.05	$V_{(p-p)}$
R, G, B Input: Resistance Capacitance	3, 4, 5	— —	10 2.0	— —	kΩ pF
Sync Threshold (See Figure 2e)	2	—	1.7	—	V
Sync Input Resistance (Input > 1.7 V)	2	—	10	—	kΩ
Chroma Output Level At 100% Saturation	13	—	1.0	—	$V_{(p-p)}$
Chroma Output Resistance	13	—	—	80	Ω
Chroma Input Level For 100% Saturation	10	—	0.7	—	$V_{(p-p)}$
Chroma Input: Resistance Capacitance	10	— —	10 2.0	— —	kΩ pF
Composite Output, 100% Saturation (See Figure 2d): Sync Luminance Chroma Burst	9	— — — —	0.6 1.4 1.7 0.6	— — — —	$V_{(p-p)}$
Output Impedance (See Note 1)	9	—	—	100	Ω
Luminance Bandwidth (3 dB), Less Delay Line	9	—	8.0	—	MHz
Subcarrier Leakage In Output	9	—	—	40	$mV_{(p-p)}$

Note 1: Output Impedance can be reduced to less than 10Ω by using a 150Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.

FIGURE 2 — SIGNAL VOLTAGES
(CIRCUIT VALUES OF FIGURE 1)



APPLICATION NOTES

R.G.B. Inputs should be set up to be 1.0 V p–p for fully saturated levels. This is not arbitrary, since sync and burst levels are internally fixed. The large (15 μF) input capacitors of Figure 1 are needed for the 50/60 Hz vertical component.

Subcarrier Oscillator. The internal common-collector Colpitts can be free run or it can easily be pulled in by a lightly coupled signal from a "master" into Pin 17. Also, it can be disabled entirely and a 0.25 V_{RMS} signal driven into Pin 17.

Modulator Phase Angles are quite accurately established internally. Taking (B–Y) as 0°, burst is at 180°, and the angle of (R–Y) is 90° ± 5.0°. The (R–Y) angle can be "tweaked." For example, 470 kΩ from Pin 19 to ground will increase the (R–Y) to (B–Y) angle about 3.0°. Pulling Pin 19 up will decrease the angle.

Composite Output is dc referenced and can be direct coupled to an RF modulator as shown in Figure 3. In this case, the 8.2 V regulator output of the MC1377 is divided down to 5.8 V to provide the zero carrier reference to Pin 1 of the MC1374.

Burst Generation is provided by a sync triggered ramp on Pin 1 and two internal level sensors. Since the early part of this ramp is used, it is quite accurate. Fixed R–C values are feasible, as shown in Figure 3.

Sync Input can be varied over a wide latitude but neverless must be applied correctly. The typical ac coupled sync signal has very little positive value and will require a pull-up resistor to 8.2 Vdc at the input. The sync input is a 10 kΩ/10 kΩ divider in the base of a common emitter stage. For PAL operation, the correctly serrated vertical sync interval must be used, in order to continuously trigger the PAL flip-flop. "Block" vertical sync can be used for NTSC.

(R–Y)(B–Y)(–Y) signals are generated to NTSC values (±5.0%) in the input matrices. They are dc clamped at black level by a sync driven clamp. Burst amplitude is internally fixed to correspond to sync level, allowing for 3.0 dB loss in the chroma bandpass filter. If the filter is not used, as shown in Figure 3, a resistor divider should be inserted between Pin 13 and Pin 10 to provide the proper chroma level. When the chroma bandpass is not used, the (–Y) delay line should also be removed, but the 1.0 k/1.0 k divider from Pin 6 to Pin 8 should be retained.

FIGURE 3 — COUPLING THE MC1377 TO THE MC1374 RF MODULATOR

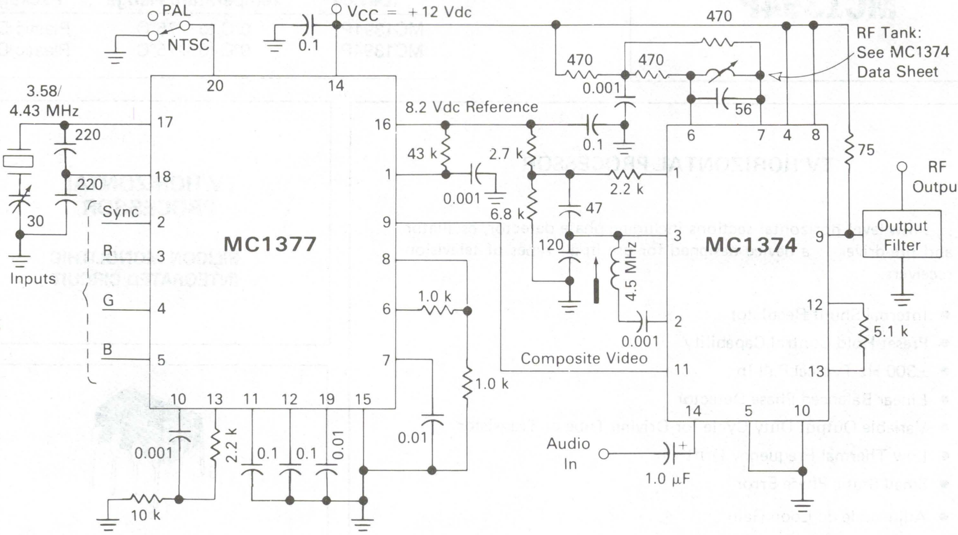

PAL
NTSC
VCC = +12 Vdc
0.1
470
470
470
0.001
RF Tank:
See MC1374
Data Sheet
56
3.58/
4.43 MHz
220
220
30
Inputs
Sync
R
G
B
MC1377
20
14
17
18
2
3
4
5
16
1
9
8
6
7
10
13
11
12
19
15
8.2 Vdc Reference
43 k
2.7 k
0.1
2.2 k
0.001
6.8 k
47
120
4.5 MHz
0.001
Composite Video
1.0 k
1.0 k
0.01
0.001
2.2 k
0.1
0.1
0.01
10 k
Audio
In
1.0 µF
MC1374
6
7
4
8
1
3
9
2
12
11
13
14
5
10
75
RF
Output
Output
Filter
5.1 k

FIGURE 4 — VECTORSCOPE DISPLAY OF 100% SATURATED NTSC COLOR BARS

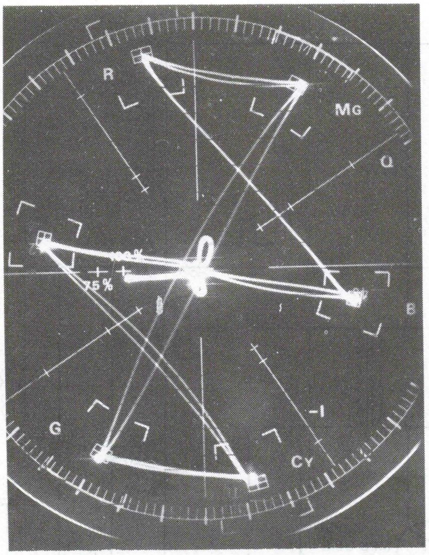
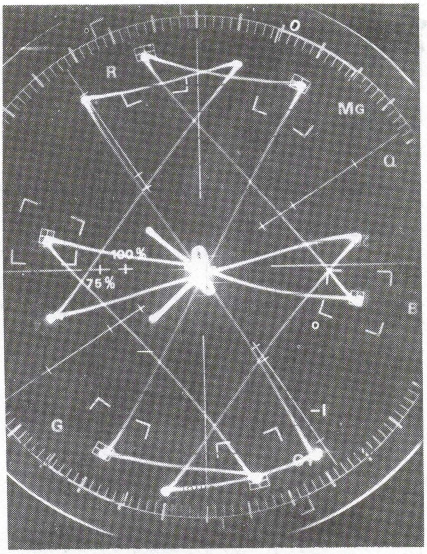

R
MG
Q
100%
75%
B
-I
G
CY

FIGURE 5 — 100% SATURATED PAL COLOR BARS ON NTSC VECTORSCOPE


R
MG
Q
100%
75%
B
-I
G
CY

MC1391P
MC1394P

ORDERING INFORMATION

Device	Temperature Range	Package
MC1391P	0°C to +75°C	Plastic DIP
MC1394P	0°C to +75°C	Plastic DIP

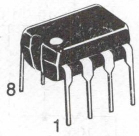
TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- MC1391P — Positive Flyback Inputs
- MC1394P — Negative Flyback Inputs

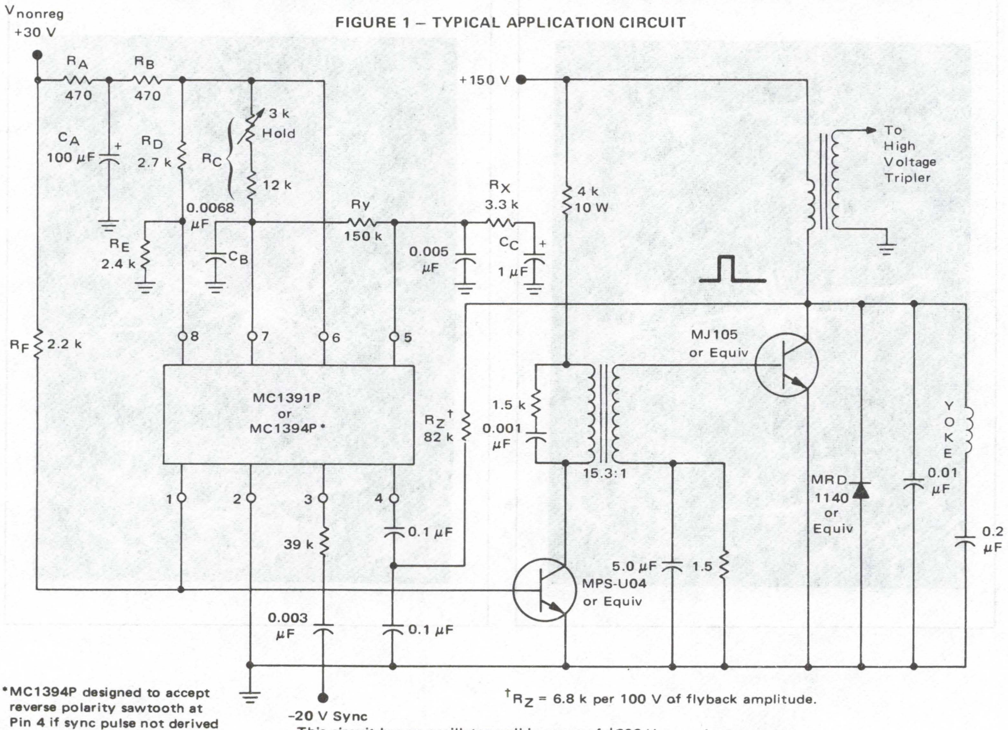
TV HORIZONTAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626-04

FIGURE 1 — TYPICAL APPLICATION CIRCUIT


Vnonreg
+30 V
RA
470
RB
470
CA
100 µF
+
RD
2.7 k
RC
3 k
Hold
12 k
0.0068 µF
RE
2.4 k
CB
Ry
150 k
RX
3.3 k
0.005 µF
CC
1 µF
+
+150 V
To High Voltage Tripler
4 k
10 W
RF
2.2 k
8
7
6
5
MC1391P or MC1394P*
RZ†
82 k
1.5 k
0.001 µF
15.3:1
MJ105 or Equiv
YOKE
MRD 1140 or Equiv
0.01 µF
0.2 µF
1
2
3
4
39 k
0.1 µF
5.0 µF
1.5
MPS-U04 or Equiv
0.003 µF
0.1 µF
-20 V Sync

*MC1394P designed to accept reverse polarity sawtooth at Pin 4 if sync pulse not derived from MJ105 collector.

†R_Z = 6.8 k per 100 V of flyback amplitude.

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p\text{-}p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p\text{-}p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above $T_A = +25^{\circ}C$	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	–65 to +150	°C

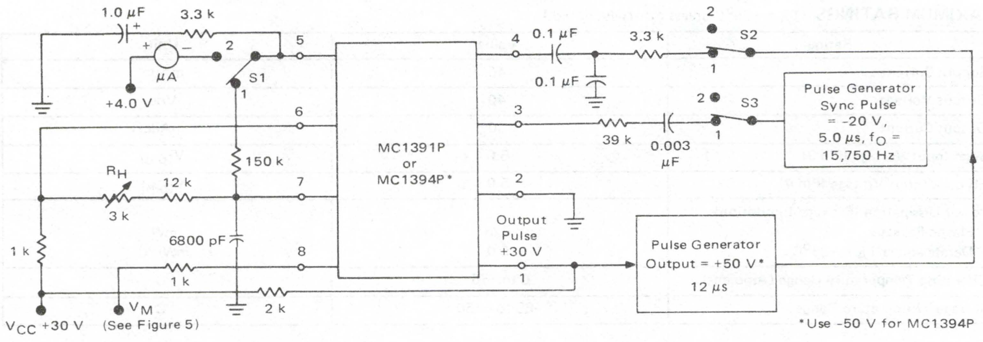
ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}C$ unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.0	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	µs
Free-running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	µA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V(p-p)

TYPICAL CHARACTERISTICS

($T_A = +25^oC$ unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT


1.0 µF
3.3 k
+
–
µA
+4.0 V
2
S1
1
5
4
0.1 µF
3.3 k
2
S2
1
0.1 µF
6
3
39 k
0.003 µF
2
S3
1
Pulse Generator
Sync Pulse
= –20 V,
5.0 µs, f$_O$ =
15,750 Hz
150 k
MC1391P
or
MC1394P*
R$_H$
12 k
3 k
7
2
Output
Pulse
+30 V
6800 pF
8
1
Pulse Generator
Output = +50 V*
12 µs
1 k
1 k
2 k
V$_M$
V$_{CC}$ +30 V
(See Figure 5)

*Use –50 V for MC1394P

FIGURE 3 – FREQUENCY versus TEMPERATURE

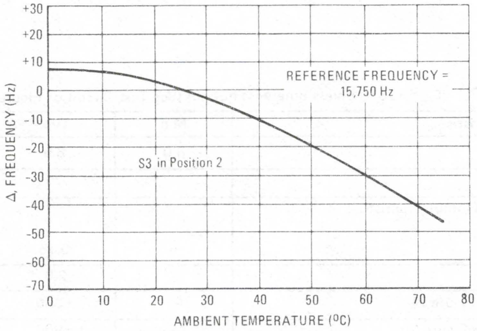


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

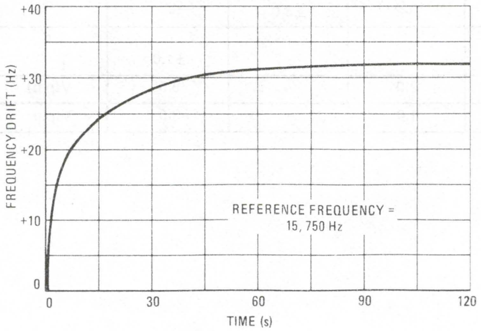


FIGURE 5 – MARK-SPACE RATIO

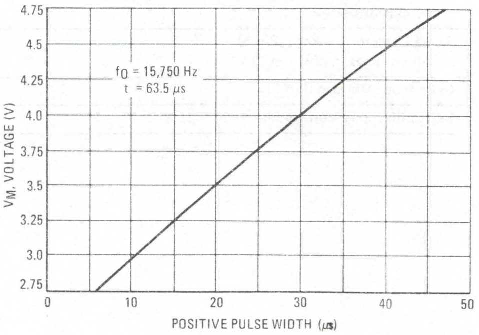
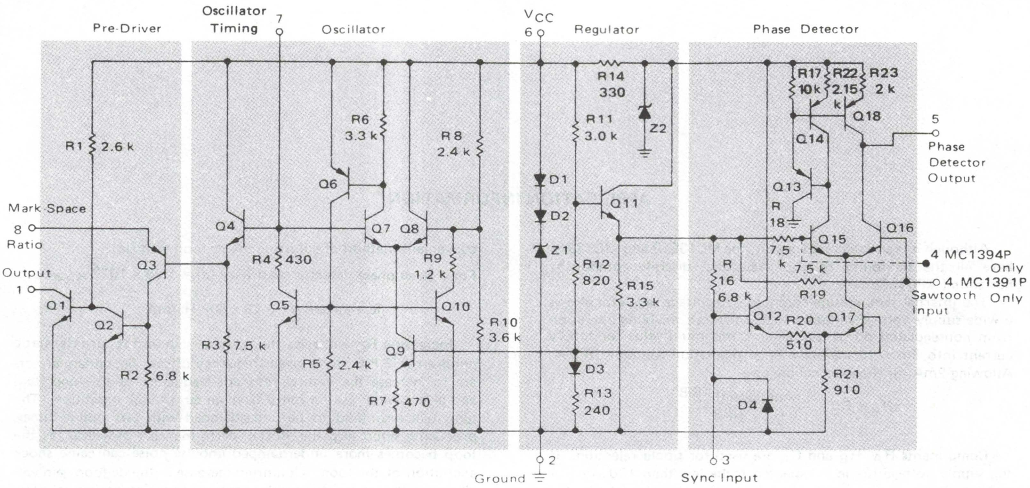


FIGURE 6 – CIRCUIT SCHEMATIC


Pre-Driver
Oscillator Timing
7
Oscillator
VCC
6
Regulator
Phase Detector
R1 2.6 k
Mark-Space
8
Ratio
Output
1
Q1
Q2
Q3
R2 6.8 k
Q4
R4 430
R3 7.5 k
Q5
R5 2.4 k
R6 3.3 k
Q6
Q7
Q8
R8 2.4 k
R9 1.2 k
Q10
R10 3.6 k
Q9
R7 470
D1
D2
Z1
R14 330
R11 3.0 k
Z2
Q11
R12 820
R15 3.3 k
D3
R13 240
2
Ground
R17 10k
R22 2.15 k
R23 2 k
Q18
5
Phase Detector Output
Q14
Q13
R 18
Q15
Q16
7.5 k
7.5 k
4 MC1394P Only
4 MC1391P Only
Sawtooth Input
R 16 6.8 k
R19
Q12
R20 510
Q17
R21 910
D4
3
Sync Input

CIRCUIT OPERATION

The MC1391P and MC1394P contain the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P and MC1394P have all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μs to 48 μs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 + \chi^2 T\omega_c}{4\chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1+\chi)\,T}} \qquad \omega_c = 2\pi fc$$

$$T = R_y C_C$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

where:

K = loop damping coefficient

MOTOROLA

MC3320P
MC3321P

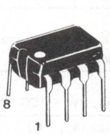
CLASS B AUDIO DRIVERS

. . . designed as preamplifiers and driver circuits for complementary output transistors.

- Driver for Auto Radios – and up to 10-Watt Amplifiers
- High Gain – 7.0 mV for 1.0 Watt, R_L = 3.2 Ohms
- High Input Impedance – 500-Kilohm Capability
- Output Biasing Diodes Included
- No Special h_{FE} Matching of Outputs Required
- Formerly MFC8020A and MFC8021A in Case 644A Package

CLASS B AUDIO DRIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

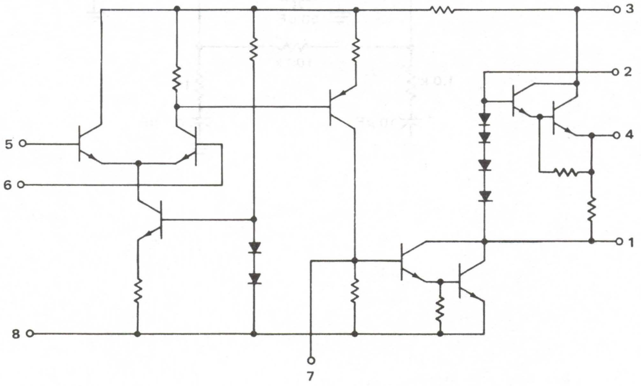


PLASTIC PACKAGE
CASE 626-04

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC3320P	MC3321P	Unit
Power Supply Voltage	V_{CC}	35	20	Vdc
Peak Output Current (Pins 4 and 1)	I_P	150		mA
Operating Ambient Temperature Range	T_A	-10 to +75		°C
Storage Temperature Range	T_{stg}	-55 to +125		°C
Junction Temperature	T_J	150		°C

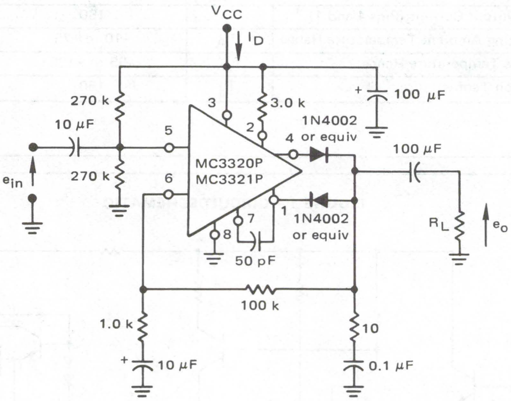
FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) (See Figure 2)

Characteristic		Min	Typ	Max	Unit
Drain Current (e_{in} = 0)					mA
(V_{CC} = 30 Vdc)	MC3320P	–	10	30	
(V_{CC} = 14 Vdc)	MC3321P	–	7.0	30	
Sensitivity (P_O = 1.0 Watt, f = 1.0 kHz)					mV
(e_o = 8.95 V(RMS), R_L = 165 Ω)	MC3320P	–	89	112	
(e_o = 3.2 V(RMS), R_L = 65 Ω)	MC3321P	–	32	40	
Total Harmonic Distortion (f = 1.0 kHz)					%
(V_{CC} = 30 V, e_o = 8.95 V(RMS), R_L = 165 Ω)	MC3320P	–	0.7	5.0	
(V_{CC} = 14 V, e_o = 3.2 V(RMS), R_L = 65 Ω)	MC3321P	–	1.0	5.0	
Open-Loop Gain					dB
(V_{CC} = 30 V, R_L = 165 Ω)	MC3320P	–	89	–	
(V_{CC} = 14 V, R_L = 65 Ω)	MC3321P	–	87	–	
Ripple Rejection (f = 60 Hz, A_v = 100, e_{in} = 0, Power Supply Ripple = 1.0 V(RMS)		–	27	–	dB
Equivalent Input Noise (e_{in} = 0, R_S = 1.0 kΩ, BW = 100 Hz – 10 Hz)		–	18	–	μV
Quiescent Output Voltage (e_{in} = 0)					Vdc
(V_{CC} = 30 V)	MC3320P	–	15	–	
(V_{CC} = 14 V)	MC3321P	–	7.0	–	

FIGURE 2 – TEST CIRCUIT

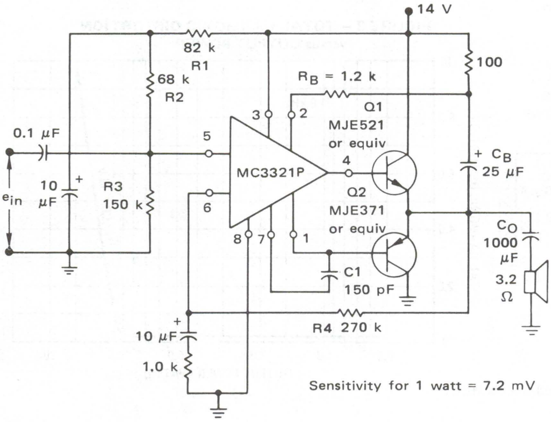


V_{CC}
I_D
270 k
10 μF
5
3
3.0 k
2
100 μF
1N4002
4 or equiv
100 μF
MC3320P
MC3321P
e_{in}
270 k
6
1
7
8
1N4002
or equiv
50 pF
R_L
e_o
100 k
1.0 k
10
10 μF
0.1 μF

TYPICAL AUTO RADIO AUDIO APPLICATIONS and CHARACTERISTICS

(T_A = +25° unless otherwise noted.)

FIGURE 3 – APPLICATION CIRCUIT FOR MC3321P*



Sensitivity for 1 watt = 7.2 mV

FIGURE 4–TOTAL HARMONIC DISTORTION versus OUTPUT POWER

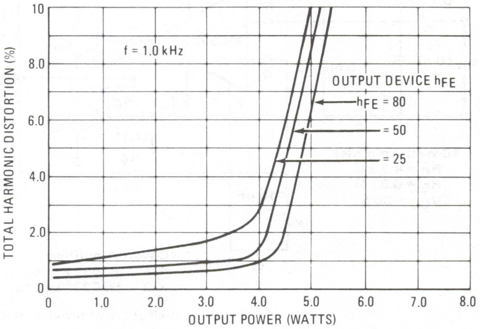


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY

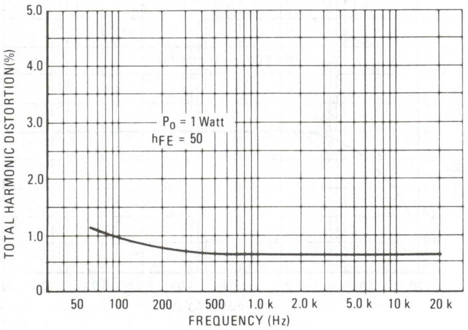
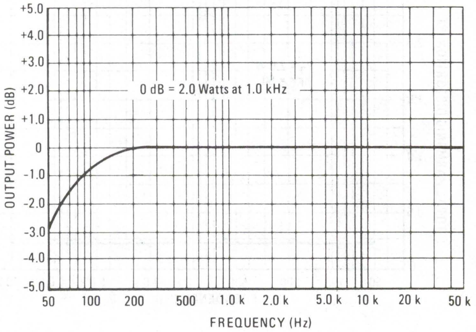


FIGURE 6 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MC3321P (AUTO RADIO AUDIO)

The MC3321P combines all the voltage gain required for an automotive radio audio amplifier into one package reducing the circuit-board area requirement. The circuit shown in Figure 3 has an input sensitivity of approximately 7.2 millivolts for a one-watt output. Sensitivity can be adjusted by changing the value of R_4. The circuit performance is a function of the output device h_{FE}, as shown in Figure 4. Figure 4 can be used to determine the minimum h_{FE} of the output transistors. The bandwidth of the amplifier is determined by the capacitor, C_1. If C_1 is increased to 390 pF the high frequency 3.0 dB point is typically 20 kHz.

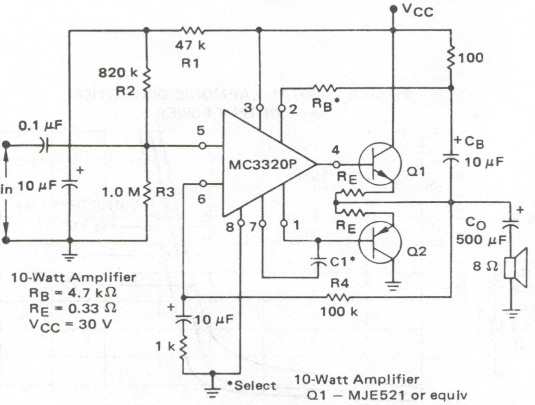
---

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

TYPICAL 10-WATT AMPLIFIER APPLICATION AND CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – APPLICATION CIRCUIT*



10-Watt Amplifier
R_B = 4.7 kΩ
R_E = 0.33 Ω
V_{CC} = 30 V

*Select

10-Watt Amplifier
Q1 – MJE521 or equiv
Q2 – MJE371 or equiv

(Select C1 to provide desired bandwidth.
C1 = 47 pF minimum)

FIGURE 8 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

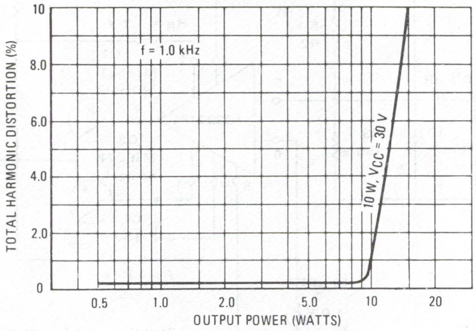


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY

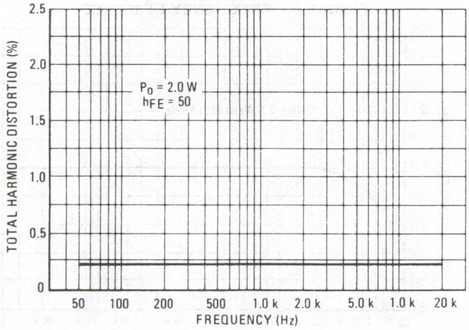
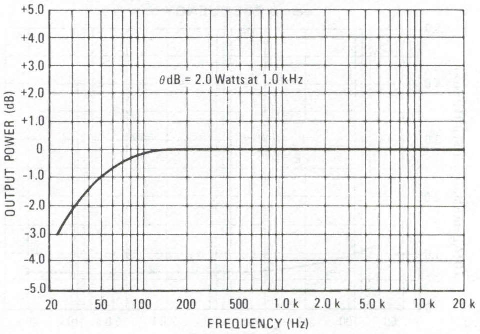


FIGURE 10 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MC3320P
(10 Watt Amplifiers)

The MC3320P is a high-voltage device capable of driving 10 Watt audio amplifiers. The gain of the circuit shown in Figure 7 changes when the value of R4 is varied and the bandwidth is determined by C1. Emitter resistors are required at the higher voltages used for 10 Watt audio amplifiers to provide thermal stability. The value of R_E is a function of the heatsink thermal resistance and supply voltage. The heatsink requirements for operation at +65°C (with both devices mounted on the same heatsink) is about 14°C/W for the 10-Watt amplifier. If the maximum ambient operating temperature is reduced then the heatsink can be reduced in size as calculated by

$$\theta SA = \frac{T_J - (\theta JS)\ P_D - T_A}{P_D}$$

where

θSA = Heatsink thermal resistance

T_J = Maximum junction operating temperature

θJS = Junction to heatsink thermal resistance (includes all surface interface components for thermal resistance such as the insulating washer)

P_D = Maximum power dissipation of transistors (This occurs at about 60% of maximum output power) 6.0 W for 10 W, 7.2 W for 12 W

T_A = Maximum ambient temperature

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

MOTOROLA

MC3325

Advance Information

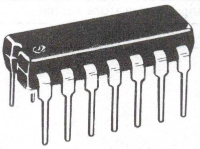
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

AUTOMOTIVE VOLTAGE REGULATOR

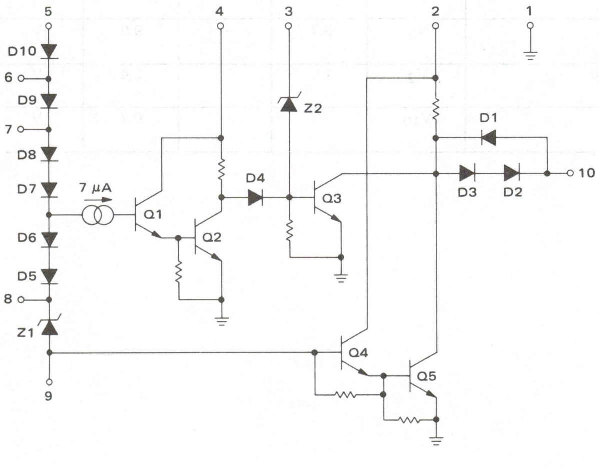
. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

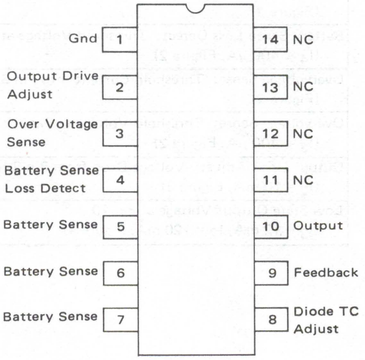


P SUFFIX
PLASTIC PACKAGE
CASE 646-05

CIRCUIT SCHEMATIC


5
4
3
2
1
D10
6
D9
7
D8
D7
7 μA
Q1
Q2
D6
D5
8
Z1
9
Z2
D4
Q3
D1
D3
D2
10
Q4
Q5

PIN CONNECTIONS


Gnd 1
Output Drive Adjust 2
Over Voltage Sense 3
Battery Sense Loss Detect 4
Battery Sense 5
Battery Sense 6
Battery Sense 7
14 NC
13 NC
12 NC
11 NC
10 Output
9 Feedback
8 Diode TC Adjust

ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5, 6, or 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7.9	–	8.95	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	–	13.3	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	–	12.75	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	–	11.9	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	–	–	600	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 400$ μA, Figure 2)	V_4	1.3	–	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	–	–	600	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 400$ μA, Figure 2)	V_3	6.7	–	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 ($I_2 = 10$ mA, Figure 3)	V_2	1.9	–	2.4	V
Low State Output Voltage at Pin 10 ($I_3 = 12$ mA, $I_2 = 120$ mA, Figure 4)	V_{10}	–	–	0.7	V

TEST CIRCUITS

FIGURE 1

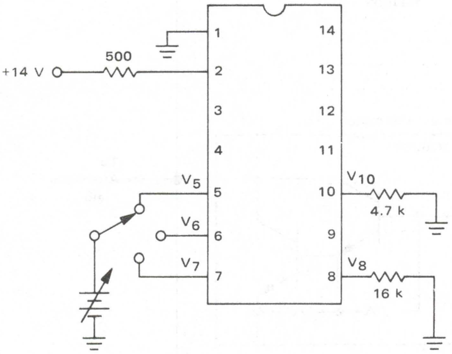

+14 V
500
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V$_5$
V$_6$
V$_7$
V$_{10}$
4.7 k
V$_8$
16 k

FIGURE 2

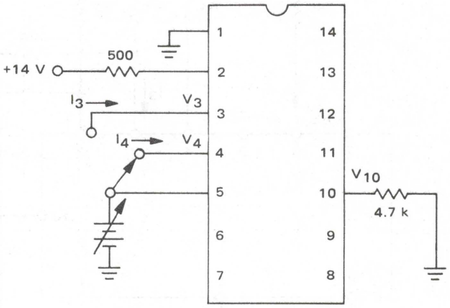

+14 V
500
I$_3$
V$_3$
I$_4$
V$_4$
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V$_{10}$
4.7 k

FIGURE 3

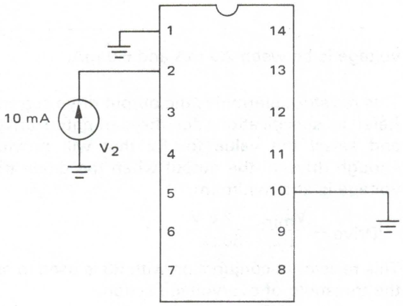

10 mA
V$_2$
1
2
3
4
5
6
7
14
13
12
11
10
9
8

FIGURE 4

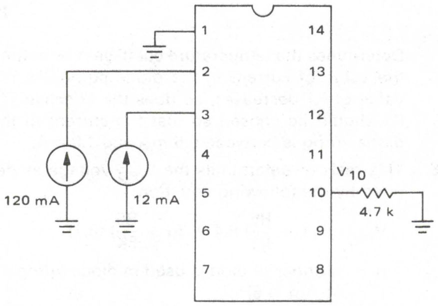
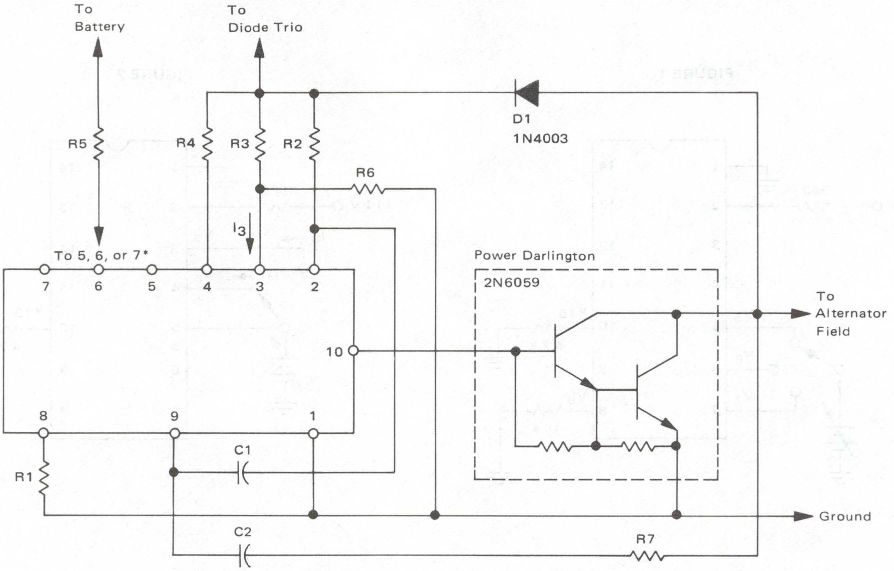

120 mA
12 mA
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V$_{10}$
4.7 k

FIGURE 5 – APPLICATION CIRCUIT



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is −2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have −2.0 mV for Q5, −2.0 mV for Q4, +3.0 mV for Z1, −8.0 mV for D5 thru D8, and an additional −2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately −9.0 mV/°C to −13 mV/°C depending on the number of the diodes in the diode string that are utilized.

APPLICATIONS CIRCUIT INFORMATION

(See Figure 5)

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as defined by the following equation:

$$V_{reg} = (1 + \frac{R5}{R1})\,8.4 + (n + \frac{R5}{5K})\,(0.7)$$

n = number of diodes used in diode string ($4 \leq n \leq 6$)

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the threshold of overvoltage action.

$$\text{Threshold} \cong \frac{R3 + R6}{R6}\,(7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

C1, C2 Used for compensation (Approximately 0.01 μF)

MOTOROLA

MC3334P
MCC3334
MCCF3334

Advance Information

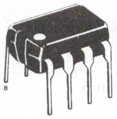
HIGH ENERGY IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH ENERGY IGNITION CIRCUIT

. . . designed to use the signal from a reluctor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0–24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts To Produce Optimum Stored Energy Without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip Chip Form
- Transient Protected Inputs and Outputs

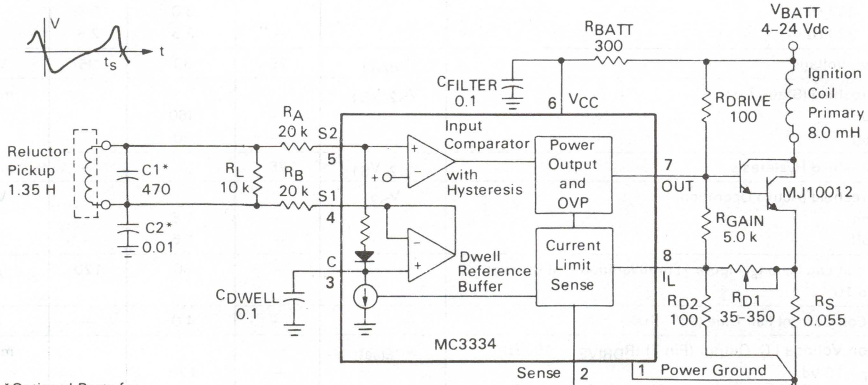


P SUFFIX
PLASTIC PACKAGE
CASE 626-04

ORDERING INFORMATION

Device	Temperature Range	Package
MC3334P	−40 to +125	Plastic DIP
MCC3334	−40 to +125	Chip
MCCF3334	−40 to +125	Flip-Chip

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION


V
t
t_S
Reluctor Pickup 1.35 H
C1* 470
C2* 0.01
R_L 10 k
R_A 20 k
R_B 20 k
S2
S1
5
4
C
3
C_{DWELL} 0.1
C_{FILTER} 0.1
R_{BATT} 300
6
V_{CC}
Input Comparator with Hysteresis
Dwell Reference Buffer
Power Output and OVP
Current Limit Sense
7
OUT
8
I_L
MC3334
Sense Ground
2
1
Power Ground
V_{BATT} 4–24 Vdc
Ignition Coil Primary 8.0 mH
R_{DRIVE} 100
MJ10012
R_{GAIN} 5.0 k
R_{D2} 100
R_{D1} 35–350
R_S 0.055

*Optional Parts for Extended Transient Protection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage - Steady State Transient 300 ms or less	V_{BATT}	24 90	Volts
Output Sink Current - Steady State Transient 300 ms or less	I_{out}	300 1.0	mA Amps
Junction Temperature	$T_{J(max)}$	150	°C
Operating Temperature Range	T_{amb}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation, Package Derate above 25°C	P_D	1.25 10	Watts mW/°C

ELECTRICAL CHARACTERISTICS (T_{amb} = -40 to +125°C, V_{BATT} = 13.2 Vdc, circuit of Figure 1, unless noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Supply Voltage, Pin 6	V_{CC}				Vdc
V_{BATT} = 4.0 Vdc		—	3.5	—	
8.0 Vdc		—	7.2	—	
12.0		—	10.4	—	
14.0		—	11.8	—	
Ignition Coil Current Peak, Cranking RPM 2.0 - 27 Hz	$I_{o(pk)}$				A pk
V_{BATT} = 4.0 Vdc		3.0	3.4	—	
6.0		4.0	5.2	—	
8.0		4.6	5.3	—	
10.0		5.1	5.4	—	
Ignition Coil Current Peak, Normal RPM	$I_{o(pk)}$				A pk
Freq. = 33 Hz		5.1	5.5	—	
133 Hz		5.1	5.5	—	
200 Hz		4.2	5.4	—	
267 Hz		3.4	4.4	—	
333 Hz		2.7	3.4	—	
Ignition Coil On-Time, Normal RPM Range	t_{on}				ms
Freq. = 33 Hz		—	7.5	14.0	
133 Hz		—	5.0	5.9	
200 Hz		—	4.0	4.6	
267 Hz		—	3.0	3.6	
333 Hz		—	2.3	2.8	
Shutdown Voltage	V_{BATT}	25	30	35	Vdc
Input Threshold (Static Test)	V_{S2}-V_{S1}				mVdc
Turn-on		—	360	—	
Turn-off		—	90	—	
Input Threshold Hysteresis	V_{S2}-V_{S1}	75	—	—	mVdc
Input Threshold (Active Operation)	V_{S2}				Vdc
Turn-on		—	1.8	—	
Turn-off		—	1.5	—	
Total Circuit Lag from t_s (Figure 1) until Ignition Coil Current Falls to 10%		—	60	120	µs
Ignition Coil Current Fall Time (90%-10%)		—	4.0	—	µs
Saturation Voltage I.C. Output (Pin 7) (R_{DRIVE} = 100 Ω)	$V_{CE(sat)}$				mVdc
V_{BATT} = 10 Vdc		—	120	—	
30 Vdc		—	280	—	
50 Vdc		—	540	—	
Current Limit Reference, Pin 8	V_{ref}	120	160	190	mVdc

The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned out to permit thick film or printed circuit module design without any crossovers.

CIRCUIT DESCRIPTION

The basic function of an ignition circuit is to permit build-up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable dc voltage reference, stored on C_{DWELL}, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output "off" for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by V_{BATT} and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by R_S and set by R_{D1}, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower V_{BATT}, the "on" period automatically stretches to accommodate the slower current build-up. At very low V_{BATT} and low RPM, a common condition during cold starting, the "on" period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at $V_{BATT} \approx 30$ V ($V_{CC} \approx 22$ V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive V_{BATT}.

COMPONENT VALUES

PICKUP	— series resistance = 800 Ω ± 10% @ 25°C inductance = 1.35 H @ 1.0 kHz @ 15 Vrms.
COIL	— leakage L = 0.6 mH primary R = 0.43 Ω ± 5% @ 25°C primary L = 7.5 to 8.5 mH @ 5.0 A
R_L	— load resistor for pick-up = 10 kΩ ± 20%
R_A, R_B	— input buffer resistors, provide additional transient protection to the already clamped inputs = 20 k ± 20%
C1, C2	— for reduction of high frequency noise and spark transients induced in pick-up and leads; optional and non-critical
R_{BATT}	— provides load dump protection (but small enough to allow operation at V_{BATT} = 4.0 V) = 300 Ω ± 20%
C_{FILTER}	— transient filter on V_{CC}, non-critical
C_{DWELL}	— stores reference, circuit designed for 0.1 μF ± 20%
R_{GAIN}	— R_{GAIN}/R_{D1} sets the dc gain of the current regulator = 5.0 k ± 20%
R_{D2}	— R_{D2}/R_{D1} set up voltage feedback from R_S
R_S	— sense resistor (PdAg in thick film techniques) = 0.055 Ω ± 50%
R_{DRIVE}	— low enough to supply drive to the output Darlington, high enough to keep $V_{CE(sat)}$ of the IC below Darlington turn-on during load dump = 100 Ω ± 20%, 5.0 W
R_{D1}	— starting with 35 Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$R_{D1} = \frac{I_{o(pk)}\,R_S - V_{ref}}{\dfrac{V_{ref}}{R_{D2}} - \dfrac{1.4}{R_{GAIN}}} \approx 100\ \Omega\ \text{(nom)}$$

FIGURE 2 — IGNITION COIL CURRENT versus FREQUENCY/PERIOD

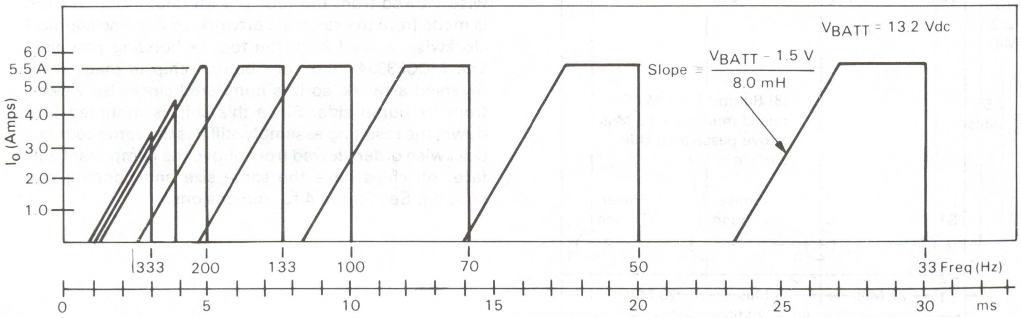


FIGURE 3 — INTERNAL SCHEMATIC

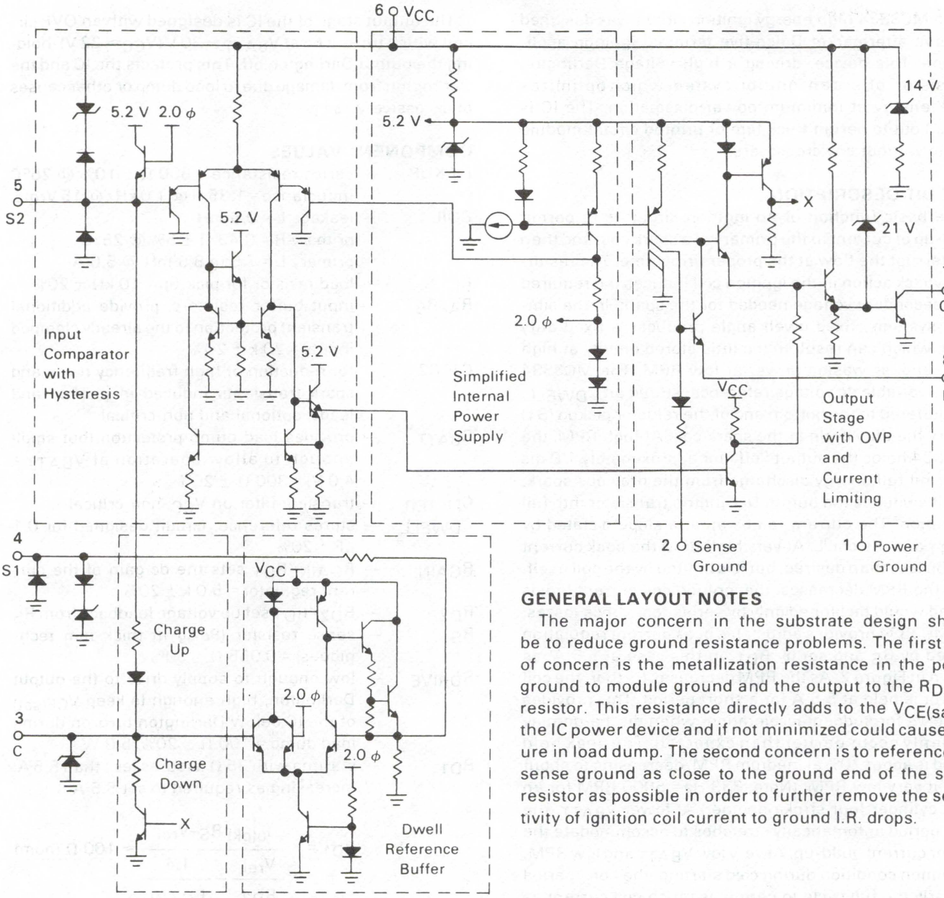
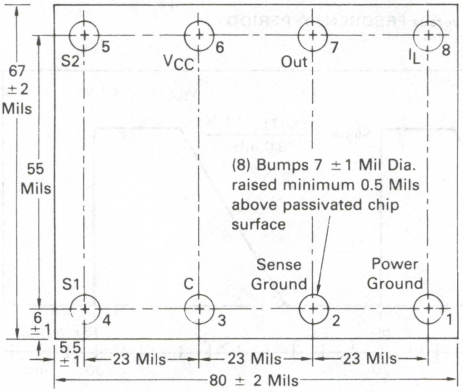

6 VCC
5.2 V
2.0 ϕ
5
S2
5.2 V
Input
Comparator
with
Hysteresis
5.2 V
5.2 V
Simplified
Internal
Power
Supply
2.0 ϕ
14 V
X
21 V
7
Out
8
IL
VCC
Output
Stage
with OVP
and
Current
Limiting
2 Sense Ground
1 Power Ground
4
S1
VCC
Charge
Up
3
C
Charge
Down
X
2.0 ϕ
2.0 ϕ
Dwell
Reference
Buffer

FIGURE 4 — MCCF3334 IGNITION CIRCUIT BUMP SIDE VIEW


5
S2
6
VCC
Out
7
IL
8
67 ±2 Mils
55 Mils
(8) Bumps 7 ±1 Mil Dia. raised minimum 0.5 Mils above passivated chip surface
S1
C
Sense Ground
Power Ground
4
3
2
1
6 ±1
5.5 ±1
23 Mils
23 Mils
23 Mils
80 ± 2 Mils

GENERAL LAYOUT NOTES

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the R_{DRIVE} resistor. This resistance directly adds to the $V_{CE(sat)}$ of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pinout order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross-overs. The standard MC3334 plastic device is numbered in the industry convention, counter-clockwise viewed from the top. The MCC3334 chip version is made from the same die artwork, so it is also counter-clockwise viewed from the top, or bonding pad side. The MCCF3334 "flip" or "bump" chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter-clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

MC3340P

ELECTRONIC ATTENUATOR

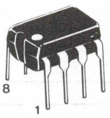
SILICON MONOLITHIC INTEGRATED CIRCUIT

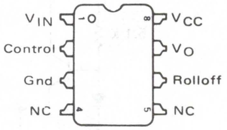
ORDERING INFORMATION

Device	Temperature Range	Package
MC3340P	0°C to +75°C	Plastic DIP

ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual In-Line Package
- Formerly MFC6040 in Case 643A Package



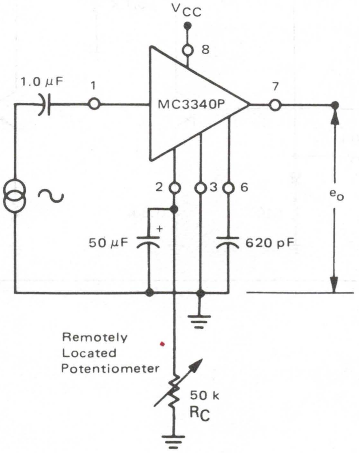

V_{IN}
Control
Gnd
NC
V_{CC}
V_O
Rolloff
NC
1
4
5
8

PLASTIC PACKAGE
CASE 626-04

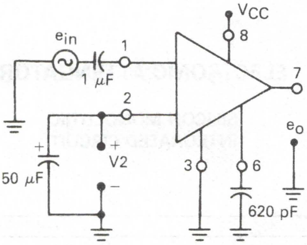
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	20	Vdc
Power Dissipation @ T_A = 25°C Derate above T_A = 25°C	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	0 to +75	°C

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL

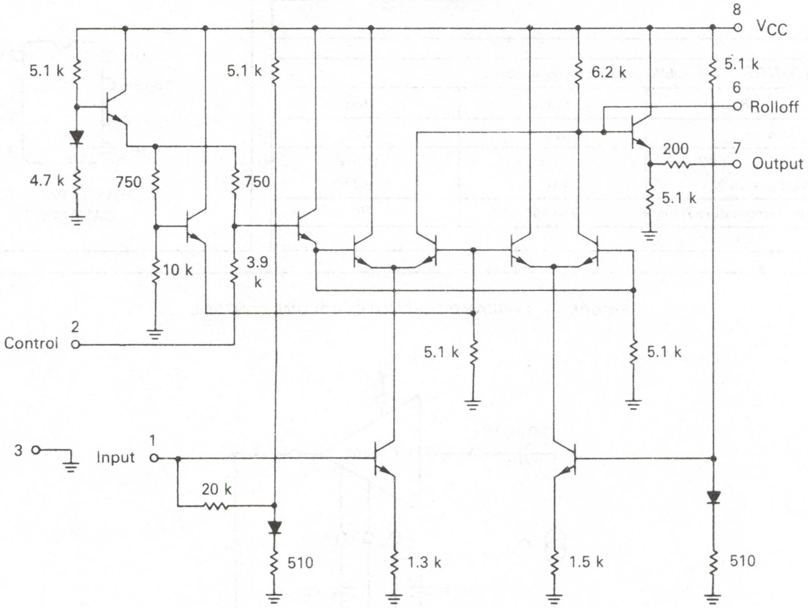

V_{CC}
8
1.0 μF
1
MC3340P
7
2
3
6
e_o
50 μF
+
620 pF
Remotely Located Potentiometer
50 k
R_C

ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV (RMS), f = 1.0 kHz, V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	8.0	—	18	Vdc
	Control Terminal Sink Current, Pin 2 (e_{in} = 0)	—	—	2.0	mAdc
	Maximum Input Voltage	—	—	0.5	V(RMS)
	Voltage Gain	11	13	—	dB
	Attenuation Range (V2 = 6.5 Vdc)	70	80	—	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mV (RMS), e_o = A_v x e_{in})	—	0.6	1.0	%

VCC
8
ein
1
1 μF
7
2
eo
+
50 μF
+
V2
−
3
6
620 pF

FIGURE 2 — CIRCUIT SCHEMATIC



8
VCC
5.1 k
5.1 k
6.2 k
5.1 k
6
Rolloff
200
7
Output
4.7 k
750
750
5.1 k
10 k
3.9 k
2
Control
5.1 k
5.1 k
3
1
Input
20 k
510
1.3 k
1.5 k
510

TYPICAL ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

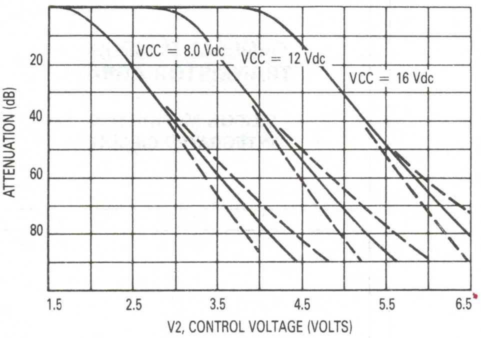


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

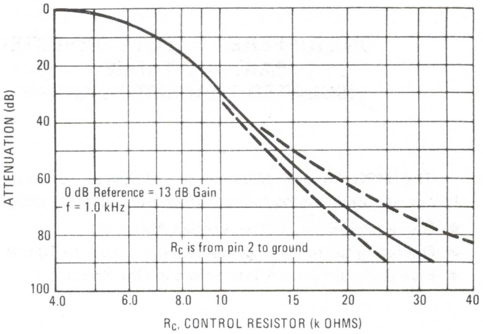


FIGURE 5 – FREQUENCY RESPONSE

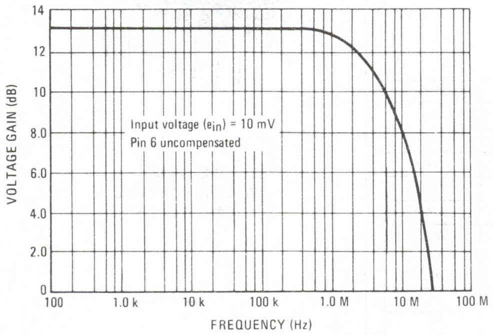


FIGURE 6 – OUTPUT VOLTAGE SWING

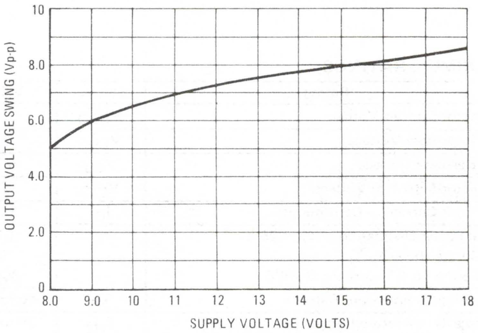
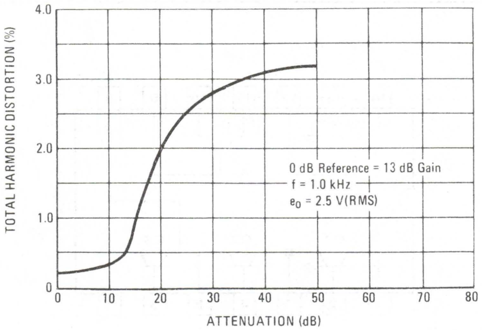


FIGURE 7 – TOTAL HARMONIC DISTORTION



MC3346
MC3386

ORDERING INFORMATION

Device	Temperature Range	Package
MC3346P	−40°C to +85°C	Plastic DIP
MC3386P	−40°C to +85°C	Plastic DIP

ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 and MC3386 are designed for general-purpose, low power applications for consumer and industrial designs.

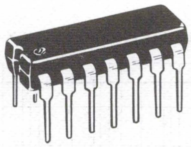
- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified — 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

GENERAL PURPOSE TRANSISTOR ARRAY

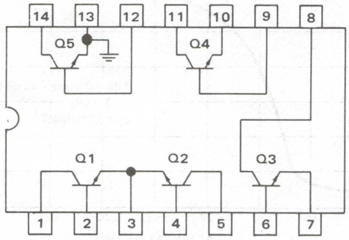
SILICON MONOLITHIC INTEGRATED CIRCUIT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/°C mW/°C
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C



P SUFFIX
PLASTIC PACKAGE
CASE 646-05



Pin 13 is connected to substrate

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3346P			MC3386P			Unit
		Min	Typ	Max	Min	Typ	Max	
STATIC CHARACTERISTICS								
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	20	60	–	20	60	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	15	–	–	15	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	60	–	20	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	$V_{(BR)EBO}$	5.0	7.0	–	5.0	7.0	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	40	–	–	100	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc) (I_C = 10 μAdc, V_{CE} = 3.0 Vdc)	h_{FE}	 – 40 –	 140 130 60	 – – –	 – 40 –	 – 130 –	 – – –	–
Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc) (V_{CE} = 3.0 Vdc, I_E = 10 mAdc)	V_{BE}	 – –	 0.72 0.80	 – –	 – –	 0.72 0.80	 – –	Vdc
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\|I_{IO1}-I_{IO2}\|$	–	0.3	2.0	–	0.3	–	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	–	–	0.5	5.0	–	0.5	–	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	–	-1.9	–	–	-1.9	–	mV/°C
Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$	–	1.0	–	–	1.0	–	μV/°C
Collector-Emitter Cutoff Current (V_{CE} = 10 Vdc, 1_B = 0)	I_{CEO}	–	–	0.5	–	–	5.0	μAdc
DYNAMIC CHARACTERISTICS								
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	–	3.25	–	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	–	110	–	–	110	–	–
Short-Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	–	3.5	–	–	3.5	–	kΩ
Open-Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	–	15.6	–	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	–	1.8	–	–	1.8	–	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	–	31–j1.5	–	–	31–j1.5	–	–
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	–	0.3+j0.04	–	–	0.3+j0.04	–	–
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	–	0.001+j0.03	–	–	0.001+j0.03	–	–
Current-Gain – Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	–	–	550	–	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	–	0.6	–	–	0.6	–	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	–	0.58	–	–	0.58	–	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	–	2.8	–	–	2.8	–	pF

TYPICAL CHARACTERISTICS

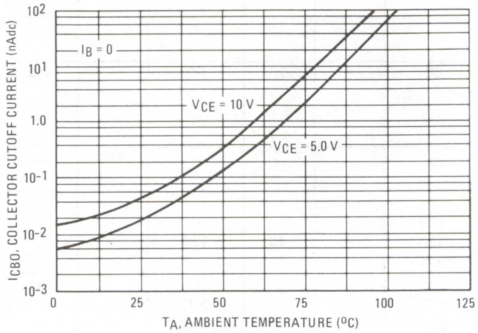


FIGURE 1 — COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

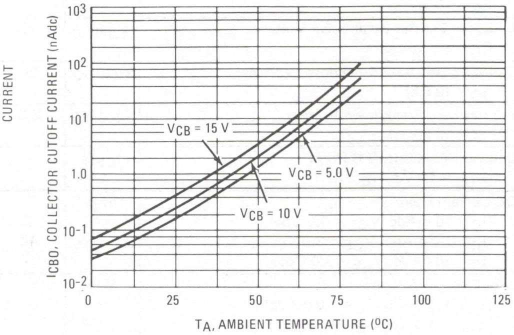


FIGURE 2 — COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

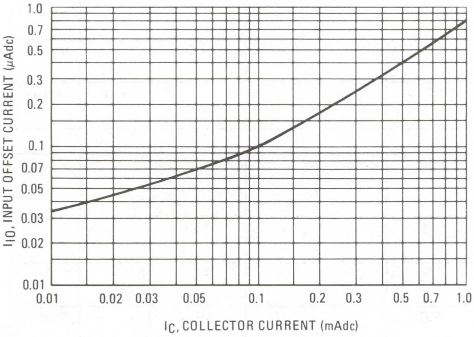


FIGURE 3 — INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2

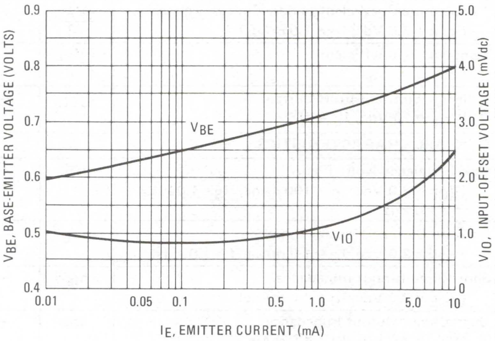


FIGURE 4 — BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS

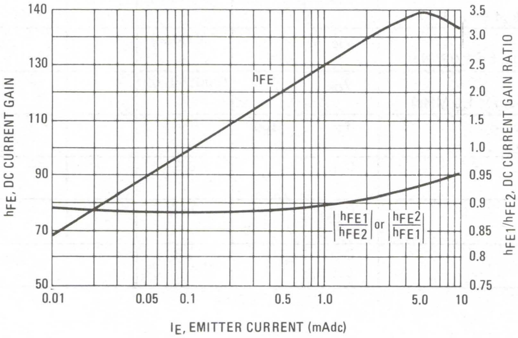


FIGURE 5 — DC CURRENT GAIN

MOTOROLA

MC3350

Advance Information

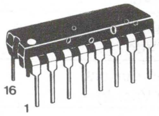
GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT

TRIPLE INDEPENDENT DIFFERENTIAL AMPLIFIER

The MC3350 consists of three independent differential amplifiers on a common monolithic substrate. The construction technique provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in multiple channel applications.

- Three Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Useful from dc to 120 MHz
- Economical Configuration



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

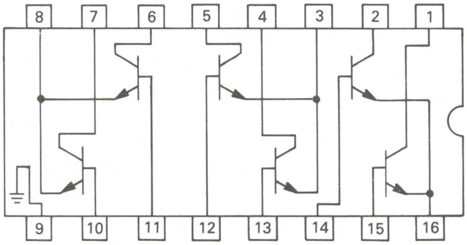
MAXIMUM RATINGS

Rating		Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	40	Vdc
Collector Current — Continuous	I_C	50	mAdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC3350P	0 to 70°C	Plastic DIP

PIN CONNECTIONS



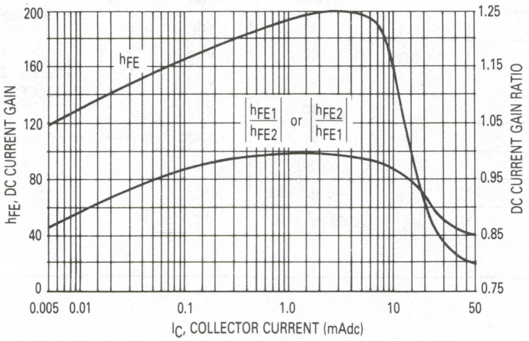
Pin 9 is connected to substrate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER					
Input Offset Voltage V_{CE} = 2.0 Vdc; I_C = 1.0 mAdc	V_{IO}	—	—	5.0	mVdc
STATIC CHARACTERISTICS FOR EACH TRANSISTOR					
Collector-Emitter Breakdown Voltage I_C = 5.0 mAdc	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Cutoff Current V_{CE} = 25 Vdc	I_{CES}	—	—	100	nAdc
Emitter Cutoff Current V_{EB} = 5.0 Vdc; I_C = 0	I_{EBO}	—	—	100	nAdc
DC Current Gain (V_{CE} = 2.0 Vdc)	h_{FE}				—
I_C = 100 μAdc		30	165	—	
I_C = 10 mAdc		75	140	—	

FIGURE 1 — DC CURRENT GAIN AND RATIO versus COLLECTOR CURRENT



MOTOROLA

MC3356

Advance Information

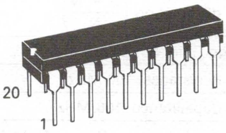
WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

WIDEBAND
FSK
RECEIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

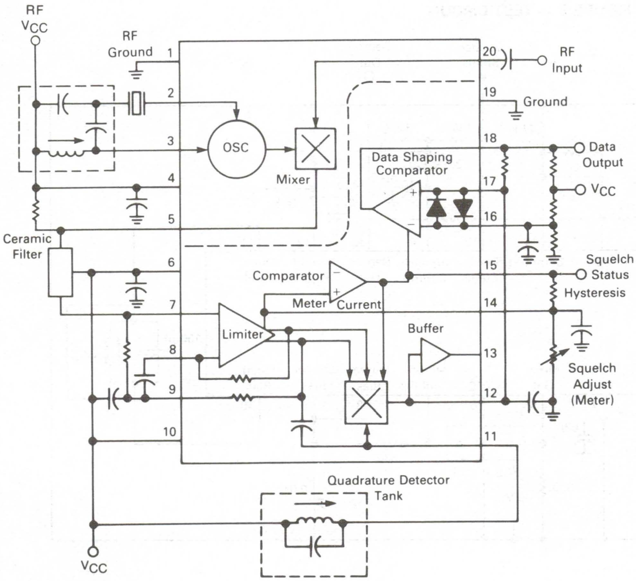
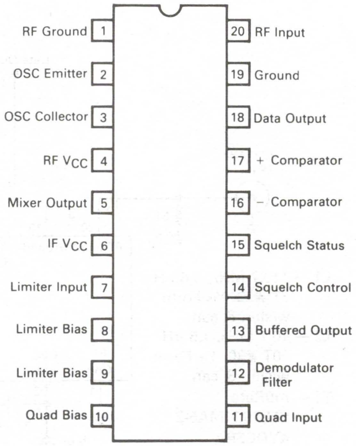

RF
VCC
RF
Ground
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
RF
Input
Ground
OSC
Mixer
Data Shaping
Comparator
Data
Output
VCC
Ceramic
Filter
Squelch
Status
Comparator
Meter
Current
Hysteresis
Limiter
Buffer
Squelch
Adjust
(Meter)
Quadrature Detector
Tank
VCC

FIGURE 2 — PIN CONNECTIONS


RF Ground 1
OSC Emitter 2
OSC Collector 3
RF VCC 4
Mixer Output 5
IF VCC 6
Limiter Input 7
Limiter Bias 8
Limiter Bias 9
Quad Bias 10
20 RF Input
19 Ground
18 Data Output
17 + Comparator
16 − Comparator
15 Squelch Status
14 Squelch Control
13 Buffered Output
12 Demodulator Filter
11 Quad Input

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

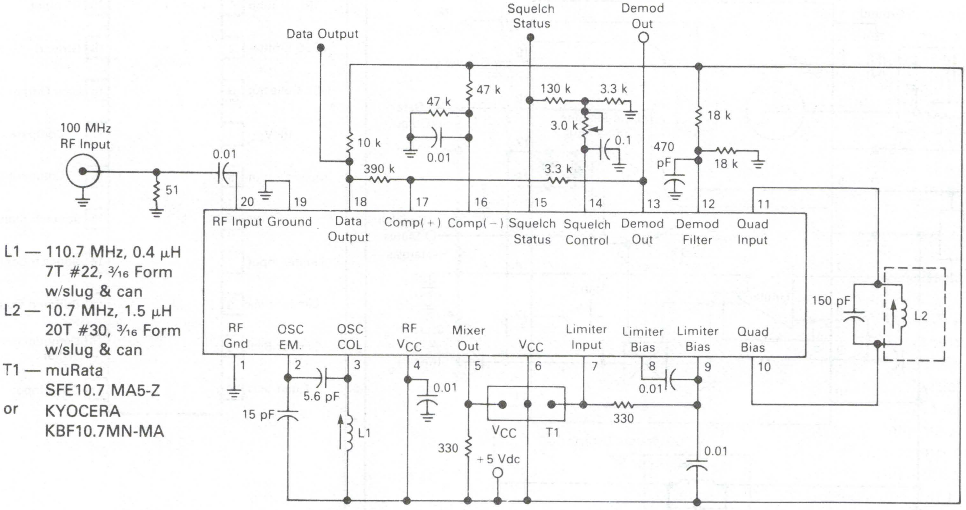
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating R.F. Supply Voltage Range (Pin 4)	R.F. V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for −3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	—	—	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	0.2 to 150	—	MHz
IF/Quadrature Detector Frequency Range (Note 1)	0.2	0.2 to 50	—	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	μA/dB
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

FIGURE 3 — TEST CIRCUIT


Squelch Status
Demod Out
Data Output
47 k
130 k
3.3 k
47 k
3.0 k
18 k
100 MHz RF Input
10 k
0.01
0.1
470 pF
0.01
390 k
3.3 k
18 k
51
20
19
18
17
16
15
14
13
12
11
RF Input Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
150 pF
L2
RF Gnd
OSC EM.
OSC COL
RF VCC
Mixer Out
VCC
Limiter Input
Limiter Bias
Limiter Bias
Quad Bias
1
2
3
4
5
6
7
8
9
10
5.6 pF
0.01
0.01
15 pF
L1
VCC
T1
330
330
+5 Vdc
0.01

L1 — 110.7 MHz, 0.4 μH
7T #22, 3/16 Form
w/slug & can

L2 — 10.7 MHz, 1.5 μH
20T #30, 3/16 Form
w/slug & can

T1 — muRata
SFE10.7 MA5-Z
or KYOCERA
KBF10.7MN-MA

FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

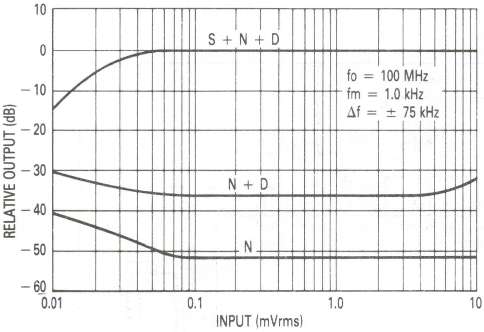
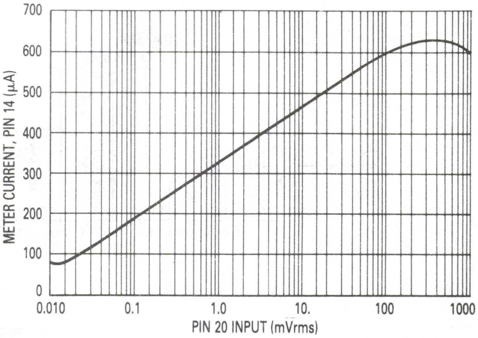


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



General Description

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

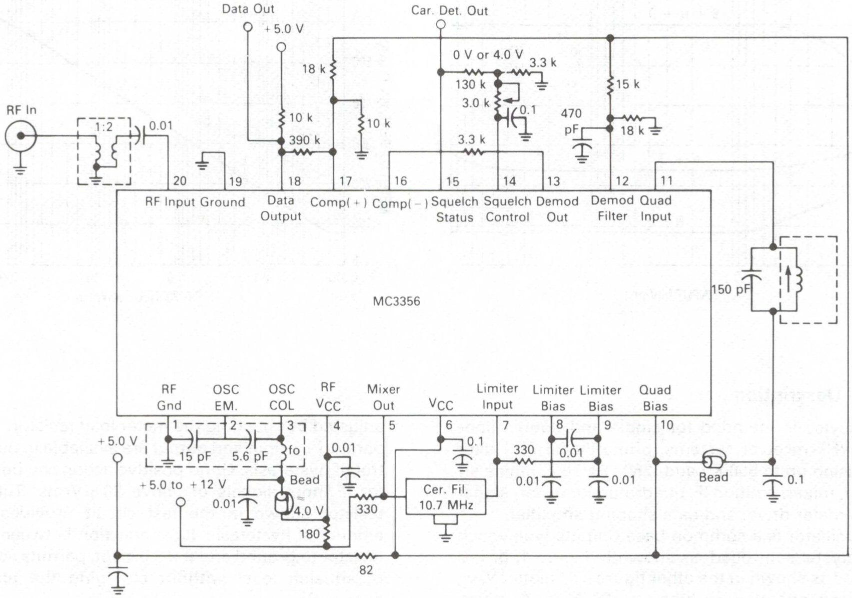
A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER


Data Out
+5.0 V
Car. Det. Out
18 k
0 V or 4.0 V
3.3 k
130 k
3.0 k
0.1
15 k
470 pF
18 k
10 k
10 k
390 k
3.3 k
RF In
1:2
0.01
20
19
18
17
16
15
14
13
12
11
RF Input Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
150 pF
MC3356
RF Gnd
OSC EM.
OSC COL
RF VCC
Mixer Out
VCC
Limiter Input
Limiter Bias
Limiter Bias
Quad Bias
1
2
3
4
5
6
7
8
9
10
+5.0 V
15 pF
5.6 pF
fo
0.01
Bead
+5.0 to +12 V
0.01
4.0 V
330
Cer. Fil. 10.7 MHz
0.1
330
0.01
0.01
0.01
Bead
0.1
180
82

Application Notes

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

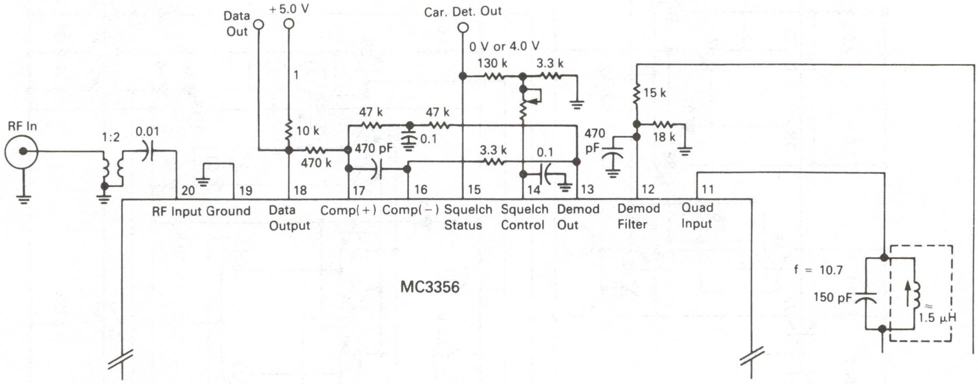
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has separate V_{CC}'s and grounds for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of figures 1 and 3 have RF, oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a *separate* path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 µV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 µV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER

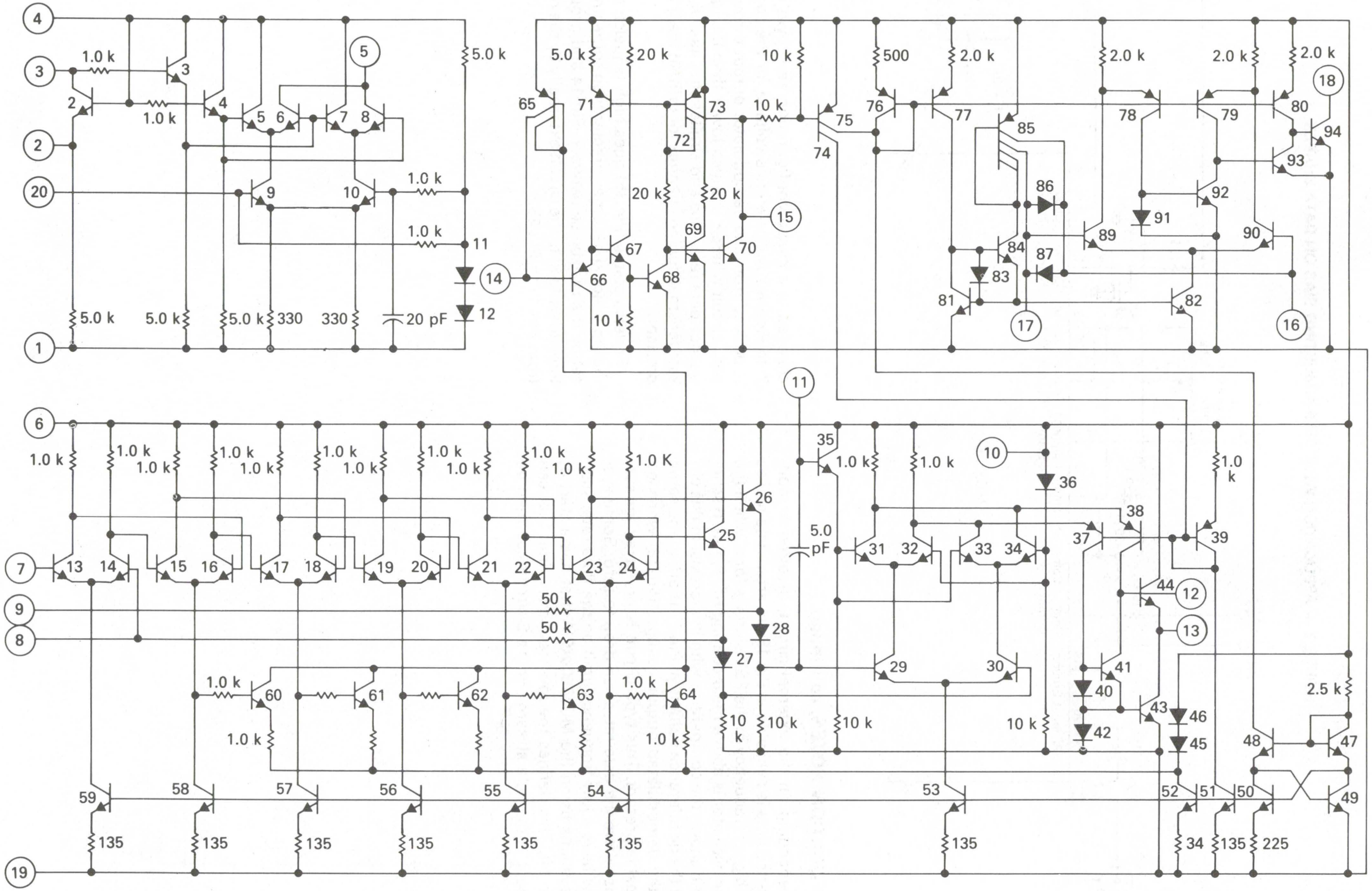

Data Out
+5.0 V
Car. Det. Out
0 V or 4.0 V
130 k
3.3 k
1
15 k
47 k
47 k
RF In
1:2
0.01
10 k
0.1
470 pF
470 k
3.3 k
0.1
470 pF
18 k
20
19
18
17
16
15
14
13
12
11
RF Input Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
MC3356
f = 10.7
150 pF
≈ 1.5 μH

APPLICATION NOTES, continued

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

FIGURE 8 — INTERNAL SCHEMATIC


4
3
2
20
1
5
6
7
9
8
19
10
11
12
13
14
15
16
17
18
1.0 k
5.0 k
330
20 pF
20 k
10 k
500
2.0 k
2.5 k
1.0 K
50 k
5.0 pF
135
34
225

MOTOROLA

MC3357

Advance Information

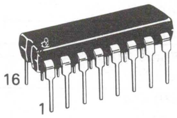
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage —
  (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

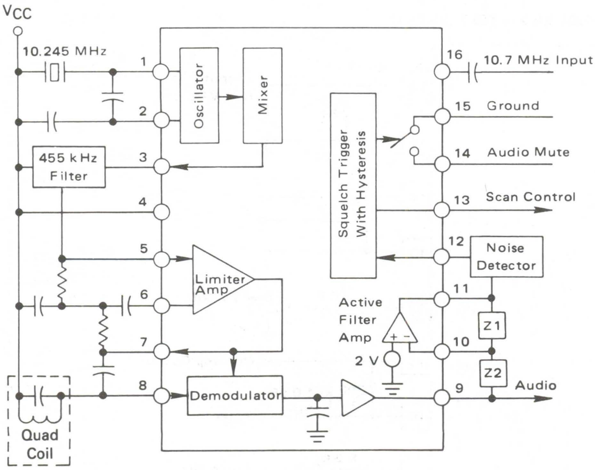
LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

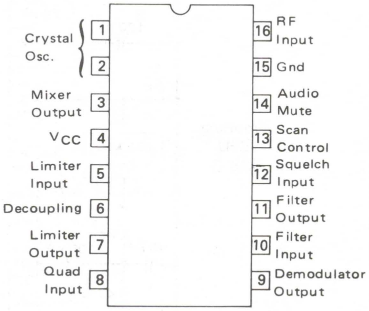


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM


VCC
10.245 MHz
1
2
3
4
5
6
7
8
455 kHz Filter
Oscillator
Mixer
Limiter Amp
Demodulator
Quad Coil
Squelch Trigger With Hysteresis
Active Filter Amp
2 V
Noise Detector
Z1
Z2
16
10.7 MHz Input
15
Ground
14
Audio Mute
13
Scan Control
12
11
10
9
Audio

PIN CONNECTIONS


Crystal Osc.
1
2
Mixer Output
3
VCC
4
Limiter Input
5
Decoupling
6
Limiter Output
7
Quad Input
8
RF Input
16
Gnd
15
Audio Mute
14
Scan Control
13
Squelch Input
12
Filter Output
11
Filter Input
10
Demodulator Output
9

This document contains information on a new product. Specifications and information herein are subject to change without notice.

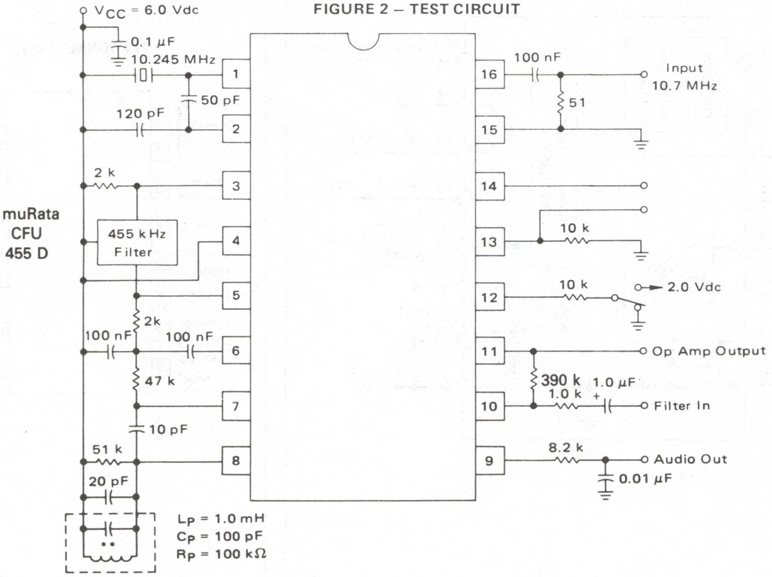
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage ($V_{CC} \geq 6.0$ Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	–30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		–	2.0	–	
Squelch On		–	3.0	5.0	
Input Limiting Voltage (–3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 — TEST CIRCUIT


V_{CC} = 6.0 Vdc
0.1 μF
10.245 MHz
50 pF
120 pF
2 k
muRata CFU 455 D
455 kHz Filter
2k
100 nF
100 nF
47 k
10 pF
51 k
20 pF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
100 nF
Input 10.7 MHz
51
10 k
10 k
2.0 Vdc
Op Amp Output
390 k
1.0 k
1.0 μF
Filter In
8.2 k
Audio Out
0.01 μF
Lp = 1.0 mH
Cp = 100 pF
Rp = 100 kΩ

CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

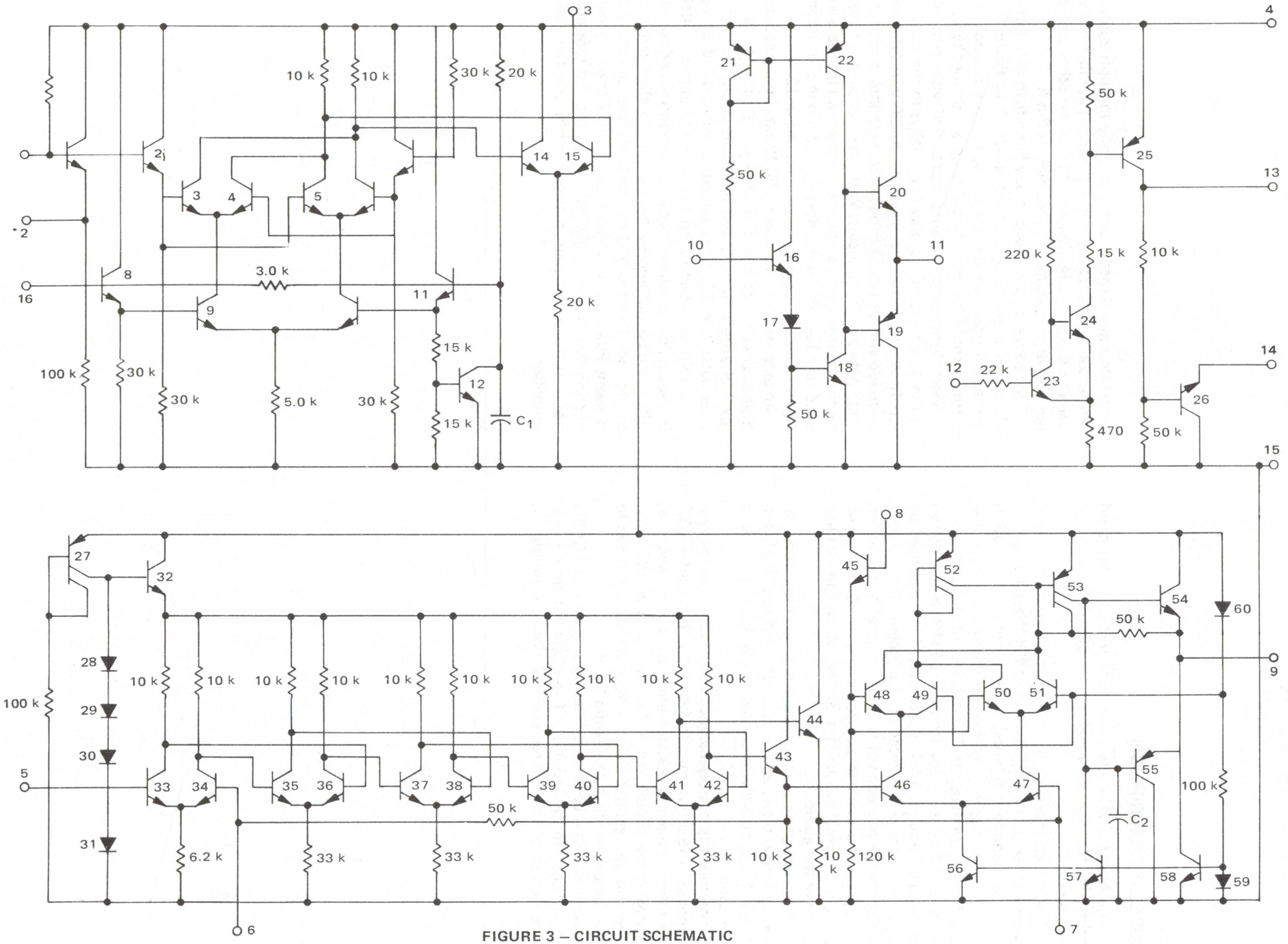

3
4
13
14
15
2
16
10
11
12
5
6
7
8
9
10 k
20 k
30 k
3.0 k
100 k
5.0 k
15 k
C1
50 k
220 k
22 k
470
6.2 k
33 k
120 k
C2
C1

FIGURE 3 – CIRCUIT SCHEMATIC

MOTOROLA

MC3359

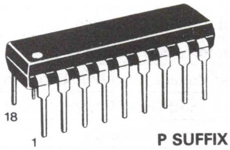
LOW-POWER NARROW-BAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrow-band FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (−3.0 dB) = 2.0 μV (Typ)
- Low Number of External Parts Required

HIGH-GAIN LOW-POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

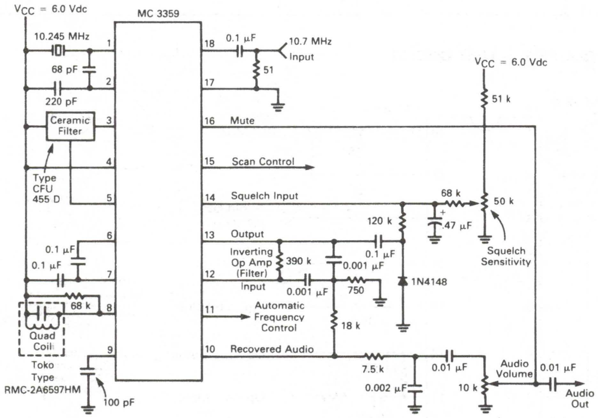
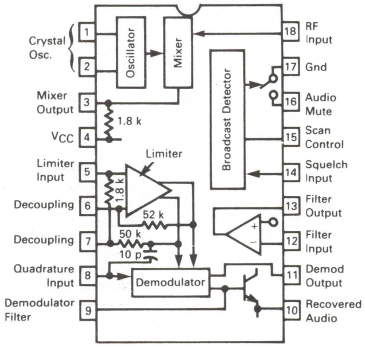

VCC = 6.0 Vdc
MC 3359
10.245 MHz
68 pF
220 pF
Ceramic Filter
Type CFU 455 D
0.1 μF
0.1 μF
68 k
Quad Coil
Toko Type RMC-2A6597HM
100 pF
18
0.1 μF
10.7 MHz Input
51
17
16 Mute
15 Scan Control
14 Squelch Input
13 Output
Inverting Op Amp (Filter) Input
12
390 k
0.001 μF
0.001 μF
750
0.1 μF
120 k
11 Automatic Frequency Control
18 k
10 Recovered Audio
1N4148
68 k
47 μF
50 k
Squelch Sensitivity
VCC = 6.0 Vdc
51 k
7.5 k
0.002 μF
0.01 μF
Audio Volume
10 k
0.01 μF
Audio Out

FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM


Crystal Osc.
1
2
Oscillator
Mixer
Mixer Output
3
1.8 k
VCC
4
Limiter Input
5
Limiter
1.8 k
Decoupling
6
52 k
Decoupling
7
50 k
10 p
Quadrature Input
8
Demodulator
Demodulator Filter
9
Broadcast Detector
18 RF Input
17 Gnd
16 Audio Mute
15 Scan Control
14 Squelch Input
13 Filter Output
12 Filter Input
11 Demod Output
10 Recovered Audio

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(max)$	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 9	Vdc
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	−0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25° C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (pins 4 and 8)	Squelch Off	—	3.6	6.0	mA
	Squelch On	—	5.4	7.0	
Input for 20 dB Quieting		—	8.0	—	µVrms
Input for −3dB Limiting		—	2.0	—	µVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	—
Mixer Third Order Intercept, 50 Ω Input		—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter gain (test circuit of Fig. 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 – High	—	0.01	1.0	µA
	– Low	2.0	2.4	—	mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 – High	—	5.0	10	Ω
	– Low		1.5	—	MΩ

FIGURE 3 — TEST CIRCUIT

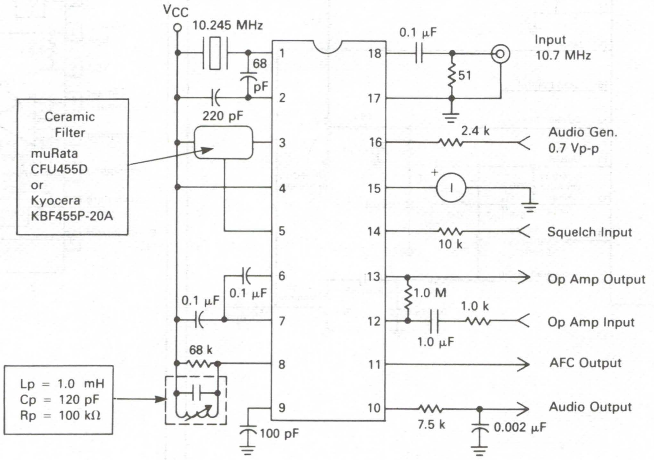

VCC
10.245 MHz
68 pF
220 pF
Ceramic Filter
muRata CFU455D or Kyocera KBF455P-20A
0.1 µF
0.1 µF
68 k
Lp = 1.0 mH
Cp = 120 pF
Rp = 100 kΩ
100 pF
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
0.1 µF
Input 10.7 MHz
51
2.4 k
Audio Gen. 0.7 Vp-p
+
I
10 k
Squelch Input
Op Amp Output
1.0 M
1.0 k
Op Amp Input
1.0 µF
AFC Output
7.5 k
0.002 µF
Audio Output

FIGURE 4 — MIXER VOLTAGE GAIN

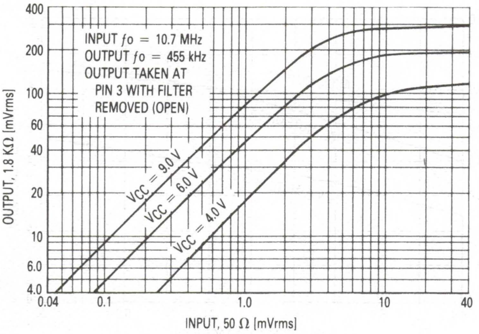


FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

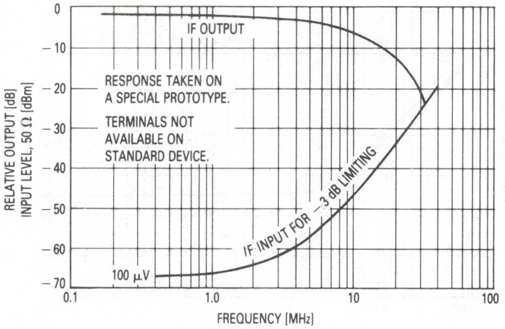


FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

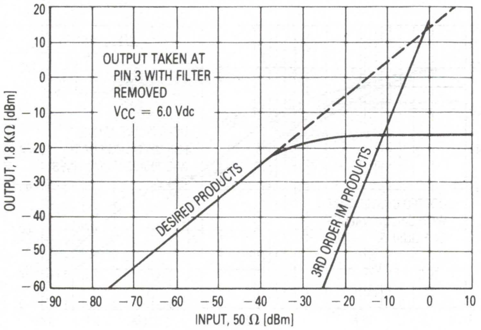


FIGURE 7 — DETECTOR AND AFC RESPONSES

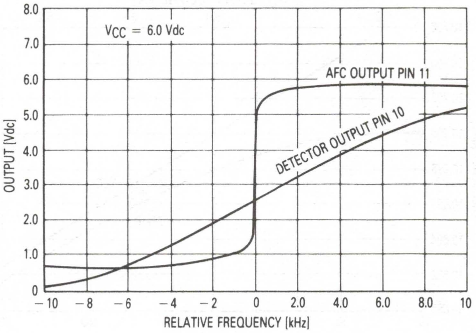


FIGURE 8 — RELATIVE MIXER GAIN

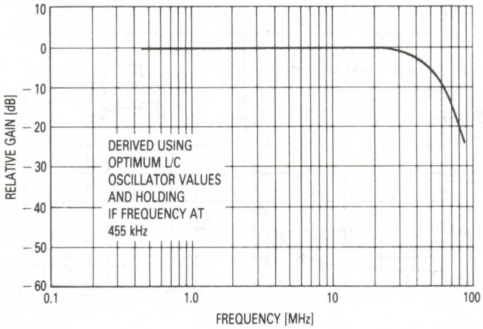


FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION

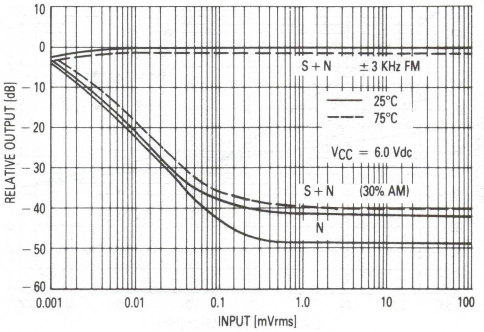


FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

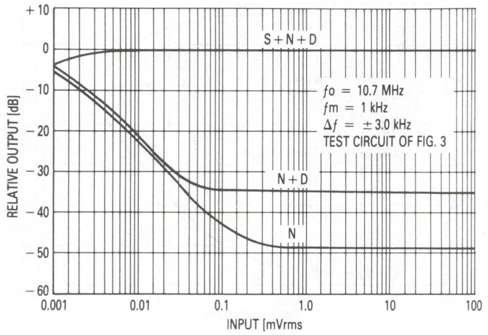


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

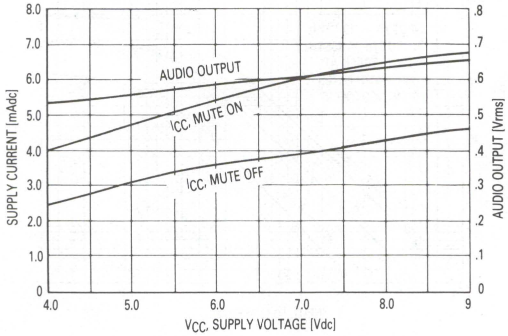


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

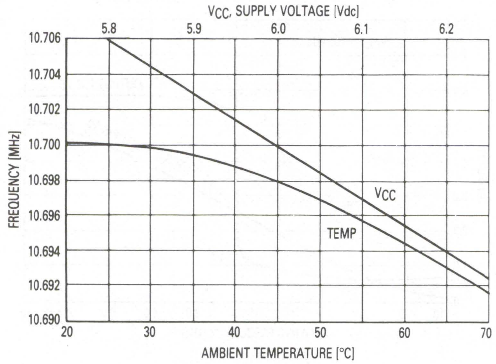


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

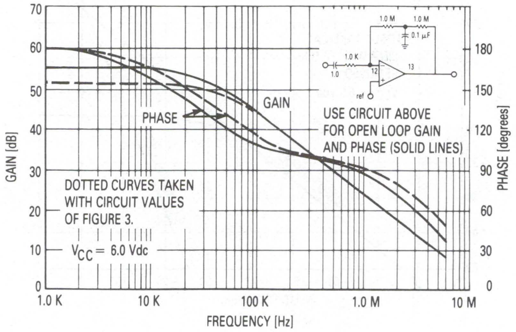


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

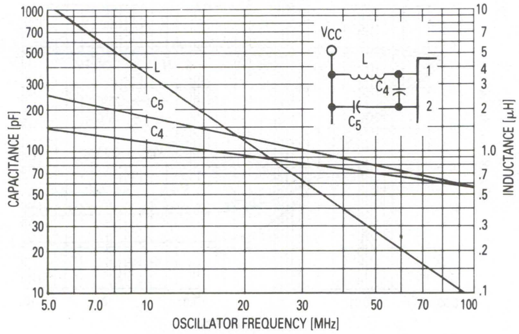
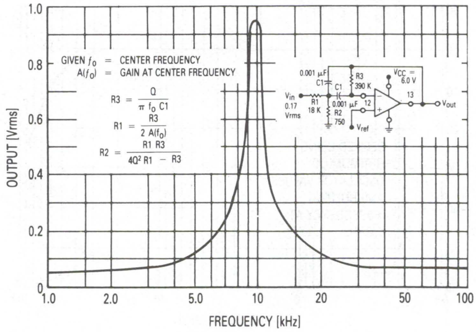


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



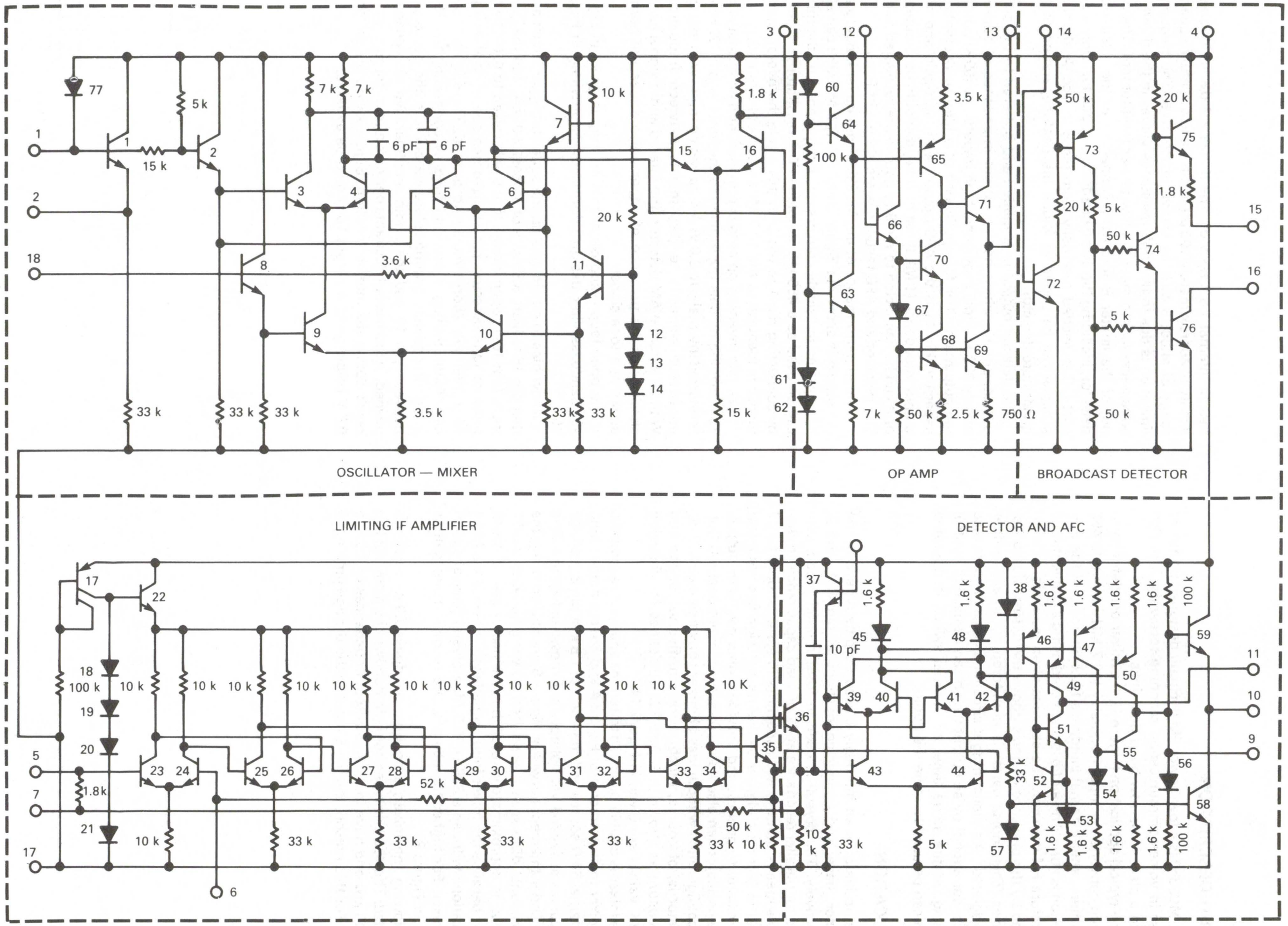

OSCILLATOR — MIXER
OP AMP
BROADCAST DETECTOR
LIMITING IF AMPLIFIER
DETECTOR AND AFC
1
2
3
4
5
6
7
9
10
11
12
13
14
15
16
17
18
77
5 k
15 k
7 k
7 k
6 pF
6 pF
10 k
1.8 k
20 k
3.6 k
33 k
3.5 k
15 k
60
64
100 k
65
3.5 k
66
70
71
67
63
68
69
61
62
7 k
50 k
2.5 k
750 Ω
50 k
73
20 k
5 k
75
1.8 k
74
72
76
50 k
37
10 pF
1.6 k
45
48
38
46
47
39
40
41
42
49
50
59
100 k
36
35
43
44
51
52
53
54
55
56
57
58
5 k
10 k
18
100 k
19
20
21
1.8k
52 k
50 k
22
23
24
25
26
27
28
29
30
31
32
33
34
10 K

FIGURE 16 — CIRCUIT SCHEMATIC

CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrow-band data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at pin 3. Voltage gain curves at several Vcc voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from pin 8 to Vcc. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, pin 10, which has an output impedance of approximately 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or deemphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting pin 1 to pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at pin 13 providing dc bias (externally) to the input at pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to pin 14 sets up the squelch-trigger circuit such that pin 15 is high, a source of at least 2.0 mA, and the audio mute (pin 16) is open-circuit. If pin 14 is raised to 0.7 V by the noise or tone detector, pin 15 becomes open-circuit and pin 16 is internally short-circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting pin 16 to a high-impedance ground-reference point in the audio path between pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on pin 16 should be avoided.

MOTOROLA

MC3361

Advance Information

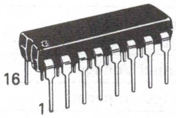
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361 is designed for use in FM dual conversion communications equipment.

- Operates From 1.8 V to 7.0 V
- Low Drain Current 4.0 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV Typ
- Low Number of External Parts Required

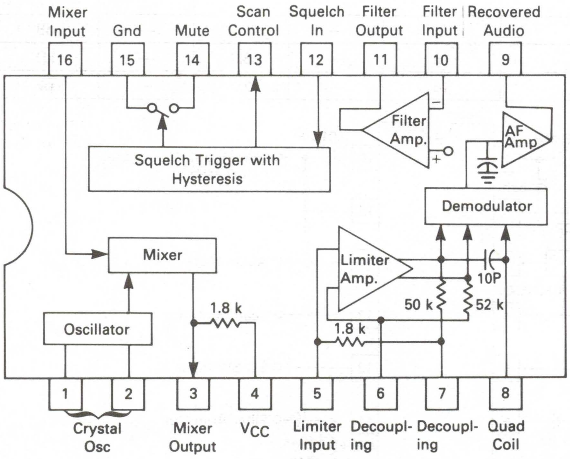
LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

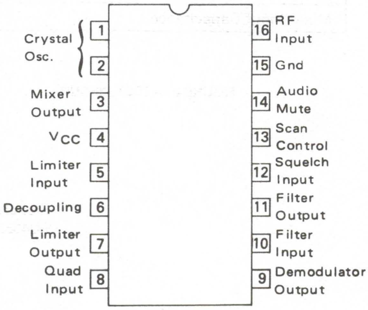


P SUFFIX
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM


Mixer Input
Gnd
Mute
Scan Control
Squelch In
Filter Output
Filter Input
Recovered Audio
16
15
14
13
12
11
10
9
Squelch Trigger with Hysteresis
Filter Amp.
AF Amp
Demodulator
Mixer
Oscillator
Limiter Amp.
1.8 k
10P
50 k
52 k
1.8 k
1
2
3
4
5
6
7
8
Crystal Osc
Mixer Output
VCC
Limiter Input
Decoupling
Decoupling
Quad Coil

PIN CONNECTIONS


Crystal Osc.
1
2
Mixer Output
3
VCC
4
Limiter Input
5
Decoupling
6
Limiter Output
7
Quad Input
8
RF Input
16
Gnd
15
Audio Mute
14
Scan Control
13
Squelch Input
12
Filter Output
11
Filter Input
10
Demodulator Output
9

This document contains information on a new product. Specifications and information herein are subject to change without notice.

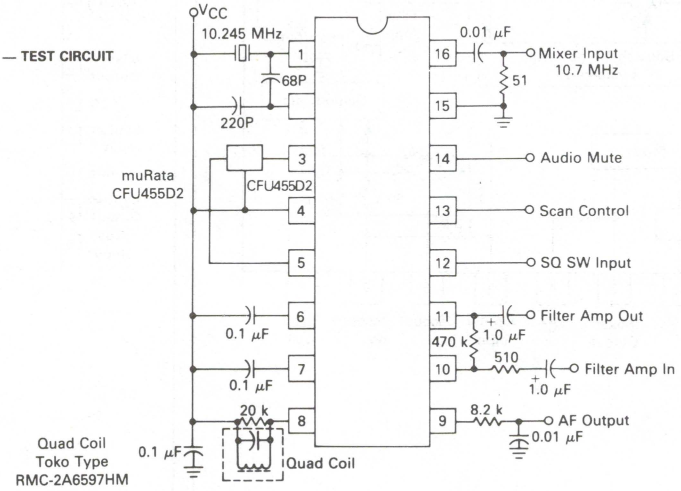
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(max)$	8.0	Vdc
Operating Supply Voltage Range	4	V_{CC}	1.8 to 7.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq 4.0$ Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	−0.5 to 5.0	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, fo = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	 — —	 4.0 6.0	 — —	mA
Input Limiting Voltage (−3.0 dB Limiting)	16	—	2.0	—	μV
Detector Output Voltage	9	—	2.0	—	Vdc
Detector Output Impedance	—	—	400	—	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	100	150	—	mVrms
Filter Gain (10 kHz) (V_{in} = 5.0 mV)	—	40	48	—	dB
Filter Output Voltage	11	—	1.5	—	Vdc
Trigger Hysteresis	—	—	50		mV
Mute Function Low	14	—	10	—	Ω
Mute Function High	14	—	10	—	MΩ
Scan Function Low (Mute Off) (V_{12} = 2.0 Vdc)	13	—	—	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	3.0	—	—	Vdc
Mixer Conversion Gain	3	—	24	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

FIGURE 2 — TEST CIRCUIT


VCC
10.245 MHz
68P
220P
muRata
CFU455D2
CFU455D2
0.1 μF
0.1 μF
20 k
Quad Coil
Toko Type
RMC-2A6597HM
0.1 μF
Quad Coil
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
0.01 μF
Mixer Input
10.7 MHz
51
Audio Mute
Scan Control
SQ SW Input
Filter Amp Out
+
1.0 μF
470 k
510
Filter Amp In
+
1.0 μF
8.2 k
AF Output
0.01 μF

MOTOROLA

MC3373

Advance Information

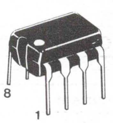
REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

REMOTE CONTROL AMPLIFIER-DETECTOR

The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

- High Gain Pre-Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- May Be Used with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Small Package Size
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved retrofit for NEC part no. µPC1373



CASE 626-04
P SUFFIX

Pin Connections

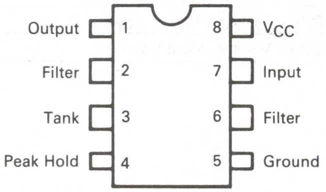
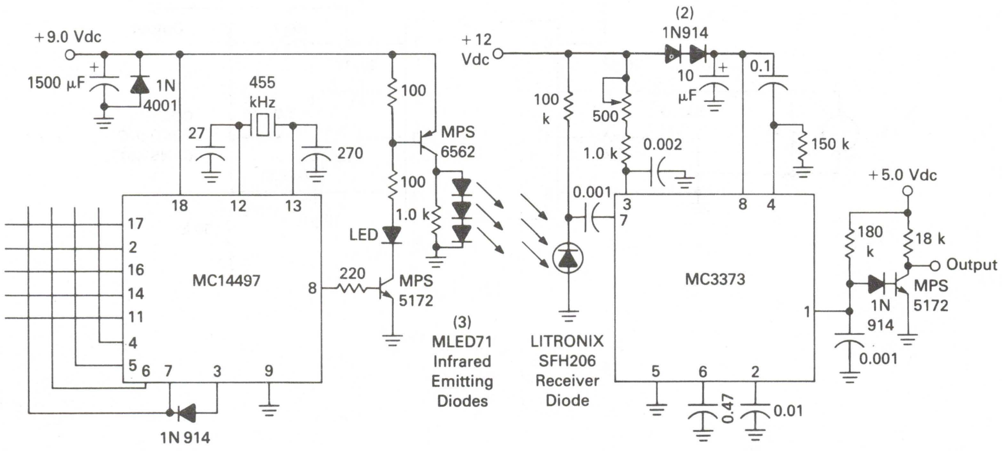

Output 1
Filter 2
Tank 3
Peak Hold 4
8 VCC
7 Input
6 Filter
5 Ground

FIGURE 1 — REMOTE CONTROL APPLICATION


+9.0 Vdc
1500 µF
+
1N
4001
455
kHz
27
270
100
MPS
6562
100
1.0 k
LED
220
MPS
5172
18
12
13
17
2
16
14
11
4
5
6
7
3
9
8
MC14497
1N 914
(3)
MLED71
Infrared
Emitting
Diodes
+12
Vdc
100
k
500
1.0 k
0.002
0.001
(2)
1N914
10
µF
0.1
150 k
LITRONIX
SFH206
Receiver
Diode
3
7
8
4
MC3373
1
5
6
2
0.47
0.01
+5.0 Vdc
180
k
18 k
Output
1N
914
MPS
5172
0.001

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Operating Temperature Range	T_A	0 to 75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Junction Temperature	T_J	150	°C
Power Dissipation, Package Rating Derate above 25°C	P_D $1/\Theta_{JA}$	1.25 10	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (25°C)	V_{CC}	4.75	—	15	Vdc
Power Supply Voltage (0°C)	V_{CC}	5.0	—	15	Vdc
Input Frequency	f_{in}	30	40	80	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, f_{in} = 40 kHz, Test circuit of Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	1.5	2.5	3.5	mAdc
Input Terminal Voltage	V(Pin 7)	2.4	2.8	3.0	Vdc
Input Voltage Threshold	V_{in}	—	50	100	μV_{P-P}
Input Amplifier Voltage Gain (V[Pin 3] = 500 mV_{P-P})	A_V	—	60	—	dB
Input Impedance	r_{in}	40	60	80	kΩ
Output Voltage, V_{in} = 1.0 mV_{P-P}	V_{OL}	—	—	0.5	V
Output Leakage, V_{CC} = V_{OH} = 15 Vdc	I_{OH}	—	—	2.0	μA
Output Voltage, Input Open	V_{OH}	—	—	5.0	Vdc

FIGURE 2 — TEST CIRCUIT

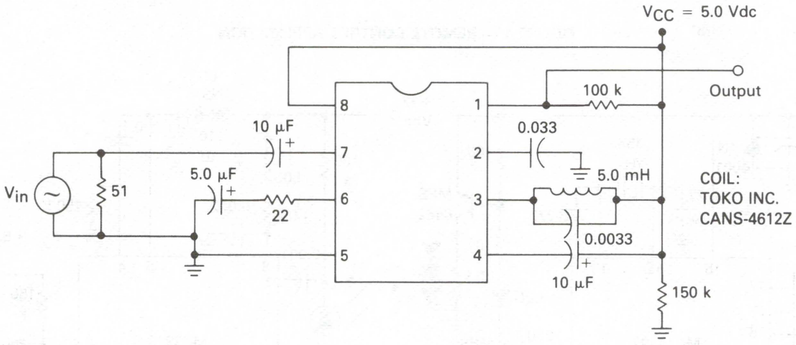


FIGURE 3 — BLOCK DIAGRAM

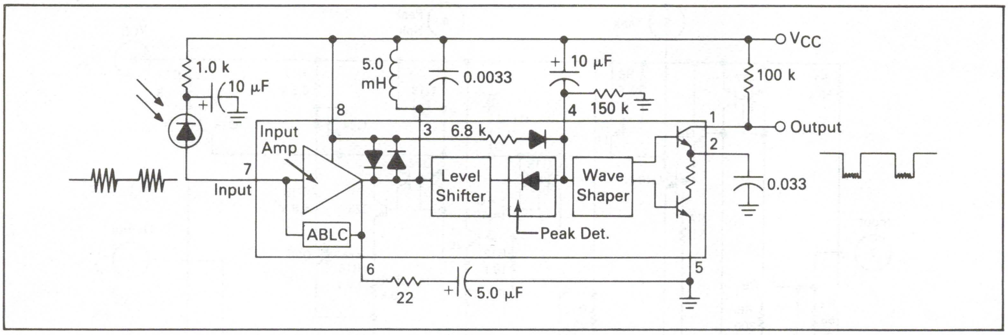

VCC
1.0 k
10 µF
5.0 mH
0.0033
10 µF
100 k
150 k
8
4
1
Output
3
6.8 k
2
Input Amp
7
Input
Level Shifter
Wave Shaper
0.033
ABLC
Peak Det.
6
5
22
5.0 µF

FIGURE 4 — INPUT AMPLIFIER GAIN

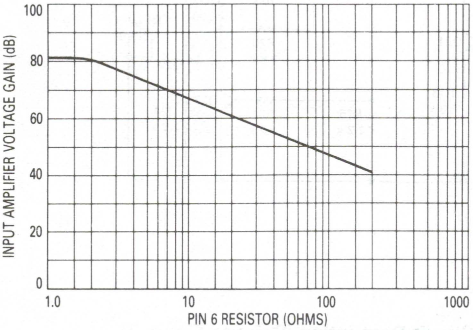


FIGURE 5 — DETECTOR THRESHOLD

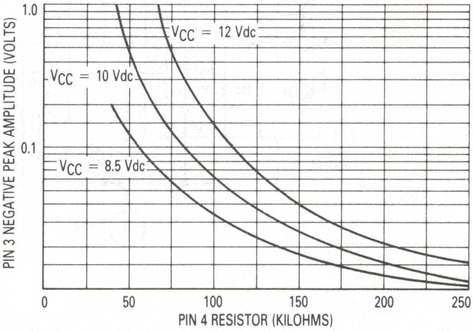
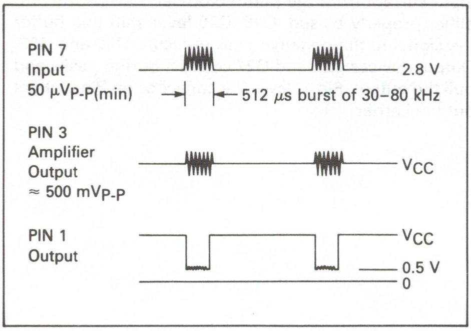


FIGURE 6 — TYPICAL SIGNAL WAVEFORMS

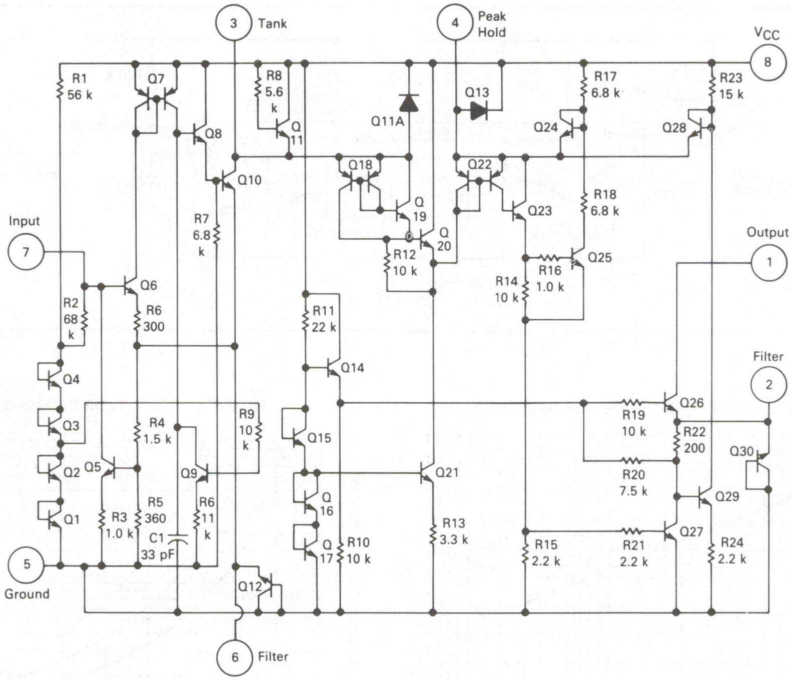

PIN 7
Input
50 µVP-P(min)
2.8 V
512 µs burst of 30–80 kHz
PIN 3
Amplifier
Output
≈ 500 mVP-P
VCC
PIN 1
Output
VCC
0.5 V
0

APPLICATIONS INFORMATION

The MC3373 is designed to amplify and detect the signal from an infrared receiver diode in a remote control system. The signal is generally in the form of ultrasonic bursts, ranging in amplitude from 50 μV_{P-P} to several hundred millivolts. The receiver diode may be directly connected to the MC3373 to save parts; the input is internally compensated by an ABLC (automatic bias level control). However, it is advantageous to ac couple the input, as shown in Figure 1, in order to provide attenuation of the power line frequency IR inputs, which are plentiful in most cases.

The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

FIGURE 7 — INTERNAL SCHEMATIC


3
Tank
4
Peak
Hold
VCC
8
R1
56 k
Q7
Q8
R8
5.6
k
Q
11
Q11A
Q13
R17
6.8 k
Q24
R23
15 k
Q28
Q10
Q18
Q22
Q
19
Q23
R18
6.8 k
Input
7
R7
6.8
k
R12
10 k
Q
20
Output
1
Q25
R16
1.0 k
R14
10 k
Q6
R2
68
k
R6
300
R11
22 k
Q14
Filter
2
Q4
Q3
Q2
Q5
R4
1.5 k
R9
10
k
Q15
Q26
R19
10 k
R22
200
Q30
Q9
Q21
R20
7.5 k
Q29
Q1
R3
1.0 k
R5
360
C1
33 pF
R6
11
k
Q
16
R13
3.3 k
Q27
Q
17
R10
10 k
R15
2.2 k
R21
2.2 k
R24
2.2 k
5
Ground
Q12
6
Filter

The load may be resistive, as shown in the application circuit, or tuned, as in the test circuit. The amplifier output is limited by back-to-back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to V_{CC}. The capacitor from V_{CC} to Pin 4 quickly charges during the negative peaks and then settles toward the set-up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

Circuit Description (Refer to Figure 7)

Q1–Q4 set the bias on the amplifier input at approximately 2.8 V. Q6–Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0. Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18–Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output, Pin 1, low. The capacitor on Pin 2 filters out the carrier.

MOTOROLA

MC3393P

Advance Information

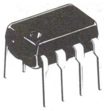
TWO MODULUS PRESCALER

The MC3393P can divide by 15 and 16, and can be used with Motorola CMOS frequency synthesizers MC145146, 52, 56 for commercial AM-FM radio, land mobile and marine two-way radios, avionic radios, and scanner receivers.

- 140 MHz (typ) Toggle Frequency
- ÷15/16
- TTL and CMOS Compatible Output
- Active Pullup and Pulldown
- +5.0 V Supply
- Buffered Clock Input
- 100–400 mV (typ) Input Sensitivity
- 200 Milliwatts (typ)

TWO MODULUS PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 626-04

FIGURE 1 — LOGIC DIAGRAM

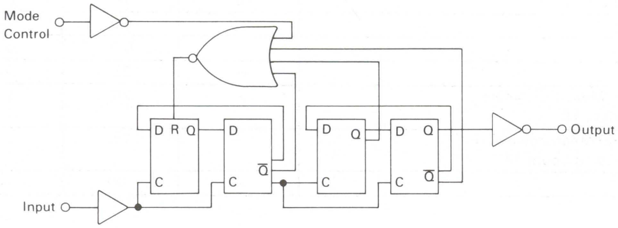
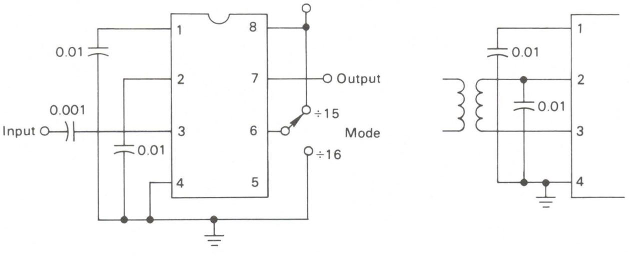

Mode Control
D R Q
C
D
C
Q̄
D Q
C
D Q
C Q̄
Output
Input

FIGURE 2 — TEST CIRCUITS


0.01
0.001
Input
0.01
1
2
3
4
8
7
6
5
Output
÷15
Mode
÷16
0.01
0.01
1
2
3
4

Capacitor Coupled Input

Link Coupled Input

Pin Outs

1. Bias Decouple
2. Bias Decouple
3. Input
4. Ground
5. NC
6. Input
7. Output
8. V_{CC}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	Vdc
Input Mode Control Voltage	V_{ICR}	10	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PRELIMINARY ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = +5.0 Vdc, T_A = 25°C, f_{in} = 100 MHz)

Characteristics	Min	Typ	Max	Units
Power Supply Voltage	4.5	—	5.5	Vdc
Current Drain	—	40	—	mA
Input Voltage	100	—	400	mV(rms)
Input Impedance: Real Part Capacitance	— —	900 6.0	— —	Ohms pF
Mode Control Voltage for 15 Count	2.7	—	10	Vdc
Mode Control Voltage for 16 Count	0	—	0.8	Vdc
Output High at 30 μA Source	2.7	4.3	—	Vdc
Output Low at 1.6 mA Sink	—	0.3	0.8	Vdc
Propagation Delay Time	—	25	—	ns
Set up Time (16 to 15 Count) Measured before Rising Edge of Clock on Count 15	—	20	—	ns
Release Time (15 to 16 Count) Measured before Falling Edge of Clock Preceding Count 15	—	15	—	ns
Thermal Resistance, $R_{\theta JC}$	—	100	—	°C/W

MOTOROLA

MC3396P

Advance Information

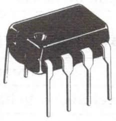
DIVIDE BY 20 PRESCALER

The MC3396P is a fixed ÷20 prescaler for use in frequency synthesizers and similar applications.

- 200 MHz (typ) Toggle Frequency
- Single 5.0 Volt Supply
- Buffered Clock Input
- 100 mV — 400 mV RMS Input Sensitivity
- Open-Collector Saturating Output is Capable of Driving TTL and CMOS.

DIVIDE BY 20 PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-04

FIGURE 1 — LOGIC DIAGRAM

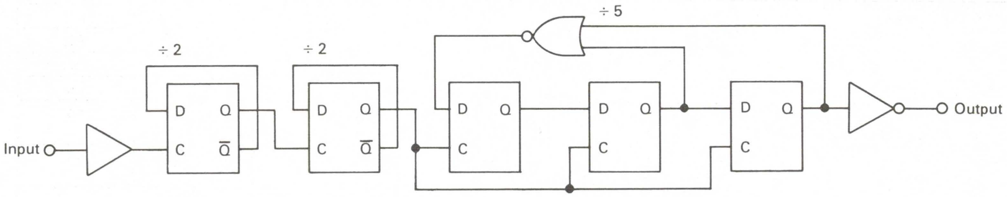
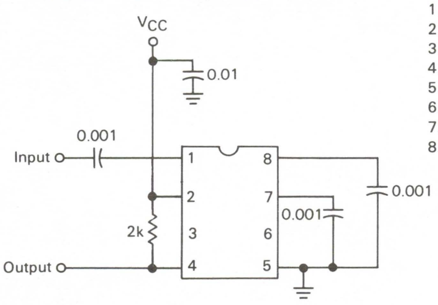

÷ 2
÷ 2
÷ 5
D
Q
C
$\overline{Q}$
Input
Output

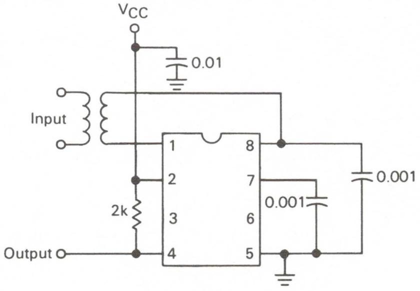
FIGURE 2 — CAPACITOR-COUPLED INPUT


V_{CC}
0.01
0.001
Input
2k
Output
1
2
3
4
5
6
7
8
0.001
0.001

PIN CONNECTIONS

1. Input
2. V_{CC}
3. NC
4. Output
5. Ground
6. NC
7. Bias Decouple
8. Bias Decouple

FIGURE 3 — LINK-COUPLED INPUT


V_{CC}
0.01
Input
2k
Output
1
2
3
4
5
6
7
8
0.001
0.001

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 5 Vdc, T_A = 25°C, f_{in} = 125 MHz measured in the circuit of Figure 2)

Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage Range	4.5	—	5.5	Vdc
Current Drain	—	30	—	mA
Operating Input Voltage Range	100	—	400	mV(rms)
Input Impedance:				
Real Part	—	600	—	Ohms
Capacitance	—	6.0	—	pF
Output Voltage	3.0	4.5	—	V_{p-p}
Thermal Resistance — θ_{JA}	—	100	—	°C/W

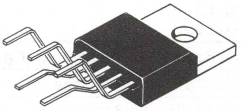
MOTOROLA

MC3484V2
MC3484V4

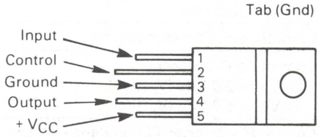
SOLENOID DRIVER
2.4 A — V2
4.0 A — V4

SILICON MONOLITHIC INTEGRATED CIRCUIT

V SUFFIX
PLASTIC PACKAGE
CASE 314B-01



PIN CONNECTIONS


Tab (Gnd)
Input
Control
Ground
Output
+ V_{CC}
1
2
3
4
5

INTEGRATED SOLENOID DRIVER

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484V4 or 2.4 A in MC3484V2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation. Other solenoid or relay applications could be served by the MC3484. Two high impedance inputs are provided which permit a variety of control options and can be driven by TTL or CMOS logic:

- Microprocessor Compatible Inputs
- On-Chip Power Device

MC3484V2	2.4 A Peak	0.6 A Sustain
MC3484V4	4.0 A Peak	1.0 A Sustain

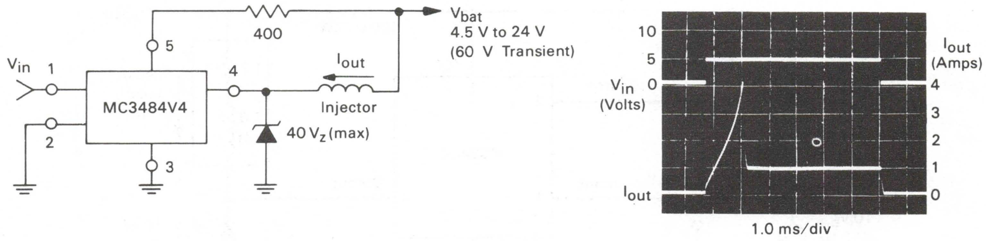
- Low Thermal Resistance to Grounded Tab
  $R_{\theta JC}$ = 2.5°C/W
- Internal Thermal Protection
  Controls die temperature to 175°C
- Load Dump Protected
- Low Saturation Voltage
  $V_{CE(sat)}$ = 1.6 V Typ @ 4.0 A
- Uncompromised Performance −40°C to +125°C
- Fully Functional from V_{bat} = 4.0 V to 24 V
- High $V_{(BR)CEO(sus)}$ = 42 V min @ 2.0 A

ORDERING INFORMATION

Device	Temperature Range	Peak Current
MC3484V2	-40 to +125°C	2.4 A
MC3484V4	-40 to +125°C	4.0 A

FIGURE 1 — TYPICAL APPLICATION

Single Injector — No Control Option


V_{in}
1
2
5
3
4
MC3484V4
400
V_{bat}
4.5 V to 24 V
(60 V Transient)
I_{out}
Injector
40 V_Z (max)
10
5
V_{in} 0
(Volts)
I_{out}
I_{out}
(Amps)
4
3
2
1
0
1.0 ms/div

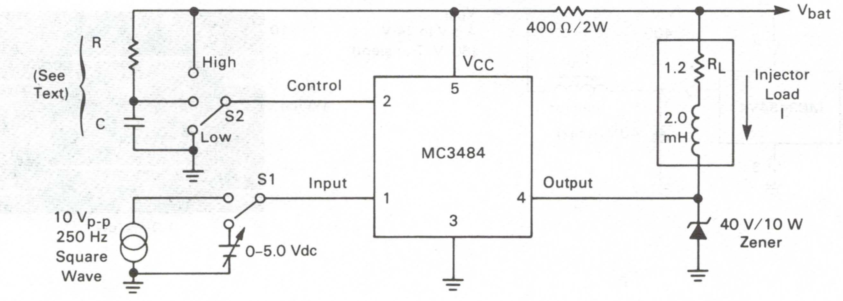
MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (V_{bat})	24	Volts
Input (Pin 1)	-6.0 to +24	V
Control (Pin 2)	-6.0 to +24	V
Internal Regulator (Pin 5)	50	mA
Junction Temperature	150	°C
Operating Temperature Range (Tab Temperature)	-40 to +125	°C
Storage Temperature Range	-65 to +150	°C
Thermal Resistance, Junction to Case	2.5	°C/W

ELECTRICAL CHARACTERISTICS (V_{bat} = 12 Vdc, T_C = 25°C, test circuit of Figure 2, unless noted)

Characteristic	Min	Typ	Max	Unit
Output Peak Current ($I_{pk[sense]}$) V4 V2	3.6 1.7	4.0 2.4	4.8 2.9	A
Output Sustaining Current (I_{sus}) V4 V2	1.0 0.5	1.1 0.6	1.3 0.7	A
$V_{(BR)CEO(sus)}$ @ 2.0 A	42	50	—	V
Output Voltage in Saturated Mode V2 @ 1.5 A V4 @ 3.0 A	 — —	 1.2 1.6	 1.8 1.8	V
Internal Regulated Voltage (V_{CC}, Figure 2)	6.6	7.1	8.1	V
Input "on" Threshold Voltage	—	1.4	1.9	V
Input "off" Threshold Voltage	0.9	1.3	—	V
Input "on" Current @ V_I = 2.0 Vdc @ V_I = 5.0 Vdc	 — —	 — —	 150 350	μA
Control "on" Threshold Voltage	0.9	—	1.9	V
Control "on" Current @ V_2 = 2.0 Vdc (V_I High) @ V_2 = 5.0 Vdc (V_I High)	 −2.0 —	 — —	 2.0 500	μA
Control Pin Discharge Impedance (V_I Low)	—	10	—	kΩ
Input Turn On Delay (t_i)	—	1.0	2.0	μs
I_{pk} sense to I_{sus} delay (tp)	—	60	—	μs
Control Signal Delay (t_t)	—	15	—	μs
Input Turn Off from Saturated Mode Delay (t_s)	—	1.0	—	μs
Input Turn Off from Sustain Mode Delay (t_d)	—	0.2	—	μs
Output Voltage Rise Time (t_V)	—	0.4	—	μs
Output Current Fall Time (t_f) 2.0 A 4.0 A	— —	0.3 0.6	1.0 1.0	μs
Internal Thermal Regulation	—	175	—	°C

FIGURE 2 — TEST CIRCUIT


R
(See Text)
C
High
Control
S2
Low
S1
Input
10 V_{p-p} 250 Hz Square Wave
0-5.0 Vdc
V_{CC}
5
2
MC3484
1
3
4
Output
400 Ω/2W
V_{bat}
1.2
R_L
2.0 mH
Injector Load I
40 V/10 W Zener

GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the MC3484 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present come in two types. The large throttle body injectors have an impedance of about 2.0 mH and 1.2 Ω and require the MC3484 V4 driver. The smaller type, popular world-wide, has an impedance of 4.0 mH and 2.4 Ω and needs about a 2.0 A pulse for good results. Some designs are planned which employ two of the smaller types in parallel. The inductance of the injectors are much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range from 5.0 Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

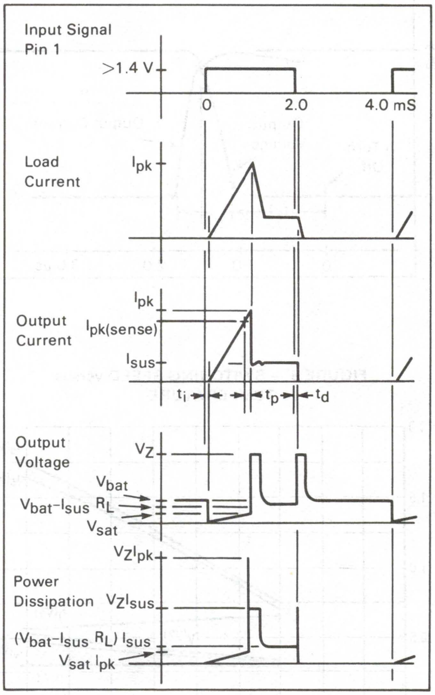
APPLICATIONS INFORMATION

The MC3484 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off". This pin has a nominal trip level of 1.4 V and an input impedance of 20 kΩ. It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which if held low or grounded, permits the device to operate in saturation to $I_{pk(sense)}$, where it will switch to I_{sus} automatically. If Pin 2 is brought high (>1.9 V), the MC3484 will switch to I_{sus} mode, whether or not $I_{pk(sense)}$ has been reached. (More on this later.)

Figure 3 shows the operating waveforms for the simplest mode; i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The MC3484 then reduces its output to I_{sus}. The fall time of the device is very rapid (⩽1.0 μs), but the decay of the load current takes 150 to 220 μs, while dumping the load energy into the protection zener clamp.

FIGURE 3 — OPERATING WAVEFORMS
(Max Frequency 250 Hz, Pin 2 Grounded)



It is essential that the zener voltage be lower than the $V_{(BR)CEO(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the MC3484, which, for the high current applications, could cause the device to fail. (See SOA, Figure 12.)

Also in Figure 3 is the graphically derived instantaneous power dissipation of the MC3484. It shows that, for practical purposes, the worst case dissipation is less than (I_{sus}) (V_{bat}) (duty cycle).

If the combined effects of dissipation, ambient temperature and poor heat sinking causes the die temperature to reach 160°C, an internal protection circuit will reduce the output current to prevent device failure. The output pulses will remain controlled by the input, but may not operate the fuel injectors.

FIGURE 4 — SWITCHING WAVEFORMS
(Expanded Time Scale)

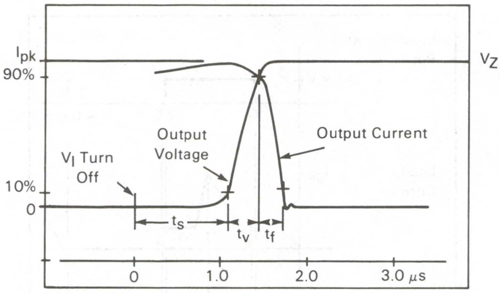
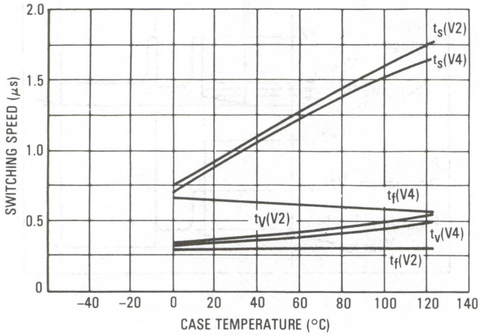


FIGURE 5 — SWITCHING SPEED versus TEMPERATURE



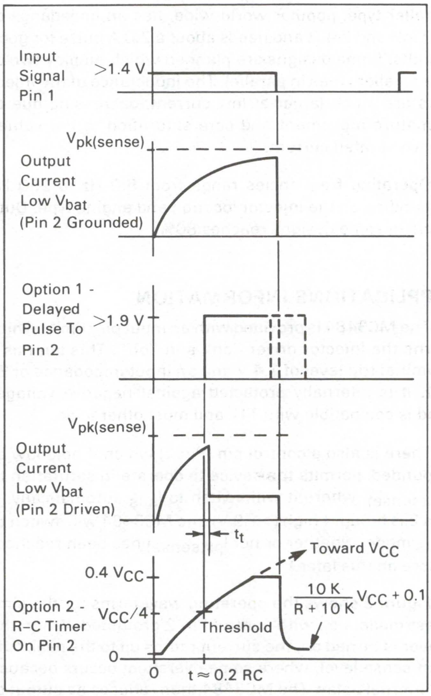
Provided in Figures 3, 4, and 6 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

In the case where V_{bat} is too low, or the input Pin 1 "on" signal is too narrow for the output current to reach $I_{pk(sense)}$, it may still be desirable to cause the MC3484 to switch to the I_{sus} mode. This can be accomplished either by driving Pin 2 with a properly delayed pulse, or by using an R-C charging circuit on Pin 2. If a pulse source is used, only the leading edge and 2.0 volts amplitude are important. The pulse duration is not critical, because once the MC3484 has changed to I_{sus} mode, it will stay there until Pin 1 has been recycled. A minimum pulse width of 15 µs will assure state change.

If the R-C circuit is used (circuit of Figure 2, switch S2 in middle position), the charging voltage will be toward V_{CC}, but will reach the Pin 2 threshold at $V_{CC}/4$. This maintains the timing of the I_{sus} transition even when V_{CC} is below regulation. When Pin 1 is turned off, the capacitor on Pin 2 is discharged through an internal 10 kΩ resistor to about 0.1 V above ground. It is important to use a high value for R, so that the capacitor will be almost fully discharged. With a recommended R = 470 K Ω and C = 0.02 µF, Pin 2 threshold will be reached in approximately 2.0 ms.

In another application option, Pin 2 can be enabled in paralled with Pin 1, or connected to V_{CC}, so that the MC3484 always turns on in the I_{sus} mode. The MC3484 thus provides a logic compatible, constant current power switch.

FIGURE 6 — APPLICATION OF CONTROL (PIN 2)
(Test Circuit of Figure 2)


Input Signal Pin 1
>1.4 V
Vpk(sense)
Output Current Low Vbat (Pin 2 Grounded)
Option 1 - Delayed Pulse To Pin 2
>1.9 V
Vpk(sense)
Output Current Low Vbat (Pin 2 Driven)
tt
Toward VCC
0.4 VCC
Option 2 - R-C Timer On Pin 2
VCC/4
Threshold
10 K / R + 10 K VCC + 0.1
0
0
t ≈ 0.2 RC

TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, V_{bat} = 12 Vdc, T_C = 25°C, 250 Hz square wave input)

FIGURE 7 — OUTPUT CURRENT versus TEMPERATURE

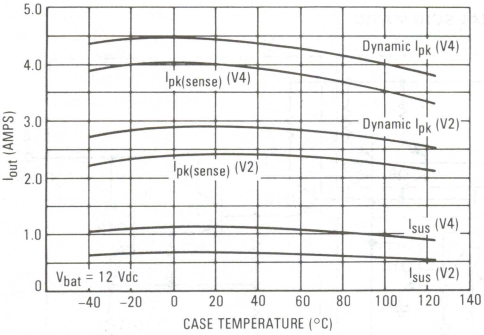


FIGURE 8 — SATURATION VOLTAGE

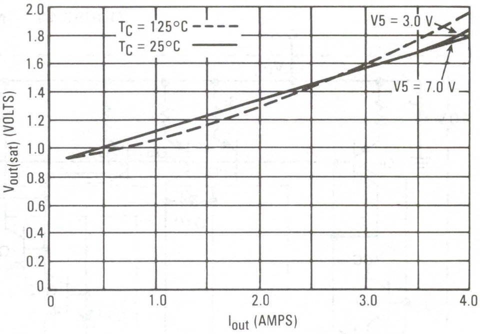


FIGURE 9 — OUTPUT CURRENT versus SUPPLY VOLTAGE

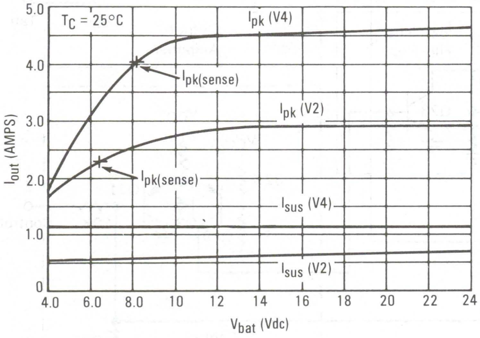


FIGURE 10 — OPERATING VOLTAGES

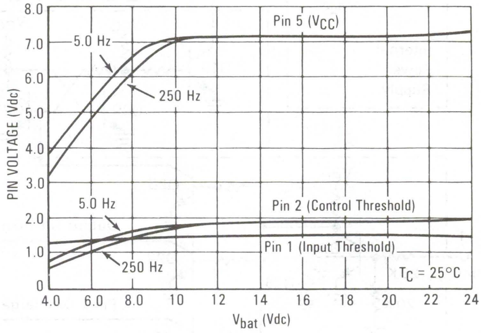


FIGURE 11 — BREAKDOWN VOLTAGE versus TEMPERATURE

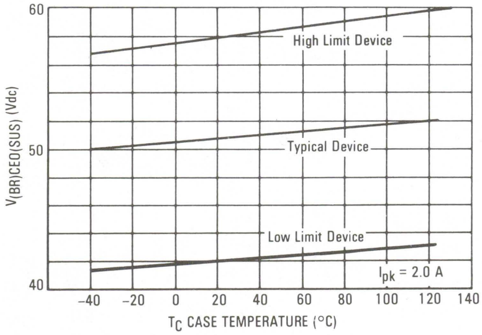


FIGURE 12 — SAFE OPERATING AREA

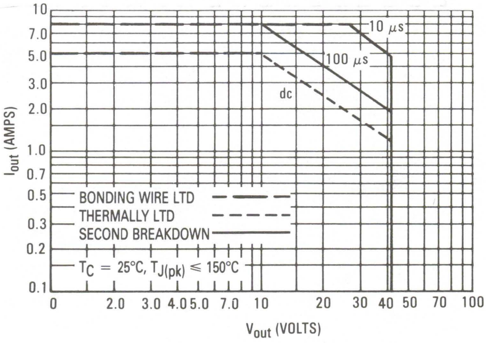
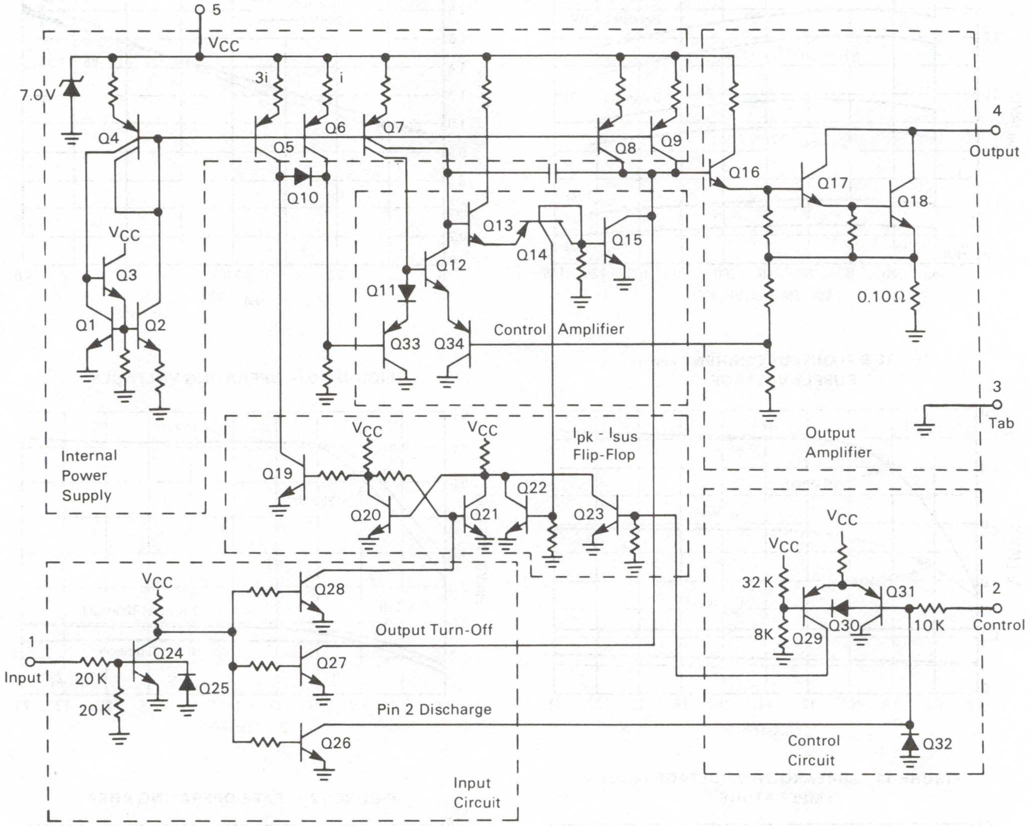


FIGURE 13 — INTERNAL SCHEMATIC


5
V_{CC}
7.0 V
3i
i
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q16
Q17
Q18
4
Output
Q13
Q14
Q15
Q12
Q11
V_{CC}
Q3
Q1
Q2
Q33
Q34
Control Amplifier
0.10 Ω
3
Tab
Output Amplifier
Internal Power Supply
V_{CC}
V_{CC}
I_{pk} - I_{sus} Flip-Flop
Q19
Q20
Q21
Q22
Q23
V_{CC}
V_{CC}
V_{CC}
32 K
8K
Q29
Q30
Q31
2
10 K
Control
Q28
Output Turn-Off
1
Input
20 K
20 K
Q24
Q25
Q27
Pin 2 Discharge
Q26
Input Circuit
Control Circuit
Q32

MOTOROLA

MC13001P
MC13002P

Advance Information

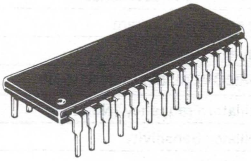
MONOMAX BLACK-AND-WHITE TV SUBSYSTEM

The MONOMAX is a single-chip IC that will perform the electronic functions of a monochrome TV receiver, with the exception of the tuner, sound channel, and power output stages.

- Full Performance Monochrome Receiver with Noise and Video Processing — Black Level Clamp, DC Contrast, Beam Limiter
- Video IF Detection on Chip — No Coils, No Pins, except Inputs
- Noise Filtering on Chip — Minimum Pins and Externals
- Oscillator Components on Chip — No Precision Capacitors Required
- MC13001P for 525 Line NTSC and MC13002P for 625 Line CCIR
- Low Dissipation in All Circuit Sections
- High-Performance Vertical Countdown
- 2-Loop Horizontal System with Low Power Start-Up Mode
- Noise Protected Sync and Gated AGC System
- Designed to work with TDA1190P or TDA3190P Sound IF and Audio Output Devices
- Reverse AGC Types are Available on Special Order. Consult Factory

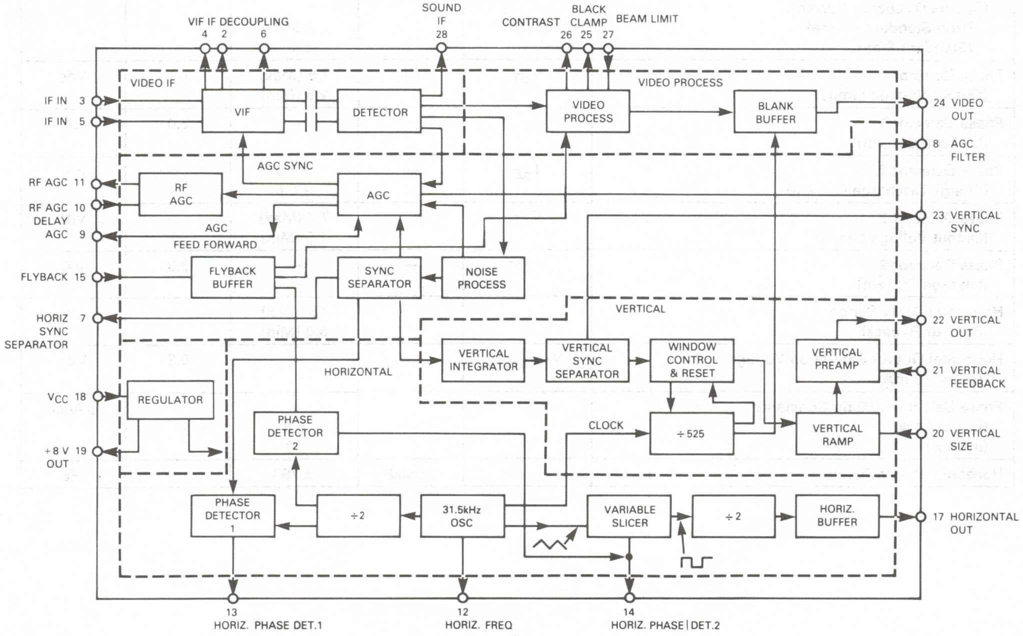
MONOMAX
BLACK-AND-WHITE TV
SUBSYSTEM

SILICON MONOLITHIC
INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM



VIF IF DECOUPLING
4 2 6
SOUND IF 28
CONTRAST
BLACK CLAMP
BEAM LIMIT
26 25 27
VIDEO IF
VIF
DETECTOR
VIDEO PROCESS
VIDEO PROCESS
BLANK BUFFER
IF IN 3
IF IN 5
24 VIDEO OUT
8 AGC FILTER
AGC SYNC
RF AGC 11
RF AGC 10 DELAY
AGC 9
RF AGC
AGC
AGC FEED FORWARD
23 VERTICAL SYNC
FLYBACK 15
FLYBACK BUFFER
SYNC SEPARATOR
NOISE PROCESS
VERTICAL
HORIZ 7 SYNC SEPARATOR
22 VERTICAL OUT
VERTICAL INTEGRATOR
VERTICAL SYNC SEPARATOR
WINDOW CONTROL & RESET
VERTICAL PREAMP
21 VERTICAL FEEDBACK
HORIZONTAL
VCC 18
REGULATOR
+8 V 19 OUT
PHASE DETECTOR 2
CLOCK
÷525
VERTICAL RAMP
20 VERTICAL SIZE
PHASE DETECTOR 1
÷2
31.5kHz OSC
VARIABLE SLICER
÷2
HORIZ. BUFFER
17 HORIZONTAL OUT
13 HORIZ. PHASE DET.1
12 HORIZ. FREQ
14 HORIZ. PHASE DET.2

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage — Pin 18	V_{CC}	+16	Vdc
Power Dissipation	P_D	1.0	Watts
Horizontal Driver Current — Pin 17	I_{HOR}	−20	mA
RF AGC Current — Pin 11	I_{RFAGC}	20	mA
Video Detector Current — Pin 24	I_{VID}	5.0	mA
Vertical Driver Current — Pin 22	I_{VERT}	5.0	mA
Auxiliary Regulator Current — Pin 19	I_{REG}	35	mA
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	60	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Horizontal Output Drive Current	I_{HOR}	≤10	mA
RF AGC Current	I_{RFAGC}	≤10	mA
Regulator Current	I_{REG}	≤20	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 11.3 V, T_A = 25°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Power Supply Current	Pins 18 & 19	I_{CC}	44	—	66	mA
Regulator Voltage	Pin 19	V_{REG}	7.2	8.2	8.8	Vdc
HORIZONTAL SPECIFICATIONS						
Oscillator Frequency (Nominal)	Pin 12	$f_{HOR(NOM)}$	13	—	19	kHz
Oscillator Sensitivity			—	230	—	Hz/μA
Start-Up Frequency (I_{18} = 4.0 mA)		f_{HOR}	−10	—	+10	%
Oscillator Temperature Stability (0 ≤ TA ≤ 75°C)		f_{HOR}	—	50	—	Hz
Phase Detector 1 (Charge/Discharge Current) (Non Standard Frame) (Standard Frame)		$I_{\phi 1}$		±900 ±400		μA
Phase Detector 1 (Output Voltage Limits)		$V_{\phi 1}$	—	7.5 (Max) 2.5 (Min)	—	Vdc
Phase Detector 1 (Leakage Current)			—	—	2.0	μA
Phase Detector 2 (Charge/Discharge Current)		$I_{\phi 2}$	—	+1.0 −0.6		mA
Phase Detector 2 (Output Voltage Limits)		$V_{\phi 2}$		7.7 (Max) 1.5 (Min)		Vdc
Phase Detector 2 (Leakage Current)			—	—	3.0	μA
Horizontal Delay Range (Sync to Flyback)				18 (Max) 5.0 (Min)		μs
Horizontal Output Saturation Voltage (I_{17} = 7.0 mA)		$V_{17(SAT)}$	—	—	0.3	Vdc
Phase Detector 1 (Gain Constant) (Out-of-Lock) (In-Lock)			—	5.0 10	—	μA/μs
Horizontal Pull-In Range			±500	±750		Hz

VERTICAL SPECIFICATIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Output Current Pin 22	I_{22}	−0.6	—	—	mA
Feedback Leakage Current Pin 21	I_{21}	—	—	6.0	µA
Ramp Retrace Current Pin 20	I_{20}	500	—	900	µA
Ramp Leakage Current Pin 20		—	—	0.3	µA
Feedback Maximum Voltage	V_{21}	—	5.1	—	Vdc
IF SPECIFICATIONS					
Regulator Voltage	V_4	—	6.2	—	Vdc
Input Bias Voltage	$V_{2,6}$	—	4.5	—	Vdc
Input Resistance Input Capacitance (V_{AGC} Pin 8 = 4.0 V)	R_{IN} C_{IN}		2.2 5.0		kΩ pF
Sensitivity (V_8 = 0 V, 400Hz 30% MOD, V_{28} = 0.8 V_{pp})		—	80	—	μV_{RMS}
Bandwidth		—	75	—	MHz
VIDEO SPECIFICATIONS					
Zero Carrier Voltage (See Figure 6A) Pin 28		—	7.0	—	Vdc
Output Voltage (See Figure 6B) Pin 24 White to Back Porch		—	1.4	—	V
Differential Gain Differential Phase (IRE Test Method)		—	6 4	—	% Degrees
Contrast Bias Current Pin 26	I_{26}	—	10	—	µA
Contrast Control Range		—	14:1	—	
Beam Limiting Voltage Pin 27	V_{27}	—	1.0	—	Vdc
AGC & SYNC					
R.F. (Tuner) AGC Output Current (V_{11} = 5.5 V)	I_{11}	5.0	—	—	mA
AGC Delay Bias Current	I_{10}	—	−10	—	µA
AGC Feedforward Current	I_9	—	1.0	—	mA
AGC Threshold (Sync Tip at Pin 28)	V_{28}	4.7	—	5.1	Vdc
Sync Separator Operating Point	V_7	—	4.2	—	Vdc
Sync Separator Charge Current	I_7	—	5.0	—	mA

FIGURE 2 — MONOMAX AGC CHARACTERISTICS

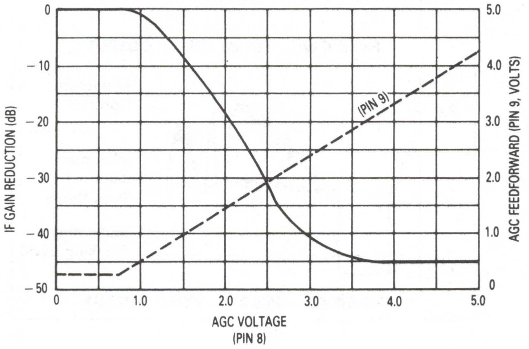


FIGURE 3 — VIDEO OUTPUT RESPONSE

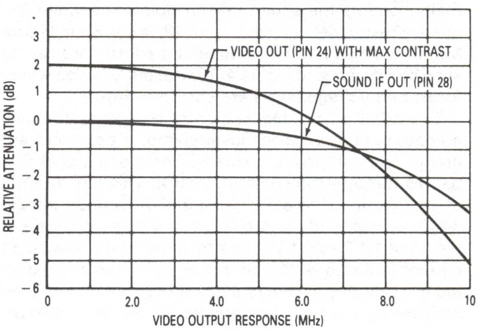


FIGURE 4 — DETECTOR PRODUCTS

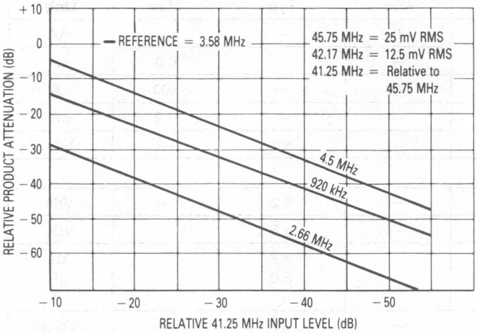
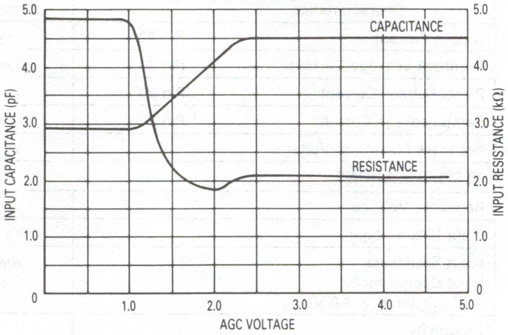


FIGURE 5 — DIFFERENTIAL INPUT IMPEDANCE CHARACTERISTICS versus AGC



GENERAL DESCRIPTION

The Video IF Amplifier is a four-stage design with 80 µV sensitivity. It uses a 6.2 V supply decoupled at pin 4. The first two stages are gain controlled, and to ensure optimum noise performance, the first stage control is delayed until the second stage has been gain reduced by 15 dB. To bias the amplifier, balanced dc feedback is used which is decoupled at pins 2 and 6 and then fed to the input pins 3 and 5 by external 2.0 k resistors. The nominal bias voltage at these input pins is approximately 4.2 Vdc. Input capacitance between pins 3 and 5 which varies with gain reduction is provided. The capacitance is nominally 2.0 pF at zero gain reduction, rising to a maximum value of approximately 5.5 pF at 30 dB gain reduction. Improved weak signal performance results when the capacitance change is allowed to move the center frequency of the final tuned circuit of the IF filter. The input, because of the high IF gain, should be driven from a balanced differential source. For the same reason, care must be taken with the IF decoupling.

The IF output is rectified in a full wave envelope detector and detector non linearity is compensated by using a similar nonlinear element in a feedback output buffer amplifier. The detected 1.9 V_{p-p} video at pin 28 contains the sound intercarrier signal, and pin 28 is normally used as the sound takeoff point. The video frequency response, detector to pin 28, is shown in Figure 3 and the detector intermodulation performance can be seen by reference to Figure 4. Typical pin 28 waveforms and voltage levels are shown in Figure 6.

The video processing section of Monomax contains a contrast control, black level clamp, a beam current limiter and composite blanking. The video signal first passes through the contrast control. This has a range of 14:1 for a 0 V to 5.0 V change of voltage on pin 26, which corresponds to a change of video amplitude at pin 24 of 1.4 V to 0.1 V (black to white level). The beam current limiter operates on the contrast control, reducing the video signal when the bean current exceeds the limit set by external components. As the beam current increases, the voltage at pin 27 moves negatively from its normal value of 1.5 V, and at 1.0 V operates the contrast control, thus initiating beam limiting action. After the contrast control, the video is passed through a buffer amplifier and dc restored by the black level clamp circuit before being fed to pin 24 where it is blanked. The black level clamp, which is gated "on" during the second half of the flyback, maintains the video black level at 2.4 V ± 0.1 V under all conditions, including changes in contrast, temperature and power supply. The loop integrating capacitor is at pin 25 and is normally at a voltage of 3.3 V. The frequency response of the video at pin 24 is shown in Figure 3 and it is blanked to within 0.5 V of ground.

The AGC loop is a gated system, and for all normal variations of the IF input signal maintains the sync tip of a noise filtered video signal at a reference voltage

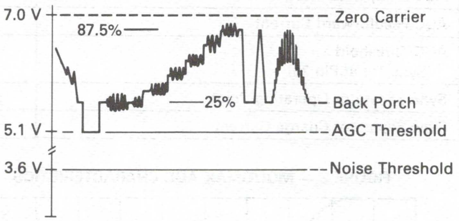


FIGURE 6A — PIN 28 SOUND OUTPUT

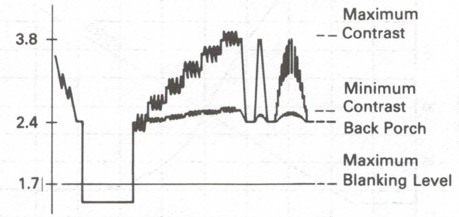


FIGURE 6B — PIN 24 — VIDEO OUTPUT

(5.1 V pin 28). The strobe for the AGC error amplifier is formed by gating together the flyback pulse with the separated sync pulse. Integration of the error signal is performed by the capacitor at pin 8, which forms the dominant AGC time constant. Improved noise performance is obtained by the use of a gated AGC system, noise protected by a dc coupled noise canceling circuit. The false AGC lock conditions, which can result from this combination, are prevented by an anti lockout circuit connected to the sync separator at pin 7. AGC lockout conditions, which occur due to large rapid changes of signal level are detected at pin 7 and recovery is ensured under these conditions by changing the AGC into a mean level system. The voltage at pin 10 sets the point at which tuner AGC takeover occurs and positive going tuner control, suitable for an NPN RF transistor, is available at pin 11. The maximum output is 5.5 V at 5.0 mA. A feed-forward output is provided at pin 9. This enables the AGC control voltage to be ac coupled into the tuner takeover control at pin 10. The coupling allows additional IF gain reduction during signal transient conditions, thus compensating for variations of AGC loop gain at the tuner AGC takeover point. In this way the AGC system stability and response are not degraded.

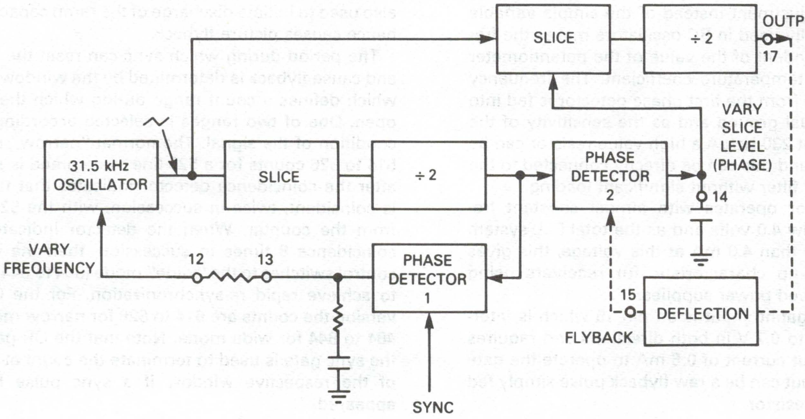
The previously mentioned noise protection is effected by detecting negative-going noise spikes at the video detector output. A dc coupled detector is used which turns on when a noise spike exceeds the video sync tip by 1.4 V. This pulse is then stretched and used to cancel the noise present on the delayed video at the input to the sync separator. Cancellation is performed by blanking the video to ground. Complete cancellation of the noise spike results from the stretching of the blanking pulse and the delay of the noise spike at the input to the sync separator. Protection of both the horizontal PLL and the AGC stems from the fact that both circuits use the noise cancelled sync for gating.

The composite sync is stripped from a delayed and filtered video in a peak detecting type of sync separator. The components connected to pin 7 determine the slice and tilt levels of the sync separator. For ideal horizontal sync separation and to ensure correct operation of AGC anti-lockup circuit, a relatively short time constant is required at pin 7. This time constant is less than optimum for good noise free vertical separation, giving rise to a vertical slice level near sync tip. An additional, longer, time-constant is therefore coupled to the first via a diode. With the correct choice of time constants, the diode is non conducting during the horizontal sync period, but conducts during the longer vertical period. This connects the longer time constant to the sync separator for the vertical period and stops the slice level from moving up to the sync tip. The separated composite sync is integrated internally, and the time constant is such that only the longer period vertical pulses produce a significant output pulse. The output is then fed to the vertical sync separator, which further processes the vertical pulse and provides increased noise protection. The selection of the external components connected to the vertical separator at pin 23 permits a wide range of performance options. A simple resistor divider from the 8.2 V regulated supply gives adequate performance for most conditions. The addition of an RC network will make the slice level adapt to varying sync amplitude and give improved weak signal performance. A resistor to the AGC voltage on pin 9 enables the sync slice level to be changed as a function of signal level. This further improves the low signal level separation while at the same time giving increased impulse noise protection on strong signals.

HORIZONTAL OSCILLATOR

The horizontal PLL (see Figure 7) is a 2-loop system using a 31.5 kHz oscillator which after a divider stage is locked to the sync pulse using phase detector 1. The control signal derived from this phase detector on pin 13 is fed via a high-value resistor to the frequency-

FIGURE 7 — HORIZONTAL OSCILLATOR SYSTEMS



control point on pin 12. The same divided oscillator frequency is also fed to phase detector 2, where the flyback pulse is compared with it and the resulting error used to change a variable slice level on the oscillator ramp waveform. This therefore changes the timing of the output square wave from the slicer and hence the timing of the buffered horizontal output on pin 17. (see Figure 8) The error on phase detector 2 is reduced until the phasing of the flyback pulse is correct with respect to the divided oscillator waveform, and hence with respect to the sync pulse.

To improve the pull-in and noise characteristics of the first PLL, the phase detector current is increased when the vertical lock indicator signals an unlocked condition and is decreased when locked. This increases the loop bandwidth and pull-in range when out of lock and decreases the loop bandwidth when in lock, thus improving the noise performance. In addition, the phase detector current during the vertical period is reduced in order to minimize the disturbance to the horizontal caused by the longer period vertical phase detector pulses.

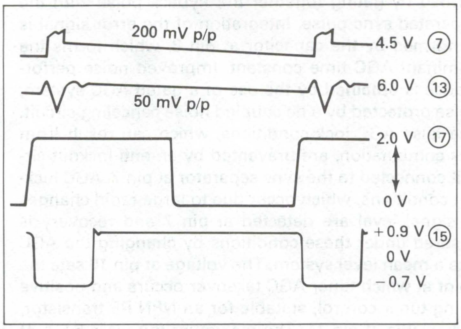
The oscillator itself is a novel design using an on-chip 50 pF silicon nitride capacitor which has a temperature drift of only 70 ppm/°C and negligible long term drift. This, in conjunction with an external resistor, gives a drift of horizontal frequency of less than 1Hz/°C — i.e., less than 100 Hz over the full operating temperature range of the chip. The pull-in range of the PLL is about ± 750 Hz, so normally this would eliminate the need for any customer adjustment of the frequency.

The second significant feature of this design is the use of a virtual ground at the frequency control point which floats at a potential derived from a divider across the power supply and this is the same divider which determines the end-points of the oscillator ramp. The frequency adjustment which is necessary to take up tolerances in the on-chip capacitor is fed in as a current to this virtual ground and when this adjustment current is derived from an external potentiometer across the same supply there is no frequency variation with supply voltage. Moreover, using the voltage from a potentiometer for the adjustment instead of the simple variable resistor normally used in RC oscillators makes the frequency independent of the value of the potentiometer and hence its temperature coefficient. The frequency control current from the first phase detector is fed into this same virtual ground and as the sensitivity of the control is about 230 Hz/μA a high value resistor can be used (680 kΩ) and this can be directly connected to the phase detector filter without significant loading.

This oscillator operates with almost constant frequency to below 4.0 volts and as the total PLL system consumes less than 4.0 mA at this voltage, this gives an ideal start-up characteristic for receivers using deflection-derived power supplies.

The flyback gating input is on pin 15 which is internally clamped to 0.7 V in both directions and requires a negative input current of 0.6 mA to operate the gate circuit. This input can be a raw flyback pulse simply fed via a suitable resistor.

FIGURE 8 — HORIZONTAL WAVEFORMS



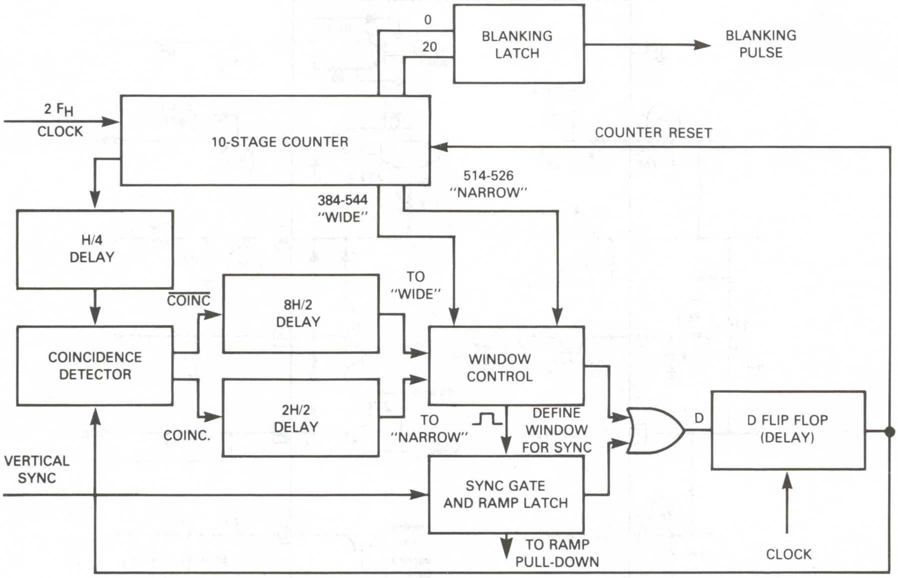
VERTICAL SYSTEM

An output switching signal is taken from the 31.5 kHz oscillator to clock the vertical counter which is used in place of a conventional vertical oscillator circuit. The counter is reset by the vertical sync pulse but the period during which it is permitted to reset is controlled by the window control. Normally, when the counter is running synchronously, the window is narrow to give some protection against spurious noise pulses in the sync signal. If the counter output is not coincident with sync however, after a short period the window opens to give reset over a much wider count range, leading to a fast picture roll towards lock. The vertical sync, gated by the counter, then resets a ramp generator on pin 20 and the 1.5 volt p-p ramp is buffered to pin 22 by the vertical preamplifier. A differential input to the preamp on pin 21 compares the signal generated across the resistor in series with the deflection coils with the generated ramp and thus controls shape and amplitude of the coil current.

The basic block diagram of the countdown system is shown in Figure 9. The 31.5 kHz (2 F_H) clock from the horizontal oscillator drives a 10-stage counter circuit which is normally reset by the vertical sync pulse via the sync gate, OR gate and D flip-flop. This D input is also used to initiate discharge of the ramp capacitor and hence causes picture flyback.

The period during which sync can reset the counter and cause flyback is determined by the window control which defines a count range during which the gate is open. One of two ranges is selected according to the condition of the signal. The normal "narrow" range is 514 to 526 counts for a 525 line system and is selected after the coincidence detector indicates that the reset is coincident, twice in succession, with the 525 count from the counter. When the detector indicates non-coincidence 8 times in succession, then the window control switches to the "wide" mode (384 to 544 counts) to achieve rapid re-synchronization. For the 625 line version the counts are 614 to 626 for narrow mode and 484 to 644 for wide mode. Note that the OR gate after the sync gate is used to terminate the count at the end of the respective window if a sync pulse has not appeared.

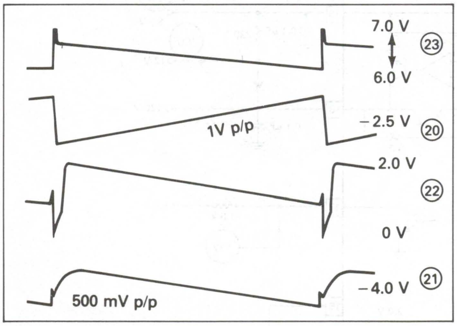
FIGURE 9 — MONOMAX VERTICAL COUNTDOWN


0
20
BLANKING LATCH
BLANKING PULSE
2 F_H CLOCK
10-STAGE COUNTER
COUNTER RESET
514-526 "NARROW"
384-544 "WIDE"
H/4 DELAY
TO "WIDE"
$\overline{\text{COINC}}$
8H/2 DELAY
COINCIDENCE DETECTOR
WINDOW CONTROL
2H/2 DELAY
COINC.
TO "NARROW"
DEFINE WINDOW FOR SYNC
D
D FLIP FLOP (DELAY)
VERTICAL SYNC
SYNC GATE AND RAMP LATCH
TO RAMP PULL-DOWN
CLOCK

This method accepts non-standard signals almost in the same way as a conventional triggered RC oscillator and has a similar fast lock-in time. However, the use of a window control on the counter reset ensures that when locked with a normal standard broadcast signal the counter will reject most spurious noise pulses.

The blanking output is provided from a latch which is set by the counter reset pulse and terminated by count 20 from the counter chain.

FIGURE 10 — VERTICAL WAVEFORMS



POWER SUPPLY

The power supply regulator, although of simple design, provides two independent power supplies — one for the horizontal PLL section and the other for the remainder of the chip. The supplies share the same reference voltage but the design of the main regulator is such that it can be switched on independently to give minimum loading on the "bleed" voltage source during start-up phase of a deflection-derived supply system.

FIGURE 11 — POWER SUPPLY CIRCUIT

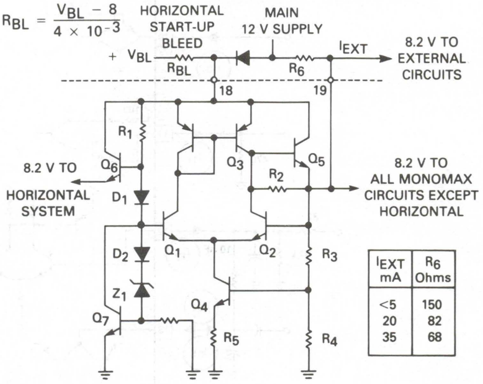

$R_{BL} = \frac{V_{BL} - 8}{4 \times 10^{-3}}$
HORIZONTAL START-UP BLEED
MAIN 12 V SUPPLY
+ V_{BL}
R_{BL}
R_6
I_{EXT}
8.2 V TO EXTERNAL CIRCUITS
18
19
R_1
Q_3
Q_5
8.2 V TO HORIZONTAL SYSTEM
Q_6
D_1
R_2
8.2 V TO ALL MONOMAX CIRCUITS EXCEPT HORIZONTAL
D_2
Q_1
Q_2
R_3
Z_1
Q_4
Q_7
R_5
R_4
I_{EXT} mA
R_6 Ohms
<5
20
35
150
82
68

FIGURE 12 — TEST CIRCUIT DIAGRAM

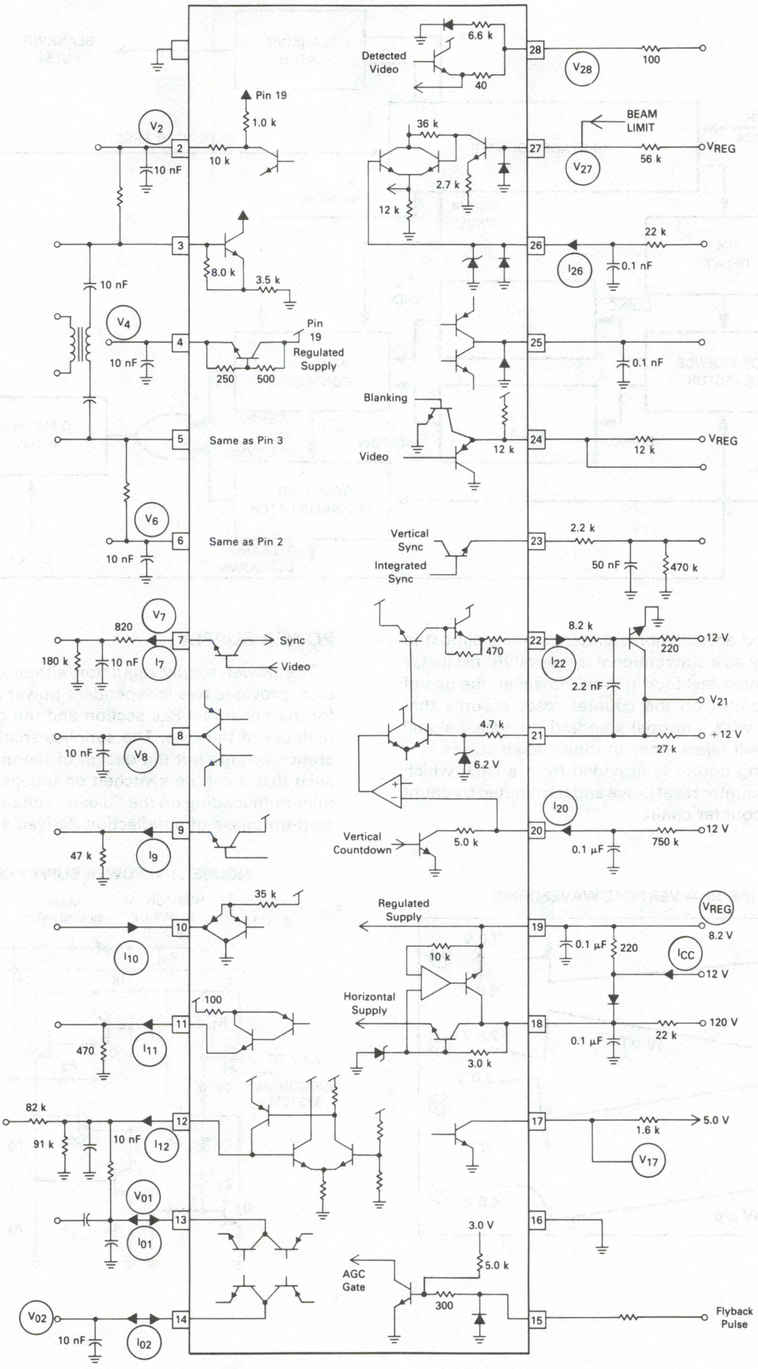
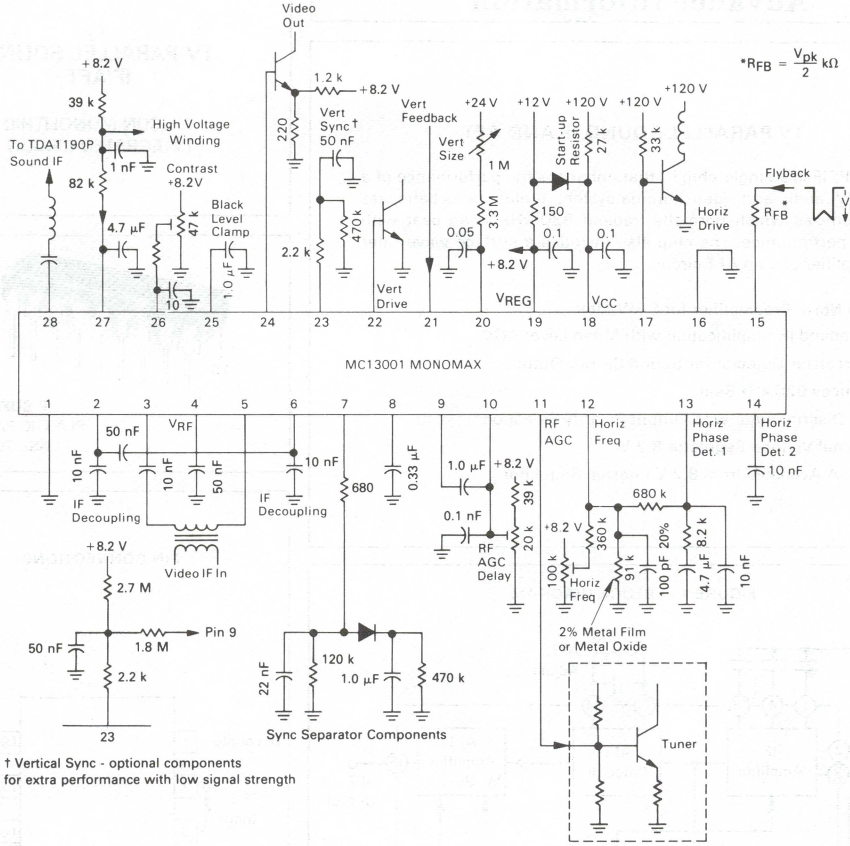

Detected Video
6.6 k
40
100
V28
Pin 19
1.0 k
V2
10 k
10 nF
36 k
2.7 k
12 k
BEAM LIMIT
56 k
VREG
V27
22 k
I26
0.1 nF
8.0 k
3.5 k
10 nF
V4
Pin 19 Regulated Supply
250
500
Blanking
Video
Same as Pin 3
12 k
V6
Same as Pin 2
Vertical Sync
Integrated Sync
2.2 k
50 nF
470 k
V7
820
180 k
I7
Sync
Video
470
8.2 k
220
12 V
I22
2.2 nF
V21
4.7 k
+12 V
27 k
6.2 V
V8
47 k
I9
Vertical Countdown
5.0 k
I20
0.1 µF
750 k
35 k
I10
Regulated Supply
10 k
0.1 µF
220
ICC
8.2 V
100
Horizontal Supply
I11
3.0 k
120 V
82 k
91 k
I12
V01
I01
17
1.6 k
5.0 V
V17
3.0 V
5.0 k
AGC Gate
300
V02
I02
Flyback Pulse
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
18
19
20
21
22
23
24
25
26
27
28

FIGURE 13 — TYPICAL APPLICATION


Video Out
+8.2 V
1.2 k
+8.2 V
39 k
High Voltage Winding
To TDA1190P Sound IF
1 nF
82 k
Contrast +8.2V
47 k
Black Level Clamp
4.7 μF
10
1.0 μF
220
Vert Sync†
50 nF
2.2 k
470 k
Vert Feedback
Vert Size
Vert Drive
+24 V
1 M
3.3 M
0.05
+8.2 V
+12 V
Start-up Resistor
150
0.1
VREG
+120 V
27 k
0.1
VCC
+120 V
33 k
+120 V
Horiz Drive
Flyback
RFB*
Vpk
*RFB = Vpk/2 kΩ
28
27
26
25
24
23
22
21
20
19
18
17
16
15
MC13001 MONOMAX
1
2
3
4
5
6
7
8
9
10
11
12
13
14
50 nF
VRF
10 nF
10 nF
50 nF
10 nF
IF Decoupling
IF Decoupling
Video IF In
680
0.33 μF
1.0 μF
+8.2 V
39 k
0.1 nF
20 k
RF AGC Delay
RF AGC
Horiz Freq
Horiz Phase Det. 1
Horiz Phase Det. 2
10 nF
680 k
+8.2 V
360 k
100 k
Horiz Freq
91 k
100 pF 20%
8.2 k
4.7 μF
10 nF
2% Metal Film or Metal Oxide
Tuner
+8.2 V
2.7 M
1.8 M
Pin 9
50 nF
2.2 k
23
22 nF
120 k
1.0 μF
470 k
Sync Separator Components

† Vertical Sync - optional components for extra performance with low signal strength

MC13010P

MOTOROLA

Advance Information

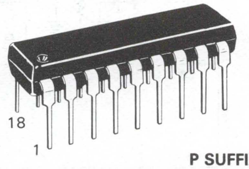
TV PARALLEL SOUND IF/AFT

SILICON MONOLITHIC INTEGRATED CIRCUIT

TV PARALLEL SOUND IF AND AFT

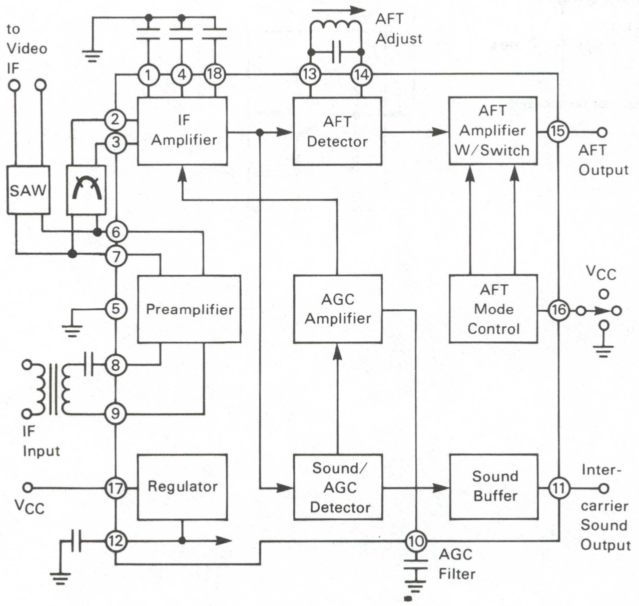
The PSIF is a single-chip IC that enhances the performance of a color TV, audio and video/chroma system. It eliminates bandpass compromises which normally tradeoff 920 kHz video beat with sound performance. The chip also includes a surface wave filter preamplifier and an AFT circuit.

- Low Noise Preamplifier for SAW filter
- Wideband IF Amplification with Mean Level AGC
- Intercarrier Detector for Sound Carrier Output
- Reduces 920 kHz Beat
- AFT Discriminator with Output Polarity Selection
- Internal Voltage Regulator 8.2 V
- 30 mA Available from 8.2 V Internal Regulator

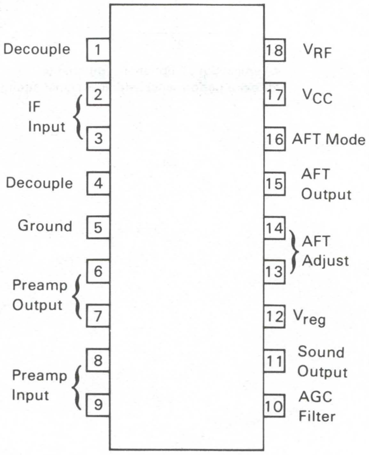


P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — BLOCK DIAGRAM


to Video IF
SAW
IF Input
VCC
AFT Adjust
IF Amplifier
AFT Detector
AFT Amplifier W/Switch
AFT Output
Preamplifier
AGC Amplifier
AFT Mode Control
VCC
Regulator
Sound/AGC Detector
Sound Buffer
Inter-carrier Sound Output
AGC Filter
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

PIN CONNECTIONS


Decouple 1
IF Input 2
3
Decouple 4
Ground 5
Preamp Output 6
7
Preamp Input 8
9
18 V_{RF}
17 V_{CC}
16 AFT Mode
15 AFT Output
14 AFT Adjust
13
12 V_{reg}
11 Sound Output
10 AGC Filter

This document contains information on a new product. Specifications and information herein are subject to change without notice.

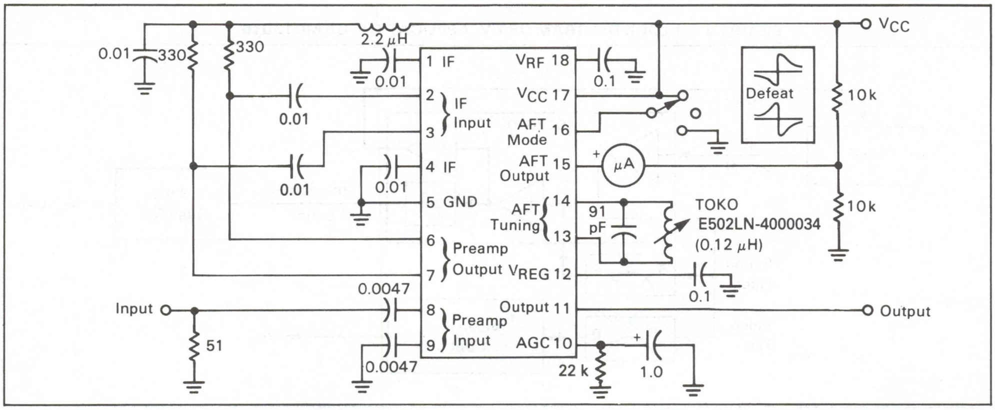
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	Vdc
Regulator Output Current	I_{REG}	30	mAdc
Thermal Resistance	$R_{\theta JA}$	70	°C/W
Power Dissipation (Package Limitation)	P_D	1.1	W
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_A = 25°C, Test Circuit of Figure 2, unless otherwise noted)

Static Characteristics	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	35	—	50	mAdc
Regulator Voltage, Pin 12	V_{reg}	7.6	8.2	8.8	Vdc
RF Supply Voltage, Pin 18	V_{RF}	5.8	6.5	7.2	Vdc
Preamplifier Current, Pins 6, 7		4.0	6.6	7.5	mAdc
Dynamic Characteristics					
Preamp Gain (Block A Removed)	Av	—	12	—	dB
IF Sensitivity, Output 1.5 V_{pp} Typ. Input 45.75 MHz, 30% AM @ 1.0 kHz, Differential Pins 2, 3		—	80	—	μVrms
AGC Range, Input CW for Output Change of ±0.25 Vdc		—	48	—	dB
Intercarrier Sound Output (Beat), Input 45.75 MHz, 2.2 mVrms; 41.25 MHz, 0.7 mVrms		40	60	100	mVrms
IF Bandwidth (3.0 db)	f_{max}	—	80	—	MHz
Preamplifier Input Resistance Preamplifier Input Capacitance	R_{in} C_{in}	— —	1.5 11.5	— —	kΩ pF
IF Input Resistance IF Input Capacitance	R_{in}' C_{in}	— —	2.2 4.0	— —	kΩ pF
Preamplifier Max Input Signal (Single Ended)	V_{in}	—	50	—	mVrms
IF Max Input Signal (Differential)	V_{in}	—	50	—	mVrms
Noise Figure IF, Max Gain Noise Figure Preamplifier		— —	6.0 5.0	— —	dB
AFT Center-Frequency Slope		0.75	4.0	—	μA/kHz
AFT Output Max, 1.0 MHz Detuning		—	±300	—	μA

FIGURE 2 — TEST CIRCUIT



0.01
330
330
2.2 μH
0.01
0.01
0.01
0.01
1 IF
2
3
IF Input
4 IF
5 GND
6
7
Preamp Output
8
9
Preamp Input
VRF 18
VCC 17
AFT Mode 16
AFT Output 15
AFT Tuning 14
13
VREG 12
Output 11
AGC 10
0.1
μA
Defeat
10k
10k
91 pF
TOKO E502LN-4000034 (0.12 μH)
0.1
VCC
Output
Input
51
0.0047
0.0047
22 k
1.0

Description

The MC13010 T.V. Parallel Sound IF/AFT is designed to be part of a high performance color television system. Its primary function is to provide a complete separate IF amplifier for sound, leaving the normal IF to be concerned only with video. Secondary functions include an AFT detector and a SAW preamp.

In most present day color television receivers, sound and video are processed by the same IF amplifier and, in many cases, the same synchronous or pseudosynchronous detector. This imposes undesirable compromises in video and sound performance. Particularly in the U.S., the avoidance of a color/sound beat product (920 kHz) can only be achieved at the expense of sound quieting and sensitivity. Earlier solutions involved a single IF amplifier driving two detectors, with numerous interstage alignments required.

A method of solving these problems is to process the sound and video separately, directly from the tuner output. The MC13010 provides the second complete IF channel, with its own wideband detector and AGC. This permits both video IF and sound IF to be free of tuned elements, except at their inputs. (See Figure 3.)

Preamplifier

The preamp is included to compensate for the high insertion loss of a Surface Acoustic Wave filter. This SAW filter may have two outputs with different responses, or it may serve only the video signal path. The preamp is optional if an LC filter is used. In any case, the selectivity ahead of the video IF must provide deep trapping of the sound carrier, while the sound bandpass is relatively broad and flat between the picture and sound carriers.

The Sound IF

The overall gain of 80 dB and gain control range of 48 dB equals the video IF's of earlier designs. This allows the full improvement of the system architecture to be realized. The AGC in the MC13010 is a peak-detecting type, driven internally from the sound detector, and requiring only one external filter. The general characteristic of the IF gain and gain control are given in Figure 4. The intercarrier sound output (Pin 11) is typically about 60 mV$_{rms}$, which easily overcomes a lossy intercarrier filter and meets the input needs of even the least sensitive FM sound IF ICs.

AFT

The AFT detector is a quadrature type operating at the picture IF frequency, with only one external L-C to be aligned. The polarity of the AFT output may be changed by taking the mode control (Pin 16) high or low. If the control pin is left open, the AFT is defeated.

Additional Applications

The MC13010 is an ideal part for stand-alone AFT. It contains the entire active system to provide a tuner with "self control". (See Figure 6.)

This device performs AM detection at the intercarrier sound output. Therefore, AM modulated digital data may be recovered. This function may be useful in cable systems where digital coding is employed.

FIGURE 4 — GAIN AND AGC CHARACTERISTICS

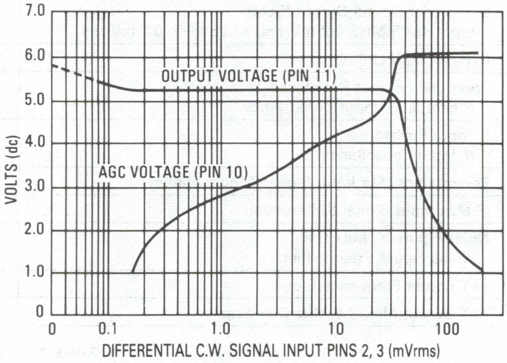


FIGURE 3 — BLOCK DIAGRAM OF T.V. APPLICATION OF MC13010

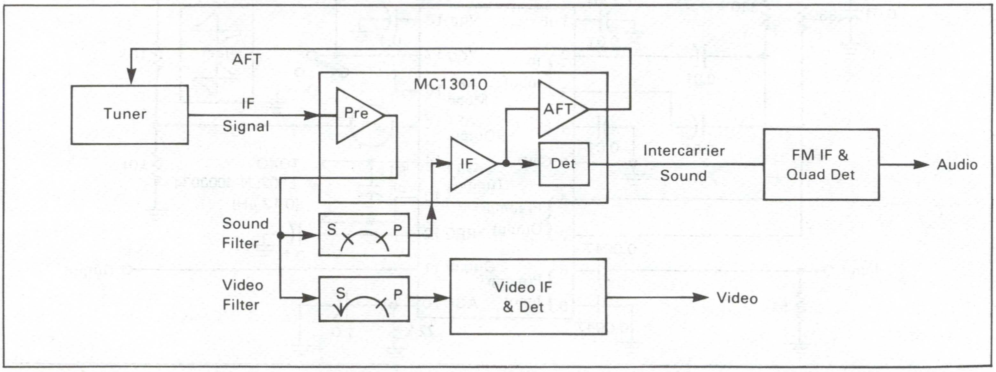
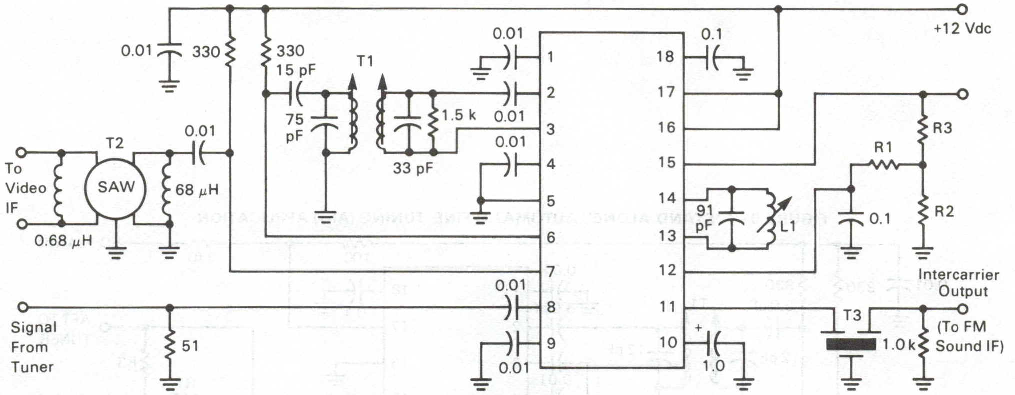
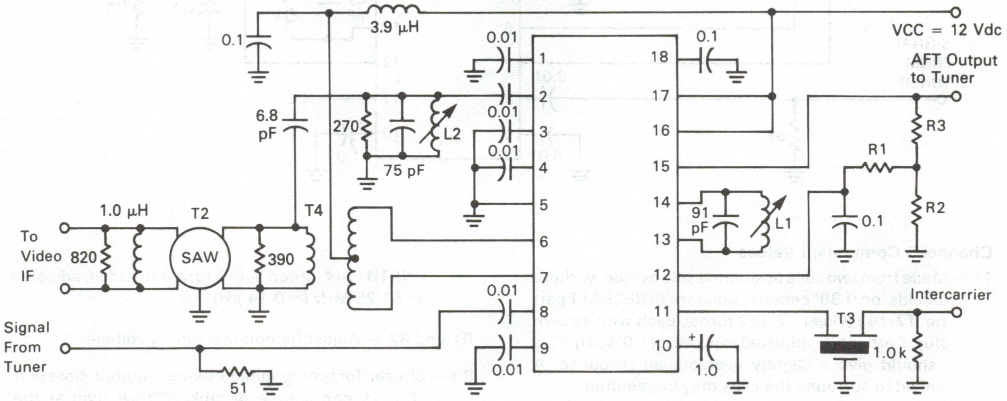


FIGURE 5(A) — TYPICAL T.V. APPLICATION



+12 Vdc
0.01
330
330
15 pF
T1
75 pF
1.5 k
0.01
0.01
0.01
33 pF
T2
To Video IF
SAW
68 μH
0.68 μH
0.01
0.1
R3
R1
R2
0.1
91 pF
L1
Intercarrier Output
Signal From Tuner
51
0.01
0.01
T3
1.0 k
(To FM Sound IF)
1.0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

FIGURE 5(B) — TYPICAL APPLICATION



3.9 μH
0.1
VCC = 12 Vdc
AFT Output to Tuner
0.01
0.1
6.8 pF
270
75 pF
L2
0.01
0.01
R3
R1
R2
0.1
91 pF
L1
1.0 μH
T2
T4
To Video IF
820
SAW
390
Intercarrier
T3
1.0 k
Signal From Tuner
51
0.01
0.01
1.0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

Shown above are two approaches to using the MC13010 in TV designs. The simpler circuit 5(a) offers the lowest cost, but the 12 dB of preamp gain does not nearly overcome the 20 to 25 dB of SAW filter loss. (Bearing in mind that discrete L/C approaches also incur some loss at this point, the 5(a) circuit is probably about equal in gain.) The transformer T4 in Figure 5(b) takes advantage of the high impedance current source nature of the preamp outputs, Pins 6 and 7, to pick up about another 6.0 dB of gain. Even more may be possible with more primary turns. When using the coil information given at the right, note that it is based on very limited experience and is offered only as a general guideline.

Experimental values for 45 MHz IF:

T1 — Primary: TOKO E502LN-4000034
Secondary: TOKO E502LN-7000037, in shield case

T2 — Video IF Surface Acoustic Wave (SAW) Filter: muRata, SAF 45MC02Z

T3 — Ceramic Intercarrier Output Filter: muRata SFE 4.5 MB

T4 — TOKO KANAS-K7060EK

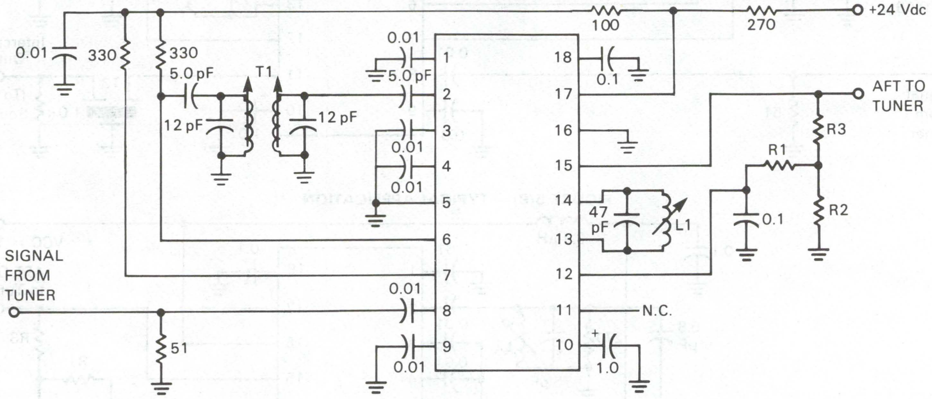
L1 — TOKO E502LN-4000034 or J. W. Miller 48A147MPC with shield case, tuned to 45.75, L ≈ 0.12 μH.

L2 — Same part as L1, except tuned to 44 MHz and loaded with 270 Ω

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

FIGURE 6 — "STAND-ALONE" AUTOMATIC FINE TUNING (AFT) APPLICATION


+24 Vdc
100
270
0.01
330
330
5.0 pF
T1
0.01
5.0 pF
12 pF
12 pF
0.01
0.01
0.1
AFT TO TUNER
R3
R1
R2
0.1
47 pF
L1
SIGNAL FROM TUNER
0.01
51
0.01
N.C.
+
1.0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

Channel 3 Component Values

T1 — Made from two coils positioned side by side, without shields, on 0.38" centers. Coils are COILCRAFT part no. T7-142 (violet - 7-1/2 turns), each with its own slug, Carbonal E, adjusted to 63 MHz (≈ 0.4 μH). This should give a slightly overcoupled response. A shield to surround the coils may be required.

L1 — COILCRAFT UNI-7/150 (blue 6-1/2 turns) or UNI-10/144 (green 5-1/2 turns) shielded, adjusted to 61.25 MHz (≈ 0.14 μH)

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

MOTOROLA

MC13020P

Advance Information

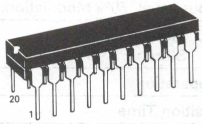
MOTOROLA CQUAM® AM STEREO DECODER

This circuit is a complete one-chip full-feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L + R signal, and decodes L − R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full-Wave Envelope Detection for L + R
- PLL Detection for L − R
- 25 Hz Pilot Presence Required To Receive L − R
- Pilot Acquisition Time 300 ms For Strong Signals, Time Extended For Noise Conditions To Prevent "Falsing"
- Internal Level Detector Can Be Used As AGC Source

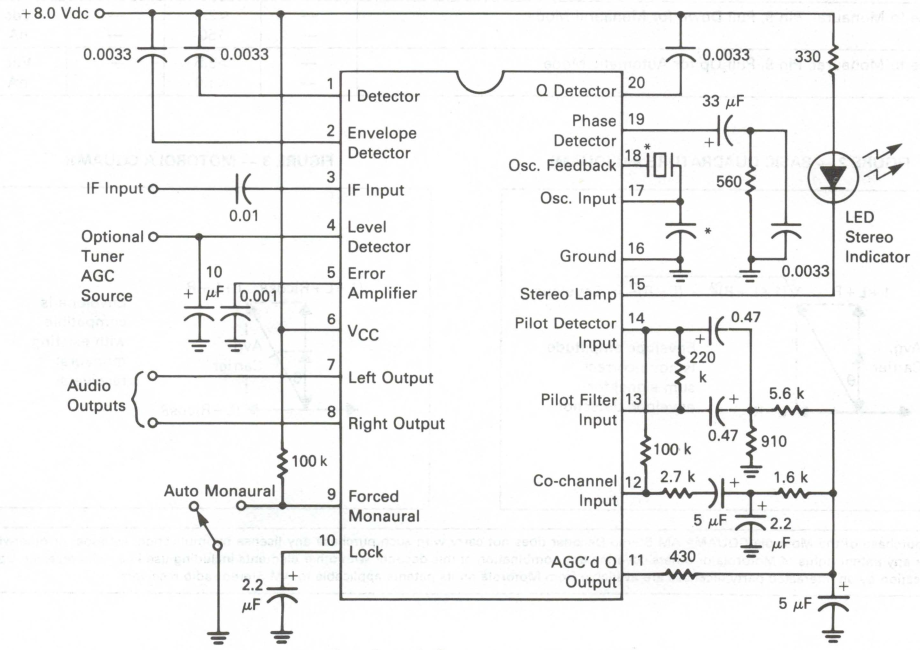
MOTOROLA CQUAM®
AM STEREO
DECODER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

FIGURE 1 — TYPICAL APPLICATION


+8.0 Vdc
0.0033
0.0033
IF Input
0.01
Optional Tuner AGC Source
10 μF
0.001
Audio Outputs
100 k
Auto Monaural
2.2 μF
1 I Detector
2 Envelope Detector
3 IF Input
4 Level Detector
5 Error Amplifier
6 VCC
7 Left Output
8 Right Output
9 Forced Monaural
10 Lock
20 Q Detector
19 Phase Detector
18 Osc. Feedback
17 Osc. Input
16 Ground
15 Stereo Lamp
14 Pilot Detector Input
13 Pilot Filter Input
12 Co-channel Input
11 AGC'd Q Output
0.0033
330
33 μF
560
0.0033
LED Stereo Indicator
0.47
220 k
0.47
5.6 k
910
100 k
2.7 k
5 μF
2.2 μF
1.6 k
430
5 μF

*muRata Ceramic Resonator — CSA3.60MT7
and Temp. Comp. Capacitor — CSC500K7

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15		50	mAdc
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Circuit Of Figure 1 Unless Otherwise Noted.)

Characteristic		Min	Typ	Max	Unit
Power Supply Operating Range		6.0	8.0	12.0	Vdc
Supply Line Current Drain, Pin 6		—	30	—	mAdc
Input Signal Level, Unmodulated, Pin 3		—	200	350	mVRMS
Audio Output Level, 50% Modulation, L only or R only		—	220	—	mVRMS
Audio Output Level, 50% Modulation, Monaural		—	110	—	mVRMS
Output THD	Monaural Stereo	— —	0.5 1.0	— —	%
Channel Separation		—	30	—	dB
Pilot Acquisition Time		—	300	—	ms
Input Impedance	R_{in} C_{in}	20	27 6.0	—	kΩ pF
Output Impedance		—	100	150	Ω
Level Detector Filter Voltage, Pin 4,	0 signal 200 mVRMS Signal	— —	1.7 2.5	— —	Vdc
Lock Detector Filter Voltage, Pin 10	In Lock Out of Lock	— —	4.3 0.8	— —	Vdc
Force to Monaural, Pin 9, Pull Down for Monaural Mode		— —	<2.5 150	— —	Vdc nA
Force to Monaural, Pin 9, Pull Up for Automatic Mode		— —	>3.5 <1.0	— —	Vdc nA

FIGURE 2 — BASIC QUADRATURE AM (QUAM)

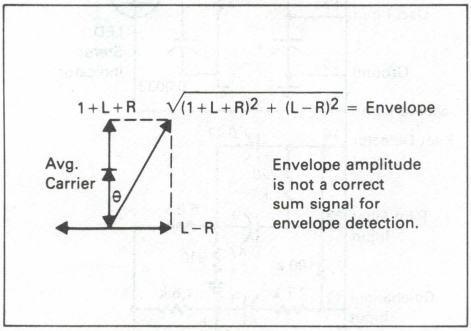
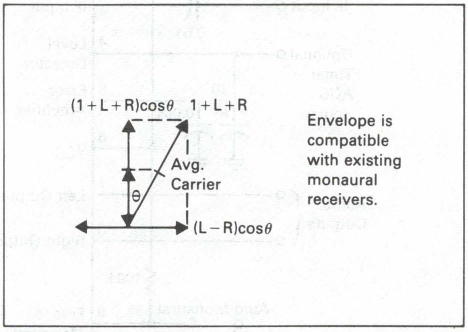
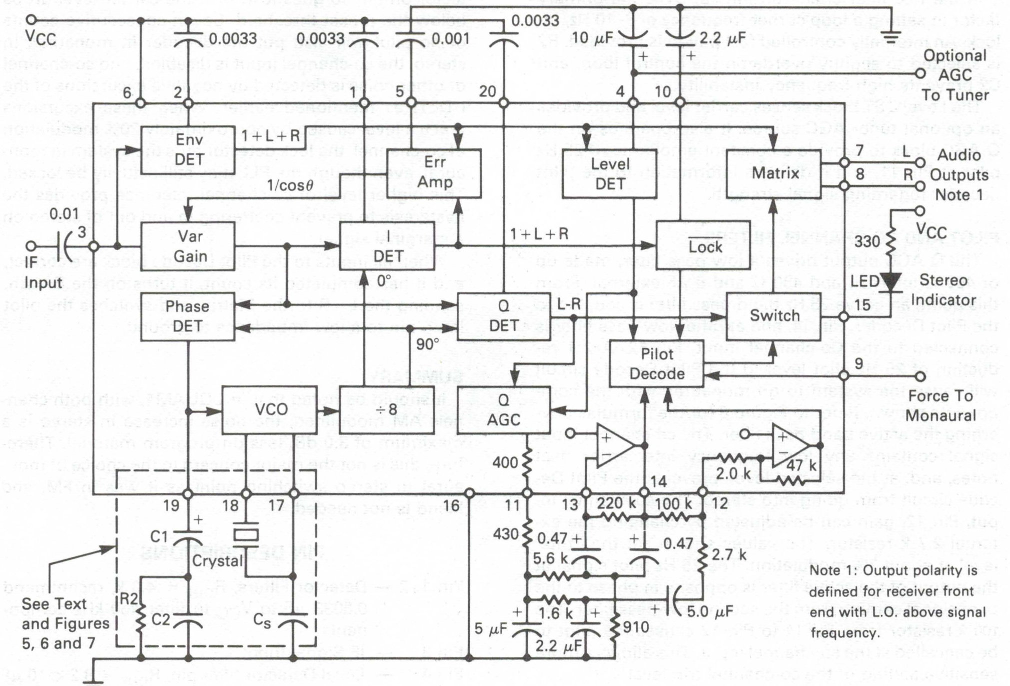

$1+L+R$
$\sqrt{(1+L+R)^2 + (L-R)^2}$ = Envelope
Avg. Carrier
θ
$L-R$
Envelope amplitude is not a correct sum signal for envelope detection.

FIGURE 3 — MOTOROLA CQUAM®


$(1+L+R)\cos\theta$
$1+L+R$
Avg. Carrier
θ
$(L-R)\cos\theta$
Envelope is compatible with existing monaural receivers.

The purchase of the Motorola CQUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

FIGURE 4 — BLOCK DIAGRAM



VCC
0.0033
0.0033
0.001
0.0033
10 μF
2.2 μF
Optional AGC To Tuner
6
2
1
5
20
4
10
Env DET
1+L+R
Err Amp
1/cosθ
Level DET
Matrix
7
8
L
R
Audio Outputs Note 1
0.01
3
IF Input
Var Gain
I DET
0°
1+L+R
Lock
VCC
330
LED
Stereo Indicator
Phase DET
Q DET
L-R
Switch
15
90°
Pilot Decode
9
Force To Monaural
VCO
÷8
Q AGC
400
47 k
2.0 k
14
19
18
17
16
11
13
220 k
100 k
12
C1
Crystal
430
0.47
0.47
5.6 k
2.7 k
See Text and Figures 5, 6 and 7
R2
C2
Cs
1.6 k
5.0 μF
5 μF
910
2.2 μF

Note 1: Output polarity is defined for receiver front end with L.O. above signal frequency.

MOTOROLA CQUAM® — COMPATIBLE QUADRATURE AM STEREO

INTRODUCTION

In CQUAM®, conventional quadrature amplitude modulation has been modified by multiplying each axis by cosθ as shown in Figures 2 and 3. The resulting carrier envelope is 1+L+R, i.e., a correct sum signal for monaural receivers and for stereo receivers operating in monaural mode. A 25 Hz pilot signal is added to the L−R information at a 4% modulation level.

THE DECODER

The MC13020P takes the output of the AM IF amplifier and performs the complete CQUAM® decoding function. In the absence of a good stereo signal, it produces an undegraded monaural output. Note in Figure 4 that the L+R information delivered to the output always comes from the envelope detector (Env DET).

The MC13020P decodes the stereo information by first converting the CQUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides the 1/cosθ correction factor, which is then multiplied by the CQUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be synchronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase-locked, divided-down VCO. The output of the I DET is 1+L+R, with the added benefit (over the Env DET) of being able to produce a negative output on strong co-channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the L−R and pilot information.

THE VCO

The VCO operates at 8 times the IF input frequency, which ensures that it is out-of-band, even when a 260 kHz IF frequency is used. Typically a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front-end mistuning. Pull-in capability of ± 100 Hz at 450 kHz is typical, and de-Q-ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front-ends. By comparison, ceramic and L−C VCO circuits offer pull-in range in the order of ±2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figures 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8–10 Hz, in-lock. An internally controlled fast pull-in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

PILOT AND CO-CHANNEL FILTERS

The Q AGC output drives a low pass filter, made up of 400 Ω internal, and 430 Ω and 5 μF external. From this point, an active 25 Hz band-pass filter is coupled to the Pilot Decoder, Pin 14, and another low-pass filter is connected to the Co-channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band-pass filter. The co-channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co-channel input, Pin 12, gain can be adjusted by changing the external 2.7 k resistor. The values shown set the "trip" level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low-pass filter. The 100 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co-channel input. This allows a more sensitive setting of the co-channel trip level.

THE PILOT DECODER

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio, the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co-channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops below the preset threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co-channel input is disabled, and co-channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co-channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co-channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L − R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

SUMMARY

It should be noted that in CQUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

PIN DESCRIPTIONS

Pin 1, 2 — Detector Filters, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz components.
Pin 3 — IF Signal Input
Pin 4 — Level Detector filter pin, R_{out} = 8.2 k, 10 μF to ground sets the AGC time constant. High impedance output, needs buffer.
Pin 5 — Error Amp compensation to stabilize the Var Gain feedback loop
Pin 6 — V_{CC}, 6–12 Vdc, suitable for low V_{batt} automotive operation, but must be protected from "high line" condition.
Pin 7, 8 — Left and Right Outputs, NPN emitter followers
Pin 9 — Forced Monaural, MOS or TTL controllable
Pin 10 — Lock detector filter, R_{out} = 27 k, recommend 2.2 μF to ground.
Pin 11 — AGC'd Q output, NPN emitter follower with 400 Ω from emitter to Pin 11
Pin 12 — Co-channel Input, 2.0 k series in and 47 k feedback
Pin 13 — Pilot Filter Input to op amp, see Figure 8
Pin 14 — Pilot Decode Input (op amp output) emitter follower, R_{out} = 100 Ω
Pin 15 — Stereo Lamp, open-collector of an NPN common emitter stage, can sink 50 mA, V_{sat} = 0.3 V at 5.0 mA
Pin 16 — Ground
Pin 17 — Oscillator input, R_{in} = 10 k, do not dc connect to Pin 18 or ground
Pin 18 — Oscillator feedback, NPN emitter, R_{out} = 100 Ω
Pin 19 — Phase Detector Output, current source to filter
Pin 20 — Detector Filter, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz

FIGURE 5 — CERAMIC VCO

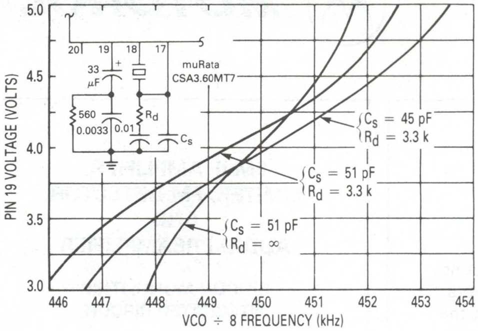


FIGURE 6 — L–C VCO

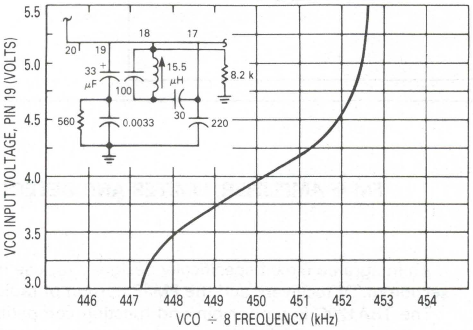


FIGURE 7 — CRYSTAL VCO

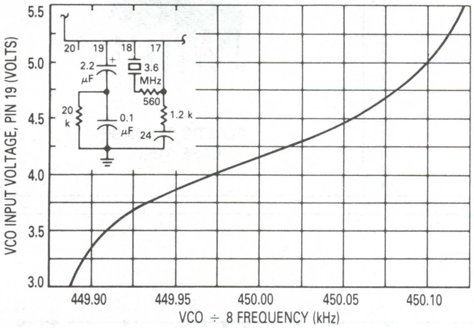
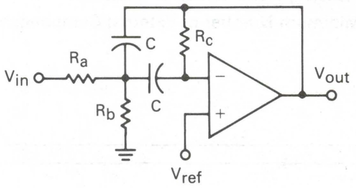


FIGURE 8 — ACTIVE BAND-PASS FILTER


Vin
Ra
Rb
C
C
Rc
Vout
Vref
−
+

$$R_c = \frac{Q}{\pi f_o C}$$

$$R_a = \frac{R_c}{2 A_o}$$

$$R_b = \frac{R_a R_c}{4Q^2 R_a - R_c}$$

where:

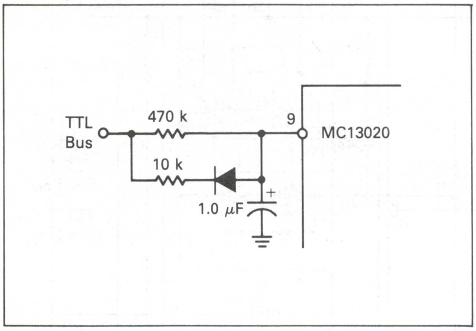
f_o = center frequency
A_o = gain at f_o
$Q \leq 10$

Choose values for F_o, A_o, Q, and convenient C, solve for resistors

In this application:

f_o = 25 Hz	R_a = 5.6 k
A_o = 20	R_b = 910
$Q \simeq 8.2$	R_c = 220 k
C = 0.47 µF	

FIGURE 9 — FORCED MONAURAL OPTIONAL DELAY CIRCUIT


TTL Bus
470 k
10 k
1.0 µF
9
MC13020

TBA120C

MOTOROLA

FM IF AMPLIFIER, LIMITER AND DETECTOR

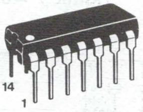
An integrated circuit specifically designed for use in the sound section of TV receivers and the FM/IF portion of radio receivers.

The TBA120C is pin for pin and function compatible with the proelectron type TBA120S but includes an improved dc volume control, which makes "grouping" or selection unnecessary.

- Excellent 3.0 dB Limiting
- High A.M. Rejection
- Wide Supply Voltage Range
- Auxiliary Zener Diode & Transistor
- Minimum Number of External Components Required

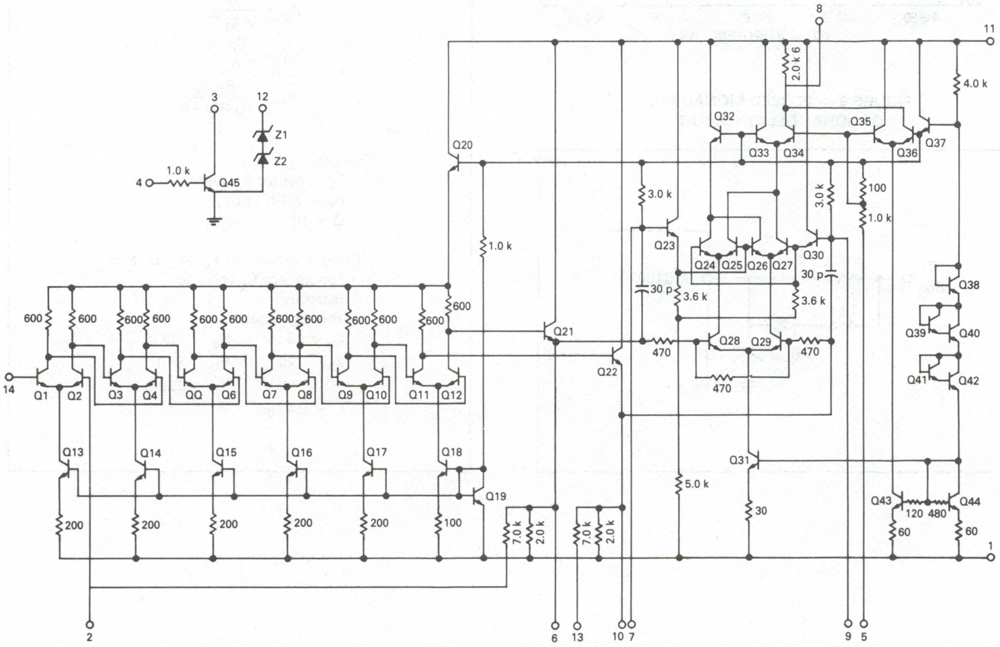
FM IF AMPLIFIER, LIMITER, FM DETECTOR AND AUDIO PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646-05

CIRCUIT SCHEMATIC


8
11
2.0 k 6
4.0 k
3
12
Z1
Z2
4
1.0 k
Q45
Q20
Q32
Q33
Q34
Q35
Q36
Q37
3.0 k
3.0 k
100
1.0 k
Q23
Q24
Q25
Q26
Q27
Q30
30 p
30 p
3.6 k
3.6 k
1.0 k
Q38
Q39
Q40
Q41
Q42
600
600
600
600
600
600
600
600
600
600
600
600
14
Q1
Q2
Q3
Q4
QQ
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q21
Q22
470
470
470
Q28
Q29
Q13
Q14
Q15
Q16
Q17
Q18
Q19
200
200
200
200
200
100
7.0 k
2.0 k
7.0 k
2.0 k
5.0 k
Q31
30
Q43
Q44
120
480
60
60
1
2
6
13
10
7
9
5

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	+18	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	−65 to +150	°C

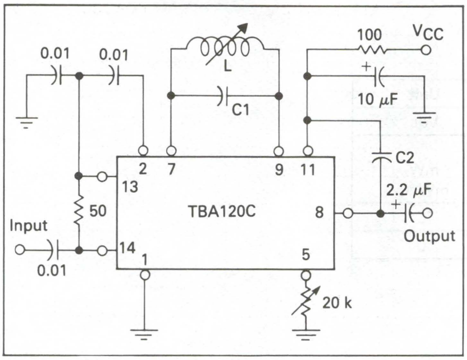
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 12 V, R = 20 k, Test circuit: Figure 1)

Characteristic	Min	Typ	Max	Unit
Supply Voltage Range	6.0	—	18	Volts
Supply Current	10	14	18	mA
Audio Output (f_o = 5.5 MHz, Δf = 50 kHz, Q = 45)	—	1.0	—	Volts RMS
Audio Output (f_o = 10.7 MHz, Δf = 75 kHz, Q = 35)	—	0.38	—	Volts RMS
3.0 dB Limiting (f_o = 5.5 MHz, Δf = 50 kHz, Q = 45)	—	30	60	μVRMS
3.0 dB Limiting (f_o = 10.7 MHz, Δf = 75 kHz, Q = 35)	—	40	—	μVRMS
A.M. Rejection (f_o = 5.5 MHz, RF Input: 500 μV)	45	—	—	dB
A.M. Rejection (f_o = 10.7 MHz, RF Input: 500 μV)	40	—	—	dB
Volume Control Range	65	75	—	dB
Output Impedance	—	2.6	—	kΩ

ELECTRICAL CHARACTERISTICS OF AUXILIARY Z DIODE AND TRANSISTOR Q45 (T_A = +25°)

Characteristic	Min	Typ	Max	Unit
Z-Voltage @ 5.0 mA (Pin 12)	11.2	—	13.2	Volts
Z-Resistance (Pin 12) @ 1.0 kHz, 5.0 mA	—	15	—	Ω
Q45 Breakdown Voltage V_{CEO}	13	—	—	Volts
Q45 Current Gain @ I_C = 1.0 mA, V_{CE} = 5.0 V	40	100	—	—

FIGURE 1 — TEST CIRCUIT


0.01
0.01
L
C1
100
VCC
10 µF
C2
2.2 µF
2
7
9
11
13
TBA120C
8
50
Input
14
1
5
0.01
Output
20 k

COMPONENT VALUES:

	L	C1	Q
5.5 MHz	0.55 µH	1.5 nF	45
6.0 MHz	0.55 µH	1.2 nF	45
10.7 MHz	2.2 µH	100 pF	35

C2 = 0.022 µF, together with the integrated resistor of 2.6 kΩ (Pin 8) gives the deemphasis and can be reduced if required. For stereo 470 pF should be used to provide H.F. decoupling.

FIGURE 2 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz

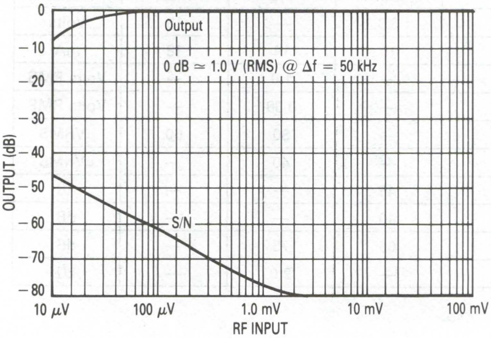


FIGURE 3 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 10.7 MHz

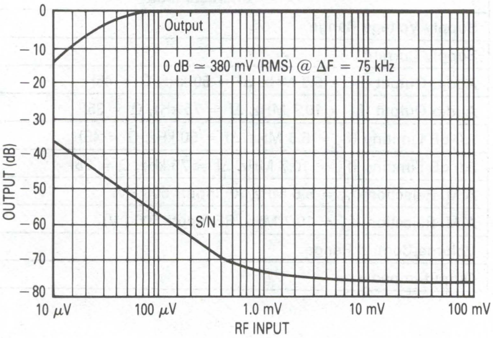


FIGURE 4 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz (30% A.M., 50 kHz F.M.)

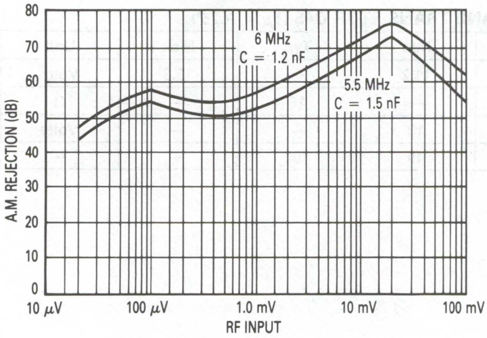


FIGURE 5 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 10.7 MHz (30% A.M., 75 kHz FM)

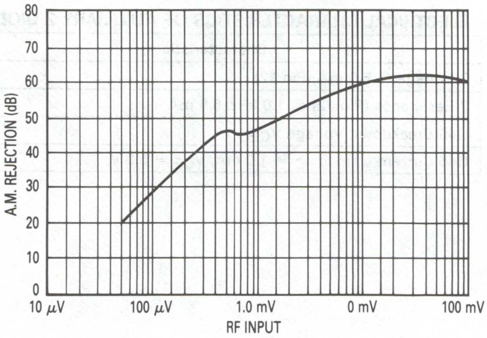


FIGURE 6 — OUTPUT VOLTAGE versus SUPPLY VOLTAGE

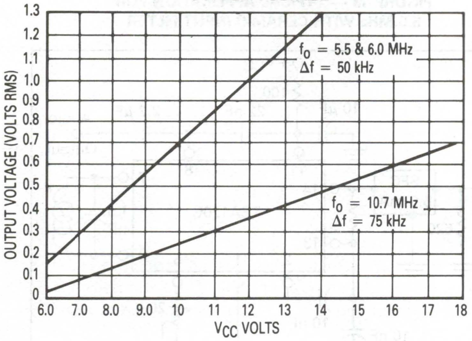


FIGURE 7 — T.H.D. + NOISE versus ATTENUATION (D.C. VOLUME CONTROL)

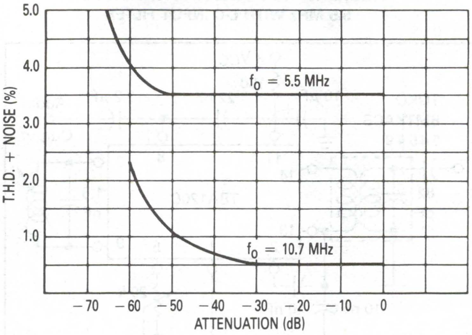


FIGURE 8 — OUTPUT SIGNAL ATTENUATION versus VOLUME CONTROL RESISTANCE

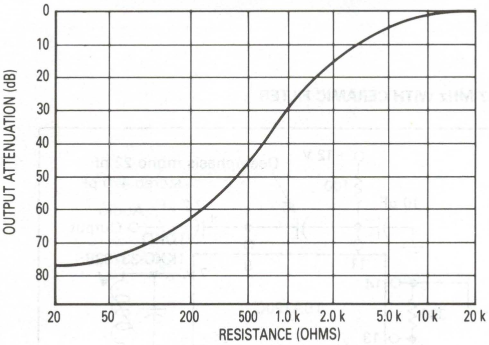


FIGURE 9 — OUTPUT SIGNAL ATTENUATION versus D.C. VOLTAGE AT PIN 5

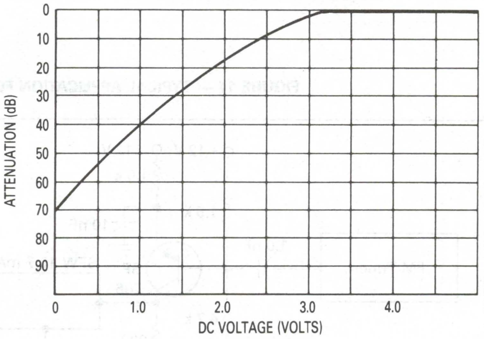


FIGURE 10 — AUDIO PREAMPLIFIER TEST CIRCUIT

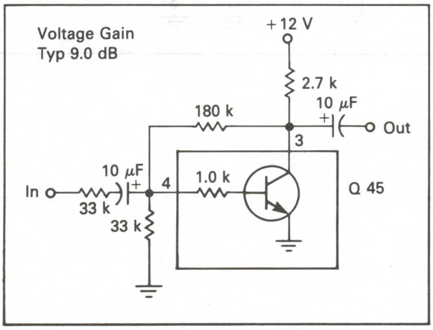

Voltage Gain
Typ 9.0 dB
+12 V
2.7 k
180 k
10 μF
+
Out
3
10 μF
+
4
1.0 k
Q 45
In
33 k
33 k

FIGURE 11 — T.H.D. versus OUTPUT VOLTAGE FOR AUDIO PREAMPLIFIER SHOWN IN FIGURE 10

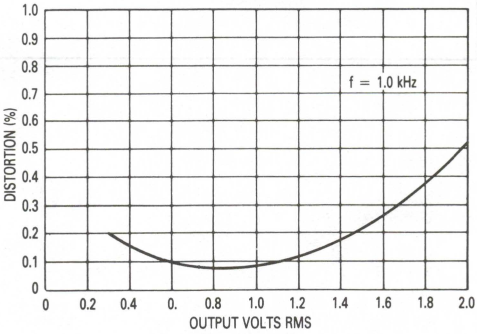


FIGURE 12 — TYPICAL APPLICATION FOR 5.5 MHz WITH L-C INPUT FILTER

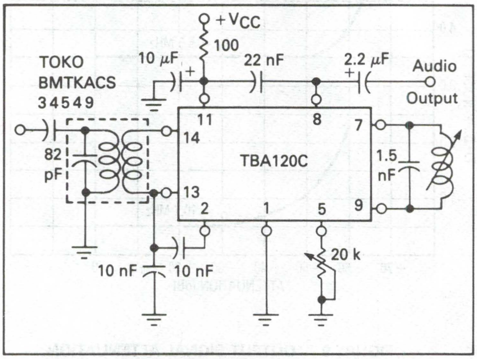

+VCC
100
TOKO
BMTKACS
34549
10 µF
+
22 nF
2.2 µF
+
Audio
Output
11
8
7
14
82
pF
TBA120C
1.5
nF
13
2
1
5
9
20 k
10 nF
10 nF

FIGURE 13 — TYPICAL APPLICATION FOR 5.5 MHz WITH CERAMIC INPUT FILTER

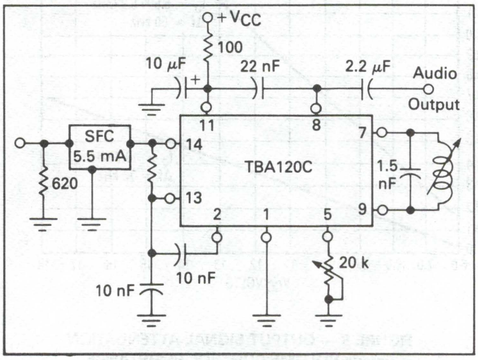
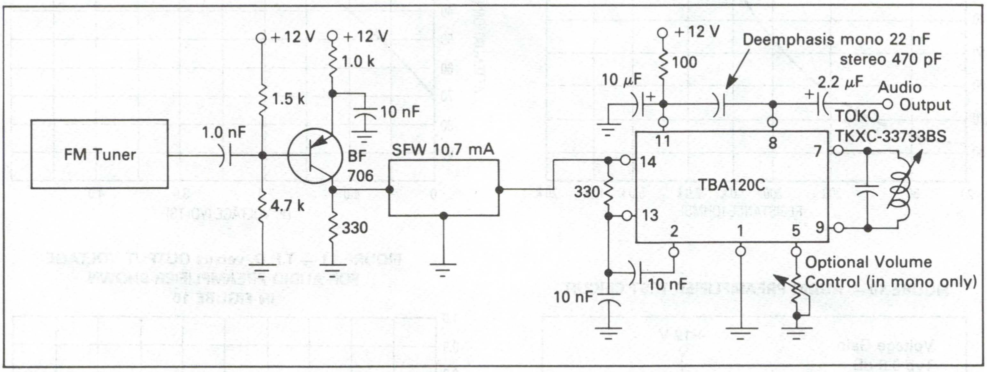

+VCC
100
10 µF
+
22 nF
2.2 µF
Audio
Output
SFC
5.5 mA
620
11
8
7
14
TBA120C
1.5
nF
13
2
1
5
9
20 k
10 nF
10 nF

FIGURE 14 — TYPICAL APPLICATION FOR 10.7 MHz WITH CERAMIC FILTER


+12 V
+12 V
1.0 k
1.5 k
10 nF
FM Tuner
1.0 nF
BF
706
SFW 10.7 mA
4.7 k
330
+12 V
100
Deemphasis mono 22 nF
stereo 470 pF
10 µF
+
2.2 µF
+
Audio
Output
TOKO
TKXC-33733BS
11
8
7
14
330
TBA120C
13
2
1
5
9
10 nF
10 nF
Optional Volume
Control (in mono only)

MOTOROLA

TCA4500A

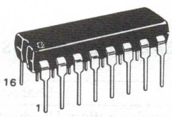
Advance Information

FM STEREO DEMODULATOR DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 kHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 kHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

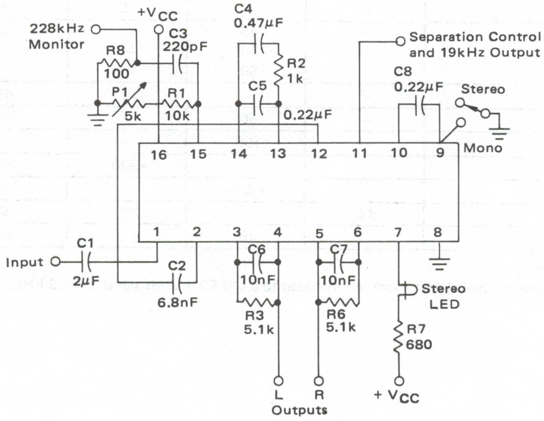
FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648-05

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



228kHz Monitor
+VCC
C3 220pF
R8 100
P1 5k
R1 10k
C4 0.47μF
R2 1k
C5
0.22μF
Separation Control and 19kHz Output
C8 0.22μF
Stereo
Mono
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
Input
C1 2μF
C2 6.8nF
C6 10nF
R3 5.1k
C7 10nF
R6 5.1k
Stereo LED
R7 680
L
R
Outputs
+VCC

PIN FUNCTIONS

1 – Input
2 – Preamplifier output
3 – Left amplifier input
4 – Left channel output
5 – Right channel output
6 – Right amplifier input
7 – Stereo indicator Lamp
8 – Ground
9 – Stereo switch filter
10 – Stereo switch filter
11 – 19 kHz output/blend
12 – Modulator input
13 – Loop filter
14 – Loop filter
15 – Oscillator RC network
16 – V_{CC}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Power Dissipation (Package limitation) Derate above T_A = +25°C	1800 15	mW mW/°C
Operating Temperature Range (Ambient)	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Lamp Drive Voltage (Max. voltage at Pin 7 with lamp "off")	30	Volts
Lamp Current	100	mA
Blend Control Input Voltage (Pin 11)	10	Volts

ELECTRICAL CHARACTERISTICS Unless otherwise noted: V_{CC} = +12 Vdc, T_A = 25°C, 2.5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of Figure 1.

Characteristic	Min.	Typ.	Max.	Unit
Stereo Channel Separation: Unadjusted Optimised on other channel[1]	30 40	– –	– –	dB
Monaural Voltage Gain[1]	0.8	1.0	1.2	
THD at 2.5 Vp-p Composite Input Signal at 1.5 Vp-p Composite Input Signal	– –	– 0.2	0.3 –	%
Signal/Noise Ratio RMS 20 Hz - 15 kHz	–	90	–	dB
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	31 50	– –	dB
Stereo Switch Level (19 kHz input level for lamp "on") Hysteresis	12 –	16 6.0	20 –	mVrms dB
Quiescent Output Voltage Change with Mono/Stereo Switching	–	5.0	20	mVdc
Stereo Blend Control Voltage (Pin 11) 3 dB Separation (see Figure 2) 30 dB Separation	– –	0.7 1.7	– –	V V
Minimum Separation (Pin 11 at 0 V)	–	–	1.0	dB
Monaural Channel Imbalance (pilot tone off)	–	–	0.3	dB
ARI 57 kHz Pilot Tone Influence on THD[2]	–	–	0.5	%
Sub-carrier Harmonic Rejection 76 kHz 114 kHz 152 kHz	– – –	45 50 50	– – –	dB
Supply Ripple Rejection	–	50	–	dB
Input Impedance	–	50	–	KΩ
Output Impedance	–	100	–	Ω
Blend Control Current[1]	–	–	-300	μA
Capture Range	–	±5.0	–	%
Operating Supply Voltage	8.0	–	16	V
Current Drain (lamp off)	–	35	–	mA

Notes: [1] See Applications Information and Circuit Description

[2] ARI Test – Input signal: 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

TYPICAL CHARACTERISTICS

Unless otherwise noted V_{CC} = +12 V, T_A = +25°C, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 16.)

———— : High Loop Gain Circuit

– – – : Normal Circuit

FIGURE 2 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

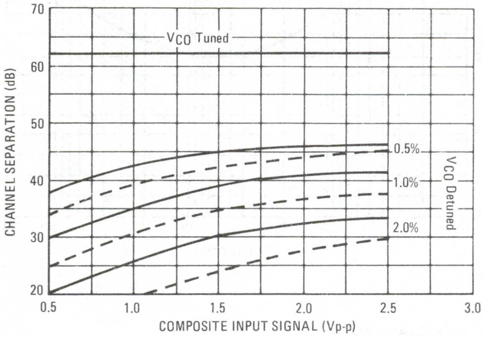


FIGURE 3 – V_{CO} FREE-RUNNING FREQUENCY versus TEMPERATURE

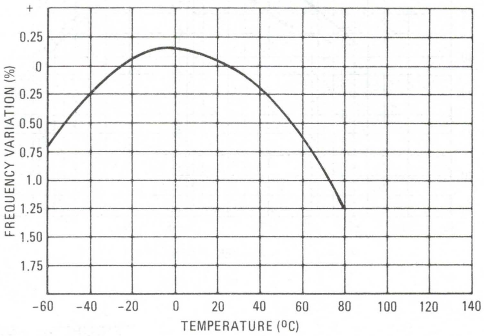


FIGURE 4 – STEREO SWITCH LEVEL versus V_{CO} FREE-RUNNING FREQUENCY

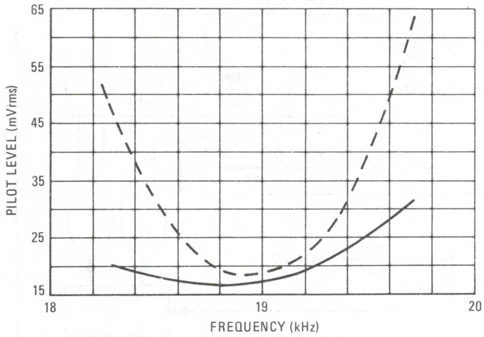


FIGURE 5 – SUPPLY RIPPLE REJECTION versus SUPPLY VOLTAGE

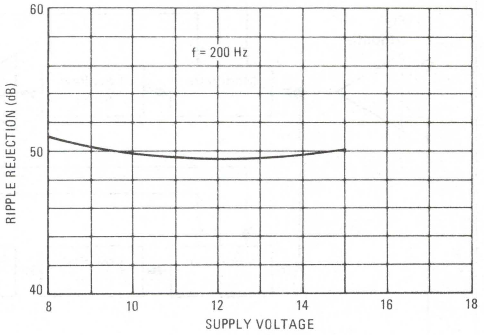


FIGURE 6 – THD versus COMPOSITE INPUT LEVEL

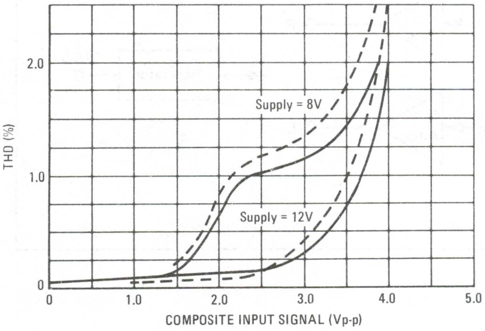


FIGURE 7 – CAPTURE and HOLDING RANGE WITH 20 mV PILOT LEVEL

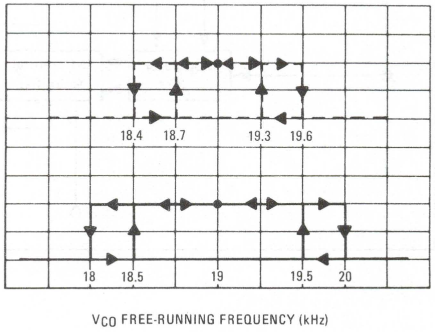


FIGURE 8 – CHANNEL SEPARATION versus FREQUENCY

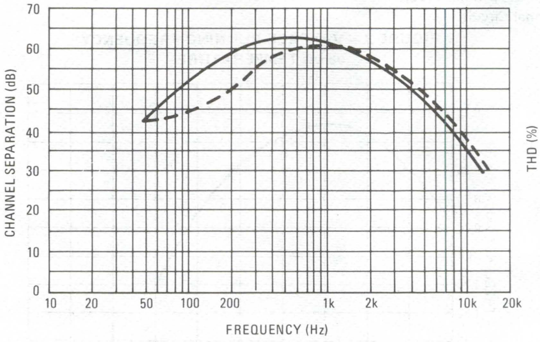


FIGURE 9 – THD versus FREQUENCY

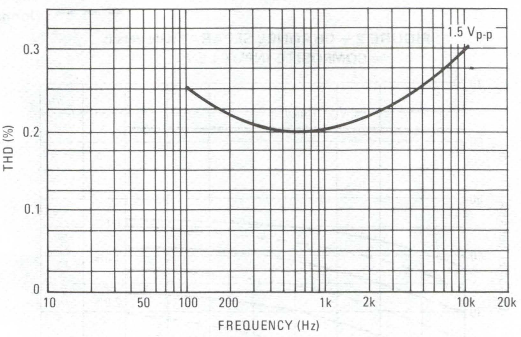
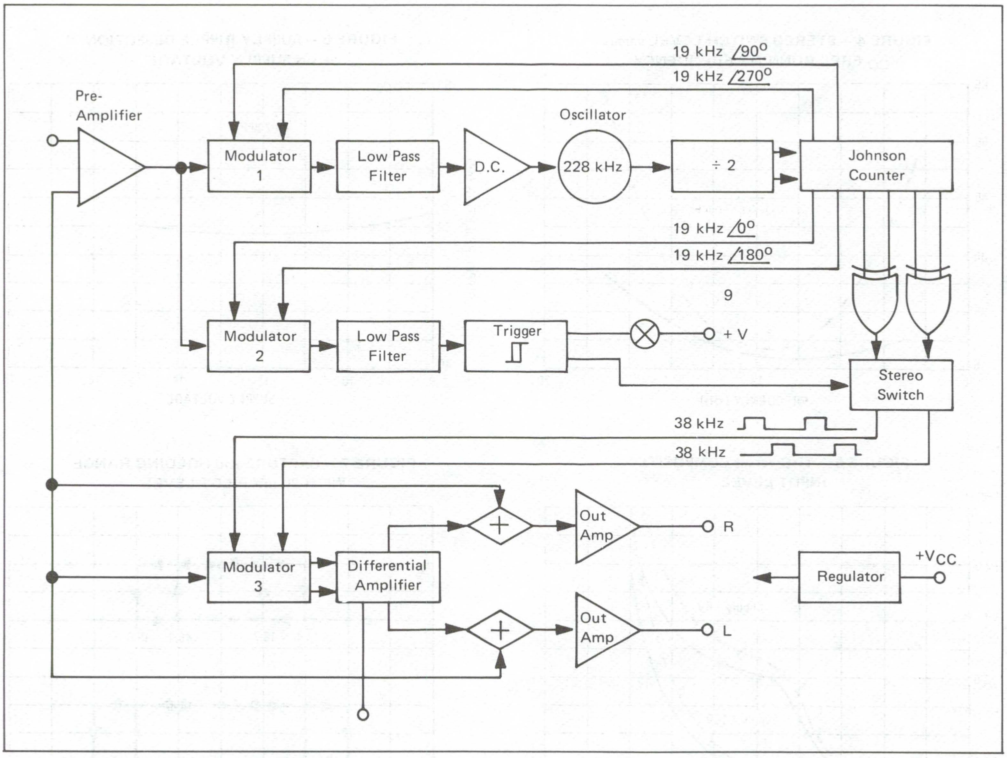


FIGURE 10 – SYSTEM BLOCK DIAGRAM


19 kHz /90°
19 kHz /270°
Pre-Amplifier
Modulator 1
Low Pass Filter
D.C.
Oscillator
228 kHz
÷ 2
Johnson Counter
19 kHz /0°
19 kHz /180°
9
Modulator 2
Low Pass Filter
Trigger
+ V
Stereo Switch
38 kHz
38 kHz
+
Out Amp
R
Modulator 3
Differential Amplifier
Regulator
$+V_{CC}$
+
Out Amp
L

CIRCUIT DESCRIPTION

INTRODUCTION

The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic (114 kHz) of the sub-carrier (38 kHz) excludes interference from the 100 kHz (European Spacing) spaced side bands of adjacent transmitters, while elimination of sensitivity to the third harmonic (57 kHz) of the pilot tone (19 kHz) excludes interference from the ARI* system employed in Europe.

*Auto Radio Information.

CIRCUIT OPERATION

The block diagram of the circuit, shown in Fig. 10, consists of three sections: the phase-lock-loop, including the digital waveform generator: the stereo switch: and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in Fig. 11, which are used to drive the various modulators in the circuit, are developed.

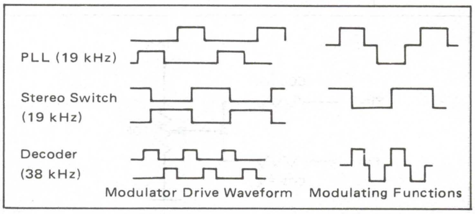
The use of such drive waveforms produces the modulating functions also shown in Fig. 11. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The TCA 4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 11) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is disactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

FIGURE 11 – DIGITAL WAVEFORM



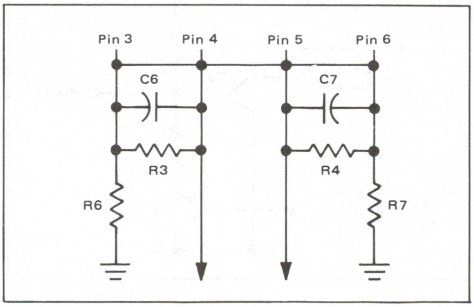
APPLICATION INFORMATION

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 12.

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

FIGURE 12 – OUTPUT AMPLIFIER FEEDBACK NETWORKS



APPLICATION INFORMATION (continued)

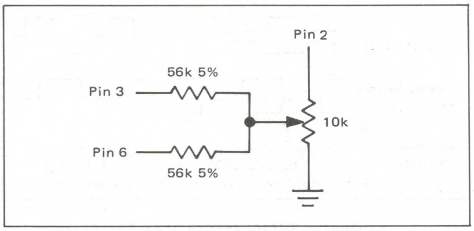
Gain (dB)	R3, R4	C6, C7		R6, R7
		50 μs	75 μs	
0	5.1kΩ	10 nF	15 nF	
3	6.8kΩ	6.8 nF	10 nF	47k ±10%
6	10k	4.7 nF	6.8 nF	27k ±10%

The maximum output level is 1 Vrms; consequently the max. input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

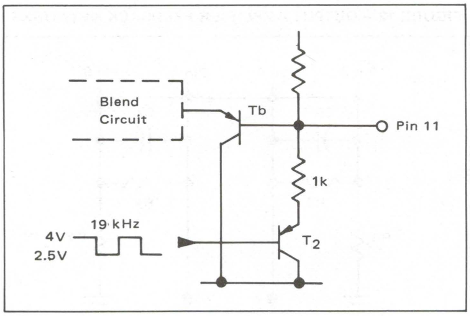
A separation adjustment may be added, as shown below, (Fig. 13), to compensate for the receiver's IF characteristics.

FIGURE 13 – NETWORK PROVIDING ADJUSTABLE SEPARATION



This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

FIGURE 14 – BLEND CONTROL INPUT CIRCUIT



VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-pin package, the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in Fig.14.

If pin 11 is left open-circuit, the 19 kHz signal appears at a mean dc level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation, the voltage on pin 11 is lowered. At 3.2 V, T2 ceases conduction and the 19 kHz signal disappears.

At 2.3 V, the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 15.

FIGURE 15 – SEPARATION CONTROL VOLTAGE

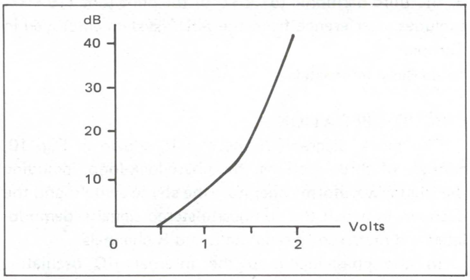
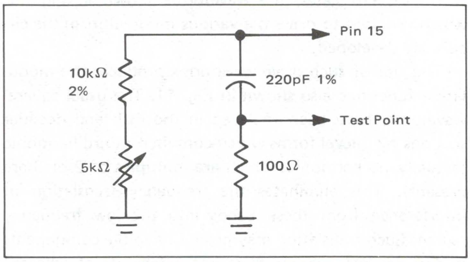


FIGURE 16 – OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT



OSCILLATOR TUNING

If the variable separation facility is not required, pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as shown in Fig. 16.

The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g., car radio) the following component changes to Fig. 1 are recommended.

R1 = 12k
R2 = 1.5k
R8 = 330
P1 = 10k
C3 = 150 pF
C4 = 330 nF
C5 = 150 nF

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required, the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 kHz oscillator will be automatically killed.

The conditions governing Mono/Stereo switching on pin 9 are the following:

- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operaton (with 100 mVrms pilot level): 10 μA (from pin 9 to ground)
  Hysteresis: 0.7μA
- Stereo/mono switching and oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS

P1 — 19 kHz frequency adjustment
P2 — channel separation adjustment and compensation for IF roll-off.
R3, R6— gain fixing resistors. The values shown in the schematic are for unity gain.
C6, C7— de-emphasis capacitors. Value to give: RC = 50 μs.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 Vrms.

TCA5550

MOTOROLA

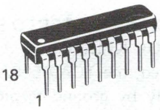
STEREO SOUND CONTROL SYSTEM

The TCA5550 is a single chip stereo balance, volume, bass and treble control circuit designed for use in car radios, TV, and audio systems. Simple dc inputs allow the control to be effected by four inexpensive potentiometers or a remote control system. The bass and treble responses are defined by a single capacitor per control per channel.

- Four High Impedance dc Controls — Vol, Bass, Treble, Balance
- A Single External Capacitor Defines Each Tone Control Characteristic
- Low Distortion, 0.1% at Nominal Input Level, 10 dB Gain with the Tone Controls Flat
- Channel Separation Better Than 45 dB
- Wide Power Supply Tolerance, 8.5 to 18 Vdc
- +14 dB of Tone Control
- More Than 75 dB of Volume Control
- Wide Dynamic Range: 100 mV to 500 mV(RMS) Input Signal
- Low Output Impedance

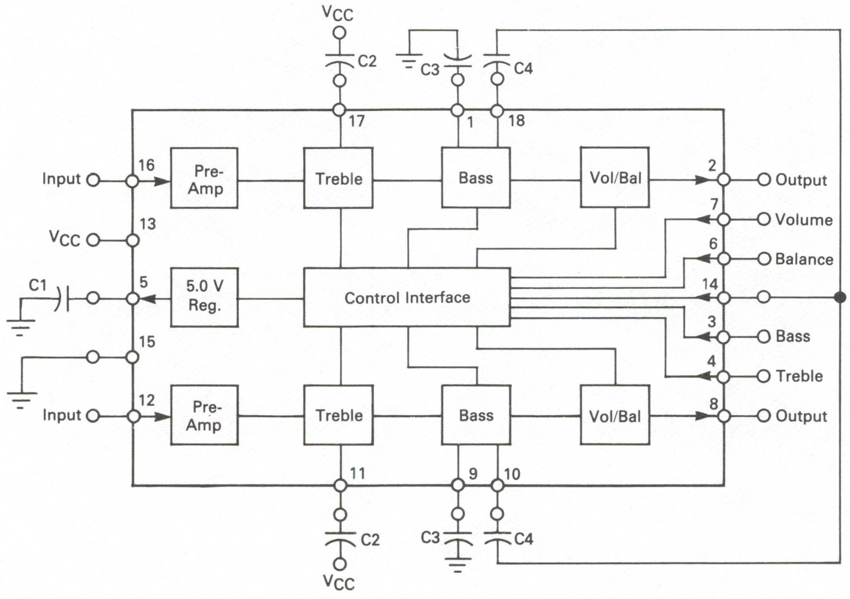
STEREO SOUND CONTROL SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — BLOCK DIAGRAM


VCC
C2
C3
C4
17
1
18
16
Input
Pre-Amp
Treble
Bass
Vol/Bal
2
Output
7
Volume
6
Balance
13
VCC
C1
5
5.0 V Reg.
Control Interface
14
3
Bass
4
Treble
15
12
Input
Pre-Amp
Treble
Bass
Vol/Bal
8
Output
11
9
10
C2
C3
C4
VCC

MAXIMUM RATINGS ($T_A = +25°C$)

Rating	Value	Unit
Power Supply Voltage	18	Volts
Power Dissipation (Package Limitation) Derate above $T_A = +25°C$	1250 10	mW mW/°C
Operating Temperature Range (Ambient)	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Regulator Current, Pin 5	3.0	mAdc

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 12$ Vdc)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	13	8.5	—	18	Vdc
Supply Current (@ Min Gain)		—	30	—	mA
(@ Max Gain)		—	15	—	
Regulated Output Voltage[1]	5	—	5.0	—	V
Input Levels (@ Max Gain)	12, 16	—	100	—	mV (RMS)
(With Reduced Gain)[3]		—	500	—	
Input Impedance	12, 16	—	100	—	kΩ
Output Impedance	2, 8	—	300	—	Ω
Tone Control Range (at 70 Hz & 10 kHz)[2]	3, 4				dB
With Pins 3 & 4 @ 0 V		—	−14	—	
With Pins 3 & 4 @ 2.0 V		—	0	—	
With Pins 3 & 4 @ 4.0 V		—	+14	—	
Balance Control Range Min Gain	6	—	−40	—	dB
(Constant Power Law) Max Gain		—	+3.0	—	dB
Voltage on Pin 6 for Balanced Gain		—	2.5	—	V
Volume Control Range	7	—	80	—	dB
With Pin 7 @ 0 V		—	+10	—	
With Pin 7 @ 2.5 V		—	−20	—	
With Pin 7 @ 5.0 V		—	−70	—	
Control Input Currents	3, 4, 6, 7	—	—	1.0	µA
Channel Separation		45	—	—	dB
Distortion (at 1.0 kHz) at 300 mV (RMS) Output[3]		—	0.1	—	%
Signal : Noise Ratio 50 Hz to 15 kHz, 10 dB Gain, Tone Controls Flat		—	70	—	dB
Noise Level 50 Hz to 15 kHz, Min Gain		—	30	—	µV (RMS)

NOTES:

1. The control potentiometers should be connected to this point, see Figure 5.
2. These figures are functions of the capacitors on Pins 1, 9, 10, 11, 17 & 18. See the application diagram, Figure 5.
3. The input level may be increased to 500 mV (RMS) but the user controls must be adjusted to ensure that the output level does not exceed 300 mV (RMS), to avoid distortion.

FIGURE 2 — TONE CONTROLS
MAX BOOST, CUT/CONTROL VOLTAGE

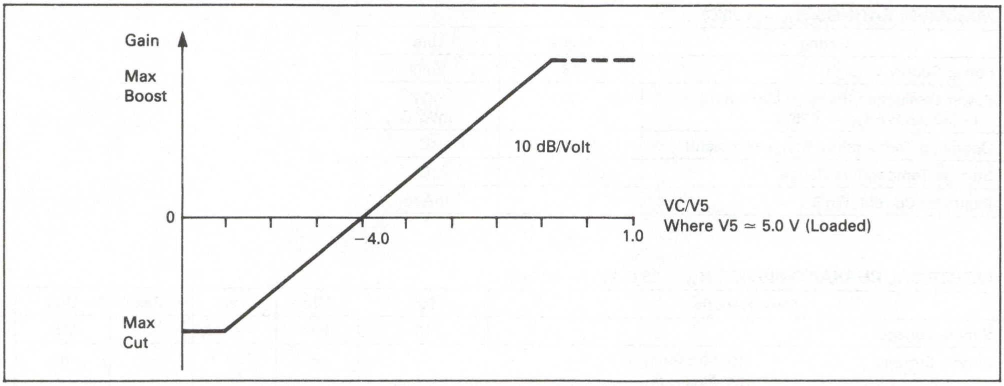


FIGURE 3 — TREBLE CONTROL LAW

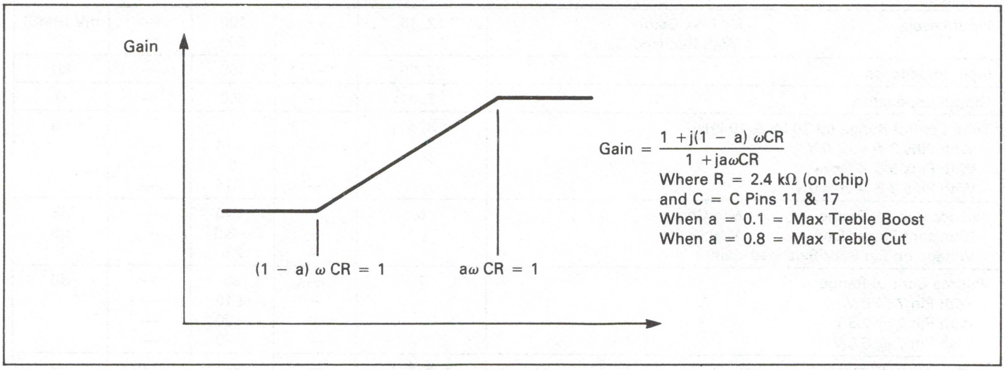


FIGURE 4 — BASS CONTROL LAW

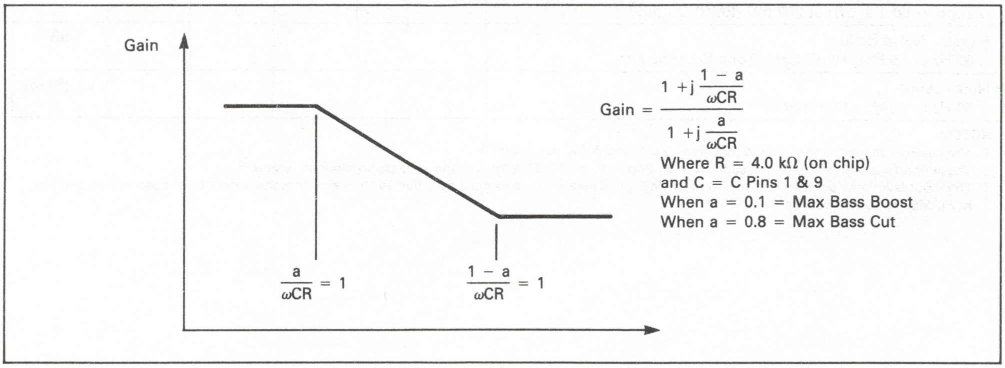
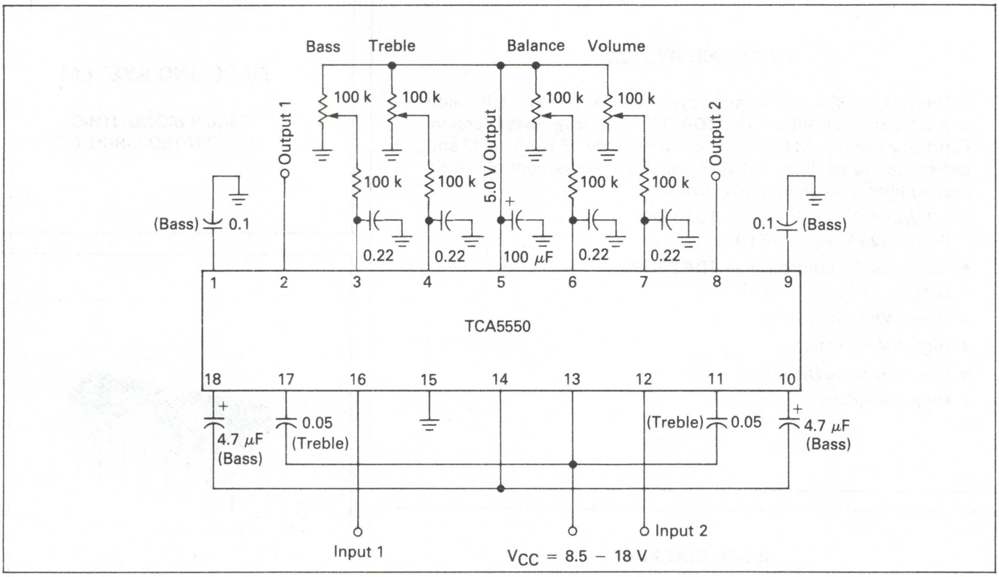


FIGURE 5 — APPLICATION CIRCUIT


Bass
Treble
Balance
Volume
100 k
Output 1
5.0 V Output
Output 2
(Bass)
0.1
0.22
100 μF
+
1
2
3
4
5
6
7
8
9
TCA5550
18
17
16
15
14
13
12
11
10
4.7 μF
(Bass)
0.05
(Treble)
Input 1
Input 2
V_{CC} = 8.5 – 18 V

TDA1190P
TDA3190P

MOTOROLA

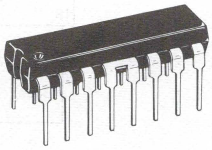
TV SOUND SYSTEM

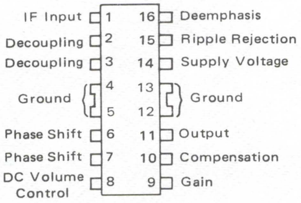
The TDA3190P 4.2-watt sound system is designed for television and related applications. The TDA1190P is a low-power version. Functions performed by these devices include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.2 Watts Output Power — TDA3190P (V_{CC} = 24 V, R_L = 16 Ω)
- 1.3 Watts Output Power — TDA1190P (V_{CC} = 18 V, R_L = 32 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

TV SOUND SYSTEM

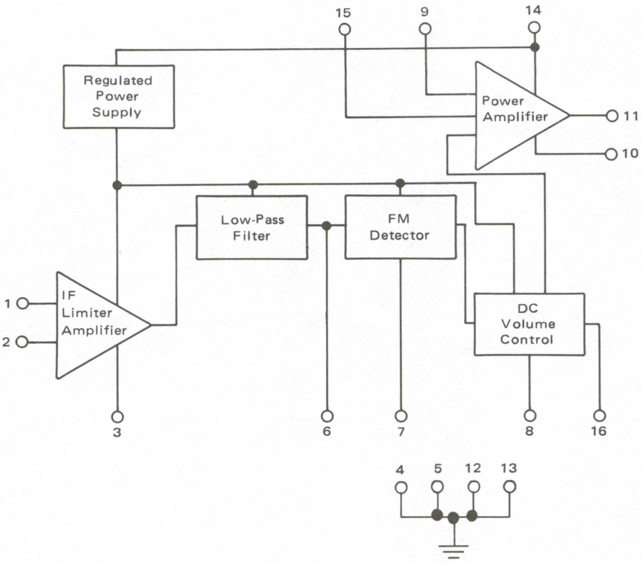
SILICON MONOLITHIC INTEGRATED CIRCUIT




IF Input 1
Decoupling 2
Decoupling 3
Ground 4
5
Phase Shift 6
Phase Shift 7
DC Volume Control 8
16 Deemphasis
15 Ripple Rejection
14 Supply Voltage
13 Ground
12
11 Output
10 Compensation
9 Gain

PLASTIC PACKAGE
CASE 648C-01

BLOCK DIAGRAM


15
9
14
Regulated Power Supply
Power Amplifier
11
10
Low-Pass Filter
FM Detector
1
2
IF Limiter Amplifier
DC Volume Control
3
6
7
8
16
4
5
12
13

ORDERING INFORMATION

Device	Temperature Range	Package
Both Devices	0 to +75°C	Plastic

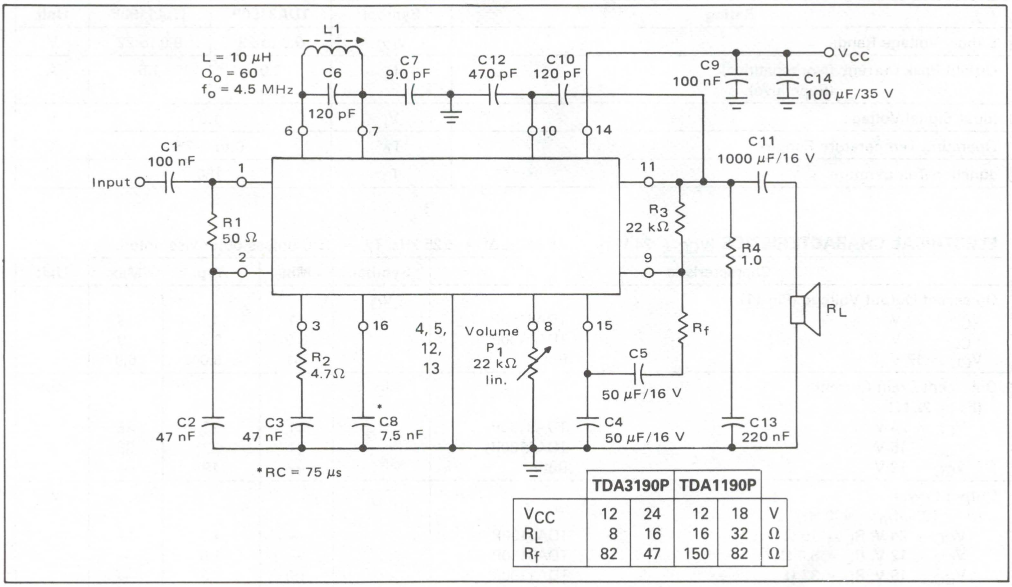
MAXIMUM RATINGS

Rating	Symbol	TDA3190P	TDA1190P	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	9.0 to 22	V
Output Peak Current (Nonrepetitive) (Repetitive)	I_O	2.0 1.5	1.5 1.0	A
Input Signal Voltage	V_I	1.0		V
Operating Temperature Range	T_A	0 to +75		°C
Junction Temperature	T_J	150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C unless otherwise noted.)

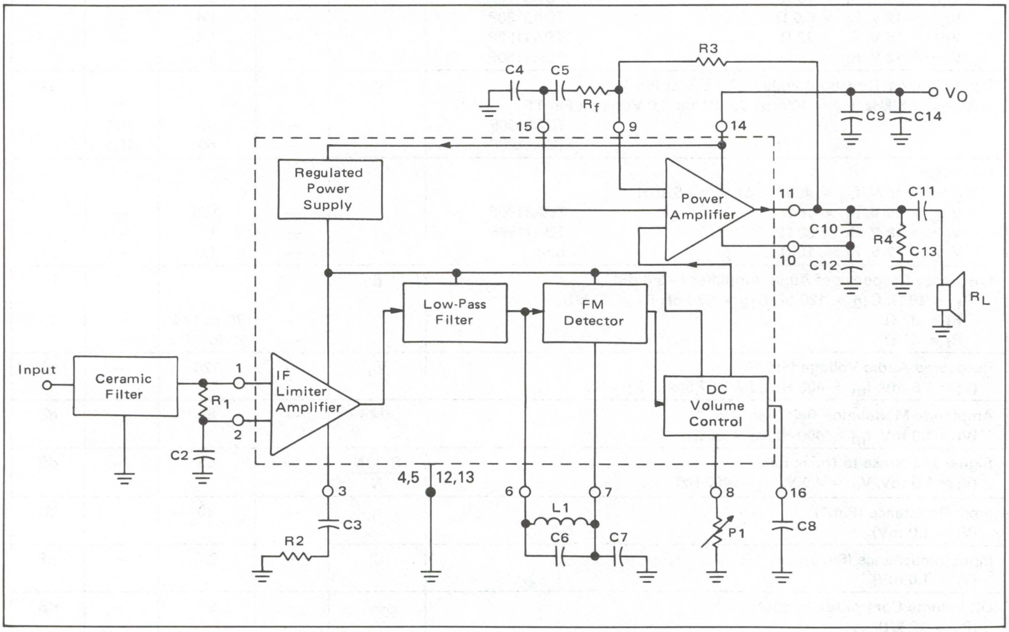
Characteristic		Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage (Pin 11)		V_O				V
V_{CC} = 24 V	TDA3190P		11	12	13	
V_{CC} = 18 V	TDA1190P		8.0	9.0	10	
V_{CC} = 12 V	Both		5.1	6.0	6.9	
Quiescent Drain Current (P1 = 22 kΩ)		I_D				mA
V_{CC} = 24 V	TDA3190P		11	22	35	
V_{CC} = 18 V	TDA1190P		11	22	35	
V_{CC} = 12 V	Both		—	19	—	
Output Power (d = 10%, f_m = 400 Hz)		P_O				W
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	4.2	—	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA3190P		—	1.5	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		1.0	1.3	—	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		0.7	0.9	—	
(d = 2%, f_m = 400 Hz)						
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	3.5	—	
V_{CC} = 12 V, R_L = 8.0 Ω	TDA3190P		—	1.4	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		—	1.0	—	
V_{CC} = 12 V, R_L = 16 Ω	TDA1190P		—	0.7	—	
Input Limiting Threshold Volts (−3.0 dB) at Pin 1 Δf = ±7.5 kHz, f_m = 400 Hz, Set P1 for 2.0 Vrms on Pin 11		V_I				μV
	TDA3190P		—	40	100	
	TDA1190P		—	60	100	
Distortion (P_O = 50 mW, f_m = 400 Hz, Δf = ±7.5 kHz)						%
V_{CC} = 24 V, R_L = 16 Ω	TDA3190P		—	0.75	—	
V_{CC} = 18 V, R_L = 32 Ω	TDA1190P		—	1.0	—	
V_{CC} = 12 V, R_L = 16 Ω	Both		—	1.0	—	
Frequency Response of Audio Amplifier (−3.0 dB) (R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ)		B				Hz
R_f = 82 Ω			—	70 to 12 k	—	
R_f = 47 Ω			—	70 to 7.0 k	—	
Recovered Audio Voltage (Pin 16) (V_I ≥ 1.0 mV, f_m = 400 Hz, Δf = ±7.5 kHz, P_1 = 0)		V_o	—	120	—	mV
Amplitude Modulation Rejection (V_I ≥ 1.0 mV, f_m = 400 Hz, m = 30%)		AMR	—	55	—	dB
Signal and Noise to Noise Ratio (V_I ≥ 1.0 mV, V_o = 4.0 V, f_m = 400 Hz)		$\frac{S+N}{N}$	50	65	—	dB
Input Resistance (Pin 1) (V_I = 1.0 mV)		r_i	—	30	—	kΩ
Input Capacitance (Pin 1) (V_I = 1.0 mV)		C_i	—	5.0	—	pF
DC Volume Control Attenuation (P1 = 12 kΩ)		—	—	90	—	dB

TEST CIRCUIT


L1
L = 10 μH
Q_o = 60
f_o = 4.5 MHz
C6
120 pF
C7
9.0 pF
C12
470 pF
C10
120 pF
C9
100 nF
C14
100 μF/35 V
V_{CC}
6
7
10
14
C1
100 nF
Input
1
11
C11
1000 μF/16 V
R1
50 Ω
2
R_3
22 kΩ
9
R4
1.0
R_L
3
16
4, 5,
12,
13
Volume
P_1
22 kΩ
lin.
8
15
R_f
R_2
4.7Ω
C5
50 μF/16 V
C2
47 nF
C3
47 nF
*
C8
7.5 nF
C4
50 μF/16 V
C13
220 nF
*RC = 75 μs

	TDA3190P		TDA1190P		
V_{CC}	12	24	12	18	V
R_L	8	16	16	32	Ω
R_f	82	47	150	82	Ω

TYPICAL CIRCUIT CONFIGURATION


R3
C4
C5
R_f
V_O
15
9
14
C9
C14
Regulated
Power
Supply
Power
Amplifier
11
C11
C10
R4
C13
10
C12
R_L
Low-Pass
Filter
FM
Detector
Input
Ceramic
Filter
1
R_1
2
IF
Limiter
Amplifier
DC
Volume
Control
C2
4,5
12,13
3
C3
R2
6
7
L1
C6
C7
8
P1
16
C8

MOTOROLA

TDA3301
TDA3303

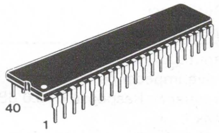
TV COLOR PROCESSOR

These devices will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes them suitable for text display, TV games, cameras, etc. The TDA3301 differs from the TDA3303 in its user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

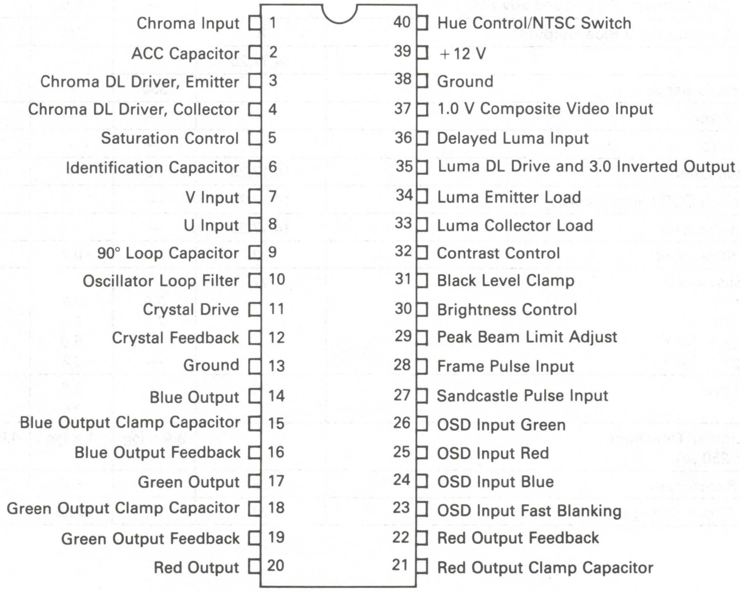
TV COLOR PROCESSOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

FIGURE 1 — PIN ASSIGNMENT


Chroma Input 1
ACC Capacitor 2
Chroma DL Driver, Emitter 3
Chroma DL Driver, Collector 4
Saturation Control 5
Identification Capacitor 6
V Input 7
U Input 8
90° Loop Capacitor 9
Oscillator Loop Filter 10
Crystal Drive 11
Crystal Feedback 12
Ground 13
Blue Output 14
Blue Output Clamp Capacitor 15
Blue Output Feedback 16
Green Output 17
Green Output Clamp Capacitor 18
Green Output Feedback 19
Red Output 20
40 Hue Control/NTSC Switch
39 +12 V
38 Ground
37 1.0 V Composite Video Input
36 Delayed Luma Input
35 Luma DL Drive and 3.0 Inverted Output
34 Luma Emitter Load
33 Luma Collector Load
32 Contrast Control
31 Black Level Clamp
30 Brightness Control
29 Peak Beam Limit Adjust
28 Frame Pulse Input
27 Sandcastle Pulse Input
26 OSD Input Green
25 OSD Input Red
24 OSD Input Blue
23 OSD Input Fast Blanking
22 Red Output Feedback
21 Red Output Clamp Capacitor

MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V
Supply Current			45	60	mA
Composite Video Input	37	—	1.0	—	Vp-p
Video Input Resistance		13	18	23	kΩ
Video Gain to Pin 35		2.7	3.2	3.6	Vp-p
Input Window		0.8–3	0.7–3.2	—	V
Chroma Input (Burst)	1	10	100	200	mVp-p
Input Resistance	1	—	5.0	—	kΩ
ACC Effectiveness	4	—	1.2	3.0	dB
OSD Input	24,25,26	0.5	0.7	1.0	V
OSD Drive Impedance		—	—	180	Ω
OSD Frequency Response (−3.0 dB)		9.0	—	—	MHz
OSD Max Gain		—	7.2	—	MHz
Gain Difference Between Any Two		—	—	15	%
Beam Current Ref. Threshold	16,19,22	1.7	2.0	2.3	V
Differential Voltage		—	—	20	mV
Beam Current Ref. Input Current		—	—	+1.5/−0.5	µA
Differential Current		—	—	1.0	µA
Luminance Gain Between Pin 36 and Outputs (depends on R_{33} and R_{34})		—	4.7	—	
Luminance Bandwidth (−3.0 dB)	14,17,20	9.0	—	—	MHz
Output Resistance		120	170	300	Ω
Residual Carrier (4.43 Mc/s)		—	30	150	mVp-p
PAL Offset (H/2)		—	—	50	mVp-p
Difference in Gain Between Y Input and any RGB o/p		—	5.0	—	%
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mVp-p
Matrix Error	14,17,20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	°
V Ref. Phase Error		—	—	5.0	°
Color Kill Attenuation	14,17,20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14,17,20	—	—	—	dB
OSD Contrast Tracking	14,17,20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level	27				
Burst Gate		6.5	7.2	8.0	V
Line Blanking		2.0	2.6	3.0	V
R Input $V_{27} > 7.0$ V		—	5.0	—	kΩ
$V_{27} < 7.0$ V		—	22	—	kΩ
Frame Slice Level	28	2	2.8	3.6	V
R Input			15	—	kΩ
Peak Beam Limiter Threshold (I_{29} Min = 250 µA)		3.4 x I_{29}	4 x I_{29}	4.6 x I_{29}	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

INPUT/OUTPUT FUNCTIONS

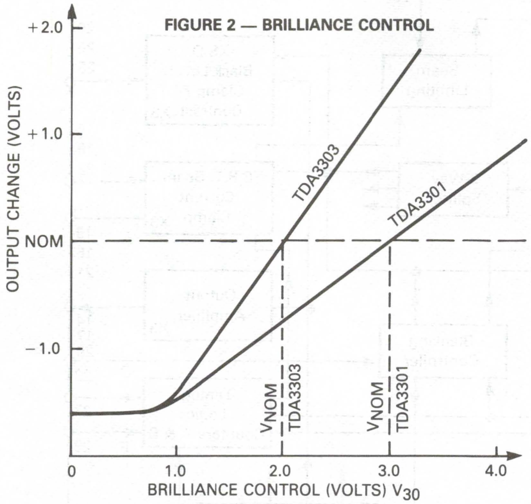


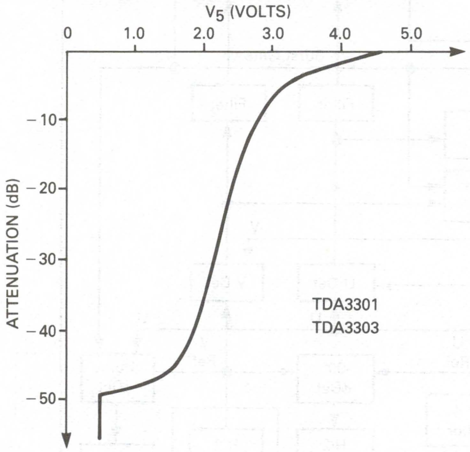
FIGURE 2 — BRILLIANCE CONTROL

The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom. Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. 3 x 20 μA with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

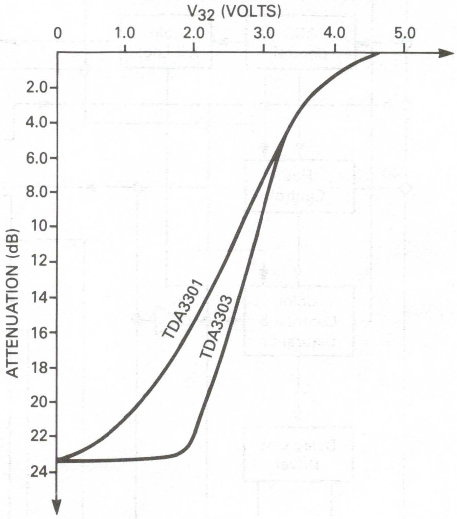
FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

FIGURE 5 — BLOCK DIAGRAM

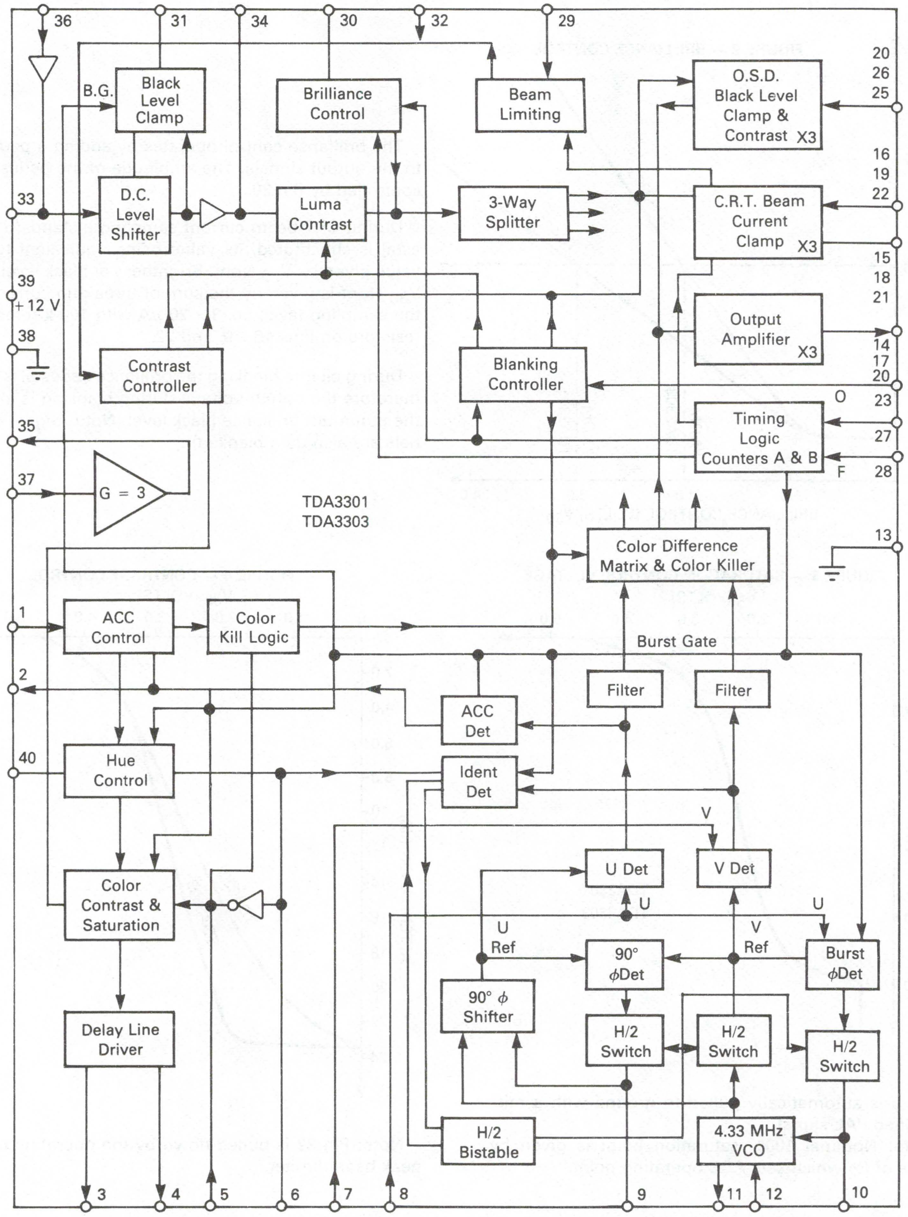
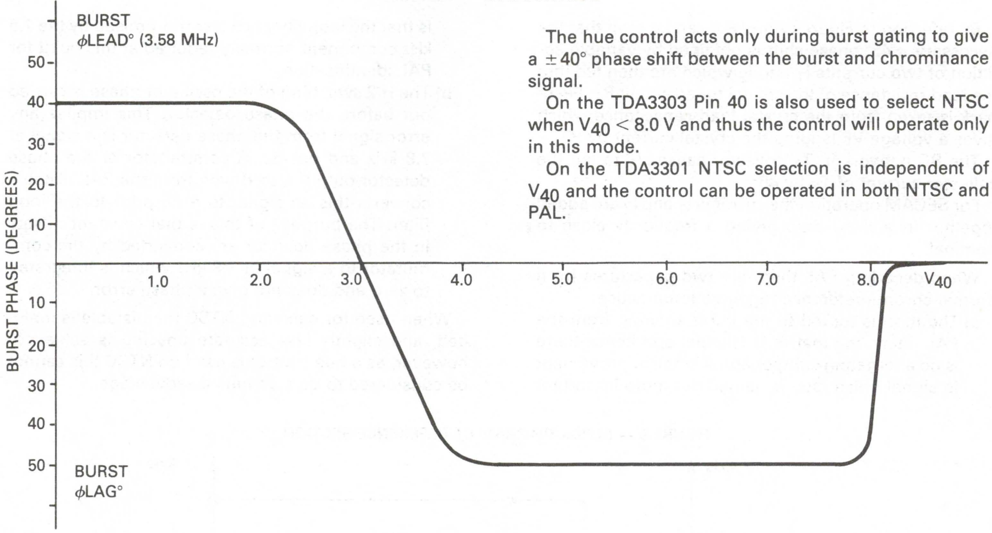

36
31
34
30
32
29
B.G.
Black Level Clamp
Brilliance Control
Beam Limiting
O.S.D. Black Level Clamp & Contrast X3
20
26
25
33
D.C. Level Shifter
Luma Contrast
3-Way Splitter
16
19
22
C.R.T. Beam Current Clamp X3
15
18
21
39
+12 V
38
Output Amplifier X3
14
17
20
Contrast Controller
Blanking Controller
O
23
Timing Logic Counters A & B
27
F
28
35
37
G = 3
TDA3301
TDA3303
13
Color Difference Matrix & Color Killer
1
ACC Control
Color Kill Logic
Burst Gate
2
Filter
Filter
ACC Det
40
Hue Control
Ident Det
V
U Det
V Det
Color Contrast & Saturation
U
U
U Ref
V Ref
90° ϕDet
Burst ϕDet
90° ϕ Shifter
H/2 Switch
H/2 Switch
H/2 Switch
Delay Line Driver
H/2 Bistable
4.33 MHz VCO
3
4
5
6
7
8
9
11
12
10

FIGURE 6 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

On the TDA3303 Pin 40 is also used to select NTSC when $V_{40} < 8.0$ V and thus the control will operate only in this mode.

On the TDA3301 NTSC selection is independent of V_{40} and the control can be operated in both NTSC and PAL.

CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3301 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- — a minimum number of factory adjustments
- — a minimum number of external components
- — compatibility with the SECAM adapter TDA3030B
- — low dissipation
- — use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

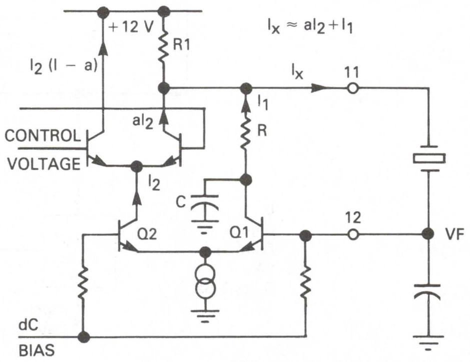
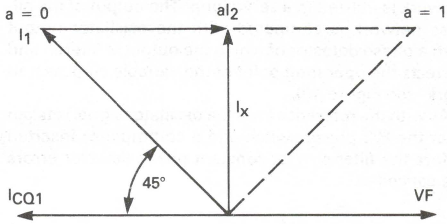


FIGURE 8 — VECTOR DIAGRAM FOR VCO



By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

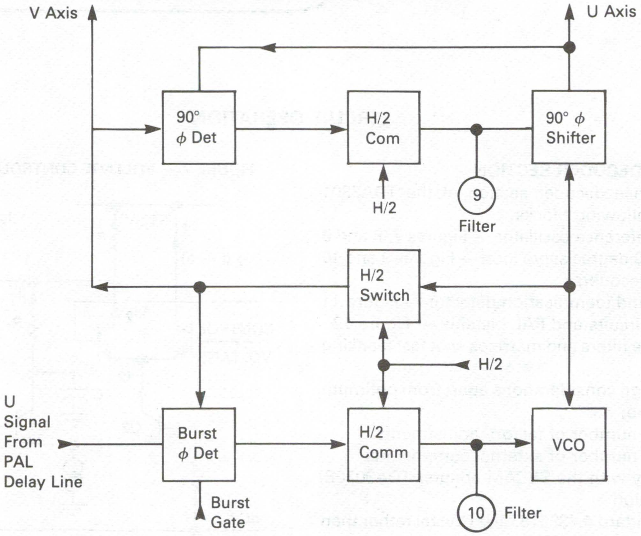
When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 10).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 10 — VARIABLE ALL-PASS NETWORK

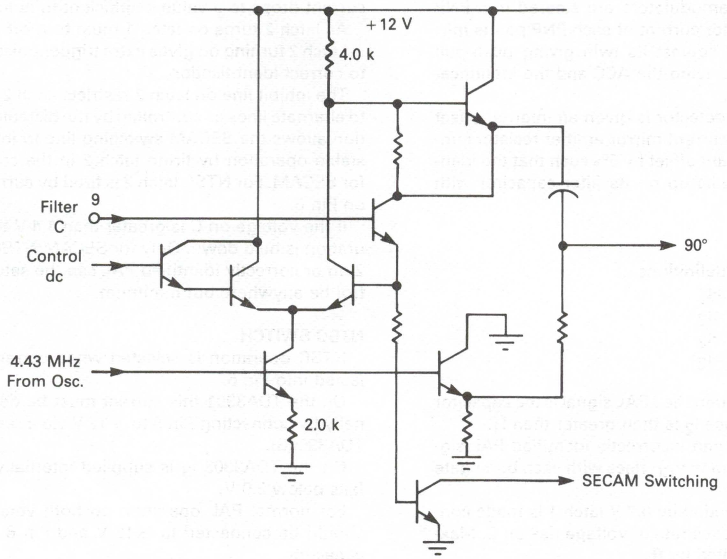
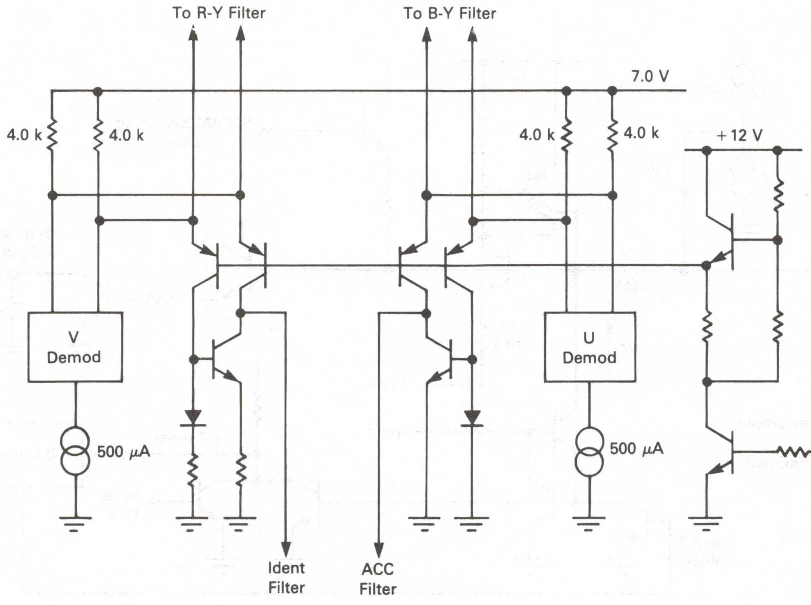

+12 V
4.0 k
Filter
9
C
Control
dc
4.43 MHz
From Osc.
2.0 k
90°
SECAM Switching

FIGURE 11 — ACC AND IDENTIFICATION DETECTORS


To R-Y Filter
To B-Y Filter
7.0 V
4.0 k
4.0 k
4.0 k
4.0 k
+12 V
V
Demod
U
Demod
500 μA
500 μA
+Burst
Gate
Ident
Filter
ACC
Filter

ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1>I_2$
PAL ident. OK	$I_1<I_2$
PAL ident. X	$I_1>I_2$
NTSC	$I_3>I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1>I_2$ hence voltage V_{CC} rises with each burst gate pulse.

When V_{ref} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When V_{ref} 2 is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected on Pin 6.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

NTSC SWITCH

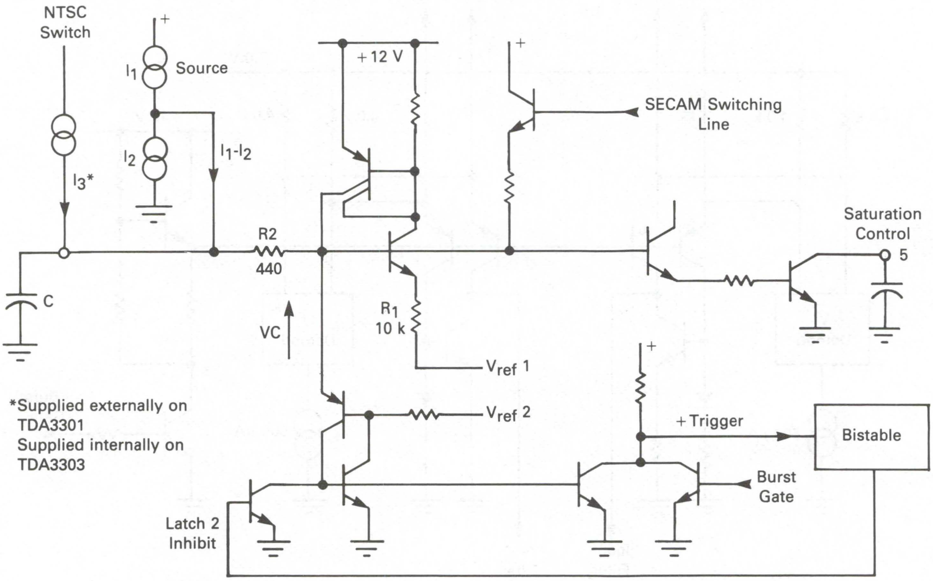
NTSC operation is selected when current (I_3) is injected into Pin 6.

On the TDA3301 this current must be derived externally by connecting Pin 6 to +12 V via a resistor (as on TDA3300B).

On the TDA3303 I_3 is supplied internally when V_{40} falls below 8.0 V;

For normal PAL operation on both versions Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

FIGURE 12 — IDENTIFICATION CIRCUIT



*Supplied externally on TDA3301
Supplied internally on TDA3303

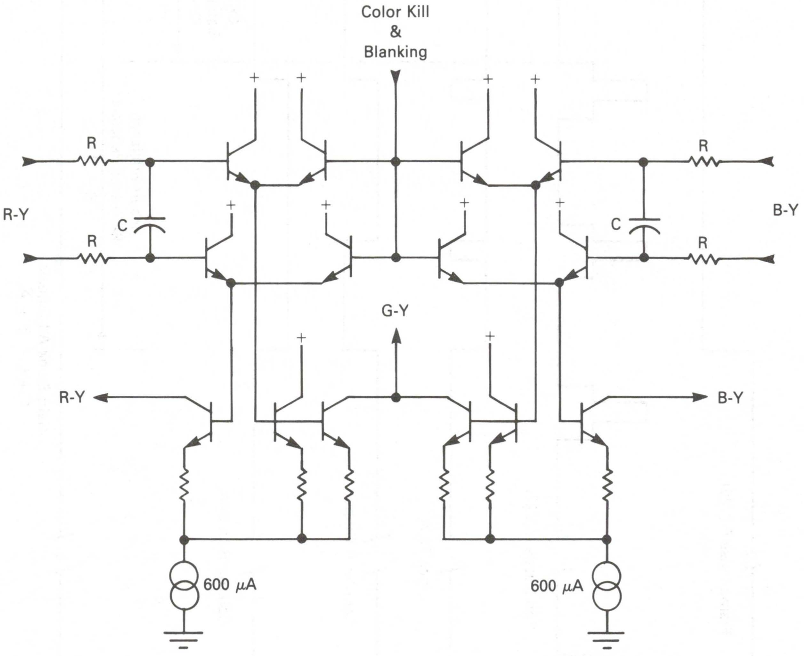
COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

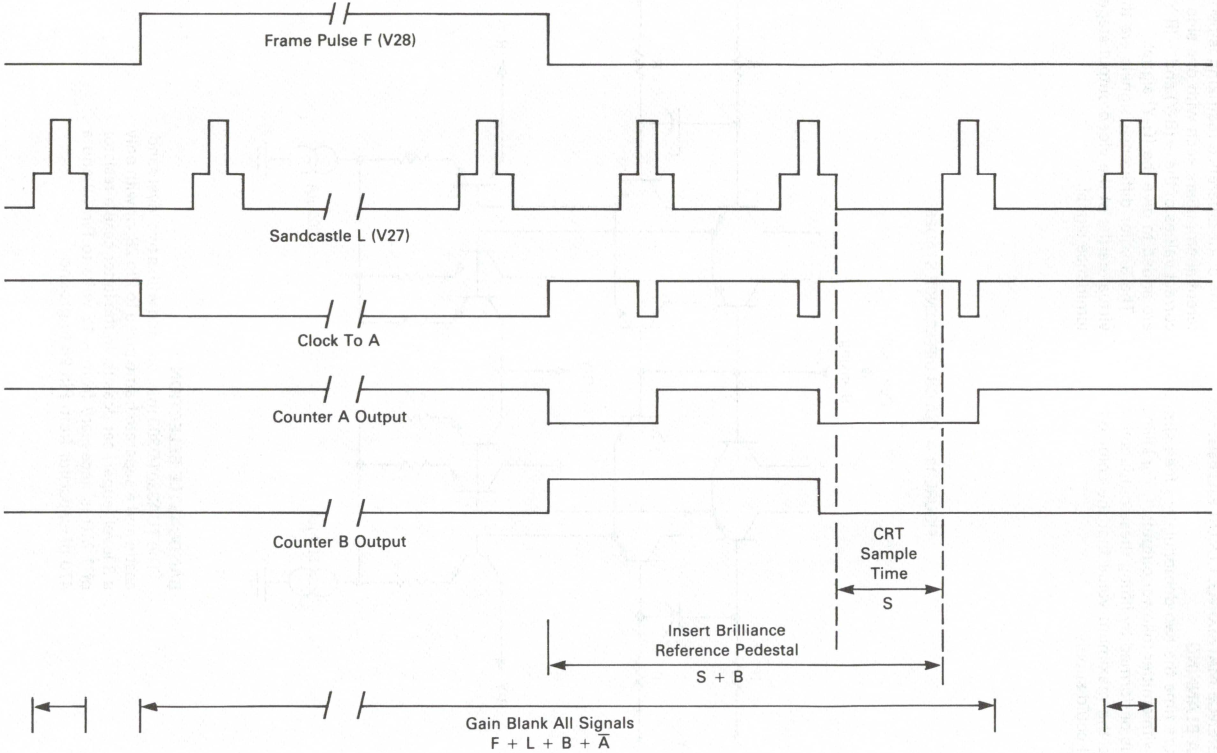
FIGURE 13 — COLOR DIFFERENCE STAGES



SANDCASTLE SELECTION

The TDA3301/3303 may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a 3 level (super) sandcastle. In the latter case a resistor of 1 MΩ is necessary from +12 volts to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

FIGURE 14 — TIMING DIAGRAM


Frame Pulse F (V28)
Sandcastle L (V27)
Clock To A
Counter A Output
Counter B Output
CRT
Sample
Time
S
Insert Brilliance
Reference Pedestal
S + B
Gain Blank All Signals
F + L + B + $\overline{A}$

TIMING COUNTER FOR SAMPLE CONTROL

In order to control the beam current sampling at the beginning of each frame scan two edge triggered flip-flops are used.

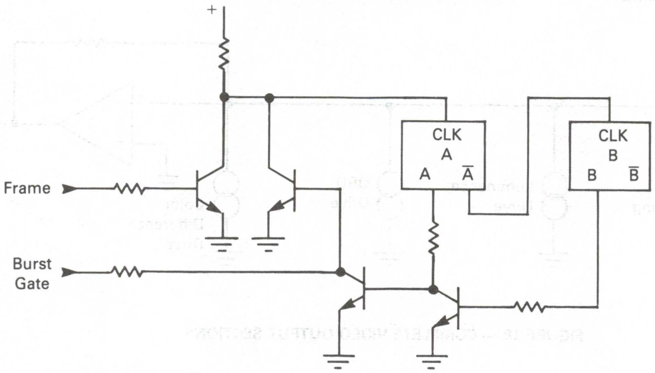
The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only by initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking,
Beam current sampling,
On-screen display blanking,
Brilliance control.

The appropriate flip-flop outputs are matrixed with sandcastle and frame signals by an emitter follower matrix.

FIGURE 15 — TIMING COUNTER



ON-SCREEN DISPLAY INPUTS

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and makes the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

FIGURE 16 — OSD STAGE

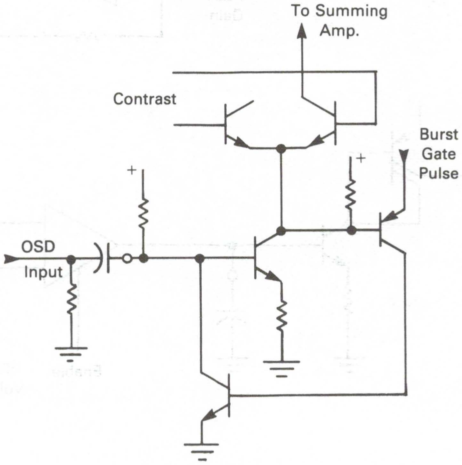


FIGURE 17 — VIDEO OUTPUT SECTION

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the dc operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

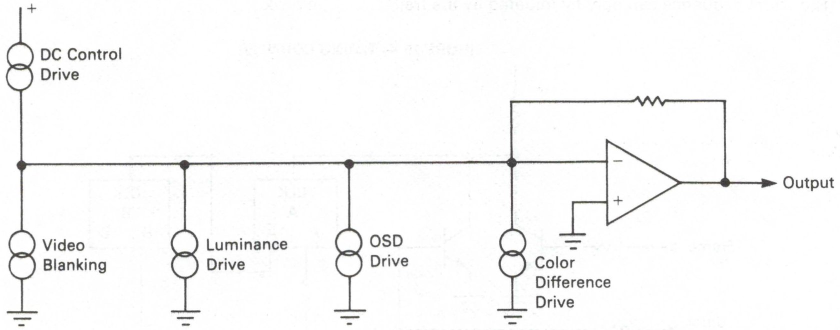

+
DC Control Drive
Output
+
−
Video Blanking
Luminance Drive
OSD Drive
Color Difference Drive

FIGURE 18 — COMPLETE VIDEO OUTPUT SECTIONS

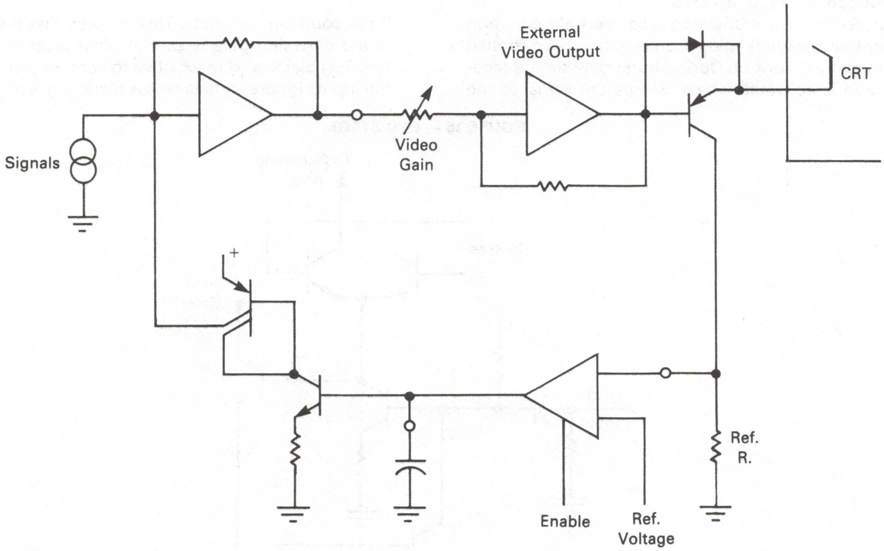
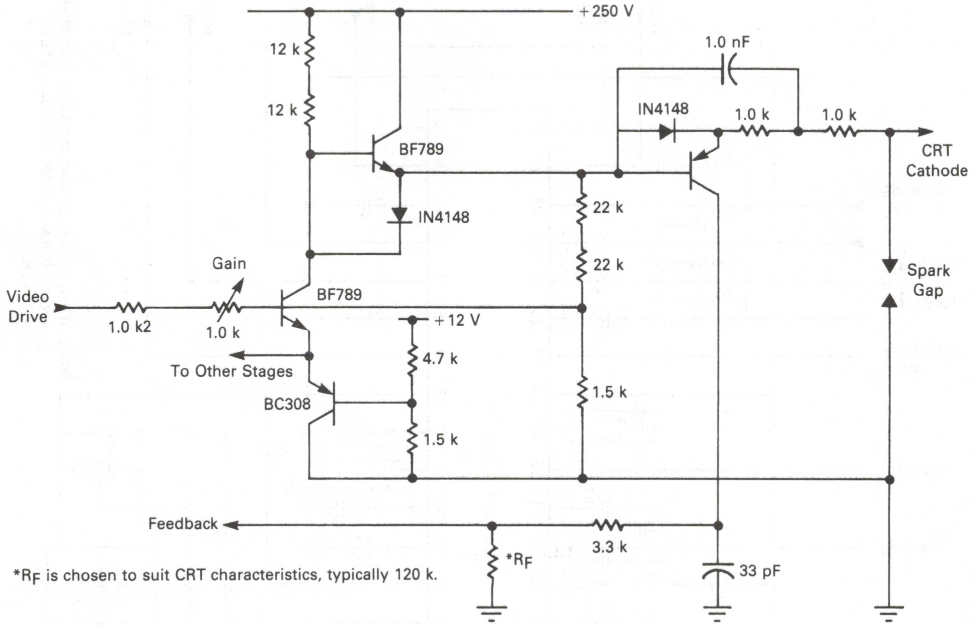

External Video Output
CRT
Signals
Video Gain
+
Ref. R.
Enable
Ref. Voltage

FIGURE 19 — TYPICAL VIDEO OUTPUT STAGE


+250 V
12 k
12 k
BF789
1.0 nF
IN4148
1.0 k
1.0 k
CRT Cathode
IN4148
22 k
22 k
Spark Gap
Gain
Video Drive
1.0 k2
1.0 k
BF789
+12 V
4.7 k
To Other Stages
BC308
1.5 k
1.5 k
Feedback
3.3 k
*RF
33 pF

*R_F is chosen to suit CRT characteristics, typically 120 k.

FIGURE 20 — CLASS A VIDEO OUTPUT STAGE WITH DIRECT FEEDBACK

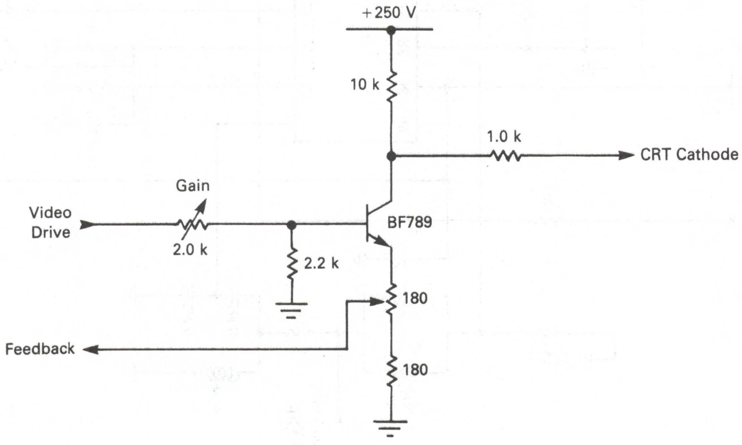
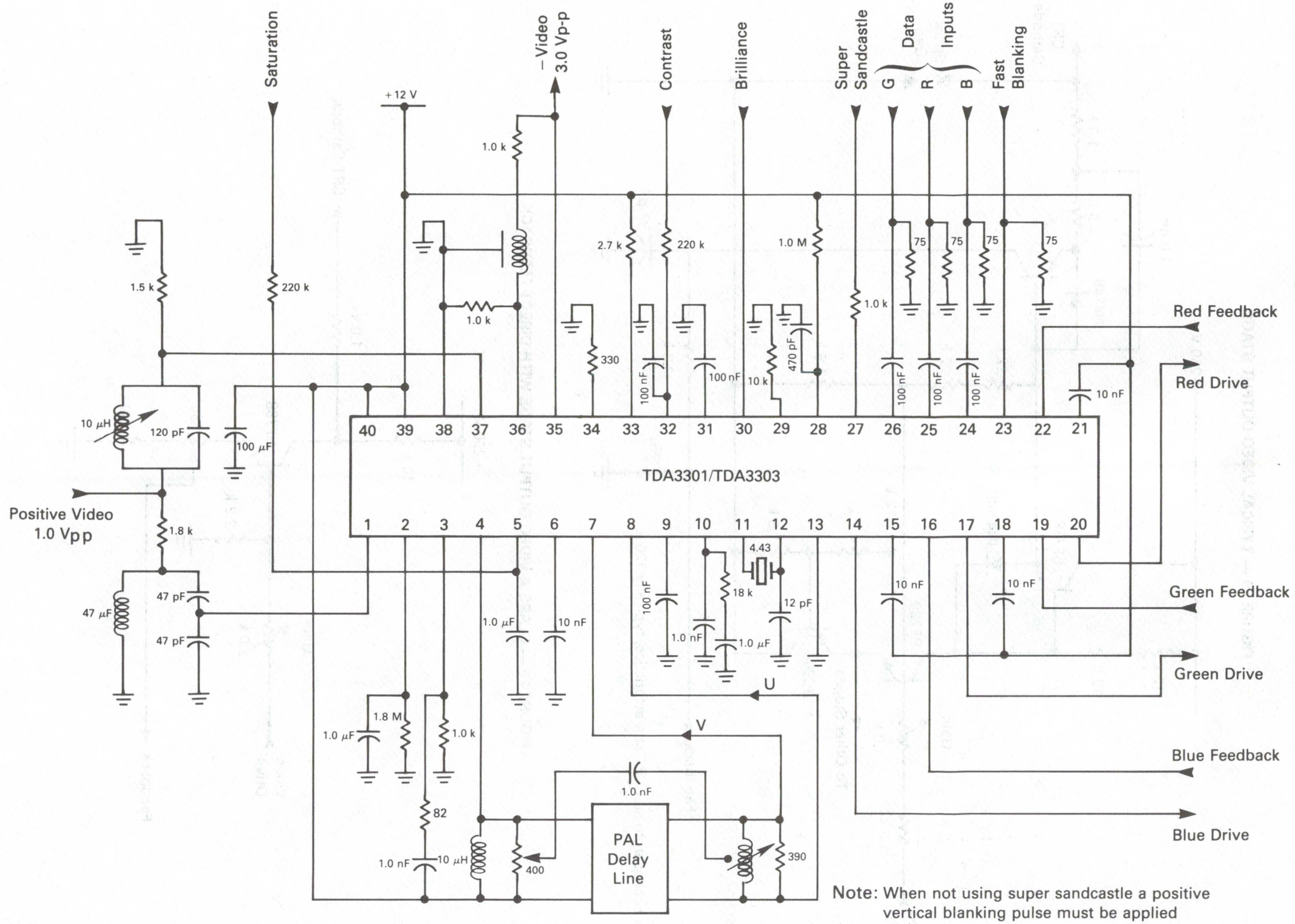

+250 V
10 k
1.0 k
CRT Cathode
Gain
Video Drive
2.0 k
BF789
2.2 k
180
Feedback
180

FIGURE 21 — TYPICAL PAL APPLICATION


Saturation
+12 V
– Video
3.0 Vp-p
Contrast
Brilliance
Super
Sandcastle
G
R
B
Data
Inputs
Fast
Blanking
1.0 k
2.7 k
220 k
1.0 M
75
75
75
75
1.5 k
220 k
1.0 k
330
100 nF
100 nF
10 k
470 pF
1.0 k
100 nF
100 nF
100 nF
Red Feedback
Red Drive
10 nF
10 µH
120 pF
100 µF
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
TDA3301/TDA3303
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Positive Video
1.0 Vpp
1.8 k
47 µF
47 pF
47 pF
1.0 µF
10 nF
100 nF
4.43
18 k
1.0 nF
1.0 µF
12 pF
10 nF
10 nF
Green Feedback
Green Drive
U
V
1.8 M
1.0 µF
1.0 k
82
1.0 nF
10 µH
400
1.0 nF
PAL
Delay
Line
390
Blue Feedback
Blue Drive

Note: When not using super sandcastle a positive vertical blanking pulse must be applied to Pin 28.

MOTOROLA

TDA3330

Advance Information

TV COLOR PROCESSOR

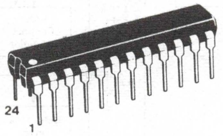
This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube.

Its simplified approach makes it particularly suitable for low cost CTV systems.

- No Oscillator Adjustment Required
- Four dc High Impedance User Controls
- Uses Inexpensive 4.43/3.58 MHz Crystals
- Interfaces With TDA3030B SECAM Adaptor
- Uses Horizontal Flyback or Super Sandcastle Pulse
- Single 12 V Supply
- Low Dissipation

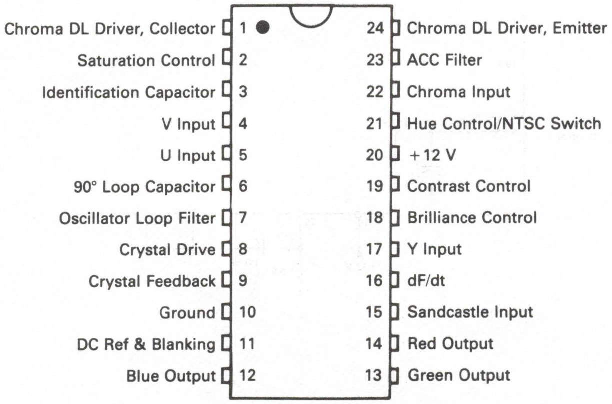
TV COLOR PROCESSOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724-02

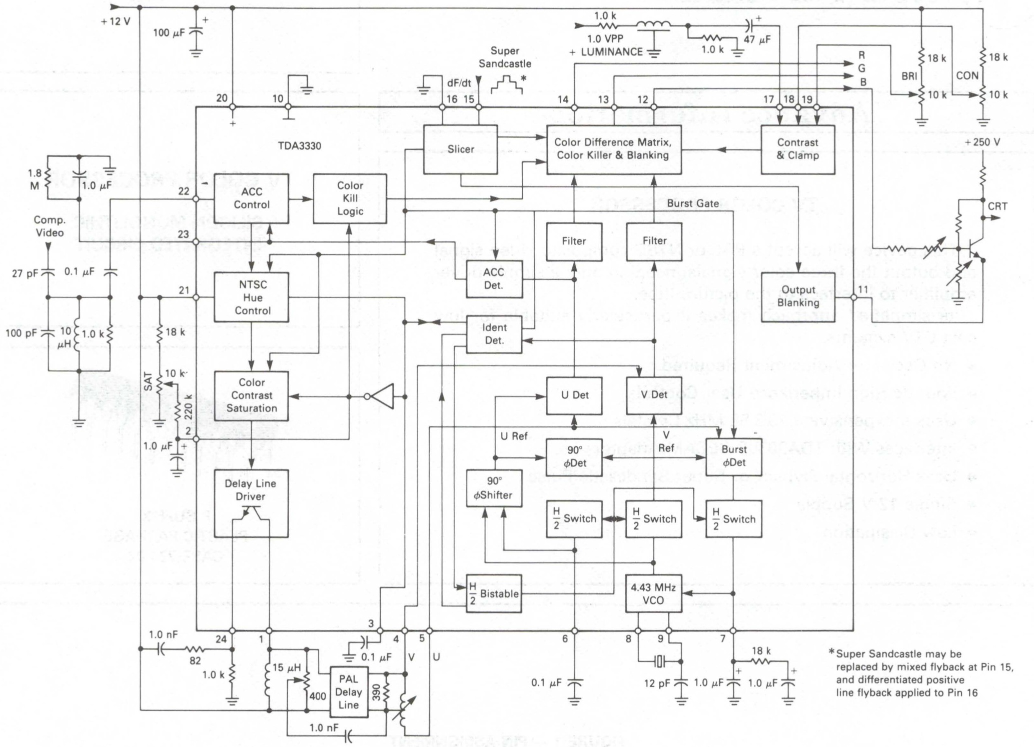
FIGURE 1 — PIN ASSIGNMENT



Chroma DL Driver, Collector 1
Saturation Control 2
Identification Capacitor 3
V Input 4
U Input 5
90° Loop Capacitor 6
Oscillator Loop Filter 7
Crystal Drive 8
Crystal Feedback 9
Ground 10
DC Ref & Blanking 11
Blue Output 12
24 Chroma DL Driver, Emitter
23 ACC Filter
22 Chroma Input
21 Hue Control/NTSC Switch
20 +12 V
19 Contrast Control
18 Brilliance Control
17 Y Input
16 dF/dt
15 Sandcastle Input
14 Red Output
13 Green Output

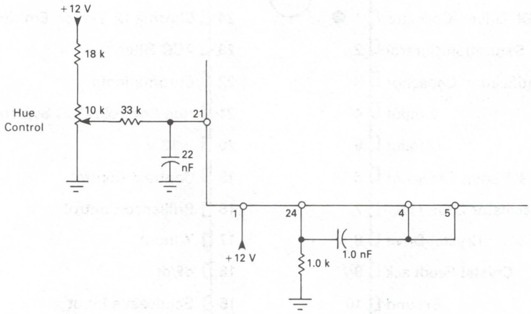
This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 2 — BLOCK DIAGRAM AND PAL APPLICATION


+12 V
100 µF
1.0 k
1.0 VPP
+ LUMINANCE
1.0 k
47 µF
R
G
B
18 k
BRI
10 k
18 k
CON
10 k
+250 V
CRT
Super
Sandcastle
dF/dt
20
10
16
15
14
13
12
17
18
19
TDA3330
Slicer
Color Difference Matrix,
Color Killer & Blanking
Contrast
& Clamp
1.8
M
1.0 µF
22
ACC
Control
Color
Kill
Logic
Burst Gate
Comp.
Video
23
Filter
Filter
27 pF
0.1 µF
ACC
Det.
Output
Blanking
11
21
NTSC
Hue
Control
100 pF
10
µH
1.0 k
18 k
Ident
Det.
SAT
10 k
220 k
Color
Contrast
Saturation
U Det
V Det
1.0 µF
2
U Ref
V
Ref
90°
ϕDet
Burst
ϕDet
Delay Line
Driver
90°
ϕShifter
H/2 Switch
H/2 Switch
H/2 Switch
H/2 Bistable
4.43 MHz
VCO
1.0 nF
24
1
3
4
5
6
8
9
7
82
1.0 k
0.1 µF
V
U
15 µH
400
PAL
Delay
Line
390
0.1 µF
12 pF
1.0 µF
18 k
1.0 µF
1.0 nF

*Super Sandcastle may be replaced by mixed flyback at Pin 15, and differentiated positive line flyback applied to Pin 16

FIGURE 3 — NTSC APPLICATION


+12 V
18 k
Hue
Control
10 k
33 k
21
22
nF
1
24
4
5
+12 V
1.0 k
1.0 nF

MOTOROLA

TDA3333

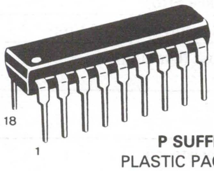
TV COLOR DIFFERENCE DEMODULATOR

This device is designed to demodulate a typical chroma input signal and output the two color difference signals, R – Y and B – Y.

- Decodes PAL or NTSC
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- On-Chip Hue Control for NTSC
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation

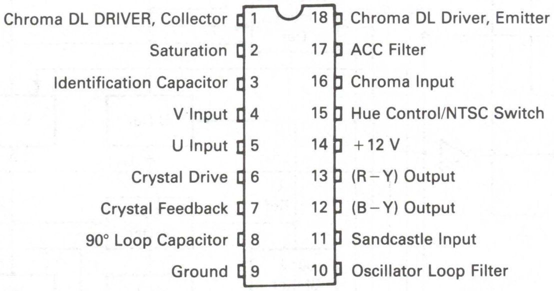
TV COLOR DIFFERENCE DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — PIN ASSIGNMENT


Chroma DL DRIVER, Collector 1
Saturation 2
Identification Capacitor 3
V Input 4
U Input 5
Crystal Drive 6
Crystal Feedback 7
90° Loop Capacitor 8
Ground 9
18 Chroma DL Driver, Emitter
17 ACC Filter
16 Chroma Input
15 Hue Control/NTSC Switch
14 +12 V
13 (R – Y) Output
12 (B – Y) Output
11 Sandcastle Input
10 Oscillator Loop Filter

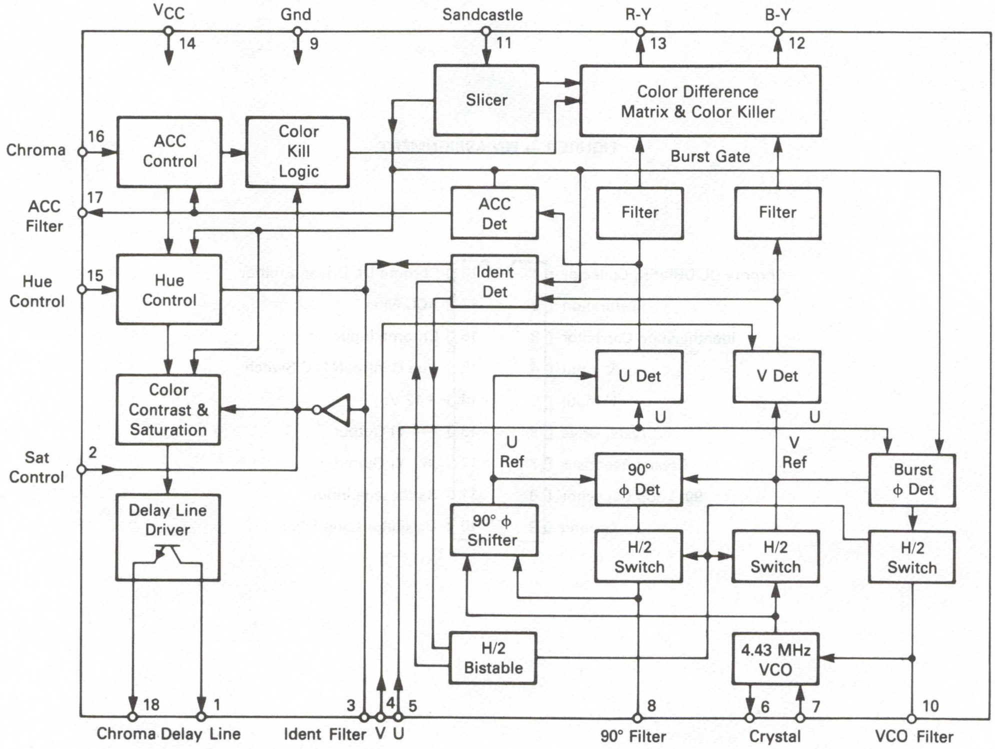
MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

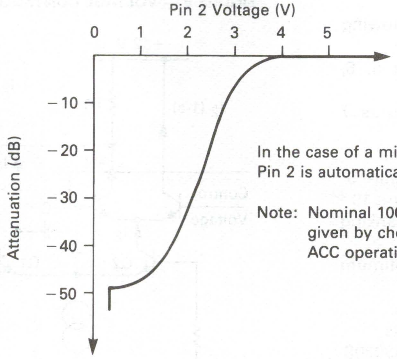
Characteristic		Pin	Min	Typ	Max	Unit
Supply Voltage		14	10.8	12	13.2	V
Chroma Input		16	10	100	200	mVp-p (burst)
ACC Effectiveness		1	—	1.2	3.0	dB
Matrix Error			—	—	10	%
Oscillator Capture Range			350	—	—	Hz
U Ref. Phase Error			—	—	5.0	°
V Ref. Phase Error			—	—	5.0	°
U Input Sensitivity for 1.0 Vp-p	(B-Y) Output	5	—	70	—	mVp-p
Max Output (Limiting)	B-Y R-Y	12 13	— —	4.2 2.4	— —	Vp-p Vp-p
DC Output	B-Y R-Y	12 13	— —	9.2 10.1	— —	V V
Output Resistance	B-Y R-Y	12 13	— —	100 80	— —	Ω Ω

FIGURE 2 — BLOCK DIAGRAM



VCC
14
Gnd
9
Sandcastle
11
R-Y
13
B-Y
12
Slicer
Color Difference Matrix & Color Killer
Chroma
16
ACC Control
Color Kill Logic
Burst Gate
ACC Filter
17
ACC Det
Filter
Filter
Hue Control
15
Hue Control
Ident Det
U Det
V Det
U
U
Color Contrast & Saturation
U Ref
V Ref
Sat Control
2
90° ϕ Det
Burst ϕ Det
Delay Line Driver
90° ϕ Shifter
H/2 Switch
H/2 Switch
H/2 Switch
H/2 Bistable
4.43 MHz VCO
18
1
3
4
5
8
6
7
10
Chroma Delay Line
Ident Filter
V
U
90° Filter
Crystal
VCO Filter

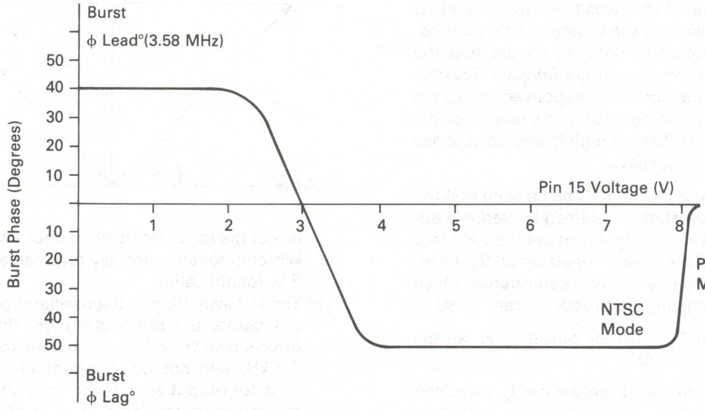
FIGURE 3 — SATURATION CONTROL VOLTAGE



In the case of a misidentified PAL signal Pin 2 is automatically pulled to ground.

Note: Nominal 100% saturation point is given by choice of R_{17} which sets ACC operating point.

FIGURE 4 — HUE CONTROL



Note: Hue control acts only during burst gating with V_{15}<8 Volts.

This condition also selects NTSC mode

CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder consists of the following blocks:

Phase-locked reference oscillator — Figures 5, 6, and 7

Phase-locked 90 degree servo loop — Figures 7 and 8

U and V axis decoders

ACC detector and identification detector — Figure 9

Identification circuits and PAL bistable — Figure 10

Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- — a minimum number of factory adjustments
- — a minimum number of external components
- — compatibility with the SECAM adapter TDA3030B
- — low dissipation
- — use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

FIGURE 5 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

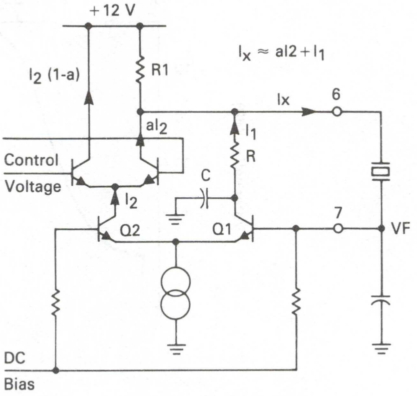
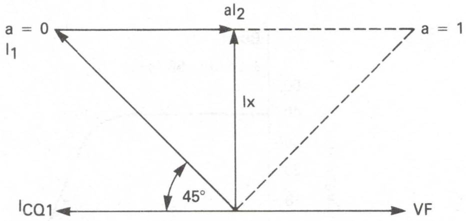


FIGURE 6 — VECTOR DIAGRAM FOR VCO



REFERENCE REGENERATION

The Crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the Crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade Crystals (Crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 5 and 6 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the Crystal tuned circuit R_1. Feedback is taken from the Crystal load capacitance which gives a voltage VF lagging the Crystal current by 90°.

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal/noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC, this cannot be considered to be a serious disadvantage.

90° REFERENCE GENERATION

FIGURE 7 — BLOCK DIAGRAM OF REFERENCE SECTION

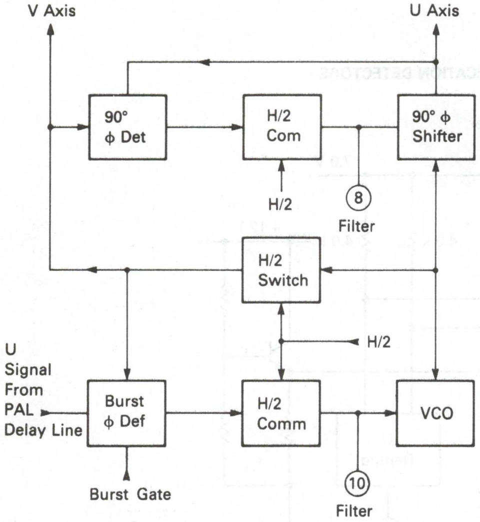
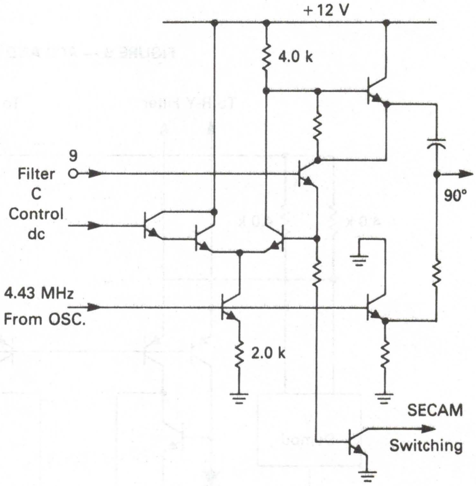


FIGURE 8 — VARIABLE ALL-PASS NETWORK



To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the varible all-pass network (see Figure 8).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B Adapter.

ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

Monochrome	$I_1>I_2$	PAL ident. X	$I_1>I_2$
PAL ident. OK	$I_1<I_2$	NTSC	$I_3>I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1>I_2$ hence voltage V_C rises with each burst gate pulse.

When V_{ref} is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When V_{ref} is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected externally on the filter capacitor.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

FIGURE 9 — ACC AND IDENTIFICATION DETECTORS

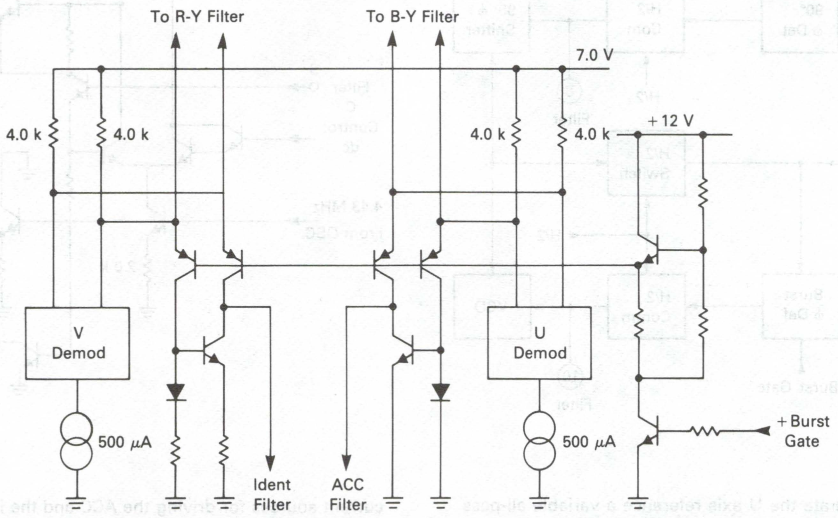
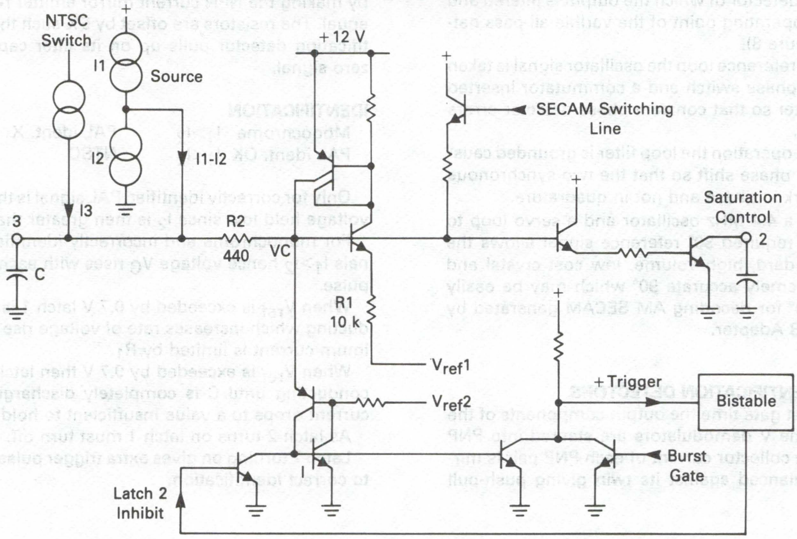

To R-Y Filter
To B-Y Filter
7.0 V
4.0 k
4.0 k
4.0 k
4.0 k
+12 V
V
Demod
U
Demod
500 μA
500 μA
+Burst
Gate
Ident
Filter
ACC
Filter

FIGURE 10 — IDENTIFICATION CIRCUIT


+
NTSC
Switch
I1
Source
+12 V
+
SECAM Switching
Line
I2
I1-I2
I3
3
C
R2
440
VC
R1
10 k
Saturation
Control
2
+
+
Vref1
Vref2
+Trigger
Bistable
Burst
Gate
I
Latch 2
Inhibit

NTSC switch operates when $V_{15}<8.0$ V.

COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The R-Y and B-Y demodulators have equal conversion gains. The demodulated signals are therefore fed through differential amplifiers with a gain ratio G (B-Y)/G (R-Y) = 1.78 in order to give correctly proportioned B-Y and R-Y signals at the output.

FIGURE 11 — COLOR DIFFERENCE STAGES

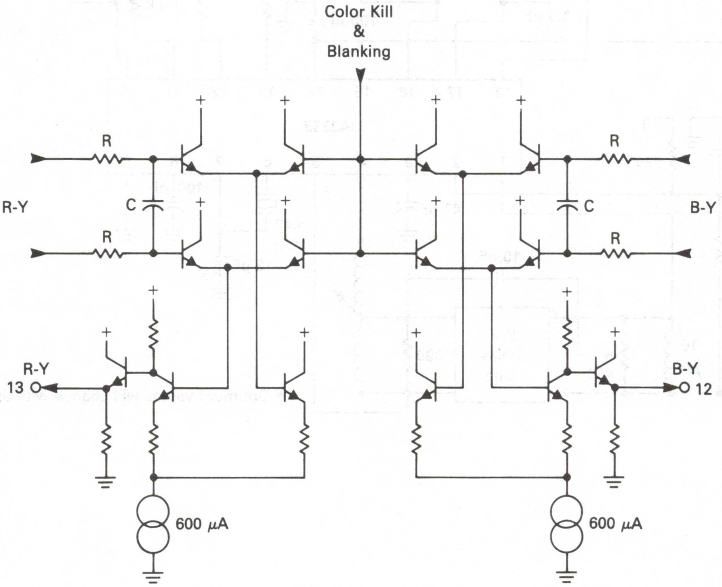
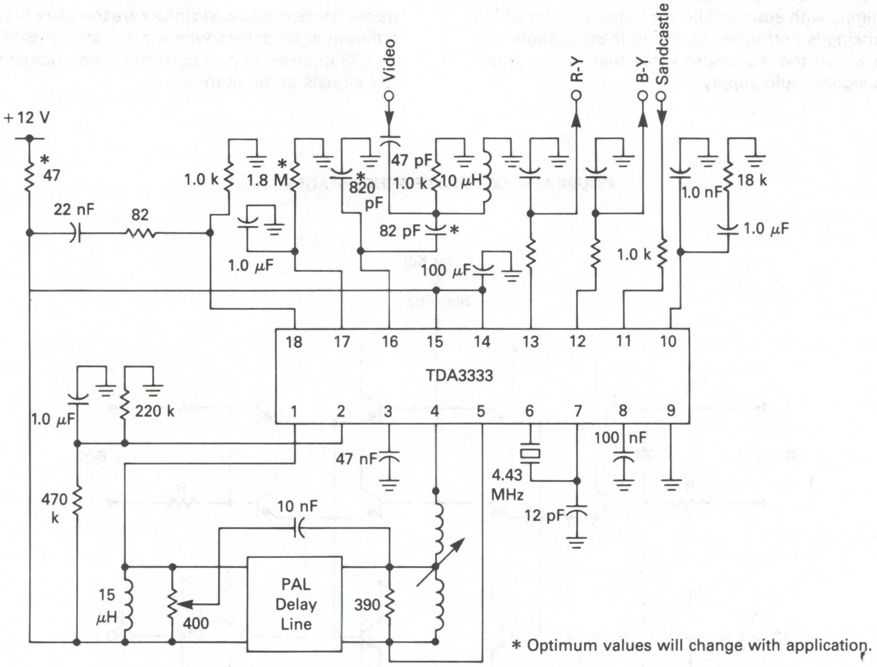


FIGURE 12 — TYPICAL PAL APPLICATION


Video
R-Y
B-Y
Sandcastle
+12 V
* 47
22 nF
82
1.0 k
* 1.8 M
1.0 µF
* 820 pF
47 pF
1.0 k
10 µH
82 pF *
100 µF
1.0 k
1.0 nF
18 k
1.0 µF
18 17 16 15 14 13 12 11 10
TDA3333
1 2 3 4 5 6 7 8 9
1.0 µF
220 k
47 nF
100 nF
4.43 MHz
12 pF
470 k
10 nF
15 µH
400
PAL Delay Line
390

* Optimum values will change with application.

MOTOROLA

µA758A

PHASE LOCK LOOP FM STEREO DEMODULATOR

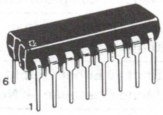
The µA758A is an improved FM stereo multiplex decoder with an extended operating supply voltage range.

It is a direct replacement for the µA758 and LM1800.

- Requires No Inductors
- Low External Part Count
- Excellent Channel Separation Without Adjustment
- Only Single Potentiometer Oscillator Frequency Adjustment Necessary
- 100 mA Lamp or LED Driving Capability With Current Limiting
- Automatic, Transient-Free Stereo/Mono Switching
- Wide Supply Range: 8–16 Vdc
- Excellent SCA Rejection
- 50 dB Power Supply Rejection
- Low Impedance, Buffered Output

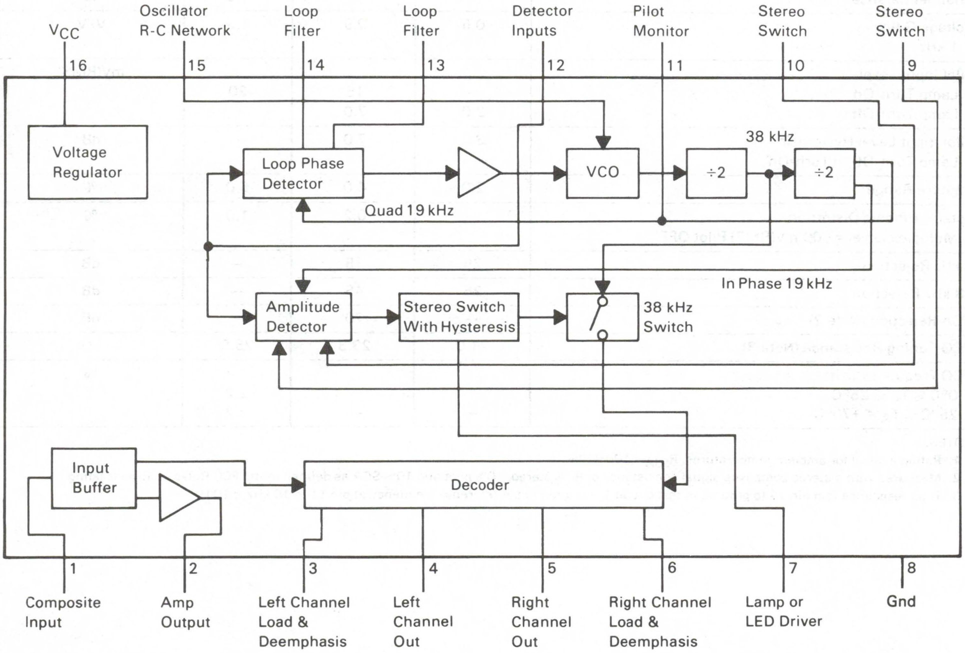
PHASE LOCK LOOP FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648-05

BLOCK DIAGRAM


VCC
Oscillator R-C Network
Loop Filter
Loop Filter
Detector Inputs
Pilot Monitor
Stereo Switch
Stereo Switch
16
15
14
13
12
11
10
9
Voltage Regulator
Loop Phase Detector
VCO
÷2
38 kHz
÷2
Quad 19 kHz
In Phase 19 kHz
Amplitude Detector
Stereo Switch With Hysteresis
38 kHz Switch
Input Buffer
Decoder
1
2
3
4
5
6
7
8
Composite Input
Amp Output
Left Channel Load & Deemphasis
Left Channel Out
Right Channel Out
Right Channel Load & Deemphasis
Lamp or LED Driver
Gnd

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	18	Vdc
Supply Voltage (⩽ 15 Seconds)	22	Vdc
Voltage at Lamp Driver Terminal (Lamp OFF)	22	Vdc
Junction Temperature	150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Operating Voltage Range	8-16	Vdc

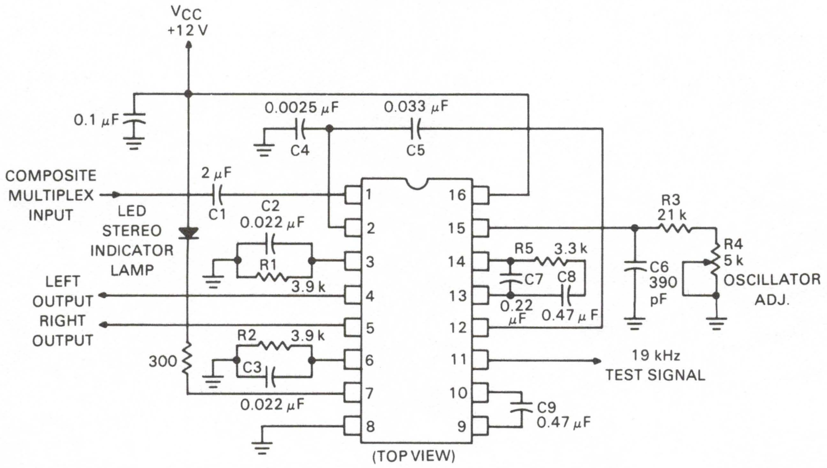
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +12 Vdc, 19 kHz pilot level = 30 mV(RMS), Multiplex Signal (L = R, pilot OFF) = 300 mV(RMS), Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified)

Characteristic	Min	Typ	Max	Unit
Current Drain Lamp OFF	—	21	35	mAdc
Maximum Available Lamp Current	100	150	—	mAdc
Voltage @ Lamp Driver Terminal I_{Lamp} = 50 mA	—	1.0	1.8	Vdc
DC Voltage Shift @ Either Output Terminal Stereo to Mono Operation — No Lamp	—	2.0	100	mVdc
Power Supply Ripple Rejection 200 Hz, 200 mV(RMS)	35	50	—	dB
Input Resistance	20	35	—	kΩ
Output Resistance	0.9	1.3	1.7	kΩ
Channel Separation				dB
100 Hz	—	40	—	
400 Hz	30	45	—	
10 kHz	—	45	—	
Channel Balance	—	0	1.0	dB
Voltage Gain 1 kHz	0.6	0.9	1.3	V/V
Pilot Input Level				mV(RMS)
Lamp Turn-On	—	15	20	
Lamp Turn-Off	2.0	7.0	—	
Pilot Input Level Hysteresis Lamp Turn-Off to Turn-On	3.0	7.0	—	dB
Capture Range	2.0	4.0	6.0	%
Total Harmonic Distortion Multiplex Level = 600 mV(RMS) Pilot OFF	—	0.2	1.0	%
9 kHz Rejection	25	35	—	dB
38 kHz Rejection	25	45	—	dB
SCA Rejection (Note 2)	—	70	—	dB
VCO Tuning Resistance (Note 3)	21.0	23.3	25.5	kΩ
VCO Frequency Drift				%
0°C ⩽ T_A ⩽ 25°C	—	—	± 2	
25°C ⩽ T_A ⩽ +70°C	—	—	± 2	

NOTES:

1. Rating applied for ambient temperatures. $R_{\theta JA}$ = 100°C/W
2. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting
3. Total resistance fom pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz ± 10 Hz

TYPICAL APPLICATION AND TEST CIRCUIT


VCC
+12 V
0.1 µF
0.0025 µF
C4
0.033 µF
C5
COMPOSITE
MULTIPLEX
INPUT
2 µF
C1
LED
STEREO
INDICATOR
LAMP
C2
0.022 µF
R1
3.9 k
LEFT
OUTPUT
RIGHT
OUTPUT
R2
3.9 k
C3
0.022 µF
300
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
R5
3.3 k
C7
C8
0.22 µF
0.47 µF
R3
21 k
R4
5 k
C6
390
pF
OSCILLATOR
ADJ.
19 kHz
TEST SIGNAL
C9
0.47 µF
(TOP VIEW)

NOTES:

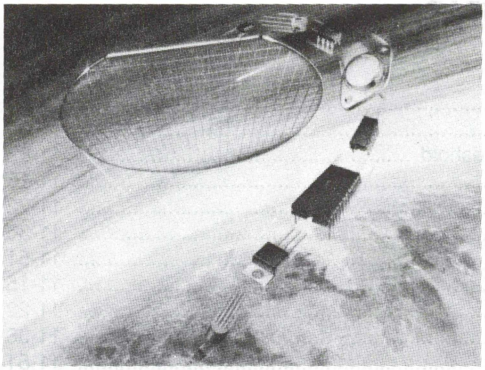
C4 may be removed for most applications

C6 Tolerance = ±1% in test circuit and ±5% in typical applications

R3 Tolerance = ±1%

R4 Tolerance = ±10%

R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application



Other Linear

11

OTHER LINEAR

Device	Function	Page
CA3059	Zero Voltage Switch	11-3
CA3079	Zero Voltage Switch	11-3
MC1422	Timing Circuit with Adjustable Threshold	11-8
MC1455	Timing Circuit	11-15
MC1494L	Four-Quadrant Multiplier	11-22
MC1495L	Four-Quadrant Multiplier	11-36
MC1496	Balanced Modulator-Demodulator	11-51
MC1555	Timing Circuit	11-15
MC1594L	Four-Quadrant Multiplier	11-22
MC1595L	Four-Quadrant Multiplier	11-36
MC1596	Balanced Modulator-Demodulator	11-51
MC3344	Programmable Frequency Switch	11-61
MC3370P	Zero Voltage Switch	11-66
MC3456	Dual Timing Circuit	11-69
MC3556	Dual Timing Circuit	11-69
NE565N	Phase-Locked Loop	11-76
SAA1042,A	Stepper Motor Driver	11-80
TDA1085A,B	Universal Motor Speed Controller	11-85
TDA1185A	Triac Phase Angle Controller	11-92
TDA1285A	Universal Motor Speed Controller	11-99
UAA1016A,B	Zero Voltage Controller	11-106

MOTOROLA

CA3059
CA3079

ZERO VOLTAGE SWITCHES

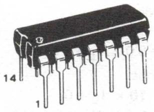
. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control

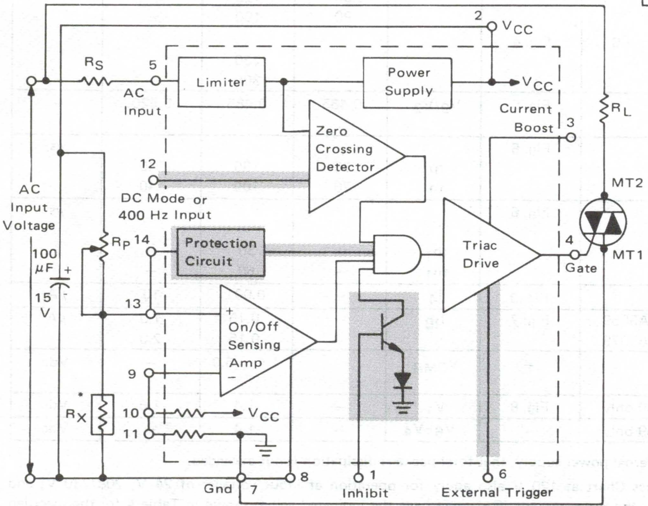
ZERO VOLTAGE SWITCHES

SILICON MONOLITHIC
INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM


2
V_{CC}
R_S
5
AC Input
Limiter
Power Supply
V_{CC}
Current Boost
3
R_L
Zero Crossing Detector
12
DC Mode or 400 Hz Input
AC Input Voltage
MT2
R_P
14
Protection Circuit
Triac Drive
4
Gate
MT1
100 µF
+
15 V
13
+
On/Off Sensing Amp
–
9
*
R_X
10
V_{CC}
11
Gnd
7
8
1
Inhibit
6
External Trigger

*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

TABLE A

AC Input Voltage (50/60 Hz) vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter-Power Supply** – Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor (R_S) values are given in Table A.

2. **Differential On/Off Sensing Amplifier** – Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.

3. **Zero-Crossing Detector** – Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.

4. **Triac Drive** – Supplies high-current pulses to the external power controlling thyristor.

5. **Protection Circuit (CA3059 only)** – A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.

6. **Inhibit Capability (CA3059 only)** – Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.

7. **High Power DC Comparator Operation (CA3059 only)** – Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
DC Supply Voltage		V_{CC}		Vdc
(Between Pins 2 and 7	CA3059		12	
	CA3079		10	
DC Supply Voltage		V_{CC}		Vdc
(Between Pins 2 and 8)	CA3059		12	
	CA3079		10	
Peak Supply Current (Pins 5 and 7)		$I_{5,7}$	±50	mA
Fail-Safe Input Current (Pin 14)		I_{14}	2.0	mA
Output Pulse Current (Pin 4)		I_{out}	150	mA
Junction Temperature		T_J	150	°C
Operating Temperature Range		T_A	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50-60 Hz, T_A = 25°C)**

Characteristic		Test Circuits	Symbol	Min	Typ	Max	Unit
DC Supply Voltage		Fig. 2	V_S				Vdc
Inhibit Mode							
R_S = 10 k, I_L = 0				6.1	6.5	7.0	
R_S = 5.0 k, I_L = 2.0 mA				–	6.1	–	
Pulse Mode							
R_S = 10 k, I_L = 0				6.0	6.4	7.0	
R_S = 5.0 k, R_L = 2.0 mA				–	6.2	–	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)		Fig. 3	I_{GT}	–	160	–	mA
Peak Output Current, Pulsed		Fig. 3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0							
Pin 3 Open				50	125	–	
Pins 3 and 2 Connected				90	190	–	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0		Fig. 4					
Pin 3 Open				–	230	–	
Pins 3 and 2 Connected				–	300	–	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)		Fig. 5	V_9/V_2	0.465	0.485	0.520	–
Total Gate Pulse Duration (C_{Ext} = 0)		Fig. 6					μs
Positive dv/dt			tp	70	100	140	
Negative dv/dt			tn	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)		Fig. 6					μs
Positive dv/dt			tp_1	–	50	–	
Negative dv/dt			tn_1	–	60	–	
Output Leakage Current Inhibit Mode***		Fig. 3	I_4	–	0.001	10	μA
Input Bias Current	CA3059	Fig. 7	I_{IB}	–	0.15	1.0	μA
	CA3079			–	0.15	2.0	
Common Mode Input Voltage Range (Pins 9 and 13 Connected)		–	V_{CMR}	–	1.4 to 5.0	–	Vdc
Inhibit Input Voltage	CA3059 only	Fig. 8	V_1	–	1.4	1.6	Vdc
External Trigger Voltage	CA3059 only	–	V_6-V_4	–	1.4	–	Vdc

*Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.

**The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.

***I_4 out of Pin 4
2 V on Pin 1
S1 position 2

TEST CIRCUITS

(All resistor values are in ohms)

FIGURE 2 – DC SUPPLY VOLTAGE

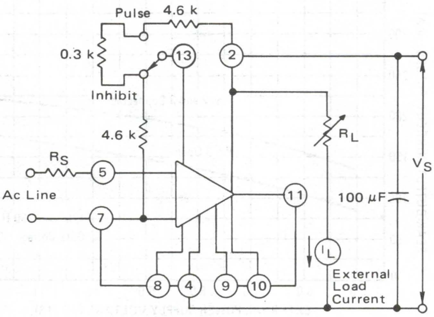

Pulse
4.6 k
0.3 k
13
2
Inhibit
4.6 k
RL
RS
5
Ac Line
7
11
100 µF
VS
IL
8
4
9
10
External
Load
Current

FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

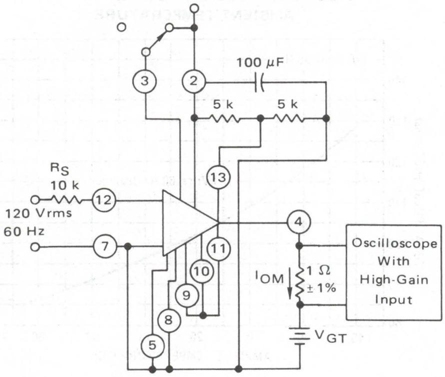

3
2
100 µF
5 k
5 k
RS
10 k
13
12
120 Vrms
60 Hz
7
4
11
10
9
8
5
IOM
1 Ω
± 1%
Oscilloscope
With
High-Gain
Input
VGT

FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

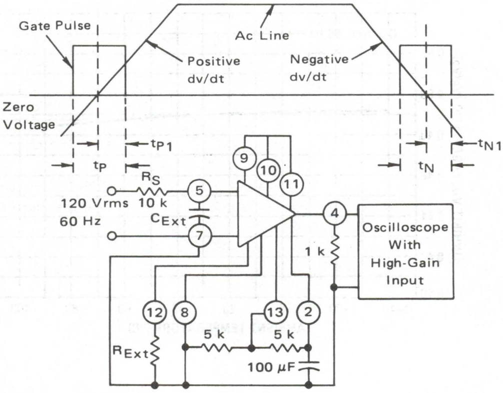

Gate Pulse
Ac Line
Positive
dv/dt
Negative
dv/dt
Zero
Voltage
tP1
tP
tN1
tN
9
10
11
RS
5
120 Vrms
10 k
60 Hz
CExt
7
4
1 k
Oscilloscope
With
High-Gain
Input
12
8
13
2
5 k
5 k
RExt
100 µF

FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

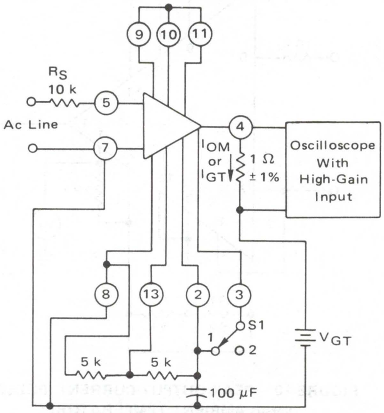

9
10
11
RS
10 k
5
Ac Line
7
4
IOM
or
IGT
1 Ω
± 1%
Oscilloscope
With
High-Gain
Input
8
13
2
3
S1
1
2
VGT
5 k
5 k
100 µF

FIGURE 5 – INPUT INHIBIT RATIO

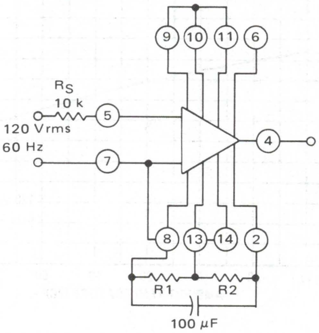
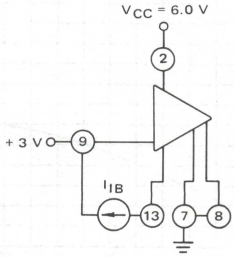

9
10
11
6
RS
10 k
5
120 Vrms
60 Hz
7
4
8
13
14
2
R1
R2
100 µF

FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT


VCC = 6.0 V
2
+ 3 V
9
IIB
13
7
8

TYPICAL CHARACTERISTICS

FIGURE 8 – INHIBIT INPUT VOLTAGE TEST

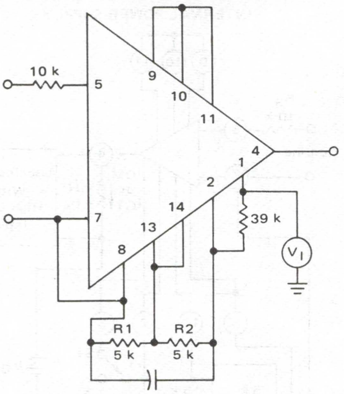


FIGURE 9 – PEAK OUTPUT CURRENT (PULSED) versus EXTERNAL POWER SUPPLY VOLTAGE

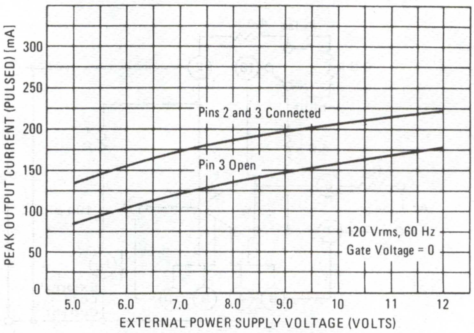


FIGURE 10 – PEAK OUTPUT CURRENT (PULSED) versus AMBIENT TEMPERATURE

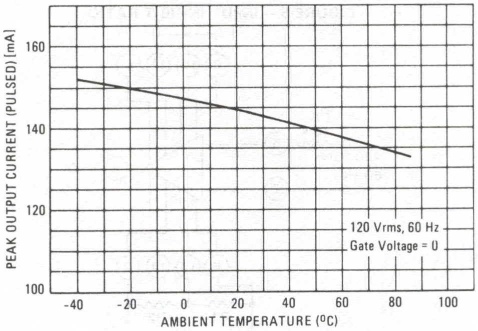


FIGURE 11 – TOTAL PULSE WIDTH versus AMBIENT TEMPERATURE

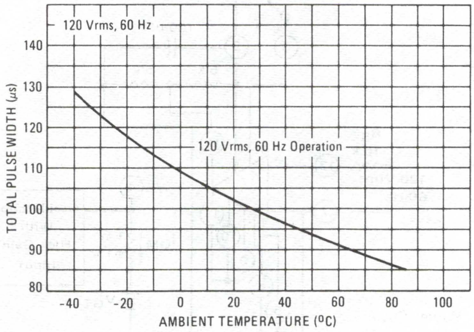


FIGURE 12 – INTERNAL SUPPLY versus AMBIENT TEMPERATURE

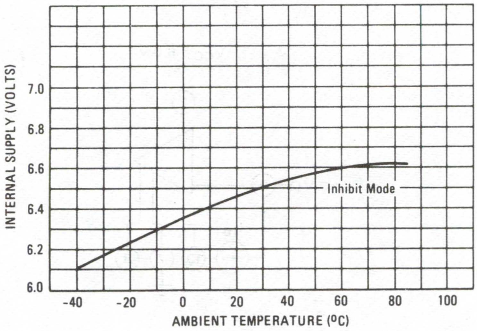


FIGURE 13 – INHIBIT VOLTAGE RATIO versus AMBIENT TEMPERATURE

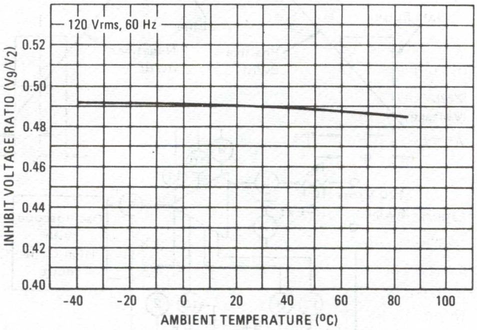
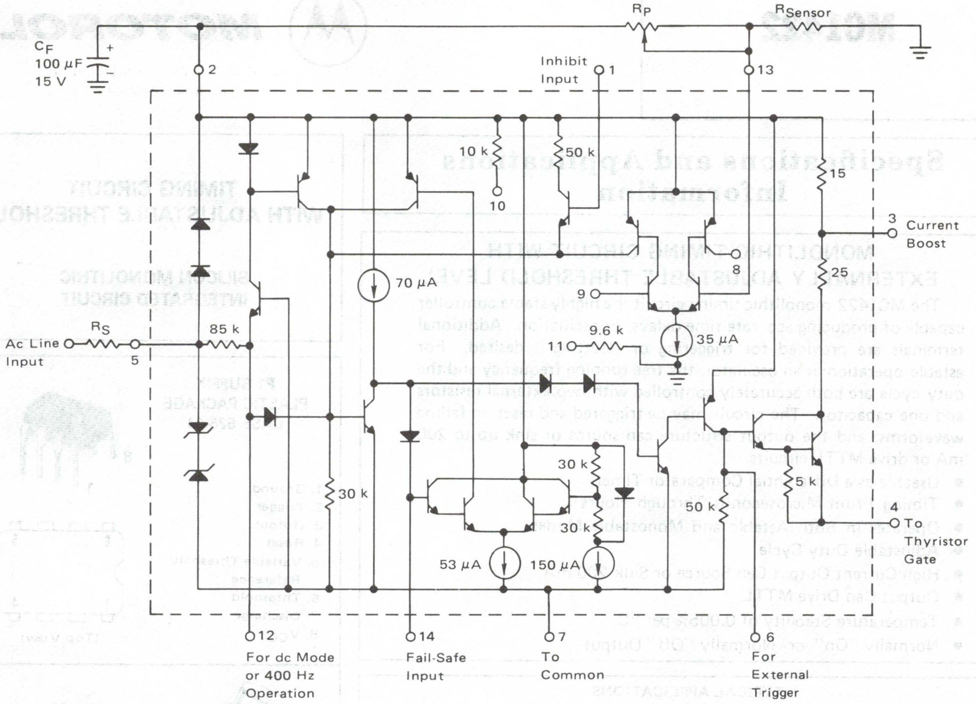


FIGURE 14 – CIRCUIT SCHEMATIC



Rp
RSensor
CF
100 μF
15 V
+
2
Inhibit Input
1
13
10 k
50 k
10
15
3
Current Boost
8
9
25
70 μA
Rs
85 k
Ac Line Input
5
9.6 k
11
35 μA
30 k
30 k
5 k
50 k
4
To Thyristor Gate
30 k
53 μA
150 μA
12
For dc Mode or 400 Hz Operation
14
Fail-Safe Input
7
To Common
6
For External Trigger

NOTE: Current sources are established by an internal reference.
Pins 1, 6, 12, and 14 are not used with CA3079.

APPLICATION INFORMATION

Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

A. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

B. Sensor Resistance (R_X) and Rp values should be between 2 kΩ and 100 kΩ.

C. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function (CA3059 Only)

A priority inihibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 μA is required. A DTL or T^2L logic 1 applied to pin 1 will activate the inhibit function.

DC Gate Current Mode (CA3059 Only)

When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

MC1422

MOTOROLA

Specifications and Applications Information

TIMING CIRCUIT WITH ADJUSTABLE THRESHOLD

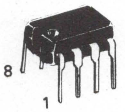
SILICON MONOLITHIC INTEGRATED CIRCUIT

MONOLITHIC TIMING CIRCUIT WITH EXTERNALLY ADJUSTABLE THRESHOLD LEVEL

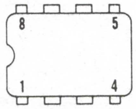
The MC1422 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Useable as a Differential Comparator Timer
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04



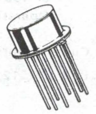
1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}



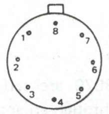
(Top View)

TYPICAL APPLICATIONS

Time Delay Generation	Precision Timing	Missing Pulse Detection
Sequential Timing	Pulse Generation	Pulse Width Modulation
Linear Sweep Generation	Pulse Shaping	Pulse Position Modulation



G SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}

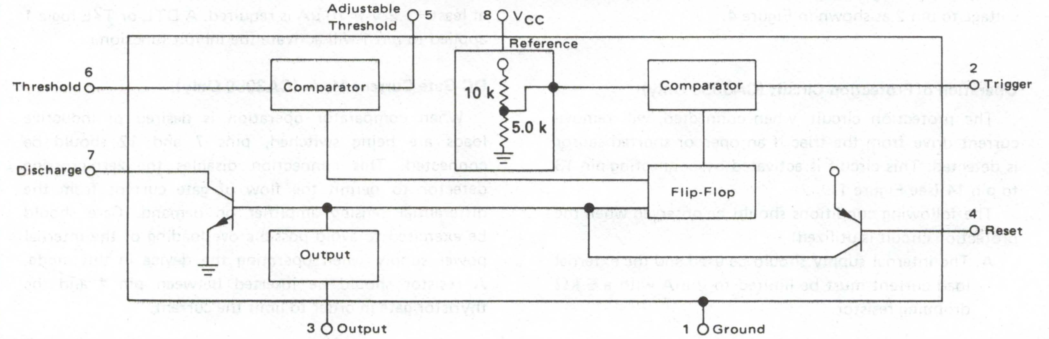
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

Type	Temperature Range	Package
MC1422G	0 to +70°C	Metal Can
MCC1422P1	0 to +70°C	Plastic DIP

FIGURE 1 – BLOCK DIAGRAM



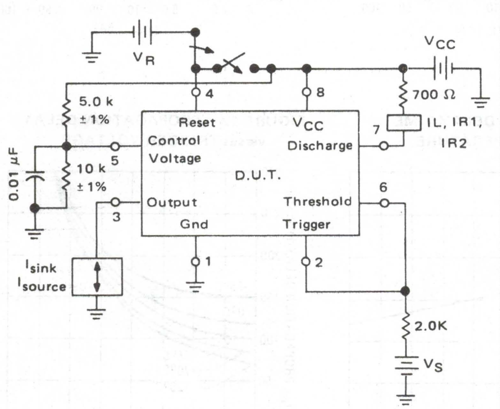
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +14 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	14	V
Supply Current	I_D				mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	6.0	
V_{CC} = 14 V, $R_L = \infty$		–	10	15	
Low State (Note 1)					
Timing Error (Note 2)					
R_A, R_B = 1.0 kΩ to 100 kΩ					
Initial Accuracy C = 0.1 μF		–	1.0	–	%
Drift with Temperature		–	50	–	PPM/°C
Drift with Supply Voltage		–	0.01	–	%/Volt
Threshold Voltage (Figure 2)	V_{th}	–	2/3	–	xV_{CC}
Trigger Voltage	V_T				V
V_{CC} = 14 V		–	5.0	–	
V_{CC} = 5.0 V		–	1.67	–	
Trigger Current	I_T	–	0.5	–	μA
Discharge Leakage Current	I_{dis}	–	–	250	nA
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	–	1.0	μA
Output Voltage Low	V_{OL}				V
(V_{CC} = 14 V)					
I_{sink} = 10 mA		–	0.1	0.35	
I_{sink} = 50 mA		–	0.4	1.0	
I_{sink} = 100 mA		–	2.0	3.5	
I_{sink} = 200 mA		–	2.5	–	
Output Voltage High	V_{OH}				V
(I_{source} = 25 mA)					
V_{CC} = 14 V		11.75	13.3	–	
V_{CC} = 5.0 V		2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	ns

NOTES:

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 14 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

FIGURE 2 – DC TEST CIRCUIT


V_R
V_{CC}
5.0 k
± 1%
4
8
700 Ω
Reset
V_{CC}
7
IL, IR1,
IR2
0.01 μF
10 k
± 1%
5
Control
Voltage
Discharge
D.U.T.
3
Output
Threshold
6
Gnd
Trigger
I_{sink}
I_{source}
1
2
2.0K
V_S

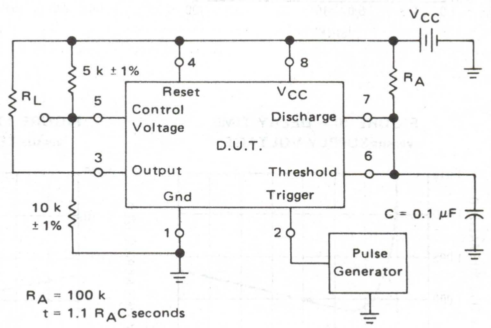
Notes:

V_{CC} = Supply Voltage: 5.0 V ⩽ V_{CC} ⩽ 14 V Range
V_S = Switching Voltage: 1.4 V ⩽ V_S ⩽ 11.0 V Range

When $V_S \geqslant 2/3\ V_{CC}$, V_O is low ≅ 0 at $R_L = \infty$
When $V_S \leqslant 1/3\ V_{CC}$, V_O is high ≅ V_{CC} at $R_L = \infty$

V_R = Reset Voltage: V_R = 0.4 V or 1.0 V during Reset Test
During other tests, Pin 4 tied to V_{CC}.

FIGURE 3 – AC TEST CIRCUIT


V_{CC}
5 k ± 1%
4
8
R_L
5
Reset
V_{CC}
7
R_A
Control
Voltage
Discharge
D.U.T.
3
6
Output
Threshold
Gnd
Trigger
10 k
± 1%
1
2
C = 0.1 μF
Pulse
Generator

R_A = 100 k
t = 1.1 R_AC seconds

External components must be bridged so that exact values are used in the frequency formula.

TYPICAL CHARACTERISTICS

($T_A = +25^{\circ}C$ unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

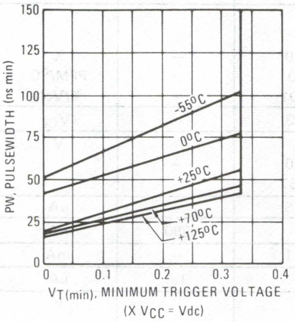


FIGURE 5 – SUPPLY CURRENT

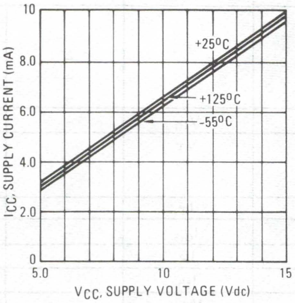


FIGURE 6 – HIGH OUTPUT VOLTAGE

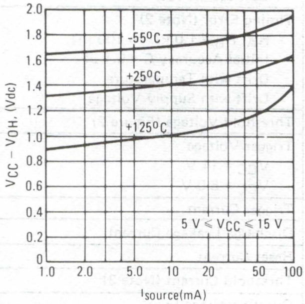


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

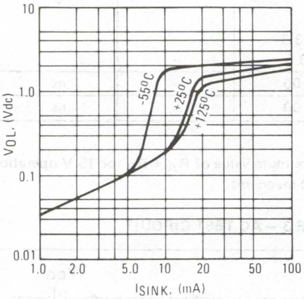


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

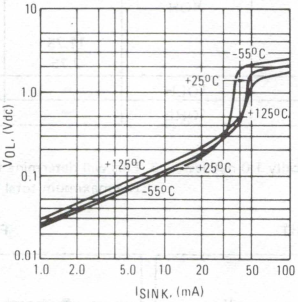


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

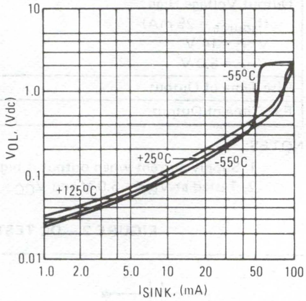


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

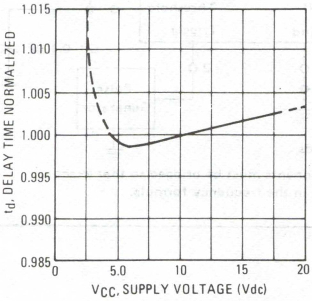


FIGURE 11 – DELAY TIME versus TEMPERATURE

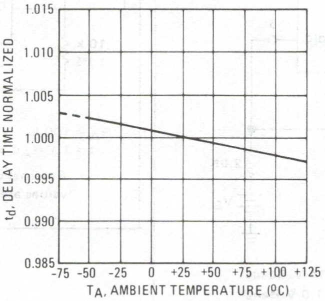


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE

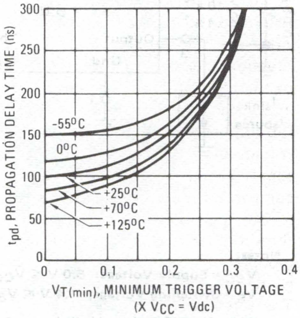
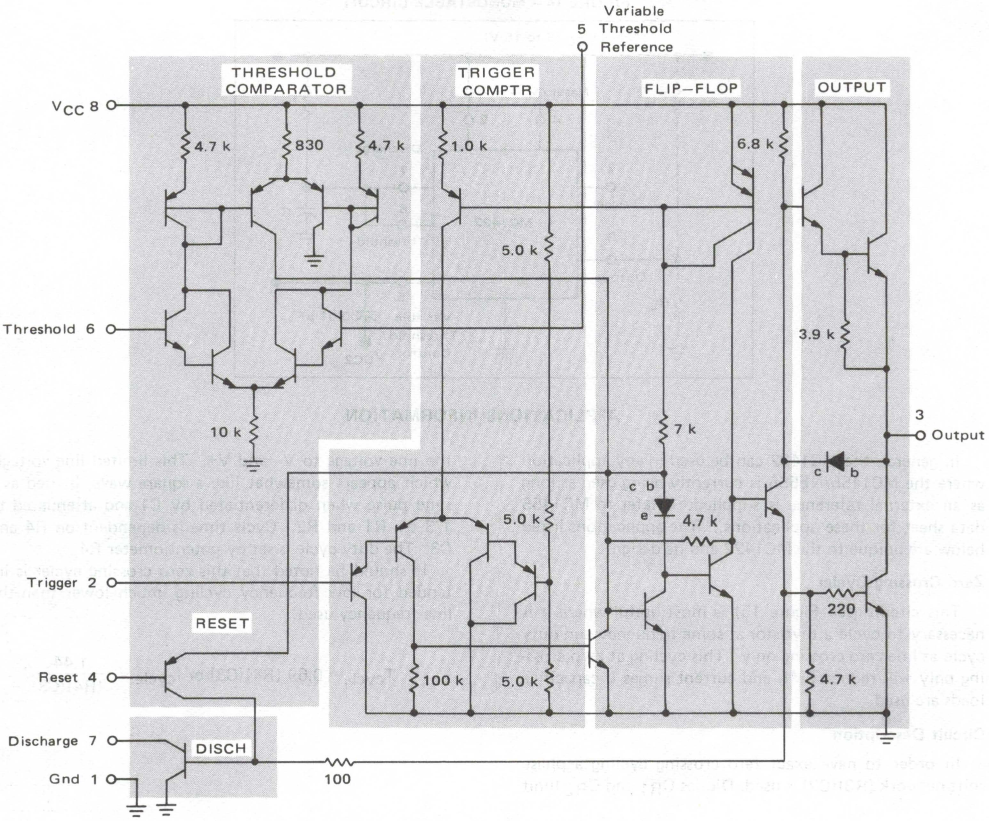


FIGURE 13 – CIRCUIT SCHEMATIC CONTROL VOLTAGE



GENERAL INFORMATION

The MC1422 is a monolithic timing circuit similar in performance and function to the MC1455 timer. It can be used in both the astable and monostable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are offered. The reference voltage of the trigger comparator is a fixed ratio of the supply voltage while the reference voltage of the threshold comparator is completely adjustable.

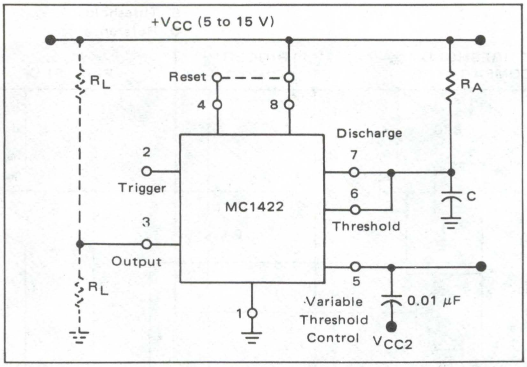
The MC1422 offers a completely independent variable threshold terminal. This feature allows it to be used as a modulation terminal as well as a synchronization terminal giving an additional degree of freedom in circuit design. The reference voltage pin (pin 5) for the threshold comparator is completely adjustable.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain low. The reset pin should be tied to the supply voltage when not in use.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches the external reference voltage the threshold comparator resets the flip-flop. This discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 15. The trigger pulse width must be less than the timing period.

FIGURE 14 – MONOSTABLE CIRCUIT


+VCC (5 to 15 V)
RL
Reset
4
8
RA
Discharge
7
2
Trigger
MC1422
6
C
Threshold
3
Output
5
RL
1
Variable
Threshold
Control
0.01 µF
VCC2

APPLICATIONS INFORMATION

In general, the MC1422 can be used in any application where the MC1455/NE555 is currently being used as long as an external reference is supplied. (Refer to MC1455 data sheet for these applications.) The applications listed below are unique to the MC1422 and its design.

Zero Crossing Cycler

This circuit (see Figure 15) is most useful where it is necessary to cycle a thyristor at some frequency and duty cycle at line zero crossing only. This cycling at zero crossing only will reduce EMI, and current surges if capacitive loads are used.

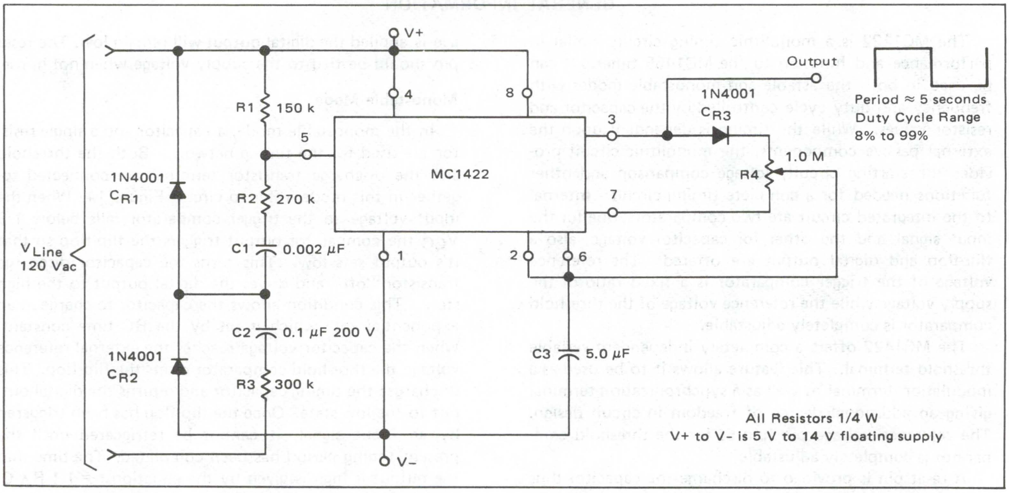
Circuit Description

In order to have exact zero crossing cycling a phase shift network (R3)(C2) is used. Diodes C_{R1} and C_{R2} limit the line voltage to V- and V+. This limited line voltage, which appears somewhat like a square wave, is used as a sync pulse when differentiated by C1 and attenuated to 1/3 by R1 and R2. Cycle time is dependent on R4 and C3. The duty cycle is set by potentiometer R4.

It should be noted that this zero crossing cycler is intended for low frequency cycling, much lower than the line frequency used.

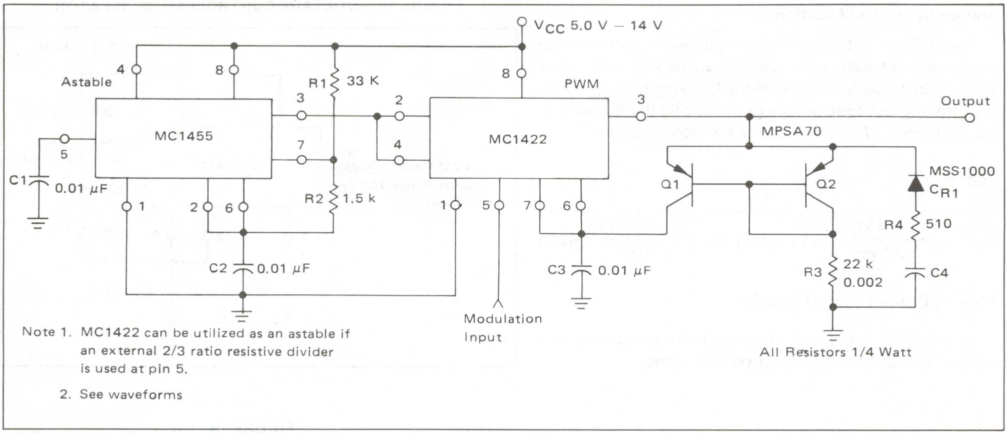
$$T_{cycle} = 0.69\,(R4)(C3) \text{ or } f_{cycle} = \frac{1.44}{(R4)(C3)}$$

FIGURE 15 – ZERO CROSSING CYCLER


V+
8
4
R1 150 k
5
MC1422
3
Output
1N4001
CR3
Period ≈ 5 seconds
Duty Cycle Range
8% to 99%
1.0 M
R4
7
1N4001
CR1
R2 270 k
VLine
120 Vac
C1 0.002 µF
1
2
6
C2 0.1 µF 200 V
1N4001
CR2
R3 300 k
C3 5.0 µF
V–

All Resistors 1/4 W
V+ to V- is 5 V to 14 V floating supply

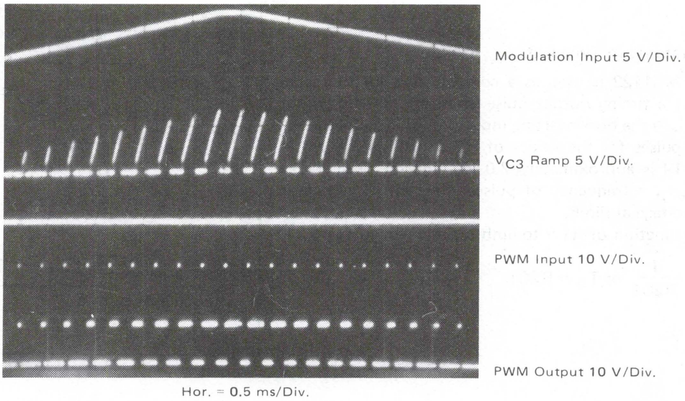
FIGURE 16 – PULSE WIDTH MODULATOR


VCC 5.0 V – 14 V
4
8
Astable
R1
33 K
3
2
8
PWM
3
Output
MC1455
7
4
MC1422
MPSA70
5
C1
0.01 µF
1
2
6
R2
1.5 k
1
5
7
6
Q1
Q2
MSS1000
CR1
R4
510
C2
0.01 µF
C3
0.01 µF
R3
22 k
0.002
C4
Modulation Input
All Resistors 1/4 Watt

Note 1. MC1422 can be utilized as an astable if an external 2/3 ratio resistive divider is used at pin 5.

2. See waveforms

FIGURE 17 – PULSE WIDTH MODULATOR WAVEFORMS



Pulse Width Modulator

The MC1422 is used as a pulse width modulator (PWM) with the MC1455 being utilized as an astable. The MC1422 can be used as an astable in place of the MC1455 if an external reference of approximately 2/3 V_{CC} is used at Pin 5.

The transistors Q1 and Q2 are configured as a current mirror to provide a linear voltage ramp across C3. This constant current scheme attributes a relatively linear transfer characteristic for the pulse width modulator.

Several considerations must be made when using this circuit.

1. The minimum duty cycle out is limited to the complement of the input signal. (i.e., a 95% duty cycle astable driving the PWM will give a minimum duty cycle output of ≃ 5%.)

   The maximum duty cycle out will also be limited to the maximum duty cycle in.

2. For the astable frequency:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)C}$$

3. Duty cycle (D.C.) for the astable:

$$DC = \frac{R_2}{R_1 + 2R_2}$$

For best results the charge time of C3 in the pulse width modulator should be equal to the period of the astable.

$$\frac{I_{Q1}}{C3\ (V_{CC} - 1)} = f_{in} = \frac{1}{T_{C3}} \quad I_{Q1} \simeq I_{Q2} = \frac{V_{CC} - V_{BE}}{R3}$$

V_{CC} = 10 V linearity typically 3% modulation input from 2 volts to 8 volts.

Voltage Controlled Oscillator

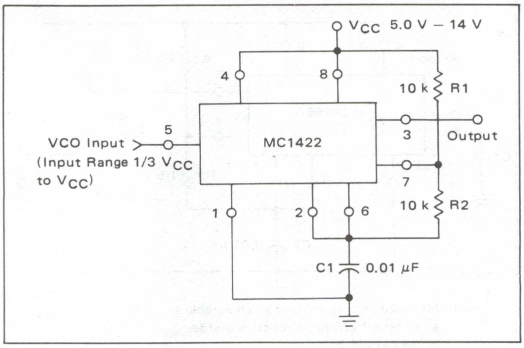
The VCO circuit, which has a nonlinear transfer characteristic will operate satisfactorily up to 200 kHz. The VCO input range is effective from 1/3 V_{CC} to V_{CC} - 2 V, with the highest control voltage producing the lowest output frequency. The equation for the frequency is:

$$f_{out} \simeq \frac{1}{\ln\left(1-\frac{V5-1/3\,V_{CC}}{2/3\,V_{CC}}\right)(R1+R2)C1+\ln\left(\frac{V5-1/3\,V_{CC}}{V5}\right)R2C1}$$

V5 = VCO input control voltage

It should be noted that, the output duty cycle will vary somewhat over the VCO input control range.

FIGURE 18 – VOLTAGE CONTROLLED OSCILLATOR


V_{CC} 5.0 V – 14 V
4
8
10 k
R1
5
3
Output
VCO Input
(Input Range 1/3 V_{CC} to V_{CC})
MC1422
7
1
2
6
10 k
R2
C1
0.01 µF

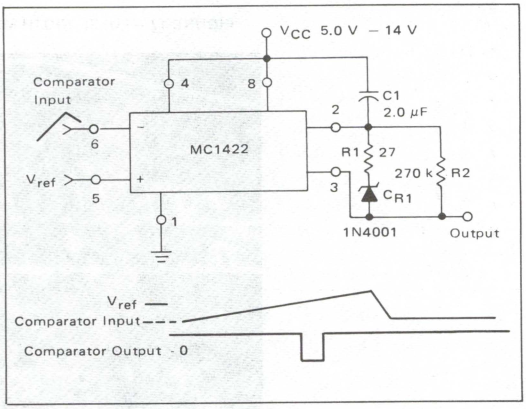
Comparator with Time Out

The MC1422 is used as a comparator with the capability of a timing output pulse when the inverting input (Pin 6) is ⩾ the non-inverting input (Pin 5). The frequency of the pulses for the values of R2 and C1 as shown in Figure 19 is approximately 2.0 Hz, and the pulse width 0.3 ms, f_p = frequency of pulses while Pin 6 voltage is above voltage at Pin 5.

The function of R1 is to limit di/dt, when charging C1.

$$f_p \simeq \frac{1}{R2C1} \text{ or } T_p \simeq R2C1$$

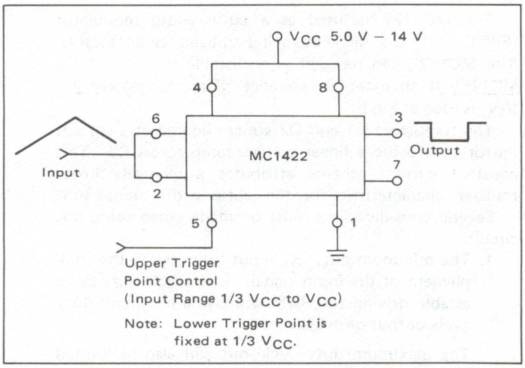
FIGURE 19


V_{CC} 5.0 V – 14 V
Comparator Input
4
8
C1
2.0 µF
2
–
6
MC1422
R1
27
270 k
R2
V_{ref}
+
5
3
C_{R1}
1
1N4001
Output
V_{ref}
Comparator Input
Comparator Output - 0

Schmitt Trigger

The MC1422 is very useful as a Schmitt Trigger as shown in Figure 20. The lower trigger point is fixed at 1/3 V_{CC}, but the upper trigger point is adjustable by means of Pin 5 from 1/3 V_{CC} to slightly less than V_{CC}. The Schmitt trigger will operate with input frequencies up to 50 kHz.

FIGURE 20


V_{CC} 5.0 V – 14 V
4
8
6
3
Output
Input
MC1422
7
2
5
1
Upper Trigger Point Control
(Input Range 1/3 V_{CC} to V_{CC})
Note: Lower Trigger Point is fixed at 1/3 V_{CC}.

MOTOROLA

MC1455
MC1555

Specifications and Applications Information

TIMING CIRCUIT

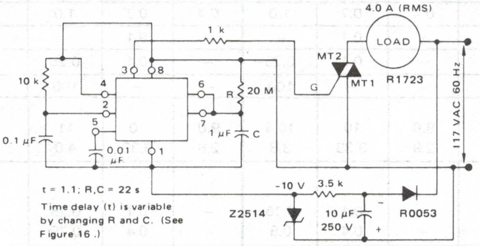
SILICON MONOLITHIC INTEGRATED CIRCUIT

TIMING CIRCUIT

The MC1555/MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

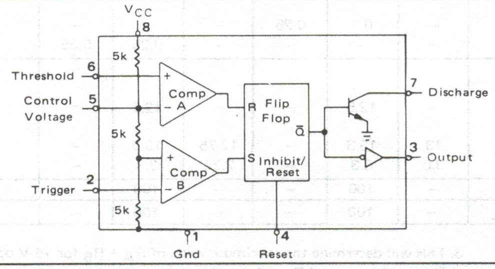
FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT


4.0 A (RMS)
LOAD
1 k
MT2
10 k
3
8
4
6
2
5
7
R
20 M
G
MT1
R1723
117 VAC 60 Hz
0.1 µF
0.01 µF
1
1 µF
C
-10 V
3.5 k
Z2514
10 µF
250 V
R0053

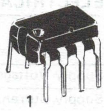
t = 1.1; R,C = 22 s

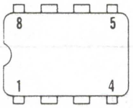
Time delay (t) is variable by changing R and C. (See Figure 16.)

FIGURE 2 – BLOCK DIAGRAM


VCC
8
5k
Threshold
6
Control Voltage
5
5k
Comp A
R
Flip Flop
Q̄
S
Inhibit/ Reset
7
Discharge
3
Output
Comp B
2
Trigger
5k
1
Gnd
4
Reset

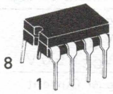
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04
(Top View)
(MC1455P1 only)

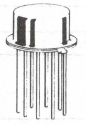




1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

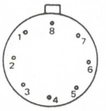
U SUFFIX
CERAMIC PACKAGE
CASE 693-02





G SUFFIX
METAL PACKAGE
CASE 601-04

(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1455G	–	0°C to +70°C	Metal Can
MC1455P1	NE555V	0°C to +70°C	Plastic DIP
MC1455U	–	0°C to +70°C	Ceramic DIP
MC1555G	–	-55°C to +125°C	Metal Can
MC1555U	–	-55°C to +125°C	Ceramic DIP

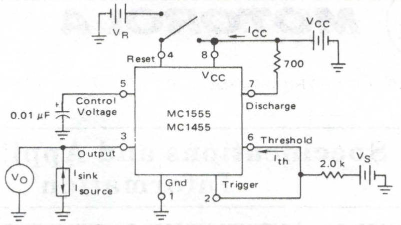
TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A		°C
MC1555		-55 to +125	
MC1455		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)

a). When $V_S \geq 2/3\ V_{CC}$, V_O is low.

b). When $V_S \leq 1/3\ V_{CC}$, V_O is high.

c). When V_O is low, pin 7 sinks current. To test for Reset, set V_O, high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC1555			MC1455			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current	I_{CC}							mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, $R_L = \infty$		–	10	12	–	10	15	
Low State, (Note 1)								
Timing Error (Note 2)								
R = 1.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 µF		–	0.5	2.0	–	1.0	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.05	0.20	–	0.10	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	–	0.1	0.25	µA
Discharge Leakage Current (Pin 7)	I_{dis}	–	–	100	–	–	100	nA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							
(V_{CC} = 15 V)								V
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.2	–	2.0	2.5	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns

NOTES:

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
   Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

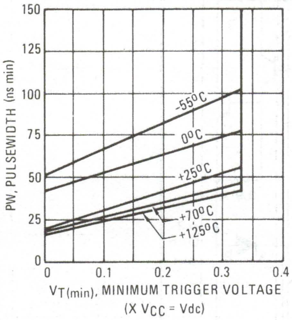


FIGURE 5 – SUPPLY CURRENT

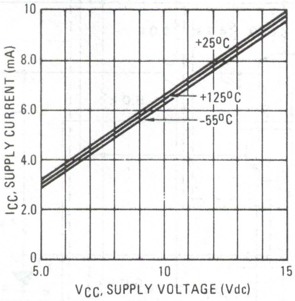


FIGURE 6 – HIGH OUTPUT VOLTAGE

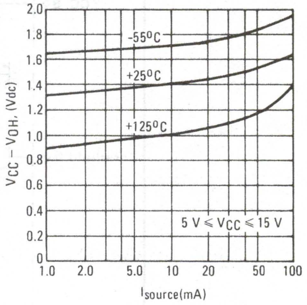


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

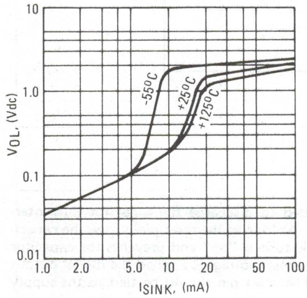


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

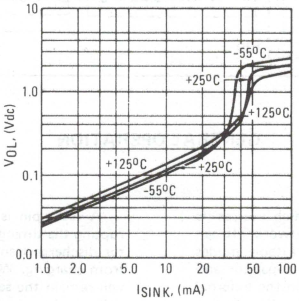


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

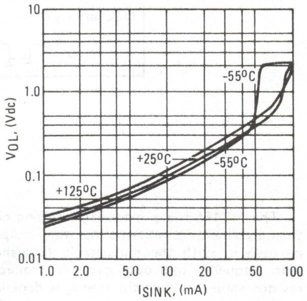


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

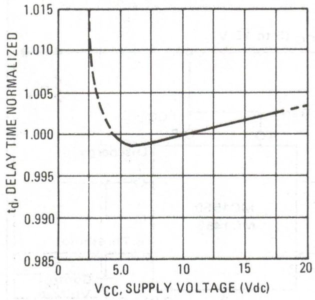


FIGURE 11 – DELAY TIME versus TEMPERATURE

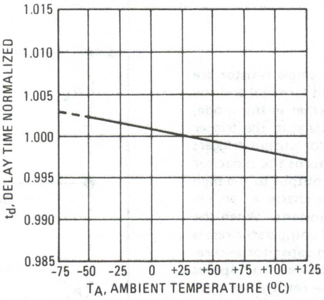


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE

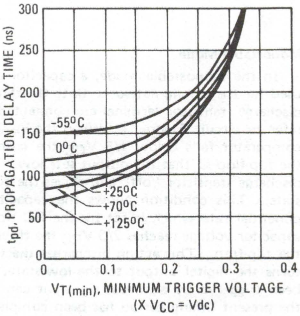
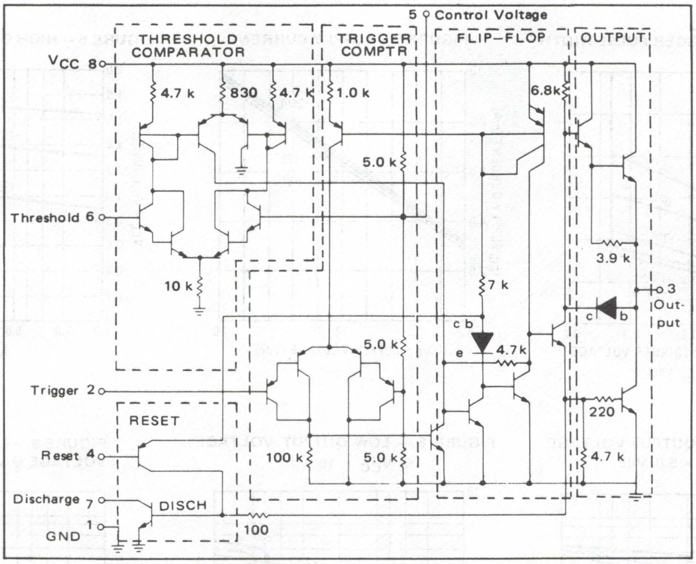


FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC


5 Control Voltage
THRESHOLD COMPARATOR
TRIGGER COMPTR
FLIP-FLOP
OUTPUT
VCC 8
4.7 k
830
4.7 k
1.0 k
6.8k
5.0 k
Threshold 6
3.9 k
10 k
7 k
3
Out-put
c b
c
b
5.0 k
e
4.7k
Trigger 2
220
RESET
Reset 4
100 k
5.0 k
4.7 k
Discharge 7
DISCH
1
GND
100

GENERAL OPERATION

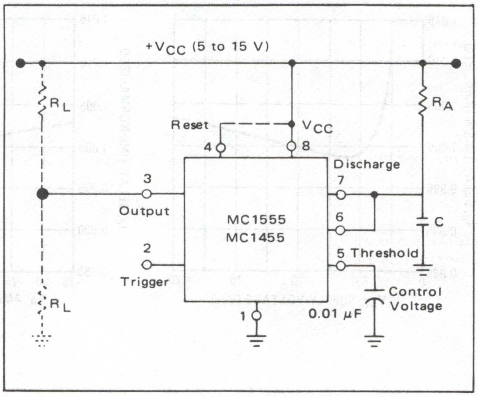
The MC1555 is a monolithic timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

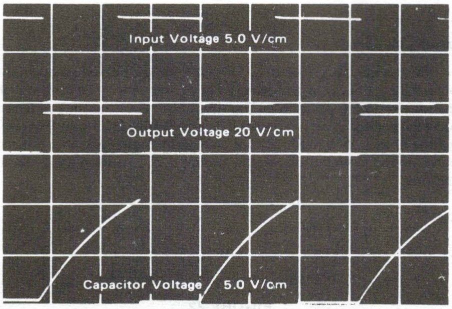
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT


+VCC (5 to 15 V)
RL
RA
Reset
VCC
4
8
Discharge
7
3
Output
MC1555
MC1455
6
C
2
5 Threshold
Trigger
Control Voltage
RL
1
0.01 μF

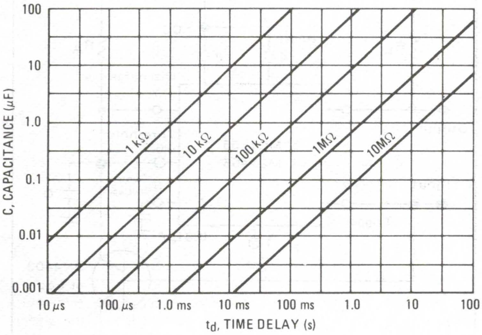
GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geqslant \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geqslant \frac{V_{CC}\ (Vdc)}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

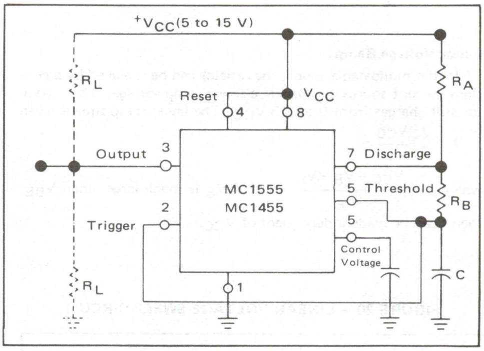
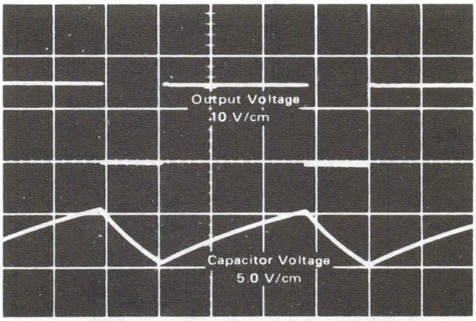


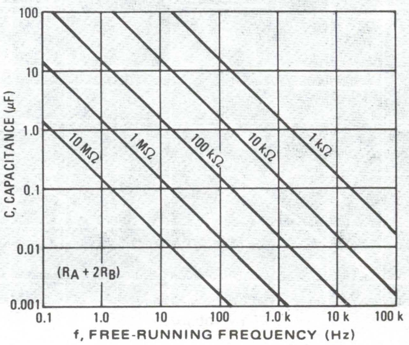
FIGURE 18 – ASTABLE WAVEFORMS



t = 20 µs/cm

(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 V_{CC}. The linear ramp time is given by

$$t = \frac{2}{3}\,\frac{V_{CC}}{I}$$

where $I = \dfrac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 20 – LINEAR VOLTAGE SWEEP CIRCUIT

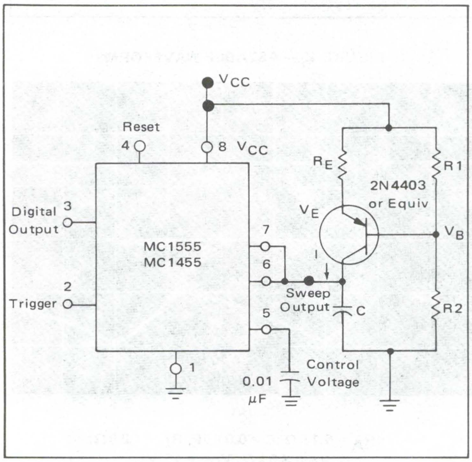

VCC
Reset
4
8 VCC
Digital Output
3
MC1555
MC1455
7
6
2
Trigger
5
1
RE
R1
2N4403 or Equiv
VE
VB
I
Sweep Output
C
R2
0.01 µF
Control Voltage

FIGURE 22

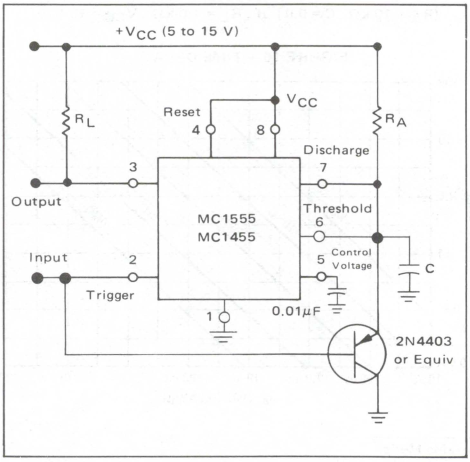

+VCC (5 to 15 V)
RL
Reset
4
8
VCC
RA
Discharge
7
3
Output
Threshold
6
MC1555
MC1455
Input
2
5
Control Voltage
C
Trigger
1
0.01µF
2N4403 or Equiv

FIGURE 21 – LINEAR VOLTAGE RAMP WAVEFORMS
(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)

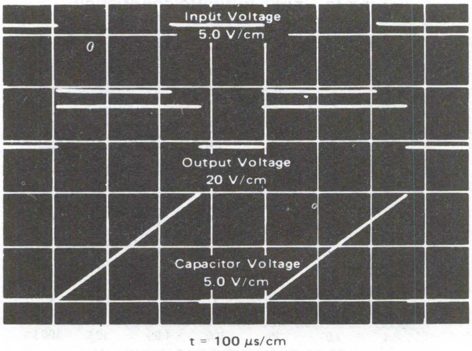
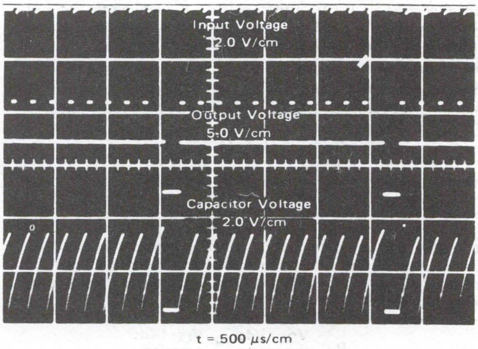


FIGURE 23 – MISSING PULSE DETECTOR WAVEFORMS
(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.1 µF, V_{CC} = 15 V)



APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 24

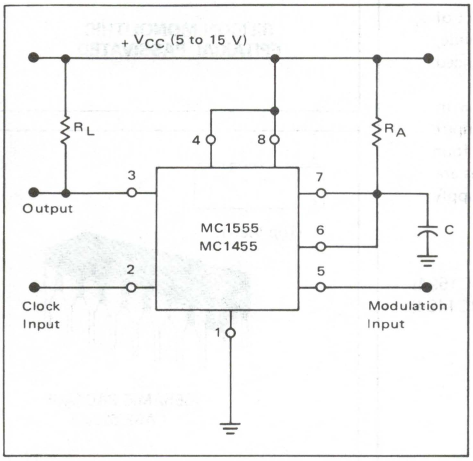
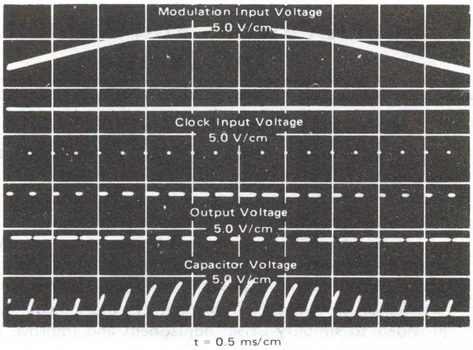

+ V_{CC} (5 to 15 V)
R_L
R_A
4
8
3
7
Output
MC1555
MC1455
6
C
2
5
Clock Input
Modulation Input
1

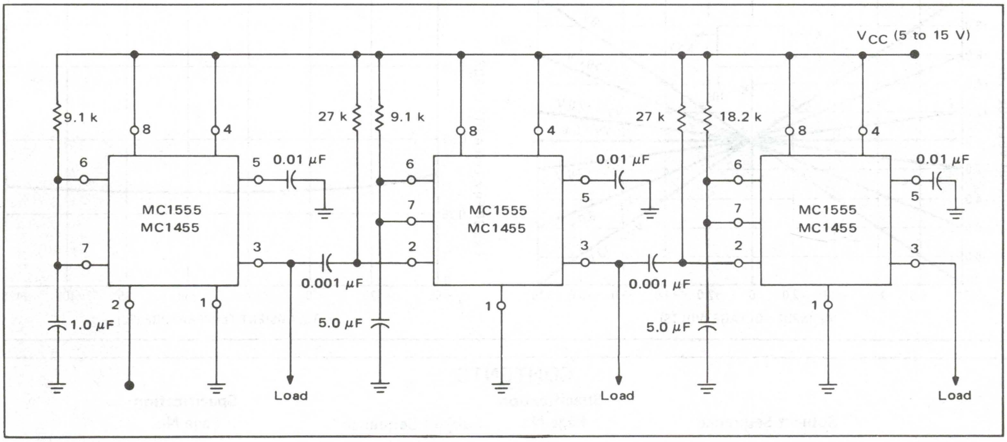
FIGURE 25 – PULSE WIDTH MODULATION WAVEFORMS (R_A = 10 kΩ, C = 0.02 µF, V_{CC} = 15 V)



Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26


V_{CC} (5 to 15 V)
9.1 k
8
4
6
5
0.01 µF
MC1555
MC1455
7
3
2
1
1.0 µF
0.001 µF
27 k
9.1 k
5.0 µF
Load
18.2 k
Load
Load

MC1494L
MC1594L

MOTOROLA

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

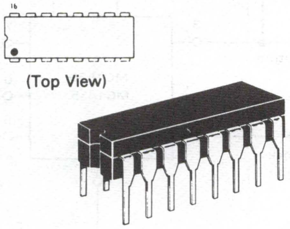
. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

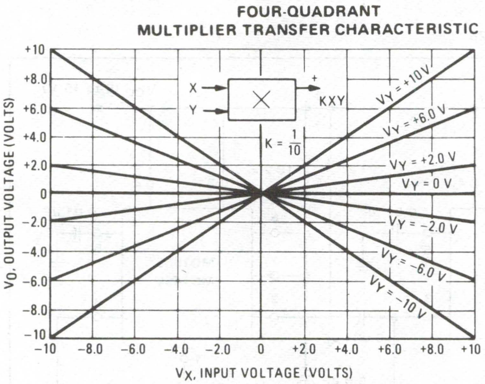
- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

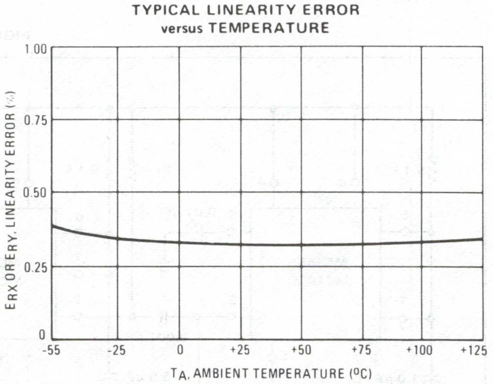
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 620-02





CONTENTS

Subject Sequence	Specification Page No.	Subject Sequence	Specification Page No.
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Electrical Characteristics	2	DC Applications	9
Test Circuits	3	AC Applications	11
Characteristic Curves	4	**Definitions**	13
Circuit Description	5	General Information Index	14
Circuit Schematic	5		
DC Operation	6		

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc
Differential Input Signal	V_9-V_6 $V_{10}-V_{13}$	$\pm\|6+I_1R_Y\|<30$ $\pm\|6+I_1R_X\|<30$	Vdc
Common-Mode Input Voltage			Vdc
$V_{CMY}=V_9=V_6$	V_{CMY}	±11.5	
$V_{CMX}=V_{10}=V_{13}$	V_{CMX}	±11.5	
Power Dissipation (Package Limitation)			
T_A = +25°C	P_D	750	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	5.0	mW/°C
Operating Temperature Range	T_A		°C
MC1594		-55 to +125	
MC1494		0 to + 70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594			MC1494			Unit
			Min	Typ	Max	Min	Typ	Max	
Linearity	1	E_{RX} or E_{RY}							%
Output error in Percent of full scale									
$-10\text{ V}<V_x<+10\text{ V}$ ($V_y=\pm10$ V)									
$-10\text{ V}<V_y<+10\text{ V}$ ($V_x=\pm10$ V)									
T_A = +25°C			–	± 0.3	± 0.5	–	± 0.5	± 1.0	
$T_A=T_{high}$ ①			–	–	± 0.8	–	–	± 1.3	
$T_A=T_{low}$ ②			–	–	± 0.8	–	–	± 1.3	
Input	2,3,4								
Voltage Range ($V_X=V_Y=V_{in}$)		V_{in}	±10	–	–	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\|V_{iox}\|$	–	0.1	1.6	–	0.2	2.5	V
(Y Input) (Note 1)		$\|V_{ioy}\|$	–	0.4	1.6	–	0.8	2.5	
Bias Current (X or Y Input)		I_b	–	0.5	1.5	–	1.0	2.5	μA
Offset Current (X or Y Input)		$\|I_{io}\|$	–	28	150	–	50	400	nA
Output	3,4								
Voltage Swing Capability		V_o	±10	–	–	±10	–	–	V_{pk}
Impedance		R_o	–	850	–	–	850	–	kΩ
Offset Voltage (Note 1)		$\|V_{oo}\|$	–	0.8	1.6	–	1.2	2.5	V
Offset Current (Note 1)		$\|I_{oo}\|$	–	17	34	–	25	52	μA
Temperature Stability (Drift)									
$T_A=T_{high}$ to T_{low}									
Output Offset (X = 0, Y = 0) Voltage		$\|TCV_{oo}\|$	–	1.3	–	–	1.3	–	mV/°C
Current		$\|TCI_{oo}\|$	–	27	–	–	27	–	nA/°C
X Input Offset (Y = 0)		$\|TCV_{iox}\|$	–	0.3	–	–	0.3	–	mV/°C
Y Input Offset (X = 0)		$\|TCV_{ioy}\|$	–	1.5	–	–	1.5	–	
Scale Factor		$\|TCK\|$	–	0.07	–	–	0.07	–	%/°C
Total dc Accuracy Drift (X = 10, Y = 10)		$\|TCE\|$	–	0.09	–	–	0.09	–	
Dynamic Response	5								
Small Signal (3 dB) X		$BW_{3\,dB(X)}$	–	0.8	–	–	0.8	–	MHz
Y		$BW_{3\,dB(Y)}$	–	1.0	–	–	1.0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	–	440	–	kHz
3° Relative Phase Shift		$f\phi$	–	240	–	–	240	–	
1% Absolute Error		$f\theta$	–	30	–	–	30	–	
Common Mode	6								
Input Swing (X or Y)		CMV	±10.5	–	–	±10.5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	-65	–	–	-65	–	dB
Power Supply	7								
Current		I_d^+	–	6.0	9.0	–	6.0	12	mAdc
		I_d^-	–	6.5	9.0	–	6.5	12	
Quiescent Power Dissipation		P_d	–	185	260	–	185	350	mW
Sensitivity		S^+	–	13	50	–	13	100	mV/V
		S^-	–	30	100	–	30	200	
Regulated Offset Adjust Voltages	7								
Positive		V_R^+	+3.5	+4.3	+5.0	+3.5	+4.3	+5.0	Vdc
Negative		V_R^-	-3.5	-4.3	-5.0	-3.5	-4.3	-5.0	
Temperature Coefficient (V_R^+ or V_R^-)		TCV_R	–	0.03	–	–	0.03	–	mV/°C
Power Supply Sensitivity (V_R^+ or V_R^-)		S_R^+, S_R^-	–	0.6	–	–	0.6	–	mV/V

Note 1: Offsets can be adjusted to zero with external potentiometers.

① T_{high} = +125°C for MC1594
+ 70°C for MC1494

② T_{low} = -55°C for MC1594
0°C for MC1494

TEST CIRCUITS

FIGURE 1 – LINEARITY

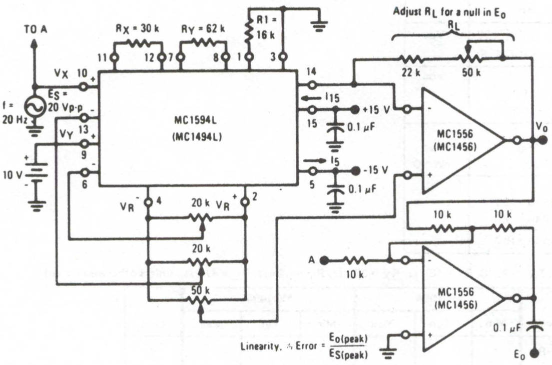

TO A
RX = 30 k
RY = 62 k
R1 = 16 k
Adjust RL for a null in Eo
RL
VX 10
ES = 20 Vp-p
f = 20 Hz
VY 13
10 V
MC1594L (MC1494L)
I15
+15 V
0.1 μF
I5
-15 V
22 k
50 k
MC1556 (MC1456)
Vo
VR- 4
20 k
VR+ 2
20 k
50 k
10 k
10 k
A
10 k
0.1 μF
Eo
Linearity, % Error = Eo(peak) / ES(peak)

FIGURE 2 – INPUT RESISTANCE

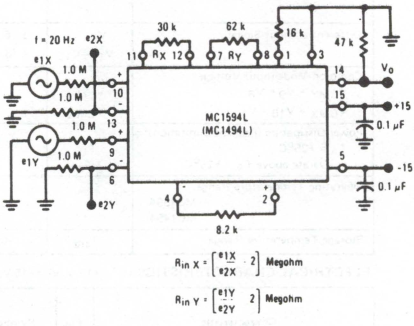

f = 20 Hz
e2X
e1X
30 k
62 k
16 k
47 k
RX
RY
1.0 M
1.0 M
1.0 M
1.0 M
e1Y
e2Y
MC1594L (MC1494L)
Vo
+15 V
0.1 μF
-15 V
0.1 μF
8.2 k
Rin X = [e1X/e2X - 2] Megohm
Rin Y = [e1Y/e2Y - 2] Megohm

FIGURE 3 – OFFSET VOLTAGES, GAIN

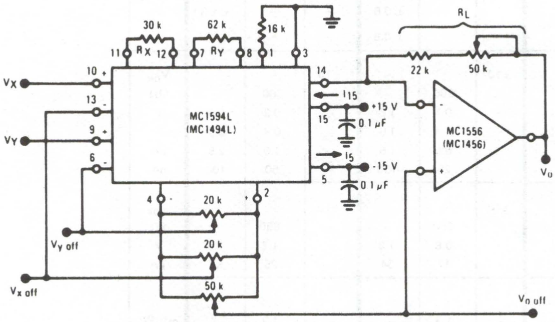

30 k
62 k
16 k
RX
RY
RL
22 k
50 k
VX
VY
MC1594L (MC1494L)
I15
+15 V
0.1 μF
I5
-15 V
0.1 μF
MC1556 (MC1456)
Vo
20 k
20 k
50 k
Vy off
Vx off
Vo off

FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

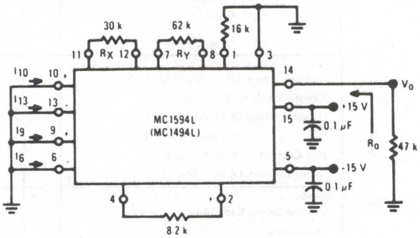

30 k
62 k
16 k
RX
RY
I10
I13
I9
I6
MC1594L (MC1494L)
Vo
+15 V
0.1 μF
-15 V
0.1 μF
Ro
47 k
8.2 k

FIGURE 5 – FREQUENCY RESPONSE

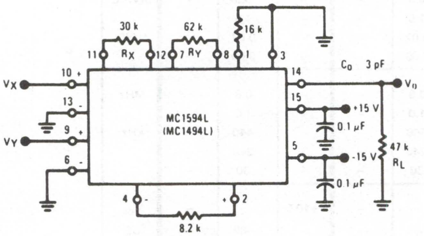

30 k
62 k
16 k
RX
RY
Co 3 pF
Vo
VX
VY
MC1594L (MC1494L)
+15 V
0.1 μF
-15 V
0.1 μF
47 k
RL
8.2 k

FIGURE 6 – COMMON MODE

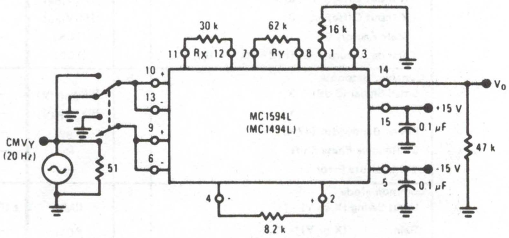

30 k
62 k
16 k
RX
RY
Vo
CMVY (20 Hz)
51
MC1594L (MC1494L)
+15 V
0.1 μF
-15 V
0.1 μF
47 k
8.2 k

FIGURE 7 – POWER-SUPPLY SENSITIVITY

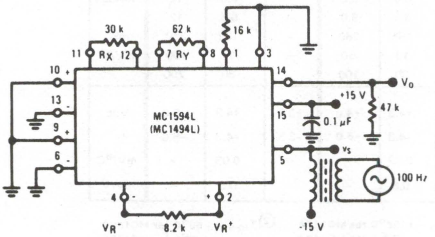
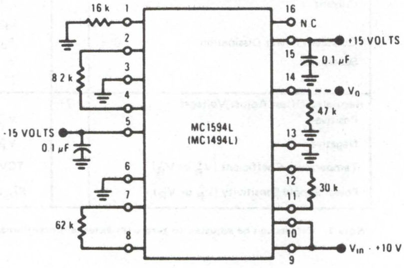

30 k
62 k
16 k
RX
RY
Vo
+15 V
47 k
0.1 μF
MC1594L (MC1494L)
vs
100 Hz
-15 V
VR-
8.2 k
VR+

FIGURE 8 – BURN-IN


16 k
NC
+15 VOLTS
8.2 k
Vo
47 k
-15 VOLTS
0.1 μF
MC1594L (MC1494L)
30 k
62 k
Vin - +10 V

TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_L = 47$ kΩ, $T_A = +25^{\circ}C$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

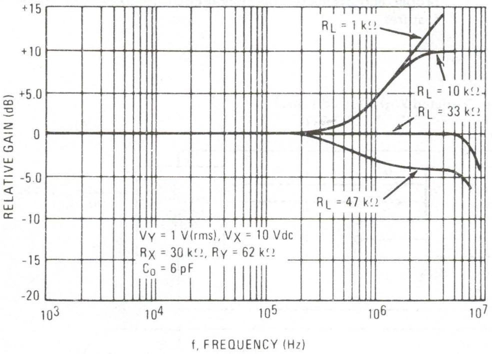


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

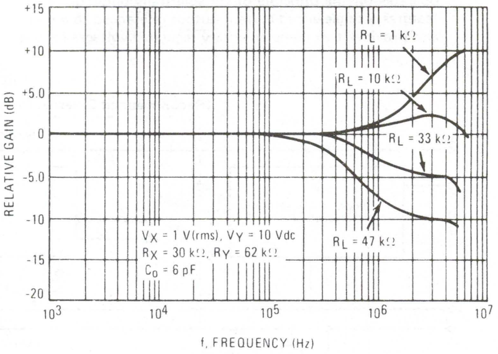


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

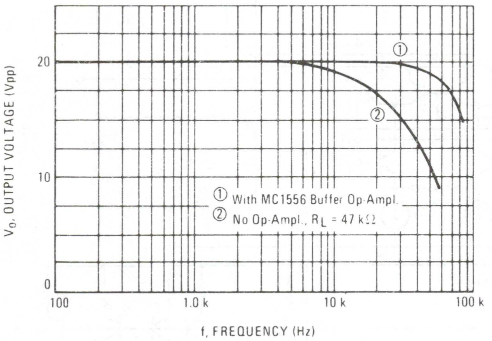


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

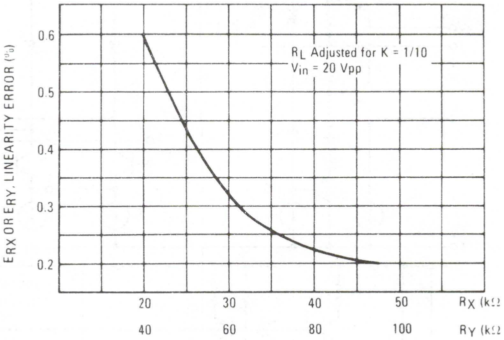


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

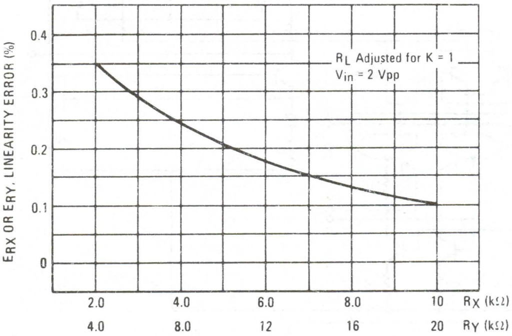
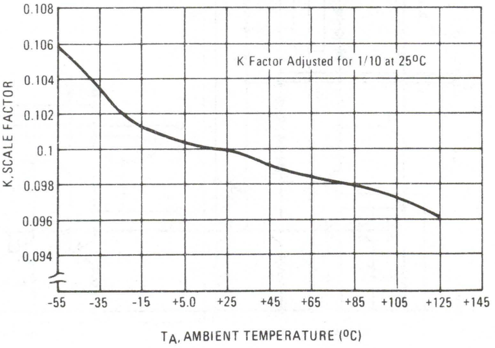


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

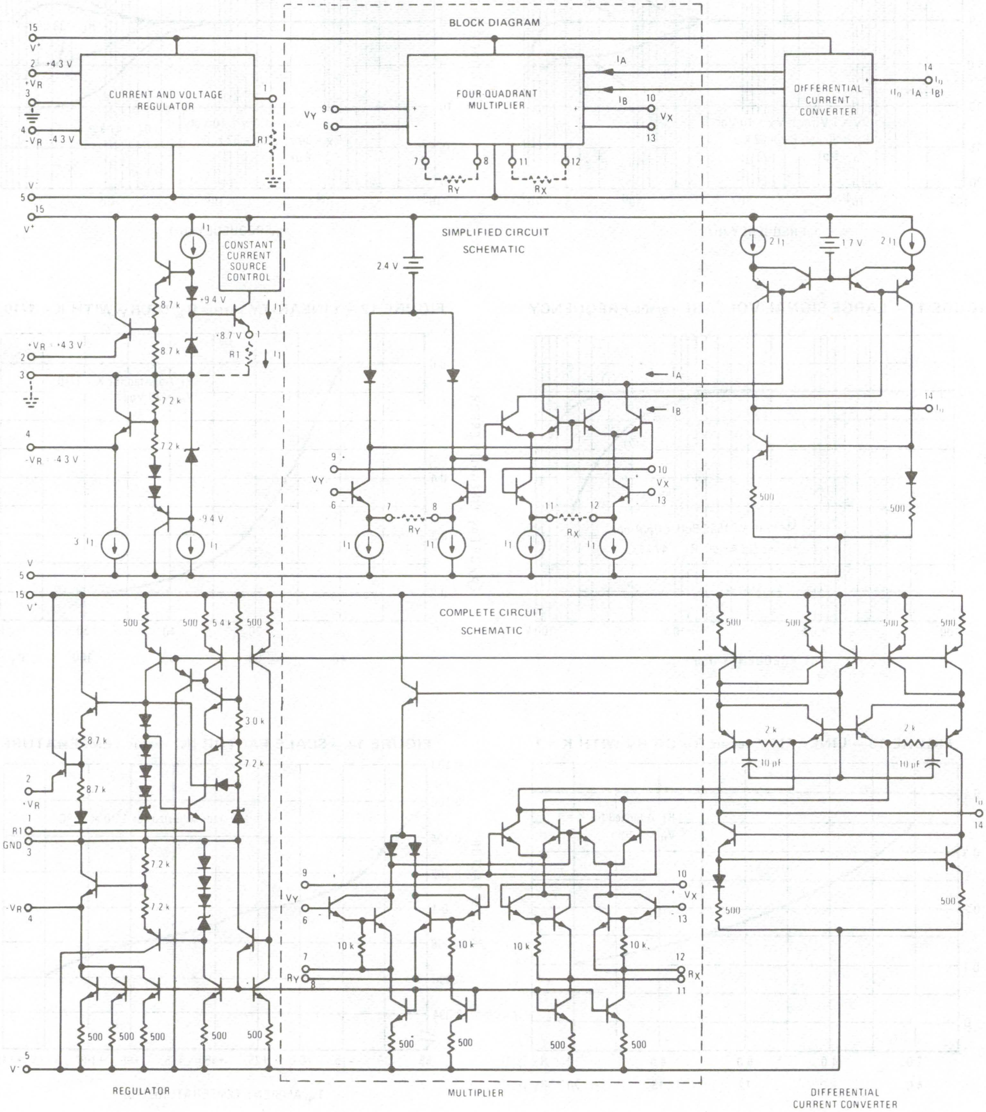
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15

(Recommended External Circuitry is Depicted With Dotted Lines)


BLOCK DIAGRAM
15 V+
2 +4.3 V +VR
3
4 -VR -4.3 V
CURRENT AND VOLTAGE REGULATOR
1
R1
VY 9 6
FOUR QUADRANT MULTIPLIER
IA
IB
10 VX 13
7 8 RY
11 12 RX
DIFFERENTIAL CURRENT CONVERTER
14 Io
Io = IA - IB
5 V-
SIMPLIFIED CIRCUIT SCHEMATIC
I1
CONSTANT CURRENT SOURCE CONTROL
2.4 V
+9.4 V
+8.7 V
8.7 k
7.2 k
2 I1
1.7 V
3 I1
-9.4 V
500
COMPLETE CIRCUIT SCHEMATIC
500
5.4 k
3.0 k
2 k
10 pF
10 k
R1
GND
REGULATOR
MULTIPLIER
DIFFERENTIAL CURRENT CONVERTER

1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately −4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595." The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

$$\text{where K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

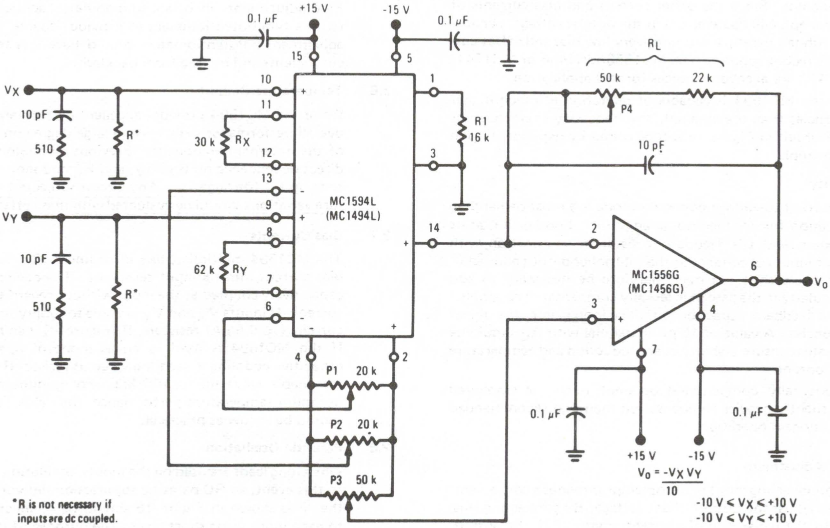
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



*R is not necessary if inputs are dc coupled.

$V_o = \frac{-V_X V_Y}{10}$

$-10\text{ V} \leqslant V_X \leqslant +10\text{ V}$
$-10\text{ V} \leqslant V_Y \leqslant +10\text{ V}$

that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set $K = 1/2$ or $K = 1$ or even $K = 100$. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$R_X \geq 3\ V_X$ (max) in kΩ when V_X is in volts

$R_Y \geq 6\ V_Y$ (max) in kΩ when V_Y is in volts

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of $K = 10$ is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
  (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
  (b) connect "X" input (pin 10) to ground
  (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
  (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
  (b) connect "Y" input (pin 9) to ground
  (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
  (a) connect both "X" and "Y" inputs to ground
  (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D. Scale Factor
  (a) apply +10 Vdc to both the "X" and "Y" inputs
  (b) adjust P4 to achieve −10.00 V at the output
  (c) apply −10 Vdc to both "X" and "Y" inputs and check for $V_O = -10.00$ V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current ($\approx 0.5\ \mu A$) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

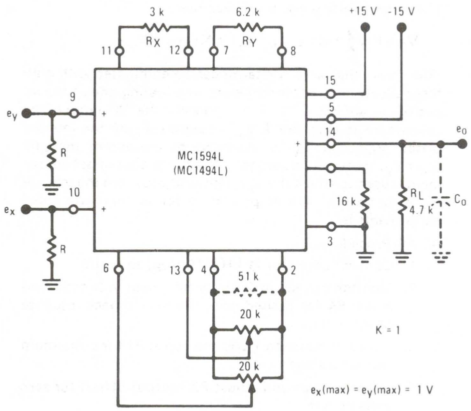
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17 shows a typical ac multiplier circuit with a scale factor K≈1. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

FIGURE 17 – WIDEBAND MULTIPLIER



The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 µA and 35 µA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \quad \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50\ \text{V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \measuredangle 0^{o}$$

and the "Y" input is described as

$$Y = B \measuredangle 0^{o}$$

then the output product would be expected to be

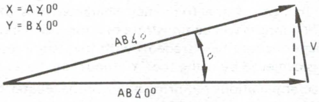
$$V_o = AB \measuredangle 0^{o} \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})\,(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

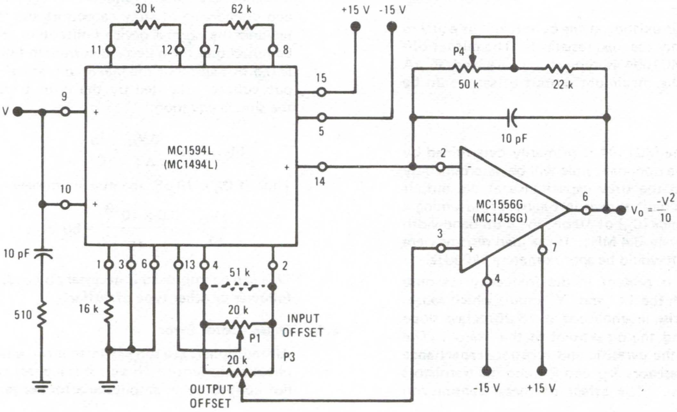
$$V_o = K\,V_x^2 + KV_x\,(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is −0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is −10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$V Repeat steps 1 through 4 as necessary.

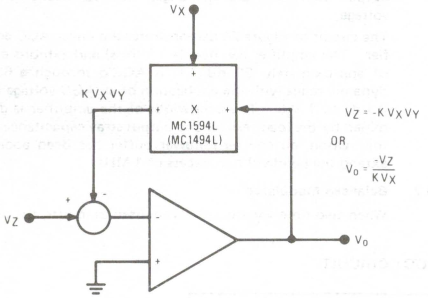
4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable.

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER



Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily − 10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_o is −10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

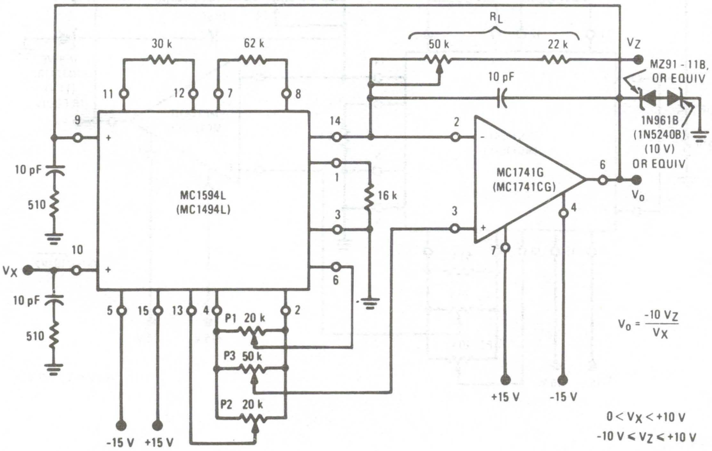
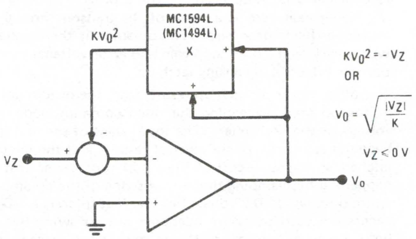


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = −0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to −0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to −10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

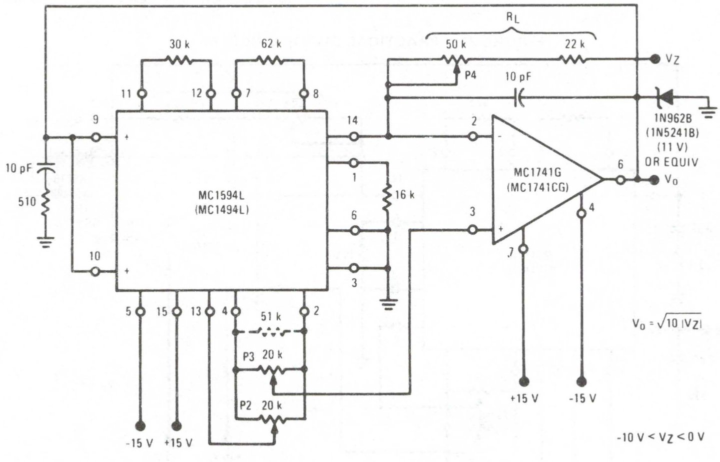
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

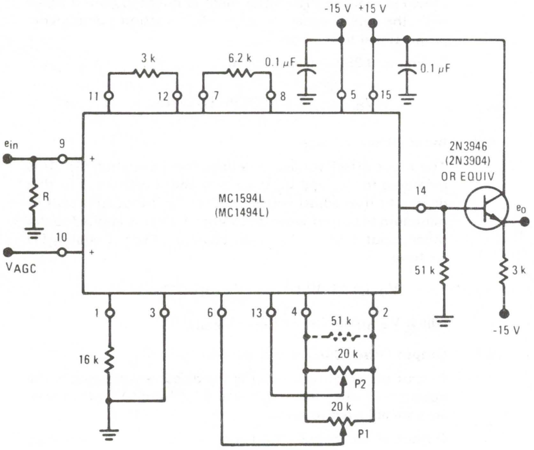
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements in a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

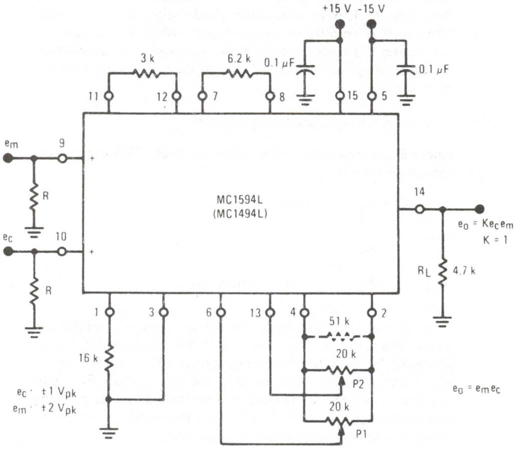


Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2 \cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modulation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\ (E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\ [1 + M \cos\omega_c t]\ \cos\omega_c t$$

where $E_o = EE_c$

and $M = \dfrac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or

$$e_o = \frac{E_c E_m}{2}\ [\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

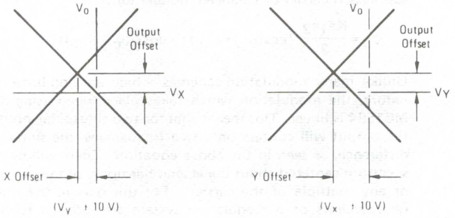
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\ (V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\ (10 \text{ volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\ (0 \pm V_{iox} - V_{x\,off})\ (\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \quad \text{where } R_x \text{ and } R_y >> \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by readjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm [K \pm K\ (TCK)\ (\Delta T)\ ]\ [\ (TCV_{iox})\ (\Delta T)\ ]\ [\ (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{OO})\ (\Delta T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at T_A = +25°C. Assuming initial offset voltages have been adjusted to zero at T_A = +25°C, then:

$$V_O = [K \pm K\ (TCK)\ (\Delta T)\ ]\ [10 \pm (TCV_{iox})\ (\Delta T)\ ]\ [10 \pm (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{OO})\ (\Delta T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note-output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op-ampl. selected.

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MC1495L
MC1595L

ORDERING INFORMATION

Device	Temperature Range	Package
MC1495L	0°C to +70°C	Ceramic DIP
MC1595L	−55°C to +125°C	Ceramic DIP

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

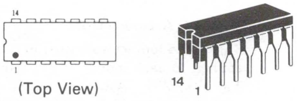
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632-02
MO-001AA

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

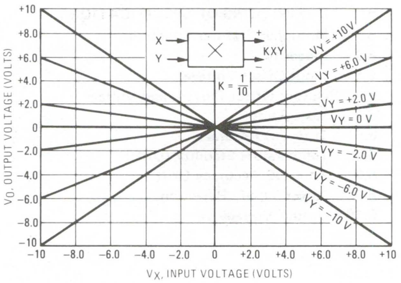


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

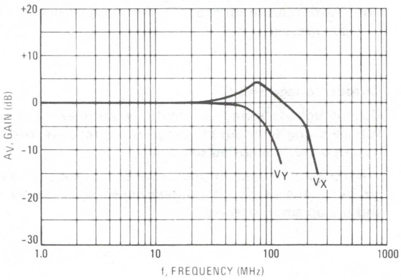
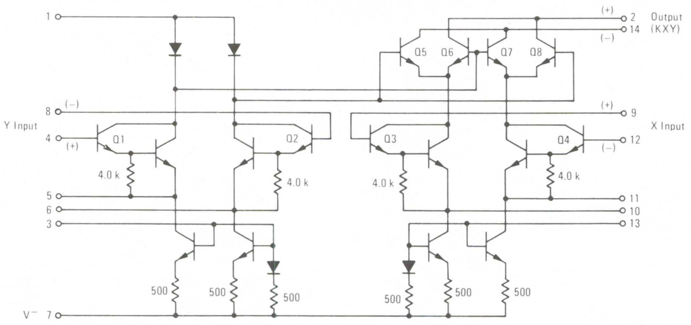


FIGURE 3 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V^+ = +32V, V^- = −15 V, T_A = +25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ unless otherwise noted)

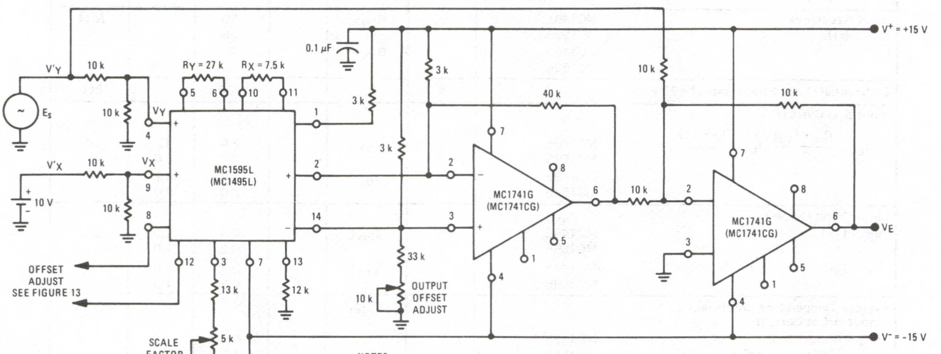
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity:							
Output Error in Percent of Full Scale:		5					%
T_A = +25°C							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	–	±1.0	±2.0	
	MC1595			–	±0.5	±1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	–	±2.0	±4.0	
	MC1595			–	±1.0	±2.0	
T_A = 0 to +70°C	MC1495						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	±1.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	±3.0	–	
T_A = −55°C to +125°C	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	±0.75	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	±1.50	–	
Squaring Mode Error:							
Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
T_A = +25°C	MC1495			–	±0.75	–	
	MC1595			–	±0.5	–	
T_A = 0 to +70°C	MC1495			–	±1.0	–	
T_A = −55°C to +125°C	MC1595			–	±0.75	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		–	K	–	0.1	–	–
Input Resistance	MC1495	7	R_{INX}	–	20	–	MΩ
(f = 20 Hz)	MC1595			–	35	–	
	MC1495		R_{INY}	–	20	–	
	MC1595			–	35	–	
Differential Output Resistance (f = 20 Hz)		8	R_o	–	300	–	kΩ
Input Bias Current							
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}	–	2.0	12	μA
	MC1595			–	2.0	8.0	
	MC1495		I_{by}	–	2.0	12	
	MC1595			–	2.0	8.0	
Input Offset Current							
$\lvert I_9 - I_{12} \rvert$	MC1495	6	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MC1495		$\lvert I_{ioy} \rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	2.5	–	
(T_A = −55°C to +125°C)	MC1595			–	2.5	–	
Output Offset Current		6	$\lvert I_{oo} \rvert$				μA
$\lvert I_{14} - I_2 \rvert$	MC1495			–	20	100	
	MC1595			–	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo} \rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	20	–	
(T_A = −55°C to +125°C)	MC1595			–	20	–	
Frequency Response							
3.0 dB Bandwidth, R_L = 11 kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)			$T_{BW3\,dB}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing		11	CMV				Vdc
(Either Input)	MC1495			±10.5	±12	–	
	MC1595			±11.5	±13	–	
Common Mode Gain		11	A_{CM}				dB
(Either Input)	MC1495			-40	-50	–	
	MC1595			-50	-60	–	
Common Mode Quiescent Output Voltage		12	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		9	V_o	–	±14	–	V_{peak}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current		12	I_7	–	6.0	7.0	mA
DC Power Dissipation		12	P_D	–	135	170	mW

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	ΔV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	750 5.0	mW mW/°C
Operating Temperature Range	T_A		°C
MC1495		0 to +70	°C
MC1595		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

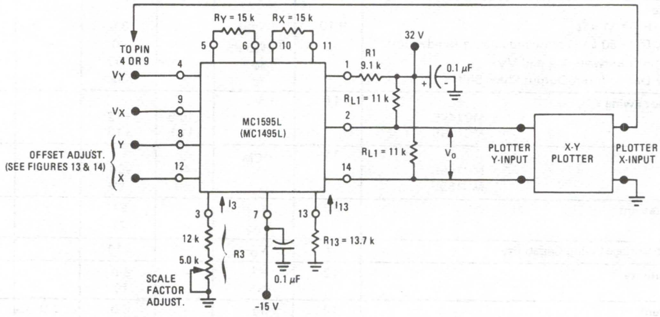
TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)


V'Y
10 k
RY = 27 k
RX = 7.5 k
5
6
10
11
Es
10 k
VY
4
0.1 µF
3 k
1
MC1595L
(MC1495L)
V'X
10 k
VX
9
10 V
10 k
8
2
14
3 k
3 k
33 k
2
3
MC1741G
(MC1741CG)
7
8
6
5
4
1
40 k
10 k
10 k
10 k
7
2
8
MC1741G
(MC1741CG)
3
6
5
1
4
VE
V+ = +15 V
V- = -15 V
12
3
7
13
13 k
12 k
OFFSET ADJUST SEE FIGURE 13
5 k
SCALE FACTOR ADJUST
0.1 µF
10 k
OUTPUT OFFSET ADJUST

NOTES:
Adjust "Scale Factor Adjust" for a null in V_E.
This schematic for illustrative purposes only – not specified for test conditions.

FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)


RY = 15 k
RX = 15 k
5
6
10
11
TO PIN 4 OR 9
VY
4
VX
9
8
12
OFFSET ADJUST. (SEE FIGURES 13 & 14)
Y
X
MC1595L
(MC1495L)
1
R1
9.1 k
32 V
0.1 µF
RL1 = 11 k
2
RL1 = 11 k
Vo
14
PLOTTER Y-INPUT
X-Y PLOTTER
PLOTTER X-INPUT
3
I3
7
13
I13
12 k
5.0 k
R3
R13 = 13.7 k
SCALE FACTOR ADJUST.
0.1 µF
-15 V

TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

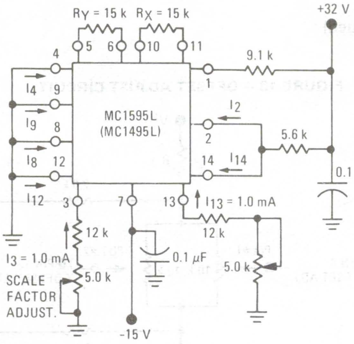

R_Y = 15 k R_X = 15 k
+32 V
4
5
6
10
11
9.1 k
1
I_4 9
I_2
I_9 8
2
5.6 k
MC1595L
(MC1495L)
I_8 12
14
I_{14}
0.1 µF
I_{12} 3
7
13
I_{13} = 1.0 mA
12 k
12 k
I_3 = 1.0 mA
0.1 µF
5.0 k
SCALE FACTOR ADJUST.
5.0 k
-15 V

FIGURE 7 – INPUT RESISTANCE

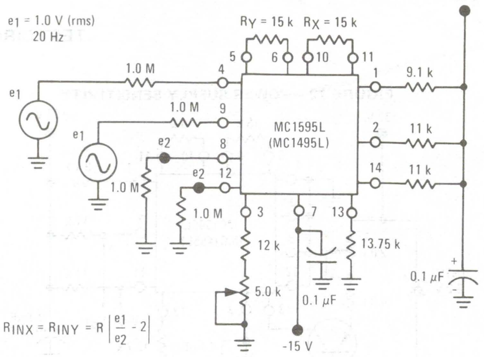

+32 V
e_1 = 1.0 V (rms)
20 Hz
R_Y = 15 k R_X = 15 k
5
6
10
11
1.0 M
4
1
9.1 k
e_1
1.0 M
9
MC1595L
(MC1495L)
e_1
e_2
8
2
11 k
e_2
12
14
11 k
1.0 M
1.0 M
3
7
13
12 k
13.75 k
5.0 k
0.1 µF
0.1 µF
$R_{INX} = R_{INY} = R \left| \frac{e_1}{e_2} - 2 \right|$
-15 V

FIGURE 8 – OUTPUT RESISTANCE

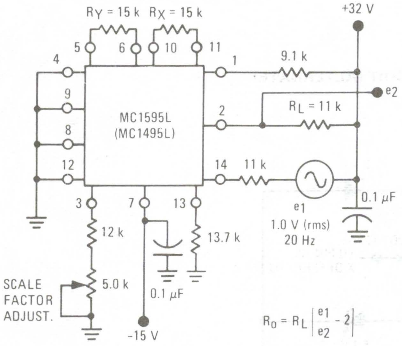

R_Y = 15 k R_X = 15 k
+32 V
5
6
10
11
4
1
9.1 k
9
e_2
R_L = 11 k
MC1595L
(MC1495L)
2
8
12
14
11 k
3
7
13
0.1 µF
e_1
1.0 V (rms)
20 Hz
12 k
13.7 k
SCALE FACTOR ADJUST.
5.0 k
0.1 µF
-15 V
$R_o = R_L \left| \frac{e_1}{e_2} - 2 \right|$

FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

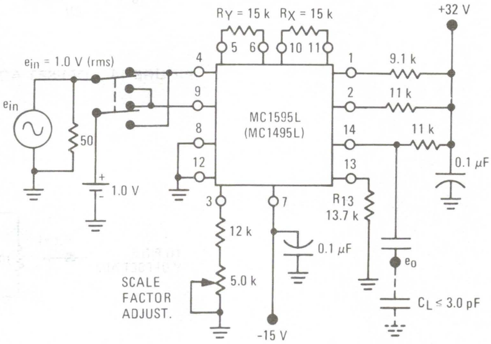

R_Y = 15 k R_X = 15 k
+32 V
5
6
10
11
e_{in} = 1.0 V (rms)
4
1
9.1 k
e_{in}
9
2
11 k
MC1595L
(MC1495L)
8
14
11 k
50
12
13
0.1 µF
1.0 V
3
7
R_{13}
13.7 k
12 k
0.1 µF
e_o
SCALE FACTOR ADJUST.
5.0 k
C_L ≤ 3.0 pF
-15 V

FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

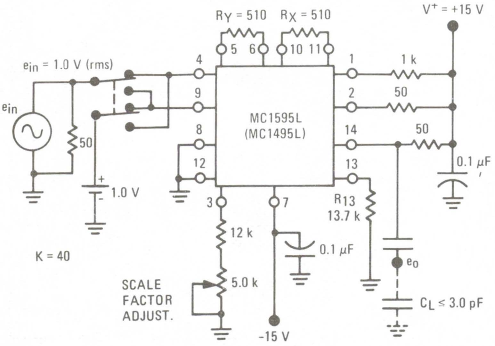
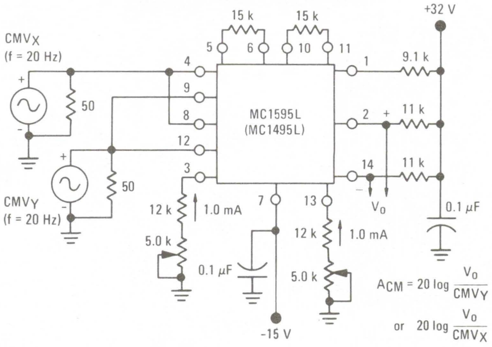
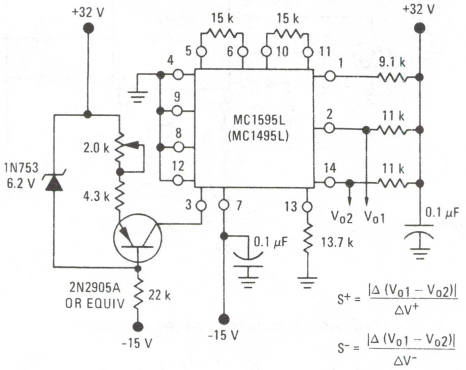

R_Y = 510 R_X = 510
V^+ = +15 V
5
6
10
11
e_{in} = 1.0 V (rms)
4
1
1 k
e_{in}
9
2
50
MC1595L
(MC1495L)
8
14
50
50
12
13
0.1 µF
1.0 V
3
7
R_{13}
13.7 k
K = 40
12 k
0.1 µF
e_o
SCALE FACTOR ADJUST.
5.0 k
C_L ≤ 3.0 pF
-15 V

FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING


15 k
15 k
+32 V
CMV_X
(f = 20 Hz)
5
6
10
11
4
1
9.1 k
50
9
8
MC1595L
(MC1495L)
2
11 k
12
50
3
14
11 k
CMV_Y
(f = 20 Hz)
12 k
1.0 mA
7
13
V_o
0.1 µF
5.0 k
12 k
1.0 mA
0.1 µF
5.0 k
$A_{CM} = 20 \log \frac{V_o}{CMV_Y}$
or $20 \log \frac{V_o}{CMV_X}$
-15 V

TEST CIRCUITS (continued)

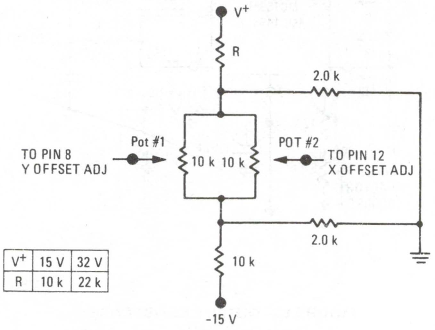
FIGURE 12 – POWER SUPPLY SENSITIVITY


+32 V
15 k
15 k
+32 V
4
5
6
10
11
1
9.1 k
9
8
12
MC1595L
(MC1495L)
2
11 k
14
11 k
2.0 k
1N753
6.2 V
4.3 k
3
7
13
V_{o2}
V_{o1}
0.1 μF
0.1 μF
13.7 k
2N2905A
OR EQUIV
22 k
-15 V
-15 V

$$S^+ = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^+}$$

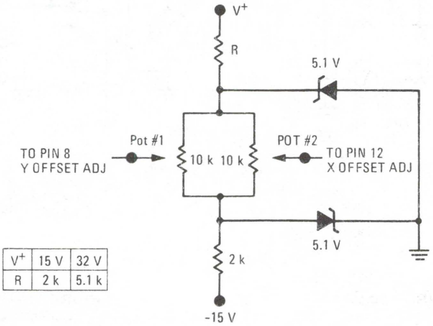
$$S^- = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^-}$$

FIGURE 13 – OFFSET ADJUST CIRCUIT


V+
R
2.0 k
TO PIN 8
Y OFFSET ADJ
Pot #1
10 k
10 k
POT #2
TO PIN 12
X OFFSET ADJ
2.0 k
10 k
-15 V

V^+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)


V+
R
5.1 V
TO PIN 8
Y OFFSET ADJ
Pot #1
10 k
10 k
POT #2
TO PIN 12
X OFFSET ADJ
5.1 V
2 k
-15 V

V^+	15 V	32 V
R	2 k	5.1 k

TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

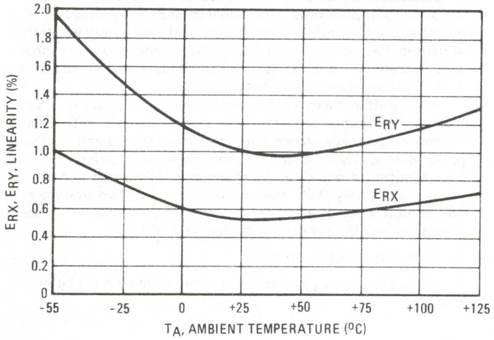


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

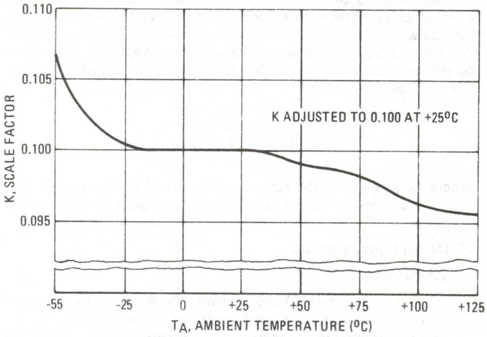


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

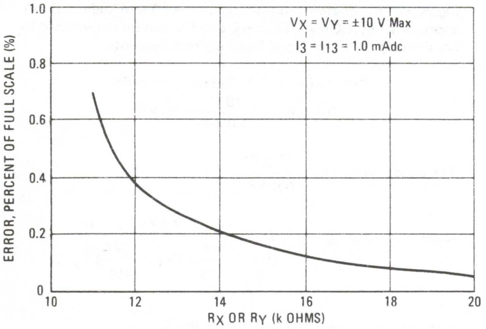


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

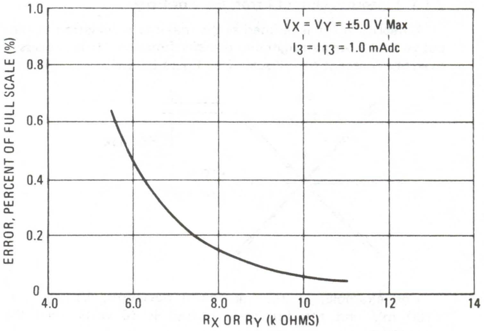
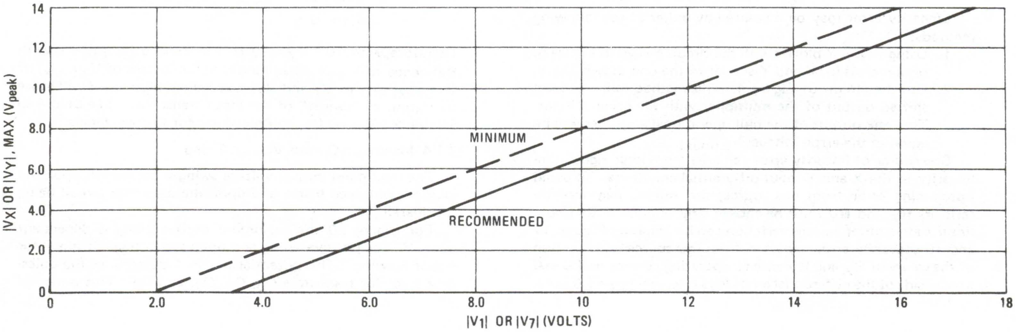


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

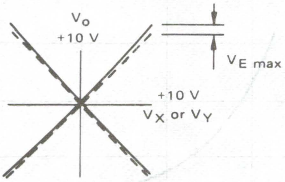
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ \text{V}}{1.0\ \text{mA}} = 10\ \text{k}\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{\left(R_X + \dfrac{2kT}{qI_{13}}\right)\left(R_Y + \dfrac{2kT}{qI_3}\right) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25°\text{C}$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10$ kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

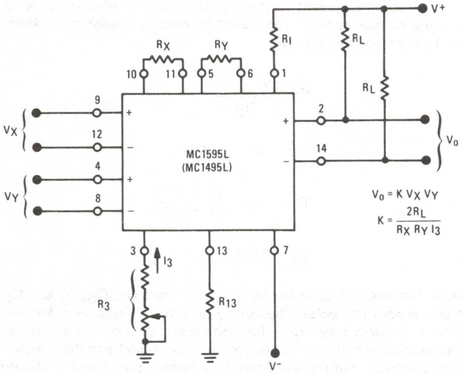
The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER


V+
R_X
R_Y
R_l
R_L
10
11
5
6
1
R_L
9
2
+
V_X
12
–
MC1595L
(MC1495L)
14
V_o
4
8
V_Y
$V_o = K V_X V_Y$
$K = \frac{2R_L}{R_X R_Y I_3}$
3
I_3
13
7
R_3
R_{13}
V-

If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y[max]}$) for a ±10-volt input ($V_X' = V_Y'_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' V_Y'}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10 \, V_X V_Y .$$

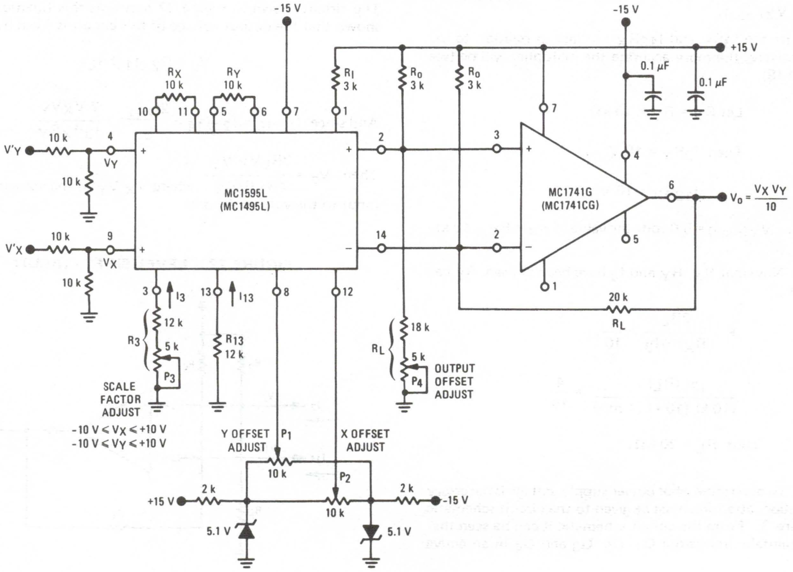
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1 \text{ mA}$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT


-15 V
-15 V
+15 V
R_X 10 k
R_Y 10 k
R_l 3 k
R_o 3 k
R_o 3 k
0.1 µF
0.1 µF
10
11
5
6
7
1
7
V'_Y
10 k
4
V_Y
10 k
+
MC1595L
(MC1495L)
2
3
+
4
MC1741G
(MC1741CG)
6
$V_o = \frac{V_X V_Y}{10}$
V'_X
10 k
9
V_X
10 k
14
2
–
5
1
20 k
R_L
3
I_3
13
I_{13}
8
12
12 k
5 k
R_3
P_3
R_{13} 12 k
18 k
5 k
R_L
P_4
OUTPUT OFFSET ADJUST
SCALE FACTOR ADJUST
$-10 \text{ V} \leq V_X \leq +10 \text{ V}$
$-10 \text{ V} \leq V_Y \leq +10 \text{ V}$
Y OFFSET ADJUST
P_1
X OFFSET ADJUST
10 k
P_2
+15 V
2 k
10 k
2 k
-15 V
5.1 V
5.1 V

OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15\ V$

$$\text{Then } R_{13} + 500 = \frac{14.3\ V}{1\ mA} \text{ or } R_{13} = 13.8\ k\Omega$$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3R_Y \geqslant 1.5\ V_{Y(max)}$ and $I_{13}\ R_X \geqslant 1.5\ V_{X(max)}$.

The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3R_Y = 10\ V$

$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_XR_YI_3} = \frac{4}{10}$$

$$\text{or} \quad \frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10\ V$ or $V_X = 5.0\ V$, $V_Y = 5.0\ V$), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15\ V$

$$\text{Then } R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$$

$$R_1 = 3\ k\Omega.$$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

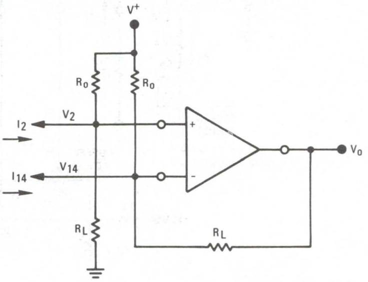
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\ R_L$$

$$\text{And since } I_A - I_B = I_2 - I_{14} = \frac{2I_XI_Y}{I_3} = \frac{2\ V_XV_Y}{I_3R_XR_Y}$$

Then $V_o = \dfrac{2R_LV_X'V_Y'}{4R_XR_XI_3}$ where $V_X'V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 — LEVEL SHIFT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ \text{V}}{20\ \text{k}\Omega} + 1\ \text{mA} = \frac{15\ \text{V} - 11\ \text{V}}{R_o}$

Solving for R_o, $R_o = 2.6\ \text{k}\Omega$

Thus, select $R_o = 3.0\ \text{k}\Omega$

For $R_o = 3.0\ \text{k}\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\ \text{volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

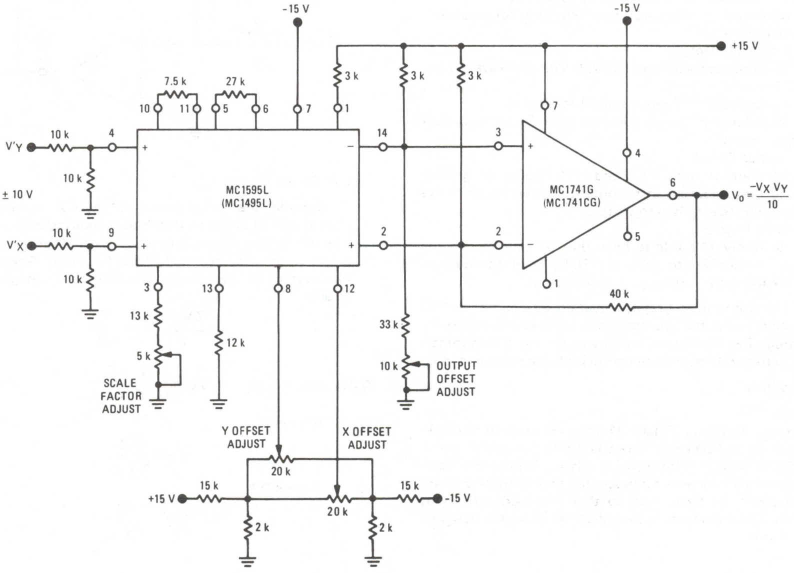
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \qquad (1)$$

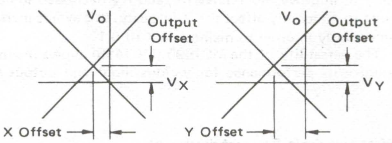
Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

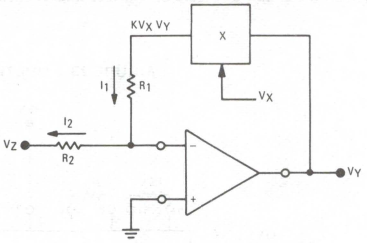
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \qquad (1)$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \qquad (2)$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \qquad (3)$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \qquad (4)$$

OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X}, \tag{5}$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \tag{6}$$

From equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$P.E._D = \frac{\dfrac{\Delta E}{KV_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \tag{7}$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

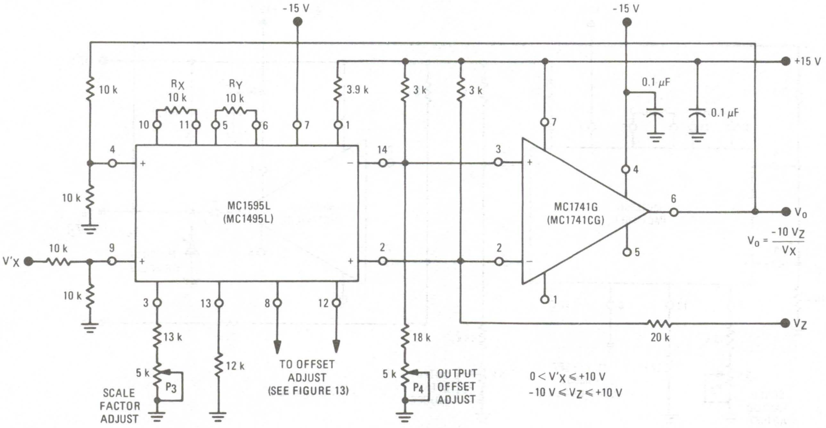
A Suggested Adjustment Procedure for the Divide Circuit

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until $V_o = 0$ volts.
3. Let $V_X' = V_Z$ and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily − 10 volts) constant value as $V_Z = V_X'$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_o is − 10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

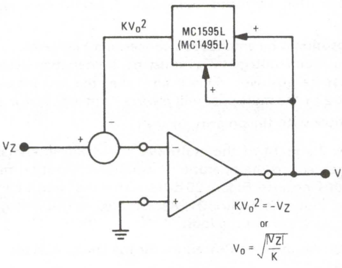
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 – DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



KV_o^2
MC1595L
(MC1495L)
+
+
−
V_Z
+
−
+
V_o
$KV_o^2 = -V_Z$
or
$V_o = \sqrt{\frac{|V_Z|}{K}}$

as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to − 0.01 volts and adjust P_4 (output offset) for V_o = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to − 0.9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to − 10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

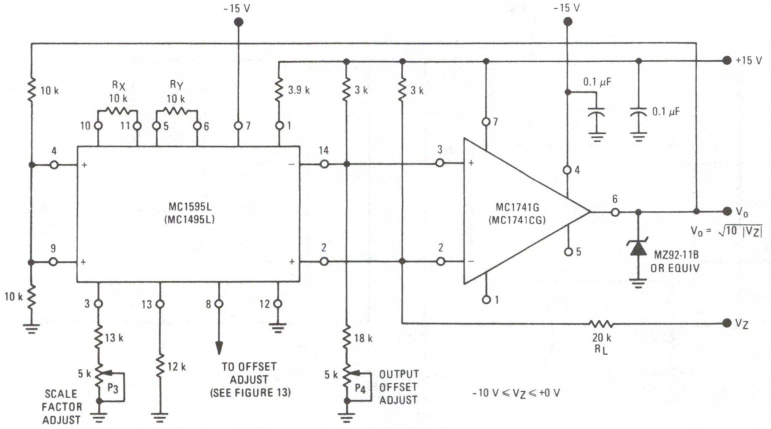
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

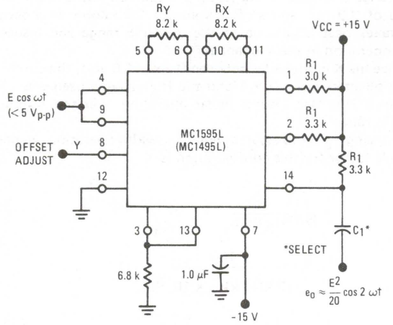
FIGURE 27 – SQUARE ROOT CIRCUIT



-15 V
-15 V
+15 V
10 k
R_X
10 k
R_Y
10 k
3.9 k
3 k
3 k
0.1 µF
0.1 µF
10
11
5
6
7
1
7
4
14
3
4
MC1595L
(MC1495L)
MC1741G
(MC1741CG)
6
V_o
$V_o = \sqrt{10\ |V_Z|}$
9
2
2
5
MZ92-11B
OR EQUIV
1
10 k
3
13
8
12
13 k
12 k
18 k
20 k
R_L
V_Z
5 k
P_3
SCALE
FACTOR
ADJUST
TO OFFSET
ADJUST
(SEE FIGURE 13)
5 k
P_4
OUTPUT
OFFSET
ADJUST
$-10\ V \leqslant V_Z \leqslant +0\ V$

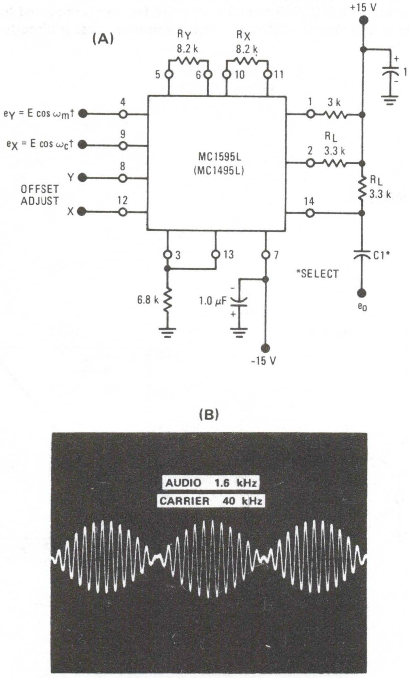
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 – FREQUENCY DOUBLER



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)\,(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}\,[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) (cos $\omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)\,E_c \cos \omega_c t = KE_mE_c\cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

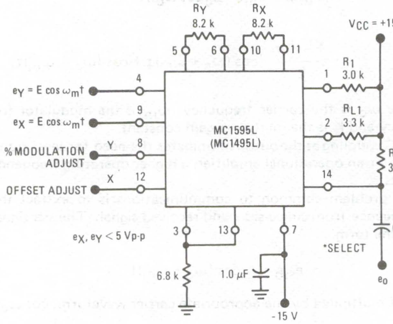
where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

6.4 Linear Gain Control

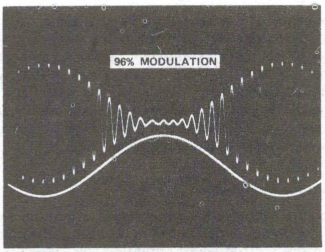
To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 — AMPLITUDE MODULATION


RY
8.2 k
RX
8.2 k
VCC = +15 V
5
6
10
11
R1
3.0 k
1
eY = E cos ωmt
4
9
eX = E cos ωmt
RL1
3.3 k
2
MC1595L
(MC1495L)
% MODULATION ADJUST
Y
8
RL1
3.3 k
X
12
OFFSET ADJUST
14
eX, eY < 5 Vp-p
3
13
7
C1*
*SELECT
6.8 k
1.0 μF
eo
-15 V

(B)


96% MODULATION

The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

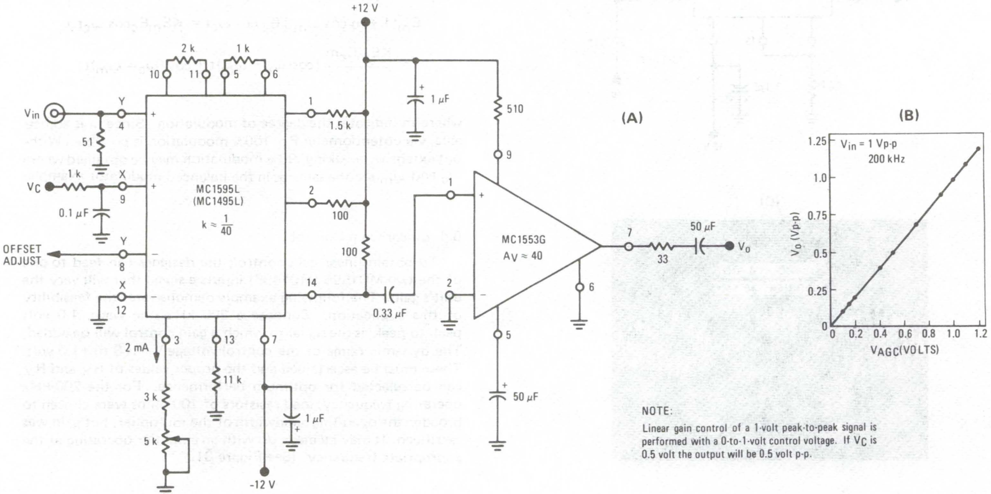
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})}\ \text{V}^{-1}$$

$$= \frac{1}{40}\ \text{V}^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 — LINEAR GAIN CONTROL


+12 V
2 k
1 k
10
11
5
6
1 μF
510
Vin
Y
4
51
1
1.5 k
9
1 k
X
VC
9
MC1595L
(MC1495L)
k ≈ 1/40
2
100
1
0.1 μF
Y
OFFSET ADJUST
8
100
MC1553G
AV ≈ 40
7
50 μF
Vo
33
X
12
14
2
0.33 μF
6
3
13
7
5
2 mA
11 k
3 k
1 μF
50 μF
5 k
-12 V
(A)
(B)
Vin = 1 Vp-p
200 kHz
1.25
1.0
0.75
0.5
0.25
0
0
0.2
0.4
0.6
0.8
1.0
1.2
Vo (Vp-p)
VAGC(VOLTS)

NOTE:
Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1496G	0°C to +70°C	Metal Can
MC1496L	0°C to +70°C	Ceramic DIP
MC1496P	0°C to +70°C	Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L	−55°C to +125°C	Ceramic DIP

Specifications and Applications Information

BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

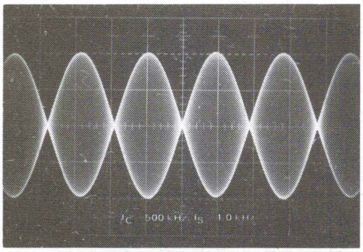


FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

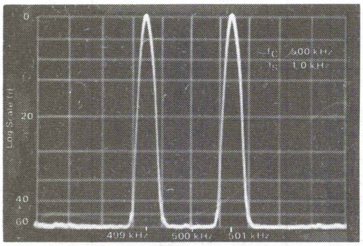


FIGURE 2 – SUPPRESSED-CARRIER SPECTRUM

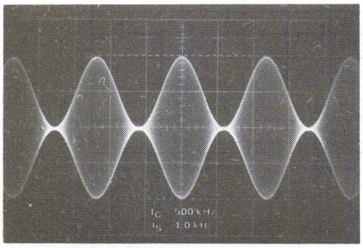
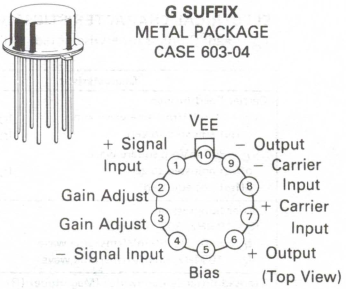


FIGURE 3 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

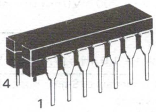
MC1496
MC1596

BALANCED MODULATOR — DEMODULATOR

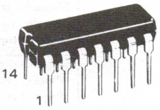
SILICON MONOLITHIC INTEGRATED CIRCUIT


VEE
+ Signal Input
Gain Adjust
Gain Adjust
− Signal Input
Bias
− Output
− Carrier Input
+ Carrier Input
+ Output
(Top View)
1
2
3
4
5
6
7
8
9
10

G SUFFIX
METAL PACKAGE
CASE 603-04



L SUFFIX
CERAMIC PACKAGE
CASE 632-02



P SUFFIX
PLASTIC PACKAGE
CASE 646-05

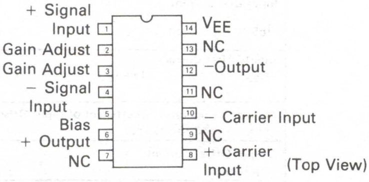
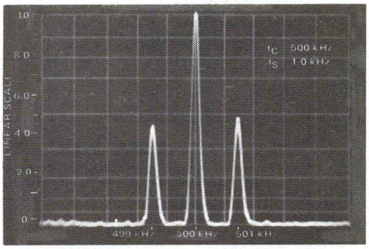

+ Signal Input
Gain Adjust
Gain Adjust
− Signal Input
Bias
+ Output
NC
VEE
NC
−Output
NC
− Carrier Input
NC
+ Carrier Input
(Top View)
1
2
3
4
5
6
7
8
9
10
11
12
13
14

FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5+I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$		°C/W
Ceramic Dual In-Line Package		180	
Plastic Dual In-Line Package		100	
Metal Package		200	
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

				MC1596			MC1496			
Characteristic	Fig	Note	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							µV(rms)
V_C = 60 mV(rms) sine wave and offset adjusted to zero, f_C = 1.0 kHz				–	40	–	–	40	–	
f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero, f_C = 1.0 kHz				–	0.04	0.2	–	0.04	0.4	
offset not adjusted, f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression f_S = 10 kHz, 300 mV(rms)	5	2	V_{CS}							dB
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave f_S = 1.0 kHz, 300 mV(rms) sine wave				–	300	–	–	300	–	
Signal Input Port, V_S = 300 mV(rms) sine wave $\lvert V_C\rvert$ = 0.5 Vdc				–	80	–	–	80	–	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C\rvert$ = 0.5 Vdc	10	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	6	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current $I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$	7	–	I_{bS} I_{bC}	– –	12 12	25 25	– –	12 12	30 30	µA
Input Offset Current $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$	7	–	$\lvert I_{ioS}\rvert$ $\lvert I_{ioC}\rvert$	– –	0.7 0.7	5.0 5.0	– –	0.7 0.7	7.0 7.0	µA
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Iio}\rvert$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	7	–	$\lvert I_{oo}\rvert$	–	14	50	–	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Ioo}\rvert$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C\rvert$ = 0.5 Vdc	9	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_9$			I_{CC}	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_{EE}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

GENERAL OPERATING INFORMATION *

Note 1 — Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Note 2 — Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 — Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Note 4 — Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 — Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\ I_5\ (V_6 - V_{10}) + I_5\ (V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 — Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega$$

where: R_5 is the resistor between pin 5 and ground

ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 — Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 — Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21C} = \left.\frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\right|\ V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21S} = \left.\frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\right|\ V_c = 0.5\text{ Vdc},\ V_o = 0$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

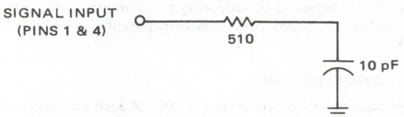
The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Negative Supply, V_{EE}

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Note 12 – Signal Port Stability

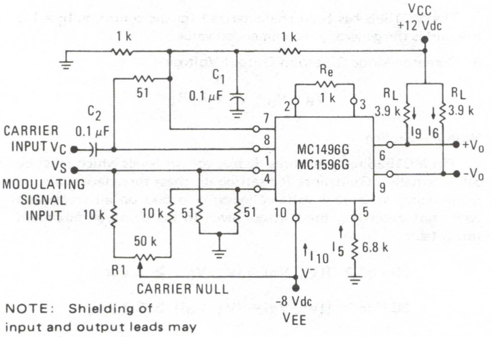
Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.


SIGNAL INPUT
(PINS 1 & 4)
510
10 pF

An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION


VCC
+12 Vdc
1 k
1 k
51
C1
0.1 µF
Re
1 k
RL
3.9 k
RL
3.9 k
I9
I6
C2
0.1 µF
CARRIER INPUT VC
VS
MODULATING SIGNAL INPUT
10 k
10 k
51
51
50 k
R1
CARRIER NULL
MC1496G
MC1596G
2
3
7
8
1
4
6
9
10
5
+Vo
-Vo
I10
I5
6.8 k
V-
-8 Vdc
VEE

NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 6 – INPUT-OUTPUT IMPEDANCE

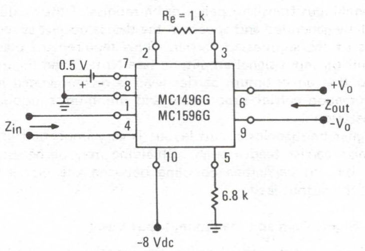

Re = 1 k
2
3
0.5 V
7
8
1
4
Zin
MC1496G
MC1596G
6
9
+Vo
Zout
-Vo
10
5
6.8 k
-8 Vdc

FIGURE 7 – BIAS AND OFFSET CURRENTS

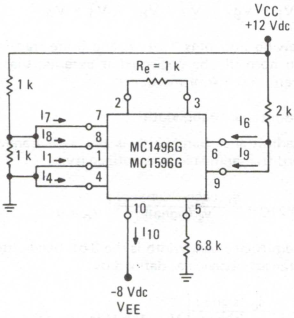
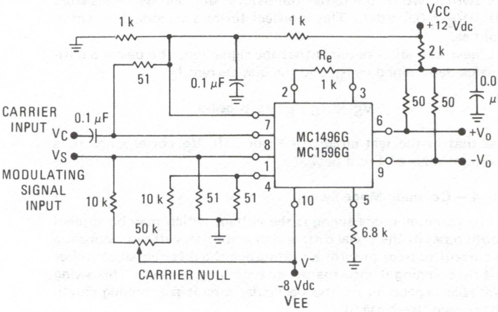

VCC
+12 Vdc
1 k
Re = 1 k
2
3
2 k
I7
I8
I1
I4
1 k
7
8
1
4
MC1496G
MC1596G
I6
6
I9
9
10
5
I10
6.8 k
-8 Vdc
VEE

FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH


VCC
+12 Vdc
1 k
1 k
2 k
51
0.1 µF
Re
1 k
2
3
50
50
0.01 µF
CARRIER INPUT
0.1 µF
VC
VS
MODULATING SIGNAL INPUT
10 k
10 k
51
51
50 k
CARRIER NULL
7
8
1
4
MC1496G
MC1596G
6
9
10
5
+Vo
-Vo
6.8 k
V-
-8 Vdc
VEE

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TEST CIRCUITS (continued)

FIGURE 9 – COMMON-MODE GAIN

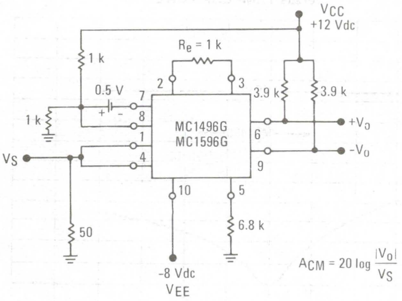
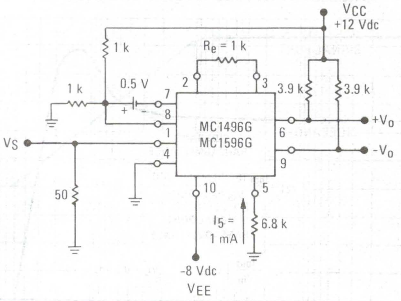

VCC
+12 Vdc
1 k
Re = 1 k
2
3
0.5 V
7
3.9 k
3.9 k
1 k
8
MC1496G
MC1596G
6
+Vo
1
-Vo
VS
4
9
10
5
50
6.8 k
-8 Vdc
VEE
ACM = 20 log |Vo| / VS

FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING


VCC
+12 Vdc
1 k
Re = 1 k
2
3
1 k
0.5 V
7
3.9 k
3.9 k
8
+Vo
MC1496G
MC1596G
VS
1
6
-Vo
4
9
10
5
50
I5 = 1 mA
6.8 k
-8 Vdc
VEE

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave), $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^{\circ}C$ unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

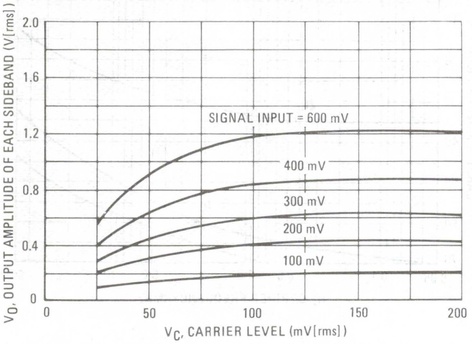


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

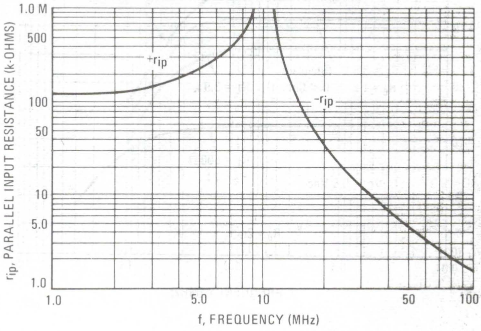


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

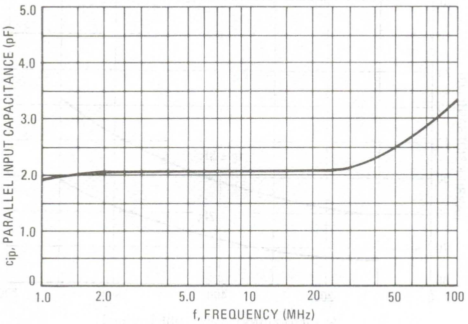
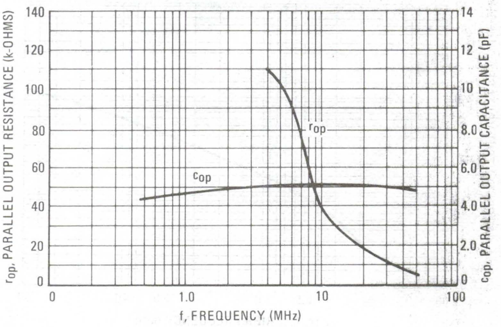


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

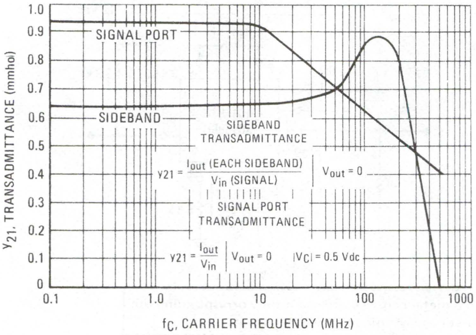


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

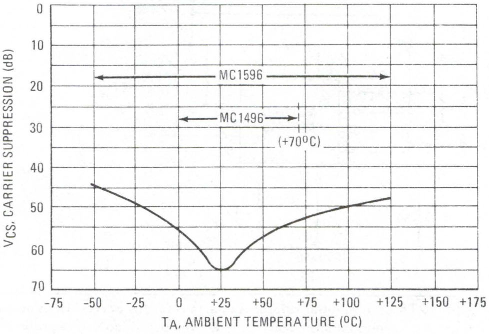


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

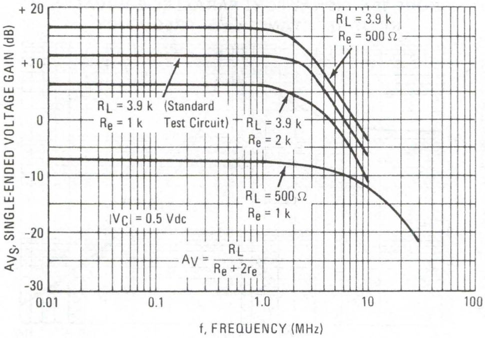


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

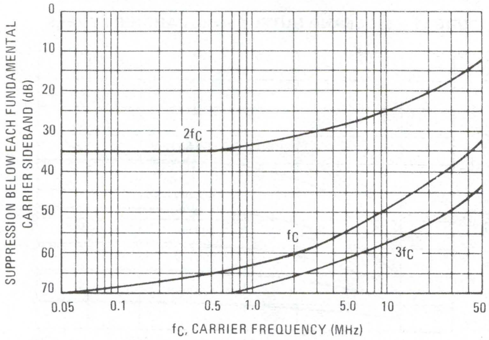


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

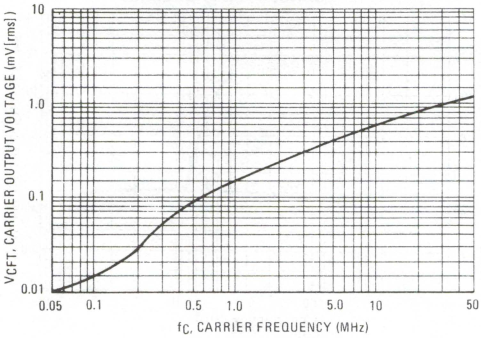
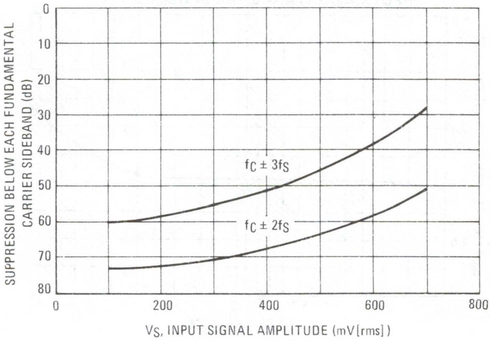


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

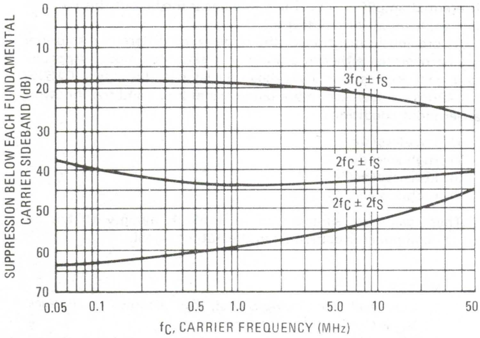
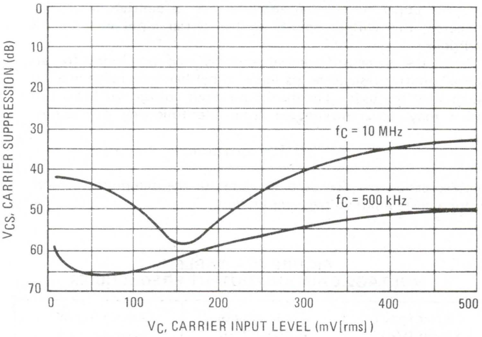


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 23 – CIRCUIT SCHEMATIC

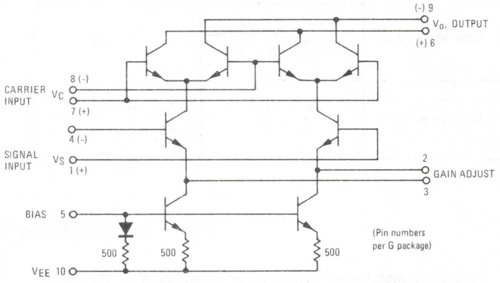
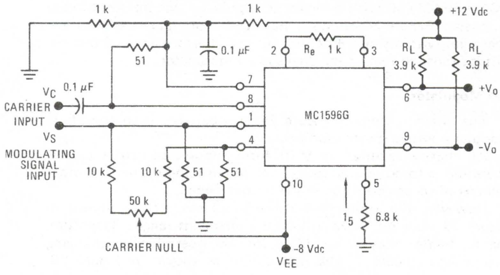

(-) 9
Vo, OUTPUT
(+) 6
8 (-)
CARRIER INPUT
VC
7 (+)
4 (-)
SIGNAL INPUT
VS
1 (+)
2
GAIN ADJUST
3
BIAS 5
500
500
500
VEE 10
(Pin numbers per G package)

FIGURE 24 – TYPICAL MODULATOR CIRCUIT


1 k
1 k
+12 Vdc
51
0.1 µF
2
Re 1 k
3
RL 3.9 k
RL 3.9 k
VC 0.1 µF
CARRIER INPUT
7
8
1
4
MC1596G
6
+Vo
VS
MODULATING SIGNAL INPUT
9
-Vo
10 k
10 k
51
51
10
5
50 k
I5
6.8 k
CARRIER NULL
-8 Vdc
VEE

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)\,(R_E)\ \text{volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\dfrac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\dfrac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\dfrac{R_L V_C(\text{rms})}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\dfrac{0.637\,R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:

1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26\ \text{mV}}{I_5\ (\text{mA})}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ \text{mV at room temperature}$$

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 µF capacitors on pins 7 and 8 should be increased to 1.0 µF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

APPLICATIONS INFORMATION (continued)

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

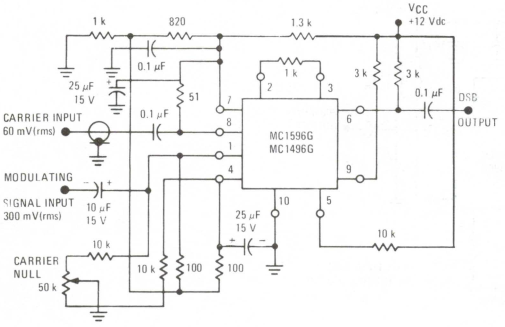

1 k
820
1.3 k
VCC
+12 Vdc
0.1 µF
25 µF
15 V
51
1 k
3 k
3 k
0.1 µF
DSB
OUTPUT
CARRIER INPUT
60 mV(rms)
0.1 µF
MC1596G
MC1496G
MODULATING
SIGNAL INPUT
300 mV(rms)
10 µF
15 V
25 µF
15 V
10 k
CARRIER
NULL
50 k
10 k
100
100
10 k
2
3
7
8
1
4
6
9
10
5

FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

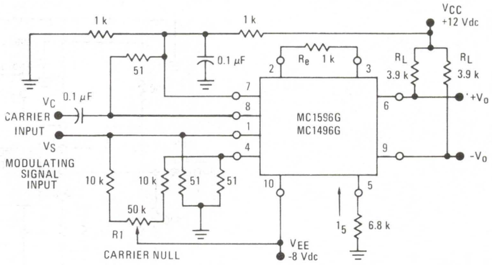

1 k
1 k
VCC
+12 Vdc
0.1 µF
51
Re 1 k
RL
3.9 k
RL
3.9 k
VC 0.1 µF
CARRIER
INPUT
VS
MODULATING
SIGNAL
INPUT
MC1596G
MC1496G
+Vo
-Vo
10 k
10 k
51
51
50 k
R1
CARRIER NULL
VEE
-8 Vdc
I5
6.8 k
2
3
7
8
1
4
6
9
10
5

FIGURE 28 – AM MODULATOR CIRCUIT

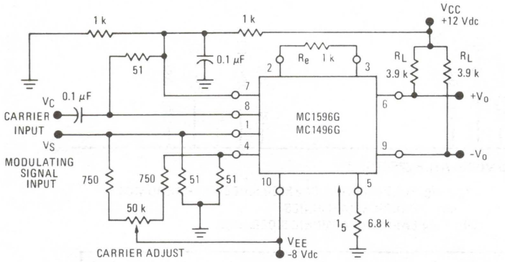
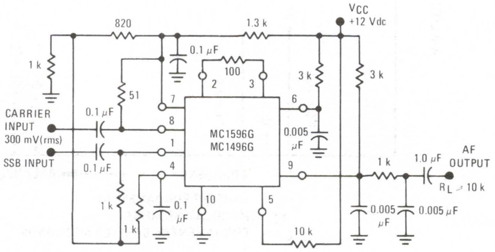
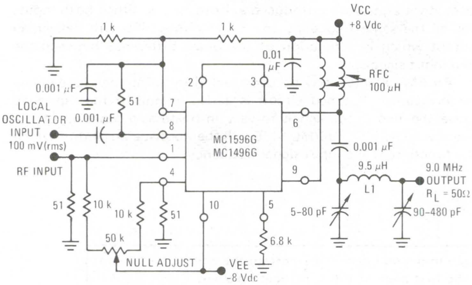

1 k
1 k
VCC
+12 Vdc
51
0.1 µF
Re 1 k
RL
3.9 k
RL
3.9 k
VC 0.1 µF
CARRIER
INPUT
VS
MODULATING
SIGNAL
INPUT
MC1596G
MC1496G
+Vo
-Vo
750
750
51
51
50 k
CARRIER ADJUST
VEE
-8 Vdc
I5
6.8 k
2
3
7
8
1
4
6
9
10
5

FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)


820
1.3 k
VCC
+12 Vdc
1 k
0.1 µF
100
3 k
3 k
51
CARRIER
INPUT
300 mV(rms)
SSB INPUT
0.1 µF
0.1 µF
MC1596G
MC1496G
0.005
µF
1 k
1.0 µF
AF
OUTPUT
RL 10 k
1 k
1 k
0.1
µF
10 k
0.005
µF
0.005 µF
2
3
7
8
1
4
6
9
10
5

TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)


VCC
+8 Vdc
1 k
1 k
0.01 μF
RFC
100 μH
0.001 μF
51
LOCAL OSCILLATOR INPUT
100 mV(rms)
0.001 μF
RF INPUT
2
3
7
8
1
4
6
9
10
5
MC1596G
MC1496G
0.001 μF
9.5 μH
L1
9.0 MHz
OUTPUT
RL = 50Ω
5–80 pF
90–480 pF
51
10 k
10 k
51
50 k
6.8 k
NULL ADJUST
VEE
-8 Vdc

L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

FIGURE 31 – LOW-FREQUENCY DOUBLER

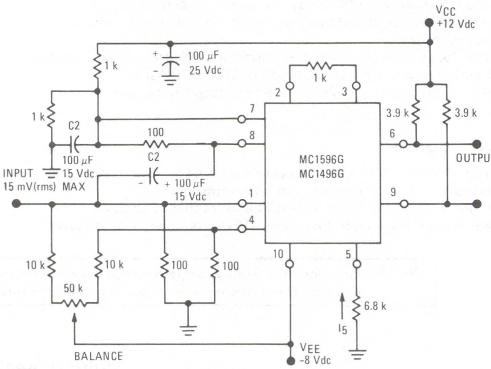
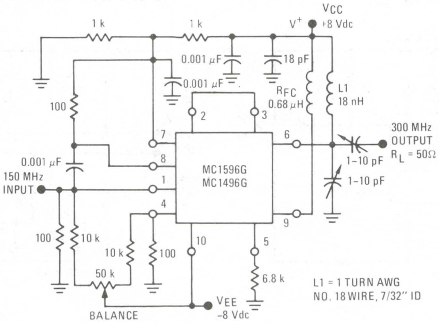
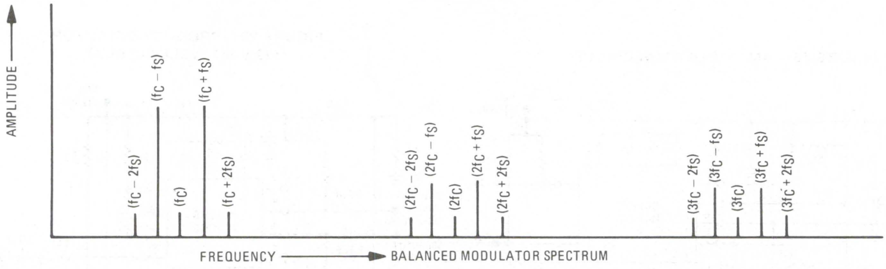

VCC
+12 Vdc
1 k
100 μF
25 Vdc
1 k
2
3
3.9 k
3.9 k
1 k
C2
100 μF
15 Vdc
100
C2
100 μF
15 Vdc
INPUT
15 mV(rms) MAX
7
8
1
4
6
9
10
5
MC1596G
MC1496G
OUTPUT
10 k
10 k
100
100
50 k
6.8 k
I5
BALANCE
VEE
-8 Vdc

FIGURE 32 – 150 to 300 MHz DOUBLER


VCC
V+
+8 Vdc
1 k
1 k
0.001 μF
18 pF
0.001 μF
RFC
0.68 μH
L1
18 nH
100
2
3
300 MHz
OUTPUT
RL = 50Ω
7
6
1–10 pF
1–10 pF
0.001 μF
150 MHz
INPUT
8
1
4
9
10
5
MC1596G
MC1496G
100
10 k
10 k
100
50 k
6.8 k
BALANCE
VEE
-8 Vdc

L1 = 1 TURN AWG NO. 18 WIRE, 7/32″ ID

DEFINITIONS



BALANCED MODULATOR SPECTRUM

f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3344L	−40°C to +85°C	Ceramic DIP
MC3344P	−40°C to +85°C	Plastic DIP

MC3344

Advance Information

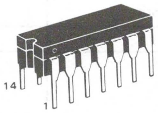
PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor (R_R) and capacitor (C_R). Hysteresis is adjustable and determined by an external resistor (R_H).

- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

PROGRAMMABLE FREQUENCY SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA

P SUFFIX
PLASTIC PACKAGE
CASE 646-05

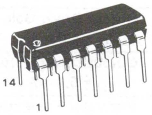
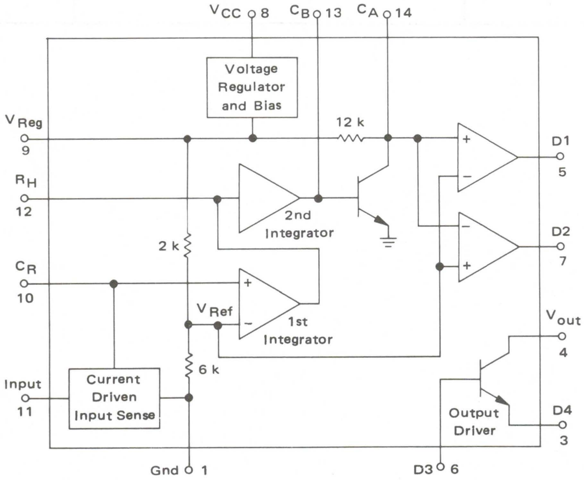
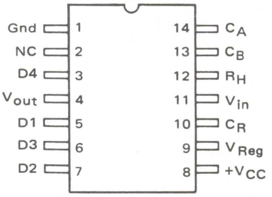


FIGURE 1 — CIRCUIT BLOCK DIAGRAM


VCC 8
CB 13
CA 14
Voltage Regulator and Bias
VReg 9
12 k
D1 5
RH 12
2nd Integrator
D2 7
2 k
CR 10
VRef
1st Integrator
Vout 4
6 k
Input 11
Current Driven Input Sense
Output Driver
D4 3
Gnd 1
D3 6

PIN CONNECTIONS


Gnd 1
NC 2
D4 3
Vout 4
D1 5
D3 6
D2 7
14 CA
13 CB
12 RH
11 Vin
10 CR
9 VReg
8 +VCC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	24	Vdc
Peak Input Current	I_I	10	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +15 Vdc unless otherwise specified)

Characteristic	Test Ckts	Symbol	Min	Typ	Max	Unit
Supply Current	2	I_D	–	2.5	4.0	mA
Trigger Reset Voltage I_{in} = 200 μA I_{in} = 600 μA	3	 V_{CR1} V_{CR2}	 0.25 –	 – –	 – 0.25	Vdc
Regulator Output Voltage	4	V_{Reg}	4.0	4.5	5.0	Vdc
Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$	5	V_{TCR}	0.739	0.750	0.761	V/V
Hysteresis Sink Current	6	I_H	100	400	–	μA
Second Comparator Output D1 Leakage D2 Source D1 Source D2 Leakage	7	 I_{D1L} I_{D2S} I_{D1S} I_{D2L}	 – 100 100 –	 – 250 200 –	 100 – – 100	 nA μA μA nA
Output Driver Gain I_C = 5.0 mA	8	h_{FE1}	50	100	–	–
Output Driver Voltage Standoff I_D = 5.0 mA	9	$V_{(BR)CEO}$	25	30	–	Vdc
Integrator Transistor Gain $h_{FE2} = \Delta I_C/\Delta I_B$, I_{C1} = 0.4 mA, I_{C2} = 0.6 mA	10	h_{FE2}	50	200	300	–

TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

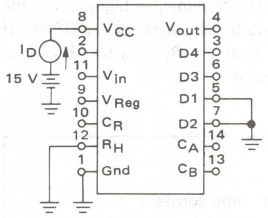
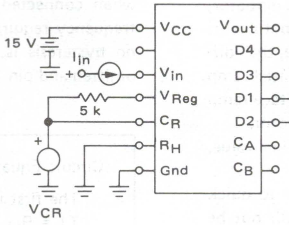

8
V_{CC}
V_{out}
4
I_D
2
D4
3
11
6
15 V
V_{in}
D3
5
9
V_{Reg}
D1
7
10
C_R
D2
14
12
R_H
C_A
13
1
Gnd
C_B

FIGURE 3 – TRIGGER RESET VOLTAGE


15 V
I_{in}
+
5 k
+
−
V_{CR}
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

$I_{in} = 200\ \mu A,\ V_{CR} \geqslant 0.25\ V$

$I_{in} = 600\ \mu A,\ V_{CR} \leqslant 0.25\ V$

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

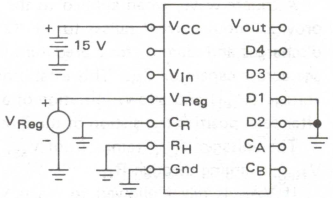
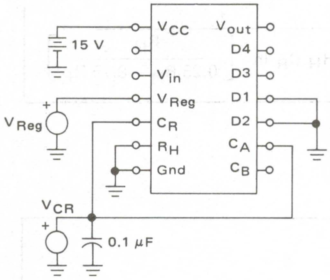

+
15 V
V_{Reg}
+
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

FIGURE 5 – THRESHOLD VOLTAGE RATIO


15 V
+
V_{Reg}
V_{CR}
+
0.1 µF
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

$V_{TCR} = V_{CR}/V_{Reg}$

FIGURE 6 – HYSTERESIS SINK CURRENT

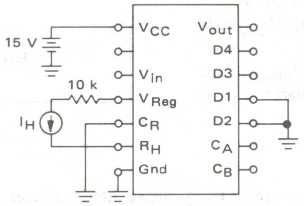
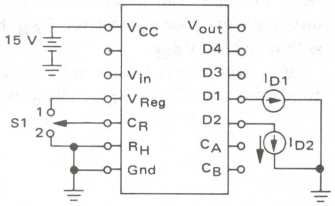

15 V
10 k
I_H
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

FIGURE 7 – I_{D1L}/I_{D2S}, I_{D2L}/I_{D1S}


15 V
S1
1
2
I_{D1}
I_{D2}
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

I_{D1L}/I_{D2S} – S1 in position 1

I_{D2L}/I_{D1S} – S1 in position 2

FIGURE 8 – OUTPUT DRIVER GAIN

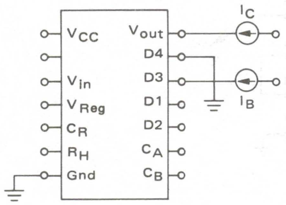

I_C
I_B
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

FIGURE 9 – BV_{CEO} OF OUTPUT TRANSISTOR

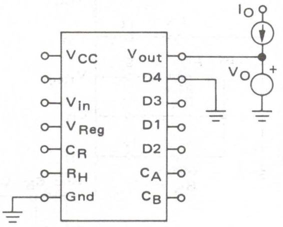
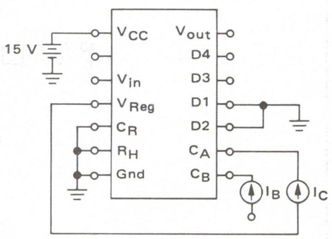

I_O
V_O
+
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

FIGURE 10 – INTEGRATOR TRANSISTOR GAIN


15 V
I_B
I_C
V_{CC}
V_{out}
D4
V_{in}
D3
V_{Reg}
D1
C_R
D2
R_H
C_A
Gnd
C_B

APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor C_R. This establishes the initial ramp voltage (V_{sat}) and allows initiation of a new voltage ramp after each positive transistion of the input waveform.

The voltage, V_{CR}, ramps from V_{sat} to the final value, V_{Reg}, charging through R_R.

If V_{CR} is never allowed to reach V_{Ref} due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor C_{AB} is allowed to charge through the 12 kΩ resistor until V_{CA} is greater than V_{Ref}. At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If V_{CR} is allowed to ramp above V_{Ref} before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor C_{AB} keeping V_{CA} low with respect to V_{Ref}.

V_{CA} will always be low with respect to V_{Ref} if the time from reset C_R to $V_{CR} = V_{Ref}$ is less than the time from reset C_{AB} to $V_{CA} = V_{Ref}$.

Resistor R_H provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the R_H resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is
$T1 = R_H \parallel R_R C_R$. If R_H is omitted then
$T1 = R_R C_R$.

The second integrator time constant is
$T2 = (12\ k)\ (h_{FE2})\ (C_{AB})$.

$$f1 = \text{Switch Point frequency} \cong \frac{1}{1.39\, R_R C_R}$$

$$f2 = \text{Hysteresis Switch Point frequency} \approx \frac{1}{R_R \parallel R_H C_R \ln\left[\dfrac{R_H}{0.25\, R_H - 0.75\, R_R}\right]}$$

FIGURE 11 — TYPICAL APPLICATION

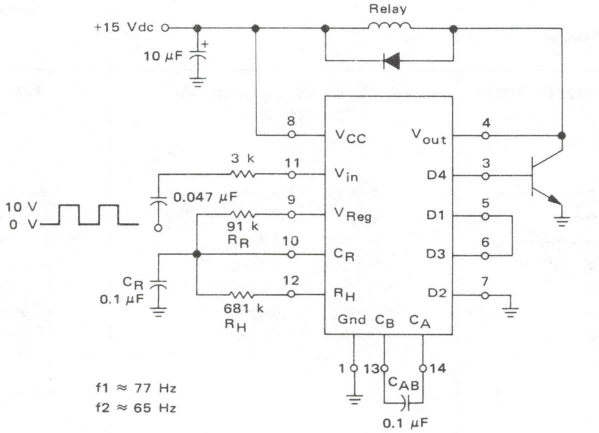
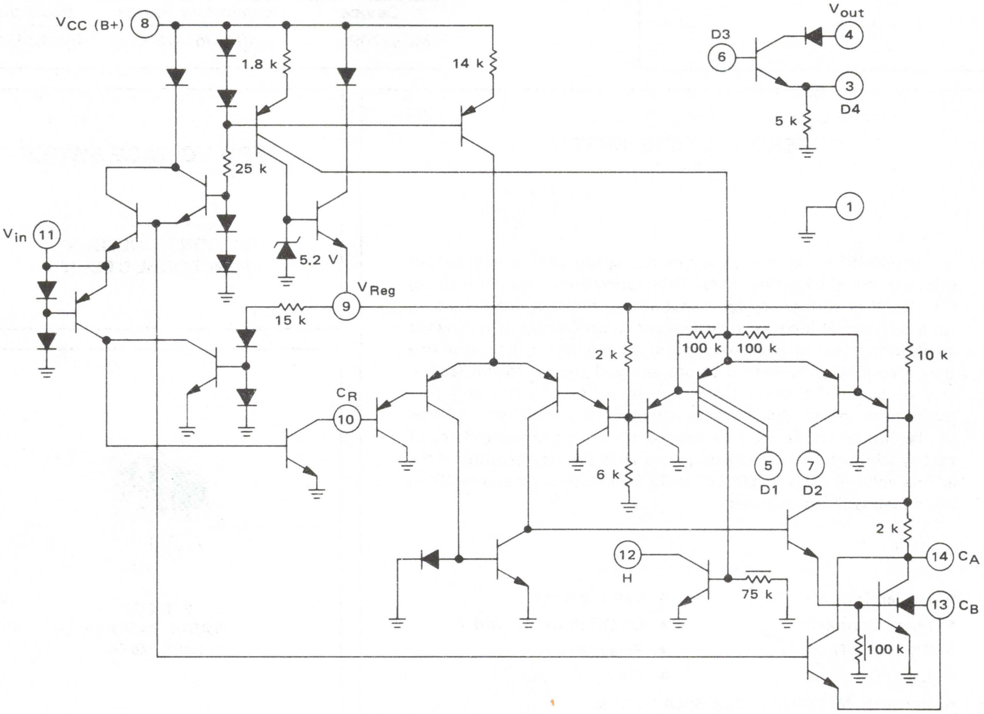


FIGURE 12 — CIRCUIT SCHEMATIC


VCC (B+)
8
1.8 k
14 k
25 k
5.2 V
Vin
11
VReg
9
15 k
CR
10
2 k
6 k
100 k
100 k
10 k
5
D1
7
D2
12
H
75 k
2 k
14
CA
13
CB
100 k
Vout
4
D3
6
3
D4
5 k
1

MC3370P

ORDERING INFORMATION

Device	Temperature Range	Package
MC3370P	−10°C to +75°C	Plastic DIP

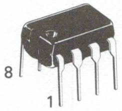
ZERO VOLTAGE SWITCH

. . . designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include; (1) a built-in voltage regulator that allows direct ac line operation, (2) a differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly; (hysteresis or proportional control to this section may be added if desired) (3) sensor input "open and short" protection; this insures that the triac will never be turned "on" if either of the inputs are shorted or opened (4) a zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (RFI) when used with resistive loads.

- Heater Controls
- Photo Controls
- Threshold Detector
- Lamp Driver
- Valve Control
- On-Off Power Controls
- Relay Driver
- Flasher Control
- Formerly MFC8070 in Case 644A Package

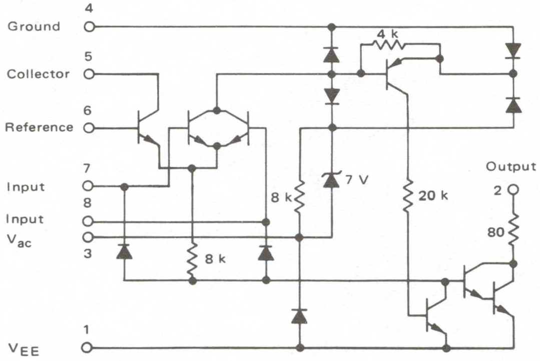
ZERO VOLTAGE SWITCH

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-04

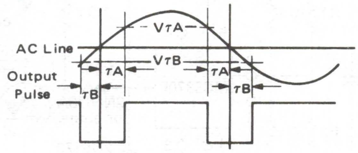
FIGURE 1 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Voltage	$V_{5\text{-}8}$	15	Vdc
DC Voltage	$V_{4\text{-}8}$	15	Vdc
DC Voltage	$V_{7\text{-}8}$	15	Vdc
Peak Supply Current	I_6	35	mA
Power Dissipation Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

FIGURE 2 – OUTPUT PULSE DEFINITION


VτA
AC Line
VτB
τA
τA
Output
Pulse
τB
τB

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

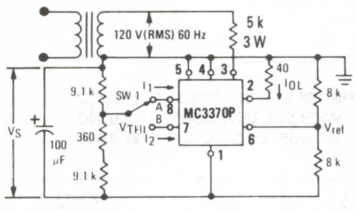
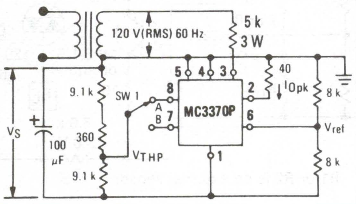
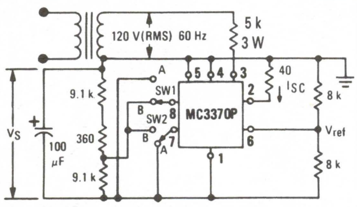
Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
 120 V(RMS) 60 Hz 5 k 3 W 40 I_{OL} 9.1 k SW 1 I_1 A B MC3370P V_{THI} I_2 8 k V_{ref} 8 k V_S 100 μF 360 9.1 k 5 4 3 2 8 7 6 1	V_S with Inhibit Output (Sw 1: A or B)	V_{SIO}	–	9.0	11	Vdc
	Output Leakage Current (Sw 1: A or B)	I_{OL}	–	5.0	100	μA
	Input Current 1 (Sw 1: A)	I_1	–	5.0	15	μA
	Input Current 2 (Sw 1: B)	I_2	–	5.0	15	μA
	Inhibit Threshold Voltage (Sw 1: A or B)	V_{THI}	V_{ref} +100 mV	V_{ref} +10 mV	–	Vdc
 120 V(RMS) 60 Hz 5 k 3 W 40 I_{Opk} 9.1 k SW 1 A B MC3370P V_{THP} 8 k V_{ref} 8 k V_S 100 μF 360 9.1 k 5 4 3 2 8 7 6 1	V_S with Pulse Output (Sw 1: A or B)	V_{SPO}	6.0	8.5	–	Vdc
	Peak Output Current (Sw 1: A or B)	$I_{O\,pk}$	50	80	–	mA
	Pulse Threshold Voltage (Sw 1: A or B)	V_{THP}	–	V_{ref} -10 mV	V_{ref} -100 mV	Vdc
	Output Pulse Width (Sw 1: A or B, See Figure 2)	τA, τB VτA, VτB	–	70 ±4.5	– –	μs V
 120 V(RMS) 60 Hz 5 k 3 W A SW1 B SW2 B A 40 I_{SC} 9.1 k MC3370P 8 k V_{ref} 8 k V_S 100 μF 360 9.1 k 5 4 3 2 8 7 6 1	Output Current With Input Short (Sw 1: B; Sw 2: A) (Sw 1: A; Sw 2: B)	I_{SC}	– –	5.0 5.0	100 100	μA

FIGURE 3 — CIRCUIT WITH INCREASED PULSE WIDTH AND TRIAC DRIVER TO CONTROL HIGH-CURRENT SCR's

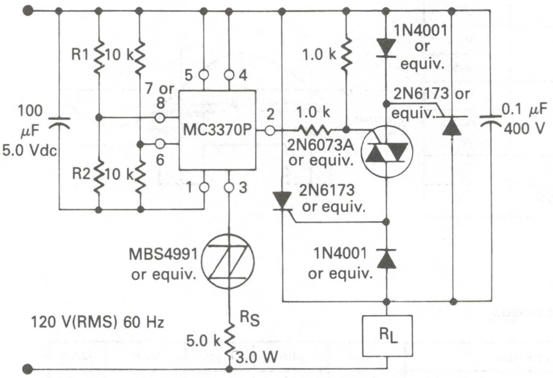

R1 10 k
5
4
7 or 8
100 μF 5.0 Vdc
MC3370P
2
6
R2 10 k
1
3
1.0 k
1N4001 or equiv.
2N6173 or equiv.
1.0 k
2N6073A or equiv.
0.1 μF 400 V
2N6173 or equiv.
MBS4991 or equiv.
1N4001 or equiv.
120 V(RMS) 60 Hz
RS
5.0 k
3.0 W
RL

FIGURE 4 — OUTPUT PULSE WIDTH versus SOURCE RESISTANCE

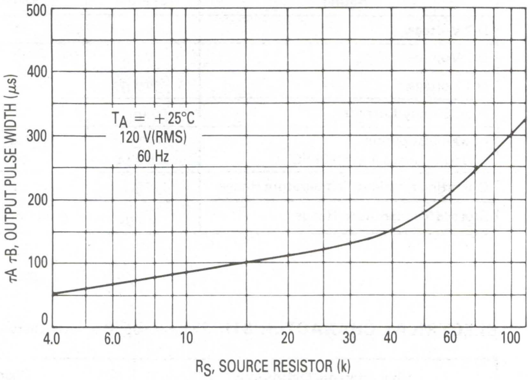
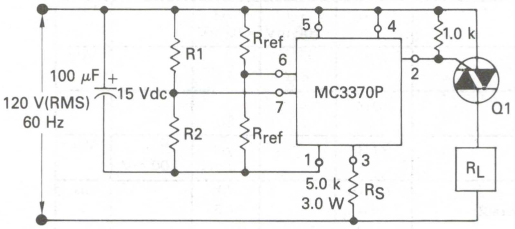
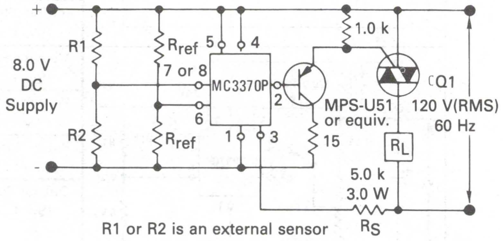


FIGURE 5 — TRIAC CONTROL CIRCUIT FOR GATE CURRENT 50 mA


R1
Rref
5
4
1.0 k
6
100 μF
15 Vdc
MC3370P
2
120 V(RMS) 60 Hz
7
Q1
R2
Rref
1
3
RL
5.0 k
3.0 W
RS

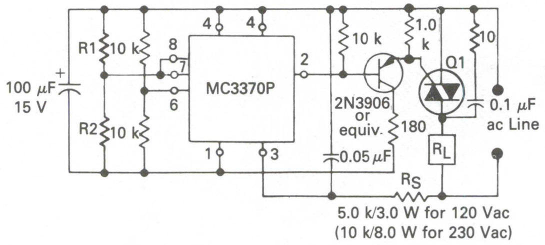
R1 or R2 is an external sensor

FIGURE 6 — TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY GATE CURRENT 0.5 A


+
R1
Rref
5
4
1.0 k
8.0 V DC Supply
7 or 8
MC3370P
2
Q1
MPS-U51 or equiv.
120 V(RMS) 60 Hz
6
R2
Rref
1
3
15
RL
-
5.0 k
3.0 W
RS

R1 or R2 is an external sensor

FIGURE 7 — TRIAC CONTROL CIRCUIT GATE CURRENT 0.1 A


4
4
R1 10 k
8
7
100 μF 15 V
+
MC3370P
2
6
R2 10 k
1
3
10 k
1.0 k
10
Q1
2N3906 or equiv.
180
0.1 μF
ac Line
0.05 μF
RL
RS
5.0 k/3.0 W for 120 Vac
(10 k/8.0 W for 230 Vac)

Recommended Motorola traics (Q1)

Maximum Continuous Current (A [RMS])	Triac Family	Case No.
12	2N6346A Series	Case 221 (TO-220AB)
25	MAC223 Series	Case 221 (TO-220AB)
40	2N5441 Series	Case 310 (TO-203)

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC3456L	—	0°C to +70°C	Ceramic DIP
MC3456P	NE556A	0°C to +70°C	Plastic DIP
MC3556L	—	−55°C to +125°C	Ceramic DIP

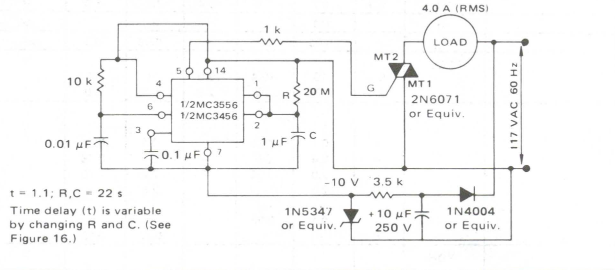
Specifications and Applications Information

DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1555/MC1455 Timer

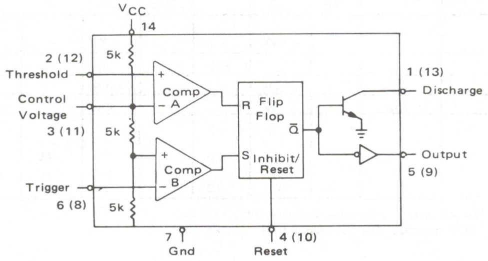
FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT



1 k
4.0 A (RMS)
LOAD
MT2
10 k
5
14
4
1
6
1/2MC3556
1/2MC3456
R
20 M
G
MT1
2N6071
or Equiv.
3
2
117 VAC 60 Hz
0.01 μF
0.1 μF
7
1 μF
C
-10 V
3.5 k
1N5347
or Equiv.
+10 μF
250 V
1N4004
or Equiv.

t = 1.1; R,C = 22 s
Time delay (t) is variable by changing R and C. (See Figure 16.)

FIGURE 2 — BLOCK DIAGRAM (1/2 SHOWN)



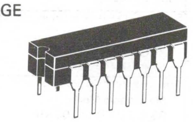
VCC
14
2 (12)
Threshold
5k
Control Voltage
3 (11)
5k
Comp A
Flip Flop
R
Q̄
S
Inhibit/ Reset
Comp B
1 (13)
Discharge
Output
5 (9)
Trigger
6 (8)
5k
7
Gnd
4 (10)
Reset

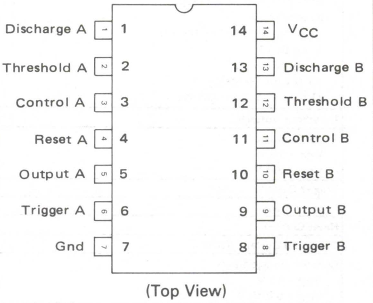
MC3456
MC3556

DUAL TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

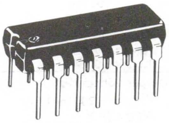
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
MO-001AA





Discharge A 1
Threshold A 2
Control A 3
Reset A 4
Output A 5
Trigger A 6
Gnd 7
14 VCC
13 Discharge B
12 Threshold B
11 Control B
10 Reset B
9 Output B
8 Trigger B
(Top View)

P SUFFIX
PLASTIC PACKAGE
CASE 646-05
(MC3456 only)



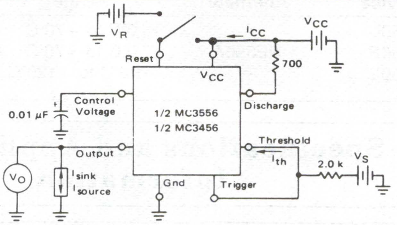
TYPICAL APPLICATIONS

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC3556		-55 to +125	
MC3456		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)
- a. When $V_S \geq 2/3\ V_{CC}$, V_O is low.
- b. When $V_S \leq 1/3\ V_{CC}$, V_O is high.
- c. When V_O is low, pin 7 sinks current. To test for Reset, set V_O, high, apply Reset voltage, and test for current flowing into discharge pin. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC3556			MC3456			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current (Per timer, double for both halfs)	I_{CC}							mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, $R_L = \infty$ Low State, (Note 1)		–	10	12	–	10	15	
Timing Error (Note 2)								
Monostable Mode R_A = 2.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 µF		–	0.5	1.5	–	0.75	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.15	0.2	–	0.1	–	%/Volt
Astable Mode $R_A = R_B$ = 2.0 kΩ to 100 kΩ C = 0.01 µF								
Initial Accuracy		–	1.5	–	–	2.25	–	%
Drift with Temperature		–	90	–	–	150	–	PPM/°C
Drift with Supply Voltage		–	0.15	–	–	0.3	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.03	0.1	–	0.03	0.1	µA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							V
(V_{CC} = 15 V)								
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.25	–	2.0	2.75	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA) V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA) V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Toggle Rate (Figures 17, 19) R_A = 3.3 kΩ, R_B = 6.8 kΩ, C = 0.003 µF	–	–	100	--	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns
Matching Characteristics Between Sections (Monostable)								
Initial Timing Accuracy		–	0.5	1.0	–	1.0	2.0	%
Timing Drift with Temperature		–	±10	–	–	±10	–	ppm/°C
Drift with Supply Voltage		–	0.1	0.2	–	0.2	0.5	%/V

NOTES:
1. Supply current when output is high is typically 2.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

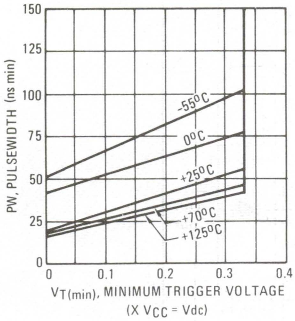


FIGURE 5 – SUPPLY CURRENT

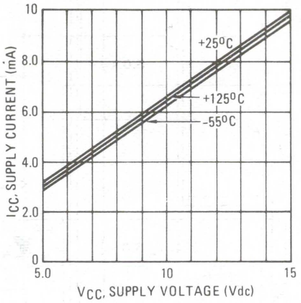


FIGURE 6 – HIGH OUTPUT VOLTAGE

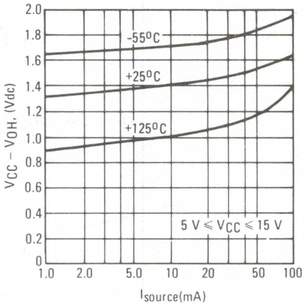


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

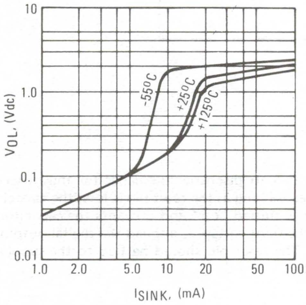


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

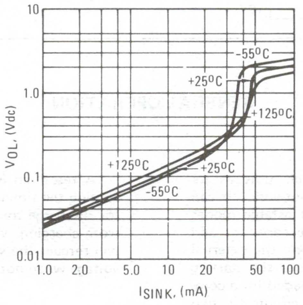


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

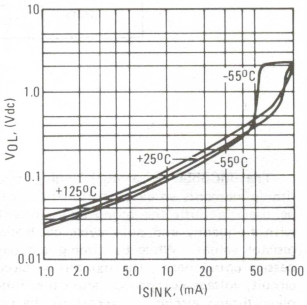


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

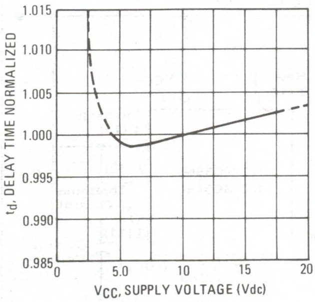


FIGURE 11 – DELAY TIME versus TEMPERATURE

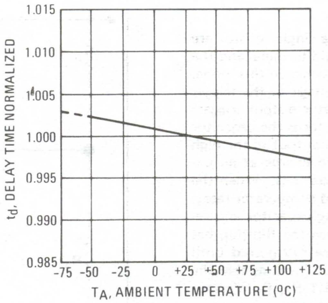


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE

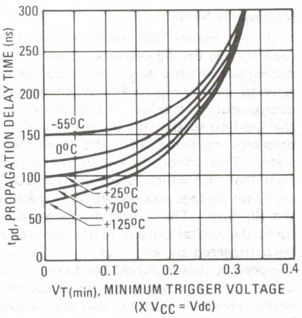
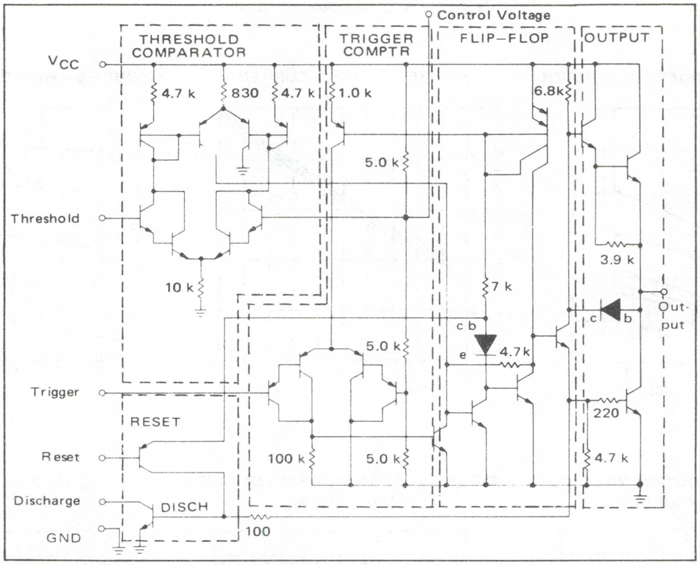


FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC


Control Voltage
THRESHOLD COMPARATOR
TRIGGER COMPTR
FLIP–FLOP
OUTPUT
VCC
4.7 k
830
4.7 k
1.0 k
6.8k
5.0 k
Threshold
3.9 k
10 k
7 k
Out-put
c
b
c b
e
5.0 k
4.7k
Trigger
220
RESET
Reset
100 k
5.0 k
4.7 k
Discharge
DISCH
GND
100

GENERAL OPERATION

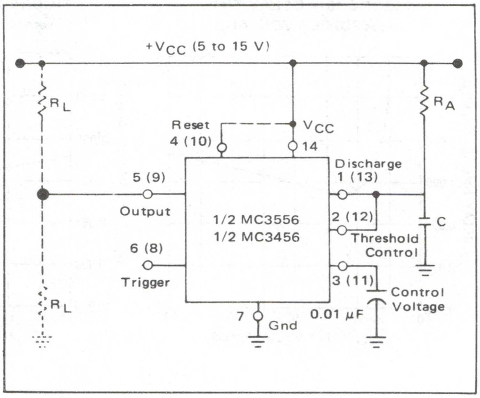
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below $1/3\ V_{CC}$ the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches $2/3\ V_{CC}$ the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

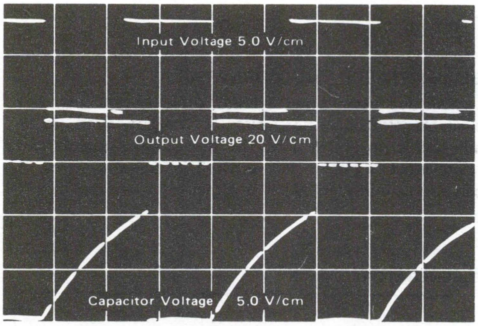
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT


+VCC (5 to 15 V)
RL
RA
Reset
4 (10)
VCC
14
Discharge
1 (13)
5 (9)
Output
1/2 MC3556
1/2 MC3456
2 (12)
C
Threshold
Control
6 (8)
Trigger
3 (11)
Control
Voltage
RL
7
Gnd
0.01 μF

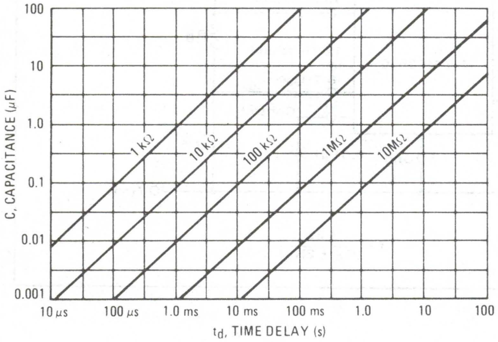
GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY



Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geqslant \frac{V_{CC}\ (\text{Vdc})}{I_7\ (\text{A})} \geqslant \frac{V_{CC}\ (\text{Vdc})}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

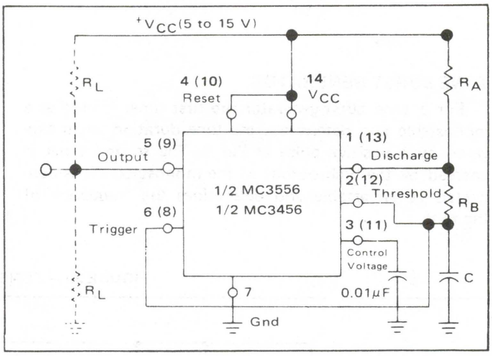
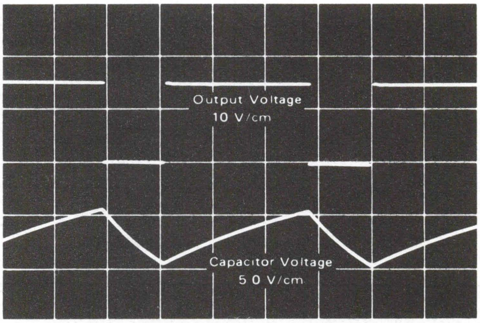
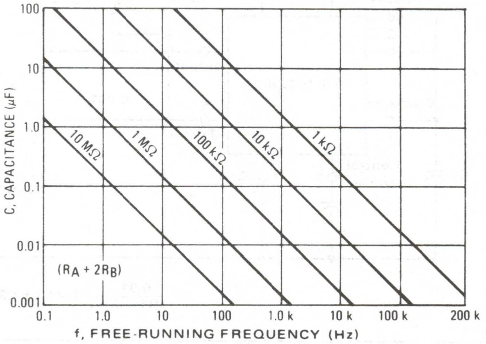


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

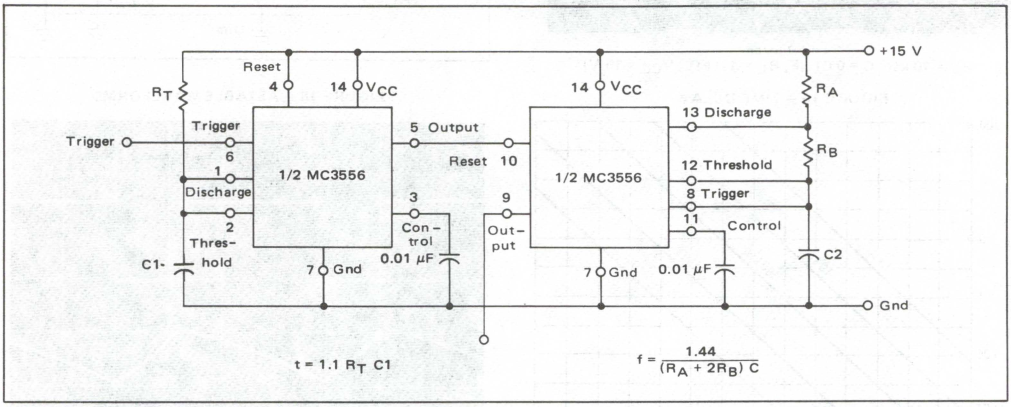
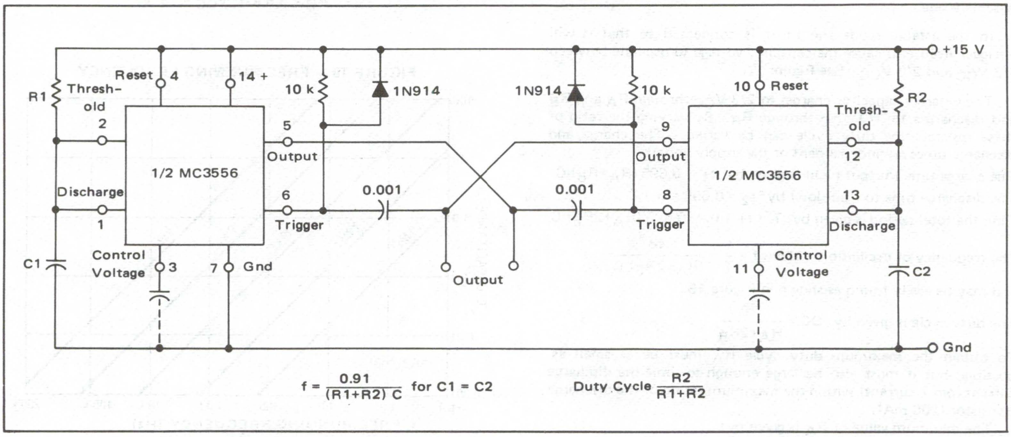

+15 V
Reset
4
14
V_{CC}
R_T
Trigger
Trigger
6
1
Discharge
2
Thres-hold
C1
1/2 MC3556
5 Output
3
Con-trol
0.01 µF
7 Gnd
Reset 10
9
Out-put
14 V_{CC}
1/2 MC3556
13 Discharge
12 Threshold
8 Trigger
11
Control
R_A
R_B
C2
0.01 µF
7 Gnd
Gnd
$t = 1.1\ R_T\ C1$
$f = \frac{1.44}{(R_A + 2R_B)\ C}$

FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR


+15 V
R1
Reset 4
14 +
Thresh-old
2
1/2 MC3556
Discharge
1
C1
Control Voltage
3
7 Gnd
10 k
1N914
5
Output
6
Trigger
0.001
Output
0.001
1N914
10 k
9
Output
8
Trigger
10 Reset
1/2 MC3556
Thresh-old
12
13
Discharge
R2
C2
Control Voltage
11
Gnd
$f = \frac{0.91}{(R1+R2)\ C}$ for C1 = C2
Duty Cycle $\frac{R2}{R1+R2}$

APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

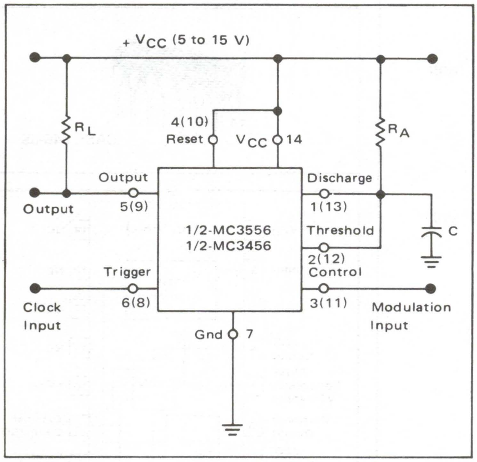
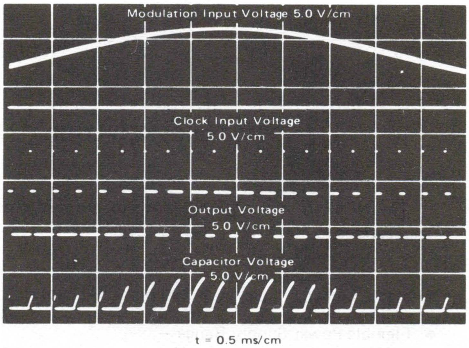

+ V_{CC} (5 to 15 V)
R_L
4(10)
Reset
V_{CC} 14
R_A
Output
5(9)
Output
Discharge
1(13)
1/2-MC3556
1/2-MC3456
Threshold
2(12)
Control
C
Trigger
6(8)
3(11)
Clock
Input
Modulation
Input
Gnd 7

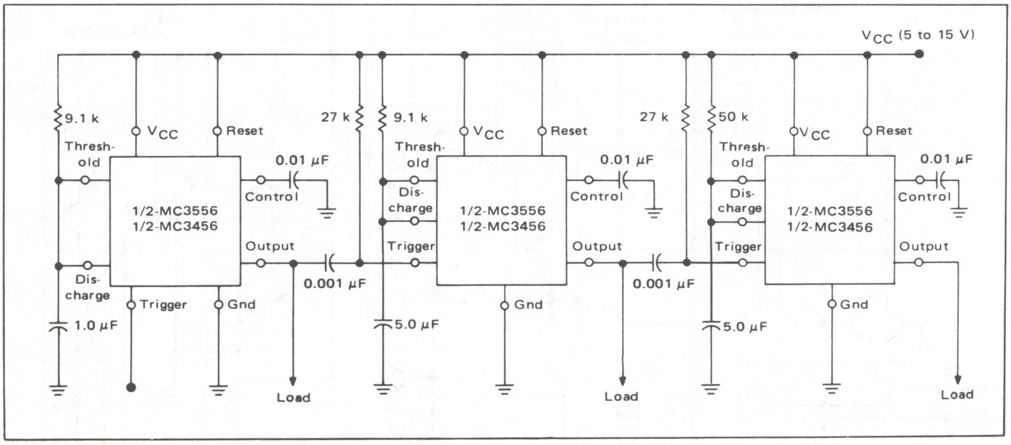
FIGURE 23 — PULSE WIDTH MODULATION WAVEFORMS (R_A = 10 kΩ, C = 0.02 µF, V_{CC} = 15 V)



Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24

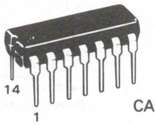

V_{CC} (5 to 15 V)
9.1 k
V_{CC}
Reset
Thresh-old
1/2-MC3556
1/2-MC3456
0.01 µF
Control
Output
Dis-charge
Trigger
Gnd
1.0 µF
Load
0.001 µF
27 k
9.1 k
V_{CC}
Reset
Thresh-old
Dis-charge
Trigger
1/2-MC3556
1/2-MC3456
0.01 µF
Control
Output
Gnd
5.0 µF
Load
0.001 µF
27 k
50 k
V_{CC}
Reset
Thresh-old
Dis-charge
Trigger
1/2-MC3556
1/2-MC3456
0.01 µF
Control
Output
Gnd
5.0 µF
Load

NE565N

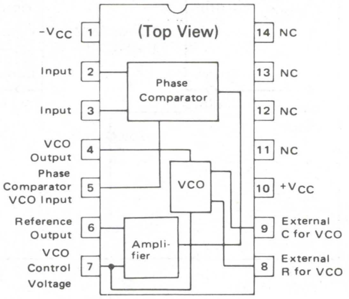
MOTOROLA

PHASE-LOCKED LOOP

SILICON MONOLITHIC
INTEGRATED CIRCUITS



CASE 646-05

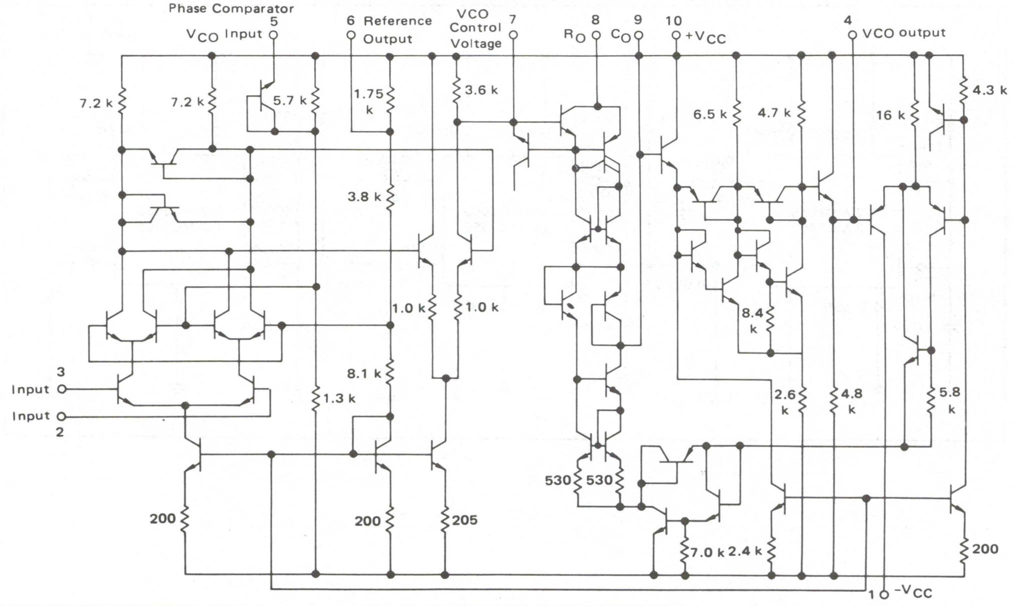

(Top View)
-VCC 1
Input 2
Input 3
VCO Output 4
Phase Comparator VCO Input 5
Reference Output 6
VCO Control Voltage 7
External R for VCO 8
External C for VCO 9
+VCC 10
NC 11
NC 12
NC 13
NC 14
Phase Comparator
VCO
Amplifier

PHASE-LOCKED LOOP

The NE565N is designed for general-purpose phase-locked loop applications to 500 kHz.

- Stable Center Frequency – 200 ppm/°C (Typ)
- Flexible Power Supply Range –
  ±5 to ±12 Volts with Small Frequency Drift – 100 ppm/% (Typ)
- Low Total Harmonic Distortion of Demodulator Output
  – 1.5% (Max)
- Linear Triangle Wave Output – 0.5% (Typ)
- TTL, DTL Compatible Inputs and Outputs
- Adjustable Hold In Range – ±1% to >±60%.

FIGURE 1 – REPRESENTATIVE CIRCUIT SCHEMATIC


Phase Comparator VCO Input 5
6 Reference Output
VCO Control Voltage 7
8 RO
9 CO
10 +VCC
4 VCO output
7.2 k
7.2 k
5.7 k
1.75 k
3.6 k
6.5 k
4.7 k
16 k
4.3 k
3.8 k
1.0 k
1.0 k
8.4 k
8.1 k
1.3 k
2.6 k
4.8 k
5.8 k
3 Input
Input 2
530
530
200
200
205
7.0 k
2.4 k
200
1 -VCC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±12	Vdc
Power Dissipation (Package Limitation) Derate above 25°C	P_D	8.25 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Test Circuit Figure 2, T_A = 25°C, V_{CC} = ±6.0 Vdc unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Current	–	8.0	12.5	mA
Input Impedance (Pins 2, 3) $-4.0 \text{ V} < V2, V3 < 0 \text{ V}$	–	5.0	–	kΩ
Input Level Required for Tracking f_O = 10 kHz, ±10% Frequency Deviation	10	–	–	mVrms
VCO Maximum Operating Frequency C_O = 2.7 pF	–	500	–	kHz
Operating Frequency Temperature Coefficient	–	200	–	ppm/°C
Frequency Drift with Supply Voltage	–	200	–	ppm/%
Triangle Wave Ouptut Voltage	2.0	2.4	3.0	Vp-p
Triangle Wave Output Linearity	–	0.5	–	%
Square Wave Output Level	4.7	5.4	–	Vp-p
VCO Output Impedance (Pin 4)	–	5.0	–	kΩ
Square Wave Duty Cycle	40	50	60	%
Square Wave Rise Time	–	20	–	ns
Square Wave Fall Time	–	50	–	ns
Output Current Sink (Pin 4)	0.6	1.0	–	mA
VCO Sensitivity	–	6600	–	Hz/V
Demodulated Output Voltage (Pin 7) f_O = 10 kHz, ±10% Frequency Deviation	200	300	–	mVp-p
Total Harmonic Distortion f_O = 10 kHz, ±10% Frequency Deviation	–	0.2	1.5	%
Output Impedance (Pin 7)	–	3.5	–	kΩ
DC Output Voltage Level (Pin 7)	4.0	4.5	5.0	V
Output Offset Voltage (Input = 0) /V7-V6/	–	50	200	mV
Temperature Drift of /V7-V6/	–	500	–	μV/°C
AM Rejection	–	40	–	dB
Phase Detector Sensitivity K_D	–	0.68	–	V/radian

FIGURE 2 – TEST CIRCUIT SCHEMATIC

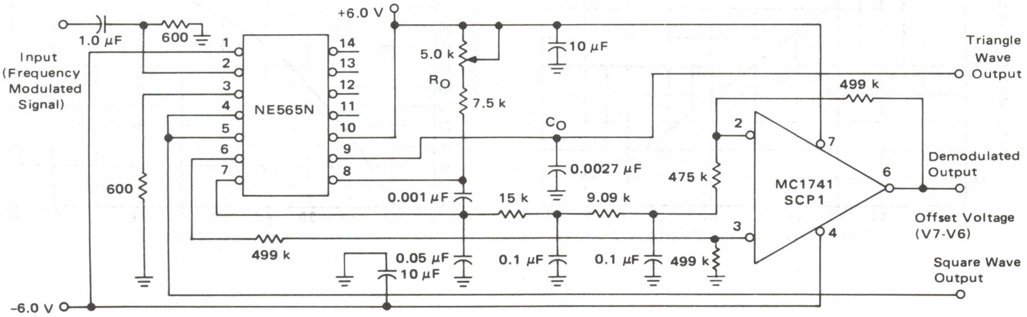

+6.0 V
1.0 μF
600
Input
(Frequency
Modulated
Signal)
NE565N
1
2
3
4
5
6
7
8
9
10
11
12
13
14
5.0 k
R_O
7.5 k
10 μF
C_O
0.0027 μF
600
0.001 μF
15 k
9.09 k
499 k
0.05 μF
10 μF
0.1 μF
0.1 μF
499 k
475 k
499 k
MC1741
SCP1
2
3
4
6
7
Triangle
Wave
Output
Demodulated
Output
Offset Voltage
(V7-V6)
Square Wave
Output
-6.0 V

FIGURE 3 – POWER SUPPLY CHARACTERISTICS

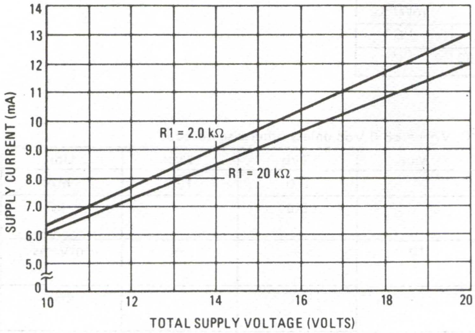


FIGURE 4 – VCO CONVERSION GAIN

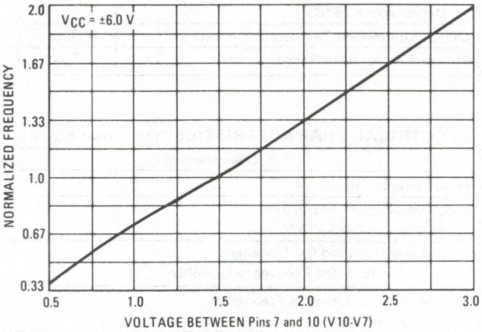


FIGURE 5 – LOCK RANGE versus INPUT VOLTAGE

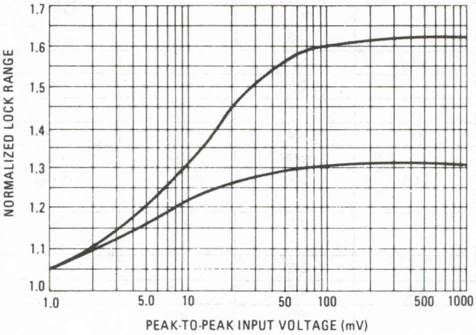


FIGURE 6 – OSCILLATOR OUTPUT WAVEFORMS

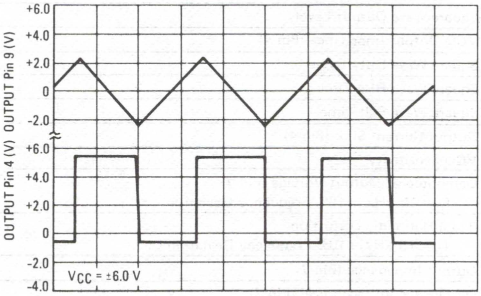


FIGURE 7 – LOCK RANGE
(As a Function of Gain Setting Resistance)

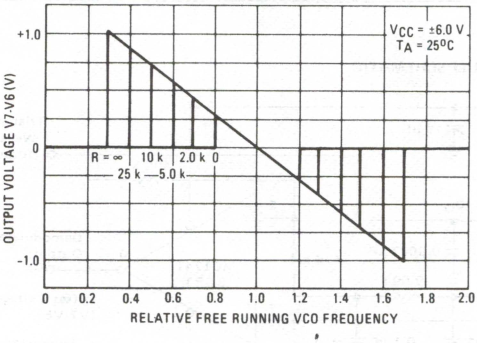
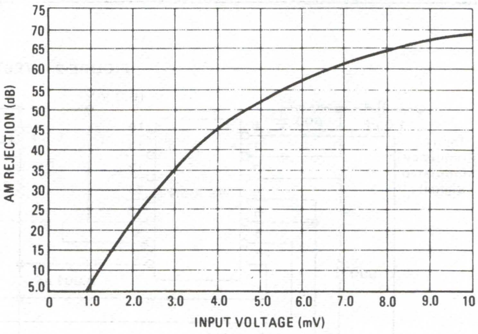


FIGURE 8 – AM REJECTION CHARACTERISTICS



GENERAL APPLICATIONS INFORMATION

The following formulas are useful when designing with the NE565N:

1. Center Frequency — $f_O \approx \frac{1}{3.7 R_O C_O}$

   Where: f_O is the frequency of the VCO without input signal. For R_O, C_O circuit location see Figure 2.

2. Loop Gain — $K_O K_D A$

   Definitions:

   K_O — VCO Conversion Gain — the conversion factor between VCO frequency and control voltage. $K_O = 4.12\ f_O$ (units are in radians/sec/volt)

   Example: for VCO Sensitivity @ 10 kHz (in Hz/volt)

   $$K_O = \frac{4.12 \times 10^4}{2\ \pi \text{ radians}} = 6600 \text{ Hz/Volt}$$

   K_D —Phase Detector Gain Factor — the conversion factor between the phase detector output voltage and the phase difference between input and VCO signals. Units are in volts/radian.

   $$K_D = \frac{8.1 \bullet A}{V_{CC}}$$

   Where: $A = f(R6 \text{ to } R7)$

   Hence: $K_D = \frac{8.1}{V_{CC}}\ [f(R6\text{-}R7)]$

   Where: V_{CC} is total system supply voltage, f(R6-R7) is internal amplifier gain (See Figure 9). V_{CC} - total supply voltage to the circuit.

3. Lock Range — $f_L = \pm \frac{8 f_O}{V_{CC}}$

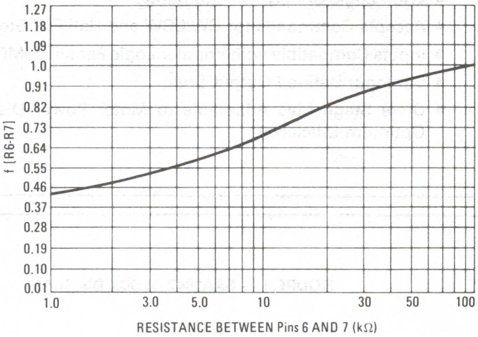
   Where: f_L is the range of frequencies in the area of f_O over which the VCO, once locked to the input signal, will remain locked.

4. Capture Range — $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\ \pi f_L}{\tau}}$

   Where: f_C is that range of frequencies around f_O over which the loop will acquire lock with an input signal initially starting out of lock.

   (τ = Time Constant at Pin 7)

FIGURE 9 — INTERNAL AMPLIFIER GAIN CHARACTERISTICS



SAA1042
SAA1042A

MOTOROLA

Specifications and Applications Information

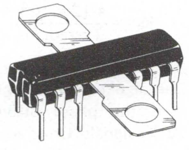
STEPPER MOTOR DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

STEPPER MOTOR DRIVER

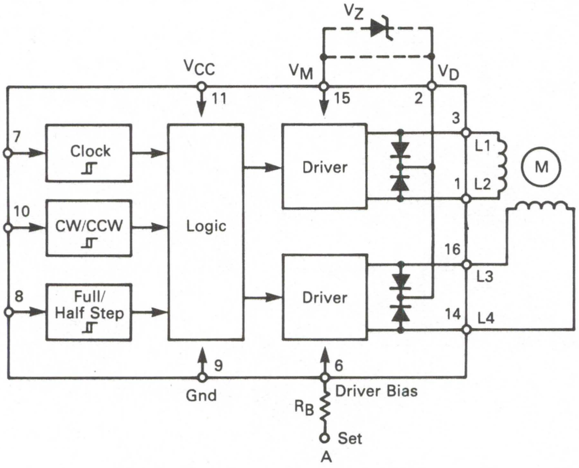
The SAA1042 drives a two-phase stepper motor in the bipolar mode. The device contains: three input stages, a logic section and two output stages.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042
  24 V: SAA1042A
- 500 mA/Coil Drive Capability
- Built-In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

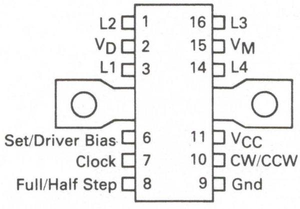


PLASTIC PACKAGE
CASE 721-02

FIGURE 1 — SAA1042 BLOCK DIAGRAM


V_Z
V_{CC}
V_M
V_D
11
15
2
3
7
Clock
Logic
Driver
L1
M
1
L2
10
CW/CCW
16
L3
8
Full/ Half Step
Driver
14
L4
9
6
Gnd
Driver Bias
R_B
Set
A

PIN ASSIGNMENT


L2 1
V_D 2
L1 3
Set/Driver Bias 6
Clock 7
Full/Half Step 8
16 L3
15 V_M
14 L4
11 V_{CC}
10 CW/CCW
9 Gnd

(Top View)

Note: Case heat sink is electrically connected to ground (Pin 9) through the die substrate.

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Rating	Symbol	SAA1042	SAA1042A	Unit
Clamping Voltage (Pins 1, 3, 14 & 16)	V_{clamp}	20	30	V
Over Voltage ($V_{OV} = V_{clamp} - V_M$)	V_{OV}	6.0		V
Supply Voltage	V_{CC}	20	30	V
Switching or Motor Current/Coil	I_M	500		mA
Input Voltage (Pins 7, 8 & 10)	V_{in} clock	V_{CC}		V
	V_{in} Full/Half			
	V_{in} CW/CCW			
Power Dissipation	P_D*	2.0		W
Derate above T_A = 25°C	$1/\theta_{JA}$	20		mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	50		°C/W
Thermal Resistance, Junction to Case	θ_{JC}	8.0		°C/W
Operating Junction Temperature Range	T_J	−30 to +125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

*The power dissipation, P_D, of the circuit is given by the supply voltage, V_M and V_{CC}, and the motor current, I_M, and can be determined from Figures 3 and 5. $P_D = P_{drive} + P_{logic}$.

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Characteristic	Pin	Symbol	V_{CC}	Min	Typ	Max	Unit
Supply Current	11	I_{CC}	5.0 V	—	—	3.5	mA
			20 V	—	—	8.5	
Motor Supply Current	15	I_M					mA
(I Pin 6 = −400 μA, Pins 1, 3, 14, 16 Open)							
V_M = 6.0 V			5.0 V	—	25	—	
V_M = 12 V			5.0 V	—	30	—	
V_M = 24 V			5.0 V	—	40	—	
Input Voltage — High State	7, 8, 10	V_{IH}	5.0 V	2.0	—	—	V
			10 V	7.0	—	—	
			15 V	10	—	—	
			20 V	14	—	—	
Input Voltage — Low State	7, 8, 10	V_{IL}	5.0 V	—	—	0.8	V
			10 V	—	—	1.5	
			15 V	—	—	2.5	
			20 V	—	—	3.5	
Input Reverse Current — High State ($V_{in} = V_{CC}$)	7, 8, 10	I_{IR}	5.0 V	—	—	2.0	μA
			10 V	—	—	2.0	
			15 V	—	—	3.0	
			20 V	—	—	5.0	
Input Forward Current — Low State (V_{in} = Gnd)	7, 8, 10	I_{IF}	5.0 V	−10	—	—	μA
			10 V	−25	—	—	
			15 V	−40	—	—	
			20 V	−55	—	—	
Output Voltage — High State	1, 3, 14, 16	V_{OH}	5.0 to 20 V				V
(V_M = 12 V) I_{out} = −500 mA				—	$V_M - 2.0$	—	
I_{out} = − 50 mA				—	$V_M - 1.2$	—	
Output Voltage — Low State	1, 3, 14, 16	V_{OL}	5.0 to 20 V				V
I_{out} = 500 mA				—	0.7	—	
I_{out} = 50 mA				—	0.2	—	
Output Leakage Current ($V_M = V_D = V_{clamp\ max}$.) Pin 6: Open	1, 3, 14, 16	I_{DR}	5.0 to 20 V	−100	—	—	μA
Clamp Diode Forward Voltage (Drop at I_M = 500 mA)	2	V_F	—	—	2.5	3.5	V
Clock Frequency	7	f_c	5.0 to 20 V	0	—	50	kHz
Clock Pulse Width	7	t_w	5.0 to 20 V	10	—	—	μs
Set Pulse Width	6	t_s	—	10	—	—	μs
Set Control Voltage — High State	6	—	—	V_M	—	—	V
Low State				—	—	0.5	

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependant on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1,' the motor direction will be nominally counter clockwise (CCW), depending on the motor connections.

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3, 14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and Pin 15 as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$V_{clamp} = V_M + 6.0\ V$

$V_Z = V_{clamp} - V_M - V_F$*

where: V_F = clamp diodes forward voltage drop (see Figure 4)

V_{clamp}:
$\leqslant 20\ V$ for SAA1042
$\leqslant 30\ V$ for SAA1042A

Pins 2 and 15 can be linked, in this case $V_Z = 0\ V$.

Set/Bias Input — (Pin 6) This input has two functions:

The resistor R_B adapts the drivers to the motor current.

A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open-collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off-state) has to sustain the motor voltage V_M. When a pulse is applied via the buffer and the bias resistor R_B:

During the pulse duration, the motor driver transistors are turned off.

After elapsing the pulse, the outputs will have defined states.

Figure 6 shows the timing diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil.

A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is V_M + 6.0 V (see the Maximum Ratings), in this application V_M = 12 V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\ V - 1.7\ V = 4.3\ V.$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase locked by the MC14046B and the MC14024.

The voltage on the clock input, is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

A Logic '0' applied to the Full/Half input, Pin 8, operates the motor in the Full Step mode. A Logic '1' at this input will result in the Half Step mode. The logic level state on the CW/CCW input, Pin 10, and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non-use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low.
(See Figure 6, the timing diagram).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. If the input is not used, the 'bottom' of R_B must be grounded.

The total power dissipation of the circuit can be determined from Figures 3 and 5.

$$P_D = 0.9\ W + 0.08\ W = 0.98\ W.$$

This results in a junction to ambient temperature, without a heatsink of:

$$T_J - T_A = 50°C/W \times 0.98\ W = 49°C.$$

or a maximum ambient temperature of 76°C. For operation at elevated temperatures a heatsink is required.

FIGURE 2 — BIAS RESISTOR R_B versus MOTOR CURRENT

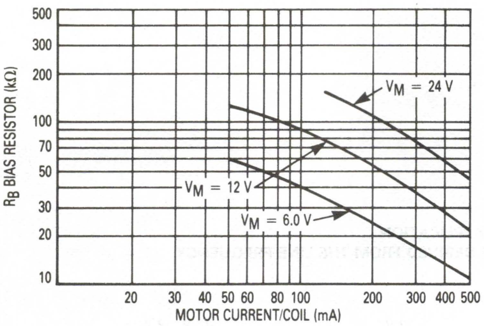


FIGURE 3 — DRIVE STAGE POWER DISSIPATION

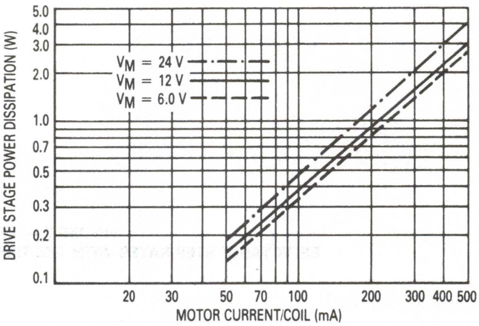


FIGURE 4 — CLAMP DIODE FORWARD CURRENT versus FORWARD VOLTAGE

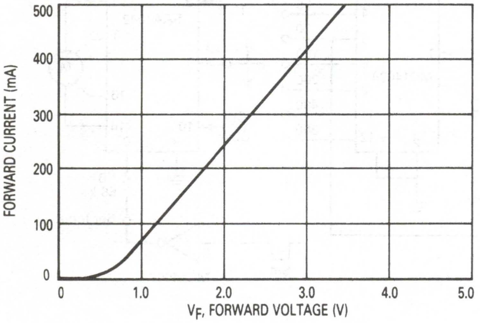


FIGURE 5 — POWER DISSIPATION versus LOGIC SUPPLY VOLTAGE

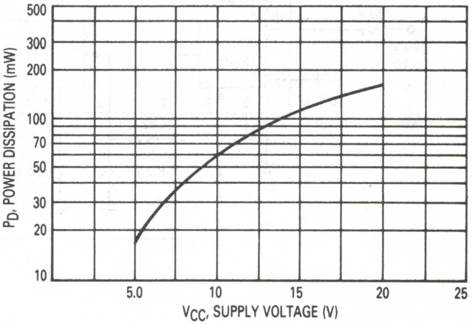


FIGURE 6 — TIMING DIAGRAM

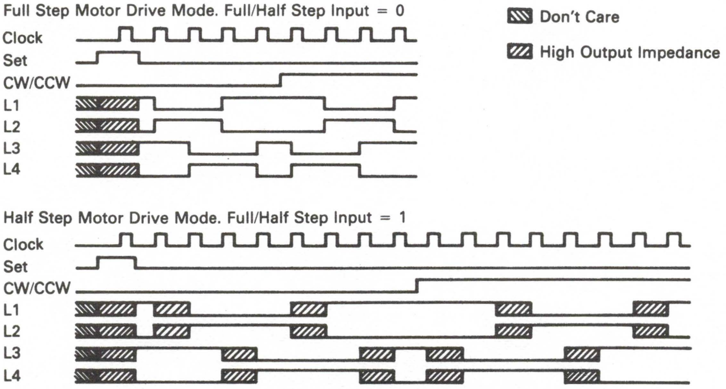
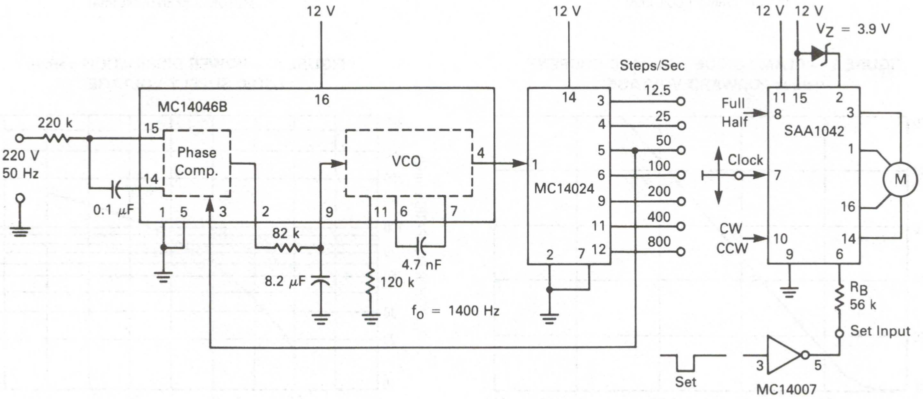

Full Step Motor Drive Mode. Full/Half Step Input = 0
Clock
Set
CW/CCW
L1
L2
L3
L4
▧ Don't Care
▨ High Output Impedance
Half Step Motor Drive Mode. Full/Half Step Input = 1
Clock
Set
CW/CCW
L1
L2
L3
L4

FIGURE 7 — TYPICAL APPLICATION
SELECTABLE STEP RATES WITH THE TIME BASE DERIVED FROM THE LINE FREQUENCY


12 V
12 V
12 V 12 V
V_Z = 3.9 V
Steps/Sec
MC14046B
16
220 k
15
220 V
50 Hz
Phase
Comp.
14
0.1 µF
1 5 3
2
9
VCO
4
11 6
7
82 k
8.2 µF
120 k
4.7 nF
fo = 1400 Hz
14
1
MC14024
3
4
5
6
9
11
12
2 7
12.5
25
50
100
200
400
800
Full
Half
Clock
CW
CCW
11 15
2
8
3
SAA1042
1
7
16
10
9
14
6
M
RB
56 k
Set Input
Set
3
5
MC14007

TDA1085A
TDA1085B

MOTOROLA

Specification and Applications Information

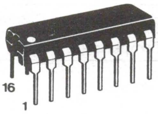
UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085A or B have all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Additionally they have the facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Powerup
- On-Chip Frequency/Voltage Convertor and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

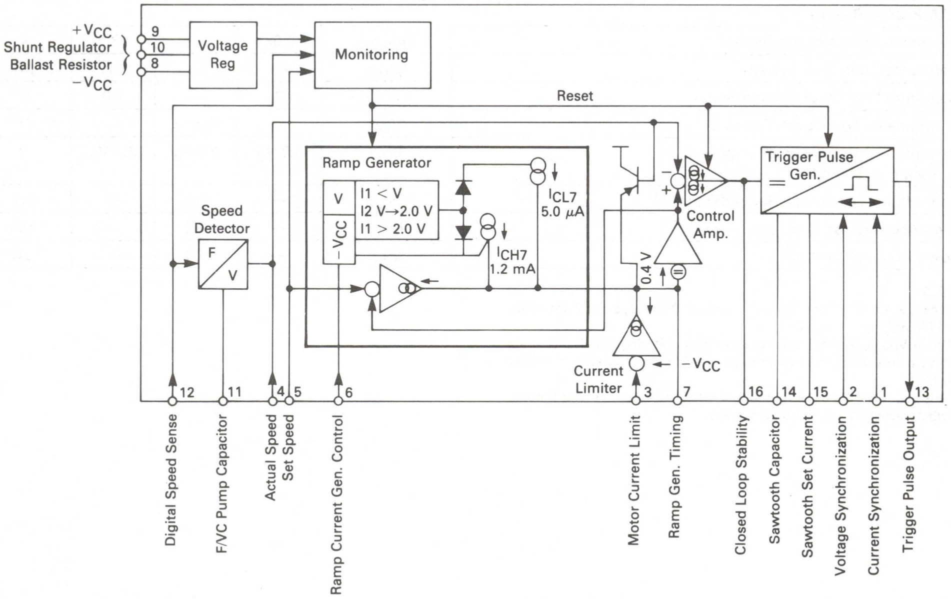
UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



+VCC
Shunt Regulator
Ballast Resistor
−VCC
9
10
8
Voltage Reg
Monitoring
Reset
Ramp Generator
V
−VCC
I1 < V
I2 V→2.0 V
I1 > 2.0 V
ICL7 5.0 μA
ICH7 1.2 mA
Speed Detector
F
V
0.4 V
Control Amp.
Current Limiter
−VCC
Trigger Pulse Gen.
12
11
4
5
6
3
7
16
14
15
2
1
13
Digital Speed Sense
F/VC Pump Capacitor
Actual Speed
Set Speed
Ramp Current Gen. Control
Motor Current Limit
Ramp Gen. Timing
Closed Loop Stability
Sawtooth Capacitor
Sawtooth Set Current
Voltage Synchronization
Current Synchronization
Trigger Pulse Output

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	$V_{Pin\ 9\text{-}8}$	17	V
Power Supply Current (Pin 10 Open)	$I_{Pin\ 9}$	15	mA
Peak Power Supply Regulation Current	$I_{Pin\ 9} + I_{Pin\ 10}$	35	mA
Peak ac Synchronization Input Current	$I_{Pin\ 1}$ $I_{Pin\ 2}$	±1.0	mA
Peak Output Triggering Current (Pulse Width 300 µs; Duty Cycle ≤ 3%)	$I_{Pin\ 13}$	200	mA
Current Drain per Listed Pin	I_{15} I_3 I_{12}	1.0 −5.0 −3.0, +0.1	mA
Power Dissipation (T_A = 25°C) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Regulated Voltage* ($I_9 + I_{10}$ = 10 mA)	V_{CC}	—	15.5	—	V
Monitoring Enable Level*	V_{ME}	—	15.1	—	V
Monitoring Disable Level*	V_{MD}	—	14.5	—	V
Internal Current Consumption[1]	$I_{Pin\ 9}$	—	4.2	—	mA
RAMP GENERATOR					
Reference Input Voltage Range[2]	$V_{Pin\ 5\text{-}8}$	0.08	—	13.5	V
Reference Input Bias Current	$I_{Pin\ 5}$	—	—	−20	µA
Distribute Low Level Voltage Range	$V_{Pin\ 6}$	0	—	2.0	V
Distribute — Low Level (Figure 2)	V_{DL}	—	$V_{Pin\ 6}$	—	V
Distribute — Upper Level* (Figure 2) ($V_{Pin\ 6}$ = 950 mV)	V_{DU}	1.9 V_6	2.0 V_6	2.1 V_6	V
Low–High Acceleration Range (Figure 2)	ΔV_{DA}	—	400	—	mV
High Acceleration Charging Current	I_{CH7}	—	1.2	—	mA
Low Charging Current[3]	I_{CL7}	—	5.0	—	µA

NOTES:

1. Pins 1, 2, 11, 12, 14 and 15 not connected; Pins 4, 5, 6 and 7 grounded to Pin 8: V_{CC} = 15.5 V
2. When $V_{Pin\ 5}$ is ≤ 80 mV, the internal monitoring circuit interprets it as a true zero, thus minimizing the effects of control amplifier offsets.
3. This value should be accounted for when externally setting the distribute acceleration charging current.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Stage Current Gain	$\frac{I_{DL7}}{\Delta I_3}$	—	170	—	—
Output Discharge Current Swing	I_{DL7}	—	35	—	mA
CONTROL AMPLIFIER					
Actual Speed Voltage Range	$V_{Pin\ 4\text{-}8}$	0	—	13.5	V
Actual Speed Input Bias Current	$I_{Pin\ 4}$	—	—	−350	nA
Total Input Offset Voltage[4]	V_{off}	−60	—	20	mV
Transconductance $\left(\frac{\Delta I_{Pin\ 16}}{V_{Pin\ 4} - V_{Pin\ 7}}\right)$	g_m	—	300	—	μA/V
Output Current Swing	$I_{Pin\ 16}$	—	±100	—	μA
FREQUENCY/VOLTAGE CONVERTER					
Input Signal Low Voltage[5]	V_{L12}	−0.1	—	—	V
Input Signal High Voltage	V_{H12}	0.1	—	5.0	V
Polarization Current	$I_{Pin\ 12}$	—	−25	—	μA
Conversion Rate[6]*	K_C	—	15	—	mV/Hz
Linearity* (Figure 3)	K_L	—	±4.0	—	%
TRIGGER PULSE GENERATOR					
Voltage Synchronization Levels	$I_{Pin\ 2}$	—	±50	—	μA
Current Synchronization Levels	$I_{Pin\ 1}$	—	±50	—	μA
Input Voltage Swing (for full angle swing)	V	—	11.7	—	V
Trigger Pulse Width[7]	t_p	—	55	—	μs
Trigger Pulse Repetition Period	t	—	215	—	μs
Trigger Pulse High Level ($I_{Pin\ 13}$ = 150 mA)	$V_{Pin\ 13}$	$V_{CC}-4$	—	—	V
Output Leakage Current ($V_{Pin\ 13}$ = 0 V)	$I_{oPin\ 13}$	—	—	30	μA

4. V_{off} is defined as being the voltage difference between Pin 5 and 4 with no current flow on Pin 16.
5. The negative swing is clamped to −0.3 V.
6. $V_{Pin\ 4} = k \cdot C_{Pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{Pin\ 4} \cdot \left(1 + \frac{180 \times 10^3}{R_{Pin\ 11}}\right)^{-1} \cdot$ freq in.
   Where: $9 < K < 13$ & $V_a = 1.3$ V.
7. The timing given is when $C_{Pin\ 14}$ = 47 nF.

* These figures apply for the application shown in Figure 4.

INPUT/OUTPUT FUNCTIONS

VOLTAGE REGULATOR — (Pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between Pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, max. consumption by the circuitry), at least 1.0 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry), the maximum resistor value is chosen so that the voltage at Pin 10 falls towards 3.0 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shutdown.

For operation from an externally regulated voltage, Pin 10 is not connected.

SPEED SENSING — (Pins 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogically (tachogenerator amplitude).

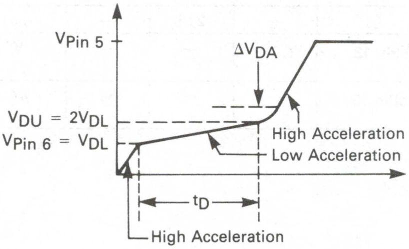
For digital sensing, a bipolar signal with respect to ground is applied to Pin 12. During positive excursions $C_{Pin\ 11}$ is charged. An internal mirror delivers ten times the charge on $C_{Pin\ 11}$ via Pin 4. However, due to internal circuitry, the charge on Pin 4 can vary in the region of 9 to 13 times the charge on $C_{Pin\ 11}$. For that reason it is necessary to calibrate the Frequency/Voltage Convertor (F/VC) with a variable resistor on Pin 4. Thus the relationship between speed and $V_{Pin\ 4}$ is defined by $R_{Pin\ 4}$ and $C_{Pin\ 11}$.

To maintain linearity in the high speed ranges it is important that $C_{Pin\ 11}$ is fully charged across an equivalent resistor of about 180 kΩ. It should be borne in mind that the impedance on Pin 11 should be kept as low as possible as $C_{Pin\ 11}$ has a large influence on the temperature coefficient of the FV/C. The time constant on Pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances $V_{Pin\ 12}$ increases. Should $V_{Pin\ 12}$ exceed 5.0 V the triac trigger pulses are inhibited and the circuit resets.

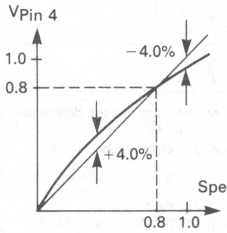
A 470 kΩ resistor from Pin 11 to $+V_{CC}$ significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

FIGURE 2 — RAMP GENERATOR TRANSFER CHARACTERISTIC



The shape of the curve is determined by $CR_{Pin\ 7}$; where $C_{Pin\ 7}$ defines the high acceleration slope and $R_{Pin\ 7}$ defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER OUTPUT CHARACTERISTIC



INPUT/OUTPUT FUNCTIONS (continued)

For analog sensing input 12 should be grounded and a positive signal, with respect to ground, Pin 8, applied to Pin 4.

RAMP GENERATOR — (Pins 5, 6, 7) (refer to Figure 2). A preset voltage applied to Pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to Pin 5. The voltage applied to Pin 6 will determine how much of the full ramp, shown in Figure 2, is used. The charging current passing through Pin 7 to the ramp generator timing capacitor determines the ramp slope.

When Pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to Pin 7, regardless of the voltage of Pin 5. This represents the high acceleration period shown in Figure 2.

If the preset voltage applied to Pin 5 is equal to or less than the voltage on Pin 6 the charging current will be 1.2 mA, or high acceleration.

If the preset voltage applied to Pin 5 is between $V_{Pin\ 6}$ and 2 $V_{Pin\ 6}$ the charging current is 1.2 mA (high acceleration) until the voltage at the reference input of the control amplifier equals $V_{Pin\ 6}$. At this point the charging current will switch to 5.0 μA; i.e. low acceleration.

If the preset voltage applied to Pin 5 is greater than 2 $V_{Pin\ 6}$ the charging current will be 1.2 mA (high acceleration) until the control amplifier's reference input reaches $V_{Pin\ 6}$ when it will switch to 5.0 μA (low acceleration) until 2 $V_{Pin\ 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value of $V_{Pin\ 5}$ is reached.

Should the preset voltage at Pin 5 fall below 80 mV, the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one preset value to another.

As long as the voltages applied at Pins 5 and 6 are derived from the internal voltage regulator, they and the voltage on Pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

CURRENT LIMITER — (Pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a preset current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and negative peaks through the shunt resistor (0.05 Ω in Figure 4).

The negative peaks of this current are fed through a resistor to Pin 3 where they are compared with a preset current defined by a resistor between Pin 3 and $+V_{CC}$. An excessive shunt current will try to pull Pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{Pin\ 7}$, consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to Pin 3 fix the level at which the limiter becomes active, while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an overcurrent condition.

CONTROL AMPLIFIER — (Pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

TRIGGER PULSE GENERATOR — (Pins 1, 2, 13, 14, 15). This circuit performs four functions:

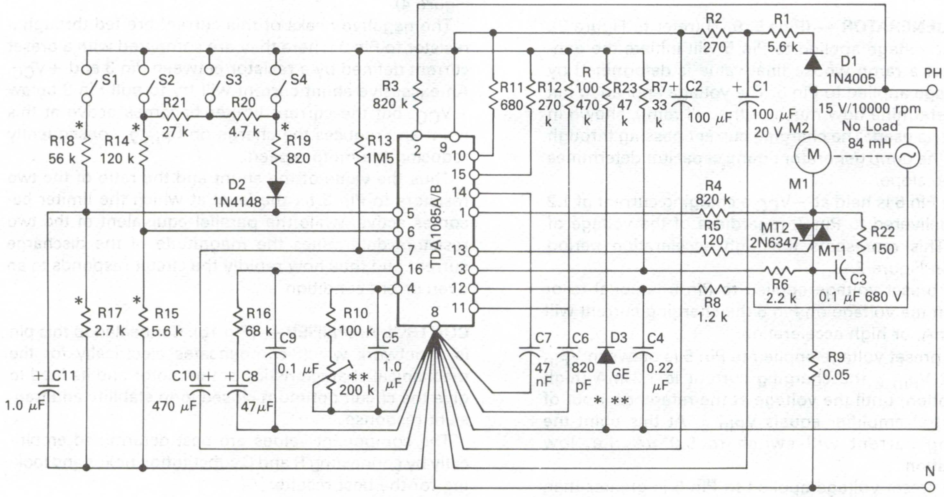
1. The conversion of the control amplifier's dc output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

$R_{Pin\ 15}$ and $C_{Pin\ 14}$ fix the sawtooth while $C_{Pin\ 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

TYPICAL APPLICATIONS

FIGURE 4 — CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING


S1
S2
S3
S4
R21 27 k
R20 4.7 k
R3 820 k
R18 56 k
R14 120 k
R19 820
D2 1N4148
R13 1M5
R11 680
R12 270 k
R 100 k
R 470 k
R23 47 k
R7 33 k
C2 100 μF
C1 100 μF 20 V
R2 270
R1 5.6 k
D1 1N4005
PH
15 V/10000 rpm
No Load
84 mH
M
M2
M1
R4 820 k
R5 120
MT2
2N6347
MT1
R22 150
R6 2.2 k
C3 0.1 μF 680 V
R8 1.2 k
R9 0.05
N
TDA1085A/B
2
9
10
15
14
1
5
6
7
13
16
3
4
12
8
11
R17 2.7 k
R15 5.6 k
R16 68 k
R10 100 k
C9 0.1 μF
C5 1.0 μF
200 k
C11 1.0 μF
C10 470 μF
C8 47 μF
C7 47 nF
C6 820 pF
D3 GE
C4 0.22 μF
*
**
***

* Chosen to suit the speeds required

** Adjust for the highest speed

*** Required only with 'A' suffix device

Speed Control Resistor Network Equations

R17	=	given
R18	=	$R17 \left(\frac{15.5\ V}{V_W} - 1\right)$
R19	=	$R17 \left(\frac{14.8\ V}{V_{spin\ 2}} - 1\right)$
R20	=	$R17 \left(\frac{14.8\ V}{V_{spin\ 1}} - 1\right) - R19$
R21	=	$R17 \left(\frac{14.8\ V}{k.V_W} - 1\right) - R19 - R20$
R15	=	$R21 \left(\frac{K.V_W}{15.5\ V\ (2\text{-}K)}\right)$
R14	=	$R15 \left(\frac{15.5\ V}{V_W} - 1\right)$

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{DIST}}{V_{WASH}} \leqslant 2 = K$$

	S1	S2	S3	S4	$V_{Pin\ 5}$	$V_{Pin\ 6}$
Wash	sc	oc	oc	oc	V_W	0
Distribute	oc	sc	oc	oc	KV_W	V_W
Spin 1	oc	oc	sc	oc	$>KV_W$	$\frac{K}{2}V_W$
Spin 2	oc	oc	oc	sc	$>>KV_W$	$\simeq\frac{K}{2}V_W$

sc = switch closed
oc = switch open

Note:
When changing from one speed to another $V_{Pin\ 5}$ must not be allowed to fall below 80 mV — otherwise the circuit will reset and restart from zero.

The component values given in Figure 4 correspond to:

V_W = 0.7 V
V_D = 1.13 V
$V_{spin\ 1}$ = 5.0 V
$V_{spin\ 2}$ = 11 V
K = 1.6

FIGURE 5 — OPEN LOOP, SOFT START — WITH PROGRAMMED TIME TO MAX. SPEED
($t = C_{Pin\ 7} \cdot 65 \times 10^5$)

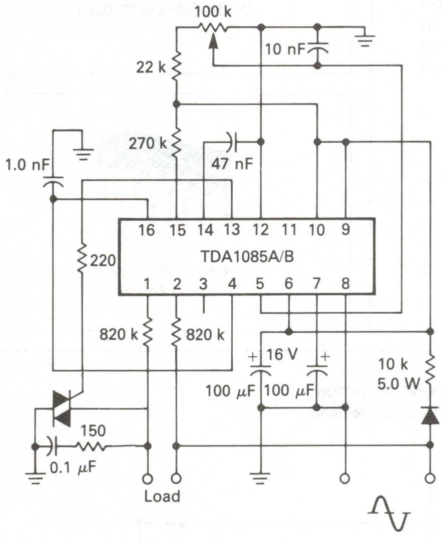
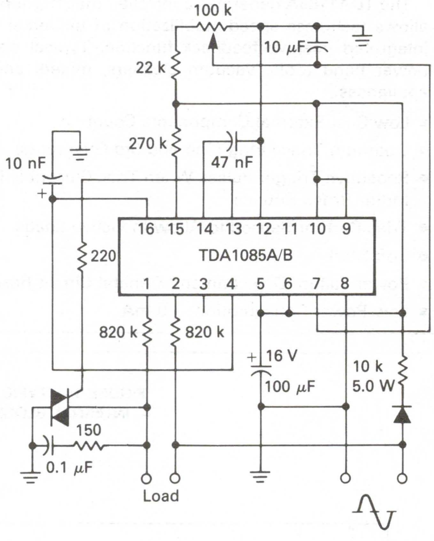

100 k
10 nF
22 k
270 k
47 nF
1.0 nF
16 15 14 13 12 11 10 9
TDA1085A/B
1 2 3 4 5 6 7 8
220
820 k
820 k
16 V
100 µF
100 µF
10 k
5.0 W
150
0.1 µF
Load

FIGURE 6 — OPEN LOOP, SOFT-START/SOFT-STOP, LIGHTING/INDUCTIVE LOAD CONTROLLER


100 k
10 µF
22 k
270 k
47 nF
10 nF
16 15 14 13 12 11 10 9
TDA1085A/B
1 2 3 4 5 6 7 8
220
820 k
820 k
16 V
100 µF
10 k
5.0 W
150
0.1 µF
Load

MOTOROLA

TDA1185A

Specifications and Applications Information

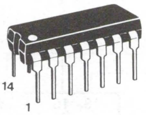
TRIAC PHASE ANGLE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

TRIAC PHASE ANGLE CONTROLLER

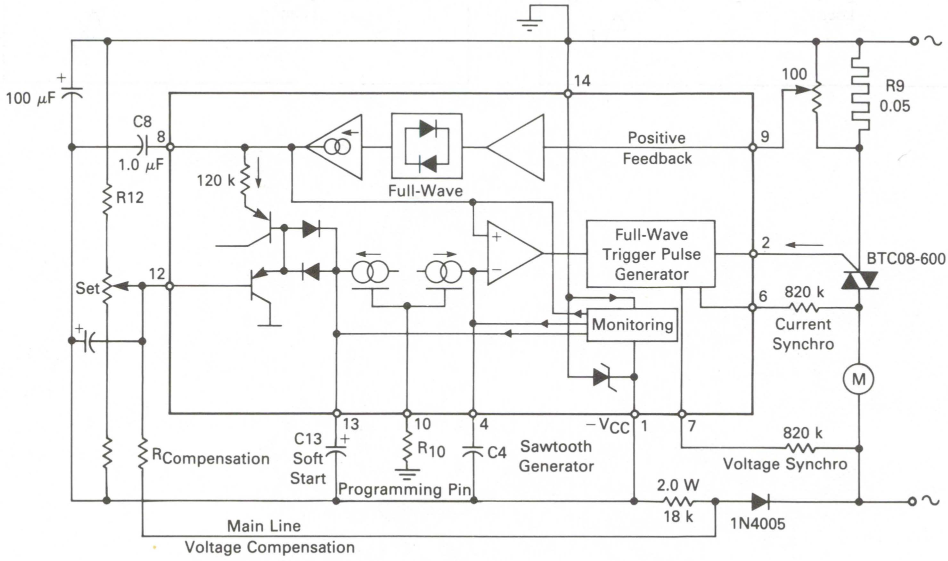
The TDA1185A generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers and other small appliances.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA



PLASTIC PACKAGE
CASE 646-05

FIGURE 1 — TYPICAL SYSTEM CONFIGURATION — INTERNAL BLOCK DIAGRAM/PIN ASSIGNMENT


100 μF
C8
8
1.0 μF
R12
120 k
Full-Wave
Positive Feedback
9
14
100
R9
0.05
Full-Wave Trigger Pulse Generator
2
BTC08-600
6
820 k
Current Synchro
Monitoring
Set
12
M
13
10
4
−VCC
1
7
820 k
Voltage Synchro
RCompensation
C13 Soft Start
R10
C4
Sawtooth Generator
Programming Pin
2.0 W
18 k
1N4005
Main Line Voltage Compensation

MAXIMUM RATINGS (Voltages are referred to Pin 14 (ground) unless otherwise noted)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin	V_{Pin}		Volt
Pins 3-5-11 (not connected)		−20 to +20	
Pins 4-8-13		$-V_{CC}$ to 0	
Pin 2		−3.0 to +3.0	
Maximum Positive Voltage (No minimum value allowed; see current ratings)	$V_{Pin\ 12}$ $V_{Pin\ 1}$	+0 +0.5	
Maximum Current per Listed Pin	I_{Pin}		
Pin 1		±20	mA
Pins 6 and 7		±2.0	mA
Pin 9		±0.5	mA
Pin 10		±300	µA
Pin 12		−500	µA
Maximum Power Dissipation (at T_A = 25°C)	P_D	250	mW
Maximum Junction to Ambient Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C) Voltages are related to Pin 14 (ground)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA	$-V_{CC}$	−9.6	−8.6	−7.6	Volt
Circuit Current Consumption, $I_{Pin\ 1}$ $V_{Pin\ 1}$ = −6.0 V, $I_{Pin\ 2}$ = 0 V	$-I_{CC}$	−2.0	−1.0	—	mA
Monitoring Enable Supply Voltage (V_{EN})	$V_{Pin\ 1EN}$	V_{CC} + 0.2	—	V_{CC} +0.5	Volt
Monitoring Disable Supply Voltage (V_{DIS})	$V_{Pin\ 1DIS}$	V_{EN} + 0.12	—	V_{EN} + 0.3	
Phase Set					
Control Voltage Static Offset $V_{Pin\ 8} - V_{Pin\ 12}$	V_{off}	1.2	—	1.8	Volt
Pin 12 Input Bias Current	$I_{Pin\ 12}$	−200	—	0	nA
$V_{Pin\ 4} - V_{Pin\ 12}$ Residual Offset		—	180	—	mV
Soft Start	$I_{Pin\ 13}$	−17	−14	−11	µA
Capacitor Charging Current					
$R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from $-V_{CC}$ to −3.0 Volts					
Sawtooth Generator					
Sawtooth Capacitor Discharge Current					
R_{10} = 100 kΩ $V_{Pin\ 4}$ from −2.0 to −6.0 Volts	$I_{Pin\ 4}$	67	70	73	µA
Capacitor Charging Current	$I_{Pin\ 4}$	−10	—	−1.5	mA
Sawtooth "High" Voltage ($V_{Pin\ 4}$)	V_{HTH}	−2.5	−1.6	−1.0	Volt
Sawtooth Minimum "Low" Voltage ($V_{Pin\ 4}$) referred to Pin 1	V_{LTH}	—	+1.5	—	Volt
Positive Feedback					
Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0	$I_{Pin\ 9}$	—	2 x $I_{Pin\ 10}$	—	
Programming Pin Voltage Related to Pin 1	$V_{Pin\ 10}$	1	1.25	1.5	Volt
Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$					
R_{10} = 100 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	75	—	
R_{10} = 270 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	$Z_{Pin\ 8}$	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) $V_{Pin\ 2}$ = 0 V	$I_{Pin\ 2}$	60	—	80	mA
Output Leakage Current $V_{Pin\ 2}$ = +2.0 V		—	—	4.0	µA
Output Pulse Width					
C_1 = 47 nF R_{10} = 270 kΩ	tp	—	55	—	µs
Output Pulse Repetition Period					
C_1 = 47 nF R_{10} = 270 kΩ	t	—	420	—	µs
Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$	I_{SYNC}	−40	—	+40	µA

CIRCUIT DESCRIPTION

The TDA1185A generates trigger pulses for triac control of power into an ac load. The firing angle is determined by generating a ramp voltage synchronized to the ac line half cycle and compared to an external set voltage representing the conduction angle.

Gate pulses are negative (sink current) and thus the triac is driven in its most effective quadrants (Q2–Q3).

If the load is a Universal motor (the speed of which is decreasing as torque increases), the TDA1185A allows to increase the firing angle proportionally to the motor current, sensed by a low value series resistor.

Notice: Perfect motor speed compensation cannot be provided by open-loop systems, since no negative feedback is used. Due to the low cost of tacholess systems, the TDA1185A is the optimum solution for applications tolerating 5% motor speed variations.

Nevertheless by accurate circuit design, these variations can be reduced down to 2% from no load to full load conditions.

CIRCUIT FUNCTIONS

DC POWER SUPPLY — DC power is directly derived from the ac line through a 2.0 watt, 18 kΩ resistor, rectifier and filtering capacitor circuit. The latter being directly connected to the dropping resistor protects the whole IC from any ac line overvoltage. The $-V_{CC}$ voltage is internally regulated by an integrated zener. Referred to Pin 14 (ground) the power supply voltage is negative (−8.6 volts). The TDA1185A internal consumption is 1.0 mA.

TRIGGER PULSE GENERATOR — It delivers a 60 mA minimum pulse current (sink) through an internally short-circuit protected output. Pulse width is roughly proportional to $R_{10} \cdot C_4$ and is repeated every 420 μs if triac fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect of the voltage: Pin 6 delays the triggering pulse up to the moment the triac is off, in order to prevent erratic power control (see Figure 2). The logic structure guarantees full-wave triac operation.

SAWTOOTH GENERATOR — A constant current generator discharges the capacitor C_4, the voltage of which is the sawtooth signal synchronized with main line. Pin 4 voltage is reset to −1.6 volt at every ac line zero crossing (see Figure 3). The constant current generator is externally programmable by an external resistor connected to Pin 10:

$$I_{Pin\ 4} = I_{Pin\ 10}\ 10 \pm 5\%$$

$$I_{Pin\ 10} = \frac{-V_{CC} \pm 1.25}{R_{10}}$$

MAIN COMPARATOR — Its role is to determine the trigger pulse time which occurs as the sawtooth voltage equals set voltage. Fixed set values lead to a constant triac conduction angle unless positive current feedback is connected or soft start capacitor is not charged.

SOFT START — The TDA1185A allows the user to avoid any abrupt inrush current in the load, for various purposes: motor soft start, protection of high performance bulbs or ac line minimum disturbances.

The firing angle is established from zero to the set value according to a voltage ramp generated by a constant current delivered to capacitor C_{13}. The constant current value is:

$$I_{Pin\ 13} = 0.2 \times I_{Pin\ 10} \pm 10\%$$

The voltage ramp lasts as long as $V_{Pin\ 13}$ is lower than $V_{Pin\ 12}$. $V_{Pin\ 13}$ reset voltage is $-V_{CC}$. See Figure 4.

Notice. Universal motors do not have any motion effect as long as a minimum conduction angle is not reached. The time the voltage ramp reaches this threshold value is considered as "dead" time and can be eliminated by a series resistor at Pin 13. The voltage drop developed by $I_{Pin\ 13}$ makes the firing angle immediately reach the threshold value and have the soft start function without dead time. See Figure 5.

POSITIVE CURRENT FEEDBACK — The Universal motor speed drops as load increases. To maintain it as stable as possible, the triac firing angle must be increased. For this purpose the Pin 9 input senses the motor current as a voltage developed in a low resistor value, R_g, amplifies, rectifies and adds it to Pin 12 set voltage. The transfer function $\Delta V_{Pin\ 8} = f(\Delta V_{Pin\ 9})$ and is represented on Figure 6.

The gain in the linear region is dependent on R_{10}. The voltage transferred to Pin 8 is proportional to the average value of the motor current and is very close to its RMS value (as motor current is not far from a sine wave). This averaging effect is represented in Figure 7.

For large amplitude Pin 9 signals, the am function presents a saturation effect which limits the maximum firing angle increase. Figure 8 presents this aspect as well as the total Pin 8 voltage which is:

$$V_{Pin\ 8} = V_{Pin\ 12} + f(|V_{Pin\ 9}|\ R_{10}) + \text{offset}$$

The offset is the addition of two PN Junctions and is compensated with respect to $V_{Pin\ 4}$ (sawtooth) by additional diodes within the main comparator (See Figure 10).

The effect of positive feedback is described per Figure 9.

MONITORING — A central logic block performs the following functions: — ENABLE/DISABLE of the IC with respect to power supply voltage. Under DISABLE conditions, Pins 4, 8, 12, and 13 are forced to appropriate voltages to prepare for the next reset (See Figure 10).

APPLICATION CONSIDERATIONS

PINS CHARACTERISTICS — Figure 10 describes more details in the internal IC layout and defines the pin characteristics. Pin 9 has a low internal impedance and requires a maximum 100 Ω trimmer on R_g to adjust reaction ratio. Pin 8 must always be connected to $-V_{CC}$ through a filtering capacitor.

TEMPERATURE EFFECTS — The TDA1185A has very efficient internal temperature compensation. If positive current feedback is not connected, the RMS power delivered to the load is stabilized within ±0.2% over a temperature range of +20 to +70°C. The positive feedback introduces in the same temperature range, a drift of 250 mV on $V_{Pin\ 8}$; this slight firing angle increase may be successfully used to compensate a motor ohmic resistance increase with temperature as well.

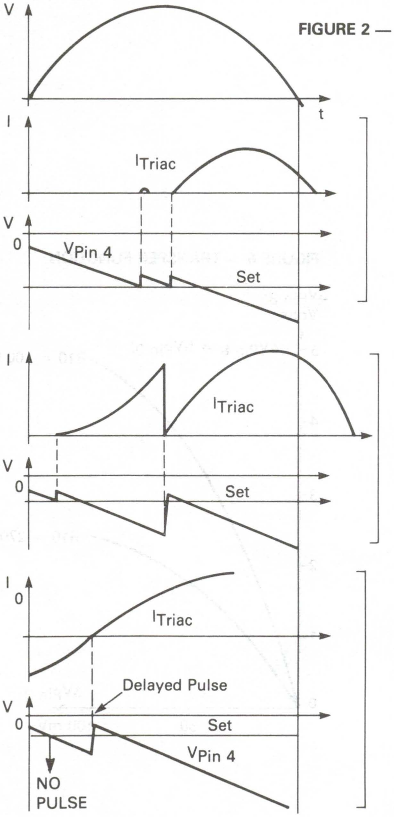
MAIN LINE VOLTAGE COMPENSATION — As the firing angle is independent of main line voltage, any change in the latter (usually ±15%) induces a very large power variation to the load. An external compensation must be used, introducing a $V_{Pin\ 12}$ decrease as V_{mains} increases. An inexpensive resistor R_{COMP}, connected to the rectifier anode and to Pin 12 performs this role and its value depends on $V_{Pin\ 12}$, $R_{10}C_4$, R_{12}. R_{COMP} can be empirically determined without difficulty under no load conditions.

FIRING ANGLE DYNAMIC — With purely resistive loads, the effective RMS applied power to the load is an increasing function of the firing angle (per Figure 11). We notice the fact that a firing angle of 150° provides 97% of the full power corresponding to 180°.

With inductive loads, as currents lag with respect to Voltage, 100% power corresponds to a firing angle which is smaller than 180°.

These considerations will simplify positive feedback design if maximum firing angle is accepted to be within 150–160°.

FIGURE 2 — MULTIPULSE GENERATION DELAYED PULSE



The triac failed to latch at the first pulse. Successive pulses are generated up to the moment latching oocurs.

The triac turned off due to brush bounce, a new pulse is immediately delivered.

Approaching full conduction, a pulse would occur when the triac still carries current; the pulse is delayed until the triac turns off.

FIGURE 3 — TRIGGERING PULSE TIMING

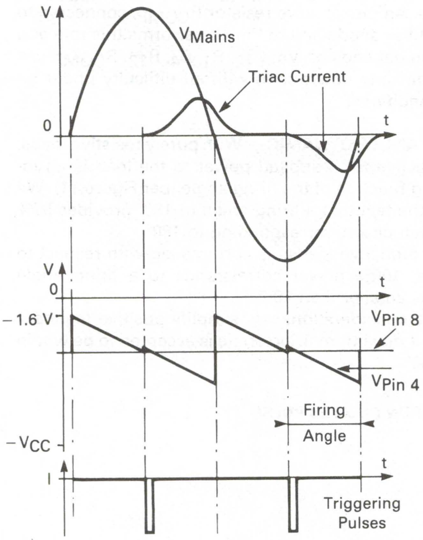

V
VMains
Triac Current
0
t
V
0
t
−1.6 V
VPin 8
VPin 4
Firing
Angle
−VCC
I
t
Triggering
Pulses

FIGURE 4 — SOFT START

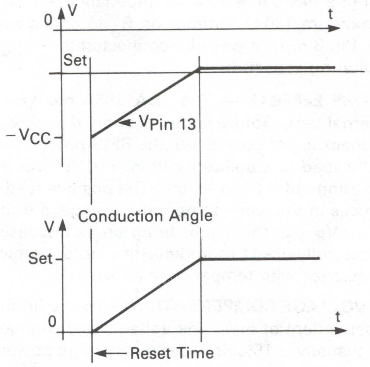

0
V
t
Set
VPin 13
−VCC
Conduction Angle
V
Set
0
t
Reset Time

FIGURE 5 — SOFT START WITHOUT DEAD TIME

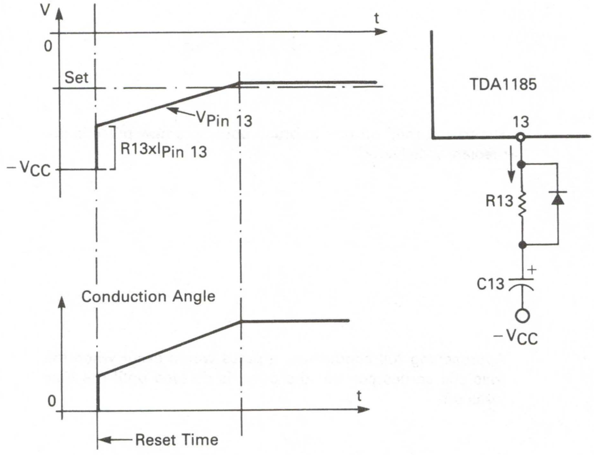

V
t
0
Set
VPin 13
R13xIPin 13
−VCC
Conduction Angle
0
t
Reset Time
TDA1185
13
R13
C13
+
−VCC

FIGURE 6 — TRANSFER FUNCTION

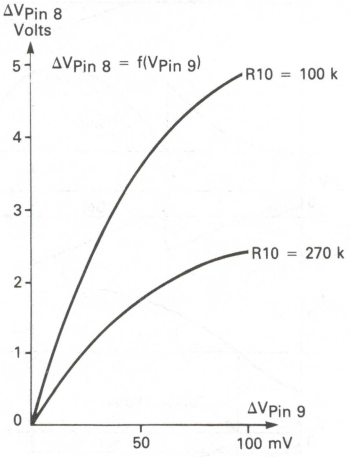


FIGURE 7 — AVERAGING EFFECT OF TRANSFER FUNCTION

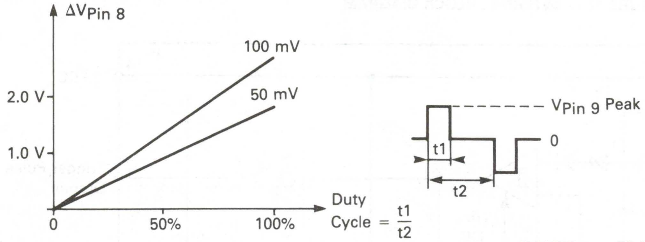


FIGURE 8 — TRANSFER FUNCTION (Pin 8/Pin 9)

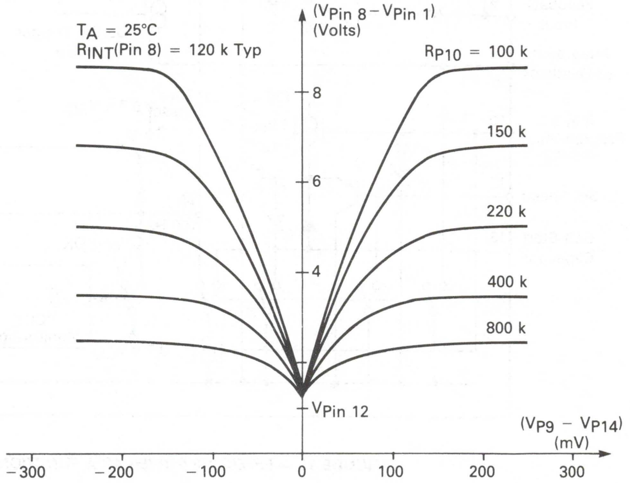


FIGURE 9 — POSITIVE FEEDBACK EFFECT
offset Voltages have been neglected

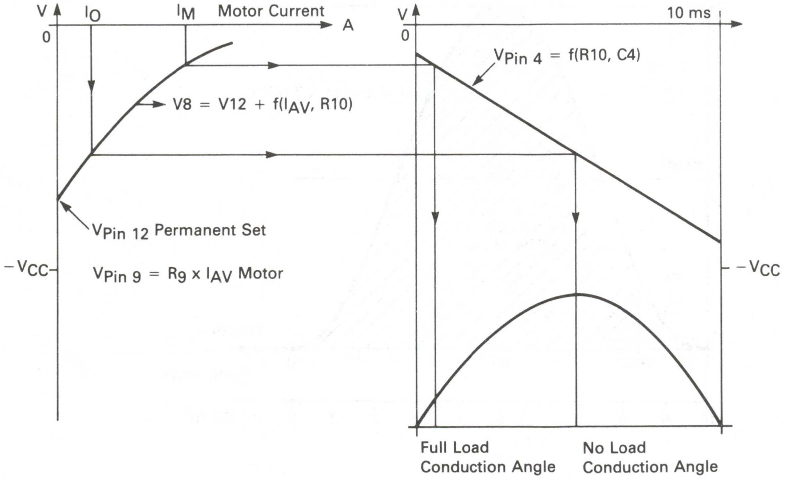

V
0
IO
IM
Motor Current
A
V8 = V12 + f(IAV, R10)
VPin 12 Permanent Set
−VCC
VPin 9 = R9 x IAV Motor
V
0
10 ms
VPin 4 = f(R10, C4)
−VCC
Full Load
Conduction Angle
No Load
Conduction Angle

FIGURE 10 — INTERNAL BLOCK DIAGRAM

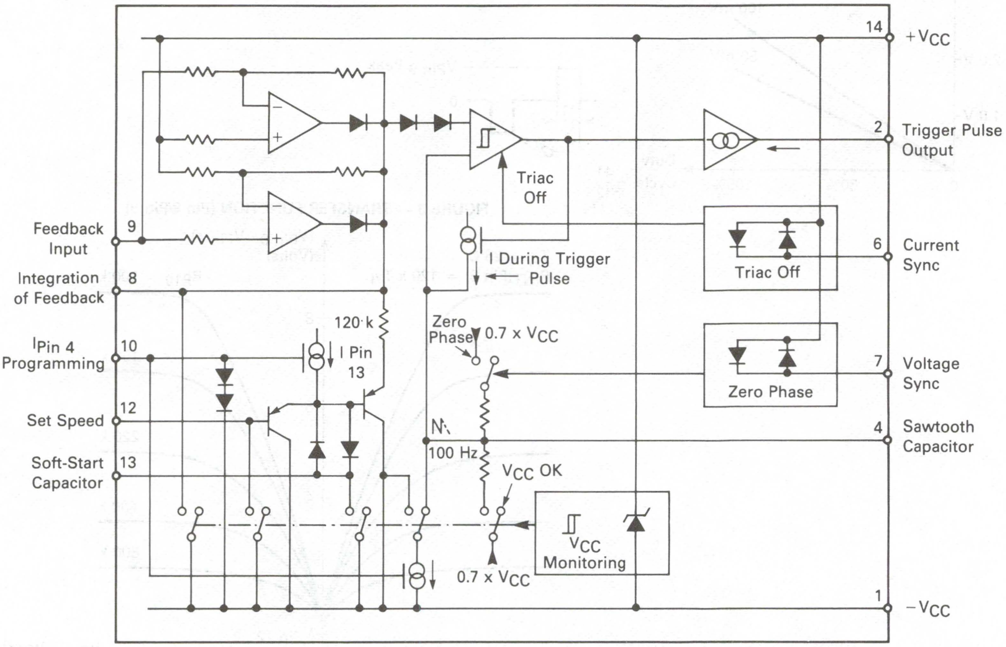
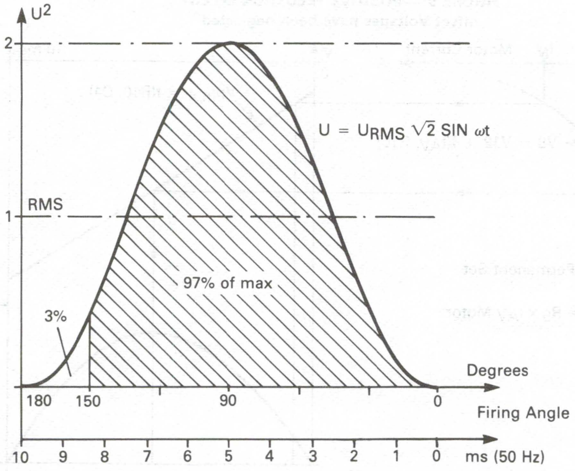

14
+VCC
2
Trigger Pulse Output
Triac Off
I During Trigger Pulse
6
Current Sync
Triac Off
7
Voltage Sync
Zero Phase
4
Sawtooth Capacitor
Feedback Input
9
Integration of Feedback
8
IPin 4 Programming
10
Set Speed
12
Soft-Start Capacitor
13
120 k
I Pin 13
Zero Phase
0.7 x VCC
N
100 Hz
VCC OK
VCC Monitoring
0.7 x VCC
1
−VCC

FIGURE 11 — EFFECTIVE POWER AS A FUNCTION OF FIRING ANGLE



MOTOROLA

TDA1285A

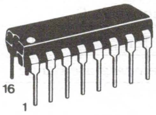
MOTOR SPEED CONTROLLER

The TDA1285A has all the necessary functions for the speed control of universal motors in a closed loop configuration. Directly driven from the ac line, the circuits generate a phase angle varied trigger pulse to the control triac. In addition it provides the following features:

- Full Wave Triac Drive
- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection
- Motor Current Limitation
- Controlled Motor Starting Acceleration
- Typical 1–2% Motor Speed Variation Within All Temperature and Load Ranges

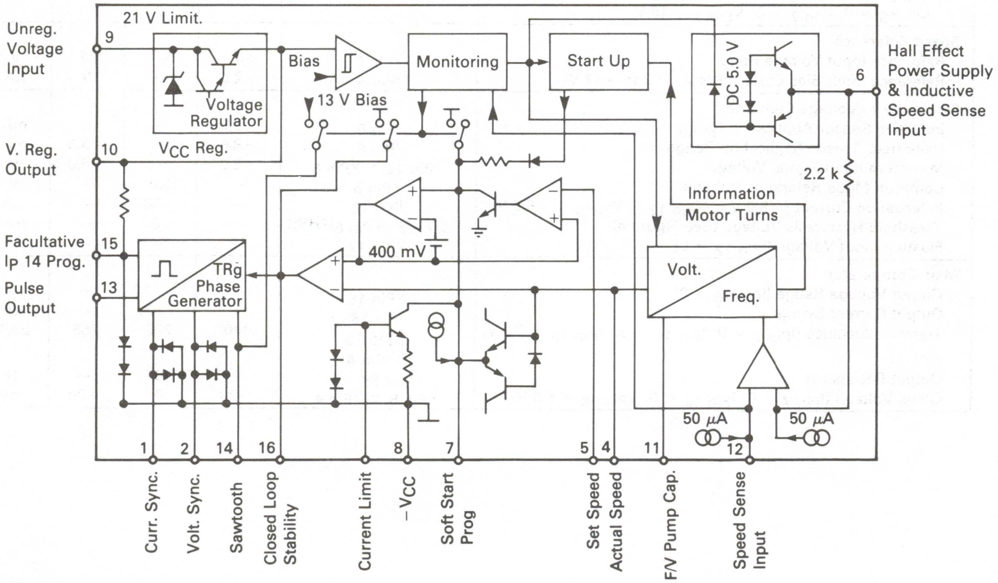
UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648-05

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT


Unreg. Voltage Input
9
21 V Limit.
Voltage Regulator
VCC Reg.
Bias
13 V Bias
Monitoring
Start Up
DC 5.0 V
6
Hall Effect Power Supply & Inductive Speed Sense Input
2.2 k
V. Reg. Output
10
400 mV
Information Motor Turns
Facultative Ip 14 Prog.
15
Pulse Output
13
TRg Phase Generator
Volt.
Freq.
50 µA
50 µA
1
2
14
16
8
7
5
4
11
12
Curr. Sync.
Volt. Sync.
Sawtooth
Closed Loop Stability
Current Limit
–VCC
Soft Start Prog
Set Speed
Actual Speed
F/V Pump Cap.
Speed Sense Input

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Current	$I_{Pin\ 9\ RMS}$	20	mA
Peak Supply Current, t < 250 μs	$I_{Pin\ 9\ PEAK}$	200	mA
Regulated Supply Current Drain	$I_{Pin\ 10}$	10	mA
Peak ac Synchronization Input Currents	$I_{Pin\ 1}$ $I_{Pin\ 2}$	±2.0 ±2.0	mA mA
Current Drain per Listed Pin	I_3	−1.0 +2.0	mA
	I_{12}	+500 −4.0	μA mA
	I_6	−7.0 +1.0	mA
	I_{15}	+1.0	mA
Pin 3 Reverse Voltage	$V_{Pin\ 3}$	−5.0	V
Power Dissipation (T_A = 25°C) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/°C
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, $I_{Pin\ 9}$ = 20 mA	$V_{Pin\ 9}$	19	20.5	23	V
Regulated Supply Voltage (Pin 10) $I_{Pin\ 10}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 15}$ = 0 $I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V	V_{CC}	13.6	14.6	15.6	V
Current Consumption ($I_{Pin\ 9}$) $I_{Pin\ 6}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 10}$ = 0 $I_{Pin\ 15}$ = 0; $I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V	I_{CC}	—	4.5	7.0	mA
Speed Reference					
Reference Input Voltage Range	$V_{Pin\ 5}$	0	—	12	V
Reference Input Bias Current ($V_{Pin\ 5}$: 0 to +12 V)	$I_{Pin\ 5}$	−2.0	—	0	μA
Frequency to Voltage Converter					
Inductive Sensor Application Range	$I_{Pin\ 6}$	−2.5	—	0	mA
Hall-Effect Sensor Application Range	$I_{Pin\ 6}$	−8.0	—	−3.5	mA
Maximum Input Signal Voltage	$V_{Pin\ 12} - V_{Pin\ 6}$	−5.0	—	+5.0	V
Common-Mode Reference Voltage	$V_{Pin\ 6}$	—	5.0	—	V
Polarization Current (−5.0 V < $V_{Pin\ 12} - V_{Pin\ 6}$ < +5.0 V)	$I_{Pin\ 12}$	—	−50	—	μA
Threshold Hysteresis Voltage (See Figure 4)	$(V_{Sensor} - V_{Pin\ 6})_{THRS}$	—	±60	—	mV
Floating Input Voltage ($I_{Pin\ 12}$ = 0)	$V_{Pin\ 12}$	12	—	—	V
Main Comparator					
Output Voltage Range ($I_{Pin\ 16}$ = 0)	$V_{Pin\ 16}$	—	0; +12	—	V
Output Current Swing	$I_{Pin\ 16}$	—	±100	—	μA
Transconductance ($I_{Pin\ 7}$ = 0; $I_{Pin\ 10}$ = 0; $V_{Pin\ 16}$ = 5.2 V)	$\frac{\Delta I_{Pin\ 16}}{\Delta V_{Pin\ 4}}$	140	205	265	μA/V
Output Resistance	$R_{out\ Pin\ 16}$	—	10^6	—	Ω
Offset Voltage ($I_{Pin\ 7}$ = 0; $I_{Pin\ 16}$ = 0; $V_{Pin\ 16}$ = 5.0 V)	$V_{Pin\ 5} - V_{Pin\ 4}$	−20	0	+20	mV

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Limitation					
Detection Level	$V_{Pin\ 3\ Min.}$	—	0.65	—	V
Clamping Voltage Level	$V_{Pin\ 3\ CLAMP}$	—	1.3	—	V
Output Discharge Current	I_{DL7}	—	0.5	—	mA
Saturation Resistance	$R_{sat\ Pin\ 7}$	—	1.6	—	kΩ
Start-up					
Maximum Start-up Voltage ($I_{Pin\ 7} = 0$)	$V_{Pin\ 7}$	—	4.5	—	V
Start-up Current (until motor turns) ($_{Pin\ 7} = 0$)	$I_{Pin\ 7}$	—	−1.0	—	mA
Soft-Start		—		—	μA
Acceleration Charging Current	$I_{Pin\ 7}$		−8.0		
Trigger Pulse Generator					
Trigger Pulse Width*	tp	—	100	—	μs
Trigger Pulse Repetition Period*	t	—	600	—	μs
Output Pulse Current ($V_{Pin\ 13} = 1.0$ V)	$I_{Pin\ 13}$	−70	—	−65	mA
Output Leakage Current ($V_{Pin\ 13} = -2.0$ V)	$I_{o\ Pin\ 13}$	—	—	10	μA
Current Synchronization Threshold Levels (Pin 1 and Pin 2)	I_{Thrs}	—	±80	—	μA
Sawtooth Current Generator	$I_{Pin\ 14}$	—	−65	—	μA
Pin 15 Voltage ($I_{Pin\ 15} = 0$)	$V_{Pin\ 15}$	—	1.3	—	Volt

* These figures apply for the application shown in this data sheet.

CIRCUIT DESCRIPTION

The TDA1285A generates trigger pulses for a triac controlling the power into an ac motor connected to mains. The firing angle of the triac is determined by comparison between a sawtooth signal (mains synchronized) and the main internal comparator signal. The latter is the difference between a set voltage (externally adjustable) representing the reference speed and the actual motor speed issued from an external sensor and converted by an internal frequency to voltage converter. This sensor may be inductive (tachometer) or Hall-effect. Other functions are also provided by the TDA1285A.

KEY CIRCUIT FUNCTIONS

DC POWER SUPPLY

DC Power is directly derived from the ac line by a low cost resistor-rectifier-capacitor circuit. The voltage on Pin 9 is Zener protected. The voltage on Pin 10 is fully regulated by a series ballast regulator, but is not self-limiting. Special provisions for Hall-effect sensor power are included.

TACHOMETER INPUT (Pins 6 and 12)

The maximum allowable voltage swing is −5.0 to +5.0 V. Circuit continuity is permanently checked by the monitor.

HALL-EFFECT INPUT (Pins 6 and 12)

When $I_{Pin\ 6}$ exceeds 3.0 mA, the circuit detects the use of a Hall-effect sensor and thus sensor circuit continuity is not checked (an open circuit would provide full triac conduction angle).

FREQUENCY TO VOLTAGE CONVERTER

This circuit converts the tachometer input frequency into a proportional voltage on Pin 4 (eventually usable for any feedback). Particular care must be devoted to the conversion ratio of the F/V converter which is under the user control. In effect, it depends on the values of the C_{11} capacitor and on tachometer frequency f(Hz).

$$V_{Pin\ 4} = 1.410 \times 10^{-10} \times C_{11}\ (pF) \times R_4 \times F(Hz) \times (1 \pm 0.15)$$

$V_{Pin\ 4}$ corresponding to maximum allowed motor speed must be chosen as close as possible to 12 V in order to minimize noise disturbance down to a negligible level.

MAIN COMPARATOR

Its role is to amplify the signal error. Negative feedback from the output (Pin 16) to the input may be used to reduce the closed loop gain of the system and increase stability.

SOFT START (Pin 7)

Set speed input (Pin 5) is overruled by similar data from Pin 7 as long as $V_{Pin\ 7}$ is smaller than $V_{Pin\ 5}$ + 400 mV (Typ). An internal 8.0 μA current source allows an external capacitor, C_7 to be charged slowly and thus lets the ac motor soft start (Figure 2). Pin 4 offset may be set appropriately by an external resistor (R_1 = 1 MΩ). Notice that R_1 may affect F/V conversion ratio. An external 10 nF capacitor on Pin 5 reduces noise sensitivity.

START-UP CIRCUIT

From the moment power is applied to the circuit (or the circuit is enabled by Monitoring) to the moment a speed input signal is detected, C_7 is charged at a high current level (typically 1.0 mA). Detection of the first tachometer input resets the Pin 7 current to its nominal value (8.0 μA). The result of such a circuit is to start the acceleration ramp at the moment the motor starts to turn, avoiding any dead time (see Figure 2). When the motor is cycled on and off in close succession, the acceleration ramp is started immediately without waiting for the motor to stop.

MOTOR CURRENT LIMITATION (Pin 3)

The motor current is sensed as a voltage developed across a resistor (R_3) in series with the triac. The limiter acts on positive peak values of $R_3 \times I$ filtered by a 22 k and 0.1 μF, RC network (Figure 7). The motor current is reduced, decreasing its speed reference by discharging C_7 until current limit equilibrium is reached (see Figure 3).

TRIGGER PULSE GENERATOR

It delivers a 65 mA min. current pulse to the triac gate and repeats it if the triac fails to latch or if brush bounce has switched it off (Figure 6). Current and voltage detection through the triac are performed by Pins 1 and 2, delaying the trigger pulse until the triac current collapses. The pulse time is determined by the comparison of a sawtooth signal (available at Pin 14 and synchronous with line voltage) and the error signal directly supplied by the comparator.

Sawtooth slope is determined by the external capacitor C_{14}. Under these conditions pulse width is typically 100 μs (Figure 5).

MONITORING

This is an internal function, disabling the circuit when

— V_{CC} is insufficient

— Tachometer circuit is open and $I_{Pin\ 6} < |-3.0\ mA|$

FIGURE 2 — START-UP AND SOFT-START CIRCUIT ACTIONS

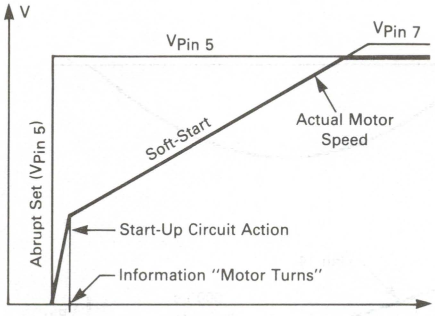
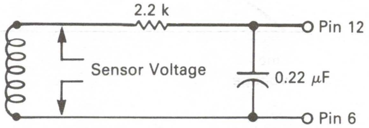

V
$V_{Pin\ 5}$
$V_{Pin\ 7}$
Actual Motor Speed
Soft-Start
Abrupt Set ($V_{Pin\ 5}$)
Start-Up Circuit Action
Information "Motor Turns"

FIGURE 4 — SENSOR VOLTAGE DEFINITION


2.2 k
Pin 12
Sensor Voltage
0.22 μF
Pin 6

2.2 k is a recommended value to balance the voltage offset caused by sensor continuity detection circuit.

FIGURE 5 — FIRING PULSE GENERATION

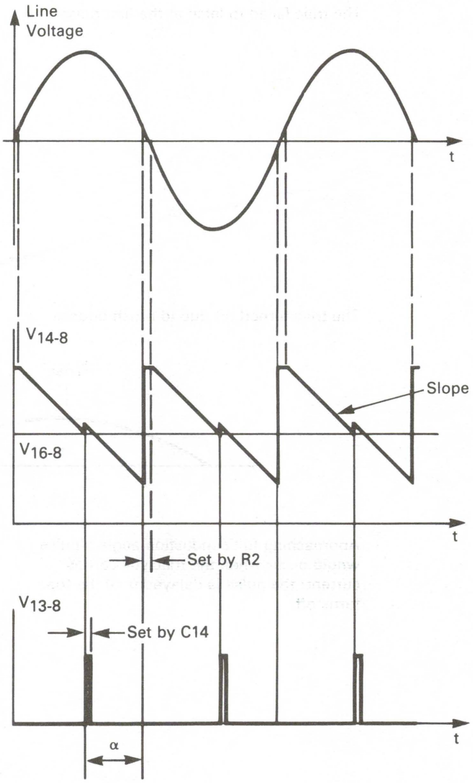

Line Voltage
t
V_{14-8}
Slope
V_{16-8}
t
Set by R2
V_{13-8}
Set by C14
t
α

FIGURE 3 — CURRENT LIMITATION

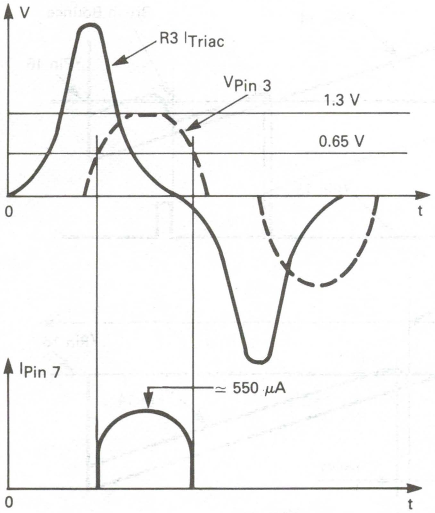
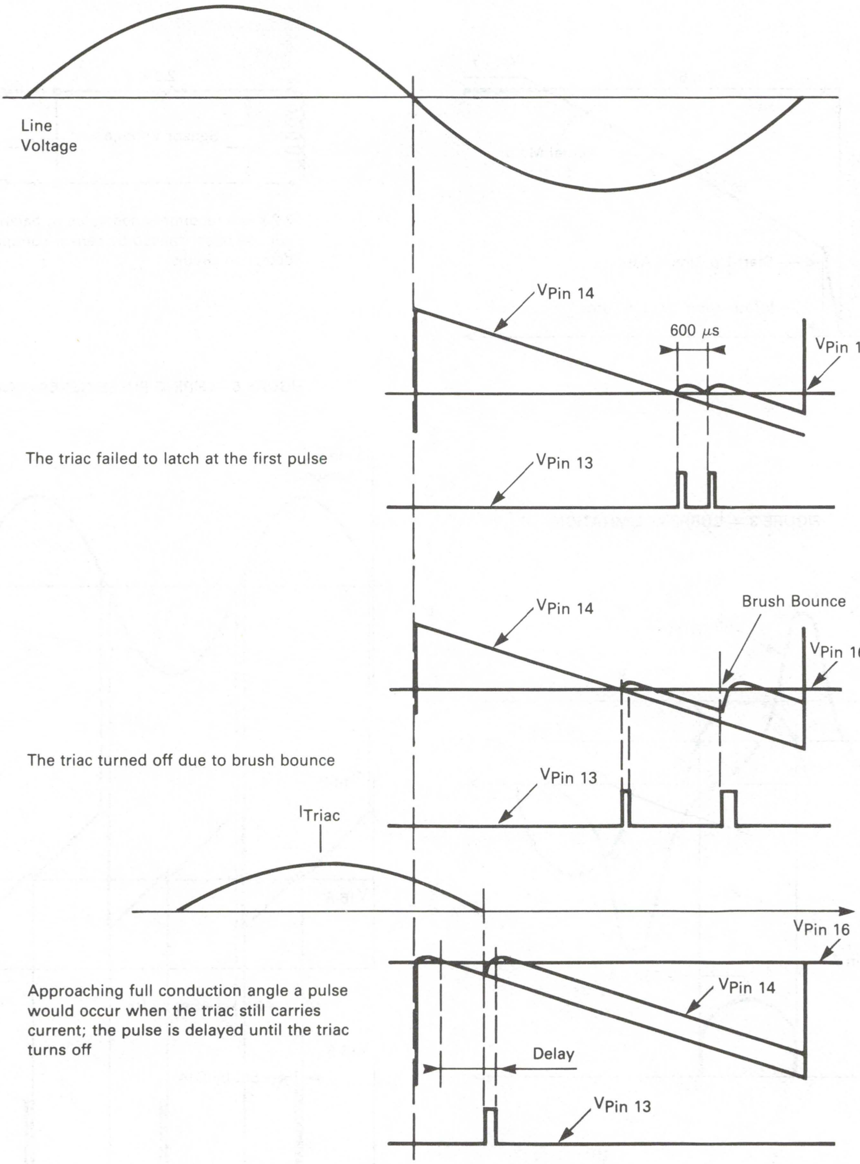

V
R3 I_{Triac}
$V_{Pin\ 3}$
1.3 V
0.65 V
0
t
$I_{Pin\ 7}$
≃ 550 μA
0
t

FIGURE 6 — MULTIPLE FIRING PULSE AND FIRING PULSE DELAY


Line
Voltage
$V_{Pin\ 14}$
600 μs
$V_{Pin\ 16}$
The triac failed to latch at the first pulse
$V_{Pin\ 13}$
$V_{Pin\ 14}$
Brush Bounce
$V_{Pin\ 16}$
The triac turned off due to brush bounce
$V_{Pin\ 13}$
I_{Triac}
$V_{Pin\ 16}$
$V_{Pin\ 14}$
Approaching full conduction angle a pulse would occur when the triac still carries current; the pulse is delayed until the triac turns off
Delay
$V_{Pin\ 13}$

TYPICAL APPLICATION CIRCUITS

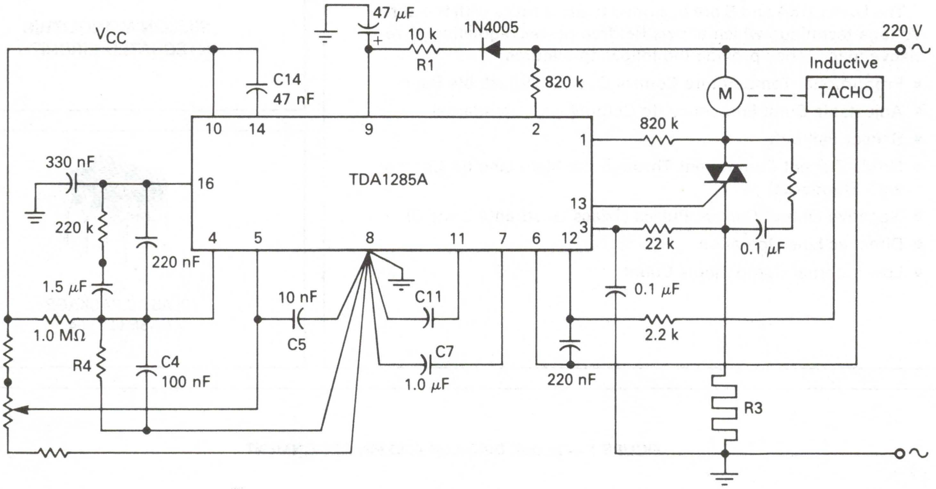
A motor control circuit using tachometer as speed sensor. It provides speed regulation as follows:

- ±1.0% from 20 to 70°C
- 1.0% in full load range.

It is strictly recommended to design the PC board in order to plug every connection to ground (Pin 8) directly and individually; otherwise, violent erratic currents may induce high level noise in the circuitry.

Motor will run full speed in case of tacho open circuit if a 47 k resistor is connncted permanently between Pins 6 and 12.

FIGURE 7 — MOTOR CONTROL CIRCUIT


VCC
47 µF
10 k
R1
1N4005
220 V
C14
47 nF
820 k
Inductive
M
TACHO
10
14
9
2
1
820 k
330 nF
16
TDA1285A
13
3
220 k
4
5
8
11
7
6
12
22 k
0.1 µF
220 nF
1.5 µF
10 nF
C11
0.1 µF
1.0 MΩ
C5
2.2 k
C7
R4
C4
100 nF
1.0 µF
220 nF
R3

NOTES:

Frequency to Voltage converter

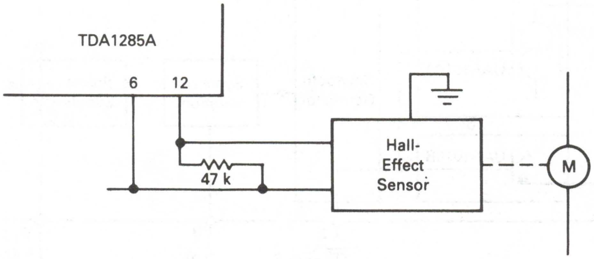
— Max. motor speed 30,000 rpm

— Tachogenerator 4 pairs of poles: max. frequency $= \frac{30,000}{60} \times 4 = 2$ kHz

— C11 = 680 pF. R4 adjusted to obtain $V_{Pin\ 4} = 12$ V at max. speed: 68 kΩ

— Power Supply
with $V_{mains} = 120$ Vac, $R_1 = 4.7$ kΩ. Perfect operation
will occur down to 80 Vac.

FIGURE 8 — CIRCUIT MODIFICATIONS TO CONNECT A HALL-EFFECT SENSOR


TDA1285A
6
12
47 k
Hall-
Effect
Sensor
M

MOTOROLA

UAA1016A
UAA1016B

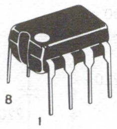
ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUITS

ZERO VOLTAGE CONTROLLER

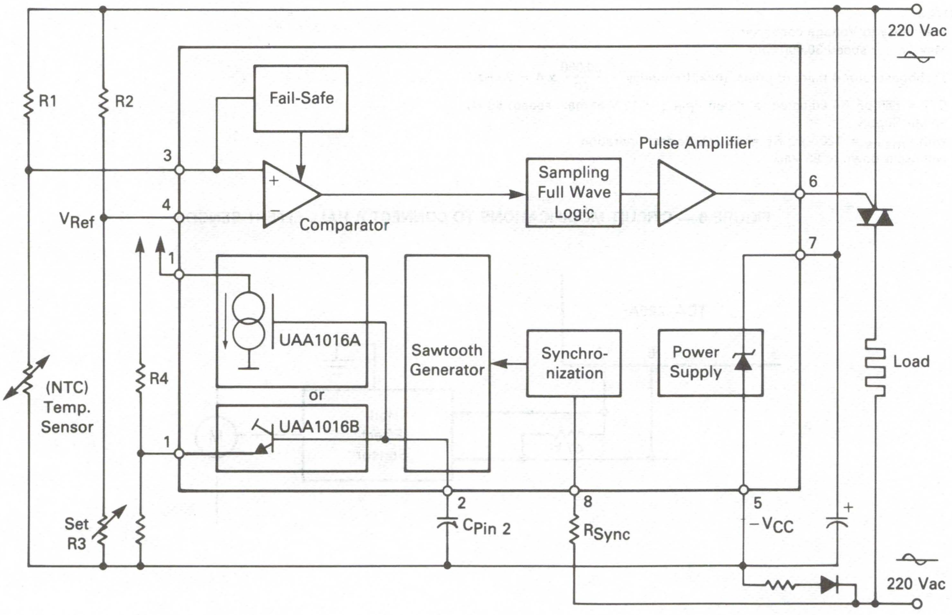
The UAA1016A and B are designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count



PLASTIC PACKAGE
CASE 626–04

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT


220 Vac
R1
R2
Fail-Safe
3
4
V_{Ref}
+
−
Comparator
Sampling Full Wave Logic
Pulse Amplifier
6
7
1
UAA1016A
or
UAA1016B
Sawtooth Generator
Synchro-nization
Power Supply
Load
(NTC) Temp. Sensor
R4
1
Set R3
2
$C_{Pin\ 2}$
8
R_{Sync}
5
$-V_{CC}$
+
220 Vac

MAXIMUM RATINGS (Voltages referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
ac Synchronization Current (Pin 8)	I_{syn}	3.0	mA (RMS)
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ +2.0; $-V_{CC}$	Volt
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation $T_A = 25°C$	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	−20 to +100	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Voltages referred to Pin 7 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	—	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) $I_{CC} = 2.0$ mA max	$-V_{CC}$	−9.6	−8.6	−7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from −1.0 to +1.0 Volt)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8} = 220\ k\Omega$, $V_{mains} = 220$ Vac, (Figures 4 and 5)	t_{p1} t_{p2}	58 160	60 220	120 320	μs
Comparator Input Offset Voltage ($V_{Pin\ 3} - V_{Pin\ 4}$)	V_{off}	−10	—	+10	mV
Comparator Common Mode Voltage Range	V_{CM}	$-V_{CC}+1$	—	−1.5	V
Input Bias Current (Pins 3 and 4)	I_{IB}	—	—	1.0	μA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6} = +2.0$ V	I_{outL}	—	—	10	μA
Fail-safe Threshold Voltage ($V_{Pin\ 3}$)	V_{FSTH}	—	−0.7	—	V
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	−20	−16	−12	μA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	—	6.4	—	mA
Sawtooth Pulse Length ($C_{Pin\ 2} = 1.0\ \mu F$)	t_{saw}	—	0.85	—	S
UAA1016A: Output Threshold Sawtooth Currents ($I_{Pin\ 1}$) ($V_{Pin\ 2} = -1.0$ V) $V_{Pin\ 2} = -V_{CC} + 1.25$ V	I_{TH1} I_{TH2}	— —	−15 −2.1	— —	μA
UAA1016B: Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	— —	−1.0 $-V_{CC}+1.25$	— —	V
Output Voltage Pin 1	$V_{Pin\ 1}$	—	$V_{Pin\ 2}-0.75$	—	V

CIRCUIT DESCRIPTION

The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync}. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{REF} corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA 1016 has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 2). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{Ref}. This deviation defines the temperature band allowing proportional power control (see Figure 3).

A fail-safe circuit inhibits output pulses when the sensor circuit has a fault (open or short circuit).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

KEY CIRCUIT FUNCTIONS DESCRIPTION

POWER SUPPLY — The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016A/B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 4 and 5 (Igt max. and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

COMPARATOR — When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{Ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 3). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV max) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 6. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typ. less than 100 ns).

SAWTOOTH GENERATOR — A sawtooth voltage signal is generated by a constant current source (typ. 7.5 μA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2}, which are respectively:

$V_{TH1} = -1.0$ V

$V_{TH2} = -V_{CC} + 1.25$ V.

Charging and discharging currents occur only with negative halfcycles of the line.

In UAA1016A, the sawtooth signal is available at Pin 1 as a source current proportional to $V_{Pin\ 2}$, varying from 2.1 to 15 μA as $V_{Pin\ 2}$ varies from V_{TH1} to V_{TH2}.

In UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75$ V. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a maximum source current of 40 μA is recommended (see Figure 7).

FAIL-SAFE — Output pulses are inhibited by the "fail-safe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if temperature sensor circuit had a fault.

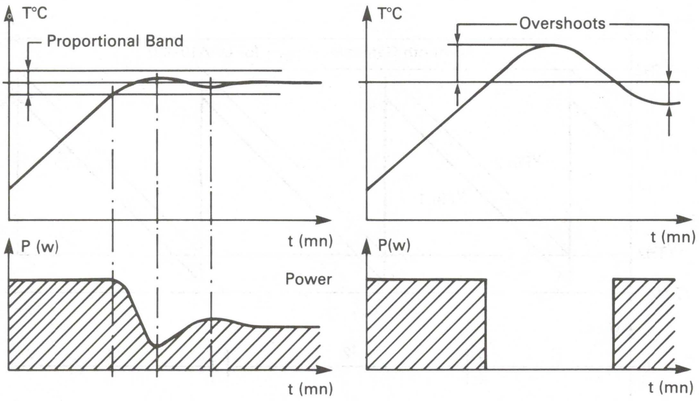
SAMPLING FULL WAVE LOGIC — Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle of the line to minimize generation of noise (as per Figure 8). Within every zero-crossing the pulses are positioned as per Figure 4. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

PULSE AMPLIFIER — The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

SYNCHRONIZATION CIRCUIT — Through R_{sync}, the synchronization circuit detects mains zero-crossing and uses this information to drive the sampling full wave logic.

R_{sync} also determines the trigger pulse length (see Figure 5).

FIGURE 2 — PROPORTIONAL TEMPERATURE CONTROL versus ON/OFF CONTROL



PROPORTIONAL TEMPERATURE CONTROL	ON/OFF CONTROL
Reduced Overshoot	Large Overshoot
Stability	Marginal Stability

COMMENTS TO FIGURE 3

Referring to Figure 1, the average value of V_{Ref} is set by R_2 and R_3. R_4 defines the amplitude of the sawtooth signal superimposed on V_{Ref}, defining the Proportional Band.

Figure 3 shows three conditions:

1) During time t_1 we always have $V_{Pin\ 3} > V_{Ref}$, and as a result, the comparator is always "on" and the triac fired (100% max. power)
2) During time t_2, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.
3) During time t_3, $V_{Pin\ 3} < V_{Ref}$, and the triac is always "off."

FIGURE 3 — SAWTOOTH GENERATOR AND PROPORTIONAL BAND

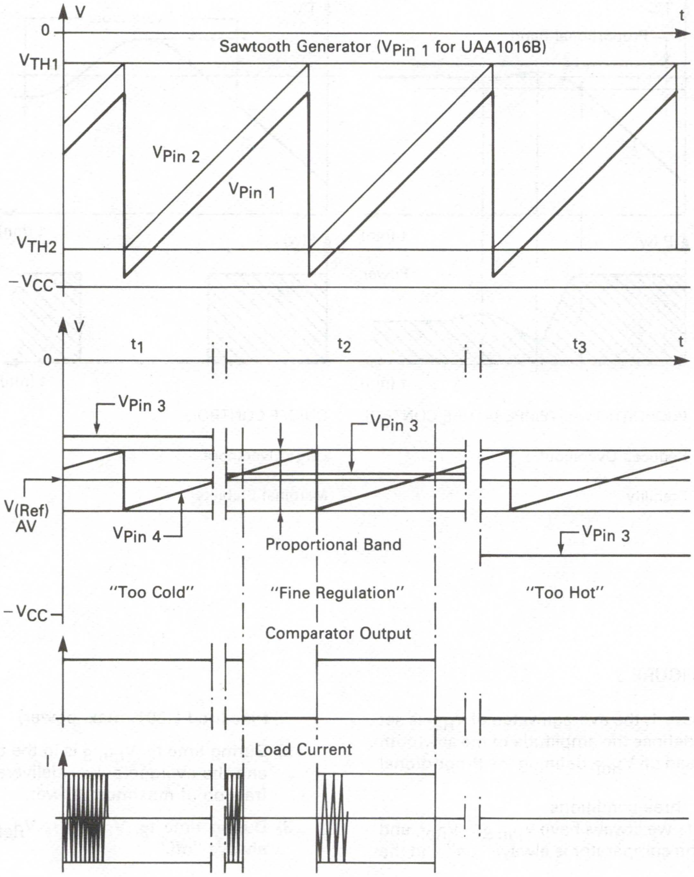

V
t
0
Sawtooth Generator (VPin 1 for UAA1016B)
VTH1
VPin 2
VPin 1
VTH2
−VCC
V
t1
t2
t3
t
0
VPin 3
VPin 3
V(Ref) AV
VPin 4
Proportional Band
VPin 3
"Too Cold"
"Fine Regulation"
"Too Hot"
−VCC
Comparator Output
Load Current
I

FIGURE 4 — OUTPUT PULSE WIDTH DEFINITIONS

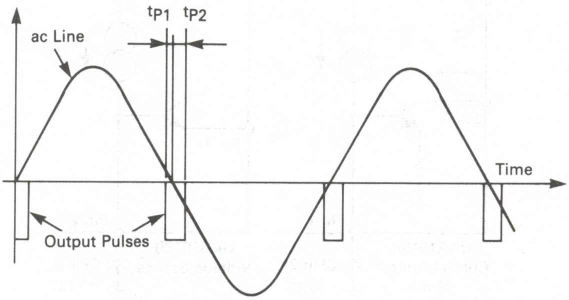

t_{P1} t_{P2}
ac Line
Time
Output Pulses

FIGURE 5 — TYPICAL OUTPUT PULSE LENGTH versus SYNCHRONIZATION RESISTOR

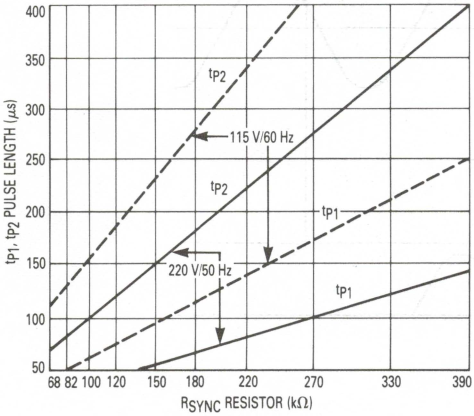
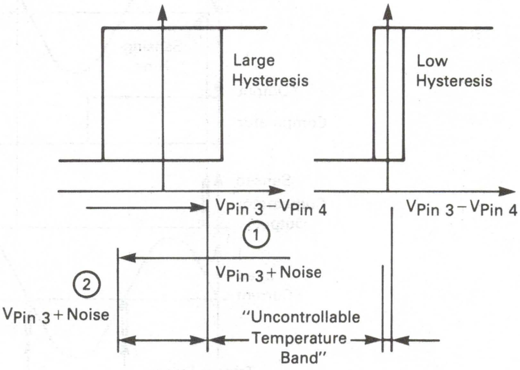


FIGURE 6 — EFFECTS OF INPUTS COMPARATOR HYSTERESIS


Large Hysteresis
Low Hysteresis
$V_{Pin\ 3} - V_{Pin\ 4}$
$V_{Pin\ 3} - V_{Pin\ 4}$
①
$V_{Pin\ 3}$ + Noise
②
$V_{Pin\ 3}$ + Noise
"Uncontrollable Temperature Band"

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} - V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

FIGURE 7 — PIN 1 INTERNAL NETWORK

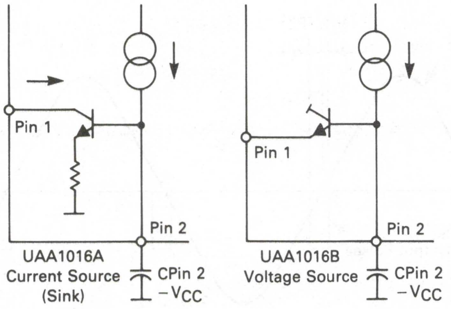
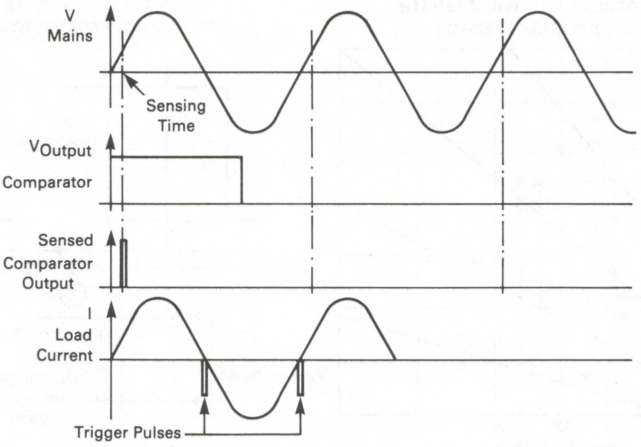

Pin 1
Pin 2
UAA1016A
Current Source
(Sink)
CPin 2
−VCC
Pin 1
Pin 2
UAA1016B
Voltage Source
CPin 2
−VCC

FIGURE 8 — TRIGGER PULSE GENERATION


V
Mains
Sensing
Time
VOutput
Comparator
Sensed
Comparator
Output
I
Load
Current
Trigger Pulses

SUGGESTIONS FOR USE

The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P-N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

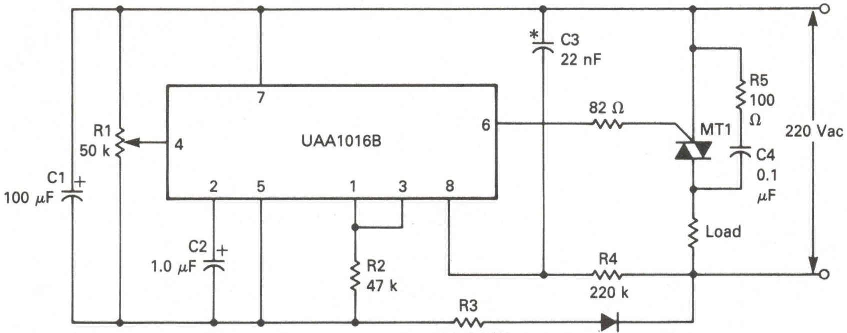
Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C_3 connected to Pin 8 network (see Figure 9).

Suggested maximum source current at Pin 1 (UAA1016B) is 40 μA, in order to have acceptable sawtooth signal linearity.

APPLICATION CIRCUITS

Figure 9 shows a very simple application of UAA1016B as an electronic rheostat having 100% efficiency. C_3 is required only if load has an inductive component. Figure 10 shows a typical application as a panel heater thermostat with a proportional temperature band of 1°C at 25°C.

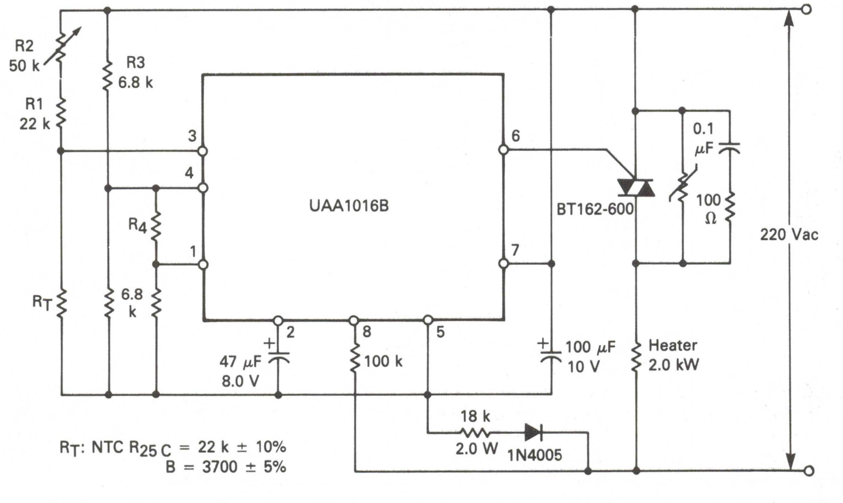
FIGURE 9 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT OR ENERGY REGULATOR



C1
100 µF
R1
50 k
UAA1016B
7
4
6
2
5
1
3
8
C2
1.0 µF
R2
47 k
R3
18 k 2.0 W
1N4005
R4
220 k
C3
22 nF
*
82 Ω
MT1
R5
100
Ω
C4
0.1
µF
Load
220 Vac

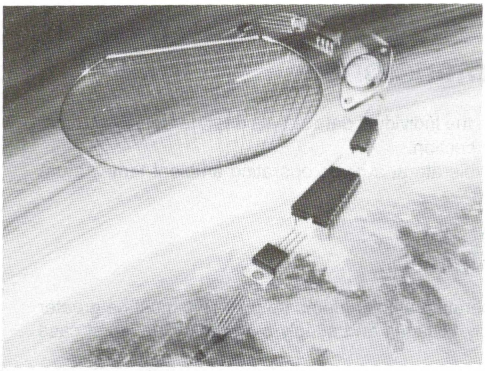
*Require for Inductive Loads only

FIGURE 10 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND THERMOSTAT, PROPORTIONAL BAND 1°C AT 25°C



R2
50 k
R1
22 k
R3
6.8 k
R4
RT
6.8
k
UAA1016B
3
4
1
6
7
2
8
5
47 µF
8.0 V
100 k
18 k
2.0 W
1N4005
100 µF
10 V
BT162-600
0.1
µF
100
Ω
Heater
2.0 kW
220 Vac

R_T: NTC $R_{25\,C}$ = 22 k ± 10%
B = 3700 ± 5%



Packaging Information, Including Small Outline Integrated Circuits (SOIC)

Case Outline Dimensions

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

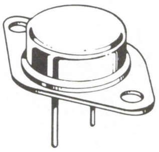
where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

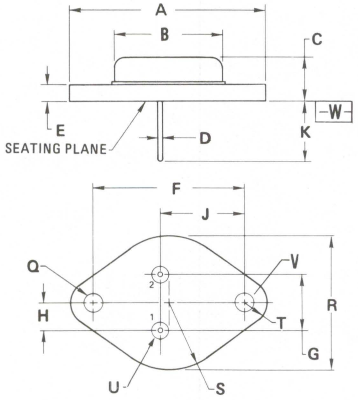
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

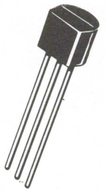
CASE 1-03
TO-204AA
(TO-3)
Metal Package
$R_{\theta JA}$ = 45° C/W(Typ)
$R_{\theta JC}$ = See Data Sheet

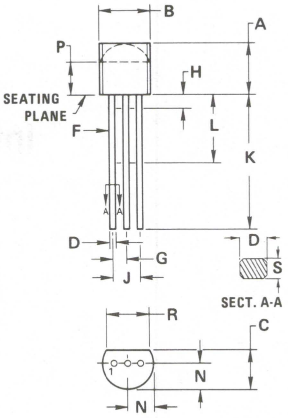




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	7.92	–	0.312	–
Q	3.84	4.09	0.151	0.161
S	–	13.34	–	0.525
T	–	4.78	–	0.188
V	3.84	4.09	0.151	0.161

CASE 29-02
TO-226AA
(TO-92)
Plastic Package
$R_{\theta JA}$ = 200° C/W

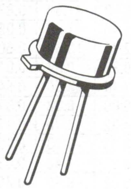


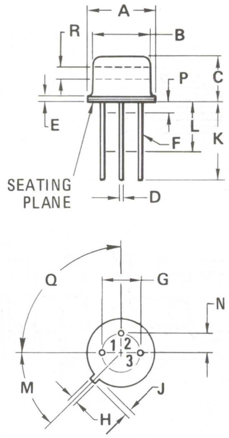


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.67	0.080	0.105
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

CASE OUTLINE DIMENSIONS (continued)

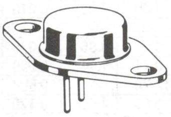
CASE 79-02
TO-205AD
(TO-39)
Metal Package
$R_{\theta JA}$ = 185° C/W(Typ)

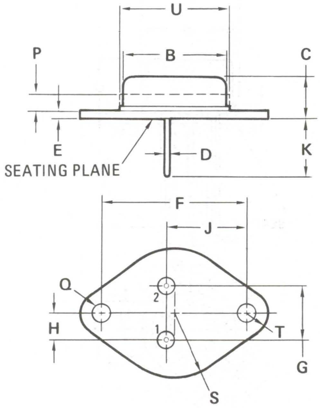




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

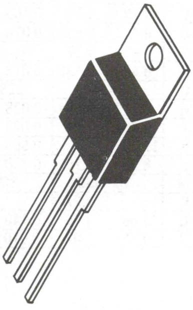
CASE 80-02
TO-213AA
(TO-66)
Metal Package
$R_{\theta JA}$ = 45°C/W(Typ)
$R_{\theta JC}$ = See Data Sheet

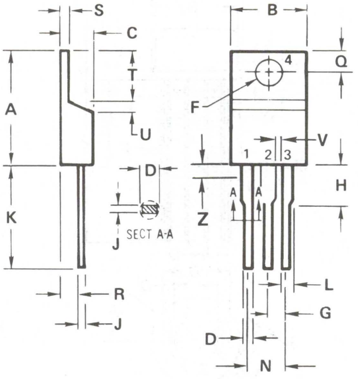




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68*	–	0.145
U	–	15.75	–	0.620

CASE 221A-02
TO-220AB
Plastic Power
$R_{\theta JA}$ = 65° C/W(Typ)
$R_{\theta JC}$ = See Data Sheet

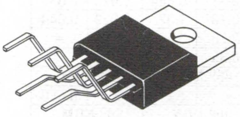


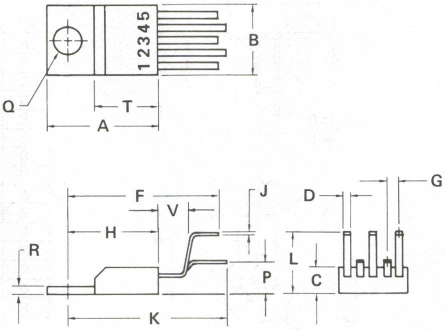


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	–	2.03	–	0.080

CASE OUTLINE DIMENSIONS (continued)

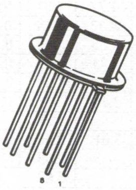
CASE 314B-01
Ceramic Package
$R_{\theta JA}$ = 65° C/W
$R_{\theta JC}$ = See Data Sheet

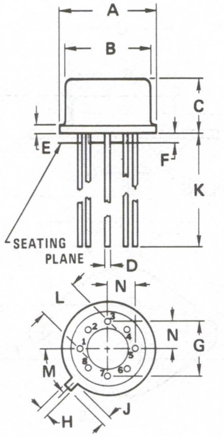




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.49	15.88	0.610	0.625
B	9.91	10.41	0.390	0.410
C	4.32	4.57	0.170	0.180
D	0.71	0.81	0.028	0.032
F	20.83	21.59	0.820	0.850
G	1.45	1.96	0.057	0.077
H	12.70	13.69	0.500	0.539
J	0.38	0.64	0.015	0.025
K	21.46	23.50	0.845	0.925
L	8.00	8.38	0.315	0.330
P	4.32	4.70	0.170	0.185
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
T	9.02	9.40	0.355	0.370
V	4.70	5.46	0.185	0.215

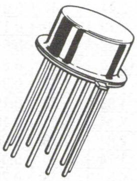
CASE 601-04
Metal Package
$R_{\theta JA}$ = 160° C/W(Typ)

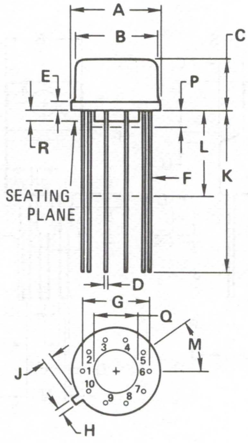




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

CASE 603-04
TO-100
Metal Can
$R_{\theta JA}$ = 160° C/W

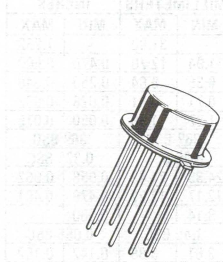


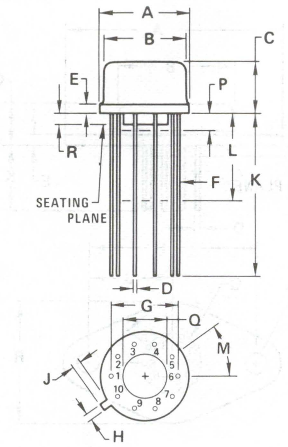


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

CASE OUTLINE DIMENSIONS (continued)

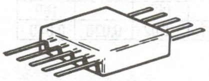
CASE 603C-01
TO-100 Type
$R_{\theta JA}$ = 150° C/W(Typ)

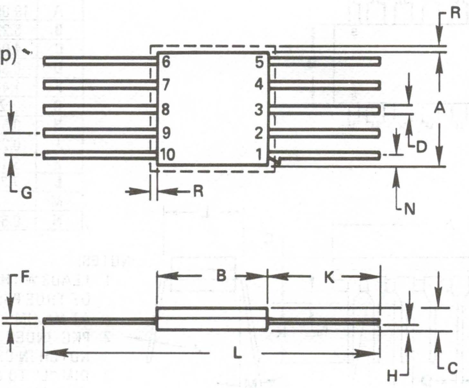




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36^0 BSC		36^0 BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

CASE 606-04
TO-91
Ceramic Package
$R_{\theta JA}$ = 165° C/W(Typ)

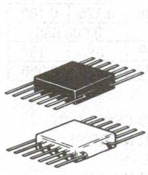


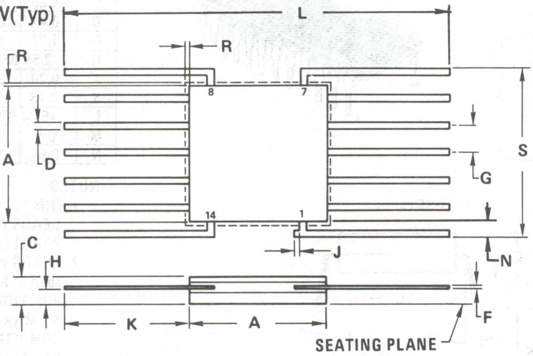


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.36	0.240	0.290
B	6.10	6.60	0.240	0.260
C	0.762	1.77	0.030	0.070
D	0.254	0.482	0.010	0.019
F	0.077	0.152	0.003	0.006
G	1.15	1.39	0.045	0.055
H	0.127	0.889	0.005	0.035
K	1.78	–	0.070	–
R	–	0.381	–	0.015

NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH TO-91 OUTLINE SHALL APPLY.
2. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION (AT BODY)

CASE 607-05
TO-86 Type
Ceramic Package
$R_{\theta JA}$ = 165° C/W(Typ)



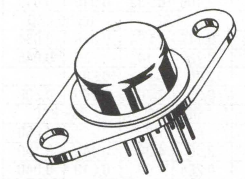


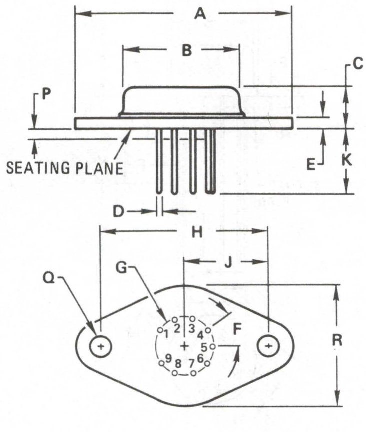
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	–	0.38	–	0.015
K	6.35	9.40	0.250	0.370
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

NOTES:
1. "R" DIMENSIONS DETERMINE ZONE WITHIN WHICH ALL BODY AND LEAD IRREGULARITIES LIE.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

CASE OUTLINE DIMENSIONS (continued)

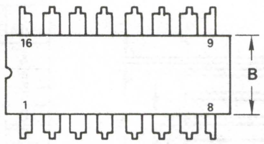
CASE 614-02
(TO-66 Type)
Metal Package
$R_{\theta JA}$ = 35° C/W(Typ)
$R_{\theta JC}$ = See Data Sheet

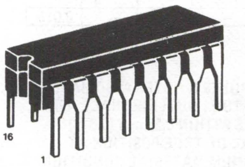


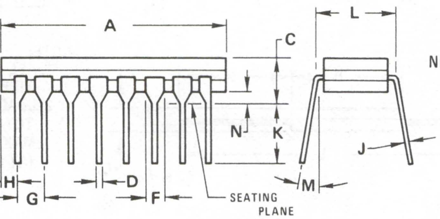


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	31.80	–	1.252
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.81	0.028	0.032
E	1.27	1.90	0.050	0.075
F	36° BSC		36° BSC	
G	8.26 BSC		0.325 BSC	
H	24.33	24.43	0.958	0.962
J	12.17	12.22	0.479	0.481
K	9.14	–	0.360	–
P	1.40 BSC		0.055 BSC	
Q	3.61	3.86	0.142	0.152
R	–	17.78	–	0.700

CASE 620-02
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)





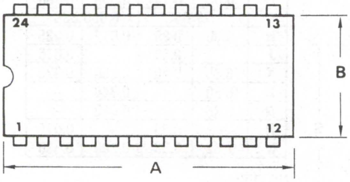


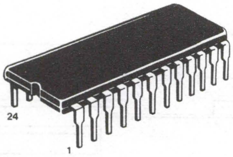
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

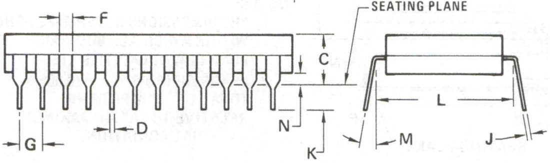
NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 623-05
Ceramic Package
$R_{\theta JA}$ = 53° C/W(Typ)







DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

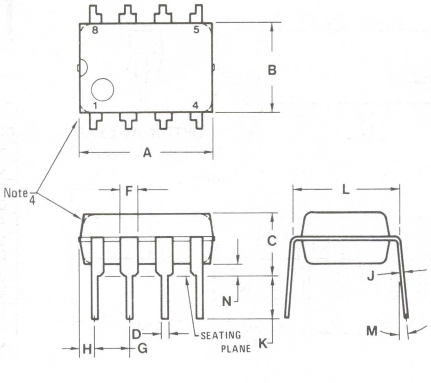
NOTES:

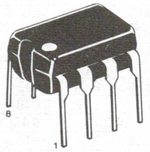
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

CASE 626-04

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030

NOTES:

1. LEAD POSITIONAL TOLERANCE:
   ⌖ | Ø 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. 626-03 OBSOLETE NEW STD 626-04.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

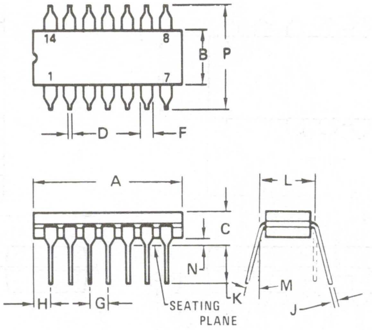
CASE 632-02

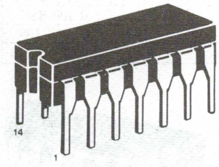
MO-001AA

(TO-116)

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

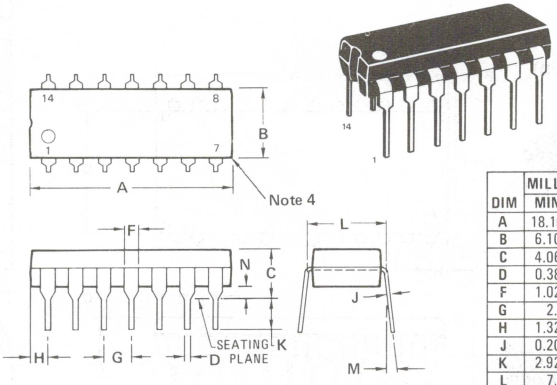
NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

CASE 646-05

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

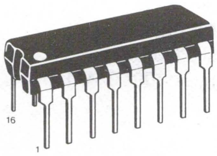
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

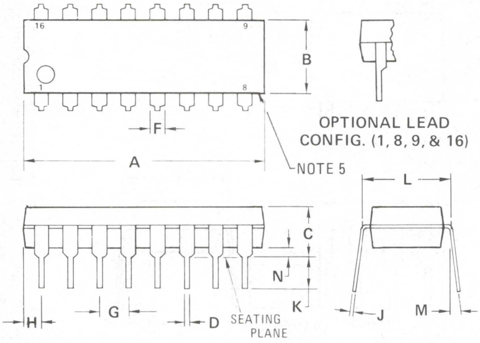
CASE OUTLINE DIMENSIONS (continued)

CASE 648-05

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

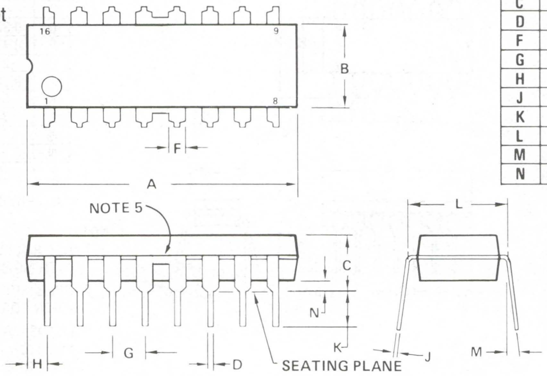
CASE 648C-01

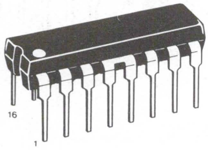
Ceramic Package

$R_{\theta JA}$ = 52° C/W

$R_{\theta JC}$ = See Data Sheet

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040





NOTES:

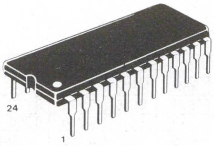
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.

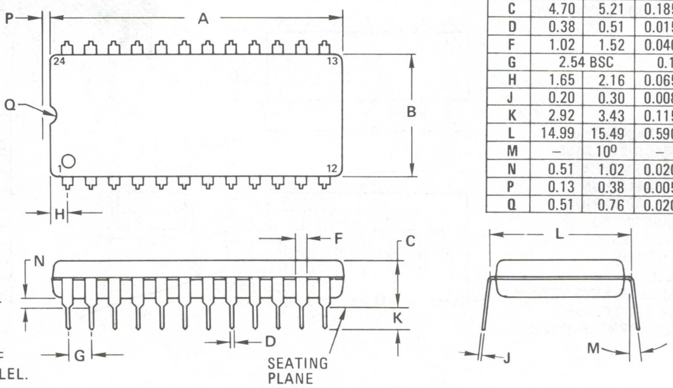
CASE 649-03

Plastic Package

$R_{\theta JA}$ = 90° C/W(Typ)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030





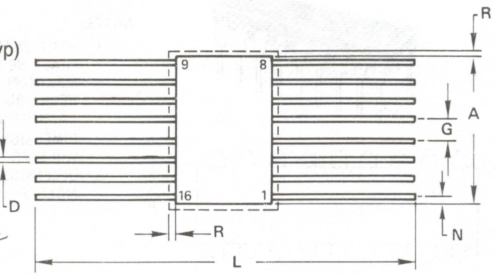
NOTES:

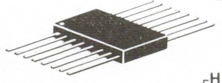
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

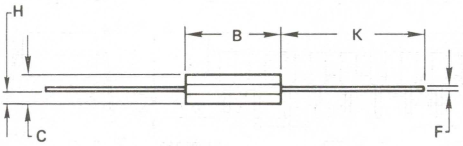
CASE OUTLINE DIMENSIONS (continued)

CASE 650-02

Ceramic Package
$R_{\theta JA}$ = 140° C/W(Typ)







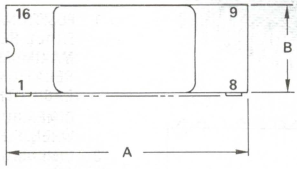
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

NOTES:

1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 690-13

Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)

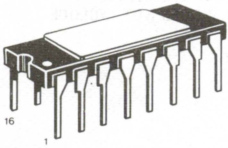


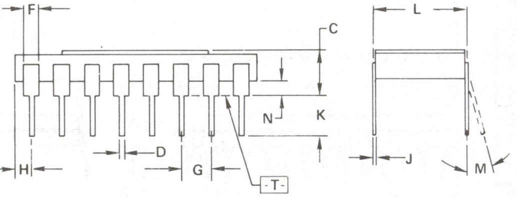
NOTES:

1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS (D).

| ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ |

4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

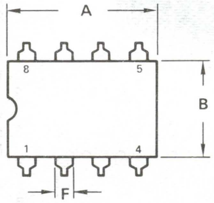


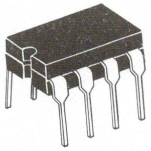


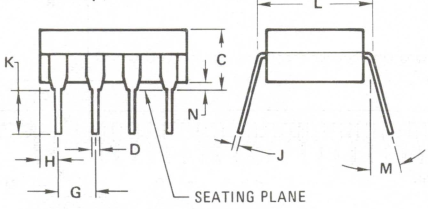
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.52	0.015	0.060

CASE 693-02

Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:

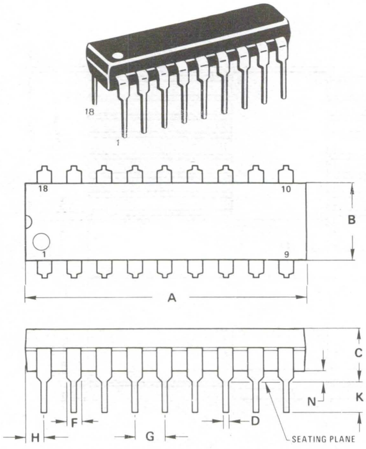
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

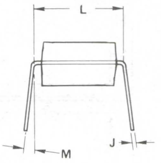
CASE OUTLINE DIMENSIONS (continued)

CASE 707-02

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





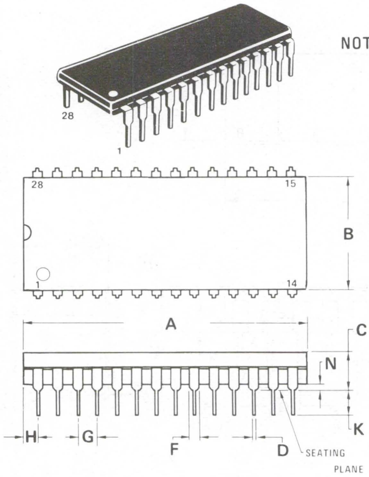
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

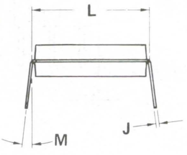
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 710-02

Ceramic Package





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:

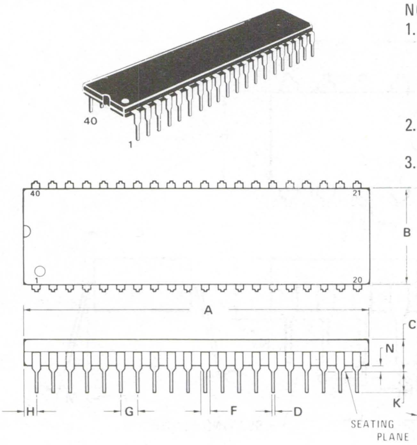
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

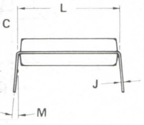
CASE 711-03

Ceramic Package

NOTES:

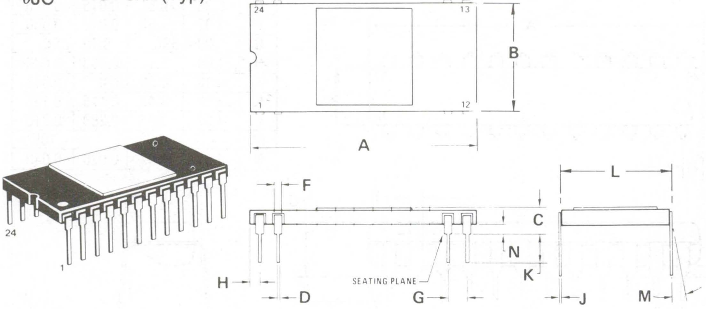
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

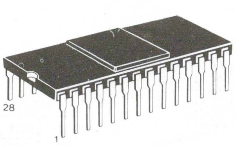
CASE 716-06
Ceramic Package
$R_{\theta JA}$ = 55° C/W
$R_{\theta JC}$ = 15° C/W(Typ)

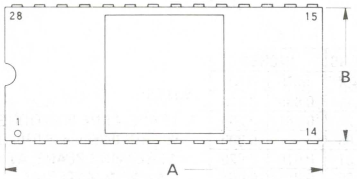


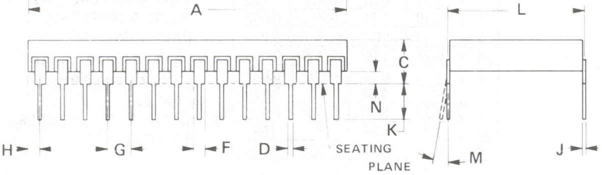
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

CASE 719-03
Ceramic Package
$R_{\theta JA}$ = 55° C/W
$R_{\theta JC}$ = 15° C/W(Typ)



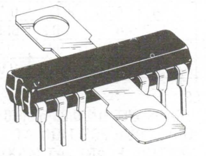


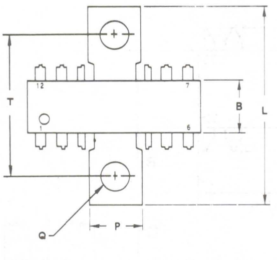


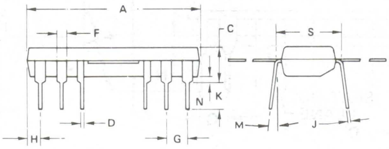
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.73	15.34	0.580	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.52	0.020	0.060

CASE 721-02
Plastic Package
$R_{\theta JA}$ = 52° C/W
$R_{\theta JC}$ = See Data Sheet







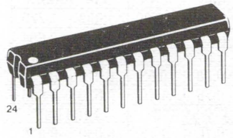
NOTES:
1. DIMENSION "S" TO CENTER OF LEADS WHEN FORMED PARALLEL.

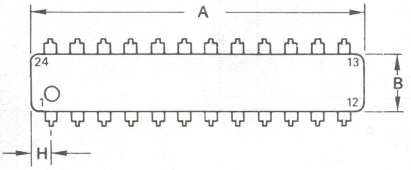
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	3.30	3.94	0.130	0.155
L	25.15	27.94	0.990	1.100
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
Q	3.48	3.73	0.137	0.147
S	7.37	7.87	0.290	0.310
T	16.26	16.76	0.640	0.660

CASE OUTLINE DIMENSIONS (continued)

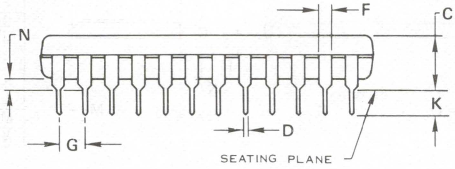
CASE 724-02
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)

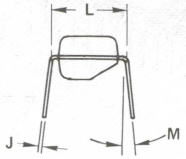
NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).



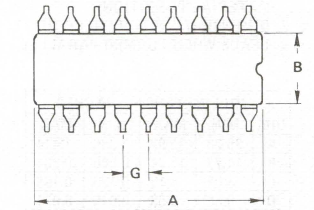


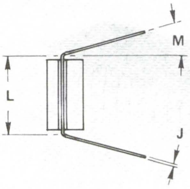
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040

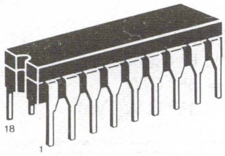


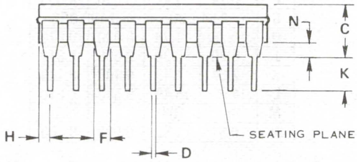


CASE 726-01
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)





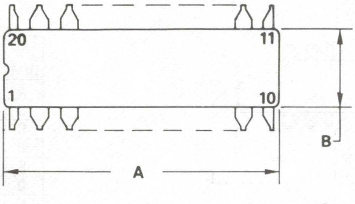


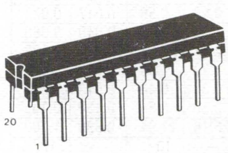


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.63	7.24	0.261	0.285
C	–	5.08	–	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.02	0.030	0.040
J	0.13	0.38	0.005	0.015
K	–	4.44	–	0.175
L	7.37	8.00	0.290	0.315
M	0°	15°	0°	15°
N	0.51	0.76	0.020	0.030

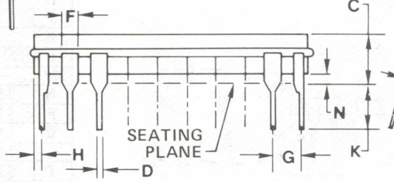
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

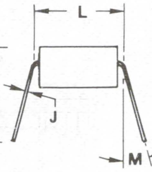
CASE 732-03
Ceramic Package
$R_{\theta JA}$ = 75° C/W





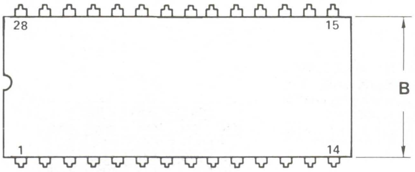
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040





NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

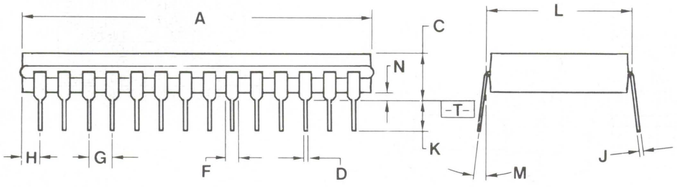
CASE 733-03
Ceramic Package

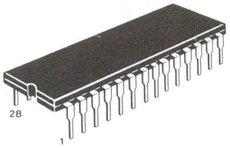


NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:

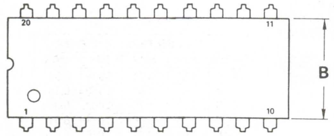
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050





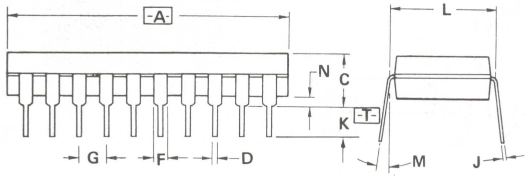
CASE 738-02
Plastic Package
$R_{\theta JA}$ = 75° C/W

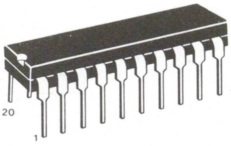


NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;

   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

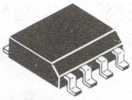
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

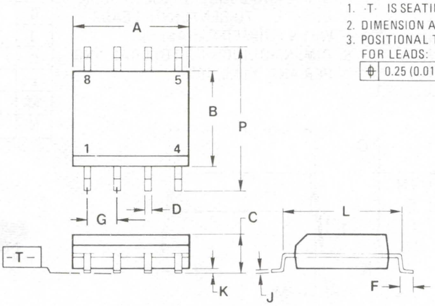




SOIC MINIATURE IC PLASTIC PACKAGE

SO8 CASE 751 D SUFFIX



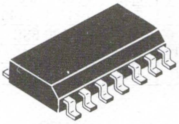


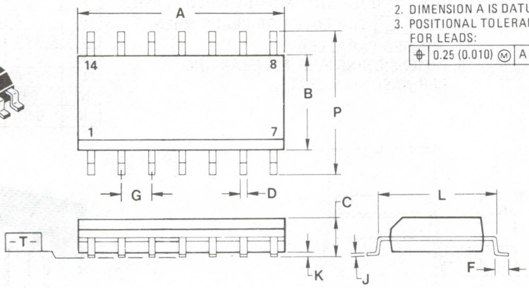
NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

SO14 CASE 751A D SUFFIX



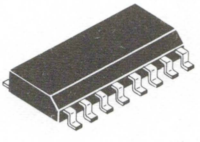


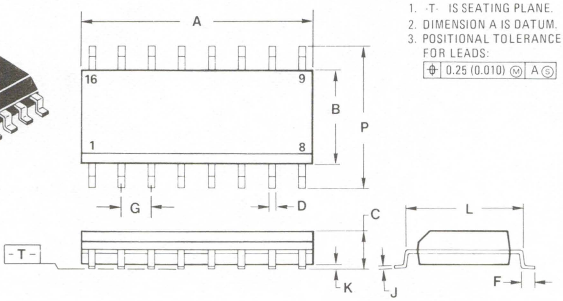
NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.54	8.74	0.336	0.344
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

SO16 CASE 751B D SUFFIX





NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

SOIC MINIATURE IC PLASTIC PACKAGE

THERMAL INFORMATION

THE MAXIMUM POWER CONSUMPTION AN INTEGRATED CIRCUIT CAN TOLERATE AT A GIVEN OPERATING AMBIENT TEMPERATURE, CAN BE FOUND FROM THE EQUATION:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

WHERE: $P_{D(T_A)}$ = POWER DISSIPATION ALLOWABLE AT A GIVEN OPERATING AMBIENT TEMPERATURE.

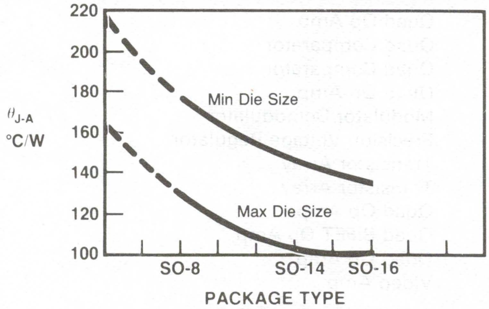
$T_{J(max)}$ = MAXIMUM OPERATING JUNCTION TEMPERATURE AS LISTED IN THE MAXIMUM RATINGS SECTION

T_A = DESIRED OPERATING AMBIENT TEMPERATURE

$R_{\theta JA(Typ)}$ = TYPICAL THERMAL RESISTANCE JUNCTION TO AMBIENT

RATING	SYMBOL	VALUE	UNIT
OPERATING AMBIENT TEMPERATURE RANGES	T_A	0 TO +70 −40 TO +85	°C °C
OPERATING JUNCTION TEMPERATURE	T_J	+150	°C
STORAGE TEMPERATURE RANGE	T_{Stg}	−55 TO +150	°C

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT (°C/W)



THERMAL RESISTANCE OF SOIC PACKAGES. MEASUREMENT SPECIMENS ARE SOLDER MOUNTED ON PRINTED CIRCUIT CARD 20mm X 32mm X 1.7mm IN STILL AIR. NO AUXILIARY THERMAL CONDUCTION AIDS ARE USED. AS THERMAL RESISTANCE VARIES INVERSELY WITH DIE AREA, A GIVEN PACKAGE TAKES VALUES BETWEEN THE MAX AND MIN VALUES SHOWN WHICH REPRESENT SMALLEST (2000 SQUARE MILS) AND LARGEST (8000 SQUARE MILS) EXPECTED TO BE ASSEMBLED IN THE SOIC PACKAGE.

MOTOROLA BIPOLAR INTEGRATED CIRCUITS GROUP
TYPES OF LINEAR IC'S AVAILABLE IN SOIC PACKAGES

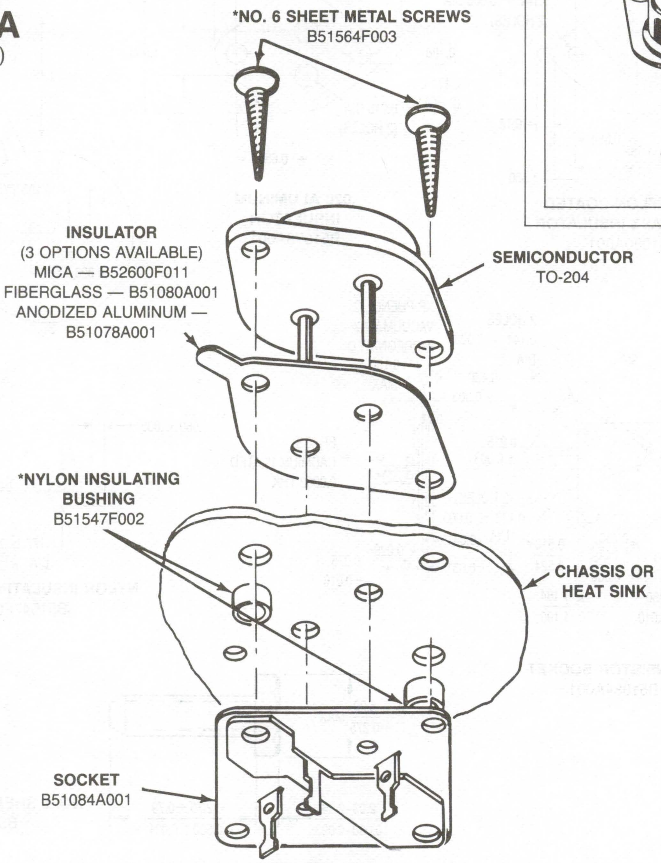
The table below lists those Linear IC devices that will form the core of our initial introduction lineup. All current and future Linear IC products are potential candidates for the SOIC packages, providing the chip size fits the die-bond area (flag) of the package and the power dissipation is within the package limits. Electrical characteristics and package pin-out configurations are as indicated in the standard device data sheet except where noted.

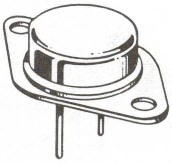
DEVICE	FUNCTION	PACKAGE
LM301AD	General Purpose Op Amp	SO-8
LM211D	Comparator	SO-8
LM311D	Comparator	SO-8
LM358D	Dual Op Amp	SO-8
LM393D	Dual Comparator	SO-8
LM2903D	Dual Comparator	SO-8
LM2904D	Dual Op Amp	SO-8
MC1403D*	Precision Voltage Reference	SO-8
MC1455D	Timer	SO-8
MC1458CD	Dual Op Amp	SO-8
MC1458D	Dual Op Amp	SO-8
MC1741CD	General Purpose Op Amp	SO-8
MC1776CD	Programmable Op Amp	SO-8
MC34001D	BIFET Op Amp	SO-8
MC34002D	Dual BIFET Op Amp	SO-8
MC4558CD	Wide BW Dual Op Amp	SO-8
LM324D	Quad Op Amp	SO-14
LM339D	Quad Comparator	SO-14
LM2901D	Quad Comparator	SO-14
LM2902D	Quad Op Amp	SO-14
MC1496D	Modulator/Demodulator	SO-14
MC1732CD	Precision Voltage Regulator	SO-14
MC3346D	Transistor Array	SO-14
MC3386D	Transistor Array	SO-14
MC3403D	Quad Op Amp	SO-14
MC34004D	Quad BIFET Op Amp	SO-14
MC4741CD	Quad Op Amp	SO-14
NE592D	Video Amp	SO-14
MC1408D8/D7/D6*	8-Bit Multiplying D/A Converter	SO-16
MC3357D	Low Power FM I/F	SO-16
MC3470AD	Floppy Disk Read Amplifier System	SO-18L

*Electrical specifications or package pin-outs will differ slightly from the standard device data sheet for these products. Contact product marketing for further information regarding these variations.

Mounting Hardware TO-204AA

(Formerly TO-3)

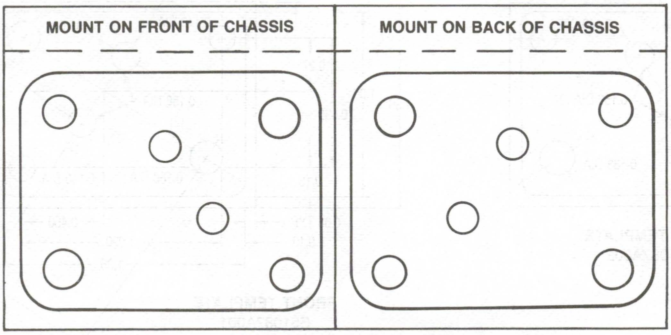

*NO. 6 SHEET METAL SCREWS
B51564F003
INSULATOR
(3 OPTIONS AVAILABLE)
MICA — B52600F011
FIBERGLASS — B51080A001
ANODIZED ALUMINUM —
B51078A001
SEMICONDUCTOR
TO-204
*NYLON INSULATING
BUSHING
B51547F002
CHASSIS OR
HEAT SINK
SOCKET
B51084A001



CASE 1-03
TO-204AA

*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

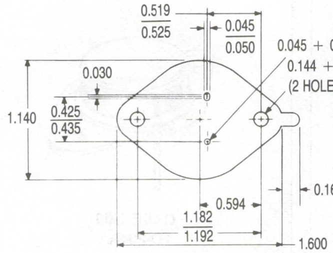
DRAWINGS NOT TO SCALE


MOUNT ON FRONT OF CHASSIS
MOUNT ON BACK OF CHASSIS

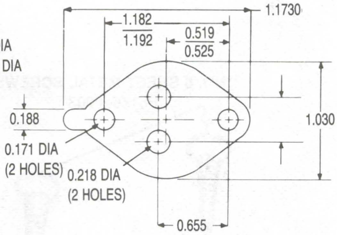
FRONT TEMPLATE
B51087A001

BACK TEMPLATE
B51087A002

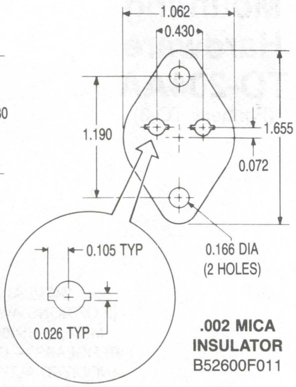
MOUNTING HARDWARE TO-204AA


0.519
0.525
0.045
0.050
0.045 + 0.003 DIA
0.144 + 0.003 DIA
(2 HOLES)
0.030
1.140
0.425
0.435
0.16
0.594
1.182
1.192
1.600

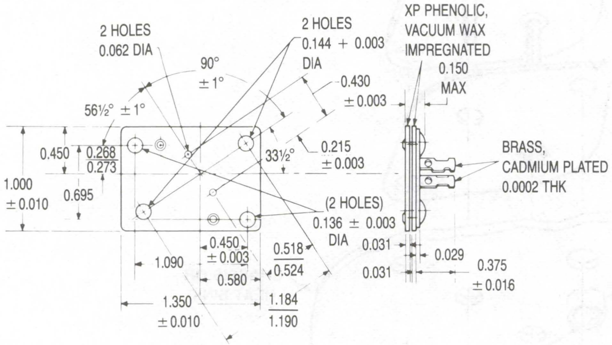
0.003 TEFLON-COATED FIBERGLASS INSULATOR
B51080A001


1.1730
1.182
1.192
0.519
0.525
0.188
0.171 DIA
(2 HOLES)
0.218 DIA
(2 HOLES)
1.030
0.655

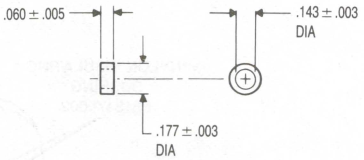
.020 ALUMINUM INSULATOR
B51078A001


1.062
0.430
1.190
1.655
0.072
0.166 DIA
(2 HOLES)
0.105 TYP
0.026 TYP

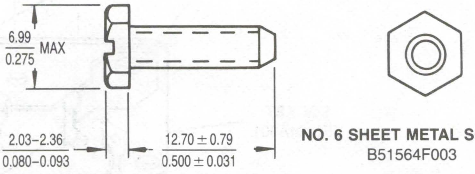
.002 MICA INSULATOR
B52600F011


2 HOLES
0.062 DIA
90°
±1°
56½° ±1°
2 HOLES
0.144 + 0.003
DIA
0.430
±0.003
XP PHENOLIC,
VACUUM WAX
IMPREGNATED
0.150
MAX
0.450
0.268
0.273
33½°
0.215
±0.003
1.000
±0.010
0.695
BRASS,
CADMIUM PLATED
0.0002 THK
(2 HOLES)
0.136 ± 0.003
DIA
0.031
0.029
0.031
0.375
±0.016
0.450
±0.003
0.518
0.524
1.090
0.580
1.350
±0.010
1.184
1.190

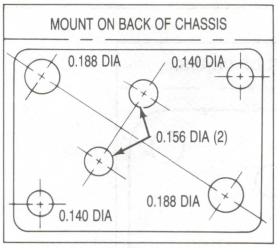
TRANSISTOR SOCKET
B51084A001


.060 ± .005
.143 ± .003
DIA
.177 ± .003
DIA

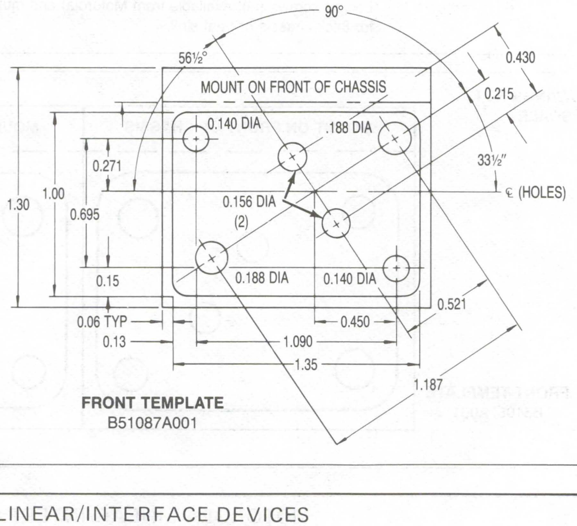
NYLON INSULATING BUSHING
B51547F002


6.99
0.275
MAX
2.03–2.36
0.080–0.093
12.70 ± 0.79
0.500 ± 0.031

NO. 6 SHEET METAL SCREW
B51564F003


MOUNT ON BACK OF CHASSIS
0.188 DIA
0.140 DIA
0.156 DIA (2)
0.140 DIA
0.188 DIA

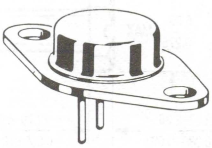
BACK TEMPLATE
B51087A002


90°
56½°
0.430
0.215
MOUNT ON FRONT OF CHASSIS
0.140 DIA
.188 DIA
33½″
℄ (HOLES)
0.271
1.30
1.00
0.695
0.156 DIA
(2)
0.15
0.188 DIA
0.140 DIA
0.521
0.06 TYP
0.13
0.450
1.090
1.35
1.187

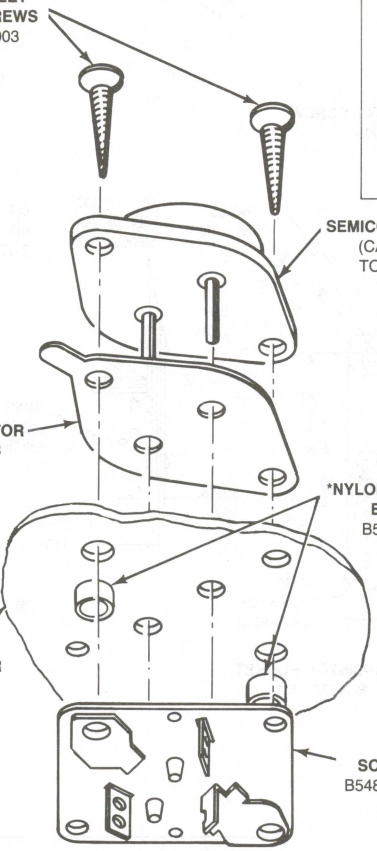
FRONT TEMPLATE
B51087A001

Mounting Hardware TO-213AA

(Formerly TO-66)

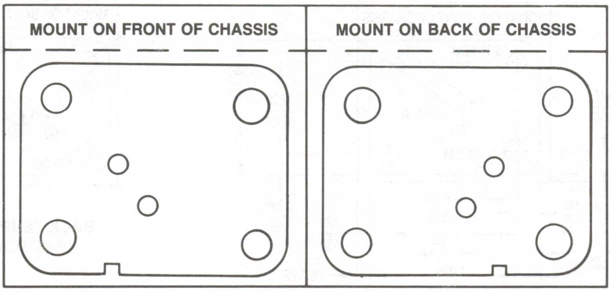


CASE 80-02
TO-213AA

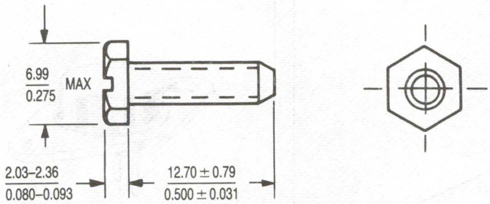

*NO. 6 SHEET METAL SCREWS
B51564F003
SEMICONDUCTOR
(CASE 80)
TO-213AA
MICA INSULATOR
B52600F008
*NYLON INSULATING BUSHING
B51547F002
CHASSIS OR HEAT SINK
SOCKET
B54837C001

*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

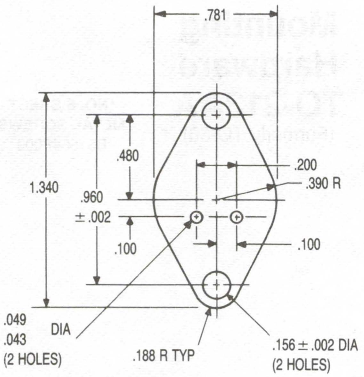
(DRAWINGS NOT TO SCALE)


MOUNT ON FRONT OF CHASSIS
MOUNT ON BACK OF CHASSIS
FRONT TEMPLATE
B54879C001
BACK TEMPLATE
B54879C002

MOUNTING HARDWARE TO-213AA

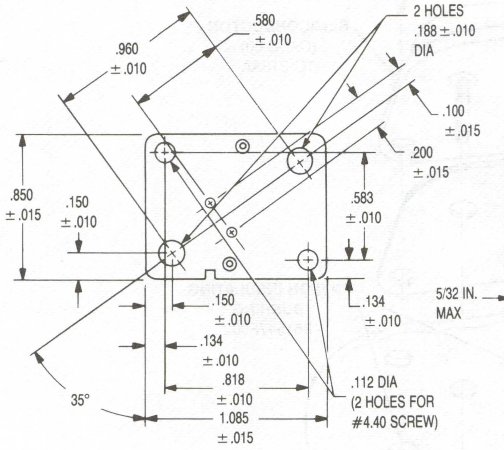

6.99
0.275
MAX
2.03–2.36
0.080–0.093
12.70 ± 0.79
0.500 ± 0.031

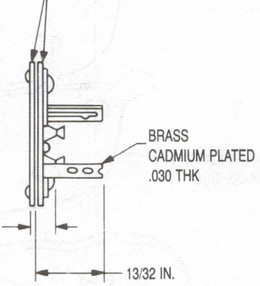
NO. 6 SHEET METAL SCREW
B51564F003


.781
1.340
.480
.960
± .002
.100
.200
.390 R
.100
.049
.043
DIA
(2 HOLES)
.188 R TYP
.156 ± .002 DIA
(2 HOLES)

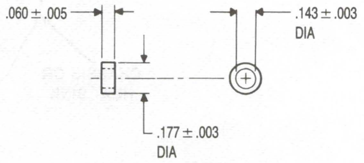
0.005 MICA INSULATOR
B52600F008

0.003 MICA INSULATOR
B52600F009

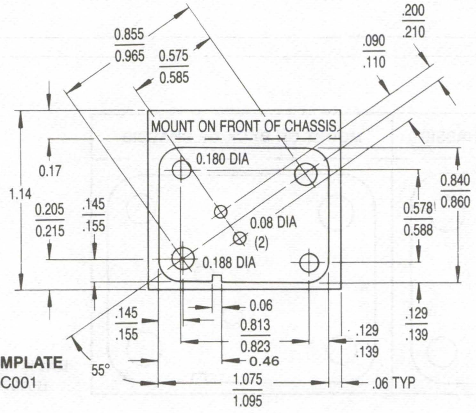

.960
± .010
.580
± .010
2 HOLES
.188 ± .010
DIA
.100
± .015
.200
± .015
.850
± .015
.150
± .010
.583
± .010
.150
± .010
.134
± .010
.134
± .010
.818
± .010
1.085
± .015
.112 DIA
(2 HOLES FOR
#4.40 SCREW)
35°


XP PHENOLIC
VACUUM WAX
IMPREGNATED
BRASS
CADMIUM PLATED
.030 THK
5/32 IN.
MAX
13/32 IN.

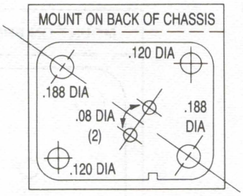
TRANSISTOR SOCKET
B54837C001


.060 ± .005
.143 ± .003
DIA
.177 ± .003
DIA

NYLON INSULATING BUSHING
B51547F002

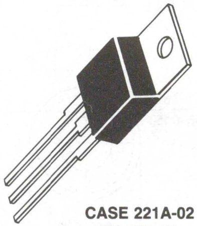

0.855
0.965
0.575
0.585
.090
.110
.200
.210
MOUNT ON FRONT OF CHASSIS
0.180 DIA
0.17
1.14
0.205
0.215
.145
.155
0.08 DIA
(2)
0.188 DIA
0.840
0.860
0.578
0.588
.145
.155
0.06
0.813
0.823
0.46
.129
.139
.129
.139
55°
1.075
1.095
.06 TYP

FRONT TEMPLATE
B54879C001


MOUNT ON BACK OF CHASSIS
.120 DIA
.188 DIA
.08 DIA
(2)
.188
DIA
.120 DIA

BACK TEMPLATE
B54879C002

Mounting Hardware TO-220AB



CASE 221A-02
TO-220AB

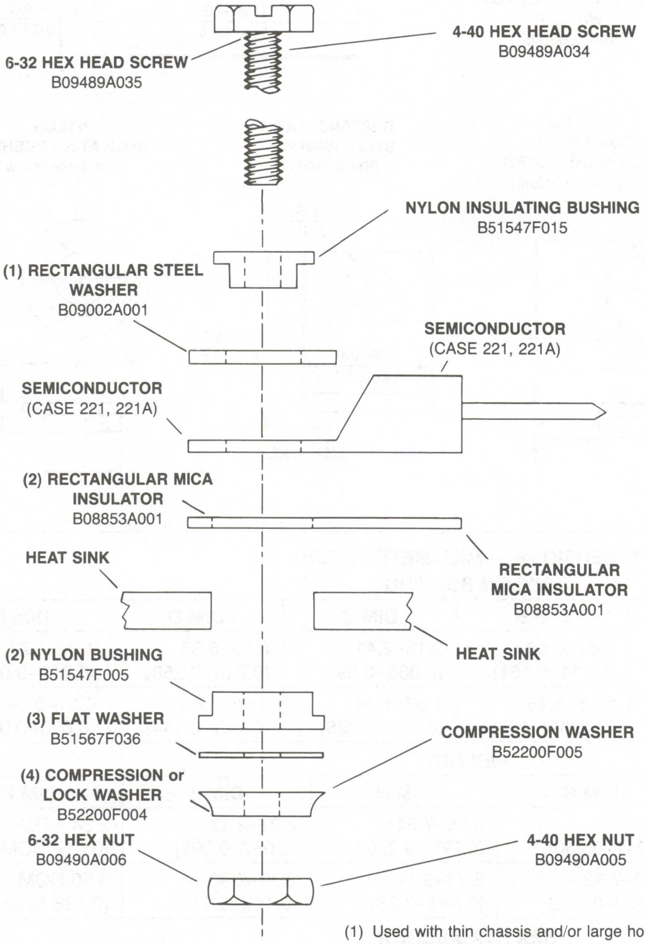
All JEDEC dimensions and notes apply

PREFERRED ARRANGEMENT
for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

ALTERNATE ARRANGEMENT
for Isolated Mounting when Screw must be at Heat-Sink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.

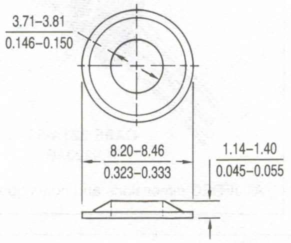

6-32 HEX HEAD SCREW
B09489A035
4-40 HEX HEAD SCREW
B09489A034
NYLON INSULATING BUSHING
B51547F015
(1) RECTANGULAR STEEL WASHER
B09002A001
SEMICONDUCTOR
(CASE 221, 221A)
SEMICONDUCTOR
(CASE 221, 221A)
(2) RECTANGULAR MICA INSULATOR
B08853A001
HEAT SINK
RECTANGULAR MICA INSULATOR
B08853A001
HEAT SINK
(2) NYLON BUSHING
B51547F005
(3) FLAT WASHER
B51567F036
COMPRESSION WASHER
B52200F005
(4) COMPRESSION or LOCK WASHER
B52200F004
6-32 HEX NUT
B09490A006
4-40 HEX NUT
B09490A005

(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

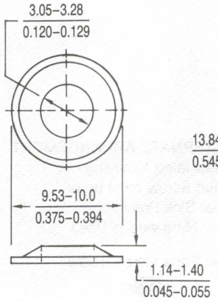
TORQUE REQUIREMENTS
Insulated 0.68 N-M (6 in.-lbs.) max
Noninsulated 0.9 N-M (8 in.-lbs.) max

MOUNTING HARDWARE TO-220AB

(DIMENSION – $\frac{\text{MILLIMETER}}{\text{INCH}}$)

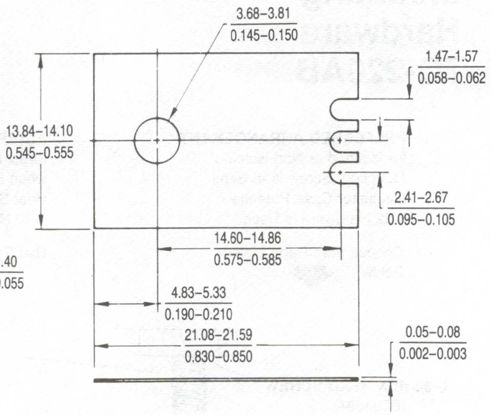

3.71–3.81
0.146–0.150
8.20–8.46
0.323–0.333
1.14–1.40
0.045–0.055

STEEL COMPRESSION WASHER
B52200F004

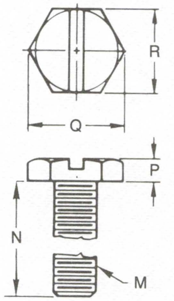

3.05–3.28
0.120–0.129
9.53–10.0
0.375–0.394
1.14–1.40
0.045–0.055

STEEL COMPRESSION WASHER
B52200F005

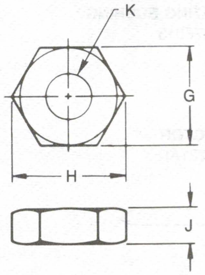
MICA INSULATOR
B08853A001


3.68–3.81
0.145–0.150
1.47–1.57
0.058–0.062
13.84–14.10
0.545–0.555
2.41–2.67
0.095–0.105
14.60–14.86
0.575–0.585
4.83–5.33
0.190–0.210
21.08–21.59
0.830–0.850
0.05–0.08
0.002–0.003

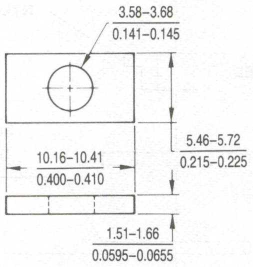
HEX HEAD SCREW
CARBON STEEL
CADMIUM-PLATED
(See table below.)



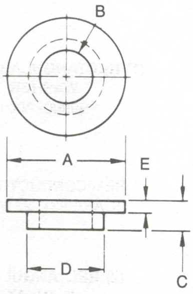
HEX NUT
CARBON STEEL
CADMIUM-PLATED
(See table below.)



RECTANGULAR STEEL WASHER
B09002A001


3.58–3.68
0.141–0.145
10.16–10.41
0.400–0.410
5.46–5.72
0.215–0.225
1.51–1.66
0.0595–0.0655

NYLON INSULATING BUSHING
(See table below.)



DIMENSIONS — MILLIMETER (INCH)

NYLON BUSHING

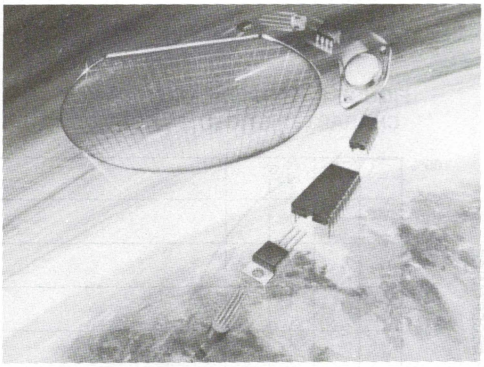
PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9.40–9.65 (0.370–0.380)	3.84–4.09 (0.151–0.161)	2.16–2.41 (0.085–0.095)	6.10–6.35 (0.240–0.250)	1.02–1.27 (0.040–0.050)
B51547F015	5.59–6.10 (0.220–0.240)	3.05–3.15 (0.120–0.124)	1.57–1.68 (0.062–0.066)	3.56–3.66 (0.140–0.144)	0.51–0.64 (0.020–0.025)

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12–6.35 (0.241–0.250)	6.98–7.34 (0.275–0.289)	2.21–2.49 (0.087–0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67–7.92 (0.302–0.312)	8.74–9.17 (0.344–0.361)	2.59–2.90 (0.102–0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A034	0.112–40	1.57 (0.62)	1.24–1.52 (0.049–0.060)	5.12 MIN (0.202 MIN)	4.60–4.75 (0.181–0.187)
6-32	B09489A035	0.138–32	1.57 (0.62)	2.03–2.36 (0.80–0.093)	6.91 MIN (0.272 MIN)	6.20–6.35 (0.244–0.250)



Quality and Reliability Assurance

Quality Concepts

The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, etc. However, when quality is used in the manufacturing environment, it has come to mean total quality as perceived by the customer. The simplest formulation that has been devised for total quality is:

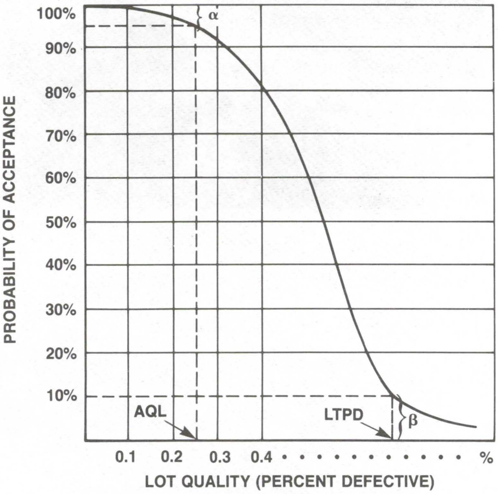
$$Q = \frac{qs}{pd}$$

Where: Q = Total Quality of a Supplier
q = Product Quality (Technical)
s = Service
p = Price Competitiveness
d = On Time Delivery

Product quality (q) of a linear integrated circuit from a product line is a measure that expresses the conformance of the device to a set of specifications. Such a measure is the percent rejects out of a collection of devices (lot, population). One hundred percent inspection has to be used to determine the actual quality of the lot. One characteristic of this approach is that it is expensive, and therefore, is used only where necessary. In addition, it may not be as accurate as it first appears because of operator errors due to fatigue and of course, it cannot be used where the inspection (test) is destructive. An alternative to 100% inspection is scientific acceptance sampling. Acceptance sampling is a method by which a portion (sample) of the total population is examined. On the basis of the sample quality (number of rejects that fail to conform to specifications out of a total sample is usually expressed in **parts per million percent rejects**) and by using the mathematics of probability and statistics, an estimate of the lot quality is made and the risk of an improper decision is specified. For example, a lot may be rejected because the sample quality was worse than that prescribed by the mathematics of sampling and our original goal (maximum percent rejects allowed in a lot). Yet, if the lot was one hundred percent inspected, we may find that the actual percent rejects in the lot was less than the maximum percent rejects established as a goal (Type I improper decision). In a similar way, the reverse may happen: a lot may be accepted on the basis of the sample quality (sample rejects are fewer than those prescribed by the mathematics of sampling and our goal) and yet, if a 100% inspection was performed, the actual percent rejects in the lot could be more than our established goal (Type II improper decision). A sampling plan is specified by the sample size and the maximum allowable defectives known as the acceptance number (ACCN).

The risks involved in sampling are described by the operating characteristic (O.C.) curve of the sampling plan. As illustrated by Figure 1, this curve shows the probability of acceptance, on the vertical axis, versus the lot quality (percent rejects), on the horizontal axis. Each particular sampling plan will have its own O.C. curve. Two points on the curve are of interest. The AQL (Acceptable Quality Level), signifies the quality level (lot quality, in percent defective) that will be accepted most of the time (usually this is set at 95%). The risk of rejecting a lot even though the lot quality is equal to or better than the AQL is called the α Risk (5% probability shown on the curve; Type I error or Producer's Risk). The other point on the curve is the LTPD (Lot Tolerance Percent Defective) which signifies the level of rejects in a lot that is unsatisfactory and should be rejected by the plan most of the time or accepted infrequently (usually set at 10% of the time). This risk of accepting a lot when it should be rejected is known as the risk of making Type II improper decision (β Risk of Consumers Risk).

FIGURE 1 — TYPICAL OPERATING CHARACTERISTIC (O.C.) CURVE



Linear integrated circuits can be produced to a variety of quality levels by combining different 100% and sample inspections and varying the criteria of acceptance and rejection. Thus, a customer can negotiate his own custom quality level if he wishes; however, this can become quite expensive in terms of time and money. That is why Motorola, in addition to the standard product level, produces Linear integrated circuits to a combination of screens which give enhanced product quality and reliability. These quality and reliability enhancement programs are the BETTER, JEDEC and JAN qualified programs and are described in this section.

Reliability Concepts

Reliability is the probability that a Linear integrated circuit will perform its specified function in a given environment for a specified period of time. In other words, reliability is quality over time and environmental conditions.

The most frequently used reliability measure for integrated circuits is the failure rate, expressed in percent per thousand hours. The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent, is called the point estimate failure rate. This, however, is a number obtained from observations from a portion (sample) of all the integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. This statement is provided by the confidence level expressed together with the failure rate. For example, a 0.1% per 1000 hours failure rate at 90% confidence level means that 90% of the integrated circuits will have a failure rate below 0.1%/1000 hours — mathematically, the failure rate at a given confidence level is obtained from the point estimate and the CHI square (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used that gives the failure rate at the confidence level desired for the number of failures and device hours under question.

It is also important to note that, as the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 device hours (FITS) or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by combining (pooling) the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an Eyring type of an equation of the form:

$$\lambda = Ae^{-\frac{\emptyset}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}} \ldots$$

Where A, B, C, Ø & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an Arrhenious type relationship of the failure rate versus the junction temperature of integrated circuits, while the causes of failure generally remain the same. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then by applying known acceleration factors, estimate the failure rates for lower junction temperatures. Figure 2 shows a curve that gives estimates of typical failure rates versus temperature for integrated circuits.

$$\text{Arrhenious type of equation: } \lambda = Ae^{-\frac{\emptyset}{KT}}$$

Where: λ = Failure Rate
A = Constant
e = 2.72
$\emptyset$ = Activation Energy
K = Botzman's Constant
T = Temperature in Degrees Kelvin

$$T_J = T_A + \theta_{JA} P_D \text{ or } T_J = T_C + \theta_{JC} P_D$$

Where: T_J = Junction Temperature
T_A = Ambient Temperature
T_C = Case Temperature
θ_{JA} = Junction to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
P_D = Power Dissipation

Failure rate curves for equipment and devices can be represented by an idealized graph called the Bathtub Curve (Figure 3).

FIGURE 2 — TYPICAL FAILURE RATE versus JUNCTION TEMPERATURE

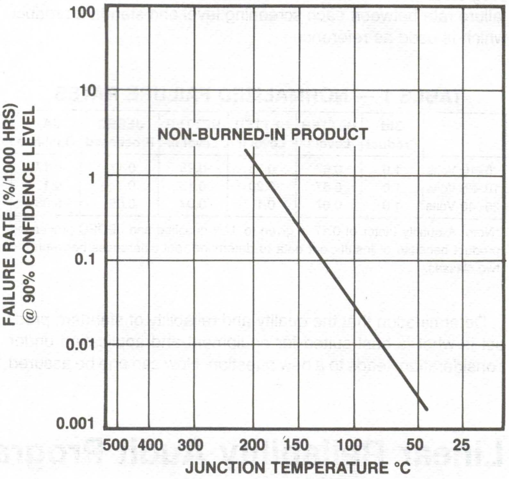
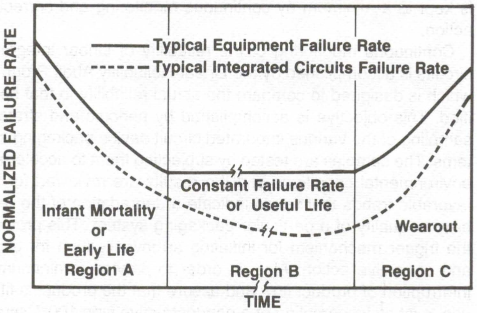


FIGURE 3 — FAILURE RATE versus TIME (BATHTUB CURVE)



There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called infant mortality or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called constant failure rate or useful life region. In the third region, the failure rate increases again and it is called wearout region. Modern integrated circuits generally do not reach the wearout portion of the curve when operated under normal use conditions. The wearout portion of the curve can be seen under highly accelerated test conditions. As a matter of fact, even their useful life portion of the curve is characterized by so few failures compared to the accumulating hours, that the useful life curve looks as a continuously decreasing curve (Figure 3). From this discussion, it becomes obvious that elimination of infant mortality is of importance.

Infant mortality in the short run is eliminated by a combination of various sample and 100% screens, with the most cost effective screen being burn-in at high temperature. These screening combinations form the various product enhancement programs such as the BETTER, JEDEC and JAN qualified, described in this section.

The most frequently asked question is which enhancement program do I need, if any at all, especially with the improvement of quality and reliability that has been achieved in integrated circuits over the last few years? The answer to this question is not simple and it depends on a number of factors such as the number of integrated circuits that will be used in a single piece of equipment, the maturity of this equipment, the environment in which the equipment will operate, the impact of a failure (safety versus entertainment), maintenance costs, etc. This question is best answered during customer-vendor interfacing, because of its' complexity and proprietary nature.

In order to obtain a feel for the effectiveness of the various programs, we will look at them on the basis of the normalized failure rate between each screening level and standard product which is used as reference.

TABLE 1 — NORMALIZED FAILURE RATES

	Std Product	BETTER Level I	BETTER Level II	BETTER Level III	JEDEC Processed	JAN Qualified
5–10 Volts	1.0	0.67	0.33	0.25	0.17*	0.17*
10–25 Volts	1.0	0.67	0.20	0.15	0.1	0.1
25–40 Volts	1.0	0.67	0.1	0.07	0.05	0.05

*Note: A quality factor of 0.17 is given to JAN qualified and JEDEC processed product because of insufficient data to determine real differences between the two classes.

Determination that the quality and reliability of standard product is what is best suited for equipment and application under consideration, leads to a new question. How can one be assured that the reliability of standard product does not degrade over time? This is accomplished by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems known as reliability auditing. A description of this program is given later in this section.

Finally, a frequently asked question is about the reliability differences between plastic versus hermetic packaged integrated circuits. In general, for all bipolar integrated circuits including Linear, the field removal rates for plastic and hermetic ICs are the same for environments where there is not high humidity. In cases where the environment contains high humidity (such as under biased 85°C and 85% humidity), higher failure rates are to be expected from plastic encapsulated devices. The determination of the best packaging system for a given application depends on many factors, one of which is protection of the equipment from hostile environments. For example, some users have reported favorable results with plastic integrated circuits, even in relatively high humidity environments (coastal areas), by properly coating (good adherence, no contaminants) the boards containing the integrated circuits with protective materials.

Linear Reliability Audit Program

The reliability of a product is a function of design and manufacturing. Inherent reliability is the reliability that a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to the actual reliability of the product. The difference between inherent reliability and actual reliability is kept to a minimum by continuous monitoring and corrective action.

Continuous monitoring of the reliability of Linear integrated circuits is accomplished by the Linear Reliability Audit Program, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for cause and corrective action. Also, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a nondestructive type 100% screen is used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The Bipolar Integrated Circuits Group has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), RRAP (Rapid Reliability Assessment Program), and RAP (Reliability Audit Program).

Currently, the Linear Reliability Audit Program consists of a Weekly Reliability Audit and a Quarterly Reliability Audit. The Weekly Reliability Audit consists of rapid (short time) type of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites and at the U.S. Linear Division Center. It provides data for use as an early warning system for identifying negative trends and triggering investigations for causes and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at the U.S. Linear Division Center. The data obtained from the Quarterly Reliability Audits is used to assure that the correlation between the short term weekly tests and long term quarterly type of tests has not changed, nor a new failure mechanism has appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rate and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Linear Reliability Audit Program provides the system of monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by the U.S. Linear Division Center, plus each assembly/test site which has the capability of assembling the Linear integrated circuits, performing final electrical testing, quality assurance electrical acceptance testing, reliability assurance testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The experimental test plan is as follows:

Electrical Measuremenns: Performed initially and after each reliability test, consists of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per the MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0eV activation energy and the Arrhenious equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to 150°C or −40°C to 125°C (JEDEC-STD-22-A104), minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is 48 hours.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environmental type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Linear Reliability Audit Program is performed at the U.S. Linear Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard dc and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0eV activation energy and the Arrhenious equation.

Approximate Acceleration Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to 150°C or −40°C to 125°C (JEDEC-STD-22-A104) for 100 and 1000 cycles. Temperature Cycling and Thermal Shock are used interchangeably.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is for 96 hours, with a 48 hours interim readout.

Pressure Temperature Humidity Bias (Biased Autoclave): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied. Temperature is 121°C, steam environment and 15psig. Duration is for 32 hours, with a 16 hour interim readout. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electric field and packaging system.

Temperature, Humidity & Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH and bias) and the 30°C, 90% RH is typically 40–50 times, depending on the type of corrosion mechanism, electric field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environmental type test are verified and characterized electrically, then submitted for failure analysis.

Commercial Product Processing Levels

Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.

The "Better" Program

THE "BETTER" program is offered on MOS, Linear ECL, TTL, LS TTL, DTL and HTL in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING — STANDARD PRODUCT PLUS:

100% Screen	Level I "S"	Level II "D"	Level III "DS"
Temp. Cycle, 10 Cycles −65°C to +150°C	X		X
Burn-In — Mil-Std-883		X	X
Post Burn-In Electrical[1,2]		X	X
100°C Functional	X		X
DC Parameter at 25°C[1,2]	X	X	X
Tightened, QA Sample	X	X	X

1. ECL and LS TTL do functional and dc 100% at T_A Max (Levels I and III, 25°C or T_A Max optional for Level II.)
2. NMOS does functional and dc 100% at 100°C.
3. Additional standardized flows, when available, will be added as BETTER Level IV, V, etc.

"BETTER" AQL GUARANTEES

Test	Condition	AQL		
		Level I	Level II	Level III
High Temperature Functional	T_A = 100°C or T_A Max	0.061	*	0.061
DC Parametric	T_A = 25°C	0.061	0.061	0.061
DC Parametric	T_A Min, T_A Max	0.30	0.30	0.30
AC Parametric	T_A = 25°C*	0.061	0.061	0.061
Dynamic Test (Linear and NMOS)	T_A = 25°C*	0.061	0.061	0.061
External Visual and Mechnical	Major/Minor	0.061	0.061	0.061
Hermeticity (Not Applicable to Plastic Packages)	Gross/Fine	0.15	0.15	0.15

"AQL" values shown are for reference only. "LTPD" type sampling plans that are equal to or tighter than values indicated may be used. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact your nearest Motorola sales office for current values.

*Some products are also AC specified at T_A Min and T_A Max. In those instances, AQL guarantees will be per Motorola standard. The AQL guarantee for Functional on "LEVEL II" processing will also be per Motorola standard.

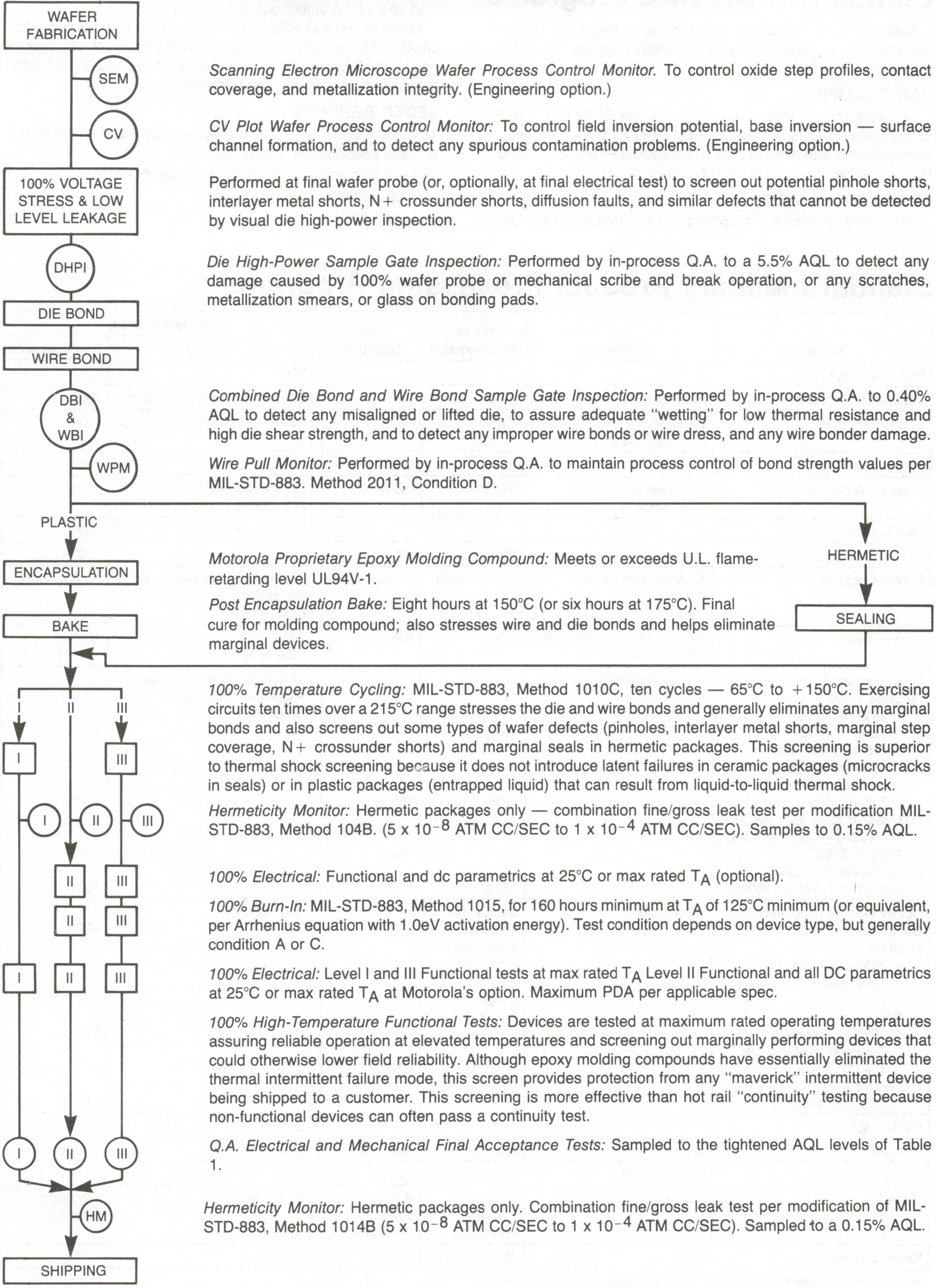
How to Order

MC34004	P	D
Part Identification	Standard Package Suffix	BETTER PROCESSING LEVEL I = SUFFIX S LEVEL II = SUFFIX D LEVEL III = SUFFIX DS

Part Marking

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

Generalized "BETTER" Product Flow for Linear



Scanning Electron Microscope Wafer Process Control Monitor. To control oxide step profiles, contact coverage, and metallization integrity. (Engineering option.)

CV Plot Wafer Process Control Monitor: To control field inversion potential, base inversion — surface channel formation, and to detect any spurious contamination problems. (Engineering option.)

Performed at final wafer probe (or, optionally, at final electrical test) to screen out potential pinhole shorts, interlayer metal shorts, N+ crossunder shorts, diffusion faults, and similar defects that cannot be detected by visual die high-power inspection.

Die High-Power Sample Gate Inspection: Performed by in-process Q.A. to a 5.5% AQL to detect any damage caused by 100% wafer probe or mechanical scribe and break operation, or any scratches, metallization smears, or glass on bonding pads.

Combined Die Bond and Wire Bond Sample Gate Inspection: Performed by in-process Q.A. to 0.40% AQL to detect any misaligned or lifted die, to assure adequate "wetting" for low thermal resistance and high die shear strength, and to detect any improper wire bonds or wire dress, and any wire bonder damage.

Wire Pull Monitor: Performed by in-process Q.A. to maintain process control of bond strength values per MIL-STD-883. Method 2011, Condition D.

Motorola Proprietary Epoxy Molding Compound: Meets or exceeds U.L. flame-retarding level UL94V-1.

Post Encapsulation Bake: Eight hours at 150°C (or six hours at 175°C). Final cure for molding compound; also stresses wire and die bonds and helps eliminate marginal devices.

100% Temperature Cycling: MIL-STD-883, Method 1010C, ten cycles — 65°C to +150°C. Exercising circuits ten times over a 215°C range stresses the die and wire bonds and generally eliminates any marginal bonds and also screens out some types of wafer defects (pinholes, interlayer metal shorts, marginal step coverage, N+ crossunder shorts) and marginal seals in hermetic packages. This screening is superior to thermal shock screening because it does not introduce latent failures in ceramic packages (microcracks in seals) or in plastic packages (entrapped liquid) that can result from liquid-to-liquid thermal shock.

Hermeticity Monitor: Hermetic packages only — combination fine/gross leak test per modification MIL-STD-883, Method 104B. (5 x 10^{-8} ATM CC/SEC to 1 x 10^{-4} ATM CC/SEC). Samples to 0.15% AQL.

100% Electrical: Functional and dc parametrics at 25°C or max rated T_A (optional).

100% Burn-In: MIL-STD-883, Method 1015, for 160 hours minimum at T_A of 125°C minimum (or equivalent, per Arrhenius equation with 1.0eV activation energy). Test condition depends on device type, but generally condition A or C.

100% Electrical: Level I and III Functional tests at max rated T_A Level II Functional and all DC parametrics at 25°C or max rated T_A at Motorola's option. Maximum PDA per applicable spec.

100% High-Temperature Functional Tests: Devices are tested at maximum rated operating temperatures assuring reliable operation at elevated temperatures and screening out marginally performing devices that could otherwise lower field reliability. Although epoxy molding compounds have essentially eliminated the thermal intermittent failure mode, this screen provides protection from any "maverick" intermittent device being shipped to a customer. This screening is more effective than hot rail "continuity" testing because non-functional devices can often pass a continuity test.

Q.A. Electrical and Mechanical Final Acceptance Tests: Sampled to the tightened AQL levels of Table 1.

Hermeticity Monitor: Hermetic packages only. Combination fine/gross leak test per modification of MIL-STD-883, Method 1014B (5 x 10^{-8} ATM CC/SEC to 1 x 10^{-4} ATM CC/SEC). Sampled to a 0.15% AQL.

Standard HIGH REL Programs

Motorola, a pioneer in the manufacture of *high-reliability* integrated circuits, now offers you a two-way program for Hi Rel products.

JAN-QUALIFIED

Motorola stocks many circuits which meet JAN-QUALIFIED specifications, and is actively pursuing an expansion of this qualification listing with product in all IC categories — encompassing Bipolar Digital, Linear and MOS technologies.

JEDEC PROCESSED

An extensive program supplying JEDEC PROCESSED devices approach Qualified Reliability goals without the delay and high cost of the actual qualification program.

Motorola JEDEC PROCESSED products complement JAN-QUALIFIED products by making available hi-rel versions of nearly all Motorola full-temperature range circuits, while adding the advantage of hi-rel standardization.

JEDEC BENEFITS

1. Standardization of environmental and electrical test procedures.
2. Less specification writing required.
3. Less time required in negotiating specifications.
4. Fast delivery.
5. Lower costs.

Standard Military Product Processing Programs

Screen	Method	JEDEC Requirements	JAN Qualified	Motorola 883 S	
				Method	Requirements
Wafer Acceptance				5007	
Internal Visual (Precap)	2010 Condition B and 38510	100%	100%	2010 Condition A and 38510	100%
Stabilization Bake	1008, 24 Hrs. Test Condition C or Equivalent	100%	100%	1008 24 Hrs. min Condition C	100%
Temperature Cycling	1010 Condition C	100%	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E min in Y_1 plane	100%	100%	2001 Condition E min in Y_1 plane	100%
Pind Testing				2020 Ceramic Pkgs.	100%
Seal Fine & Gross	1014	100%	100%	1014	100%
Interim Electrical	As Applicable Device Note 1	As Applicable	As Applicable	JAN slash sheet elec. spec. Serialization R&R. Variable data. Note 1	As Applicable
Burn-In Test	1015 @ 125°C or Equivalent PDA = 10%	100%	100%	1015 125°C min 240 Hrs. PDA = 5%	100%
Final Electrical Tests (a) Static Tests	Per Applicable Device Specification			JAN slash sheet elec. spec. Read and Record 25°C Note 1	
1. 25°C (Subgroup 1, Table 1, 5005)		100%	100%		100%
2. Max and min rated operating temperature (Subgroups 2 and 3 Table 1, 5005)		100%	100%		100%
(b) Dynamic Tests and Switching Tests 25°C (Subgroup 4 and 9 Table 1, 5005)		100%	100%		100%
(c) Functional Test 25°C (Subgroup 7, Table 1, 5005)		100%	100%	25°C, −55°C, 125°C	100%
Quality Conformance Inspection: Group A	5005 Class B	Sample per Applicable Specification (Provision) Equal to or tighter than 883	LTPD	5005 Class S	LTPD
(a) Static					
1. 25°C (Subgroup 1)			5%		3%
2. Temperature (Subgroup 2&3)			7%		5%
(b) Switching					
1. 25°C (Subgroup 9)			7%		5%
2. Temperature (Subgroup 10&11)			10%		
(c) Functional					
1. 25°C (Subgroup 7)			5%		3%
RadioGraphic				2012	100%
Group B	5005 Class B	Insp. Lot	Insp. Lot	5005 Class S	Insp. Lot
Group C	5005 Class B	52 Wks. Prod.	13 Wks. Prod.		
Group D	5005 Class B	12 Mos. Package Production	6 Mos. Package Production	5005 Class S	Generic or Insp. Lot
External Visual	2009	100%	100%	2009	100%

NOTE 1: Motorola data sheet electricals where JAN slash sheets are not available.

Ordering and Marking for Better Level Product

MC34004 — Part Identification

P — Standard Package Suffix

D — Better Processing
Level I = Suffix S
Level II = Suffix D
Level III = Suffix DS

Ordering & Marking for JEDEC Hi-Rel Processing Program

139 — **Motorola Device Type (Without letter prefix)**

/ — **Slash**

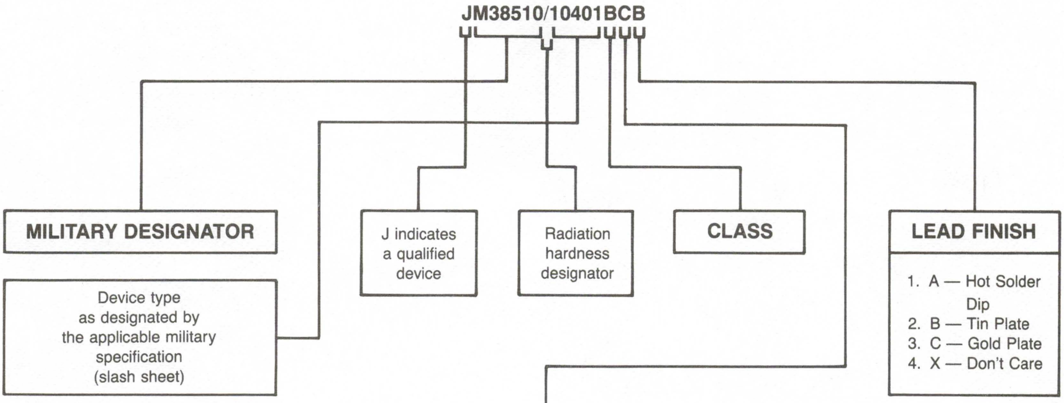
B — **Device Class (See Table)**

C — **Case Outline (Same as JAN Qualified Product, See Table Below)**

B — **Lead Finish Same as JAN Qualified Product, See Table Below**

JC — **JEDEC Designator**

Ordering & Marking for JAN Qualified Program


JM38510/10401BCB
MILITARY DESIGNATOR
Device type as designated by the applicable military specification (slash sheet)
J indicates a qualified device
Radiation hardness designator
CLASS
LEAD FINISH

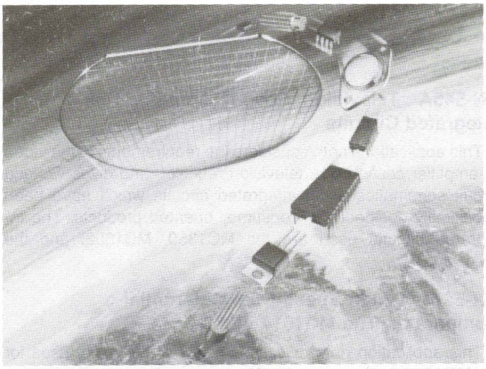
LEAD FINISH

1. A — Hot Solder Dip
2. B — Tin Plate
3. C — Gold Plate
4. X — Don't Care

CASE OUTLINE

1. A — ¼″ x ¼+ flat pack, 14-pin
2. B — 3⁄16″ x ¼″ flat pack, 14-pin
3. C — ¼″ x ¾″ dual-in-line, 14-pin
4. D — ¼″ x ⅜″ flat pack, 14-pin
5. E — ¼″ x ⅞″ dual-in-line, 16-pin
6. F — ¼″ x ⅜″ flat pack, 16-pin
7. G — 8-lead can
8. H — ¼″ x ¼″ flat pack, 10-lead
9. I — 10-lead can
10. J — ½″ x 1¼″ dual-in-line, 24-pin
11. K — ⅜″ x ⅝″ flat pack, 24-pin
12. L — ⅜″ x ½″ flat pack, 24-pin
13. M — 12-lead can
14. N — (Size *N/D) flat pack, 24-pin
15. P — ¼″ x ⅜″ dual-in-line, 8-pin
16. Q — 0.60″ x 2.00″ dual-in-line, 40-pin
17. R — ¼″ x 1 1⁄16″ dual-in-line, 20-pin
18. S — ¼″ x ½″ flat pack, 20-pin
19. T — (Size *N/D) flat pack, 22-pin
20. U — 0.40″ x 0.40″ leadless flat pack, 24-pin
21. V — 0.30″ x 1.00″ dual-in-line, 18-pin
22. W — 0.40″ x 1.10″ dual-in-line, 22-pin
23. X
24. Y Variable per applicable slash sheet
25. Z

*N/D — NOT DEFINED



Applications Literature

14

Applications Literature

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the publication number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

Application Note Abstracts

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including dc characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications Using The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators/demodulators for AM, SSB, and suppressed carrier AM; frequency doublers and HF/VHF double balanced mixers.

AN-543A Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545A Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.

AN-547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multivibrators, and peak level detectors are presented.

AN-587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN-599 Mounting Techniques for Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

AN-702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN-703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

AN-708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

AN-713 Binary D/A Converters can Provide BCD-Coded Conversion

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

APPLICATIONS LITERATURE (continued)

AN-714 A Personalized Heart-Rate Monitor with Digital Readout

Using the micropower operational amplifier MC1776 and CMOS digital integrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-716 Successive Approximation A/D Conversion

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

An-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-720 Interfacing with MECL 10,000

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as input impedance, output drive, gain and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling of non-compatible signals.

AN-727 Television Horizontal APC/AFC Loops: The Last 10 Percent

A discussion of some common problems that may be encountered with the design of Horizontal APC/AFC loops and methods to avoid or overcome them.

AN-737A Switched Mode Power Supplies — Highlighting A 5.0-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in ac to dc power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5.0-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3.0-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a feroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-760 Application of The MC3416 Crosspoint Switch

The operation and application of the MC3416 4 x 4 balanced crosspoint switch is described in detail. Special emphasis is given to balanced switching systems like those in space division PABX. Discussion of the total system design using the MC3416 is also included.

AN-767 A Line Operated, Regulated 5.0 V/50 A Switching Power Supply

This application note describes a regulated 220 Vac to 5.0 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

AN-775 M6800 Systems Utilizing the MC6875 Clock Generator/Driver

This application note describes the use of the MC6875 clock generator/driver in M6800 based systems. Design examples will demonstrate the capabilities of the driver in systems using slow and/or dynamic memories. Multiprocessing and DMA methods are also covered.

AN-778 Mounting Techniques for Power Semiconductors

For reliable operation, semiconductors must be properly mounted. Discussed are aspects of preparing the mounting surface, using thermal compounds, insulation techniques, fastening techniques, handling of leads and pins, and evaluation methods for the thermal system.

AN-781A Revised Data Interface Standards

This application note provides a brief overview and comparison of communication interface standards RS-232-C, RS-422A, RS-423, RS-449 and RS-485 for the hardware designer. A listing of the standard's specifications and appropriate Motorola devices are included.

AN-787 An M6800 Clock System That Handles DMA and Memory Refresh Cycle Stealing

Dynamic memory and three-state cycle stealing for Direct Memory Access transfers require a clock generator and priority logic to maintain proper refresh times of the dynamic MPU and dynamic memory. The design presented here demonstrates use of the MC6875 clock generator with an MC6800 MPU.

AN-829 Application of the MC1374 TV Modulator

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It's idealy suited as an output device for subscription TV decoders, video disk and video tape players.

AN-842 Microprocessor-Compatible DACs and the MC6890

As the range of applications and consequently the usage, of microprocessors steadily increases, the need for more efficient interfacing also increases. There has been developed a class of DACs which incorporate the commonly used circuits necessary for microprocessor interfacing, thus easing the design problems involved.

AN-844 Extending the Capabilities of the MC10315/MC10317 Flash A/D Converters

Recent advances in manufacturing capabilities have provided the means to produce 7-bit flash converters in monolithic form. This application note will discuss some of the means whereby the user may extend the resolution and speed of the basic devices.

AN-848 An Evaluation System for High-Speed A-D and D-A Converters

The purpose of this application note is to describe the capabilities and operation of the MC10315 and MC10317 flash A-D converter, as well as their application in an Evaluation Board designed for their use at frequencies which include video rates.

AN-877 Precision Voltage References for the MC10315/MC10317 Flash A-D Converters

In order to produce a digital representation of an analog signal, all analog-to-digital converters require a reference voltage. The digital output word is the result of a comparison of that analog voltage versus the reference voltage.

While most analog-to-digital converters have a high input impedance for the reference voltage, the MC10315/10317 flash A-D converters have a reference input resistance of (typically) 64 ohms, thus requiring a significant current be supplied from a precision source. This application note describes several circuit configurations which can be used to supply the reference voltage, and current, at the stability by the A-D converters.

AN-879 Monomax—Application of the MC13001 Monochrome Television Integrated Circuit

This application note presents a complete 12″ black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed.

AN-917 Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head as well as defined read/write signals in order to be a viable system. This application note describes the use of the MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering.

Engineering Bulletin Abstracts

EB-20 Multiplier/OP Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described by EB-20 to obtain the true rms of an input voltage ranging from 2 to 10 Vpk.

EB-51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB-51.

EB-57 An Economical FM Transmitter Voice Processor from a Single IC

An MC3401 Quad Op-Amp is used as a Microphone/Modulation interface in an FM transmitter.

EB-66A A Symmetry Correcting Circuit for Use with the MC3420

EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

EB-78 New ICs Perform Control and Ancillary Functions in High Performance Switching Supplies

This bulletin discusses the MC3420 and MC3423. The MC3420 performs a great number of functions required for the control of inverter type Switchmode power supplies. The MC3423 is for the overvoltage protection of power supplies.

EB-85A Full-Bridge Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a full-bridge-configuration supply from 500 to 1000 watts.

EB-86 Half-Bridge Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a half-bridge-configuration supply from 100 to 500 watts.

EB-87A Flyback Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a flyback-configuration supply from 100 to 250 watts.

EB-88 Push-Pull Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a push-pull-configuration supply from 100 to 500 watts.

EB-100 A Simplified Power-Supply Design Using the TL494 Control Circuit

This bulletin describes the operation and characteristics of the TL494 Switchmode Voltage Regulator and shows its application in a 400-watt off-line power supply.

TMOS Design Tip Abstracts

TDT-101B A 100 kHz FET Switcher

This note describes a circuit for a 60 W, 100 kHz FET switcher with four output voltages, operating from 120 Vac.

1 Alphanumeric Index and Cross Reference

2 Selector Guides

Integrated Circuits Data Sheets

3 Amplifiers

4 Power Supply

5 Voltage References

6 Data Conversion

7 Interface

8 Comparators

9 Telecommunications

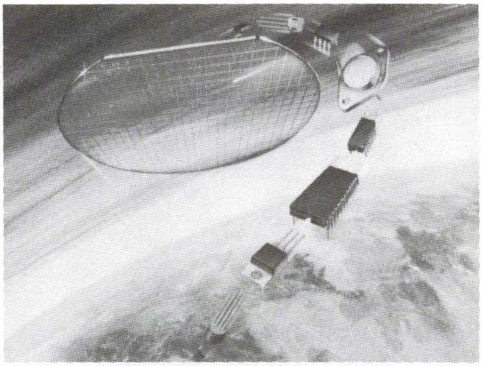
10 Consumer

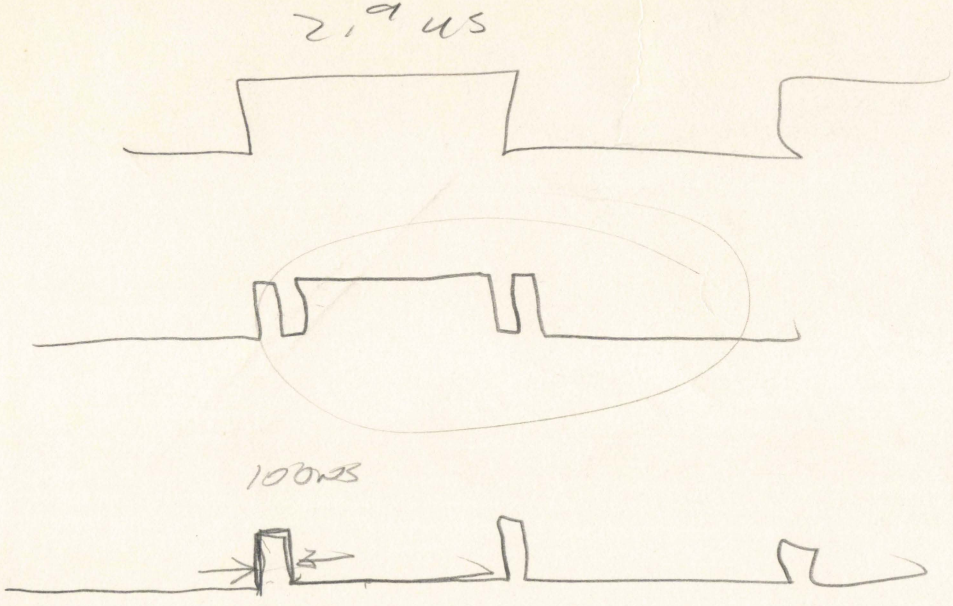
11 Other Linear

12 Packaging Information, Including Small Outline Integrated Circuits (SOIC)

13 Quality and Reliability Assurance

14 Applications Literature

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